EEE 313- Electronic Circuit Design

-Lab 03-

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Introduction

The purpose of this lab was to design a nMOS common source amplifier firstly by setting up two test circuits for finding the threshold voltage (Vth), the K_n and λ values and the I_{DS} - V_{DS} relationship of the transistor. The second part consists of setting up the amplifier circuit by finding the values of the unknown resistances and capacitor, g_m and r_o values. At the end, what is expected is to show input and output voltages on the same oscilloscope screen in order to see the amplification effect.

Theory

1. Test Circuit for finding V_{th}

The circuit design is as follows:

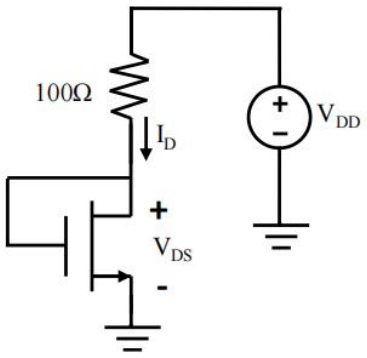

Fig.1 Test Circuit for finding V_{th}

After setting up the circuit in Fig.1, V_{DD} is increased until I_D became 30 mA. The I_D current is measured using a multimeter connected in series to the 100Ω resistor. The transistor is assumed as ON when I_D=1mA. In order to find the threshold voltage we need to find the V_{GS} value due to the condition given by (1). For this test circuit since V_{GS} = V_{DS} we can use the same relation (1) for V_{DS} as well. V_{DS} can be found by doing KVL which gives the equation (2).

$$\text{ON state condition: } V_{GS} > V_{TH} \quad (1)$$

$$V_{DS} = V_{DD} - I_D * 100\Omega \quad (2)$$

Since the transistor is assumed ON when I_D=1mA, when the I_D value read on the multimeter becomes 1 mA, the corresponding V_{DS} voltage is hence equal to the V_{TH}. The results are as follows:

- V_{DD} = 2.13 V when I_D=1mA
- V_{TH} = 2.13- $100*10^{-3}$ = 2.03V

For the plotting part, V_{DD} value is increased until I_D becomes 30 mA and the corresponding I_D versus V_{DS} curve is obtained:

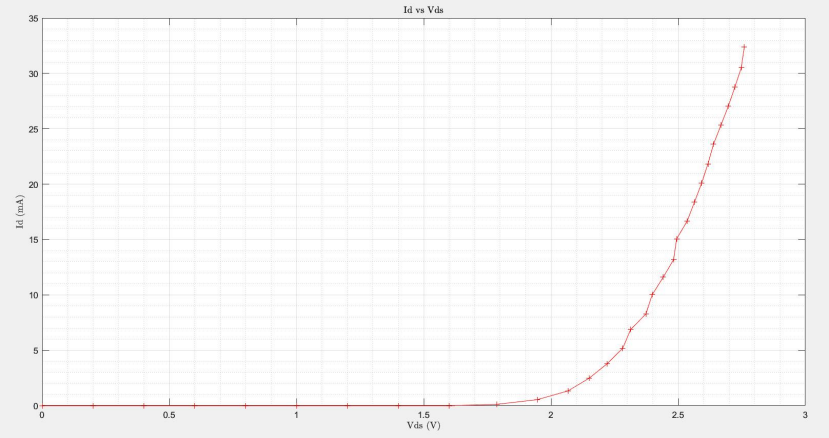

Fig.2. I_D-V_{DS} curve for part 1 test circuit

This biasing circuit, due to the equality between V_{GS} and V_{DS}, allows us to find the threshold voltage by changing the V_{DD}.

2. Test Circuit to Plot I_D-V_{DS} Curves

For this part the following circuit design is used:

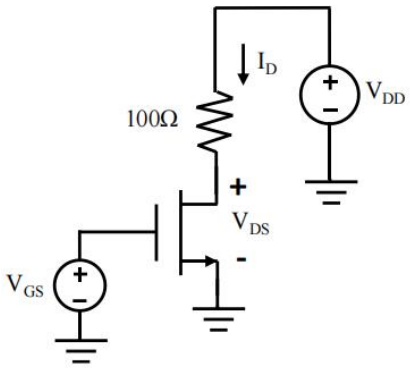

Fig.3. Test Circuit to Plot I_D-V_{DS} Curves

The V_{GS} value is sweep fixed and the V_{DD} value is slowly changed while recording the I_D. 3 I_D versus V_{DS} curves are plotted for different V_{GS} values. For finding the V_{DS}, same relation (2) stated in part 1. is used. The corresponding plots can be seen below.

- When $V_{GS} = V_{TH} + 0.3V = 2.33V$:

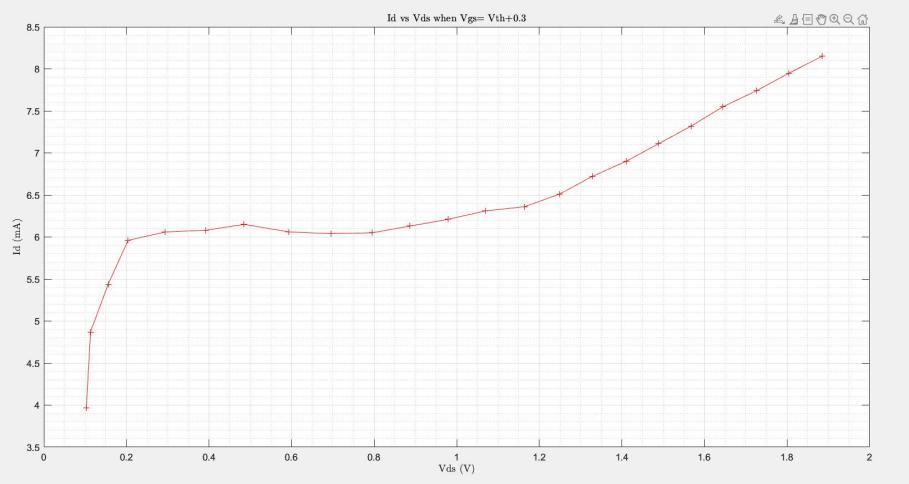

Fig.4. Plot of I_D-V_{DS} when V_{GS}=2.33V

- When $V_{GS} = V_{TH} + 0.4V = 2.43V$:

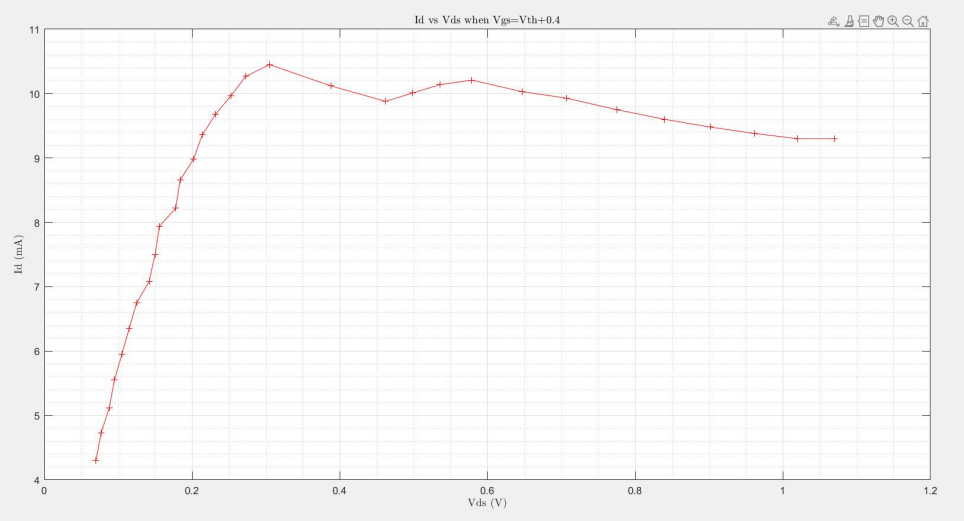

Fig.5. Plot of I_D-V_{DS} when V_{GS}=2.43V

- When $V_{GS} = V_{TH} + 0.5V = 2.53V$:

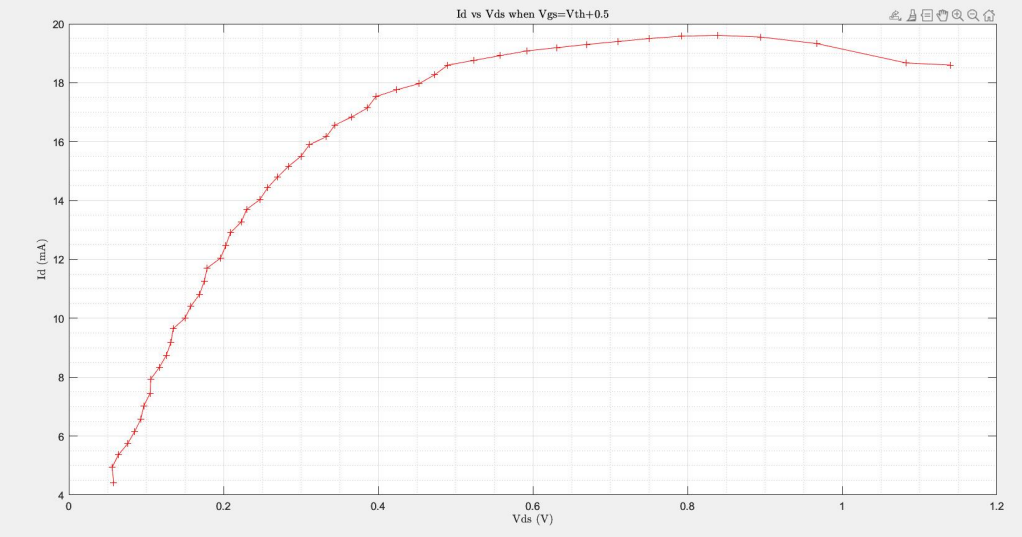

Fig.6. Plot of I_D-V_{DS} when V_{GS}=2.53V

In the ideal case, when the transistor is operating in the SAT region the drain current I_D is independent from V_{DS} value hence after saturation even though the drain voltage increases, the drain to source current becomes stabilized creating a I_D-V_{DS} curve with slope equal to zero. However in real life conditions there exist a nonzero slope, hence the increase in the drain voltage effects the drain to source current. This event decreases the effective channel length and causes the phenomenon called channel length modulation [1]. For a non-ideal n-channel device, the I_D versus V_{DS} characteristics in SAT region with nonzero slope is given in eq.(3).

$$I_D = K_n[(V_{GS} - V_{TH})^2(1 + \lambda V_{DS})] \qquad (3)$$

Where
-Kn is the transconduction or simply conduction parameter which is a device specific function of both the electrical (oxide permittivity and thickness, mobility of the electrons) and geometric (width and length) parameters[1].
-λ is a positive parameter called the length modulation parameter.

The effect of channel length modulation produce a finite output resistance named r_0. The plot for I_D versus V_{DS} curve for different V_{GS} values is shown in Fig.6.

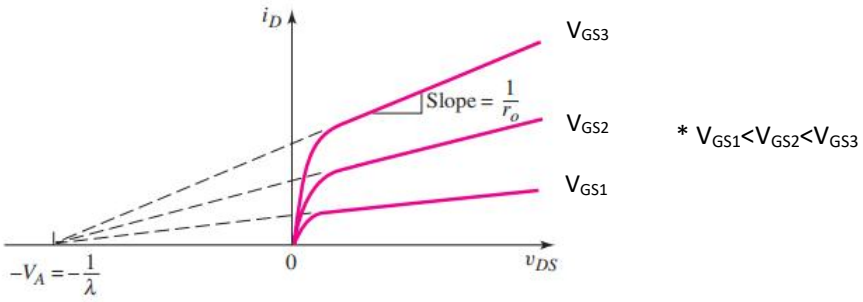

Fig.7. The effect of channel length modulation on I_D-V_{DS} relationship

From Fig.7. we can see that the Q point shifts towards left and up meaning that the corresponding I_D value increases for larger values of V_{GS}. When we compare the experimental plots in Figs. 4,5,6. it can be seen that for a specific V_{DS} value the corresponding drain current is smallest when V_{GS} =2.33V and largest when V_{GS} =2.53V which is consistent with the theory.

For K_n and λ calculations the plot in Fig.6 is used when V_{GS} =2.53V. Two value from the SAT region is taken as shown in Fig.8. Expressing the chosen values as (V_{DS1},I_{D1}),(V_{DS2},I_{D2}) and placing them in eq.3. with V_{GS}-V_{TH}=0.5 we get:

$$I_{D1} = K_n[(0.5)^2(1 + \lambda V_{DS1})] \qquad (4)$$

$$I_{D2} = K_n[(0.5)^2(1 + \lambda V_{DS2})] \qquad (5)$$

Taking the ratio, λ is found as:

$$\lambda = \frac{I_{D2} - I_{D1}}{(I_{D1}V_{DS2} - I_{D2}V_{DS1})} \qquad (6)$$

Placing the chosen values into their places λ is calculated as 0.039 V^{-1}. Placing λ in one of the equations K_n is then calculated as 75.98 mA/V^2.

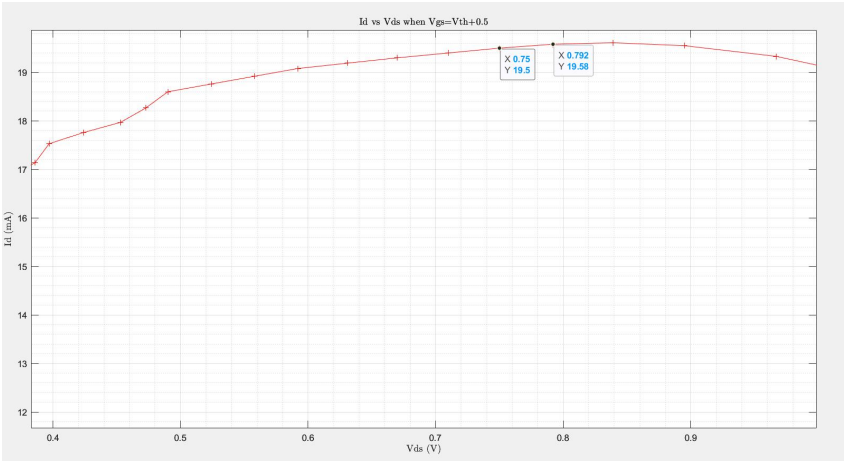

Fig.8. Values chosen for K_n & λ calculations

3. Common Source Amplifier

The common source amplifier design for this part is shown in Fig.9.

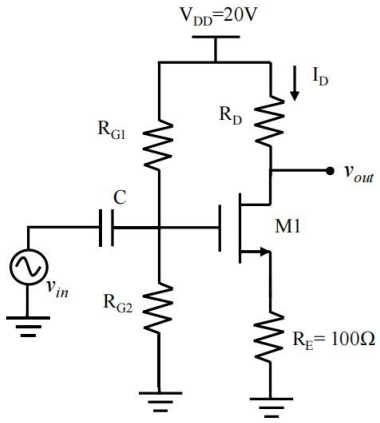

Fig.9. Common source amplifier design

The circuit specifications are as follows.

- R_{in} >30 K
- R_{out} < 2K
- 10 mA < I_D< 15 mA
- |Av|> 9 when V_{in} = 0.1sin(10KHz*t)

<u>R_o and Gm Calculations</u>

Moving to the gm and r_o calculations, from eq (3) we know that:

$$\frac{1}{r_o} = \frac{\partial i_D}{\partial v_{DS}} = \lambda K_n (V_{GS} - V_{TN})^2 \quad (7)$$

From (7) r_o is calculated as

$$r_o = \frac{1}{\lambda I_{DQ}} = 1.34K\Omega \quad (8)$$

The small signal amplifier circuit consists of DC and AC gate to source currents. By internalization we can separate the two and apply superposition. Hence the total instantaneous current (i_D) has two components: quiescent drain current I_{DQ} & small signal current i_d

$$i_D = I_{DQ} + i_d \quad (9)$$

The small signal AC current is given by

$$i_d = 2K_n(V_{GS} - V_{TN})v_{gs} \qquad (10)$$

From (9) the transconductance parameter gm is found as

$$gm = 2K_n(V_{GS} - V_{TN}) = 75.98\Omega^{-1} \quad (11)$$

Resistor, Capacitor & Gain Calculations

Continuing with the resistor and capacitor calculations firstly the small signal model of the circuit should be drawn (Fig.10).

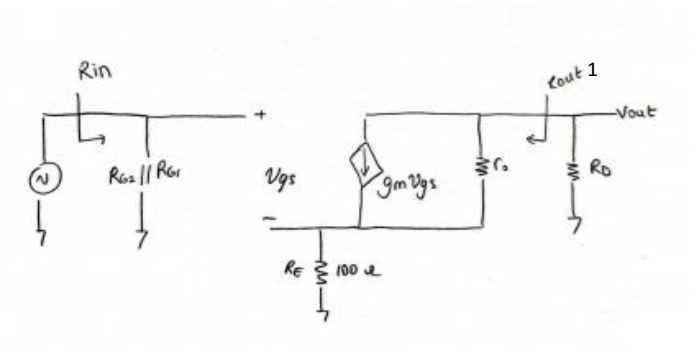

Fig.10. Small Signal model of the circuit

$$R_{in} = R_{G1} // R_{G2} > 30k\Omega$$
$$R_{out} = R_{out1} // R_D < 2k\Omega \qquad (12)$$

Using the conditions in (12) R_{G1} and R_{G2} are chosen as 330K and 39K respectively. However the gain with these values was lower than 9 hence R_{G1} is replaced with 180K. The reason for this is explained later in this report.

For R_D, firstly R_{out1} is needed to be calculated, hence the analysis in Fig.11 is made. Using (12) calculated R_{out1} and R_{out} are used for choosing an R_D within the given specifications. For the choosing process a more experimental path is followed. I started with 1.2K and increased R_D up to 1.8K for the correct gain.

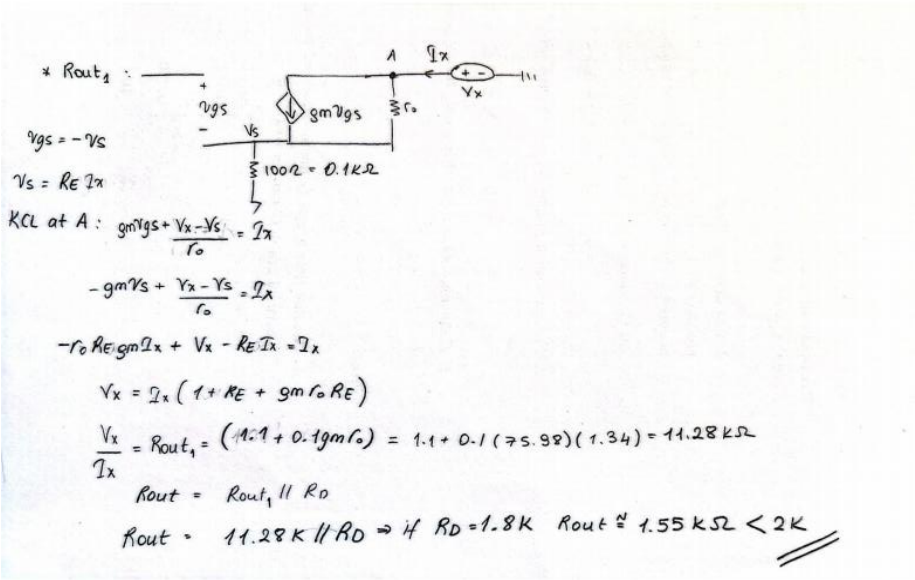

Fig.11. R_D, R_{out1},R_{out} calculations

For all the resistor values, after finding a convenient interval meeting the lab conditions, the values are changed by trial and error for achieving a gain larger than 9. How to change the values depends on how each component effects the gain. Hence the following calculations are made.

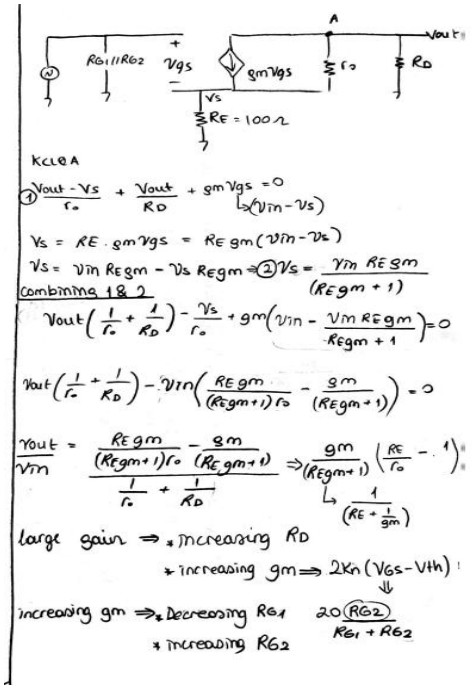

Fig.12. Gain Calculation

Therefore considering the gain relationship and experimental results the resistor values are chosen as:

- R_{G1} = 180K
- R_{G2} = 39K
- R_D= 1.8K

For the capacitance value, the magnitude of the capacitor impedance (eq.13) should be less than the thevenin resistance between the capacitor terminals in order to have a short circuit [1].

$$|Z_c| = \frac{1}{2\pi f C_c} \quad (13)$$

For small impedance the capacitance value should be large. If it is chosen as 100μF, this condition is satisfied. The 100μF is found by trial and error in the experimental part. The coupling capacitor here helps to separate the DC and Ac voltages by acting as a short circuit for AC and open circuit for DC.

Saturation Check

In order to make sure that the chosen value satisfy the saturation the following calculations are made. If the drain current is 10 mA, the transistor is in the Sat region with the chosen values.

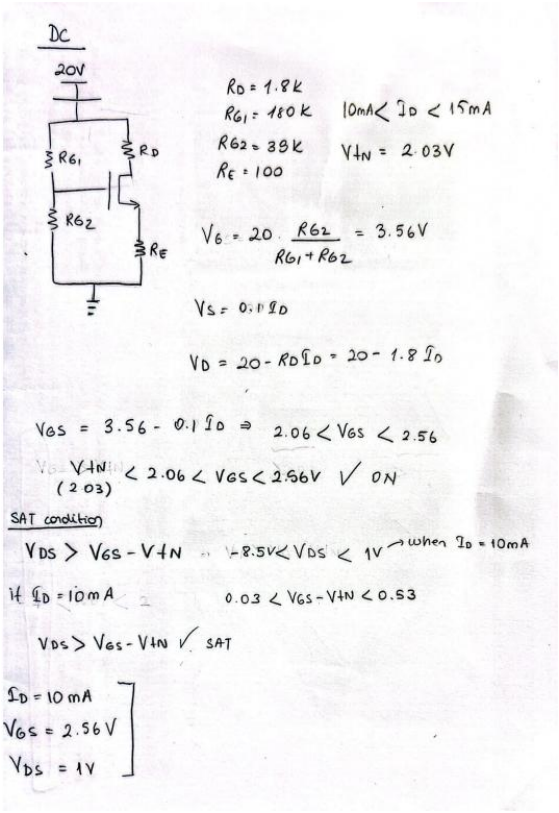

Fig.13. Saturation Check

Hardware Implementation

Gain

Fig.14 shows the common source amplifier circuit.

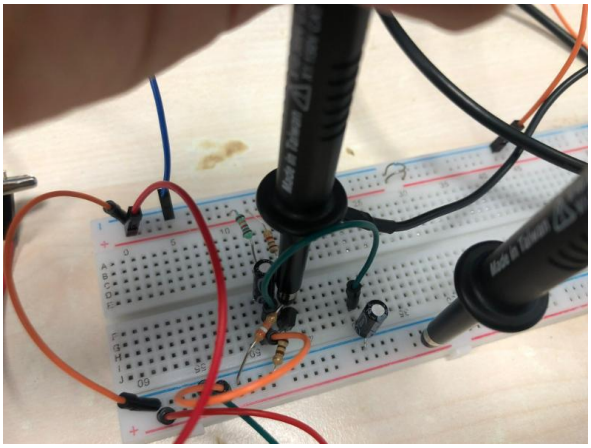

Fig.14. Common Source Amplifier

The input and output voltages are measured at the same time for seeing the amplification effect. Normally due to the internal resistance of the source generator, instead of $100mV_{pp}sin(10KHz*t)$, $50mV_{pp}sin(10KHz*t)$ should be applied for seeing the $100MV_{pp}$ at the load resistance. However the pictures that I have taken shows the results for $100mV_{pp}sin(10KHz*t)$ applied input which results in $200mV_{pp}$. This is an error that I have made and I didn't had time to retake the pictures. Nevertheless, the gain is still the same hence for the gain measurement they are still valid.

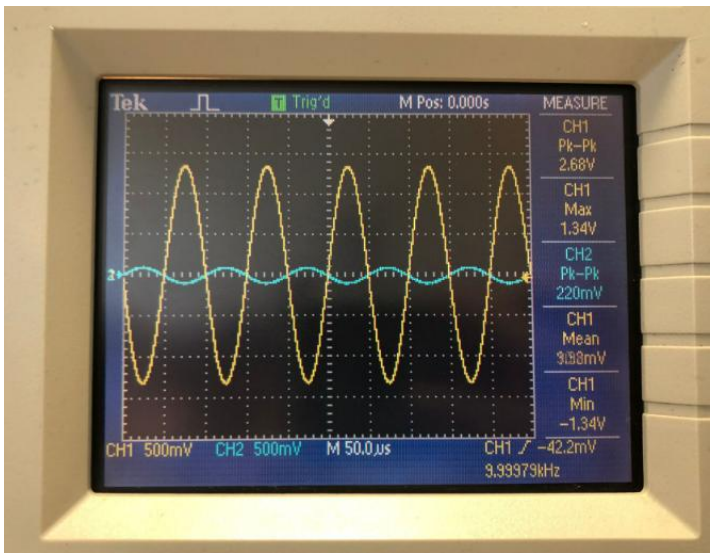

Fig.15. Input (Blue) & Output (Yellow) signals

As can be seen from fig.15. the gain of the amplifier $Av = |\frac{Vout}{Vin}| = \frac{2.68}{0.2} = 13.4 > 9$.

Moving to the distortion effect, if the input signal is increased up to a point where the sinusoidal fluctuations pass beyond the linear region, that is the saturation limits, distortion starts to occur. And the output waves seem like cut off sine waves. When the input V_{pp} is increased up to 0.5 V resulting 1V read on the load seen from the signal generator, that is to say when $1V_{pp}sin(10KHz*t)$ is applied, the distortion started to occur as seen in Fig.16.

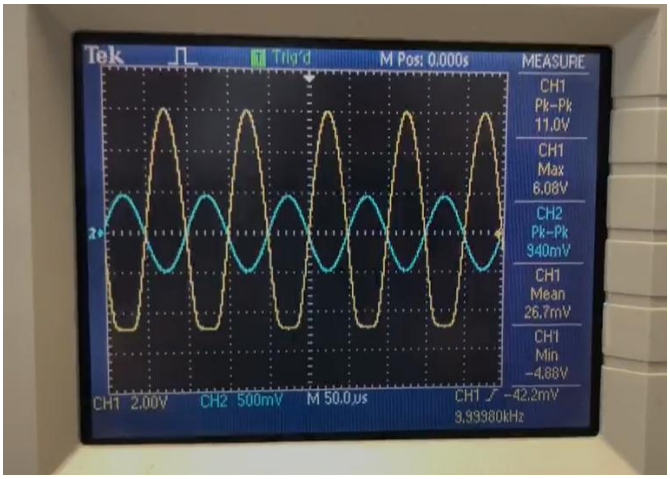

Fig.16. Distorted Output Signal

Adding a Capacitor Parallel to R_E

Since the capacitor acts as short circuit for AC inputs, the gate resistance becomes shorted with the added capacitor as shown in Fig.17.

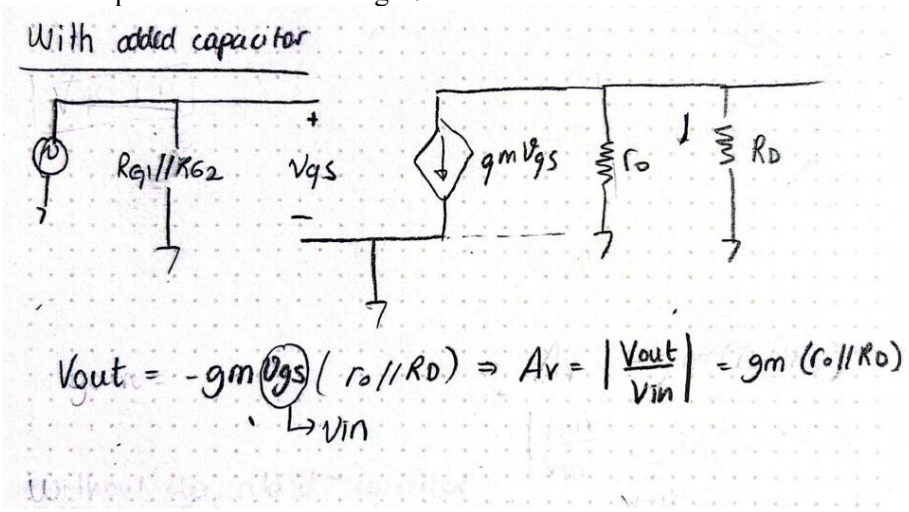

Fig.17. Gain with the added capacitor

From the calculated gm, r_o and R_D values the gain can be calculated as

$$Av = \left|\frac{Vout}{Vin}\right| = 58.36$$

Which is way more larger than with the R_E case. Fig.18. shows the real life implementation results of the capacitor.

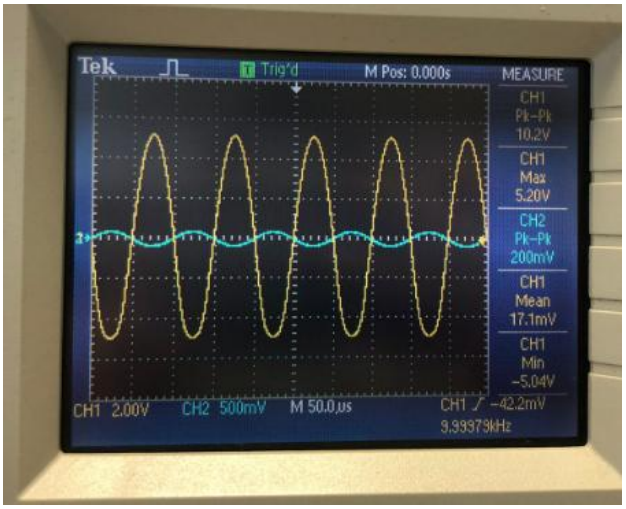

Fig.18. Input (Blue) & Output (Yellow) signals without R_E

The experimental gain is: Av = $|\frac{Vout}{Vin}| = \frac{10.2}{0.2} = 51$ which is even if lower than the expected value enough to show the increase in the gain with the added capacitor.

Conclusion

This lab was very useful for understanding the DC and AC analysis of MOSFET amplifiers. The first two parts was for understanding the general characteristics of the transistor such as threshold voltage, I_D-V_{DS} characteristics, K_n,λ, gm and r_o values. The most challenging part was definitely the I_D-V_{DS} plots. It took so long to get the correct data points and even though I tried to obtain plots close to ideal case some plots did not turn out as nice as expected. Due to the variations in plots calculations of K_n,λ was also hard as well. Choosing the suitable two points was crucial for this part. Depending on the chosen points the results were changing a lot. For the amplifier part, I learned how to decide on the values of different parameters without surpassing the required specifications. The analysis of the circuit helped me a lot while deciding on the resistor values. Being able to see how each component effects the gain is an important skill to have. Maintaining the SAT state was also important, I saw that even though in the small signal analysis the DC part is kept ignored you also have to think about the changes in the DC analysis as well. The distortion was one of the examples, it seems like the input voltage can be increased as much as wanted in the AC analysis however I saw that this is not the case. Lastly the added capacitor showed that the gain can be increased drastically however since in that case gm directly affects the gain, changes in the current can indirectly modify the gain. Which is not a desired case considering the stability of the amplifier.

References

[1] D. Neaman, *Microelectronics Circuit Analysis and Design*. McGraw-Hill Science Engineering, 2007.

Appendix

Vth calculation

```
Vdd= [0:0.2:6];
Ids=[0 0 0 0 0 0 0 0 0 0.12 0.54 1.33 2.49 3.79 5.18 6.87 8.27 10.02 11.59
13.18 15.06 16.65 18.36 20.08 21.83 23.61 25.32 27.03 28.77 30.52 32.40];
Vds= Vdd- 0.1*Ids
figure
plot (Vds,Ids,'r-+');
ylabel ({'Id (mA)'},'Interpreter','latex');
xlabel ({'Vds (V)'},'Interpreter','latex');
box on
grid, grid minor
title({'Id vs Vds'},'Interpreter','latex')

%Vth
Vth=2.13- 100*(10^-3) % 2.03V
```

I_D-V_{DS} plots for different V_{GS} values

```
%Part 2
%1) Vgs=2.33V:
Vdd= [0.5:0.1:2.7]
Id=[3.97 4.87 5.44 5.96 6.06 6.08 6.15 6.06 6.04 6.05 6.13 6.21 6.31 6.36
6.51 6.72 6.90 7.11 7.32 7.55 7.74 7.95 8.15]

%8.90 9.09 9.51 9.93 10.45 10.93 11.40 11.87 12.33 12.79 13.24 13.73 14.16
14.68 15.16 15.63 16.49 16.99 17.50 18.06 18.57 19.04 19.59 20.2];
Vds= Vdd- 0.1*Id
figure
plot (Vds,Id,'r-+');
ylabel ({'Id (mA)'},'Interpreter','latex');
xlabel ({'Vds (V)'},'Interpreter','latex');
box on
grid, grid minor
title({'Id vs Vds when Vgs= Vth+0.3'},'Interpreter','latex')
%%
%2) Vgs=2.43V:
Vdd= [0.5:0.1:4]
Id=[4.35 5.15 5.97 6.77 7.55 8.27 9.00 9.68 10.31 10.26 9.99 10.09 9.66
9.33 9.10 9.00 8.99 9.03 9.10 9.24 9.40 9.57 9.76 9.94 10.15 10.33 10.58
10.82 11.02 11.26 11.51 11.75 11.95 12.20 12.45 12.70]

%8.90 9.09 9.51 9.93 10.45 10.93 11.40 11.87 12.33 12.79 13.24 13.73 14.16
14.68 15.16 15.63 16.49 16.99 17.50 18.06 18.57 19.04 19.59 20.2];
Vds= Vdd- 0.1*Id
figure

plot (Vds,Id,'r-+');
ylabel ({'Id (mA)'},'Interpreter','latex');
xlabel ({'Vds (V)'},'Interpreter','latex');
box on
grid, grid minor
title({'Id vs Vds when Vgs=Vth+0.4'},'Interpreter','latex')


Vdd1= [0.5:0.05:2]
```

```
Id=[4.30 4.73 5.12 5.55 5.95 6.35 6.75 7.08 7.50 7.94 8.22 8.66 8.98 9.36
9.68 9.97 10.27 10.45 10.12 9.88 10.01 10.14 10.21 10.03 9.93 9.75 9.60
9.48 9.38 9.30 9.30]

%8.90 9.09 9.51 9.93 10.45 10.93 11.40 11.87 12.33 12.79 13.24 13.73 14.16
14.68 15.16 15.63 16.49 16.99 17.50 18.06 18.57 19.04 19.59 20.2];
Vds= Vdd1- 0.1*Id
figure

plot (Vds,Id,'r-+');
ylabel ({'Id (mA)'},'Interpreter','latex');
xlabel ({'Vds (V)'},'Interpreter','latex');
box on
grid, grid minor
title({'Id vs Vds when Vgs=Vth+0.4'},'Interpreter','latex')


%%
%2) Vgs=2.53V:
Vdd= [0.5:0.2:4.1]
Id=[4.41 6.15 7.93 9.63 11.27 12.85 14.47 15.90 16.03 15.77 14.96 13.69
13.23 12.98 13.11 13.34 13.70 14.07 14.54]

%8.90 9.09 9.51 9.93 10.45 10.93 11.40 11.87 12.33 12.79 13.24 13.73 14.16
14.68 15.16 15.63 16.49 16.99 17.50 18.06 18.57 19.04 19.59 20.2];
Vds= Vdd- 0.1*Id
figure
plot (Vds,Id,'r-+');
ylabel ({'Id (mA)'},'Interpreter','latex');
xlabel ({'Vds (V)'},'Interpreter','latex');
box on
grid, grid minor
title({'Id vs Vds when Vgs=Vth+0.5'},'Interpreter','latex')


Vdd1= [0.5:0.05:3]
Id=[4.42 4.94 5.36 5.74 6.15 6.57 7.03 7.45 7.94 8.33 8.74 9.18 9.65 10.00
10.42 10.81 11.25 11.71 12.04 12.47 12.91 13.27 13.70 14.03 14.43 14.80
15.16 15.50 15.89 16.17 16.56 16.84 17.14 17.53 17.76 17.97 18.27 18.60
18.76 18.92 19.08 19.19 19.30 19.40 19.50 19.58 19.61 19.55 19.33 18.67
18.60]

%8.90 9.09 9.51 9.93 10.45 10.93 11.40 11.87 12.33 12.79 13.24 13.73 14.16
14.68 15.16 15.63 16.49 16.99 17.50 18.06 18.57 19.04 19.59 20.2];
Vds= Vdd1- 0.1*Id
figure

plot (Vds,Id,'r-+');
ylabel ({'Id (mA)'},'Interpreter','latex');
xlabel ({'Vds (V)'},'Interpreter','latex');
box on
grid, grid minor
title({'Id vs Vds when Vgs=Vth+0.5'},'Interpreter','latex')
```