IPC-6012E

2020 - March

Qualification and Performance Specification for Rigid Printed Boards

Supersedes IPC-6012D
September 2015

An international standard developed by IPC

Association Connecting Electronics Industries

The Principles of Standardization

In May 1995 the IPC's Technical Activities Executive Committee (TAEC) adopted Principles of Standardization as a guiding principle of IPC's standardization efforts.

Standards Should:

- Show relationship to Design for Manufacturability (DFM) and Design for the Environment (DFE)
- Minimize time to market
- Contain simple (simplified) language
- Just include spec information
- Focus on end product performance
- Include a feedback system on use and problems for future improvement

Standards Should Not:

- Inhibit innovation
- Increase time-to-market
- Keep people out
- Increase cycle time
- Tell you how to make something
- Contain anything that cannot be defended with data

Notice

IPC Standards and Publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for his particular need. Existence of such Standards and Publications shall not in any respect preclude any member or nonmember of IPC from manufacturing or selling products not conforming to such Standards and Publication, nor shall the existence of such Standards and Publications preclude their voluntary use by those other than IPC members, whether the standard is to be used either domestically or internationally.

Recommended Standards and Publications are adopted by IPC without regard to whether their adoption may involve patents on articles, materials, or processes. By such action, IPC does not assume any liability to any patent owner, nor do they assume any obligation whatever to parties adopting the Recommended Standard or Publication. Users are also wholly responsible for protecting themselves against all claims of liabilities for patent infringement.

IPC Position Statement on Specification Revision Change

It is the position of IPC's Technical Activities Executive Committee that the use and implementation of IPC publications is voluntary and is part of a relationship entered into by customer and supplier. When an IPC publication is updated and a new revision is published, it is the opinion of the TAEC that the use of the new revision as part of an existing relationship is not automatic unless required by the contract. The TAEC recommends the use of the latest revision. Adopted October 6, 1998

Why is there a charge for this document?

Your purchase of this document contributes to the ongoing development of new and updated industry standards and publications. Standards allow manufacturers, customers, and suppliers to understand one another better. Standards allow manufacturers greater efficiencies when they can set up their processes to meet industry standards, allowing them to offer their customers lower costs.

IPC spends hundreds of thousands of dollars annually to support IPC's volunteers in the standards and publications development process. There are many rounds of drafts sent out for review and the committees spend hundreds of hours in review and development. IPC's staff attends and participates in committee activities, typesets and circulates document drafts, and follows all necessary procedures to qualify for ANSI approval.

IPC's membership dues have been kept low to allow as many companies as possible to participate. Therefore, the standards and publications revenue is necessary to complement dues revenue. The price schedule offers a 50% discount to IPC members. If your company buys IPC standards and publications, why not take advantage of this and the many other benefits of IPC membership as well? For more information on membership in IPC, please visit www.ipc.org or call 847/597-2809.

Thank you for your continued support.

IPC-6012E

Qualification and Performance Specification for Rigid Printed Boards

Developed by the Rigid Printed Board Performance Specifications Task Group (D-33a) of the Rigid Printed Board Committee (D-30) of IPC

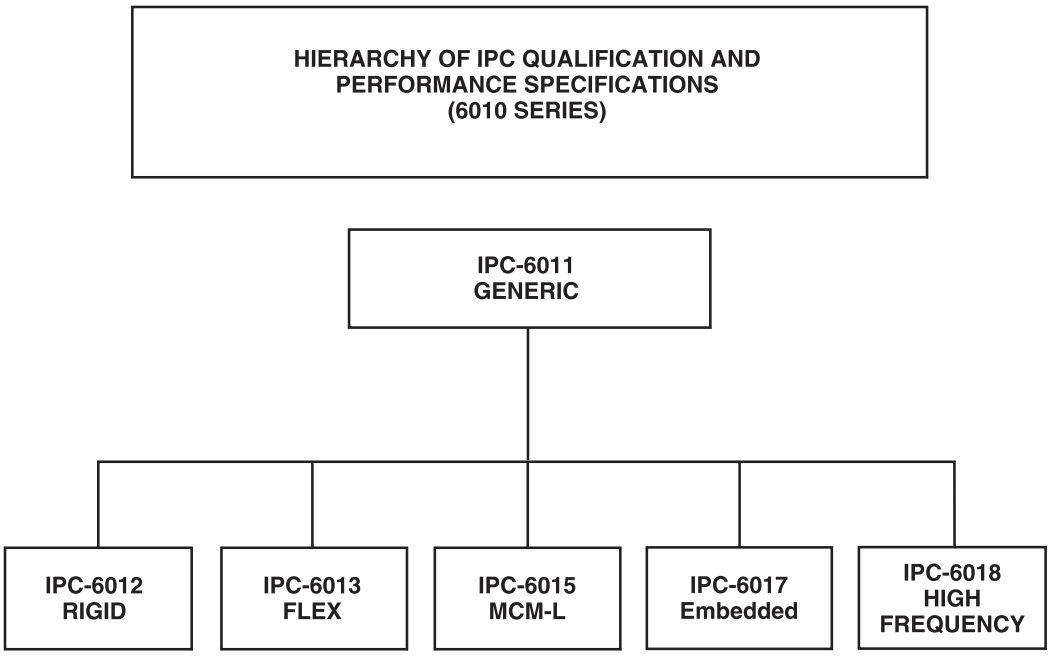
Supersedes:

IPC-6012D - September 2015
IPC-6012C - April 2010
IPC-6012B with
Amendment 1 - July 2007
IPC-6012B - August 2004
IPC-6012A with
Amendment 1 - July 2000
IPC-6012A - October 1999
IPC-6012 - July 1996
IPC-RB-276 - March 1992

Users of this publication are encouraged to participate in the development of future revisions.

Contact:

IPC
3000 Lakeside Drive, Suite 105N
Bannockburn, Illinois
60015-1249
Tel 847 615.7100
Fax 847 615.7105



FOREWORD

This specification is intended to provide information on the detailed performance criteria of rigid printed boards. It supersedes IPC-6012B and was developed as a revision to those documents. The information contained herein is also intended to supplement the generic requirements identified in IPC-6011. When used together, these documents should lead both manufacturer and customer to consistent terms of acceptability.

IPC's documentation strategy is to provide distinct documents that focus on specific aspects of electronic packaging issues. In this regard, document sets are used to provide the total information related to a particular electronic packaging topic. A document set is identified by a four digit number that ends in zero (0) (i.e., IPC-6010).

Included in the set is the generic information, which is contained in the first document of the set. The generic specification is supplemented by one or multiple performance documents, each of which provide a specific focus on one aspect of the topic or the technology selected.

Failure to have all information available prior to building a board may result in a conflict in terms of acceptability.

As technology changes, a performance specification will be updated, or new focus specifications will be added to the document set. The IPC invites input on the effectiveness of the documentation and encourages user response through completion of ''Suggestions for Improvement'' forms located at the end of each document.

Acknowledgment

Any document involving a complex technology draws material from a vast number of sources across many continents. While the principal members of the Rigid Printed Board Performance Specifications Task Group (D-33a) of the Rigid Printed Board Committee (D-30) are shown below, it is not possible to include all of those who assisted in the evolution of this standard. To each of them, the members of the IPC extend their gratitude.

Rigid Printed Board Committee	Rigid Printed Board Performance Specifications Task Group	Technical Liaison of the IPC Board of Directors
Chair Cliff Maddox Boeing Company	Co-Chairs Mark Buechner BAE Systems Randy Reed R. Reed Consultancy LLC	Bob Neves Microtek (Changzhou) Laboratories

Rigid Printed Board Performance Specifications Task Group

Elizabeth A. Allison, NTS - Baltimore
David Anderson, Raytheon Company
Norman Armendariz, Raytheon Company
Lance A. Auer, Conductor Analysis Technologies, Inc.
Jimmy Baccam, Lockheed Martin Missiles & Fire Control
Chris R. Ballou, TTM Technologies Inc.
Tiberiu Baranyi, Flextronics Romania SRL
John A. Bauer, Collins Aerospace
James Frederick Blanche, NASA Marshall Space Flight Center
William Bowerman, MacDermid Enthone Electronics Solutions
Scott A. Bowles, Lockheed Martin Corporation
Steven A. Bowles, DuPont SVTC
Alex Chandy, Advanced Circuits - Chandler Division
Denise Charest, Amphenol Printed Circuits, Inc.
Patrice Chetanneau, Sagem
Thomas Joe Clark, Lockheed Martin Missiles & Fire Control
Carl Colangelo, Dow Electronic Materials
Michael A. Collier, Teledyne Leeman Labs
Robert W. Cooke NASA, Marshall Space Flight Center
Jiong (Crystal) Dai, Shennan Circuits Co. Ltd.
Cesar De Luna, NTS - Anaheim
Radu C. Dinica, TTM Technologies
Don Dupriest, Lockheed Martin Missiles & Fire Control
Julie Ellis, TTM Technologies
Judi Emerson, Flex-N-Gate
Gary F. Erickson, Sanmina Corporation
Richard K. Etchells, Electronic Technology Resource Partners
Stephan Dennis Evans, L3Harris Communications
Robert Farfan, TTM Technologies
Gary M. Ferrari, FTG Circuits
Chris Fitzgerald, Nasa Goddard Space Flight Center
Eric Foote, GE Aviation
William Fox, Lockheed Martin Missile & Fire Control
Bryan Gahan, Electrotek Corp.
Mahendra S. Gandhi, Northrop Grumman Aerospace Systems
Gonzalo J Garcia Leypon, Cirexx International, Inc.
Pierre-Emmanuel Goutorbe, Airbus Defence & Space
Ty Gragg, Unicircuit Inc.
William H. Graver, NTS - Baltimore
Chad Gustafson, TTM Technologies
Vicka Hammill, Honeywell Inc. Air Transport Systems
Hardeep S. Heer, FTG Circuits
Philip M. Henault, Raytheon
Allen Holl, TTM Technologies
Joe Hughes, Hughes Circuits, Inc.
Frank Huijsmans, PIEK International Education Centre (I.E.C.) BV
Joseph E. Kane, BAE Systems
Don Kaufman, Cirexx International, Inc.
Allen Keeney, Johns Hopkins University
Warren S. Kenzie, MacDermid Alpha Automotive
Suriyakan Vongtragool, Kleitz Schlumberger Well Services
Kelly Kovalovsky, BAE Systems
Ernest J. Kreiner, L3Harris
Nick S. Koop, TE Connectivity
Kevin Kusiak, Lockheed Martin Corporation
Meredith LaBeau, Calumet Electronics Corp.
Jeremy Lakoskey, Honeywell International
Leo P. Lambert, EPTAC Corporation
Christina Landon, NSWC Crane
Minsu Lee, Korea Printed Circuit Association
David Lee, BMK Professional Electronics Gmb
Peggy LeGrand, TTM Technologies
Jeff Lewis, Holaday Circuits Inc.

Peter B. Lindhardt TTM Technologies - Logan Division

Jennifer Ly, BAE Systems

Clifford R. Maddox, Boeing Company

Chris Mahanna, Robisan Laboratory Inc.

Jefferson Mao, Schweizer Electronic (Jiangsu) Co.,Ltd.

John B. Marke, UL LLC

Rene R. Martinez, Northrop Grumman Aerospace Systems

Daniel McCormick, NSWC Crane

Tim McKliget, Holaday Circuits Inc.

Matthew T. McQueen, NSWC Crane

Melissa Meagher, Raytheon Missile Systems

Peter B. Menuez, L3Harris Technologies, Inc.

Michael P. Miller, NSWC Crane

Timothy Minko, BAE Systems

James J. Monarchio, TTM Technologies

Steven Murray, Northrop Grumman Corporation

Thi V. Nguyen, Lockheed Martin Missile & Fire Control

Jamie Noland, Blackfox Training Institute

Gerard A. O'Brien, Solderability Testing & Solutions, Inc.

William A. Ortloff, Raytheon Company

Gianluca Parodi, IIS Progress SRL

Gerry Partida, Summit Interconnect - Anaheim

Helena Pasquito, EPTAC Corporation

Yogen M. Patel, Candor Industries Inc.

Trevor Patterson, Hughes Circuits, Inc.

Stephen Pierce, SGP Ventures, Inc.

John A. Potenza, Lockheed Martin Mission Systems & Training

Alan Preston, TTM Technologies

Owen Reid, Lockheed Martin Missiles & Fire Control

Yaoru Ren, Shengyi Electronics Co. Ltd.

Curtis R. Ricotta, Lockheed Martin Space Systems Company

Jose A. Rios, Raytheon

Nef Rios, Summit Interconnect - Anaheim

Thomas Romont, IFTEC

Steven D. Roy, Roy Design and Manufacturing Service

Karl A. Sauter, Oracle America, Inc.

Joseph C. Schmidt, Raytheon Missile Systems

Mark William Scrimes, Raytheon Company

Gilbert Shelby, Raytheon Systems Company

Russell S. Shepherd, NTS - Anaheim

Hans L. Shin, Pacific Testing Laboratories, Inc.

Patrick Smith, Cirexx International, Inc.

David Sommervold, Henkel US Operations Corp.

Bhanu Sood, NASA Goddard Space Flight Center

Brian Stevens, Collins Aerospace

Marshall Hamilton Stolstrom, TTM Technologies, Inc.

Bradley E. Toone, L3Harris Communications

Crystal E. Vanderpan, UL LLC

Jennet Volden, Collins Aerospace

Debbie Wade, Advanced Rework Technology-A.R.T

Table of Contents

Figures

Tables

This Page Intentionally Left Blank

Qualification and Performance Specification for Rigid Printed Boards

1 SCOPE

1.1 Statement of Scope This specification establishes and defines the qualification and performance requirements for the fabrication of rigid printed boards.

1.2 Purpose The purpose of this specification is to provide requirements for qualification and performance of rigid printed boards based on the following constructions and/or technologies. These requirements apply to the finished product unless otherwise specified:

- Single-sided, double-sided printed boards with or without plated-through holes (PTHs).
- Multilayer printed boards with PTHs with or without buried/blind vias/microvias.
- Active/passive embedded circuitry printed boards with distributive capacitive planes and/or capacitive or resistive components.
- Metal core printed boards with or without an external metal heat frame, which may be active or non-active.

1.2.1 Supporting Documentation IPC-A-600, which contains figures, illustrations and photographs that can aid in the visualization of externally and internally observable acceptable/nonconforming conditions, may be used in conjunction with this specification for a more complete understanding of the recommendations and requirements.

1.3 Performance Classification and Type

1.3.1 Classification This specification establishes acceptance criteria for the performance classification of rigid printed boards based on customer and/or end-use requirements. Printed boards are classified by one of three general Performance Classes as defined in IPC-6011.

1.3.1.1 Requirement Deviations Requirements deviating from these heritage classifications **shall** be as agreed between user and supplier (AABUS).

1.3.1.2 Space Requirement Deviations Space performance classification deviations are provided in the IPC-6012ES Addendum and are applicable when the addendum is specified within the procurement documentation.

1.3.2 Printed Board Type Printed boards without PTHs (Type 1) and with PTHs (Types 2-6) are classified as follows and may include technology adders as described in Table 1-1:

Type 1 — Single-Sided Printed Board
Type 2 — Double-Sided Printed Board
Type 3 — Multilayer Printed Board without blind or buried vias
Type 4 — Multilayer Printed Board with blind and/or buried vias (may include microvias)
Type 5 — Multilayer metal core Printed Board without blind or buried vias
Type 6 — Multilayer metal core Printed Board with blind and/or buried vias (may include microvias)

1.3.3 Selection for Procurement Performance Class **shall** be specified in the procurement documentation.

The procurement documentation **shall** provide sufficient information to fabricate the printed board and ensure that the user receives the desired product. Information that should be included in the procurement documentation is to be in accordance with IPC-2611 and IPC-2614.

The procurement documentation **shall** specify the thermal stress test method to be used to meet the requirement of 3.6.1. Selection **shall** be from those depicted in 3.6.1.1, 3.6.1.2 and 3.6.1.3. If not specified (see 5.1), the default **shall** be per Table 1-2.

During the selection process, the user should take into consideration the following when determining the appropriate thermal stress test method:

• Wave solder, selective solder, hand solder assembly processes (see 3.6.1.1)

• Conventional (eutectic SnPb) reflow processes (see 3.6.1.2)

• Lead-free reflow processes (see 3.6.1.3)

The addition of IPC-2221 Appendix A conformance coupons by the printed board manufacturer to the manufacturing panel **shall** be AABUS.

1.3.3.1 Selection (Default) The procurement documentation **shall** specify those requirements that are a result of the selection process within this specification. This includes all references to "AABUS." If the requirement selection is not made in accordance with 1.3.3.2, the procurement documentation, Ordering Data (see 5.1), Customer Drawing and/or supplier control plan (SCP), then the default requirement in Table 1-2 **shall** apply.

1.3.3.2 Selection System (Optional) The following product selection identifier system is provided for clarification of the build type.

Quality Specification, the generic quality specification.

Specification, the base performance specification.

Type, the printed board type per 1.3.2.

Plating Process, the plating process per 1.3.4.2.

Surface Finish, the surface finish code per 1.3.4.3.

Selective Finish, the selective finish code adder per 1.3.4.3, enter "-" when no selective finish is required.

Classification, the classification per 1.3.1 or performance specification sheet.

Technology Adder, the technology adder as specified in Table 1-1. Add multiple codes as required.

Table_1-1 Technology Adders

Technology Code	Technology
HDI	HDI build-up features
VP	Via Protection
WBP	Wire Bondable Pads
MB	Metal Base
AMC	Active Metal Core
NAMC	Non-active Metal Core
HF	External Heat Frame
EP	Embedded Passives per IPC-6017
VIP-C	Via-in-Pad, Conductive Fill
VIP-N	Via-in-Pad, Nonconductive Fill

Example: IPC-6011/6012/3/1/S/-/3/HDI/EP

1.3.4 Material, Plating Process and Surface Finish

1.3.4.1 Laminate Material Laminate material is identified by numbers and/or letters, classes and types as specified by the appropriate specification listed in the procurement documentation.

Table 1-2 Default Requirements

Category	Default Selection
Performance Class	Class 2
Material	Epoxy-Glass Laminate per 3.2.1
Surface Finish	Finish X per Table 3-3
Minimum Starting Foil Weight	1/2 oz. for all internal and external layers except Type 1 which **shall** start with 1 oz. For plated HDI layers - 1/4 oz. for all layers (internal or external)
Copper Foil Type	Electrodeposited per 3.2.4
Hole Diameter Tolerance Plated, components Plated, via only Non-plated	 (±) 100 µm [3,937 µin] (+) 80 µm [3,150 µin], (-) no requirement, (may be totally or partially plugged) (±) 80 µm [3,150 µin]
Conductor Width tolerance	Class 2 requirements per 3.5.1
Conductor Spacing tolerance	Class 2 requirements per 3.5.2
Dielectric Separation	90 µm [3,543 µin] minimum per 3.6.2.18
Lateral Conductor Spacing (Metal Cores)	100 µm [3,937 µin] minimum per 3.6.2.17
Marking Ink	Contrasting color, nonconductive per 3.3.5
Solder Mask	Not applied, if not specified per 1.3.4.3
Solder Mask, specified	Class T of IPC-SM-840 if class not specified per 3.7
Solder Coating	Sn63/Pb37 per 3.2.7.3.1
Solderability Test	Per 3.3.6, Category 2 for SnPb and Category A for Pb-free of J-STD-003.
Thermal Stress Test	IPC-TM-650, Method 2.6.8, Condition A per 3.6.1.1
Test Voltage, Isolation Resistance	Per IPC-9252
Qualification not specified	See IPC-6011

1.3.4.2 Plating Process The copper plating process, which is used to provide conductivity in the holes, is identified by a single number as follows:

1. Acid copper electroplating only
2. Pyrophosphate copper electroplating only
3. Acid and/or pyrophosphate copper electroplating
4. Additive/electroless copper
5. Electrodeposited Nickel underplate with acid and/or pyrophosphate copper electroplating

1.3.4.3 Surface Finish and Coatings The surface finish/coating can be one of the finishes/coatings specified below or a combination of several platings and is dependent on assembly processes and end-use. If required, the thickness **shall** be specified in the procurement documentation. If not specified, the thickness **shall** be as listed in Table 3-3. Coating thickness may be exempted in Table 3-3 (i.e., tin-lead plate or solder coating). Designators for surface finish are as follows:

S Solder Coating ..... (Table 3-3)
T Electrodeposited Tin-Lead, (fused) ..... (Table 3-3)
X Either Type S or T ..... (Table 3-3)
TLU Electrodeposited Tin-Lead (unfused) ..... (Table 3-3)
b1 Lead-free Solder Coating ..... (Table 3-3)
G Gold Electroplate for Edge Printed Board Connectors ..... (Table 3-3)
GS Gold Electroplate for Areas to be Soldered ..... (Table 3-3)
GWB-1 Gold Electroplate for areas to be wire bonded (ultrasonic) ..... (Table 3-3)
GWB-2 Gold Electroplate for areas to be wire bonded (thermosonic) ..... (Table 3-3)
N Nickel for Edge Printed Board Connectors ..... (Table 3-3)
NB Nickel as a Barrier to Copper-Tin Diffusion ..... (Table 3-3)

OSP	Organic Solderability Preservative	(Table 3-3)
HT OSP	High Temperature OSP	(Table 3-3)
ENIG	Electroless Nickel Immersion Gold	(Table 3-3)
ENEPIG	Electroless Nickel/Electroless Palladium/Immersion Gold	(Table 3-3)
DIG	Direct Immersion Gold	(Table 3-3)
NBEG	Nickel Barrier/Electroless Gold	AABUS
IAg	Immersion Silver	(Table 3-3)
ISn	Immersion Tin	(Table 3-3)
C	Bare Copper	(Table 3-3)
SMOBC	Solder Mask over Bare Copper	(3.2.8)
SM	Solder Mask over Non-Melting Metal	(3.2.8)
SM-LPI	Liquid Photoimageable Solder Mask over Non-Melting Metal	(3.2.8)
SM-DF	Dry Film Solder Mask over Non-Melting Metal	(3.2.8)
SM-TM	Thermal Mask Solder Mask over Non-Melting Metal	(3.2.8)
Y	Other	(3.2.7.11)

1.4 Terms and Definitions The definition of all terms used herein **shall** be in accordance with IPC-T-50 and as follows.

1.4.1 Back-Drilling A method of reducing the overall length of any plated hole by drilling out a portion of the plated hole from either side to a predetermined depth, for purposes of signal integrity or circuit isolation (See Figure 1-1).

Figure 1-2 provides an example of a "shallow back-drill" where the external layer is pierced and approximately 0.05 - 0.127 mm [0.002 - 0.005 in] of the barrel is drilled out in order to prevent shorting of the plated via to any component/ chassis placed directly above or below the back-drill side.

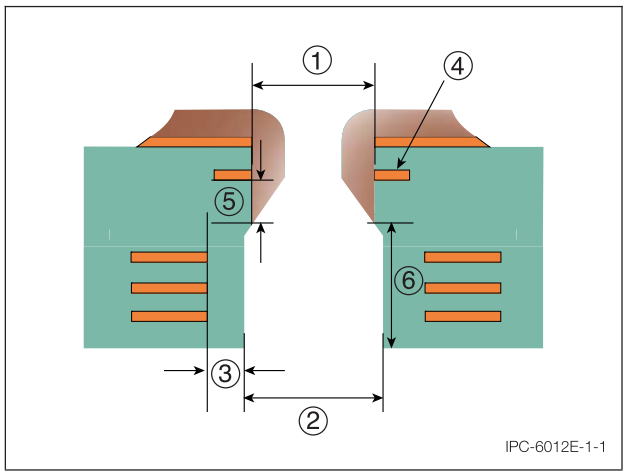


Figure 1-1 Example of a Back-Drilled Hole (Not To Scale)
Note 1. Primary drilled hole diameter.
Note 2. Back-drill hole diameter.
Note 3. Distance between nearest conductive feature and back-drill hole.
Note 4. Target Layer (e.g., Must Not Cut Layer).
Note 5. Stub length (excluding target layer copper thickness).
Note 6. Back-drill depth.

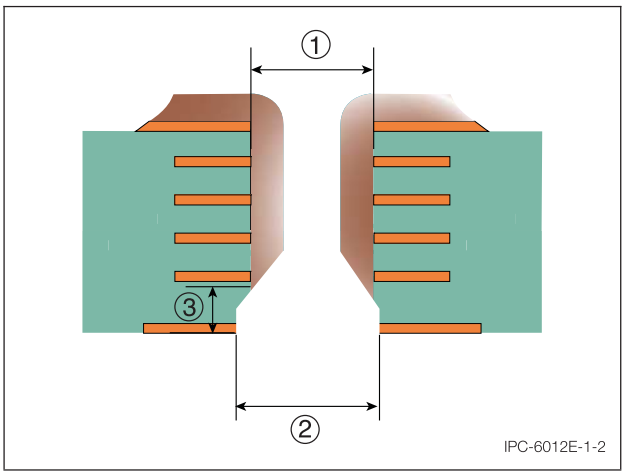


Figure 1-2 Example of a Shallow Back-Drill
Note 1. Primary drilled hole diameter.
Note 2. Back-drill hole diameter.
Note 3. Back-drill depth.

1.4.2 Stub (Plated Hole) Maximum remaining length of the hole wall plating from target layer to back drill termination.

1.4.3 High Density Interconnects (HDI) Designs with an average of 20 electrical connections/cm^2 (130 electrical connections/in^2) on one or both sides of the printed board. These designs typically have vias (≤ 0.15 mm [0.006 in.]), conductor width and spacing ≤ 100 µm [0.004 in.], via in SMT pads, and/or thin dielectric thickness where microvias (see 1.4.4) are employed.

1.4.4 Microvia A blind structure (as plated) with a maximum aspect ratio of 1:1 when measured in accordance with Figure 1-3, terminating on or penetrating a target land, with a total depth (X) of no more than 0.25 mm [0.00984 in] measured from the structure's capture land foil to the target land.

1.4.5 Design Data Data which is communicated to a printed circuit board fabricator and may include mechanical information, electrical design information and requirements concerning end item performance, item end-use environment, item configuration, materials, components, and processes.

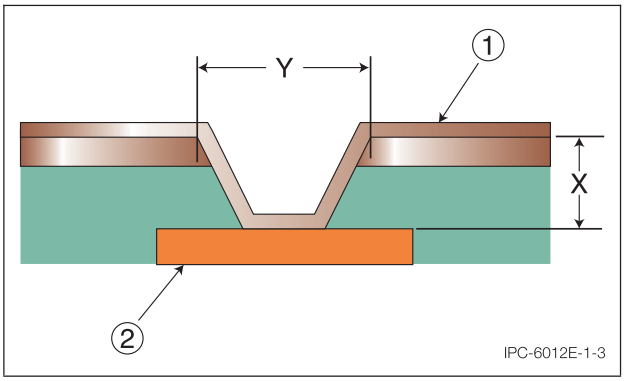


Figure 1-3 Microvia Definition

Note 1. Capture Land.
Note 2. Target Land.
Note 3: X/Y = Microvia Plating Aspect Ratio, with X ≤ 0.25 mm [0.00984 in] and aspect ratio ≤ 1:1.

1.5 Interpretation "**Shall**," the imperative form of the verb, is used throughout this standard whenever a requirement is intended to express a provision that is mandatory. Deviation from a "**shall**" requirement may be considered if sufficient data is supplied to justify the exception. To assist the reader, the word "**shall**" is presented in bold characters.

The words "should" and "may" are used whenever it is necessary to express non-mandatory provisions. "Will" is used to express a declaration of purpose.

The examples shown in the photographs and/or illustrations in this specification are sometimes exaggerated to make the referenced imperfection more apparent. The relationship between the text and the examples is not always parallel; it would be difficult to find many cases so specific that they would always match the acceptance criteria. When photographs or illustrations contained in this standard are not consistent with discussion in the written text, the written text takes precedence and **shall** be followed.

1.6 Presentation All dimensions and tolerances in this specification are expressed in hard SI (metric) units and parenthetical soft imperial (inch) units. Users of this specification are expected to use metric dimensions. All dimensions greater than or equal to 1.0 mm [0.0394 in] will be expressed in millimeters and inches. All dimensions less than 1.0 mm [0.0394 in] will be expressed in micrometers and microinches.

1.7 Design Data Protection Design data is property owned by an organization or business entity. When design data is known to or in the custody of the printed board fabricator or their agents, it **shall** be protected as-specified by the procurement documentation.

If not specified in procurement documentation, the printed board fabricator **shall** nonetheless have internal policies and procedures for protection of the design data.

An optional protocol is defined in 3.10.14.

1.8 Revision Level Changes Changes that were incorporated in the current revision of this specification are indicated throughout by gray shading of the relevant subsection(s). Changes to a figure or table are indicated by gray shading of the figure or table header.

2 APPLICABLE DOCUMENTS

The following specifications of the revision in effect at the time of order form a part of this document to the extent specified herein. If a conflict of requirements exists between this specification and the listed applicable documents, this specification **shall** take precedence.

2.1 IPC[1]

IPC-WP-023 IPC Technology Solutions White Paper on Performance-Based Printed Board OEM Acceptance: Via Chain Continuity Reflow Test: The Hidden Reliability Threat

IPC-A-47 Composite Test Pattern Ten Layer Phototool

IPC-T-50 Terms and Definitions for Interconnecting and Packaging Electronic Circuits

IPC-CF-152 Composite Metallic Material Specification for Printed Wiring Boards

IPC-A-600 Acceptability of Printed Boards

IPC-TM-650 Test Methods Manual[2]

2.1.1 Microsectioning, Manual and Semi or Automatic Method
2.3.15 Purity, Copper Foil or Plating
2.3.25 Detection and Measurement of Ionizable Surface Contaminants
2.4.1 Adhesion, Tape Testing
2.4.15 Surface Finish, Metal Foil
2.4.18.1 Tensile Strength and Elongation, In-House Plating
2.4.21 Land Bond Strength, Unsupported Component Hole
2.4.22 Bow and Twist
2.4.28.1 Adhesion, Solder Resist (Mask), Tape Test Method
2.4.36 Rework Simulation, Plated-Through Holes for Leaded Components
2.4.41.2 Coefficient of Thermal Expansion, Strain Gage Method
2.5.5.7 Characteristic Impedance and Time Delay of Lines on Printed Boards by TDR
2.5.7 Dielectric Withstand Voltage, PWB
2.6.1 Fungus Resistance, Printed Wiring Materials
2.6.3 Moisture and Insulation Resistance, Rigid Boards
2.6.3.7 Surface Insulation Resistance
2.6.4 Outgassing, Printed Boards
2.6.5 Physical Shock, Multilayer Printed Wiring
2.6.7.2 Thermal Shock, Continuity and Microsection, Printed Boards
2.6.8 Thermal Stress, Plated-Through Holes
2.6.9 Vibration, Rigid Printed Wiring
2.6.25 Conductive Anodic Filament (CAF) Resistance Test (Electrochemical Migration Test)
2.6.27 Thermal Stress, Convection Reflow Assembly Simulation

IPC-QL-653 Certification of Facilities that Inspect/Test Printed Boards, Components and Materials

IPC-CC-830 Qualification and Performance of Electrical Insulating Compound for Printed Board Assemblies

IPC-SM-840 Qualification and Performance Specification of Permanent Solder Mask

1. www.ipc.org
2. Current and revised IPC Test Methods are available on the IPC Web site (www.ipc.org/html/testmethods.htm)

IPC-1601 Printed Board Handling and Storage Guidelines

IPC-1791 Trusted Electronic Designer, Manufacturer and Assembler Requirements

IPC-2221 Generic Standard on Printed Board Design

IPC-2251 Design Guide for the Packaging of High Speed Electronic Circuits

IPC-2611 Generic Requirements for Electronic Product Documentation

IPC-2614 Sectional Requirements for Board Fabrication Documentation

IPC-4101 Specification for Base Materials for Rigid and Multilayer Printed Boards

IPC-4103 Specification for Base Materials for High Speed/High Frequency Applications

IPC-4202 Flexible Base Dielectrics for use in Flexible Printed Circuitry

IPC-4203 Adhesive Coated Dielectric Films for Use as Cover Sheets for Flexible Printed Circuitry and Flexible Adhesive Bonding Films

IPC-4552 Specification for Electroless Nickel/Immersion Gold (ENIG) Plating for Printed Circuit Boards

IPC-4553 Specification for Immersion Silver Plating for Printed Circuit Boards

IPC-4554 Specification for Immersion Tin Plating for Printed Circuit Boards

IPC-4556 Specification for Electroless Nickel/Electroless Palladium/Immersion Gold (ENEPIG) Plating for Printed Circuit Boards

IPC-4562 Metal Foil for Printed Wiring Applications

IPC-4563 Resin Coated Copper Foil for Printed Boards Guideline

IPC-4761 Design Guide for Protection of Printed Board Via Structures

IPC-4781 Qualification and Performance Specification of Permanent, Semi-Permanent and Temporary Legend and/or Marking Inks

IPC-4811 Specification for Embedded Passive Device Resistor Materials for Rigid and Multilayer Printed Boards

IPC-4821 Specification for Embedded Passive Device Capacitor Materials for Rigid and Multilayer Printed Boards

IPC-6011 Generic Performance Specification for Printed Boards

IPC-6012ES Space and Military Avionics Applications Addendum to IPC-6012 Qualification and Performance Specification for Rigid Printed Boards

IPC-6017 Qualification and Performance Specification for Printed Boards Containing Embedded Passive Devices

IPC-7711/7721 Rework, Modification and Repair of Electronic Assemblies

IPC-9151 Printed Board Process, Capability, Quality and Relative Reliability (PCQR2) Benchmark Test Standard and Database

IPC-9252 Requirements for Electrical Testing of Unpopulated Printed Boards

IPC-9691 User Guide for the IPC-TM-650, Method 2.6.25, Conductive Anodic Filament (CAF) Resistance Test (Electrochemical Migration Test)

2.2 Joint Industry Standards[3]

J-STD-001 Requirements for Soldered Electrical and Electronic Assemblies

J-STD-003 Solderability Tests for Printed Boards

J-STD-006 Requirements for Electronic Grade Solder Alloys and Fluxed and Non-Fluxed Solid Solders for Electronic Soldering Applications

J-STD-609 Marking and Labeling of Components, PCBs and PCBAs to Identify Lead (Pb), Pb-Free and Other Attributes

JP002 Current Tin Whiskers Theory and Mitigation Practices Guideline

2.3 Federal[4]

QQ-S-635 Military Standard Steel Plate, Carbon

2.4 Other Publications

2.4.1 American Society for Testing and Materials[5]

ASTM B-152 Standard Specification for Copper Sheet, Strip, Plate, and Rolled Bar

ASTM B-488 Standard Specification for Electrodeposited Coatings of Gold for Engineering Uses

ASTM B-579 Standard Specification for Electrodeposited Coating of Tin-Lead Alloy (Solder Plate)

2.4.2 Underwriters Lab[6]

UL 94 Tests for Flammability of Plastic Materials for Parts in Devices and Appliances

2.4.3 National Electrical Manufacturers Association[7]

NEMA LI-1 Industrial Laminated Thermosetting Product Standard

2.4.4 American Society for Quality[8]

H1331 Zero Acceptance Number Sampling Plans

Z1.4 Sampling Procedures and Tables for Inspection by Attributes

2.4.5 AMS[9]

SAE-AMS-QQ-A-250 General Specification for Aluminum and Aluminum Alloy, Plate and Sheet

SAE-AMS-2451 Plating, Brush General Requirements

2.4.6 American Society of Mechanical Engineers[10]

ASME B46.1 Surface Texture (Surface Roughness, Waviness and Lay)

3. www.ipc.org
4. www.sae.org
5. www.astm.org
6. www.ul.com
7. www.nema.org
8. www.asq.org
9. www.sae.org
10. www.asme.org

3 REQUIREMENTS

3.1 General Printed boards furnished under this specification **shall** meet or exceed the requirements of IPC-6011 and the specific performance class as required by the procurement documentation. Descriptions and purposes of test coupons are documented in IPC-2221 and its related appendices.

3.2 Materials

3.2.1 Laminates and Bonding Material Metal clad laminates, unclad laminates and bonding material (prepreg) **shall** be selected from IPC-4101, IPC-4202, IPC-4203, or NEMA LI-1. Polytetrafluoroethylene (PTFE) material types **shall** be selected from IPC-4103. Embedded device materials **shall** be selected from IPC-4811 or IPC-4821. The procurement documentation should specify dielectric, conductive, resistive and insulating characteristics as applicable. The specification sheet number, metal cladding type and metal clad thickness (e.g., weight) **shall** be as specified in the procurement documentation. When specific requirements such as the flammability requirements shown in UL 94 for laminate and bonding materials are required, it is necessary to specify those requirements in material procurement documents.

3.2.2 External Bonding Materials The material used to adhere external heat sinks or stiffeners or used as an insulator layer to the printed board **shall** be selected from IPC-4101, IPC-4203 or as specified in the procurement documentation.

3.2.3 Other Dielectric Materials Photoimageable dielectrics should be specified in the procurement documentation. Other dielectric materials may be specified in the procurement documentation.

3.2.4 Metal Foils Copper foil **shall** be in accordance with IPC-4562. Foil type, foil grade, foil thickness, bond enhancement treatment and foil profile should be specified on the master drawing if critical to the function of the printed board. Resin coated copper foil **shall** be in accordance with IPC-4563.

3.2.4.1 Resistive Metal Foil Resistive metal foil **shall** be as specified on the master drawing.

3.2.5 Metal Planes/Cores Internal or external metal planes and/or metal core substrates **shall** be specified on the master drawing as shown in Table 3-1.

Table 3-1 Metal Planes/Cores

Material	Specification	Alloy
Aluminum	SAE-AMS-QQ-A-250	As Specified
Steel	QQ-S-635	As Specified
Copper	ASTM-B-152 or IPC-4562	As Specified
Copper-Invar-Copper	IPC-CF-152	As Specified
Copper-Moly-Copper	IPC-CF-152	As Specified
Other	As Specified	As Specified

3.2.6 Base Metallic Plating Depositions and Conductive Coatings The thickness of the plating/surface finish coatings **shall** be in accordance with Table 3-3. The copper plating thickness for the surface, PTHs, via holes, blind vias, buried vias and microvias **shall** be as specified in Table 3-4, Table 3-5 and Table 3-6. The greater wrap plating thickness is only applicable to legacy designs per the effectivity dates listed. The thickness for specific use platings **shall** be as specified in Table 3-3. The plating thickness for surface finishes or combinations there-of selected from those listed in 1.3.4.3 **shall** be as specified in Table 3-3. Fused tin-lead plating or solder coating only requires visual coverage and acceptable solderability testing per J-STD-003. Coverage of platings and metallic coatings does not apply to vertical conductor edges. Conductor surfaces may have exposed copper in areas not to be soldered within the limits of 3.5.4.7.

Revisions to legacy designs, including those made following the effectivity date after January 01, 2018, **shall** be held at the greater wrap plating thickness unless specifically noted by the User.

Note: Changes to acceptance criteria for copper wrap plating measurements occurred within Amendment 1 to the previous Revision D of IPC-6012D. A dual criterion for Class 3 copper wrap plating was established based on design effectivity before and after 01 January 2018. This precludes imposing onto legacy designs any additional qualification activity associated with adopting newer wrap acceptance requirements.

3.2.6.1 Electroless Copper Depositions and Conductive Coatings Electroless depositions and conductive coatings **shall** be sufficient for subsequent plating processes and may be either electroless metal, vacuum deposited metal, or conductive coatings (metallic or non-metallic).

3.2.6.2 Electrodeposited Copper Electrodeposited copper plating **shall** meet the following criteria. Frequency of testing **shall** be in accordance with Table 4-4.

a) When tested in accordance with IPC-TM-650, Method 2.3.15, the purity of copper **shall** be no less than 99.50%.

b) When tested in accordance with IPC-TM-650, Method 2.4.18.1, using 50 - 100 µm [1,969 - 3,937 µin] thick samples, the tensile strength **shall** be no less than 248 MPa [36,000 PSI] and the elongation **shall** be no less than 12%.

3.2.6.3 Fully Additive Electroless Copper Depositions Additive/electroless copper platings applied as the main conductor metal **shall** meet the requirements of this specification. Deviations **shall** be AABUS.

3.2.7 Surface Finish Depositions and Coatings – Metallic and Non-Metallic

3.2.7.1 Electrodeposited Tin The allowance of and the requirements for use of electrodeposited tin **shall** be AABUS. It is recommended that the user refer to JEDEC/IPC JP002 for guidance on potential mitigation practices that may delay the onset of, or prevent, tin whisker formation.

3.2.7.2 Electrodeposited Tin-Lead Tin-lead plating **shall** meet the composition (50-70% tin) requirements of ASTM B-579. Fusing is required unless the unfused option is selected wherein the thickness specified in Table 3-3 (Code TLU) applies.

3.2.7.3 Hot Air Solder Leveling (HASL)/Solder Coating The solder coating **shall** be as specified on the master drawing and the procured solder used for coating **shall** meet the requirements of J-STD-006. HASL is the process for solder coating that involves dipping a printed board into solder and using hot air to level the resultant solder surface.

The frequency of analysis for the HASL solder pot to the limits of Table 3-2 as reprinted from IPC-J-STD-001 below **shall** be determined on the basis of Statistical Process Control (SPC) data or monthly analyses. Records containing the results of all analyses and solder bath usage (e.g., total time in use, amount of replacement solder, or area throughput) **shall** be maintained for a minimum of one year for each process/system. The percentage of each element in an alloy **shall** be determined by any standard analytical procedure with sufficient resolution. The tolerance and impurity levels of the alloy **shall** conform to limits of Table 3-2. If contamination exceeds the limits, intervals between the analyses, replacement or replenishment **shall** be shortened.

The tin content of the solder **shall** be maintained within ± 1.5% of the nominal alloy being used. Tin content **shall** be tested at the same frequency as testing for copper/gold contamination. The balance of the bath **shall** be lead and/or the items listed above. The total of copper, gold, cadmium, zinc, and aluminum contaminants **shall not** exceed 0.4%. Not applicable to lead-free alloys.

Table 3-2 Maximum Limits of SnPb Solder Bath Contaminant

Contaminant	Maximum Contaminant Weight Percentage Limit
Copper	0.3
Gold	0.2
Cadmium	0.005
Zinc	0.005
Aluminum	0.006
Antimony	0.500
Iron	0.020
Arsenic	0.030
Bismuth	0.250
Silver	0.100
Nickel	0.010
Lead	N/A

3.2.7.3.1 Eutectic Tin-Lead Solder Coating The solder used for conventional, lead-bearing coatings **shall** be in accordance with the requirements of 3.2.7.3. SnPb solder **shall** conform to the contaminant level specified in Table 3-2.

3.2.7.3.2 Lead-Free Solder Coating The solder used for lead-free solder coating **shall** be in accordance with the requirements of 3.2.7.3. Lead-free solder alloys/maximum contamination weight percentage limits **shall** be AABUS.

3.2.7.3.3 Deviations to these requirements **shall** be AABUS.

3.2.7.4 Electrodeposited Nickel Nickel plating thickness **shall** be as specified in Table 3-3 (Code N). When used as an undercoat or barrier layer for gold or other metals, the thicknesses **shall** be as specified in Table 3-3 (Code NB).

3.2.7.5 Electrodeposited Gold Electrodeposited gold plating **shall** be in accordance with ASTM-B-488. Purity and hardness **shall** be specified in the procurement documentation. The thickness **shall** be as specified in Table 3-3 (Code G, GS, GWB-1 and GWB-2).

For Reference Only: Industry investigations have shown that a gold-tin intermetallic phase forms under normal soldering process parameters. Prevention of detrimental gold embrittlement of solder joints is possible, provided there is enough solder volume present to allow dissolution of the gold so that the overall weight percentage of gold in the solder joint is below the 3-4% range.

3.2.7.6 Electroless Nickel Immersion Gold (ENIG) ENIG plating deposit **shall** be in accordance with IPC-4552. Deposit thickness **shall** be in accordance with IPC-4552 and as specified in Table 3-3 (Code ENIG). Measurement methodology **shall** be by XRF Spectrometry in accordance with Appendix 3 of IPC-4552. Frequency of sample thickness measurement for Class 1, Class 2 and Class 3 **shall** be in accordance with Table 4-3 for plating/coating thickness.

Thickness measurements **shall** be made on both sides (if applicable) of the panel.

3.2.7.7 Electroless Nickel/Electroless Palladium/Immersion Gold (ENEPIG) ENEPIG plating deposit **shall** be in accordance with IPC-4556. Deposit thickness **shall** be in accordance with IPC-4556 and as specified in Table 3-3 (Code ENEPIG). Measurement methodology **shall** be by XRF Spectrometry in accordance with Appendices 4 and 9 of IPC-4556. Frequency of sample thickness measurement for Class 1, Class 2 and Class 3 **shall** be in accordance with Table 4-3 for plating/coating thickness.

Thickness measurements **shall** be made on both sides (if applicable) of the panel.

3.2.7.8 Immersion Silver Immersion silver plating **shall** be in accordance with IPC-4553. Pad size for thickness measurements **shall** be in accordance with IPC-4553. Measurement methodology **shall** be by XRF Spectrometry in accordance with Appendix 5 of IPC-4553. Frequency of sample thickness measurement for Class 1, Class 2 and Class 3 **shall** be in accordance with Table 4-3 for plating/coating thickness.

3.2.7.9 Immersion Tin Immersion tin plating deposit **shall** be in accordance with IPC-4554. Deposit thickness range **shall** be in accordance with IPC-4554. Measurement methodology **shall** be by XRF Spectrometry in accordance with Appendix 4 of IPC-4554. Frequency of sample thickness measurement for Class 1, Class 2 and Class 3 **shall** be in accordance with Table 4-3 for plating/coating thickness.

3.2.7.10 Organic Solderability Preservative (OSP) OSPs are anti-tarnish and solderability protectors applied to copper to withstand storage and assembly processes in order to maintain solderability of surfaces. The coating storage, pre-assembly baking and sequential soldering processes impact solderability. Coating requirements for standard (Code OSP) and high-temperature (Code HT OSP) OSP formulations are in Table 3-3.

3.2.7.11 Other Metals and Coatings The allowance of and the requirements for use of other depositions as a surface finish per 1.3.4.3 such as bare copper, palladium and rhodium **shall** be AABUS.

Table 3-3 Surface Finish and Coating Requirements

Code	Finish	Thickness	Applicable Acceptability Specification	Marking Code[1]
S	Solder Coating over Bare Copper	Coverage & Solderable[2]	J-STD-003 J-STD-006	b0
b1	Lead-Free Solder Coating over Bare Copper	Coverage & Solderable[2]	J-STD-003 J-STD-006	b1
T	Electrodeposited Tin-Lead (fused) – minimum	Coverage & Solderable[2]	J-STD-003	b0
X	Either Type S or T	b0		
TLU	Electrodeposited Tin-Lead Unfused – minimum	8.0 µm [315 µin]	J-STD-003	b0
G	Gold for edge printed board connectors and areas not to be soldered – minimum	Class 1 and Class 2 0.8 µm [31.5 µin]	ASTM-B-488	b4
		Class 3 1.25 µm [49.21 µin]		
GS	Gold Electroplate on areas to be soldered – maximum[3]	0.45 µm [17.72 µin]	ASTM-B-488 J-STD-003	b4
GWB-1	Gold Electroplate for areas to be wire bonded (ultrasonic) – minimum	0.05 µm [1.97 µin]	ASTM-B-488	b4
	Electrolytic nickel under gold for areas to be wire bonded (ultrasonic) – minimum	3.0 µm [118 µin]	None	b4
GWB-2	Gold Electroplate for areas to be wire bonded (thermosonic) – minimum	Class 1 and Class 2 0.3 µm [11.8 µin]	ASTM-B-488	b4
		Class 3 0.8 µm [31.5 µin]		
	Electrolytic nickel under gold for areas to be wire bonded (thermosonic) – minimum	3.0 µm [118 µin]	None	b4
N	Nickel – Electroplate for edge printed board connectors – minimum	Class 1 2.0 µm [78.7 µin]	None	N/A
		Class 2 and Class 3 2.5 µm [98.4 µin]		
NB	Nickel-Electroplate as a barrier[4] – minimum	1.3 µm [51.2 µin]	None	N/A
OSP	Organic Solderability Preservative	Solderable[6]	J-STD-003	b6
HT OSP	High Temperature OSP	Solderable[6]	J-STD-003	b6
ENIG[5]	Electroless Nickel	IPC-4552 J-STD-003		b4
	Immersion Gold			b4
ENEPIG[5]	Electroless Nickel	IPC-4556 J-STD-003		b4
	Electroless Palladium			N/A
	Immersion Gold			b4
DIG	Direct Immersion Gold (Solderable Surface)	Solderable[6]	J-STD-003	b4
IAg[5]	Immersion Silver	IPC-4553 J-STD-003		b2
ISn[5]	Immersion Tin	IPC-4554 J-STD-003		b3
C	Bare Copper	AABUS	AABUS	N/A

Note 1. These marking and labeling codes represent the codes for surface finish categories established in IPC/JEDEC-J-STD-609.

Note 2. Hot Air Leveling (HAL) or Hot Air Solder Leveling (HASL) processes are considered to have a degree of difficulty in their control. This, coupled with pad sizes and geometries placing additional challenges on such processes, places the creation of a practical minimum thickness outside the scope of this specification. See also 3.3.6.

Note 3. See notation in 3.2.7.5.

Note 4. Nickel plating used under the tin-lead or solder coating for high temperature operating environments act as a barrier to prevent the formation of copper-tin compounds.

Note 5. For process control and qualification, surface measurements are evaluated to the applicable IPC-455X standard for coating thickness as measured on a nominal pad size of 1.5 mm x 1.5 mm [0.060 in x 0.060 in] or equivalent area.

Note 6. See 3.3.6.

Table 3-4 Surface and Hole Copper Plating Minimum Requirements for Buried Vias > 2 Layers, Through-Holes, and Blind Vias[1]

	Class 1	Class 2	Class 3
Copper – average[2,4]	20 µm [787 µin]	20 µm [787 µin]	25 µm [984 µin]
Thin areas[4]	18 µm [709 µin]	18 µm [709 µin]	20 µm [787 µin]
Wrap[3]	AABUS	5 µm [197 µin]	12 µm [472 µin][5]
Wrap[3]	AABUS	5 µm [197 µin]	5 µm [197 µin][6]

Note 1. Does not apply to microvias (see 1.4.4).
Note 2. Copper plating (1.3.4.2) thickness **shall** be continuous and extend or wrap from hole walls onto outer surfaces. Refer to IPC-A-600 for discussion on copper plating thickness for hole walls.
Note 3. Wrap copper plating for PTHs and vias **shall** be in accordance with 3.6.2.11.1. Alternatives to wrap plating **shall** be AABUS.
Note 4. See 3.6.2.11.
Note 5. Initial Release of designs (drawings) on or prior to December 31, 2017.
Note 6. Initial Release of designs (drawings) on or after January 01, 2018.

Table 3-5 Surface and Hole Copper Plating Minimum Requirements for Microvias (Blind and Buried)[1]

	Class 1	Class 2	Class 3
Copper – average[2,4]	12 µm [472 µin]	12 µm [472 µin]	12 µm [472 µin]
Thin areas[4]	10 µm [394 µin]	10 µm [394 µin]	10 µm [394 µin]
Wrap[3]	AABUS	5 µm [197 µin]	6 µm [236 µin][5]
Wrap[3]	AABUS	5 µm [197 µin]	5 µm [197 µin][6]

Note 1. See 1.4.4 for definition of microvia.
Note 2. Copper plating (1.3.4.2) thickness **shall** be continuous and extend or wrap from hole walls onto outer surfaces. Refer to IPC-A-600 for discussion on copper plating thickness for hole walls.
Note 3. Wrap copper plating for microvias **shall** be in accordance with 3.6.2.11.1 or 3.6.2.11.3. Alternatives to wrap plating **shall** be AABUS.
Note 4. See 3.6.2.11.
Note 5. Initial Release of designs (drawings) on or prior to December 31, 2017.
Note 6. Initial Release of designs (drawings) on or after January 01, 2018.

Table 3-6 Surface and Hole Copper Plating Minimum Requirements for Buried Cores (2 layers)[1]

	Class 1	Class 2	Class 3
Copper – average[2,4]	13 µm [512 µin]	15 µm [592 µin]	15 µm [592 µin]
Thin areas[4]	11 µm [433 µin]	13 µm [512 µin]	13 µm [512 µin]
Wrap[3]	AABUS	5 µm [197 µin]	7 µm [276 µin][5]
Wrap[3]	AABUS	5 µm [197 µin]	5 µm [197 µin][6]

Note 1. For through vias in the buried core.
Note 2. Copper plating (1.3.4.2) thickness **shall** be continuous and extend or wrap from hole walls onto outer surfaces. Refer to IPC-A-600 for discussion on copper plating thickness for hole walls.
Note 3. Wrap copper plating for buried via cores **shall** be in accordance with 3.6.2.11.1 or 3.6.2.11.3. Alternatives to wrap plating **shall** be AABUS.
Note 4. See 3.6.2.11.
Note 5. Initial Release of designs (drawings) on or prior to December 31, 2017.
Note 6. Initial Release of designs (drawings) on or after January 01, 2018.

3.2.8 Polymer Coating (Solder Mask) When permanent solder mask coating is specified as a surface finish per 1.3.4.3, it **shall** be a polymer coating conforming to the requirements of 3.7.

3.2.9 Fusing Fluids and Fluxes The composition of the fusing fluids and fluxes used in solder coating applications **shall** be capable of cleaning and fusing the tin-lead plating and bare copper to allow for a smooth adherent coating. The fusing fluid **shall** act as a heat transfer and distribution medium to prevent damage to the bare laminate of the printed board.

Note: Fusing fluid compatibility should be confirmed with end users' cleanliness requirements due to the diverse interactions experienced at assembly soldering.

3.2.10 Marking Inks Marking inks **shall** be permanent and **shall** conform to IPC-4781 or be as specified in the procurement documentation. Marking inks **shall** be applied to the printed board, or to a label applied to the printed board. If a conductive marking ink is used, the marking **shall** be treated as a conductive element on the printed board.

3.2.11 Hole Fill Insulation Material Electrical insulation material used for hole-fill for metal core printed boards **shall** be AABUS.

3.2.12 Heatsink Planes, External Thickness and materials for construction of heatsink planes **shall** be as specified in Table 3-1 and/or the procurement documentation. Bonding material **shall** be as specified in 3.2.2. Deviations to this requirement **shall** be AABUS.

3.2.13 Via Protection Materials used for a via protection method **shall** be as specified. Via protection types are described in IPC-4761.

3.2.14 Embedded Passive Materials Embedded passive materials are defined as materials and processes which add capacitive, resistive and/or inductive functionality within the printed board, and which may be used with conventional core materials for the manufacture of printed boards. These include laminate materials, resistive metal foils, plated resistors, conductive pastes, protectant materials, etc. Embedded passive materials **shall** be in accordance with IPC-4811 or IPC-4821.

3.3 Visual Examination Finished printed boards **shall** be examined in accordance with the following procedure. They **shall** be of uniform quality and **shall** conform to 3.3.1 through 3.3.10.

Visual examination for applicable attributes **shall** be conducted at 3 diopters (approx.1.75X).

Visual examination of microvia features for applicable dimensional or workmanship attributes **shall** be conducted at 30X minimum.

If confirmation of a suspected non-conformance cannot be made at 3 diopters, it should be verified at progressively higher magnifications (up to 40X) to confirm conformance. Dimensional requirements such as spacing or conductor width measurements may require other magnifications and devices with reticules or scales in the instrument, which allow accurate measurements of the specified dimensions. Contract or specification may require other magnifications.

3.3.1 Edges When edge spacing is designed in accordance with IPC-2222, nicks or crazing along the edge of the printed board, edges of cutouts and edges of non-plated holes are acceptable provided the penetration does not exceed the specified minimum distance between printed board edge and conductive pattern. If no edge spacing requirement is specified, any nicks or crazing **shall not** exceed 50% of the distance from the edge to the nearest conductor or 2.5 mm [0.0984 in], whichever is less.

When edge spacing is designed in accordance with IPC-2222, the distance between any edge delamination or blister and the nearest conductive feature **shall not** be less than the minimum lateral conductor spacing, or 100 µm [3,937 µin] if not specified.

When edge spacing is designed in accordance with IPC-2222, the distance between the haloing penetration and the nearest conductive feature **shall not** be less than the minimum lateral conductor spacing, or 100 µm [3,937 µin] if not specified.

When edge spacing is not designed in accordance with IPC-2222, evaluations for nicks, crazing, delamination and haloing **shall** be AABUS.

Edges **shall** be clean cut and without metallic burrs. Nonmetallic burrs are acceptable as long as they are not loose and/or do not affect fit and function. Panels, which are scored or routed with a breakaway tab, **shall** meet the depanelization requirements of the assembled printed board.

3.3.2 Laminate Imperfections Laminate imperfections include those characteristics that are both internal and external within the printed board but are visible from the surface.

3.3.2.1 Measling Measling is acceptable for Class 1, Class 2 and Class 3 end product. Measled areas in laminate substrates exceeding 50% of the spacing between non-common conductors are a process indicator for Class 3 end product, indicating a variation in material, equipment operation, workmanship or process that is not a non-conformance. Although process indicators should be monitored as part of the process control system, disposition of individual process indicators is not required and affected product should be used as is.

Note: Measling is an internal condition which does not propagate as a result of thermal stress testing per IPC-TM-650, Method 2.6.8, and has not been conclusively shown to be a catalyst for Conductive Anodic Filament (CAF) growth. Delamination is an internal condition which may propagate as a result of thermal stress testing and may be a catalyst for CAF growth. The IPC-9691 user's guide for CAF resistance testing and IPC-TM-650, Method 2.6.25, provide additional information for determining laminate performance regarding CAF growth. Users who wish to incorporate additional criteria for measling conditions may consider invoking IPC-6012ES requirements which does not allow measles.

3.3.2.2 Crazing Crazing is acceptable for all classes of end product provided the imperfection does not reduce the conductor spacing below the minimum and there is no propagation of the imperfection as a result of thermal stress testing that replicates future assembly processes. For Class 2 and Class 3, the distance of crazing **shall not** span more than 50% of the distance between adjacent conductors. Refer to IPC-A-600 for more information.

3.3.2.3 Delamination/Blistering Delamination and blistering is acceptable for all classes of end product provided the area affected by imperfections does not exceed 1% of the printed board area on each side and does not reduce the spacing between conductive patterns below the minimum conductor spacing. There **shall** be no propagation of imperfections as a result of thermal stress testing that replicates future assembly processes. For Class 2 and Class 3, the blister or delamination **shall not** span more than 25% of the distance between adjacent conductive patterns. Refer to IPC-A-600 for more information.

3.3.2.4 Foreign Inclusions Translucent particles trapped within the printed board **shall** be acceptable. Other particles trapped within the printed board **shall** be acceptable, provided the particle does not reduce the spacing between adjacent conductors to below the minimum spacing specified in 3.5.2.

3.3.2.5 Weave Exposure There **shall** be no weave exposure on the printed board for Class 3. Weave exposure is acceptable for Class 2 and Class 1 provided the imperfection does not reduce the remaining conductor spacing (excluding the area(s) with weave exposure) below the minimum. Refer to IPC-A-600 for more information.

3.3.2.6 Disrupted Fibers Disrupted fibers are acceptable for all Classes provided the imperfection does not bridge conductors and does not reduce the remaining lateral conductor spacing below the minimum.

3.3.2.7 Scratches, Dents, and Tool Marks Scratches, dents, and tool marks are acceptable provided they do not bridge conductors or disrupt fibers greater than allowed in the paragraphs above and do not reduce the dielectric spacing below the minimum specified.

3.3.2.8 Surface Voids Surface voids are acceptable provided they do not exceed 0.8 mm [0.031 in] in the longest dimension; bridge conductors; nor can the voids exceed 5% of the total printed board area per side.

3.3.2.9 Color Variations in Bond Enhancement Treatment Mottled appearance or color variation in bond enhancement treatment is acceptable. Random missing areas of treatment **shall not** exceed 10% of the total conductor surface area of the affected layer.

3.3.2.10 Pink Ring No evidence exists that pink ring affects functionality. The presence of pink ring may be considered an indicator of process or design variation but is not a cause for rejection. The focus of concern should be the quality of the lamination bond.

3.3.3 Plating and Coating Voids in the Hole When visually examined in accordance with 3.3 (not in microsection), plating and coating voids **shall not** exceed that allowed by Table 3-7.

Table 3-7 Plating and Coating Voids in the Hole

Material	Class 1	Class 2	Class 3
Copper[1]	Three voids allowed per hole in not more than 10% of the holes.	One void allowed per hole in not more than 5% of the holes.	None
Finish Coating[2]	Five voids allowed per hole in not more than 15% of the holes.	Three voids allowed per hole in not more than 5% of the holes.	One void allowed per hole in not more than 5% of the holes.

Note 1. For Class 2 product, copper voids **shall not** exceed 5% of the hole length. For Class 1 product, copper voids **shall not** exceed 10% of the hole length. Circumferential voids **shall not** extend beyond 90° of the circumference.

Note 2. For Class 2 and Class 3 product, finished coating voids **shall not** exceed 5% of the hole length. For Class 1, finished coating voids **shall not** exceed 10% of the hole length. Circumferential voids **shall not** extend beyond 90° for Class 1, Class 2 or Class 3.

3.3.4 Lifted Lands When visually examined in accordance with 3.3, there **shall** be no lifted lands on the delivered (nonstressed) printed board.

3.3.5 Marking Each individual printed board, each qualification printed board, and quality conformance test circuitry (as opposed to each individual test coupon) **shall** be marked in order to ensure traceability between the printed boards/quality conformance test circuitry and the manufacturing history and to identify the supplier (logo, etc.). The marking **shall** be produced by the same process as used in producing the conductive pattern, or by use of a permanent fungistatic ink or paint (see 3.2.10), LASER marker or by vibrating pencil marking on a metallic area provided for marking purposes or a permanently attached label. Conductive markings, either etched copper or conductive ink (see 3.2.10) **shall** be considered as electrical elements of the circuit and **shall not** reduce the electrical spacing requirements. All markings **shall** be compatible with materials and parts, legible for all tests, and in no case affect printed board performance. The use of bar code marking is permissible. When used, date code **shall** be formatted per the supplier's discretion in order to establish traceability as to

when the manufacturing operations were performed. For lead-free end product, the labeling requirements of J-STD-609 **shall** be met.

3.3.5.1 Etched Marking Etched markings are subject to the following requirements for Class 1, Class 2 and Class 3 product:

- Marking defects are acceptable regardless of cause, (i.e., solder bridging, overetching, etc.) as long as characters are legible.
- Marking does not violate the minimum electrical clearance limits.
- Irregularly formed legends are acceptable provided the general intent of the legend or marking is legible.

3.3.5.2 Ink Marking Marking **shall not** cover areas of lands that are to be soldered in excess of the following for Class 1, Class 2 and Class 3 product:

- Characters are legible.
- Ink may be built up outside the character line providing the character is legible.
- Portion of component clocking symbol outline may be missing, providing the required clocking is clearly defined.
- Marking ink on component hole land does not extend into the part mounting hole or reduce minimum annular ring.
- Marking ink is allowed in plated holes into which no component lead is soldered unless the procurement document requires that the holes be completely solder filled.
- No encroachment of marking ink on edge board printed contacts or test points.
- On surface mount lands with a pitch of 1.25 mm [0.04921 in] or greater, encroachment of marking ink is on one side of land only and does not exceed 0.05 mm [0.0020 in].
- On surface mount lands with a pitch less than 1.25 mm [0.04921 in], encroachment of marking ink is on one side of land only and does not exceed 0.025 mm [0.00098 in].
- Marking may be smeared or blurred provided it is still legible.
- Double images are legible.

3.3.5.3 Ink Marking Adhesion Ink marking adhesion **shall** be tested in accordance with IPC-TM-650 Method 2.4.1. There **shall** be no evidence of the marking ink being removed.

3.3.6 Solderability Only those printed boards that require soldering in a subsequent assembly operation require solderability testing. Printed boards that do not require soldering do not require solderability testing and this **shall** be specified on the master drawing, as in the case where press-fit components are used. Printed boards to be used only for surface mount do not require PTH solderability testing. When required by the procurement documentation, accelerated conditioning for coating durability **shall** be in accordance with J-STD-003. If the accelerated conditioning for coating durability Category is not specified, Category 2 **shall** be used for SnPb and Category A **shall** be used for lead-free. Test coupons or printed boards to be tested **shall** be conditioned, if required, and evaluated for surface and PTH solderability using J-STD-003.

Unless otherwise specified, the default test for through-hole **shall** be a solder float of the "S" coupon; the default test for surface mount **shall** be edge-dip of the "M" or "W" coupon.

SnPb solder **shall** conform to the contaminant level specified in Table 3-2 of this specification.

When solderability testing is required, consideration should be given to printed board thickness and copper thickness. As both increase, the amount of time to properly wet the sides of the PTH and the tops of the lands increases proportionately.

Note: As per the J-STD-003, edge dip testing **shall** require the use of a mechanical or electromechanical device unless AABUS (e.g., a set of tweezers does not constitute a mechanical device).

3.3.7 Plating Adhesion Plating adhesion **shall** be tested in accordance with IPC-TM-650, Method 2.4.1. There **shall** be no evidence of any portion of the protective plating or the conductor pattern foil being removed, as shown by particles of the plating or pattern foil adhering to the tape. If overhanging metal (slivers) breaks off and adheres to the tape, it is evidence of overhang or slivers, but not of plating adhesion failure.

3.3.8 Edge Printed Board Contact, Junction of Gold Plate to Solder Finish Exposed copper/plating overlap between the solder finish and gold plate **shall** meet the requirements of Table 3-8. The exposed copper/plating or gold overlap may exhibit a discolored or gray-black area which is acceptable (see 3.5.4.4).

Table 3-8 Edge Printed Board Contact Gap

	Max. Exposed Copper Gap	Max. Gold Overlap
Class 1	2.5 mm [0.0984 in]	2.5 mm [0.0984 in]
Class 2	1.25 mm [0.0492 in]	1.25 mm [0.0492 in]
Class 3	0.8 mm [0.031 in]	0.8 mm [0.031 in]

3.3.9 Back-Drilled Holes There **shall** be no plating slivers, loose debris (conductive or non-conductive) or evidence of the external land remnant in the barrel or on the outer surface of a back-drill hole. The back-drilled hole is excluded from the edge spacing requirements of 3.3.1. Finished hole size tolerance **shall** meet the requirements of 3.4.1.

3.3.10 Workmanship Printed boards **shall** be processed in such a manner as to be uniform in quality and show no visual evidence of dirt, foreign matter, oil, fingerprints, tin/ lead or solder smear transfer to the dielectric surface, flux residue and other contaminants that affect life, ability to assemble and serviceability. Visually dark appearances in nonplated holes, which are seen when a metallic or non-metallic semi-conductive coating is used, are not foreign material and do not affect life or function. Printed boards **shall** be free of non-conformances in excess of those allowed in this specification. There **shall** be no evidence of any lifting or separation of platings from the surface of the conductive pattern, or of the conductor from the base laminate in excess of that allowed. There **shall** be no loose plating slivers on the surface of the printed board.

3.4 Printed Board Dimensional Requirements Inspection of dimensional requirements **shall** be as defined herein unless otherwise AABUS. The printed board **shall** meet the dimensional requirements specified in the procurement documentation. All dimensional characteristics such as, but not limited to, printed board periphery, thickness, cutouts, slots, notches, holes, scoring and edge printed board contacts to connector key area **shall** be as specified in the procurement documentation. However, in the event that dimensional tolerances are not specified in the procurement documentation, the feature tolerances of the applicable design series specification **shall** apply. Printed board dimensional locations of basic or bilateral tolerance as defined in the procurement documentation **shall** be inspected in accordance with the applicable C=0 classification as specified in Table 4-3.

Automated inspection technology such as Automated Optical Inspection (AOI) or Coordinate Measurement Machine (CMM) is allowed.

Supplier in-process certification of features of accuracy to reduce inspection is allowed provided the method is documented and demonstrates capability to meet the specified requirements. The supplier may provide a statement of certification of accuracy based on the suppliers sampling plan which includes a process data collection and recording system.

In the event that the supplier does not have a process certification system for dimensional accuracy the C=0 levels of Table 4-3 **shall** apply for each production lot.

3.4.1 Hole Size, Hole Pattern Accuracy and Pattern Feature Accuracy The hole size tolerance, hole pattern accuracy and feature location accuracy **shall** be as specified in the procurement documentation.

Finished hole size tolerance **shall** be verified on a sample basis across all hole sizes applicable to the design. The number of measures per hole size **shall** be determined by the manufacturer to adequately sample the quantity of holes within the population.

Only holes specifically dimensioned on the master drawing that are visible from the surface **shall** be inspected for hole pattern accuracy to meet printed board dimensional requirements of 3.4. Unless required by the master drawing, hole pattern accuracy for other holes need not be checked as they are database supplied locations and are controlled by annular ring requirements to surface or internal lands. If required by master drawing, hole pattern accuracy may be certified by a statement of qualification or by C=0 sampling per 3.4.

Pattern feature accuracy **shall** be as specified in the procurement documentation. Pattern feature accuracy may be certified through a statement of qualification or by C=0 sampling per 3.4. However, in the event that any of these characteristics are not specified in the procurement documentation, the feature tolerances of Level B in the applicable IPC-2220 design series **shall** apply.

Nodules or rough plating in plated holes **shall not** reduce the hole diameter below the minimum limits defined in the procurement document.

3.4.2 Annular Ring and Breakout (External) The minimum external annular ring **shall** meet the requirements of Table 3-9. The measurement of the annular ring on external layers is from the inside surface (within the hole) to the outer edge of the

annular ring on the surface of the printed board as shown in Figure 3-1. This measurement applies to all hole structures where the inside hole wall is visually discernable from the surface. When breakout occurs and meets the requirements of Table 3-9, the plated hole **shall** meet the requirements of 3.6.2.1 and 3.6.2.2 and Figure 3-12 within the corresponding quality conformance coupon(s). When breakout is permitted at the conductor/land intersection it **shall** be in accordance with Figure 3-3. The printed board with the related breakout **shall** meet the electrical requirements of 3.8.2 (see Figure 3-2 and Figure 3-3). Unless prohibited by the customer, the employment of filleting or "tear drops" to create additional land area at the conductor junction **shall** be acceptable for Class 1 and Class 2 and in accordance with general requirements for lands with holes detailed in IPC-2221. Employment of filleting or "tear drops" in Class 3 product **shall** be AABUS.

For Class 1 and Class 2 product, when the employment of filleting or "tear drops" are prohibited by the customer or are not used, the minimum annular ring **shall** be 25um [984 µin.] at the land/conductor junction.

Table 3-9 Minimum Annular Ring[1,2]

Characteristic	Class 1	Class 2	Class 3
EXTERNAL Plated Holes	Not greater than 180° breakout of hole from land when visually assessed. The land/conductor junction **shall** not be reduced below the allowable width reduction in 3.5.3.1. If filleting or keyholing have not been employed on lands, the minimum annular ring **shall** be 25 µm [984 µin] at the land/conductor junction.	Not greater than 90° breakout of hole from land when visually assessed. The land/conductor junction **shall not** be reduced below the allowable width reduction in 3.5.3.1. The conductor junction should never be less than 50 µm [1,969 µin] or the minimum line width, whichever is smaller. If filleting or keyholing have not been employed on lands, the minimum annular ring **shall** be 25 µm [984 µin] at the land/conductor junction.	The minimum annular ring **shall** be 50 µm [1,969 µin]. The minimum external annular ring may have 20% reduction of the minimum annular ring in isolated areas due to defects such as pits, dents, nicks, pinholes, or splay in the annular ring of isolated areas.
Microvia Capture Land	Not greater than 180° breakout of hole from land when visually assessed. The land/conductor junction **shall not** be reduced below the allowable width reduction in 3.5.3.1.	Not greater than 90° breakout of hole from land when visually assessed. The land/conductor junction **shall not** be reduced below the allowable width reduction in 3.5.3.1. The conductor junction should never be less than 50 µm [1,969 µin] or the minimum line width, whichever is smaller.	There **shall** be no evidence of breakout.
INTERNAL Plated Holes	Hole breakout is allowed provided the land/conductor junction is not reduced below the allowable width reduction in 3.5.3.1. If filleting or keyholing have not been employed on lands, the minimum annular ring **shall** be 25 µm [984 µin].	90° hole breakout is allowed provided the land/conductor junction is not reduced below the allowable width reduction in 3.5.3.1. If filleting or keyholing have not been employed on lands, the minimum annular ring **shall** be 25 µm [984 µin].	The minimum internal annular ring[3] **shall** be 25 µm [984 µin].
Microvia Target Land[4]	180° hole breakout is allowed in accordance with 3.6.2.9.2	180° hole breakout is allowed in accordance with 3.6.2.9.2	There **shall** be no evidence of breakout.
EXTERNAL Unsupported Holes	Not greater than 90° breakout of hole from land when visually assessed. The land/conductor junction **shall not** be reduced below the allowable width reduction in 3.5.3.1.	Not greater than 90° breakout of hole from land when visually assessed. The land/conductor junction **shall not** be reduced below the allowable width reduction in 3.5.3.1.	The minimum annular ring **shall** be 150 µm [5,906 µin]. The minimum external annular ring may have a 20% reduction of the minimum annular ring in isolated areas due to defects such as pits, dents, nicks, pinholes or splay in the annular ring of isolated areas.

Note 1. See Figure 3-2 and Figure 3-3 for visual examples of land breakout and conductor width reduction at land.
Note 2. Minimal lateral spacing specified in 3.5.2 **shall** be met.
Note 3. See 3.6.2.9 regarding internal annular ring requirements for functional and nonfunctional lands.
Note 4. See Figure 3-4 for an example of an intermediate microvia target land.

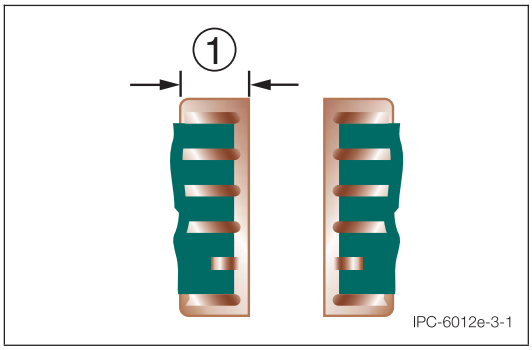


Figure 3-1 Annular Ring Measurement (External)
Note 1. Measurement of External Annular Ring

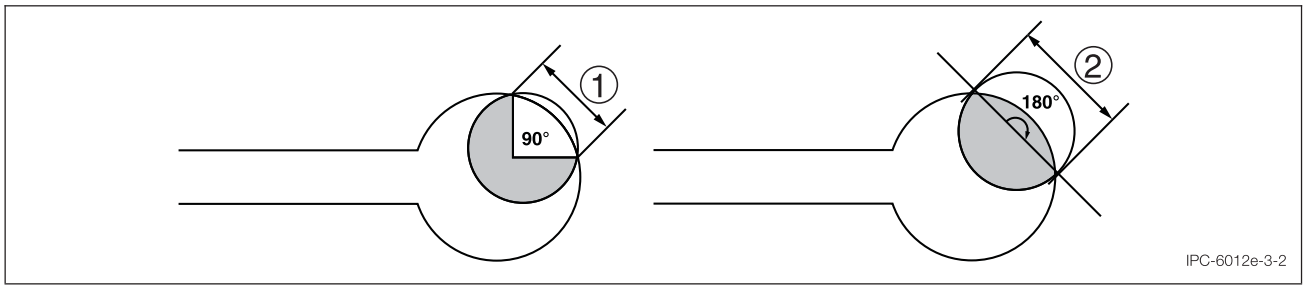


Figure 3-2 Breakout of 90° and 180°
Note 1. 1.414 x Radius of PTH
Note 2. Diameter of PTH

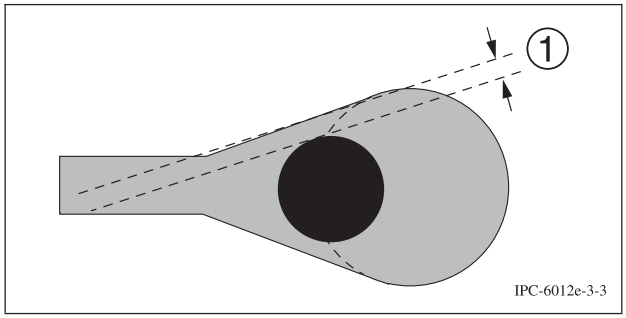


Figure 3-3 External Conductor Width Reduction
Note 1. Land/Conductor Junction meets requirements of Table 3-9 for minimum annular ring.

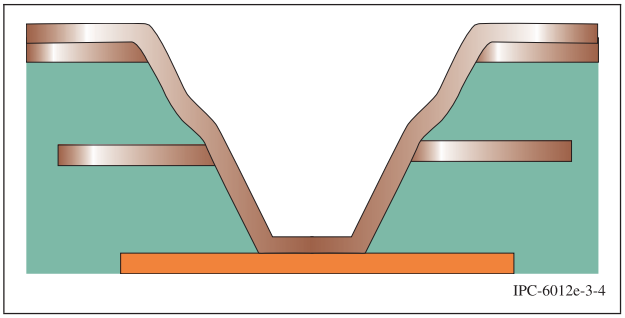


Figure 3-4 Example of Intermediate Target Land in a Microvia
Note 1. Inspection requirements for the intermediate target land within a microvia as shown in Figure 3-4 **shall** be AABUS.

3.4.3 Bow and Twist Unless otherwise specified in the procurement documentation, when designed in accordance with IPC-2221, the printed board **shall** have a maximum bow and twist of 0.75% for printed boards that use surface mount components and 1.5% for all other printed boards. Finished printed boards **shall** be assessed in the delivered form. For any product grouped in pallet arrays for assembly purposes, bow and twist requirements of the array **shall** be AABUS.

Bow, twist, or any combination thereof, **shall** be determined by physical measurement and percentage calculation in accordance with IPC-TM-650, Method 2.4.22, CMM or equivalent method.

Acceptance limits for bow and twist resulting from unbalanced construction **shall** be AABUS.

3.5 Conductor Definition All conductive areas on printed boards including conductors, lands and planes **shall** meet the visual and dimensional requirements of the following sections. The conductor pattern **shall** be as specified in the procurement documentation. Verification of dimensional attributes **shall** be performed in accordance with 3.3. AOI and CMM inspection methods are allowed, but conductor dimensional assessments by AOI **shall** be AABUS.

Internal conductors are examined during internal layer processing prior to multilayer lamination.

3.5.1 Conductor Width and Thickness When not specified on the master drawing, the minimum conductor width **shall** be 80% of the conductor pattern supplied in the procurement documentation. When not specified on the master drawing, the minimum conductor thickness **shall** be in accordance with 3.6.2.14 and 3.6.2.15.

3.5.2 Conductor Spacing The conductor spacing **shall** be within the tolerance specified on the master drawing. If minimum spacing is not specified, the allowed reduction in the nominal conductor spacings shown in the engineering documentation due to processing **shall** be 20% for Class 3 and 30% for Class 1 and Class 2 (minimum product spacing requirements as previously stated apply). Minimum spacing between the conductor and the edge of the printed board **shall** be as specified on the master drawing.

3.5.3 Conductor Imperfections The conductive pattern **shall** contain no cracks, splits or tears. The physical geometry of a conductor is defined by its width x thickness x length. Any combination of defects specified in 3.5.3.1 and 3.5.3.2 **shall not** reduce the equivalent cross-sectional area (width x thickness) of the conductor by more than 20% of the minimum value (minimum thickness x minimum width) for Class 2 and Class 3, and 30% of the minimum value for Class 1. The total combination of defect area lengths on a conductor **shall not** be greater than 10% of the conductor length or 25.0 mm [0.984 in] for Class 1 or 13.0 mm [0.512 in] for Class 2 or Class 3, whichever is less.

3.5.3.1 Conductor Width Reduction Allowable reduction of the minimum conductor width (specified or derived) due to misregistration or isolated defects (i.e., edge roughness, nicks, pinholes and scratches) which exposes base material **shall not** exceed 20% of the minimum conductor width for Class 2 and Class 3, and 30% of the minimum conductor width for Class 1.

Note: The allowable reductions assume that the manufacturer at front end tooling (CAM) understands its etch allowance and adds a producibility compensation to the original artwork design.

3.5.3.2 Conductor Thickness Reduction Allowable reduction of the minimum conductor thickness due to isolated defects (i.e., edge roughness, nicks, pinholes, depressions and scratches) **shall not** exceed 20% of the minimum conductor thickness for Class 2 and Class 3, and 30% of the minimum conductor thickness for Class 1.

3.5.4 Conductive Surfaces

3.5.4.1 Nicks and Pinholes in Ground or Voltage Planes Nicks and pinholes are acceptable in ground or voltage planes for Class 2 and Class 3 provided they do not exceed 1.0 mm [0.0394 in] in their longest dimension and there are no more than four per side per 625 cm^2 [96.88 in^2]. For Class 1, the longest dimension **shall** be 1.5 mm [0.0591 in] with no more than six per side, per 625 cm^2 [96.88 in^2].

3.5.4.2 Solderable Surface Mount Lands Defects along the edge of the land or internal to the land **shall not** exceed the requirements in 3.5.4.2.1 and 3.5.4.2.2.

3.5.4.2.1 Rectangular Surface Mount Lands Defects including but not limited to nicks, dents, nodules and pin holes along the external edge of the land **shall not** exceed 20% of either the length or width of the land for Class 2 or Class 3 printed boards, or 30% for Class 1, and **shall not** encroach the pristine area, which is defined by the central 80% of the land width by 80% of the land length as shown in Figure 3-5. Defects internal to the land **shall not** exceed 10% of the length or width of the land for Class 2 or Class 3 printed boards, or 20% for Class 1, and **shall** remain outside of the pristine area of the surface mount land. Electrical test probe "witness" marks within the pristine area for Class 1, Class 2 and Class 3 are considered cosmetic in nature and are acceptable provided the requirements for surface finish are met.

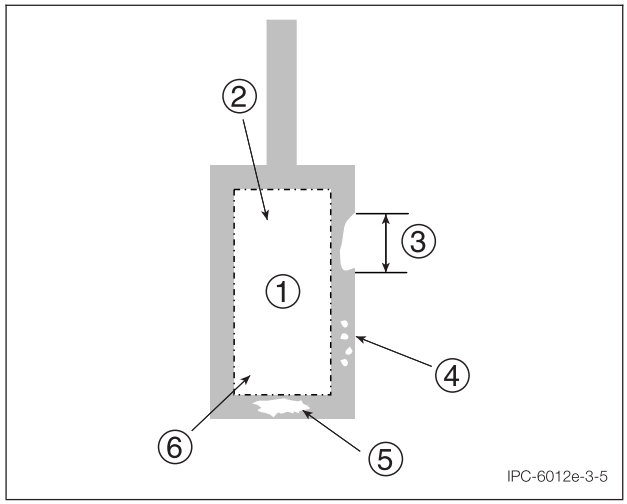


Figure 3-5 Rectangular Surface Mount Lands

Note 1. Pristine Area.
Note 2. Electrical test probe "witness" marks within the pristine area are acceptable provided the requirements for final finish are met.
Note 3. ≤ 20% of length or width for Class 2 and Class 3 does not encroach pristine area.
Note 4. Pin Holes Acceptable outside of pristine area.
Note 5. ≤ 10% length and width for Class 2 and Class 3 outside of pristine area.
Note 6. Equal to central 80% of length and width of SMT pad (land).

Any combination of isolated surface anomalies (e.g., nicks, dents, nodules, dewetting or pinholes) within the pristine area are acceptable provided the final finish requirements are met, that they are within the dimple/protrusion limits of 3.5.4.8 & 3.5.4.9 and do not occupy more than 5% of the pad area.

3.5.4.2.2 Round Surface Mount Lands (BGA Pads) Nonconformances including but not limited to nick, dents, nodules and pin-holes along the edge of the land **shall not** radially extend towards the center of the land by more than 10% of the diameter of the land for Class 1, Class 2 or Class 3 printed boards and **shall not** extend more than 20% around the circumference of the land for Class 2 or Class 3 printed boards or 30% for Class 1 as shown in Figure 3-6. There **shall** be no nonconformances within the pristine area which is defined by the central 80% of the land diameter. Electrical test probe ''witness'' marks within the pristine area for Class 1, Class 2 and Class 3 are considered cosmetic in nature and are acceptable provided the requirements for surface finish are met.

Any combination of isolated surface anomalies (e.g., nicks, dents, nodules, dewetting or pin-holes) within the pristine area are acceptable provided the final finish requirements are met, that they are within the dimple/protrusion limits of 3.5.4.8 & 3.5.4.9 and do not occupy more than 5% of the pad area.

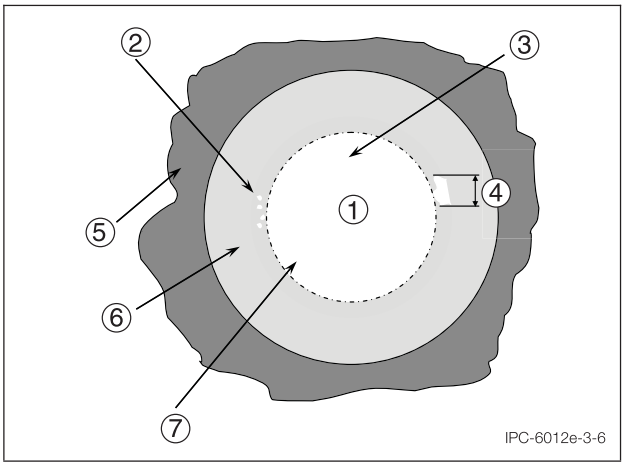


Figure 3-6 Round Surface Mount Lands

Note 1. Pristine area (80% of diameter).
Note 2. Pin holes acceptable outside of pristine area.
Note 3. Electrical test probe "witness" marks within the pristine area are acceptable provided the requirements for final finish are met.
Note 4. Defect ≤ 10% of land diameter and ≤ 20% of land circumference for Class 2 or Class 3 and does not encroach pristine area.
Note 5. Solder mask.
Note 6. Clearance in mask.
Note 7. Solderable ball pad (land).

For via-in-pad, dimples and protrusions **shall** be evaluated in accordance with 3.5.4.8 and 3.5.4.9.

3.5.4.3 Wire Bond Pad (WBP) The wire bond pad **shall** have a surface conductor finish as specified in 1.3.4.3 for ultrasonic (GWB-1) and thermosonic (GWB-2) wire bonding of gold electroplate or electroless nickel/immersion gold (ENIG), or as specified in the procurement documentation. The surface finish coating thickness **shall** be per Table 3-3 for the applicable coating used. The pristine area **shall** consist of the central 80% of the pad width by 80% of the pad length of the wire bond pad as shown in Figure 3-5. The maximum surface roughness in the pristine area of the wire bond pad **shall** be measured in accordance with an applicable test method or AABUS and **shall** be 0.8 µm [32 µin] RMS (Root-Mean-Square). If using IPC-TM-650, Method 2.4.15, it is recommended that the roughness-width cutoff identified in that method be adjusted to approximately 80% of the maximum length of the wire bond pad in order to obtain the RMS value within the pristine area. There **shall** be no pits, nodules, scratches, electrical test probe ''witness'' marks, or other defects in the pristine area that violate the 0.8 µm [32 µin] RMS roughness requirement. For more information on surface roughness, refer to ASME B46.1.3.6.2.

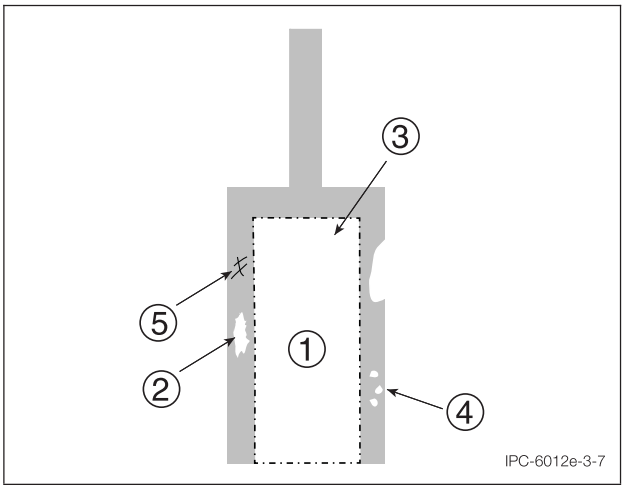


Figure 3-7 Printed Board Edge Connector Lands

Note 1. Pristine area
Note 2. Solder splash, exposed nickel or exposed copper are acceptable outside of the pristine area.
Note 3. Electrical test probe "witness" marks within the pristine area are acceptable provided the requirements for final finish are met.
Note 4. Pits, dents and depressions outside of the pristine area are acceptable provided they meet the requirements of 3.5.4.4.
Note 5. Cuts and scratches outside of the pristine area are acceptable.

3.5.4.4 Printed Board Edge Connector Lands On gold or other noble metal plated edge printed board connector lands, except as noted below, the insertion or critical contact area **shall** be free of cuts or scratches that expose underlying nickel or copper, solder splashes or tin-lead plating, and nodules or metal bumps that protrude above the surface. Pits, dents or depressions are acceptable if they do not exceed 150 µm [5,906 µin] in their longest dimension and there are not more than three per land and do not appear on more than 30% of the lands. The imperfection limits do not apply to a pristine area equal to the central 80% of the width and 90% of the length as shown in Figure 3-7.

3.5.4.5 Dewetting For tin, tin/lead reflowed, or solder coated surfaces, dewetting on conductors, areas of solder connection, and ground or voltage planes is allowed to the extent listed below:

a) Conductors and planes—permitted for all classes.

b) Individual areas of solder connection – Class 1-15%; Class 2-5%; Class 3-5%.

3.5.4.6 Nonwetting For tin, tin/lead reflowed or solder coated surfaces, nonwetting is not permitted on any conductive surface where a solder connection will be required.

3.5.4.7 Surface Finish Coverage Surface finish **shall** meet the solderability requirements of J-STD-003.

3.5.4.7.1 Exposed Basis Metal(s) (Areas not to be soldered) Exposed basis metal(s) on areas not to be soldered is permitted on 1% of the conductive surfaces for Class 3 and 5% of the surfaces for Class 1 and Class 2. Coverage does not apply to vertical conductor and plane edges. Rework of up to 5% exposed of a basis metal not to be soldered is allowed by brush plate in accordance with SAE AMS-2451.

3.5.4.7.2 Tin-Lead under Solder Mask (Areas not to be soldered) Solder mask overlap or encroachment onto tin lead or solder on areas not to be soldered is acceptable provided the overlap does not exceed 150 µm [5,906 µin].

3.5.4.8 Cap Plating of Filled Holes When cap plating of the filled hole is specified on the procurement documentation, plating voids exposing the resin fill are not allowed, unless covered by solder mask. Visually discernible depressions (dimples) and protrusions (bumps) over filled holes are acceptable providing the structural integrity requirements of 3.6.2.11.2 and Table 3-11 on the IPC-2221 Appendix B coupons are acceptable.

3.5.4.9 Copper Filled Microvias Visually discernible depressions (dimples) and protrusions (bumps) over copper filled microvias are acceptable.

3.5.4.10 Nonfunctional Lands A fabricator **shall not** remove nonfunctional lands without specific approval of the design activity or unless allowed within the procurement documentation.

3.6 Structural Integrity Printed boards **shall** meet structural integrity requirements specified in 3.6.2 for thermally stressed (see 3.6.1) test coupons. A plated hole structural integrity evaluation of a manufacturing panel requires the inspection of one A and one B, or one A/B coupon, thermally stressed. In addition, one B or A/B coupon **shall** be thermally stressed for each type of via structure, including microvias, blind and buried vias. In designs with a single hole type, a minimum of one thermally stressed coupon (A or B or A/B) **shall** be evaluated.

Although the A and B or A/B coupons are assigned for this test, the usage of printed boards to perform acceptance testing for the product **shall** be AABUS. For HDI structures with no IPC-2221 defined coupons, the usage of printed boards to perform acceptance testing for the product is acceptable. Areas selected from printed boards **shall** contain plated holes and copper features so that all criteria within this specification can be evaluated. Microsections selected from printed boards **shall** be removed from opposite panel corners, **shall** be inspected in the x and y axis, and **shall** each have three (3) holes minimum.

The printed boards and all other test coupons in the quality conformance test circuitry which contain plated holes **shall** be capable of meeting the requirements of this section. Structural integrity **shall** be used to evaluate test coupons or printed boards from Type 2 through Type 6 printed boards by micro-sectioning techniques. Characteristics not applicable to Type 2 printed boards (i.e., requirements for inner layer separations, inner layer inclusions, and inner foil cracks) are not evaluated. Dimensional measurements that are only possible through the use of microsectioning techniques are also defined in this section. Refer to IPC-2221 for coupon design to complete the structural integrity evaluation.

The evaluation of all properties and requirements **shall** be performed on the thermally stressed test coupon or printed board and all requirements **shall** be met. The coupons **shall** be tested after the printed board is exposed to all coating, surface finish and thermal processing.

Caution: As microvia structures have become more prevalent in printed board designs, there have been many examples of post fabrication microvia failures of printed boards that had otherwise met all specified lot conformance requirements of this specification. Typically, these failures occur during assembly level reflow processing, however they are often undetectable (latent) at room temperature. The further along in the assembly process that these failures manifest themselves the more expensive they become. If they remain undetected until after the end product has been placed into service, they become a much greater cost risk and, more importantly, may pose a safety risk. For this reason, a performance-based acceptance test

in accordance with 3.10.15 is recommended for all Class 3 Printed Boards containing microvias. A review by the fabricator is also recommended to evaluate the ability of the microvia structures in the design to pass a performance-based acceptance test. Refer to IPC-WP-023 for additional information.

3.6.1 Thermal Stress Testing Test coupons or printed boards **shall** be thermally stressed. Per the applicable criteria listed in 1.3.3, one or more of the following Test Methods **shall** be required.

3.6.1.1 Thermal Stress Testing, Method 2.6.8 Test coupons or printed boards **shall** be thermally stressed in accordance with IPC-TM-650, Method 2.6.8, Test condition A.

3.6.1.1.1 Thermal Stress Testing, Method 2.6.8 (Microvias) For printed boards utilizing microvias, the microvias **shall** be in contact with the solder when floated. If microvias exist on both sides of the test coupon or printed board in the test coupon to be evaluated, both sides **shall** be individually floated and evaluated after thermal stress, either on the same coupon or on individual coupons.

3.6.1.2 Thermal Stress Testing, Method 2.6.27 (230 °C) Test coupons or printed boards **shall** be thermally stressed in accordance with IPC-TM-650, Method 2.6.27, 230° C reflow profile.

3.6.1.3 Thermal Stress Testing, Method 2.6.27 (260 °C) Test coupons or printed boards **shall** be thermally stressed in accordance with IPC-TM-650, Method 2.6.27, 260° C reflow profile.

3.6.1.4 Deviations to Thermal Stress Testing Deviations to these requirements **shall** be AABUS.

3.6.1.5 Microsection Requirements Following thermal stress, test coupons or printed boards **shall** be microsectioned. Microsectioning **shall** be accomplished per IPC-TM-650, Method 2.1.1 on test coupons or printed boards. The grinding and polishing accuracy of the microsection **shall** be such that the viewing area of each of the plated holes is within 10% of the drilled hole diameter (see Figure 3-8). Evaluation of all applicable PTHs, vias and microvias, including blind and buried, for all such structures found on the finished printed board **shall** be inspected in the vertical cross section in accordance with 3.6.2 and Table 4-3.

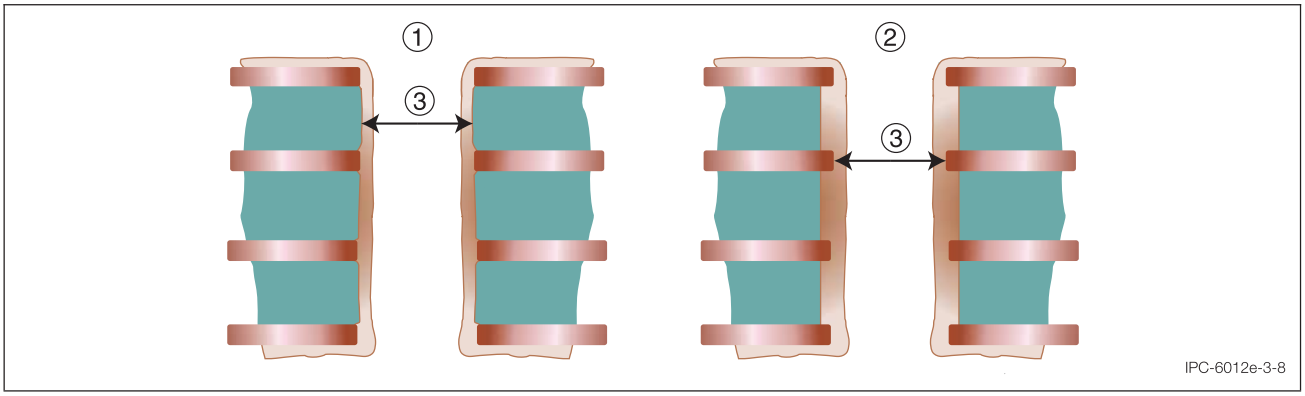


Figure 3-8 Plated Hole Microsection (Grinding/Polishing) Tolerance

Note 1: Measurement Example with a Negative Etchback Process
Note 2. Measurement Example with an Etchback/Desmear Process
Note 3. Center of Hole Measurement Location
Note 4. Minimum Viewing Area Length = Drill Diameter x 0.9
Note 5. Maximum Viewing Area Length = Drill Diameter

Evaluation of microsectioned test coupons or printed boards **shall** be performed in the "as-polished" condition (prior to microetch). Unallowable inner layer separations (see Table 3-10) and plating to target lands separations **shall not** be visible (see Figure 3-9).

Micro-etch the microsection test coupon or printed board per IPC-TM-650, Method 2.1.1.

PTHs, including buried and blind vias, **shall** be examined for foil and plating integrity at a magnification of 100X ± 5%. Referee examinations **shall** be accomplished at a magnification of 200X ± 5%. Each side of the hole **shall** be examined

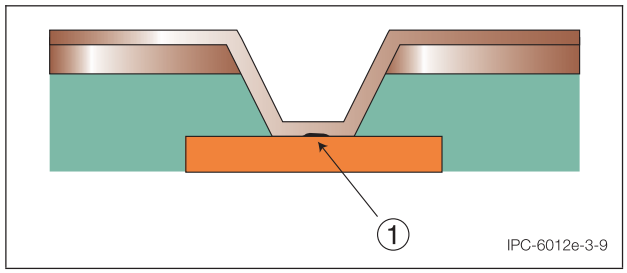


Figure 3-9 An Example of Plating to Target Land Separation

Note 1. Separation of plating on target land.

independently. Examination for laminate thickness, foil thickness, plating thickness, lay-up orientation, lamination and plating voids, and so forth, **shall** be accomplished at magnifications specified above. For foils less than 3/8 oz., 200X magnification and 400-500X referee magnification may be required to confirm minimum thickness requirement. Plating thicknesses below 1.0 µm [39.4 µin] **shall not** be measured using metallographic techniques.

Microvias **shall** be examined for plating integrity and interconnection integrity at a magnification of 200X ± 5%. Referee examinations **shall** be accomplished at a magnification of 400 - 500X. Each side of the hole **shall** be examined independently. The grinding and polishing accuracy of the microsection **shall** be such that the viewing area of the microvia is within 10% of the drilled hole diameter for three microvias (see Figure 3-8). For copper filled microvias, the grinding and polishing accuracy **shall** be sufficient to evaluate contact dimension.

Note: Alternate techniques used to supplement microsection evaluation **shall** be AABUS.

3.6.2 Requirements for Microsectioned Coupons or Printed Boards When examined in microsection, the test coupons or printed boards **shall** meet the requirements of Table 3-10 and paragraph 3.6.2.1 through 3.6.2.21.

3.6.2.1 Plating Integrity Plating integrity in the plated holes **shall** meet the requirements detailed in Table 3-10. For Class 2 and Class 3 product, there **shall** be no separation of plating layers (except as noted in Table 3-10), no copper plating cracks, and internal interconnections **shall** exhibit no separation or contamination between the plated hole wall and internal layers.

Isolated and random microanomalies (inclusions not otherwise described or prohibited) at the interface of plating and foil (excluding interconnects) or between plated layers, that do not propagate as a result of thermal stress are an indicator of process variation but **shall not** be a cause for rejection (see IPC-A-600 for examples of microanomalies).

Metal core or thermal planes, when used as electrically functional circuitry, **shall** meet the above requirements when made from copper; but those made from dissimilar metals may have small spots or pits at their junction with the hole wall plating. Those areas of contamination or inclusions **shall** neither exceed 50% of each side of the interconnection, nor occur in the interface of the copper cladding on the core and the copper plating in the hole wall when viewed in the microsection evaluation.

3.6.2.2 Copper Plating Voids Any copper plating thickness less than that specified for minimum thin areas in Table 3-4 through Table 3-6 **shall** be considered a void. Allowances for copper plating voids are established in Table 3-10 for all Classes of end product. For Class 2 and Class 3 product, the following criteria **shall** also be met:

a) There **shall** be no more than one copper plating void per test coupon or printed board, regardless of length or size.

b) There **shall** be no copper plating void in excess of 5% of the total printed board thickness.

c) There **shall** be no copper plating voids evident at the interface of an internal conductive layer and the plated hole or microvia wall.

d) Circumferential copper plating voids greater than 90° are not allowed.

Conductor finish plating or coating material between the base material and copper plating (i.e., behind the hole wall copper plating) is evidence of a void. Any plated hole exhibiting this condition **shall** be counted as having a single void for panel acceptance purposes.

If a void is detected during evaluation of a microsection which meets the above criteria, resample in accordance with 4.2.2 using samples from the same panel(s) to determine if the plating void is random. If the additional test coupons or printed boards have no plating voids, the product which the test coupon or printed boards represent are considered acceptable; however, if a plating void is present in the resampled microsections, the affected panel(s) **shall** be considered non-conforming.

Table 3-10 Plated Hole Integrity After Stress

Property	Class 1	Class 2	Class 3
Copper plating voids[2]	Three voids allowed per hole. Voids in the same plane are not allowed. No void **shall** be longer than 5% of printed board thickness. No circumferential voids greater than 90° allowed.	One void allowed per specimen provided the additional microsection criteria of 3.6.2.2 are met.	
Plating folds/inclusions	The minimum copper thickness in Table 3-4 through Table 3-6 **shall** be met. For positive etchback, measurements should follow the topography of the dielectric. When negative etchback results in folds in the copper plating, the copper thickness **shall** meet the minimum requirements as measured from the face of the internal layer as depicted in Figure 3-12. The negative etchback limits **shall** be in accordance with Figure 3-16.		
Burrs and nodules[2]	Allowed if minimum hole diameter is met.		
Glass fiber protrusion[2]	Allowed. See 3.6.2.11.		
Dielectric Removal (see Figure 3-15)	125 µm [4,921 µin] wicking allowance plus maximum etchback or smear removal allowance	100 µm [3,937 µin] wicking allowance plus maximum etchback or smear removal allowance	80 µm [3,150 µin] wicking allowance plus maximum etchback or smear removal allowance
Inner layer inclusions (inclusions at the interface between internal lands and plated hole)	Allowed on only one side of hole wall at each land location on 20% of each available land.	None allowed.	
Internal foil cracks[1]	"C" cracks allowed on only one side of hole provided it does not extend through foil thickness.	None allowed.	
External foil cracks[1,3] (Type "A," "B" and "D" cracks)	"D" cracks not allowed. "A" and "B" cracks allowed.	"D" and "B" cracks not allowed. "A" cracks allowed.	
Barrel/Corner cracks[1] (type "E" and "F" cracks)	None allowed.		
Inner layer separation (separation at the interface between internal lands and plated hole)	Allowed on only one side of hole wall at each land location on 20% of each available land.	None allowed.	
Separations along the vertical edge of the external land(s)	Allowed at knee (see Figure 3-11), maximum length 130 µm [5,118 µin].	Allowed (see Figure 3-11) provided it does not extend beyond the vertical edge of the external copper foil.	
Plating separation	None allowed.		
Hole wall dielectric/plated barrel separation	Acceptable provided dimensional and plating requirements are met.		
Lifted lands after thermal stress or rework simulation[4]	Allowed provided the finished printed boards meet the visual criteria of 3.3.4.		

Note 1. Copper crack definition: See Figure 3-10.
Note 2. The minimum copper thickness in Table 3-4 through Table 3-6 **shall** be met.
Note 3. The category "B" and "D" cracks apply regardless of the number of plating layers (may or may not include cap plating).
Note 4. No lifted lands in blind microvias after thermal stress (see 3.6.2.10).

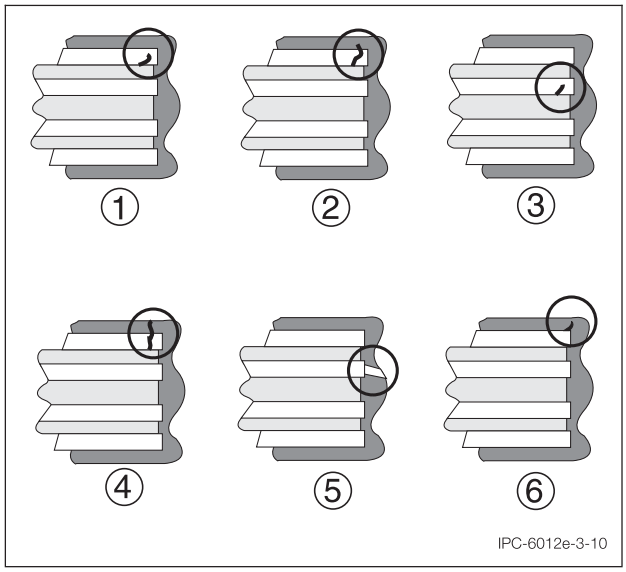


Figure 3-10 Copper Crack Definition[7]

Note 1. "A" cracks - crack in external foil.
Note 2. "B" cracks - crack does not completely break plating.
Note 3. "C" cracks - crack in internal foil.
Note 4. "D" cracks - complete fracture.
Note 5. "E" cracks - barrel crack in plating only.
Note 6. "F" cracks - corner crack in plating only.
Note 7: Copper plating as shown may include multiple plating layers or cap plating.

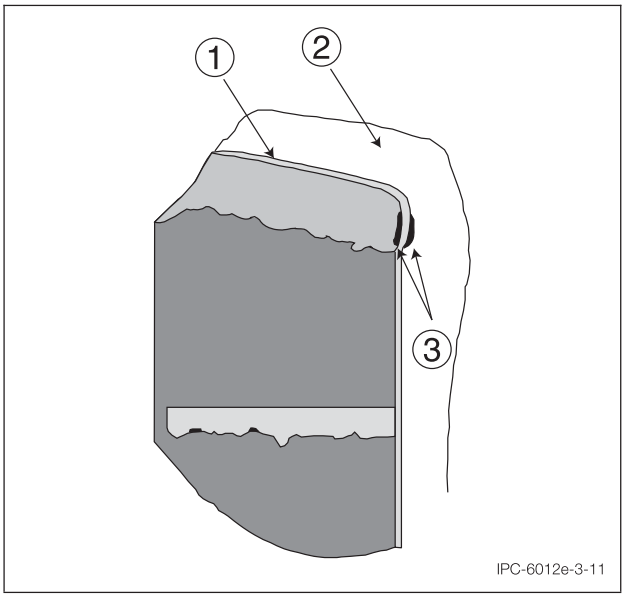


Figure 3-11 Separations at External Foil

Note 1. Conductive coatings.
Note 2. Electrolytic copper.
Note 3. Area of acceptable separation along the vertical edge of the external foil.

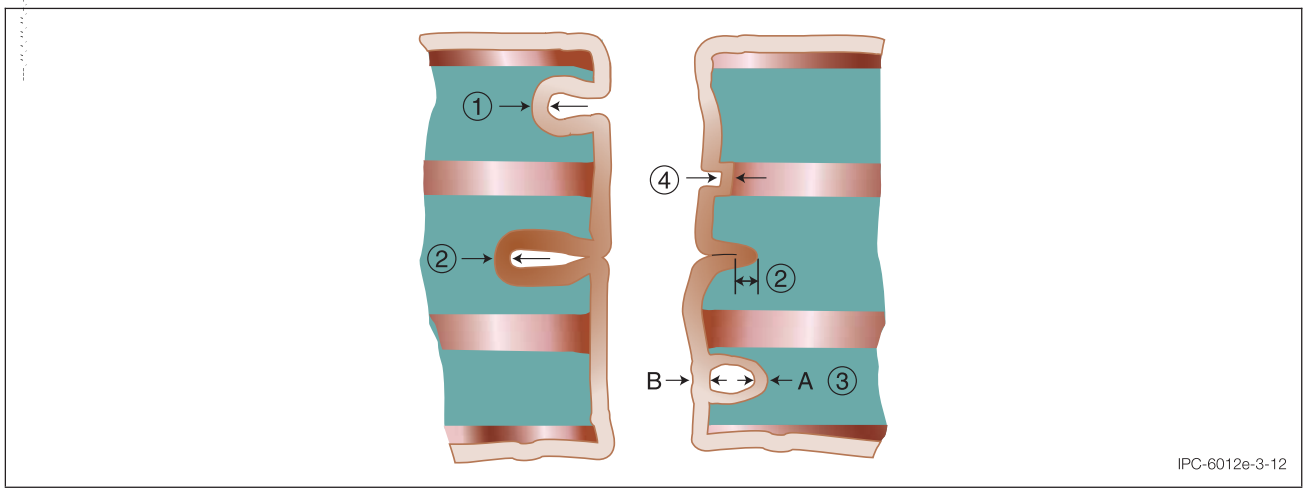


Figure 3-12 Plating Folds/Inclusions – Minimum Measurement Points

Note 1. Minimum copper plate measurement point. Plating folds that are not enclosed and where the minimum copper plate thickness in Tables 3-4, 3-5, or 3-6 is met are acceptable.
Note 2. Enclosed plating folds (inclusions) with demarcation line visible. Measure and accept per **Note 1.**
Note 3. Enclosed plating fold with no visible demarcation line. The thickness measurement A+B shall comply with the minimum copper plate thickness in Tables 3-4, 3-5, or 3-6.
Note 4. Minimum copper plate measurement point for negative etchback.

3.6.2.3 Laminate Voids For Class 2 and Class 3 products, there **shall** be no laminate voids outside of any thermal zones (see Figure 3-13) in excess of 80 µm [3,150 µin]. For Class 1 products, voids allowed outside of any thermal zone (see Figure 3-13) **shall not** exceed 150 µm [5,906 µin]. Boundary line voids that overlap into a thermal zone **shall not** be in excess of 80 µm [3,150 µin] for Class 2 or Class 3 products and 150 µm [5,906 µin] for Class 1 products. Multiple voids between two adjacent plated holes in the same plane **shall not** have a combined length which exceeds these limits. Voids between conductive patterns that are not electrically common in either the horizontal or vertical direction **shall not** decrease the minimum dielectric spacing.

3.6.2.4 Laminate Cracks Laminate cracks between conductive patterns that are not electrically common in a thermal zone (see Figure 3-13) **shall not** reduce the conductor spacing below the minimum in the horizontal direction or the minimum dielectric spacing in the vertical direction. Boundary line cracks that overlap into a thermal zone **shall not** be in excess of 80 µm [3,150 µin] for Class 2 or Class 3 products, and 150 µm [5,906 µin] for Class 1 products. Multiple cracks between two adjacent plated holes in the same plane **shall not** have a combined length which exceeds these limits.

3.6.2.5 Delamination or Blistering For Class 2 and Class 3 there **shall** be no evidence of delamination or blistering. For Class 1, if delamination or blistering is present, evaluate the entire printed board per 3.3.2.3.

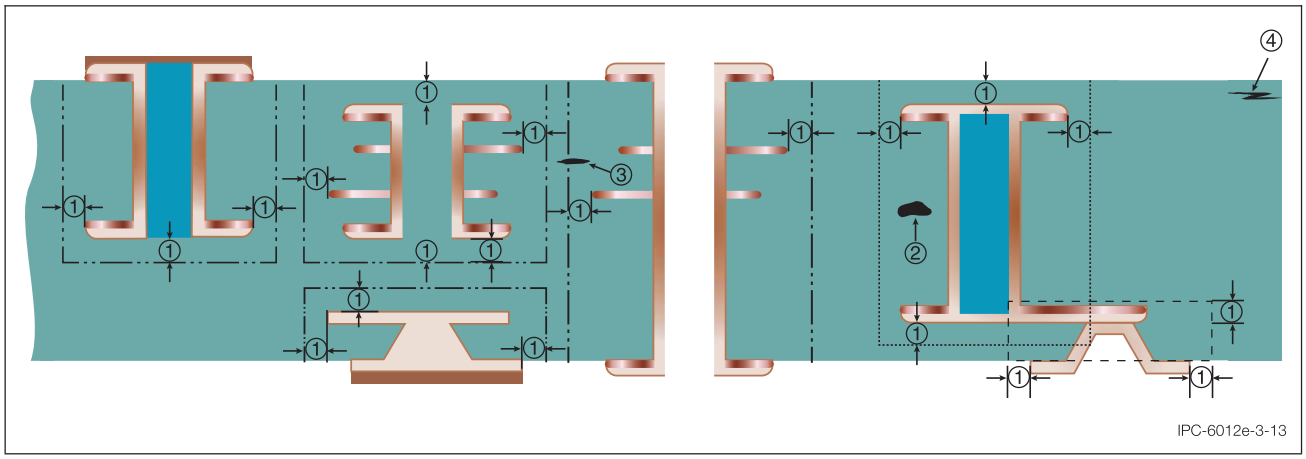


Figure 3-13 Microsection Evaluation Laminate Attributes[4]

Note 1. Thermal zones are defined by a 0.08 mm [0.0031 in] perimeter around the entirety of each via or through-hole structure (including internal and external lands). For lands that are increased in size to accommodate an offset (staggered) structure, the thermal zone is governed by the offset (staggered) structure.

Note 2. Laminate voids and cracks fully encapsulated within thermal zones are not evaluated on specimens which have been exposed to thermal stress or rework simulation.

Note 3. Delamination/Blistering is evaluated regardless of whether any portion of the anomaly is within or without a thermal zone.

Note 4: Laminate voids and cracks resulting from sample removal that are limited to the edges of the sample (at either end of the microsection specimen) are not evaluated on specimens which have been exposed to thermal stress or rework simulation.

3.6.2.6 Etchback When specified on the master drawing, printed boards **shall** be etched back for the lateral removal of resin and/or glass fibers from the drilled hole walls prior to plating. The etchback **shall** be between 5 µm [197 µin] and 80 µm [3,150 µin] with a preferred depth of 13 µm [512 µin] as shown in Figure 3-14. Shadowing is permitted on one side of each land. When no etchback is specified and the printed board manufacturer elects to use etchback, the manufacturer **shall** be qualified to perform etchback through demonstration of qualification test coupons or printed boards.

The combination of dielectric removal from etchback plus wicking allowance (wicking and random tears or drill gouges resulting from hole formation and/or hole cleaning) **shall not** exceed the sum of the maximum allowable etchback or smear removal and the maximum allowable wicking limits in Table 3-10 and as depicted in Figure 3-15.

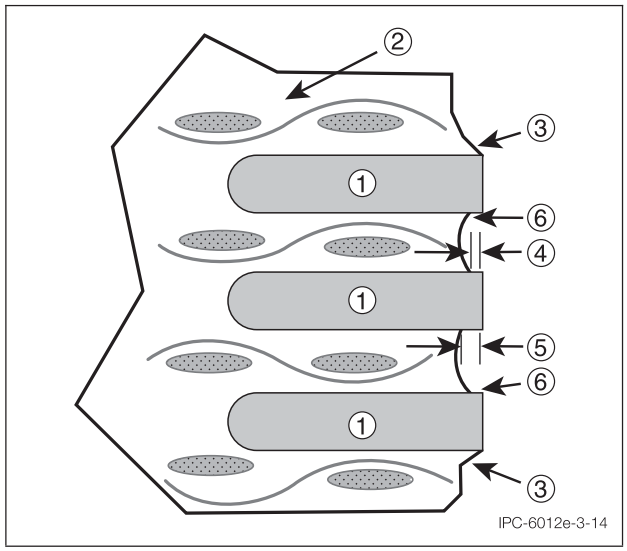


Figure 3-14 Measurement for Etchback

Note 1. Internal conductor.

Note 2. Dielectric (resin and/or glass fiber).

Note 3. Shadowing is permitted on one side of each land.

Note 4. Positive etchback measurement (minimum).

Note 5. Positive etchback measurement (maximum).

Note 6. The etchback **shall** be effective on at least the top or bottom surface of each internal conductor.

3.6.2.7 Smear Removal Smear removal is removal of resin debris that results from the formation of the hole. Smear removal **shall** be sufficient to meet the acceptability criteria for plating separation per Table 3-10. Smear removal **shall not** exceed 25 µm [984 µin]. The combination of smear removal, drill gouges, random tears, and hole formation **shall not**

exceed the dielectric removal limits in Table 3-10 as shown in Figure 3-15. Smear removal is not required of Type 1 or Type 2 printed boards. Measurement for maximum dielectric removal is depicted in Figure 3-15.

3.6.2.8 Negative Etchback Negative etchback **shall not** exceed the dimensions in Figure 3-16 when measured as shown in Figure 3-16. Negative etchback **shall not** be allowed when etchback has been specified on the procurement documentation.

3.6.2.9 Annular Ring and Breakout (Internal) Internal annular ring, if not determined by alternate techniques as agreed upon between user and supplier (AABUS), **shall** be measured by microsection to verify conformance to Table 3-9. Measurements for internal annular ring are taken at the copper hole wall plating/internal land interface to the outer most tip of the internal land as shown in Figure 3-17.

For Class 1 and Class 2 product, breakout is allowed if modified land shapes such as filleting or "keyholing" have been employed. For Class 1 and Class 2 product, if filleting or keyholing have not been employed on lands, the minimum annular ring **shall** be 25 µm [984 µin]. Employment of filleting or "tear drops" in Class 3 product **shall** be AABUS. Unless prohibited by the customer, the employment of filleting or "tear drops" to create additional land area at the conductor junction **shall** be acceptable for Class 1 and Class 2 and in accordance with general requirements for lands with holes detailed in IPC-2221.

External pads of sequentially laminated structures that are buried are considered as an external layer and are evaluated in process prior to additional lamination(s) to the annular ring and breakout requirements as stated in 3.4.2, which **shall** be met in the microsection after final lamination. Microsection analysis is performed per 3.6.2.

Note: Consideration should be given to how the microsection cut is "clocked," or rotated. Misregistration can occur randomly as opposed to orthogonally and therefore an orthogonal cut will not guarantee that a microsection view will portray hole breakout, if it exists. See Figure 3-18 and Figure 3-19 for an example of how breakout may or may not be detected within a microsection based on the rotation.

When the annular ring requirement is less than Class 3 (i.e., tangency or breakout), the minimum foil, conductor height and wrap plating requirements of Table 3-14, Table 3-15 and 3.6.2.11 do not apply where an annular ring is not required.

For Class 2 printed boards, if internal annular ring breakout is detected in the vertical cross section, but the degree of breakout cannot be determined, internal registration may be assessed by nondestructive techniques other than microsection, such as special patterns, probes, and/or software, which

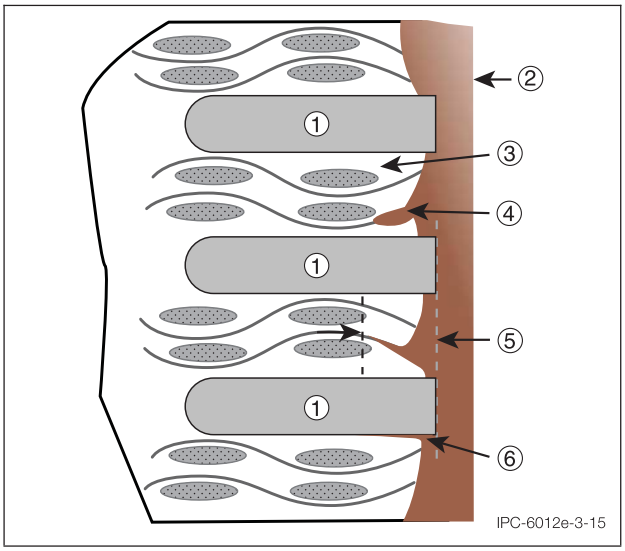


Figure 3-15 Measurement for Dielectric Removal

Note 1. Internal conductor.
Note 2. Copper plating.
Note 3. Dielectric (resin and/or glass fiber).
Note 4. Example of drill gouge or random "tear outs."
Note 5. Dielectric removal: Combined wicking allowance plus etchback or smear removal allowance (maximum) is measured from the drilled edge of the foil.
Note 6. Dielectric removal along the inner layer foil combined with copper penetration resulting from combined allowances for wicking plus etchback or smear removal allowance (maximum) as measured from the drilled edge of the foil.

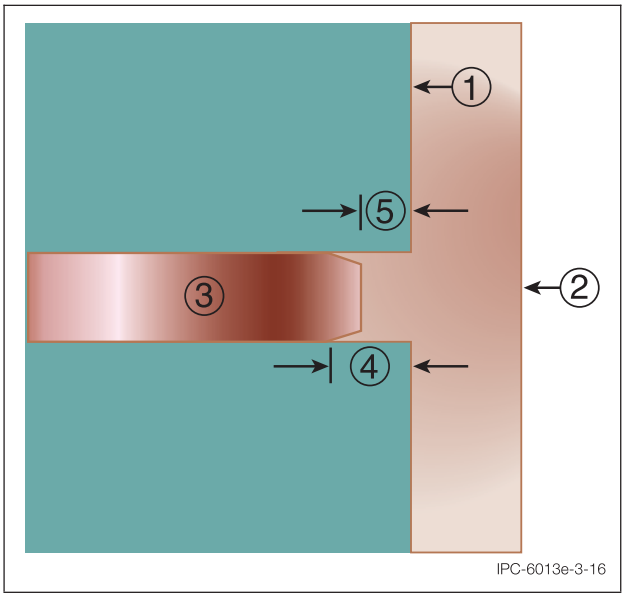


Figure 3-16 Measurement for Negative Etchback

Note 1. Drilled hole wall.
Note 2. Copper plating.
Note 3. Internal land.
Note 4. Distance "Z" **shall not** exceed:
Class 1 – 37.5 µm [1,476 µin]
Class 2 – 37.5 µm [1,476 µin]
Class 3 – 19.5 µm [768 µin]
Note 5. Distance "X" **shall not** exceed:
Class 1 – 25 µm [984 µin]
Class 2 – 25 µm [984 µin]
Class 3 – 13 µm [512 µin]

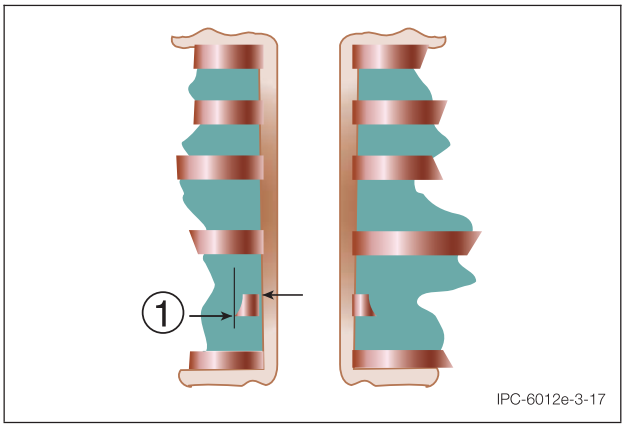


Figure 3-17 Annular Ring Measurement (Internal)
Note 1. Measurement of internal annular ring.

are configured to provide information on the interpolated annular ring remaining and pattern skew. Techniques include, but are not limited to the following:

a) The optional F or R coupon.

b) Custom designed electrically testable coupons.

c) Radiographic (x-ray) techniques.

d) Horizontal microsection.

e) CAD/CAM data analysis as correlated to pattern skew by layer.

Note: Microsectioning or statistical sampling **shall** be used to verify correlation of the approved technique, and a calibration standard established for the specific technique employed.

3.6.2.9.1 Breakout (Internal) Conditions If misregistration to the point of breakout is detected in vertical micro sections, the concerns are that:

a) The conductor width minimum may be compromised at the land junction and,

b) There is insufficient electrical spacing.

The extent and direction of misregistration **shall** be determined.

Actual printed boards or appropriate test coupons **shall** then be tested to determine compliance. This may be accomplished by the techniques listed in 3.6.2.9.

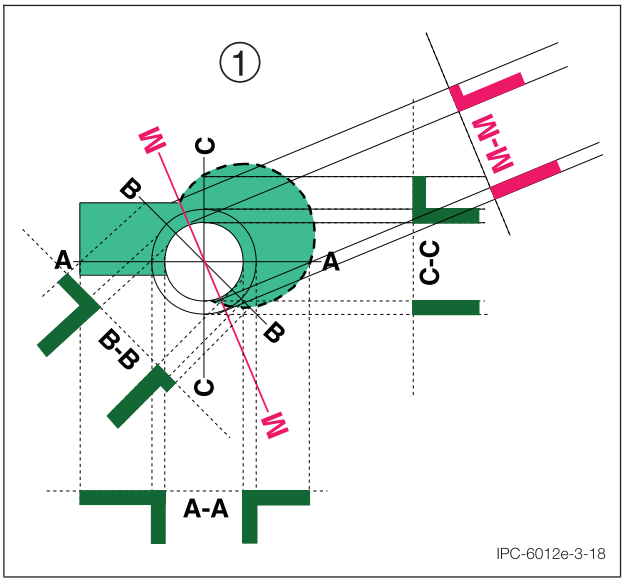


Figure 3-18 Microsection Rotations for Breakout Detection
Note 1. Only a vertical cut at M-M reveals the minimum conductor width.

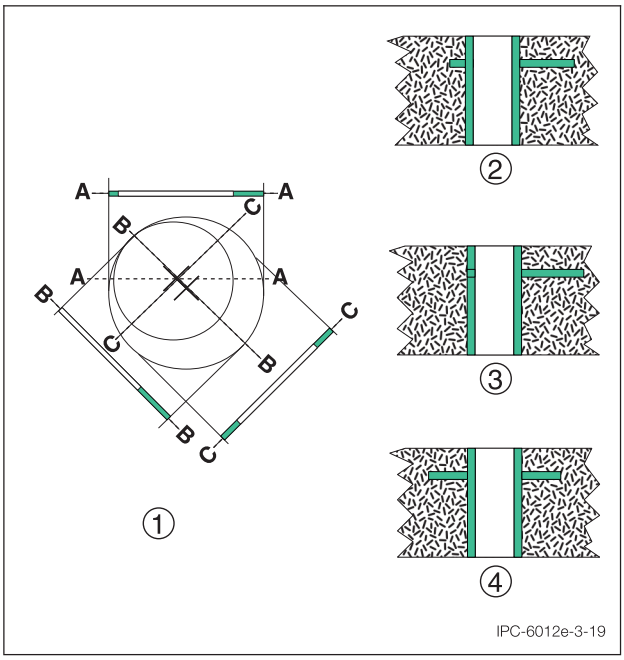


Figure 3-19 Comparison of Microsection Rotations
Note 1. Only microsection cut B-B reveals the actual annular ring reduction.
Note 2. If the mount were cut through section A-A, the microsection would look like this.
Note 3. If the mount were cut through section B-B, the microsection would look like this.
Note 4. If the mount were cut through section C-C, the microsection would look like this.

3.6.2.9.2 Microvia to Target Land Breakout in Class 1 or Class 2 product **shall** comply to the microvia contact dimension as described in 3.6.2.12. Breakout, if it occurs, **shall** neither reduce minimum spacing below that specified in 3.5.2, the minimum dielectric spacing specified in 3.6.2.18 and as shown in Figure 3-20, and/or the microvia **shall** comply to the plating thickness in accordance with 3.6.2.1. For plated copper filled microvias, the portion of plating below the target land is excluded from compliance to the plating thickness in accordance with 3.6.2.1.

3.6.2.10 Lifted Lands Lifted lands, with the exception of those in blind microvias, are allowed on the thermally stressed microsection.

3.6.2.11 Plating/Coating Thickness Based on microsection examination or on the use of suitable electronic measuring equipment, plating/coating thicknesses **shall** meet the requirements of Table 3-3 through Table 3-6. Deviations to these requirements **shall** be AABUS. Measurements in the plated hole **shall** be reported as an average thickness of 3 measurements per side of the hole, with at least one taken within approximately 40 - 60% of the hole height. Isolated thick or thin sections **shall not** be used for averaging. Isolated areas of reduced copper thickness due to glass fiber protrusions **shall** meet the minimum thickness requirements of Table 3-4 through Table 3-6 as measured from the end of the protrusion to the hole wall.

If copper thickness less than the minimum specified in Table 3-4 through Table 3-6 is detected in isolated areas, it should be considered a void and resampled in accordance with Table 4-2 using samples from the same lot to determine if the defect is random. If the additional test coupons or printed boards have no isolated areas of reduced copper thickness, the product which the test coupons or printed boards represent are considered acceptable; however, if reduced copper thickness is present in the microsections, the product **shall** be considered nonconforming.

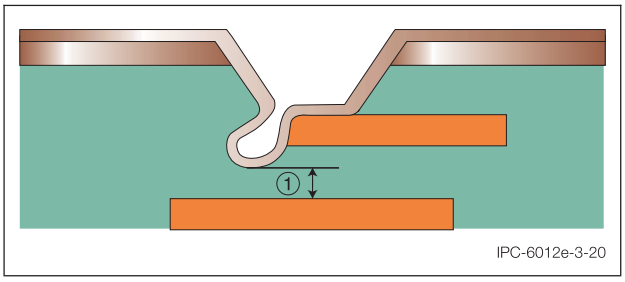


Figure 3-20 Example of Non-Conforming Dielectric Spacing Reduction Due to Breakout at Microvia Target Land

Note 1. Dielectric Spacing Reduced Below Allowable Minimum Specified in 3.6.2.18 due to Breakout

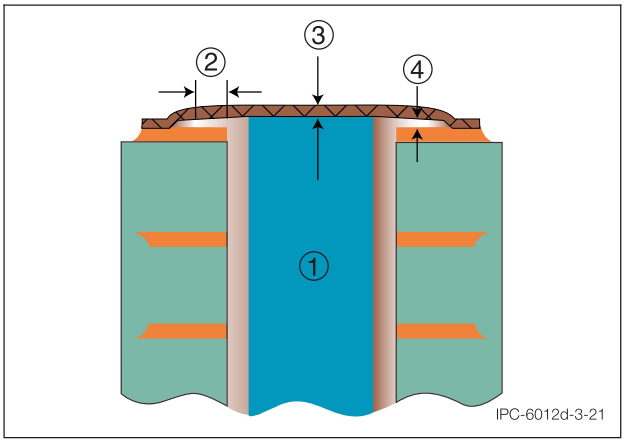


Figure 3-21 Surface Copper Wrap Measurement for Filled Holes (Over Foil)

Note 1. Fill.
Note 2. Minimum wrap distance 25 µm [984 µin].
Note 3. Cap plating, if required, over filled holes is not considered in copper wrap thickness measurements.
Note 4. Minimum copper wrap thickness.

3.6.2.11.1 Copper Wrap Plating Where an external annular ring is required, copper wrap plating minimum as specified in Table 3-4 through Table 3-6 **shall** be continuous from the plated hole onto the external surface of any plated structure and extend by a minimum of 25 µm [984 µin] (see Figure 3-21 and Figure 3-23). Copper wrap plating extending from the plated structure onto the external dielectric surface by a minimum of 25 µm [984 µin] **shall** be acceptable when specified and provided with conforming cap-plating, and free of separation at the adjacent foil edge (see Figure 3-22). Reduction of surface copper wrap plating by processing (sanding, etching, planarization, etc.) resulting in insufficient wrap plating is not allowed (see Figure 3-24 for an acceptable example and Figure 3-25 for a nonconforming example), with the exception of copper filled vias (through, blind buried and microvia) (see 3.6.2.11.3).

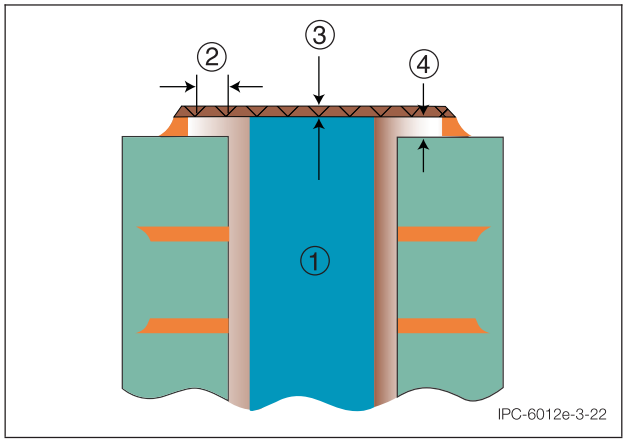


Figure 3-22 Surface Copper Wrap Measurement for Filled Holes (Over Laminate)

Note 1. Fill.
Note 2. Minimum wrap distance 25 µm [984 µin].
Note 3. Cap plating over filled holes is not considered in copper wrap thickness measurements.
Note 4. Minimum copper wrap thickness.

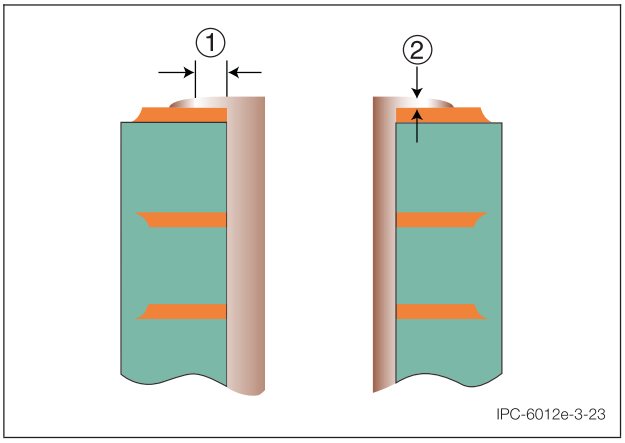


Figure 3-23 Surface Copper Wrap Measurement for Non-Filled Holes

Note 1. Minimum wrap distance 25 µm [984 µin].
Note 2. Minimum copper wrap thickness.

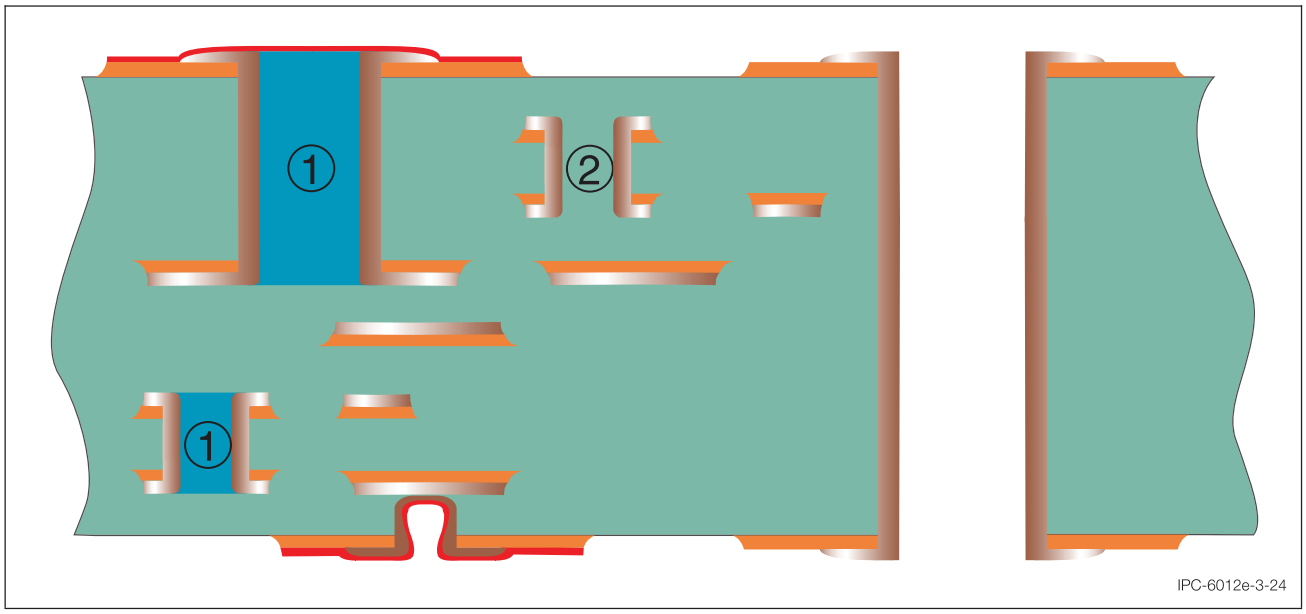


Figure 3-24 Wrap Copper (Acceptable)

Note 1. Material Fill.
Note 2. Resin Fill.

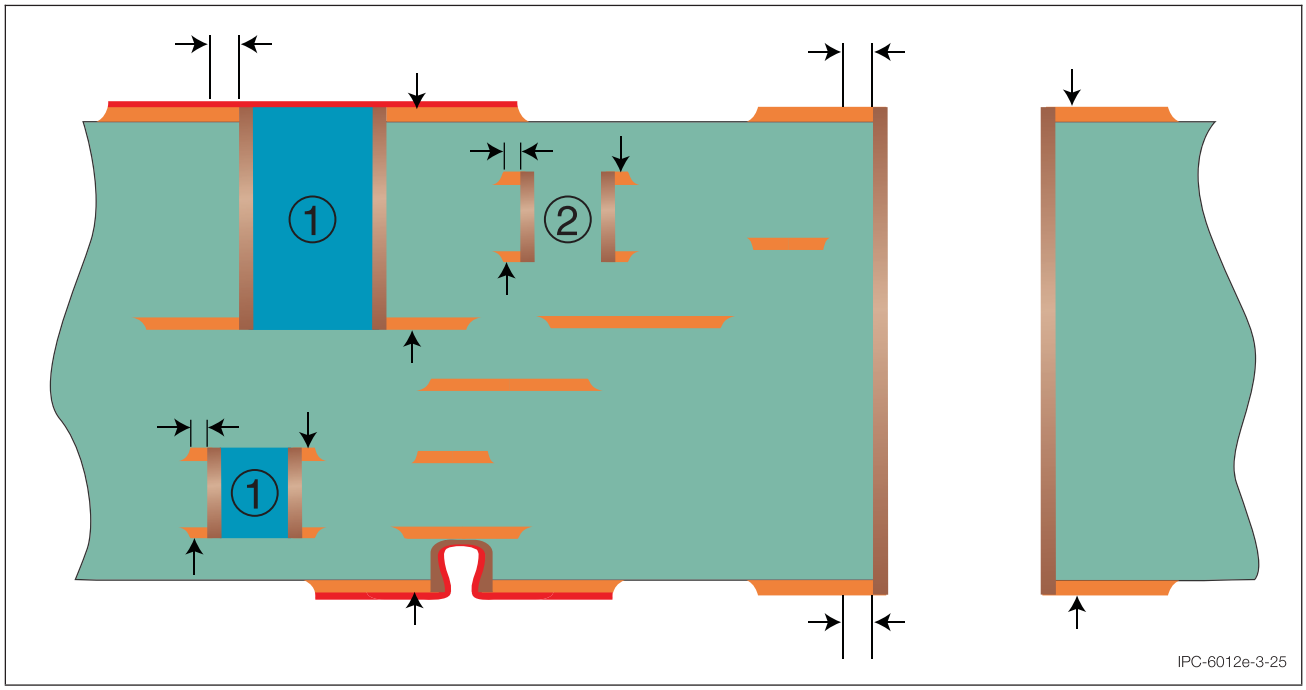


Figure 3-25 Wrap Copper Removed by Excessive Processing, e.g., Sanding/Planarization/Etching (Not Acceptable)

Note 1. Material Fill.
Note 2. Resin Fill.
Note 3. Arrows indicate where wrap copper is required but has been removed.
Note 4. Dimension lines indicate where wrap copper is required but has been removed.

3.6.2.11.2 Copper Cap Plating of Filled Holes When copper cap plating of filled holes (e.g., resin, conductive or non-conductive material) is specified by the procurement documentation, the requirements in Table 3-11 and the following **shall** apply to the outer layer surfaces or for a microvia stacked on a buried via. The copper cap plating thickness **shall** be measured as shown in Figure 3-26. The cap protrusion (bump) and depression (dimple) **shall** be measured as shown in Figure 3-27 and Figure 3-28. Voids over resin fill plated holes are not allowed (see Figure 3-29) unless covered by solder mask on the printed board (see 3.5.4.8) and the coupon.

Table 3-11 Cap Plating Requirements for Filled Holes

	Class 1	Class 2	Class 3
Copper Cap – Minimum Thickness	AABUS	5 µm [197 µin]	12 µm [472 µin]
Filled via Depression (Dimple) – Maximum[1]	AABUS	127 µm [5,000 µin]	76 µm [2,992 µin]
Filled Via Protrusion (Bump) – Maximum[1]	AABUS	50 µm [1,970 µin]	50 µm [1,970 µin]

Note 1. Does not apply to plated copper filled structures.

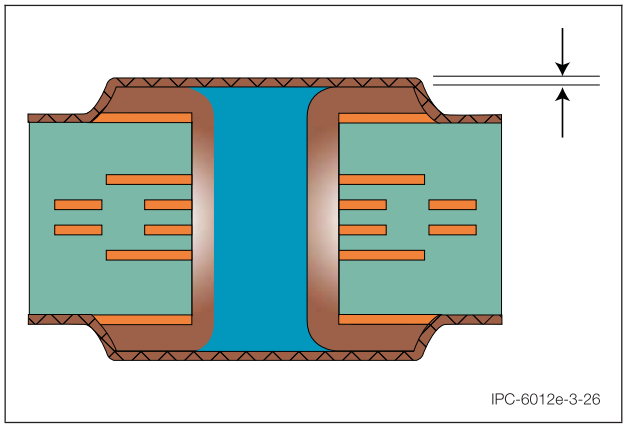


Figure 3-26 Copper Cap Thickness

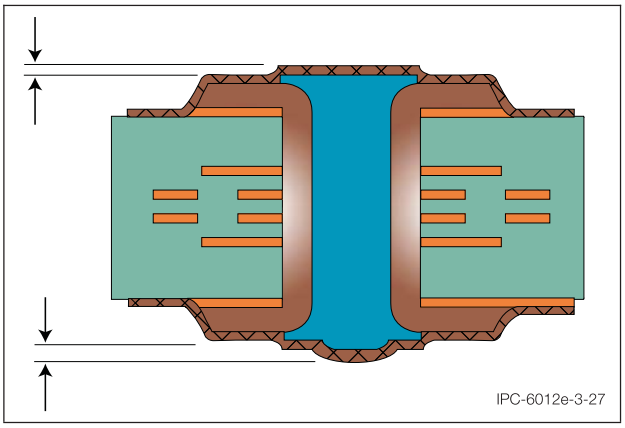


Figure 3-27 Copper Cap Filled Via Height (Bump)

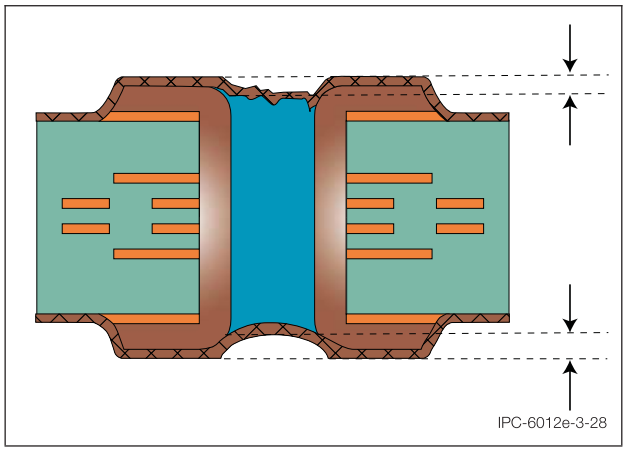


Figure 3-28 Copper Cap Depression (Dimple)

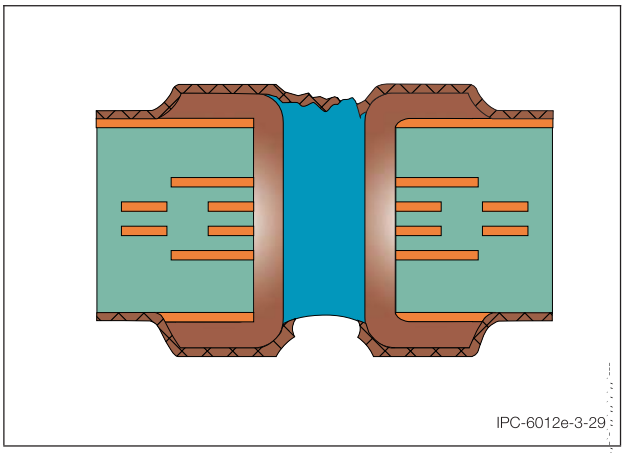


Figure 3-29 Copper Cap Plating Voids

Separation of the cap plating to underlying plating **shall not** be acceptable.

Separation of copper cap plating to fill material is acceptable. Residual via fill material as shown in Figure 3-30 and Figure 3-31 between the cap plating due to dimple(s) and the underlying plating **shall** be acceptable provided it does not extend beyond the vertical extension of the drilled hole wall.

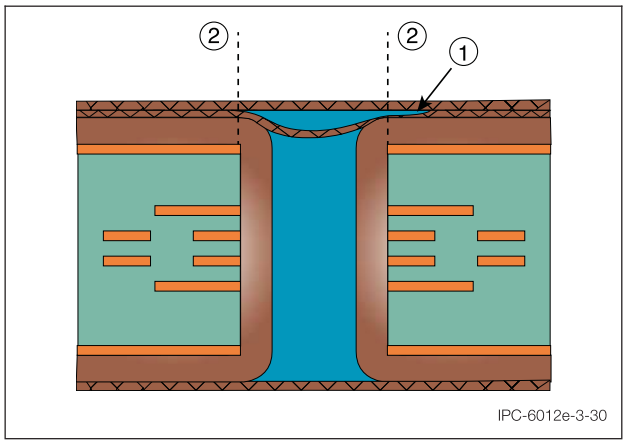


Figure 3-30 Nonconforming Via Fill Between Copper Cap Plating Layers

Note 1. Via fill material between the copper cap plating and the underlying plating (non-conforming).
Note 2. Vertical extension of the drilled hole wall.

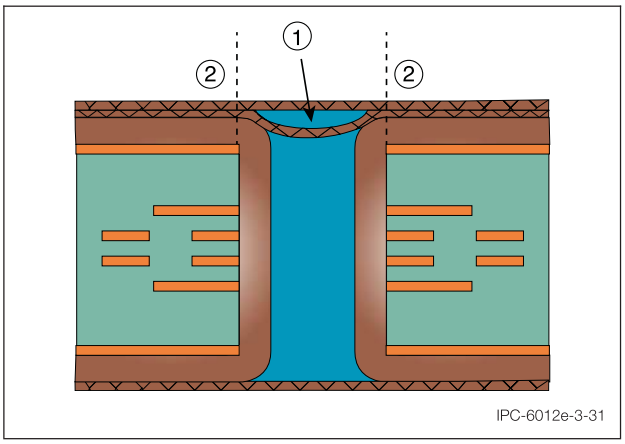


Figure 3-31 Acceptable Via Fill Between Copper Cap Plating Layers

Note 1. Via fill material between layers of copper cap plating .
Note 2. Vertical extension of the drilled hole wall.

3.6.2.11.3 Plated Copper Filled Vias (Through, Blind, Buried and Microvia) When copper filled vias are specified in the procurement documentation, vias **shall** be completely filled with copper. Voids **shall** be acceptable provided they are completely encapsulated and in total do not exceed 25% of the cross-sectional area of the filled via as shown in Figure 3-32 and Figure 3-33. The minimum plating thickness adjacent to the void **shall** meet the minimum copper thickness requirements in Table 3-4 through Table 3-6 within the "X" and "Y" dimension lines shown on Figure 1-3 and **shall not** include cap plating. Voids not fully encapsulated within these limits are not acceptable, as shown in Figure 3-34 and Figure 3-35.

Requirements for protrusions (bumps) or depressions (dimples) in blind copper filled microvias **shall** be AABUS. There are no protrusion or depression requirements for buried copper filled microvias. Via fill material between the copper filled microvia and the cap overplate **shall** be acceptable within the vertical extension of the drilled hole.

Copper filled vias are exempt from copper wrap requirements when overplated with 5 µm [0.0002 in.] minimum copper thickness. Separation of the overplate to underlying plating and copper fill **shall not** be acceptable.

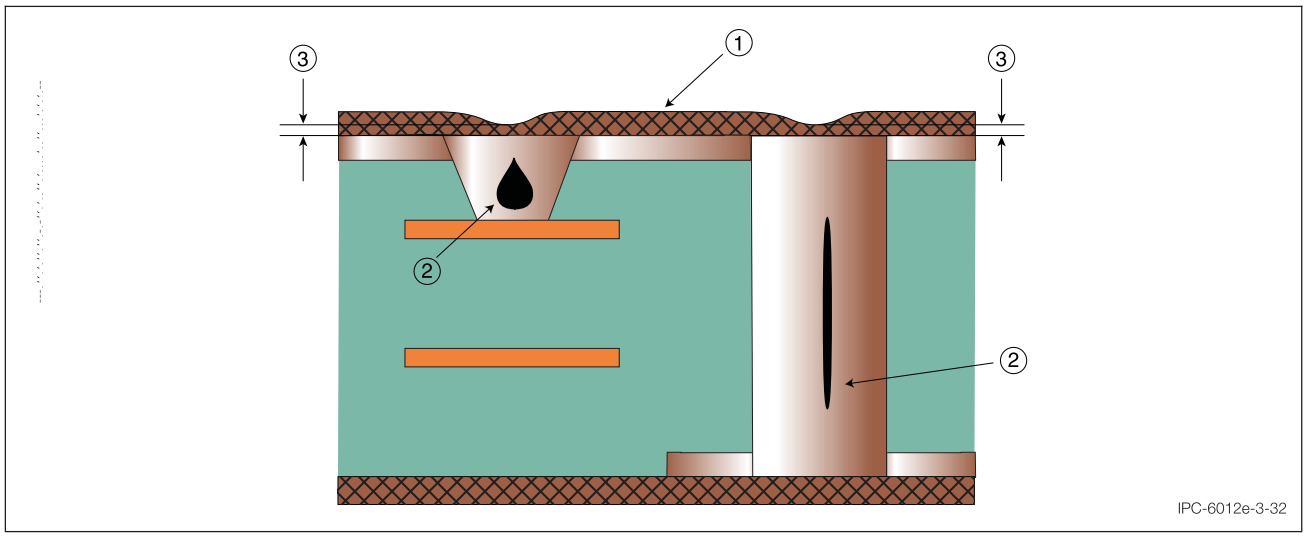


Figure 3-32 Example of Acceptable Voiding in a Cap Plated, Copper Filled Via
Note 1. Copper cap plating, if specified.
Note 2. Void/Cavity.
Note 3. Minimum Copper Overplate.

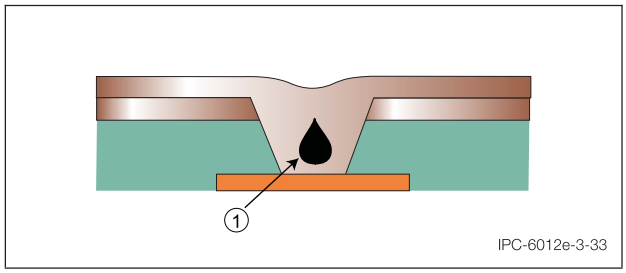


Figure 3-33 Example of Acceptable Voiding in a Copper Filled Microvia without Cap Plating
Note 1: Void/Cavity.

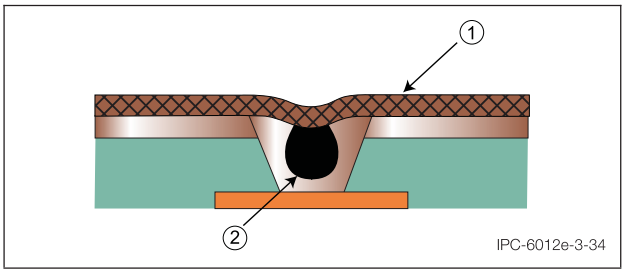


Figure 3-34 Example of Nonconforming Void in a Cap Plated, Copper Filled Microvia
Note 1: Copper cap plating, if specified.
Note 2: Void/Cavity.

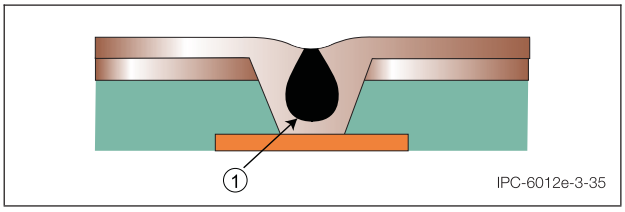


Figure 3-35 Example of Nonconforming Void in a Copper Filled Microvia
Note 1: Void/Cavity.

3.6.2.12 Microvia Target Land Contact Dimension The microvia target land contact dimension **shall** be a minimum of 50% of the microvia dimension at the capture land as defined in Figure 3-36 and Table 3-12 for laser drilled microvias. The contact dimension is the surface of the target land only; any portion of the measurement in the vertical plane created by penetration of the target land is not considered as part of this dimension. The length defined in Note 1 of Figure 3-36 is exempt from the requirements of Table 3-14.

Measure the distance between the target land contact dimension lines (see Figure 3-36 Note 1) and the distance between the microvia diameter (see Figure 3-36, Note 2) dimension lines. When measuring the target land contact dimension, the width of any foreign inclusion or the length of any separation on the target land **shall** be subtracted from the measurement in accordance with Table 3-12 and as shown in Figure 3-37. The microvia contact dimension requirements for mechanically drilled microvias **shall** be as specified in Table 3-13. Alternate measurement methods for microvia target land contact **shall** be AABUS.

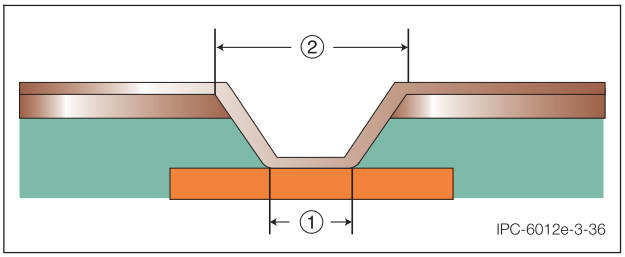


Figure 3-36 Microvia Contact Dimension
Note 1. Target Land Contact Dimension (area of contact in the vertical plane is exempt from this dimension)
Note 2. Microvia Hole Diameter at Capture Land

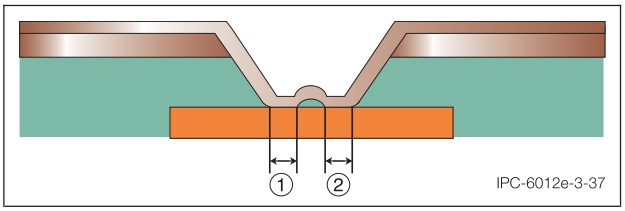


Figure 3-37 Exclusion of Separations in Microvia Target Land Contact Dimension
Note 1. The sum of 1+2 represents the microvia target land contact dimension.

Table 3-12 Microvia Contact Dimension (Laser Drilled)

Property	Class 1	Class 2	Class 3
Minimum Target Land Contact Dimension	50% Total		50% Continuous
Allowable Inclusions within the Minimum Microvia Target Land Contact Dimension	One Inclusion, not to exceed 10% of microvia hole diameter at capture land		No inclusions within the 50% contact dimension

Table 3-13 Microvia Contact Dimension (Mechanically Drilled)

Property	Class 1	Class 2	Class 3
Minimum Target Land Contact Dimension	Pierced target land to full drill diameter		
Inner layer separation (separation at the interface between internal lands and via plating)	Allowed on only one side of the plated via to target land on 20% of each layer.	None allowed.	

3.6.2.13 Microvia Target Land Piercing When microvia piercing of the target land occurs as shown in Figure 3-38 (unintended piercing) and Figure 3-39 (intentional piercing), dielectric thickness below the target land **shall not** reduce the dielectric spacing below that specified in 3.6.2.18. The area of piercing **shall** meet the requirements of 3.6.2. For laser drilled microvias, the area of piercing **shall not** be evaluated as a reduction in the microvia target land contact dimension.

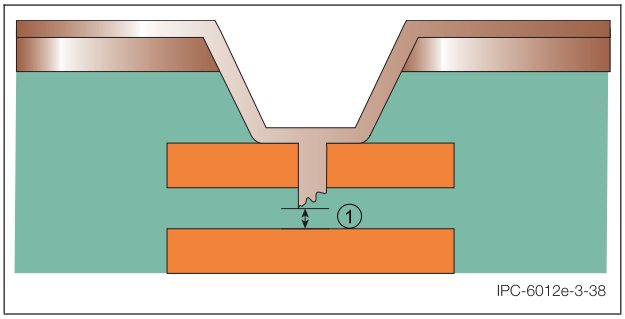


Figure 3-38 Unintended Piercing of Microvia Target Land (Laser Drilled)
Note 1. Minimum dielectric spacing **shall** be maintained.

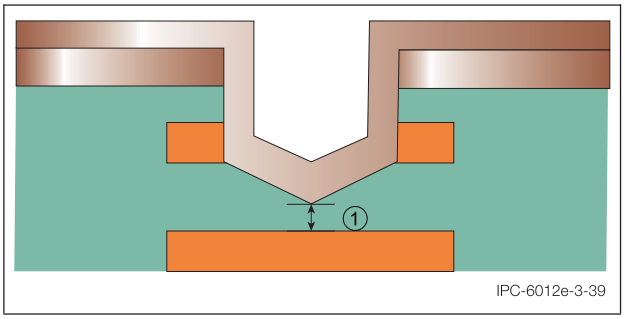


Figure 3-39 Intentional Piercing of Microvia Target Land (Mechanically Drilled[2])
Note 1. Minimum dielectric spacing **shall** be maintained.
Note 2. The shape of the bottom of the mechanical drill is dependent on the tool style used.

3.6.2.14 Minimum Internal Layer Copper Foil Thickness If the internal conductor thickness of the finished printed board is specified by a foil weight, the minimum internal copper thickness after processing **shall** be in accordance with Table 3-14 for all classes. This requirement is based on minimum copper foil thickness allowances per IPC-4562 followed by two successive scrubbings. Each scrub is expected to remove a specific amount of copper and is represented by a variable processing allowance reduction. When the procurement documentation specifies a minimum copper thickness, the conductor **shall** meet or exceed that minimum thickness.

Table 3-14 Internal Layer Foil Thickness after Processing[1]

Weight (µm) [oz./ft^2]	Absolute Cu Min. (IPC-4562 less 10% reduction) (µm) [µin] FOR REFERENCE PURPOSES ONLY[2]	Maximum Variable Processing Allowance Reduction[3] (µm) [µin] FOR REFERENCE PURPOSES ONLY	Minimum Foil Thickness after Processing (µm) [µin]
5.10 [1/8 oz.]	4.60 [181]	1.50 [59]	3.1 [122]
8.50 [1/4 oz.]	7.70 [303]	1.50 [59]	6.2 [244]
12.00 [3/8 oz.]	10.80 [425]	1.50 [59]	9.3 [366]
17.10 [1/2 oz.]	15.40 [606]	4.00 [157]	11.4 [449]
34.30 [1 oz.]	30.90 [1,217]	6.00 [236]	24.9 [980]
68.60 [2 oz.]	61.70 [2,429]	6.00 [236]	55.7 [2,193]
102.90 [3 oz.]	92.60 [3,646]	6.00 [236]	86.6 [3,409]
137.20 [4 oz.]	123.50 [4,862]	6.00 [236]	117.5 [4,626]
Above 137.20 [4 oz.]	IPC-4562 value less 10% reduction	6.00 [236]	6 µm [236 µin] below minimum thickness of calculated 10% reduction of foil thickness in IPC-4562

Note 1. This table also applies to external, non-plated layers.
Note 2. Process allowance reduction does not allow for rework processes for weights below 1/2 oz. For 1/2 oz. and above, the process allowance reduction allows for one rework process.
Note 3. For foil weights not listed in Table 3-13, the finished copper foil thickness **shall** be calculated using the following algorithms. For microns (µm) use [(34.3 X Weight) X 0.9] and for [µin] microinches use [(1.35 X Weight) X 0.9] X 1000.

3.6.2.15 Minimum Surface Conductor Thickness The minimum total (copper foil plus copper plating) surface conductor thickness for the finished printed board **shall** be in accordance with Table 3-15. When the procurement documentation specifies a minimum copper thickness for external conductors, the test coupon or printed board **shall** meet or exceed that minimum thickness. When the overall finished conductor is specified in weight rather than thickness, the minimum conductor thickness after plating **shall** be the Minimum Foil Thickness after Processing from Table 3-14 for that particular copper weight. The minimum surface conductor thickness after processing values given in Table 3-15 are determined by the following equation:

Minimum Surface Conductor Thickness = a + b - c

Where:

a = Absolute copper foil minimum (IPC-4562 nominal less 10% reduction).
b = Average copper plating thickness (e.g., 20 µm [787 µin] for Class 1 and Class 2; 25 µm [984 µin] for Class 3).
c = A maximum variable processing allowance reduction.

Table 3-15 External Conductor Thickness after Plating

Weight[1,4]	Absolute Cu Min. (IPC-4562 less 10% reduction) (µm) [µin][5]	Plus average plating for Class 1 and 2 (20 µm) [787 µin][2] FOR REFERENCE PURPOSES ONLY	Plus average plating for Class 3 (25 µm) [984 µin][2] FOR REFERENCE PURPOSES ONLY	Maximum Variable Processing Allowance Reduction[3] (µm) [µin] FOR REFERENCE PURPOSES ONLY	Minimum Surface Conductor Thickness after Processing (µm) [µin]	
					Class 1 & 2	Class 3
1/8 oz.	4.60 [181]	24.60 [967]	29.60 [1,165]	1.50 [59]	23.1 [909]	28.1 [1,106]
1/4 oz.	7.70 [303]	27.70 [1,091]	32.70 [1,287]	1.50 [59]	26.2 [1,031]	31.2 [1,228]
3/8 oz.	10.80 [425]	30.80 [1,213]	35.80 [1,409]	1.50 [59]	29.3 [1,154]	34.3 [1,350]
1/2 oz.	15.40 [606]	35.40 [1,394]	40.40 [1,591]	2.00 [79]	33.4 [1,315]	38.4 [1,512]
1 oz.	30.90 [1,217]	50.90 [2,004]	55.90 [2,201]	3.00 [118]	47.9 [1,886]	52.9 [2,083]
2 oz.	61.70 [2,429]	81.70 [3,217]	86.70 [3,413]	3.00 [118]	78.7 [3,098]	83.7 [3,295]
3 oz.	92.60 [3,646]	112.60 [4,433]	117.60 [4,630]	4.00 [157]	108.6 [4,276]	113.6 [4,472]
4 oz.	123.50 [4,862]	143.50 [5,650]	148.50 [5,846]	4.00 [157]	139.5 [5,492]	144.5 [5,689]

Note 1. Starting foil weight of design requirement per procurement documentation.
Note 2. Process allowance reduction does not allow for rework processes for weights below 1/2 oz. For 1/2 oz. and above, the process allowance reduction allows for one rework process.
Note 3. Reference: Average Cu Plating Thickness
Class 1 = 20 µm [787 µin] Class 2 = 20 µm [787 µin] Class 3 = 25 µm [984 µin]
Note 4. For copper foil above 4 oz., utilize the formula provided in 3.6.2.15.
Note 5. For foil weights not listed in Table 3-14, the finished copper foil thickness **shall** be calculated using the following algorithms. For microns (µm) use [(34.3 X Weight) X 0.9] and for [µin] microinches use [(1.35 X Weight) X 0.9] X 1000.

3.6.2.16 Overhang When the surface finish metal is used as the etch resist, overhang will result in the surface finish metal not being supported by the underlying copper and can create slivers as shown in Note 6 of Figure 3-40. The overhang of the conductor **shall not** exceed the total thickness of clad and plated copper when measured laterally.

3.6.2.17 Metal Cores The minimum lateral spacing between adjacent conductive surfaces, nonfunctional lands and/or plated holes **shall** be 100 µm [3,937 µin] (see Figure 3-41).

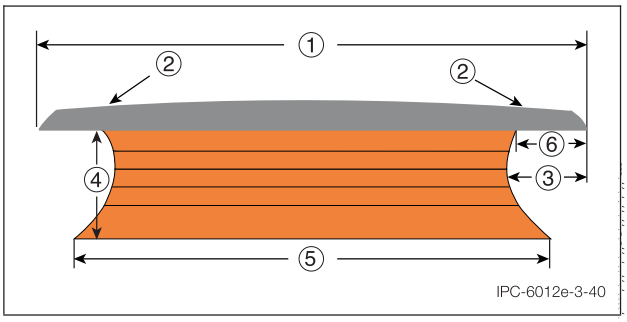


Figure 3-40 Overhang
Note 1. Conductor Width as on Production Master.
Note 2. Surface Finish (Etch Resist).
Note 3. Undercut.
Note 4. Clad plus Plated Copper.
Note 5. Conductor Width in Accordance with 3.5.1.
Note 6. Overhang.

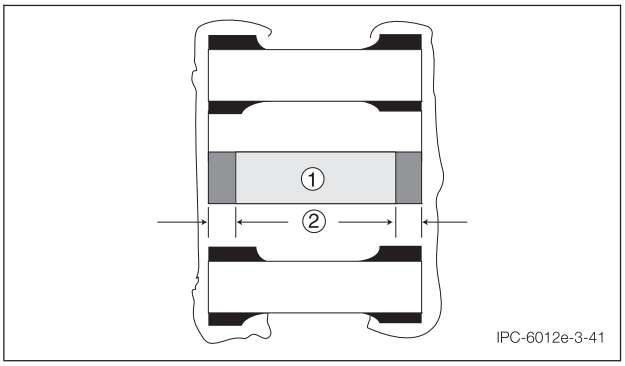


Figure 3-41 Metal Core to PTH Spacing
Note 1. Metal Core.
Note 2. Minimum Metal Core Spacing.

3.6.2.18 Dielectric Spacing The minimum dielectric spacing **shall** be specified in the procurement documentation. Figure 3-42 provides an example of a measurement technique for minimum dielectric spacing.

Note: If the minimum dielectric spacing and/or the number of reinforcing layers are not specified, the minimum dielectric spacing **shall** be 90 µm [3,543 µin] and the number of reinforcing layers **shall** be selected by the supplier to ensure the minimum dielectric spacing. Low profile copper foils should be used with dielectrics below 90 µm [3,543 µin]. When the nominal dielectric spacing on the drawing is less than 90 µm [3,543 µin], the minimum dielectric spacing is 25 µm [984 µin] and the number of reinforcing layers may be selected by the supplier. Core layers of 25 µm [984 µin] nominal or less dielectric spacing are excluded from the above requirement. Products designed for transmission line impedance applications may have special requirements and measurement methods specified within the procurement documentation.

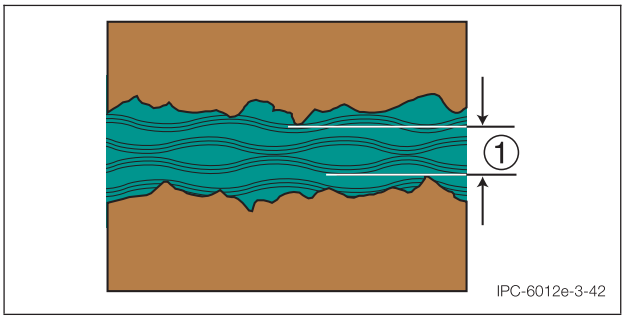


Figure 3-42 Measurement of Minimum Dielectric Spacing
Note 1. Minimum Dielectric Spacing

3.6.2.19 Material Fill of Through, Blind, Buried and Microvia Structures When specified, material fill (other than copper plating) in through, blind, buried and microvia structures are subject to the following requirements:

- Material **shall** fill a minimum of 60% of the hole for Class 2 and Class 3. Holes may be completely void of fill material for Class 1.
- When cap plating of filled holes is specified, the requirements **shall** meet 3.6.2.11.2 and Table 3-11.
- When cap plating is not specified for Class 2 and Class 3, fill material within the blind and through via **shall** seal internal voids from external surfaces and be planar with the surface within +/- 0.076 mm [0.003 in] as shown in Figure 3-43 and Figure 3-44.
- When filled back-drilled holes are employed, fill material on the back-drilled side of the hole **shall** seal internal voids from external surfaces.

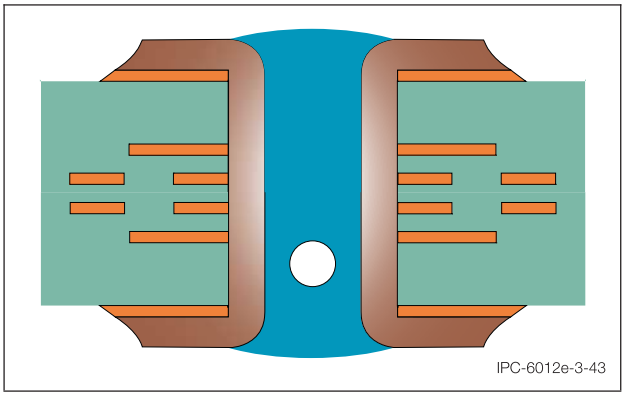


Figure 3-43 Fill Material in Blind/Through Vias When Cap Plating Not Specified

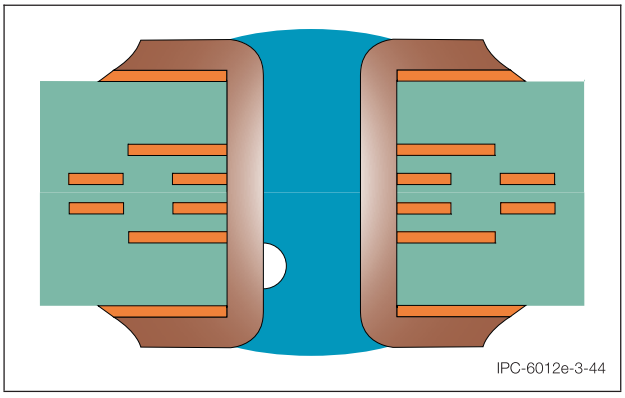


Figure 3-44 Void in Fill Material at Hole Wall Interface

3.6.2.20 Back-Drilled Holes (Microsection Evaluation) All back-drill structures with z-axis dimensional requirements in the procurement documentation **shall** be evaluated for depth and registration. Back-drilling of plated holes are subject to the following requirements:

- Back-drill **shall** be as specified in the procurement documentation. Loose or connected metal beyond the allowable stub length **shall not** be acceptable.
- Back-drill misregistration from the primary drill **shall** be acceptable provided the above requirements for loose or connected metal beyond the stub length are met.
- Isolated or connected metal (e.g., burr) within the allowable stub length **shall** be considered acceptable provided the hole is filled and minimum hole fill requirements of 3.6.2.19 are met.
- If the back-drill structure is filled and plated over, the surface plating over the back-drill portion, including any dimple, **shall not** violate the minimum dielectric spacing to the remaining stub or adjacent conductors.

Back-drill structures without z-axis dimensional requirements (e.g., pierce/do-not pierce layer) in the procurement documentation **shall** be evaluated by microsection or alternative methods such as a design specific electrical test coupon.

3.6.2.21 Nail Heading No evidence exists that nail heading affects functionality. The presence of nail heading may be considered an indicator of process or design variation but is not a cause for rejection.

3.7 Solder Mask Requirements When solder mask is required on printed boards, it **shall** meet the qualification/conformance requirements of IPC-SM-840. If a solder mask performance class is not specified for Class 1 or 2, IPC-SM-840 Class T **shall** be used. For Class 3, IPC-SM-840 Class H **shall** be used.

3.7.1 Solder Mask Coverage Solder mask coverage manufacturing variations resulting in skips, voids, and misregistration are subject to the following restrictions:

a) Metal conductors **shall not** be exposed in areas where solder mask is required (including solder dams or webs). Touch up, if required to cover these areas with solder mask, **shall** be of a material that is compatible to and of equal resistance to soldering and cleaning as the originally applied solder mask.

b) In areas containing parallel conductors, solder mask variations **shall not** expose adjacent conductors unless specified by procurement documentation/Master drawing (e.g., for a test point or surface mount device).

c) Conductors under components **shall not** be exposed or **shall** be otherwise electrically isolated. If the component pattern is not readily apparent, the area covered by a component **shall** be shown in the procurement document.

d) Solder mask need not be flush with the surface of the land. Misregistration of a solder mask defined feature **shall not** expose adjacent isolated lands or conductors.

e) Solder mask is allowed on lands for PTHs to which solder connections are to be made provided the external annular ring requirements for that Class of products are not violated; mask **shall not** encroach upon the barrel of this type of PTHs. Other surfaces such as edge printed board connector fingers and surface mount lands **shall** be free of solder mask except as specified. Solder mask is allowed in PTHs and via holes into which no component lead is soldered unless the procurement document requires that the holes be completely solder filled. Solder mask may tent or plug via holes and may be required for that purpose, provided that the maximum height is 50 µm [0.002 in] above pad. Test points that are intended for assembly testing must be free of solder mask unless coverage is specified.

f) When a land contains no PTHs, as in the case of surface mount or ball grid array lands, misregistration **shall not** cause encroachment of the solder mask on the land or lack of solder-mask-definition in excess of the following:

   1) On rectangular surface mount lands:
      - Over the land area greater than 50 µm [1,969 µin] for a pitch greater than 1.25 mm [0.04921 in];
      - Over the land area greater than 25 µm [984 µin] for a pitch between 0.65 mm [0.0256 in] and 1.25 mm [0.04921 in];
      - Solder mask encroachment for a pitch less than 0.65 mm [0.0256 in] **shall** be AABUS.

      Encroachment may occur on adjacent sides but not on opposite sides of a surface mount land.

   2) on round surface mount lands (e.g., BGA pads), if the land is solder-mask defined, misregistration may allow a 90° breakout of the solder mask on the land.

   3) on round surface mount lands (e.g., BGA pads), if the land is copper defined, no encroachment of the solder mask on the solder land is allowed except at the conductor attachment.

g) Pits, voids and bubbles are allowed in nonconductor areas provided they have adherent edges and do not exhibit lifting or blistering in excess of the allowance in 3.7.2.

h) Coverage between closely spaced surface mount lands **shall** be as required by procurement documentation.

i) When design requires coverage to the printed board edge, chipping or lifting of solder mask along the printed board edge after fabrication **shall not** penetrate more than 1.25 mm [0.04921 in] or 50% of the distance to the closest conductor, whichever is less.

3.7.2 Solder Mask Cure and Adhesion Visual assessment of the cured solder mask coating **shall not** exhibit tackiness, delamination, or blistering to the following extent:

a) Class 1 does not bridge between conductors.

b) Class 2 and Class 3 two per side, maximum size 250 µm [9,843 µin] in longest dimension and does not reduce electrical spacing between conductors by more than 25%.

Rework and touch up, if required to cover these areas with solder mask, **shall** be of a material that is compatible to and of equal resistance to soldering and cleaning as the originally applied solder mask.

When tested in accordance with IPC-TM-650, Method 2.4.28.1, the maximum percentage of cured solder mask lifting from the G coupon or printed board **shall** be in accordance with Table 3-16.

Table 3-16 Solder Mask Adhesion

Surface	Maximum Percentage Loss Allowed		
	Class 1	Class 2	Class 3
Bare Copper	10	5	0
Gold or Nickel	25	10	5
Base Laminate	10	5	0
Melting Metals (Tin-lead plating, fused tin-lead, and bright acid-tin)	50	25	10

3.7.3 Solder Mask Thickness Any requirement for the measurement of solder mask thickness **shall** be AABUS. If a thickness measurement is required, instrumental methods may be used or assessment may be made using a microsection of the parallel conductors on the E coupon or Destructive Physical Analysis (DPA) (see 3.10.12, thermal stress not required). For additional guidance on solder mask thickness measurement options, see the IPC-6012 Automotive Addendum.

3.8 Electrical Requirements When tested as specified in Table 4-3 and Table 4-4, the printed boards **shall** meet the electrical requirements detailed in the following paragraphs.

3.8.1 Dielectric Withstanding Voltage Applicable test coupons or printed boards **shall** meet the requirements of Table 3-17, without flashover, or breakdown between conductors, or conductors and lands. The dielectric withstanding voltage test **shall** be performed in accordance with IPC-TM-650, Method 2.5.7. The dielectric withstanding voltage **shall** be applied between all common portions of each conductor pattern and adjacent common portions of each conductor pattern. The voltage **shall** be applied between conductor patterns of each layer and the electrically isolated pattern of each adjacent layer. For embedded passive device capacitor materials, the dielectric withstanding voltage for adjacent plane layers that are not electrically common **shall** be per IPC-6017.

Table 3-17 Dielectric Withstanding Voltages

	Class 1	Class 2 and Class 3
Voltage for Spacing 80 µm [3,150 µin] or greater	No requirement	(500 +15 -0) V (dc)
Voltage for Spacing less than 80 µm [3,150 µin]	No requirement	(250 +15 -0) V (dc)
Time	No requirement	30 sec +3, -0

3.8.2 Electrical Continuity and Isolation Resistance Finished printed boards **shall** be tested in accordance with IPC-9252. Electrical continuity and isolation resistance testing of blind and buried structures is not required for in process checks.

3.8.3 Circuit/Plated Hole Shorts to Metal Substrate Printed boards **shall** be tested in accordance with 3.8.1 except that polarizing voltage of (500 +15 -0) V (dc) **shall** be applied between conductors and/or lands and the metal substrate (heat sink or core) in a manner such that each conductor/land area is tested (e.g., using a metallic brush or aluminum foil). The printed board **shall** be capable of withstanding (500 +15 -0) V (dc) between circuitry/plated holes and the metal core substrates. There **shall** be no flashover or dielectric breakdown.

3.8.4 Moisture and Insulation Resistance (MIR) Test coupons **shall** be tested in accordance with the procedure outlined below. The test coupon **shall not** exhibit subsurface imperfections in excess of that allowed in 3.3.2. Insulation resistance **shall** meet the minimum requirements shown in Table 3-18 (at (500 +15 -0) V (dc)). Non-component flush printed boards **shall** have a minimum requirement of 50 MΩ for all classes.

Table 3-18 Insulation Resistance

	Class 1	Class 2	Class 3
As received[1]	Maintain electrical function	500 MΩ	500 MΩ
After exposure to moisture	Maintain electrical function	100 MΩ	500 MΩ

Note 1. This measurement is taken after conformal coating material has been applied to the test coupon in accordance with IPC-TM-650, Method 2.6.3.

The moisture and insulation resistance for printed boards **shall** be performed in accordance with IPC-TM-650, Method 2.6.3. Conformal coating in accordance with IPC-CC-830 **shall** be applied to the external conductors prior to chamber exposure. Final measurements **shall** be made at room temperature within two hours after removal from the test chamber. All layers

have a 100 ± 10 V (dc) polarizing voltage applied during chamber exposure. Mealing of the conformal coating **shall not** extend more than 3.0 mm [0.12 in] from the edge of the test coupon or printed board.

3.8.4.1 Dielectric Withstanding Voltage After MIR A dielectric withstanding voltage test **shall** be performed after moisture and insulation resistance in accordance with 3.8.1.

3.9 Cleanliness Printed boards **shall** be tested in accordance with IPC-TM-650, Method 2.3.25. Equivalent methods may be used in lieu of the method specified; however it **shall** be demonstrated to have equal or better sensitivity and employ solvents with the ability to dissolve flux residue or other contaminants as does the solution presently specified. When tested in accordance with IPC-TM-650 Test Method 2.3.25, a calibrated hydrometer is not required to determine the percent alcohol in solution.

3.9.1 Cleanliness Prior to Solder Mask Application When a printed board requires a permanent solder mask coating, the uncoated printed boards **shall** be within the allowable limits of ionic and other contaminants prior to the application of solder mask coating. When noncoated printed boards are tested per 3.9, the contamination level **shall not** be greater than 1.56 µg/cm^2 of sodium chloride equivalence.

3.9.2 Cleanliness After Solder Mask, Solder, or Alternative Surface Coating Application When specified, printed boards **shall** be tested per 3.9 and meet the requirements in the procurement documentation.

3.9.3 Cleanliness of Inner Layers After Oxide Treatment Prior to Lamination The requirements to test the printed boards in accordance with 3.9 and the acceptance criteria for that testing **shall** be AABUS.

3.10 Special Requirements When specified in the procurement documentation, some or all of the special requirements listed in 3.10.1 through 3.10.15 **shall** apply. The procurement documentation and/or ordering data (see 5.1) **shall** specify which are required.

3.10.1 Outgassing The degree of Outgassing **shall** have a Total Mass Loss (TML) of less than one percent (1%) and Collectible Volatile Condensable Material (CVCM) of less than one tenth of one percent (0.1%). Mass loss **shall** be determined on test coupons or printed boards of representative substrates when tested in accordance with IPC-TM-650, Method 2.6.4.

3.10.2 Fungus Resistance Completed printed boards or representative printed board sections from the lot **shall not** support fungus growth when tested in accordance with IPC-TM-650, Method 2.6.1.

3.10.3 Vibration The test coupon or printed board **shall** pass the circuitry test in 3.8.2 following the vibration test procedure below and **shall not** exhibit bow or twist in excess of that allowed in 3.4.3 following testing.

The printed boards **shall** be subjected to both a cycling and resonance dwell test with the flat surface of the printed board mounted perpendicular to the axis of vibration in accordance with IPC-TM-650, Method 2.6.9.

Cycling Test – The cycling test **shall** consist of one sweep from 20 to 2000 Hz performed in 16 minutes. Input acceleration over the 20 to 2000 Hz frequency range **shall** be maintained to 15 Gs.

Resonance Dwell – Test coupons or printed boards **shall** be subjected to a 30 minute resonance dwell with 25 Gs input or a maximum of 100 Gs output measured at the geometric center of the test coupon or printed board. The test coupons or printed boards **shall** be restrained from movement by fixturing on all four sides.

3.10.4 Mechanical Shock The test printed boards **shall** pass the circuitry test in 3.8.2 after being subjected to mechanical shock testing as follows.

The mechanical shock test **shall** be performed in accordance with IPC-TM-650, Method 2.6.5. The printed boards **shall** be subjected three times to a shock pulse of 100 Gs with a duration of 6.5 milliseconds in each of the three principal planes. The test coupons or printed boards **shall** be restrained from movement by fixturing on all four sides.

3.10.5 Impedance Testing Requirements for impedance **shall** be AABUS. The TDR (Time Domain Reflectometer) technique in accordance with IPC-TM-650, Method 2.5.5.7 may be used to perform impedance testing on a test coupon or a designated circuit in the printed board. For large impedance tolerances, dimensional measurements from a micro-section utilizing a special test coupon may be used to calculate and verify impedance values in accordance with IPC-2251.

3.10.6 Coefficient of Thermal Expansion (CTE) When printed boards that have metal cores or reinforcements with a requirement to constrain the thermal expansion in the planar directions, the CTE **shall** be within ± 2 ppm/°C for the CTE and temperature range specified on the procurement documentation. Testing **shall** be by the strain gauge method in accordance with IPC-TM-650, Method 2.4.41.2. Testing of boards less than 1.5 mm [0.060 in] thick and other methods of determining the CTE **shall** be AABUS.

3.10.7 Thermal Shock Printed board or test coupons **shall** be tested and evaluated in accordance with IPC-TM-650, Method 2.6.7.2. Unless otherwise specified, microsectioning is not required. If microsectioning is specified, the printed boards or test coupons **shall** meet the requirements of Table 3-10 and Figure 3-10.

3.10.8 Surface Insulation Resistance (As Received) Test coupons **shall** be tested in accordance with the procedure outlined below. The insulation resistance **shall** be no less than that shown in Table 3-17.

Test coupons or printed boards should be conditioned at 50 ± 5 °C [122 ± 9 °F] with no added humidity for a period of 24 hours. After cooling, the insulation resistance test **shall** be performed in accordance with the ambient temperature measurements specified in IPC-TM-650, Method 2.6.3.7.

3.10.9 Metal Core (Horizontal Microsection) Metal core printed boards which have clearance between the plated holes and the metal core **shall** require a horizontal microsection prepared to view the metal core/hole fill insulation. Test coupons or printed boards **shall** have been subjected to thermal stress in accordance with 3.6.1 prior to microsectioning. Wicking, radial cracks, lateral spacing or voids in the hole-fill insulation material **shall not** reduce the electrical spacing between adjacent conductive surfaces to less than 100 µm [3,937 µin]. Wicking and/or radial cracks **shall not** exceed 75 µm [2,953 µin] from the plated hole edge into the hole-fill.

3.10.10 Rework Simulation

3.10.10.1 Through Hole Components Test coupons or printed boards **shall** be tested in accordance with IPC-TM-650, Method 2.4.36 and then microsectioned and examined in accordance with 3.6. Lifted lands are allowed.

3.10.10.2 Surface Mount Components Test coupons or printed boards **shall** be 100% tested.

3.10.11 Bond Strength, Unsupported Component Hole Land The unsupported component hole lands **shall** be tested in accordance with IPC-TM-650, Method 2.4.21. The unsupported component hole land **shall** withstand 2 kg or 35 kg/cm^2, whichever is less.

Calculations of land area of the unsupported hole do not include the area occupied by the hole.

3.10.12 Destructive Physical Analysis Lot acceptance **shall** require the destructive physical analysis (DPA) of a representative printed board per lot. The DPA printed board **shall** be selected from a single common inspection lot from a panel that has previously passed acceptance testing for structural integrity after stress in accordance with Table 4-3. Each DPA printed board **shall** be thermally stressed, microsectioned and inspected in accordance with 3.6. DPA microsections **shall** include a minimum of three holes for each plated hole type (e.g., through holes, filled through holes, buried, blind, microvias, etc.) on the finished printed board. For designs with less than three holes, microsection all holes. Disposition of lots where DPA has failed **shall** be AABUS.

3.10.13 Peel Strength Requirements (For Foil Laminated Construction Only) When tested as specified in IPC-TM-650, Method 2.4.8, Condition A, the surface conductor **shall** yield an average peel strength greater than or equal to the values specified by the applicable base material specification. Unless otherwise specified, the peel strength **shall** correspond to "after thermal stress" condition, and the base material thickness over 0.50 mm 0.0197 in] values specified by the base material specification. For foil types not specified, a value of 60% of the standard profile copper foil after thermal stress, for a base material thickness over 0.50 mm [0.0197 in], **shall** apply. This requirement is only applicable to foil laminated printed boards that have surface conductors or surface mount lands. The test samples **shall** have no surface finish.

3.10.14 Design Data Protection For clarification and standardization of trust requirements within the design process, a formal protocol has been developed by a collaboration between IPC and USA Department of Defense (DoD). When specified, the printed board fabricator **shall** be able to demonstrate and produce objective evidence of compliance with IPC-1791.

3.10.15 Performance Based Testing for Microvia Structures – Structural Integrity During Thermal Stress When specified, conformance testing **shall** include IPC-TM-650, Method 2.6.27. When printed boards contain microvias, a minimum of one IPC-2221, Appendix A "D" Coupon for each microvia structure **shall** be tested from each fabrication panel. When a structure includes both microvias and buried vias, the "D" coupons should include the entire structure. Results are based on resistance change and the microsection requirement of IPC-TM-650 2.6.27 does not apply.

Other performance-based test methods may be utilized in lieu of IPC-TM-650, Method 2.6.27 when specified. However, the originating D-32 Thermal Stress Test Methodology Subcommittee does not have nor ever received correlating data to validate alternative methods for detecting microvia failures.

3.11 Repair The allowance of and the requirements for repair of bare printed boards **shall** be AABUS. Unless otherwise specified by the procurement documentation, the repairs **shall** be in accordance with IPC-7711/7721.

3.11.1 Circuit Repairs Allowance of circuit repairs on Class 1, Class 2, and Class 3 printed boards **shall** be AABUS. As a guideline, there should be no more than two circuit repairs for each 0.09 m^2 or less of layer area per side. Circuit repairs on any impedance controlled circuits **shall not** violate the impedance requirement. Circuit repairs **shall not** violate the minimum electrical spacing requirements.

3.12 Rework Rework is permitted for all Classes. The touch-up of surface imperfections in the base material or removal of residual plating materials or extraneous copper will be permitted for all products when such action does not affect the functional integrity of the printed board.

4 QUALITY ASSURANCE PROVISIONS

4.1 General General Quality Assurance Provisions are specified in IPC-6011 and each sectional specification. The requirements specific to rigid printed boards are contained in this specification and include the Qualification Testing, Acceptance Testing and Frequency of Quality Conformance Testing.

4.1.1 Qualification Qualification **shall** be AABUS (see IPC-6011). The qualification should consist of capability analysis assessments (see IPC-9151), preproduction samples, production sample or test coupons that are produced by the same equipment and procedures planned for the printed boards. Qualification should include those applicable tests as referenced in Table 4-3 and Table 4-4. Qualification as AABUS may consist of documentation that the supplier has furnished similar product to other users or to other similar specifications.

4.1.2 Sample Test Coupons Sample test coupons may be used for qualification or for on-going process control. Master drawings, databases, or phototools are available from IPC. For each type defined in 1.3.2, the master drawing and artwork is listed as follows:

Type 1 Use surface layers of IPC-A-47 artwork
Type 2 Use surface layers of IPC-A-47 artwork
Type 3 Use Master Drawing IPC-100103 within IPC-A-47 artwork

Note: IPC-100001 is the universal drilling and profile master drawing. Both the IPC-100103 and IPC-100002 are part of the IPC-A-47 artwork package available in Gerber format.

Table 4-1 specifies the test coupons on the sample used for qualification and process capability evaluations. The numerical designation following each coupon, such as M5, relates to multiple instances of the coupon on the sample as indicated within IPC-A-47.

Table 4-1 Qualification Test Coupons

Test	Type 1	Types 2,3,5	Types 4, 6	Printed Board[3]
Visual[1]	All	All	All	X
Solderability				
Surface[1]	M2, M5	–	–	–
Hole[1]	–	S1,S6	S1,S6	–
Dimensional[1]	All	All	All	X
Physical				
Plating Adhesion[1]	N1, N4, N5	N1, N4, N5	N1, N4, N5	–
Bond Strength	A2, A3, A6	–	–	–
Construction Integrity				
Plated Hole Prior to Stress	–	A1, A4, A5	Design Requirement	–
Additional Dimensions	–	A1, A4, A5	Design Requirement	–
Plated Hole After Stress				
Thermal Stress	–	A1, A4, A5	Design Requirement	–
Horizontal micro (Metal Core)	–	B4, B5	A1, B4, B5	–
Rework Simulation	–	B3, B6	Design Requirement	–
Electrical Requirements				
DWV	E1, E4, E5	E1, E4, E5	E4, E5	–
Continuity	D1, D4, D5	D1, D4, D5	Design Requirement	–
Insulation Resistance	E2, E3, E6	E2, E3, E6	E3, E6	–
Environmental				
Thermal Shock	D2, D3, D6	D2, D3, D6	Design Requirement	–
Cleanliness[1]	–	–	–	X
Moisture/Insulation Resistance	E1, E4, E5	E1, E4, E5	E1, E4, E5	–
Special Requirements[2]				
Outgassing	–	–	–	X
Organic Contamination	–	–	–	X
Fungus	–	–	–	X
Vibration	–	–	–	X
Mechanical Shock	–	–	–	X
Impedance	–	H1, H2, H3	–	–
Thermal Expansion	–	–	–	X

Note 1. Not technology dependent.
Note 2. The requirement for additional test coupons **shall** be AABUS.
Note 3. An "X" in the "Printed Board" column denotes that the respective test is to be performed on the entire printed board and not on individual test coupons. The "X in this column is not to be confused with the X test coupon which is described in IPC-2221 and IPC-A-47 and used for flexural endurance testing.

4.2 Acceptance Tests Use the C=0 Zero Acceptance Number Sampling Plan specified in Table 4-2 when "Sample" is indicated in Table 4-3. Acceptance testing **shall** be performed as specified in Table 4-3 to the requirements of this specification and IPC-6011 using either test coupons and/or printed boards. The test coupons are described in IPC-2221 Appendix B, which indicates the purpose of each coupon and its frequency on a manufacturing panel.

4.2.1 C=0 Zero Acceptance Number Sampling Plan The C=0 Acceptance Number Sampling Plan provided in Table 4-2 is derived from principles established within ASQ Z1.4. The C=0 Acceptance Number Sampling Plan provides greater or equal protection for the Lot Tolerance Percent Defective (L.T.P.D.) protection at the 0.10 "consumer risk" level. The Index Value at the top of each sample size column defines the Acceptable Quality Level (AQL). For a lot to be accepted, all samples (shown in Table 4-2) **shall** conform to the requirements. Disposition of rejected lots **shall** be fully documented. For further information on the use of sampling plans refer to ASQ H1331.

4.2.2 Referee Tests Two additional microsection sets from the same panel may be prepared and evaluated for microsection nonconformances that are considered to be isolated or random in nature or caused by microsection preparation. For acceptance, both referee sets must be defect free.

4.3 Quality Conformance Testing Quality Conformance Testing **shall** consist of inspections specified in Table 4-4 in a laboratory, which meets all requirements of IPC-QL-653. Class 3 testing may be extended to reliability test and evaluation for Class 2. Inspection failures do not automatically fail or disqualify an inspection lot of printed boards; however, failure analysis **shall** be performed on all failed quality conformance inspection test coupon(s). Corrective action and customer notification **shall** be based on the failure analysis results of the failed inspection lot. Deviations to these requirements **shall** be AABUS.

4.3.1 Coupon Selection Two sets of test coupons of the most complex printed board of each type of material (primary resin system and primary reinforcement) processed during the inspection period **shall** be selected from lots that have passed acceptance testing.

Table 4-2 C=0 Sampling Plan per Lot Size[1]

Lot Size[2]	AQL Value					
	0.10	1.0	1.5	2.5	4.0	6.5
1-8	**	**	**	5	3	3
9-15	**	13	8	5	3	3
16-25	**	13	8	5	3	3
26-50	**	13	8	5	7	5
51-90	**	13	13	11	8	5
91-150	125	19	19	11	9	6
151-280	125	29	19	13	10	7
281-500	125	29	21	16	11	9
501-1,200	125	34	27	19	15	11
1,201-3,200	125	42	35	23	18	13
3,201-10,000	192	50	38	29	22	15
10,001-35,000	294	60	46	35	29	15

Note 1. Instances of "**" in this table denotes inspection of the entire lot.
Note 2. The "Remarks" column in Table 4-3 indicate whether the values in this column represent individual printed boards, panels or the entire production lot.

Table 4-3 Acceptance Testing and Frequency

Inspection	Requirement and Method Section	Sample		Test Frequency			
		Printed Board	Test Coupon By Printed Board	Class 1[1]	Class 2[1]	Class 3[1]	Remarks
Material	3.2.1-3.2.14			Manufacturer's Certification			Verifiable certificate of compliance or SPC program
Visual							
Edges of Printed Board	3.3.1	X		Sample (4.0)	Sample (2.5)	Sample (2.5)	Per Printed Board
Laminate imperfections	3.3.2	X		Sample (4.0)	Sample (2.5)	Sample (2.5)	Per Printed Board
Plating and Coating Voids in the Hole	3.3.3	X		Sample (4.0)	Sample (2.5)	Sample (1.0)	Per Printed Board
Lifted lands	3.3.4	X		Sample (6.5)	Sample (4.0)	Sample (4.0)	Per Printed Board
Marking and traceability	3.3.5	X	Coupons and Printed Board	Sample (6.5)	Sample (4.0)	Sample (4.0)	Per Printed Board
Workmanship	3.3.10	X		Sample (6.5)	Sample (4.0)	Sample (4.0)	Per Printed Board
Solderability							
Surface	3.3.6		M or W[13]	Sample (4.0)	Sample (2.5)	Sample (2.5)	Per panel
Plated Hole[7]	3.3.6		S	Sample (4.0)	Sample (2.5)	Sample (2.5)	Per panel
Dimensional							
Printed Board Dimensional	3.4	X		Sample (6.5)	Sample (4.0)	Sample (4.0)	Per Printed Board
Hole size	3.4.1	X		Sample (6.5)	Sample (4.0)	Sample (4.0)	Per Printed Board
Hole pattern accuracy	3.4.1	X		Sample (6.5)	Sample (4.0)	Sample (4.0)	Supplier certification allowed
Pattern feature accuracy	3.4.1	X		Sample (6.5)	Sample (4.0)	Sample (4.0)	Supplier certification allowed
Annular ring (external)	3.4.2	X		Sample (6.5)	Sample (4.0)	Sample (4.0)	Per panel
Bow and twist	3.4.3	X		Sample (6.5)	Sample (4.0)	Sample (4.0)	Per Printed Board
Solder mask coverage	3.7-3.7.1	X		Sample (6.5)	Sample (4.0)	Sample (4.0)	Per Printed Board
Plating/coating thickness (electronic)[2]	3.6.2.11	X	Choose coupon per plating/ coating specification	Sample (6.5)	Sample (4.0)	Sample (2.5)	Per panel
Conductor Width							
Internal	3.5.1	X		Sample (4.0)	Sample (2.5)	Sample (2.5)	Per internal panel layer
External	3.5.1	X		Sample (4.0)	Sample (2.5)	Sample (2.5)	Per Printed Board

Table 4-3 Acceptance Testing and Frequency (cont.)

Inspection	Requirement and Method Section	Sample		Test Frequency			
		Printed Board	Test Coupon By Printed Board	Class 1[1]	Class 2[1]	Class 3[1]	Remarks
Conductor Spacing							
Internal	3.5.2	X		Sample (4.0)	Sample (2.5)	Sample (2.5)	Per panel layer (minimum 5 evaluations per layer set)
External	3.5.2	X		Sample (4.0)	Sample (2.5)	Sample (2.5)	Per Printed Board
Conductive Surfaces (Surface Only)							
Edge printed board contact, junction of gold plate to solder finish	3.3.8	X		Sample (6.5)	Sample (4.0)	Sample (2.5)	Per Printed Board
Nicks, dents, pinholes	3.5.4.1	X		Sample (6.5)	Sample (4.0)	Sample (2.5)	Per Printed Board
Dewetting/ nonwetting/ surface finish coverage	3.5.4.5 3.5.4.6 3.5.4.7	X		Sample (6.5)	Sample (4.0)	Sample (2.5)	Per Printed Board
Edge printed board connector	3.5.4.4	X		Sample (6.5)	Sample (4.0)	Sample (2.5)	Per Printed Board
Surface mount	3.5.4.2	X		Sample (6.5)	Sample (4.0)	Sample (2.5)	Minimum 10 evaluations per panel
Physical							
Plating adhesion	3.3.7	X	C or N	Sample (6.5)	Sample (4.0)	Sample (4.0)	Per panel (1 coupon)
Ink Marking Adhesion	3.3.5.3	X		Sample (6.5)	Sample (4.0)	Sample (4.0)	Per panel
Solder mask cure and adhesion	3.7.2	X	G	Sample (6.5)	Sample (4.0)	Sample (4.0)	Per panel (1 coupon)
Structural Integrity After Stress Types 3-6 (Microsection)[3]							
Plating integrity	3.6.2.1		A and B or A/B	Sample (2.5)	Sample (1.5)	Sample (0.1)	Per panel
Laminate integrity	3.6.2.3 3.6.2.4 3.6.2.5		A and B or A/B	Sample (2.5)	Sample (1.5)	Sample (0.1)	Per panel
Etchback/ negative etchback	3.6 3.6.2.6 3.6.2.8		A and B or A/B	Sample (2.5)	Sample (1.5)	Sample (0.1)	Per panel
Annular ring and Breakout (internal)	3.6 3.6.2.9		A and 2B or 2 A/B	Sample (2.5)	Sample (1.5)	Sample (0.1)	Per panel[4,5]
Lifted lands	3.6.2.10		A and B or A/B	Sample (2.5)	Sample (1.5)	Sample (0.1)	Per panel
Hole plating thickness	3.6.2.11		A and B or A/B	Sample (2.5)	Sample (1.5)	Sample (0.1)	Per panel
Copper Wrap Plating	3.6.2.11.1		A and B or A/B	Sample (2.5)	Sample (1.5)	Sample (0.1)	Per panel
Copper Cap Plating	3.6.2.11.2		A and B or A/B	Sample (2.5)	Sample (1.5)	Sample (0.1)	Per panel
Copper filled Microvias	3.6.2.11.3		B	Sample (2.5)	Sample (1.5)	Sample (0.1)	Per panel

Table 4-3 Acceptance Testing and Frequency (cont.)

Inspection	Requirement and Method Section	Sample		Test Frequency			
		Printed Board	Test Coupon By Printed Board	Class 1[1]	Class 2[1]	Class 3[1]	Remarks
Microvia Target Land Contact	3.6.2.12		B	Sample (2.5)	Sample (1.5)	Sample (0.1)	Per panel
Microvia Target Land Penetration	3.6.2.13		B	Sample (2.5)	Sample (1.5)	Sample (0.1)	Per panel
Surface conductor thickness	3.6 3.6.2.15		A and B or A/B	Sample (2.5)	Sample (1.5)	Sample (0.1)	Per panel
Copper foil thickness (internal)	3.6 3.6.2.14		A and B or A/B	Sample (2.5)	Sample (1.5)	Sample (0.1)	Per panel
Metal core spacing	3.6.2.17		A and B or A/B	Sample (2.5)	Sample (1.5)	Sample (0.1)	Per panel
Dielectric thickness	3.6 3.6.2.18		A and B or A/B	Sample (2.5)	Sample (1.5)	Sample (0.1)	Per panel
Material Fill of Blind and Buried Vias	3.6.2.19		A and B or A/B	Sample (6.5)	Sample (4.0)	Sample (2.5)	Per panel
Back drill[10]	3.6.2.20		2 Custom Coupons[11,12]	Sample (2.5)	Sample (1.5)	Sample (0.1)	Per panel
Nailheading	3.6.2.21		A and B or A/B	Sample (2.5)	Sample (1.5)	Sample (0.1)	Per panel
Structural Integrity After Stress Type 2 (Microsection)[8]							
Plating integrity	3.6.2.1		B or A/B	Sample (6.5)	Sample (4.0)	Sample (2.5)	Per panel
Laminate integrity	3.6.2.3 3.6.2.4 3.6.2.5		B or A/B	Sample (6.5)	Sample (4.0)	Sample (2.5)	Per panel
Lifted lands	3.6.2.10		B or A/B	Sample (6.5)	Sample (4.0)	Sample (2.5)	Per panel
Hole plating thickness	3.6 3.6.2.11		B or A/B	Sample (6.5)	Sample (4.0)	Sample (2.5)	Per panel
Surface plating and conductor thickness	3.6 3.6.2.11 3.6.2.15		B or A/B	Sample (6.5)	Sample (4.0)	Sample (2.5)	Per panel
Electrical							
Electrical continuity and Isolation Resistance	3.8.2	X		Type 1-2[6] / Type 3-6 Sample (2.5)	Type 1-2[6] / Type 3-6 100%	Type 1-2[6] / Type 3-6 100%	Per Printed Board
Cleanliness	3.9	X		N/A	N/A	Sample (4.0)	Per lot
Cleanliness prior to solder mask application	3.9.1	X		Sample (6.5)	Sample (4.0)	Sample (4.0)	Per lot

Table 4-3 Acceptance Testing and Frequency (cont.)

Inspection	Requirement and Method Section	Sample		Test Frequency			
		Printed Board	Test Coupon By Printed Board	Class 1[1]	Class 2[1]	Class 3[1]	Remarks
Special Requirements (when specified)							
Metal core (horizontal microsection)	3.10.9	As specified by contract or master drawing (frequency of inspection **shall** be AABUS)					
Solder mask thickness	3.7.3						
Dielectric withstanding voltage	3.8.1						
Circuit/plated through shorts to metal substrate	3.8.3						
Cleanliness after surface coating application	3.9.2						
Cleanliness of inner layers after oxide treatment prior to lamination	3.9.3						
Outgassing	3.10.1						
Fungus resistance	3.10.2						
Vibration	3.10.3						
Mechanical shock	3.10.4						
Impedance testing	3.10.5						
Coefficient of thermal expansion	3.10.6						
Thermal shock	3.10.7						
Surface insulation resistance (as received)	3.10.8						
Destructive Physical Analysis	3.10.12						
Peel Strength Requirements (For Foil Laminated Constructions only)	3.10.13						
Design Data Protection	3.10.14						
Performance Based Testing for Microvia Structures	3.10.15						
Repair	3.11						
Circuit repair	3.11.1						

Table 4-3 Acceptance Testing and Frequency (cont.)

Inspection	Requirement and Method Section	Sample		Test Frequency			
		Printed Board	Test Coupon By Printed Board	Class 1[1]	Class 2[1]	Class 3[1]	Remarks

Note 1. Number in parentheses is the C=0 level.
Note 2. Choose a suitable plating/coating coupon or printed board area per Table 3-3.
Note 3. All via structures **shall** be represented in the thermally stressed evaluations. Unique construction (e.g., blind, buried, unfilled through-hole, filled through-hole, etc.) and plating steps define a via structure.
Note 4. For Class 2 product, the degree of breakout may be assessed by methods other than horizontal microsection.
Note 5. The A and 2B or 2 A/B test coupons **shall** be taken from opposite corners of the manufacturing panel and in opposing axes (one in the "x" axis and the other in the "y" axis). For each B or A/B plated hole test coupon location, the coupon **shall** be located closest to the corner of the panel (no other test coupon **shall** move the B or A/B plated hole coupon from the corner of the panel). Structural integrity sample can be used as 1/2 of the registration pair.
Note 6. For Type 1 and Type 2 printed boards, visual or AOI inspection may be used in lieu of electrical testing.
Note 7. Hole solderability testing not required for Type 2 double-sided printed boards without PTHs. The "S" coupon is the primary coupon for this inspection. The "A" coupon is considered inactive for new designs. Usage of the "A" coupon for hold solderability testing **shall** be AABUS.
Note 8. MIcrosectioning for PTH evaluation not required for Type 2 double-sided printed boards without PTHs.
Note 9. Average peel strength is calculated independently for each side of the printed board.
Note 10. Samples are not required to be thermally stressed.
Note 11. The associated originating drill sizes, back drill size and annular ring **shall** be used on the custom coupon.
Note 12. Unless otherwise specified in the procurement documentation, designs released following January 01, 2020 require that one hole per back drill depth **shall** be represented on custom back drill coupons and evaluated from opposing sides of the manufacturing panel and in opposing axes (one in the "X" axis and the other in the "Y" axis).
Note 13. "M" is a legacy coupon from IPC-2221B Appendix B. "W" is a current test coupon design from IPC-2221B Appendix A.

Table 4-4 Quality Conformance Testing[1]

Inspection	Requirement and Method Section	Test Coupon		Test Frequency		
		Type 1	Types 2-6	Class 1	Class 2	Class 3
Electrodeposited Copper Properties	3.2.6.2	Tension Test Specimen[4]	Tension Test Specimen[4]	N/A	Quarterly	Monthly
Rework simulation (when specified)	3.10.10	N/A	A[2] or A/B[2]	N/A	N/A	Monthly
Bond strength	3.10.11	A[3] or A/B[3]	N/A	N/A	Quarterly	Monthly
Peel Strength Requirements	3.10.13	P	P	N/A	N/A	Monthly
Dielectric withstanding voltage	3.8.1	E	E	N/A	Quarterly	Monthly
Moisture and insulation resistance	3.8.4	E	E	N/A	Quarterly	Monthly

Note 1. N/A = Not Applicable
Note 2. Test Coupon A or A/B contains the largest component PTH and land associated with that PTH that can be fitted to a 2.5 mm [0.0984 in] grid.
Note 3. Denotes fabricating an A or A/B coupon with an unsupported annular ring.
Note 4. Refer to ASTM E-345.

5 NOTES

5.1 Ordering Data The procurement documentation should specify the following:

a) Title, number, issue, revision letter, and date of current applicable master drawing.

b) Specific exceptions, variations, additions or conditions to this specification that are required by the user, as well as the criteria invoked by the "AABUS" requirements.

c) Part Identification and Marking instructions.

d) Information for packaging, handling and delivery (see IPC-1601 for guidelines).

e) Special tests required and frequency.

5.2 Superseded Specifications This specification supersedes and replaces IPC-6012D in the performance and requirements section.

APPENDIX A

Appendix A presents the performance requirements of IPC-6012E in an abbreviated form and alphabetical order. Special conditions, lengthy requirements, and tutorial information may be shortened or partially omitted in this appendix. See the referenced paragraph in this appendix for the full specification requirements.

Characteristic Inspection	Requirements			Requirement Paragraph
	Class 1	Class 2	Class 3	
Etched Annular Ring (External Plated Holes)	Not greater than 180° breakout of hole from land when visually assessed.	Not greater than 90° breakout of hole from land when visually assessed.	The minimum annular ring **shall** be 50 µm [1,969 µin].	3.4.2 and Table 3-9
	If filleting or keyholing have not been employed on lands, the minimum annular ring **shall** be 25 µm [984 µin].			
Etched Annular Ring (External Unsupported Holes)	Not greater than 90° breakout of hole from land when visually assessed.		The minimum annular ring **shall** be 150 µm [5,906 µin].	3.4.2 and Table 3-9
Etched Annular Ring (Internal Plated Holes)	Hole breakout is allowed provided the land/conductor junction is not reduced below the allowable width reduction in 3.5.3.1.	90° hole breakout is allowed provided the land/conductor junction is not reduced below the allowable width reduction in 3.5.3.1.	The minimum internal annular ring **shall** be 25 µm [984 µin].	3.6.2.9 and Table 3-9
	For Class 1 and Class 2 product, breakout is allowed if modified land shapes such as filleting or "keyholing" have been employed. For Class 1 and Class 2 product, if filleting or keyholing have not been employed on lands, the minimum annular ring **shall** be 25 µm [984 µin].			
Etched Annular Ring (Microvia Capture Land)	Not greater than 180° breakout of hole from land when visually assessed. The land/conductor junction **shall not** be reduced below the allowable width reduction in 3.5.3.1.	Not greater than 90° breakout of hole from land when visually assessed. The land/conductor junction **shall not** be reduced below the allowable width reduction in 3.5.3.1. The conductor junction should never be less than 50 µm [1,969 µin] or the minimum line width, whichever is smaller.	There **shall** be no evidence of breakout.	3.4.2 and Table 3-9
Etched Annular Ring (Microvia Target Land)	180° hole breakout is allowed in accordance with 3.6.2.9.2		There **shall** be no evidence of breakout.	3.6.2.9.2 and Table 3-9
Back-Drilled Holes (Visual)	There **shall** be no plating slivers, loose debris (conductive or non-conductive) or evidence of the external land remnant in the barrel or outer surface of a back-drill hole. The back-drilled hole is excluded from the edge spacing requirements of 3.3.1. Finished hole size tolerance **shall** meet the requirements of 3.4.1.			3.3.9
Back-Drilled Holes (Microsection)	Back-drilling of plated holes are subject to the following requirements: • Back-drill **shall** be as specified in the procurement documentation. Loose or connected metal beyond the allowable stub length **shall not** be acceptable. • Back-drill misregistration from the primary drill **shall** be acceptable provided the above requirements for loose or connected metal beyond the stub length are met. • Isolated or connected metal (e.g., burr) within the allowable stub length **shall** be considered acceptable provided the hole is filled and minimum hole fill requirements of 3.6.2.19 are met. • If the back-drill structure is filled and plated over, the surface plating over the back-drill portion, including any dimple, **shall not** violate the minimum dielectric spacing to the remaining stub or adjacent conductors.			3.6.2.20
Bow and Twist	Maximum of 0.75% for surface mount printed boards and 1.5% for all other printed board technologies. Finished printed boards **shall** be assessed in the delivered form.			3.4.3
Burrs and Nodules	Allowed if minimum hole diameter is met.			Table 3-10

Characteristic Inspection	Requirements			Requirement Paragraph
	Class 1	Class 2	Class 3	
Cap Plating of Filled Holes (Visual)	When cap plating of the filled hole is specified on the procurement documentation, plating voids exposing the resin fill are not allowed. Visually discernible depressions (dimples) and protrusions (bumps) over filled holes are acceptable providing the structural integrity requirements of 3.6.2.11.2 and Table 3-11 on the IPC-2221 coupons are acceptable.			3.5.4.8
Cap Plating of Filled Holes (Microsection)	When copper cap plating of filled holes (e.g., resin, conductive or non-conductive material) is specified by the procurement documentation, the requirements in Table 3-11 and the following **shall** apply to the outer layer surfaces or for a microvia stacked on a buried via: Voids over resin fill plated holes are not allowed (see Figure 3-29) unless covered by solder mask on the printed board (see 3.5.4.8) and the coupon. Separation of the cap plating to fill material is acceptable. Separation of the cap plating to underlying plating **shall not** be acceptable. Residual via fill material as shown in Figure 3-30 and Figure 3-31 between the cap plating due to dimple(s) and the underlying plating **shall** be acceptable provided it does not extend beyond the vertical extension of the drilled hole wall.			3.6.2.11.2
Circuit Repair	The allowance of and the requirements for repair of bare printed boards **shall** be AABUS. No more than two repairs for each 0.09 m^2 [0.969 ft^2]; no impedance or minimum electrical spacing requirements violated.			3.11.1
Circuits/Plated Hole Shorts to Metal Substrates	The printed board **shall** be capable of withstanding 500 volts (DC) +15, -0 between circuitry/Plated holes and the metal core substrates. There **shall** be no flashover or dielectric breakdown.			3.8.3
Cleanliness	Printed boards **shall** be tested in accordance with IPC-TM-650, Method 2.3.25. Equivalent methods may be used in lieu of the method specified; however it **shall** be demonstrated to have equal or better sensitivity and employ solvents with the ability to dissolve flux residue or other contaminants as does the solution presently specified. When tested in accordance with IPC-TM-650 Test Method 2.3.25, a calibrated hydrometer is not required to determine the percent alcohol in solution.			3.9.1
Coefficient of Thermal Expansion	When printed boards that have metal cores or reinforcements with a requirement to constrain the thermal expansion in the planar directions, the CTE **shall** be within ± 2 ppm/°C for the CTE and temperature range specified on the procurement documentation. Testing **shall** be by the strain gauge method in accordance with IPC-TM-650, Method 2.4.41.2. Testing of boards less than 1.5 mm [0.060 in] thick and other methods of determining the CTE **shall** be AABUS.			3.10.6
Color Variations in Bond Enhancement Treatment	Mottled appearance/color variation accept; Random missing areas of treatment **shall not** be > 10%.			3.3.2.9
Conductor Definition	Meet visual and dimension req., pattern and thickness as specified in procurement documentation.			3.5
Conductor Imperfections	30% of minimum specified in 10% of length or 25 mm [0.984 in], whichever is less.	20% of minimum specified in 10% of length or 13 mm [0.512 in], whichever is less.		3.5.3
	No cracks, splits or tears.			
Conductor Spacing	Minimum spacing **shall** be as specified on the drawing. Minimum conductor spacing may be reduced an additional 30% due to processing, if not specified.		Minimum spacing **shall** be as specified on the drawing. Minimum conductor spacing may be reduced an additional 20% due to processing, if not specified.	3.5.2
Conductor Surfaces				3.5.4
Conductor Thickness	If not specified, minimum conductor thickness **shall** be in accordance with 3.6.2.14 and 3.6.2.15.			3.5.1
Conductor Thickness Reduction	Reduction of conductor thickness not > 30% of minimum.	Reduction of conductor thickness not more than 20% of minimum.		3.5.3.2
Conductor Width	If not specified, minimum conductor width **shall** be 80% of conductor pattern furnished.			3.5.1
Conductor Width Reduction	Reduction of conductor width not > 30% of minimum.	Reduction of conductor width not more than 20% of minimum.		3.5.3.1

Characteristic Inspection	Requirements			Requirement Paragraph
	Class 1	Class 2	Class 3	
Copper Filled Vias, Plated (Through, Blind, Buried and Microvia)	Vias **shall** be completely filled with copper, except that voids **shall** be acceptable provided they are completely encapsulated and in total do not exceed 25% of the viewable area of the filled via as shown in Figure 3-32 and Figure 3-33. The minimum plating thickness adjacent to the void **shall** meet the minimum copper thickness requirements in Table 3-4 through 3-6 within the "X" and "Y" dimension lines shown on Figure 1-3 and **shall not** include cap plating. Requirements for protrusions (bumps) or depressions (dimples) in blind copper filled microvias **shall** be AABUS. There are no requirements for buried copper filled microvias. Via fill material between the copper filled microvia and the cap over plate **shall** be acceptable within the vertical extension of the drilled hole. Copper filled vias are exempt from copper wrap requirements when overplated with 5 µm [0.0002 in.] minimum copper thickness. Separation of the overplate to underlying plating and copper fill **shall not** be acceptable.			3.6.2.11.3
Copper Purity Elongation and Tensile Strength	Purity **shall** be no less than 99.5% pure, tensile strength not less than 248 MPa [36,000 PSI], elongation not less than 12%.			3.2.6.2
Copper Wrap Plating	Where an external annular ring is required, copper wrap plating minimum as specified in Table 3-4 through Table 3-6 **shall** be continuous from the plated hole onto the external surface of any plated structure and extend by a minimum of 25 µm [984 µin] (see Figure 3-21 and Figure 3-23). Copper wrap plating extending from the plated structure onto the external dielectric surface by a minimum of 25 µm [984 µin] **shall** be acceptable when specified and provided with conforming cap-plating, and free of separation at the adjacent foil edge (see Figure 3-22). Reduction of surface copper wrap plating by processing (sanding, etching, planarization, etc.) resulting in insufficient wrap plating is not allowed (see Figure 3-24 for an acceptable example and Figure 3-25 for a nonconforming example), with the exception of copper filled vias (through, blind buried and microvia) (see 3.6.2.11.3).			3.6.2.11.1
Cracks, Barrel/Corner	None allowed for Class 1, 2 and 3.			Table 3-10
Cracks, External Foil	Class 1 - "D" Cracks not allowed. "A" and "B" cracks allowed. Class 2 and Class 3 - "D" and "B" cracks not allowed. "A" cracks allowed.			Table 3-10
Cracks, Internal Foil	"C" cracks allowed on only one side of hole provided cracks do not extend through foil thickness.	None allowed.		Table 3-10
Cracks, Laminate	Boundary line cracks that overlap into a thermal zone **shall not** be in excess of 150 µm [5,906 µin] for Class 1 products.	Boundary line cracks that overlap into a thermal zone **shall not** be in excess of 80 µm [3,150 µin] for Class 2 or Class 3 products.		3.6.2.4
	Laminate cracks between conductive patterns that are not electrically common in a thermal zone (see Figure 3-13) **shall not** reduce the conductor spacing below the minimum in the horizontal direction or the minimum dielectric spacing in the vertical direction. Multiple cracks between two adjacent plated holes in the same plane **shall not** have a combined length which exceeds these limits.			
Crazing	Imperfection does not reduce the conductor spacing below the minimum and there is no propagation of the imperfection as a result of thermal testing that replicates the manufacturing process. For Class 2 and 3, the distance of crazing **shall not** span more than 50% of the distance between adjacent conductors.			3.3.2.2
Delamination/ Blistering (Visual)	Acceptable for all classes of end product provided the area affected by imperfections does not exceed 1% of the printed board area on each side and does not reduce the spacing between conductive patterns below the minimum conductor spacing. There **shall** be no propagation of imperfections as a result of thermal testing that replicates the manufacturing process. For Class 2 and 3, the blister or delamination **shall not** span more than 25% of the distance between adjacent conductive patterns.			3.3.2.3
Delamination or Blistering (Microsection)	If present evaluate entire printed board per 3.3.2.3.	No evidence of delamination or blistering.		3.6.2.5
Dewetting	Solder connection: 15%.	Solder connection: 5%.		3.5.4.5
	Conductors and planes are permitted.			

Characteristic Inspection	Requirements			Requirement Paragraph
	Class 1	Class 2	Class 3	
Dielectric Thickness	The minimum dielectric spacing **shall** be specified in the procurement documentation. If the minimum dielectric spacing and/or the number of reinforcing layers are not specified, the minimum dielectric spacing **shall** be 90 µm [3,543 µin] and the number of reinforcing layers **shall** be selected by the supplier to ensure the minimum dielectric spacing. Core layers of 25 µm [984 µin] nominal or less dielectric spacing are excluded from the above requirement.			3.6.2.18
Dielectric Removal	125 µm [4,921 µin] wicking allowance plus maximum etchback or smear removal allowance	100 µm [3,937 µin] wicking allowance plus maximum etchback or smear removal allowance	80 µm [3,150 µin] wicking allowance plus maximum etchback or smear removal allowance	Table 3-10 and Figure 3-15
Dielectric Withstand Voltage	No requirement.	Spacing 80 µm [3,150 µin] or greater, 500 Vdc Time: 30 sec (+3, -0) Spacing less than 80 µm [3,150 µin], 250 Vdc Time: 30 sec (+3, -0)		3.8.1 and Table 3-17
Disrupted Fibers	Disrupted fibers are acceptable for all Classes provided the imperfection does not bridge conductors and does not reduce the remaining lateral conductor spacing below the minimum.			3.3.2.6
Dimensional Requirements	AABUS.			3.4
Edge Printed Board Contact, Junction of Gold Plate to Solder Finish	Max copper gap: 2.5 mm [0.0984 in]	Max copper gap: 1.25 mm [0.04921 in]	Max copper gap: 0.8 mm [0.031 in]	3.3.8
Edge Printed Board Contact, Junction of Gold Plate to Solder Finish	Max gold overlap: 2.5 mm [0.0984 in]	Max gold overlap: 1.25 mm [0.04291 in]	Max gold overlap: 0.8 mm [0.031 in]	3.3.8
Edge Connector Lands	No cuts or scratches that expose nickel or copper; Pits, dents, or depressions accept if not exceed 150 µm [5,906 µin] in longest dimension with no more than three per land, and not appear in > 30% of lands.			3.5.4.4
Edges (Visual)	When edge spacing is designed in accordance with IPC-2222, nicks or crazing along the edge of the printed board, edges of cutouts and edges of non-plated holes are acceptable provided the penetration does not exceed the specified minimum distance between printed board edge and conductive pattern. If no edge spacing requirement is specified, any nicks or crazing **shall not** exceed 50% of the distance from the edge to the nearest conductor or 2.5 mm [0.0984 in], whichever is less. When edge spacing is designed in accordance with IPC-2222, the distance between the haloing penetration and the nearest conductive feature **shall not** be less than the minimum lateral conductor spacing, or 100 µm [3,937 µin] if not specified. When edge spacing is not designed in accordance with IPC-2222, evaluations for nicks, crazing, and haloing **shall** be AABUS.			3.3.1
Electrical Requirements				3.8
Electrical Continuity and Isolation Resistance	Finished printed boards **shall** be tested in accordance with IPC-9252. Electrical continuity and isolation resistance testing of blind and buried structures is not required for in process checks.			3.8.2
Etchback (When Specified)	Between 5 µm [197 µin] and 80 µm [3,150 µin] with a preferred depth of 13 µm [512 µin]. Shadowing is permitted on one side of each land. The combination of dielectric removal from etchback plus wicking allowance (wicking and random tears or drill gouges resulting from hole formation and/or hole cleaning) **shall not** exceed the sum of the maximum allowable etchback or smear removal and the maximum allowable wicking limits in Table 3-10 and as depicted in Figure 3-15.			3.6.2.6
Surface Finish and Coating Thickness	See Table 3-3.			3.6.2.11, Table 3-3
Surface Finish Coverage (Areas not to be Soldered)	Exposed basis metal(s) on areas not to be soldered is permitted on 1% of the conductive surfaces for Class 3 and 5% of the surfaces for Class 1 and Class 2. Coverage does not apply to vertical conductor and plane edges. Rework of up to 5% exposed of a basis metal not to be soldered is allowed by brush plate in accordance with SAE AMS-2451.			3.5.4.7.1
Foreign Inclusions	Translucent and other particles acceptable provided the particle does not reduce the spacing between adjacent conductors to below the minimum spacing specified in 3.5.2.			3.3.2.4

Characteristic Inspection	Requirements			Requirement Paragraph
	Class 1	Class 2	Class 3	
Fungus Resistance	No fungus growth when tested in accordance with IPC-TM-650, Method 2.6.1.			3.10.2
Haloing	When edge spacing is designed in accordance with IPC-2222, the distance between the haloing penetration and the nearest conductive feature **shall not** be less than the minimum lateral conductor spacing, or 100 µm [3,937 µin] if not specified. When edge spacing is not designed in accordance with IPC-2222, evaluations for haloing **shall** be AABUS.			3.3.1
Hole Size and Hole Pattern Accuracy	AABUS. Applicable design series requirements **shall** apply if not specified.			3.4.1
Hot Air Solder Leveling	The solder coating **shall** be as specified on the master drawing and the procured solder used for coating **shall** meet the requirements of J-STD-006. HASL is the process for solder coating that involves dipping a printed board into solder and using hot air to level the resultant solder surface. The frequency of analysis for the HASL solder pot to the limits of Table 3-2 as reprinted from IPC-J-STD-001 **shall** be determined on the basis of Statistical Process Control (SPC) data or monthly analyses. Records containing the results of all analyses and solder bath usage (e.g., total time in use, amount of replacement solder, or area throughput) **shall** be maintained for a minimum of one year for each process/system. The percentage of each element in an alloy **shall** be determined by any standard analytical procedure with sufficient resolution. If contamination exceeds the limits, intervals between the analyses, replacement or replenishment **shall** be shortened.			3.2.7.3
Impedance Testing	Requirements for impedance **shall** be AABUS. The TDR (Time Domain Reflectometer) technique in accordance with IPC-TM-650, Method 2.5.5.7 may be used to perform impedance testing on a test coupon or a designated circuit in the printed board.			3.10.5
Inclusions, Inner layer (Inclusions Between Interface of Internal Land and Plated Hole)	Allowed on only one side of hole wall at each land location on 20% of each available land.	None allowed.		Table 3-10
Insulation Resistance (As Received)	As received: Maintain electrical function.	As received: 500 megohms.		3.10.8 and Table 3-17
	After exposure to moisture: Maintain electrical function.	After exposure to moisture: 100 megohms.	After exposure to moisture: 500 megohms.	3.8.4 and Table 3-18
Laminate Integrity	See Voids, Laminate.			3.6.2.3
Lifted Lands (Microsection)	Lifted lands, with the exception of those in blind microvias, are allowed on the thermally stressed microsection.			3.6.2.10
Lifted Lands (Visual)	No lifted lands on the delivered (non-stressed) printed board.			3.3.4
Marking (Visual)	Conductive marking must be compatible with materials, and not reduce electrical spacing requirements. For lead-free end product, the labeling requirements of J-STD-609 **shall** be met. Requirements for etched markings are provided in 3.3.5.1. Requirements for marking inks are provided in 3.3.5.2. Ink marking adhesion **shall** be tested in accordance with IPC-TM-650 Method 2.4.1. There **shall** be no evidence of the marking ink being removed.			3.3.5
Material				3.2
Material Fill of Through, Blind, Buried and Microvia Vias	Material fill (other than copper plating) in through, blind, buried and microvia structures are subject to the following requirements: • Material **shall** fill a minimum of 60% of the hole for Class 2 and Class 3. Holes may be completely void of fill material for Class 1. • When cap plating of filled holes is specified, the requirements **shall** meet 3.6.2.11.2 and Table 3-11. • When cap plating is not specified for Class 2 and Class 3, fill material within the blind and through via **shall** seal internal voids from external surfaces and be planar with the surface within +/- 0.076 mm [0.003 in] as shown in Figure 3-43 and Figure 3-44. • When filled back-drilled holes are employed, fill material on the back-drilled side of the hole **shall** seal internal voids from external surfaces. • When cap plating is not specified, voids that extend from either external surfaces **shall not** be allowed.			3.6.2.19

Characteristic Inspection	Requirements			Requirement Paragraph
	Class 1	Class 2	Class 3	
Measling	Measling is acceptable for Class 1, Class 2 and Class 3 end product. Measled areas in laminate substrates exceeding 50% of the spacing between non-common conductors are a process indicator for Class 3 end product, indicating a variation in material, equipment operation, workmanship or process that is not a defect.			3.3.2.1
Mechanical Shock	Printed board **shall** pass test requirements of 3.8.2 after mechanical shock.			3.10.4
Metal Cores, Horizontal Microsection	Wicking, radial cracks, lateral spacing, or voids in the hole-fill insulation material **shall not** reduce electrical spacing between adjacent conductive surfaces to < 100 µm [3,937 µin]. Wicking and/or radial cracks **shall not** exceed 75 µm [2,953 µin] from the plated hole edge into the hole-fill.			3.10.9
Metal Core, Internal Spacing	The minimum lateral spacing between adjacent conductive surfaces, nonfunctional lands and/or plated holes **shall** be 100 µm [3,937 µin].			3.6.2.17
Microvia to Target Land	Breakout in Class 1 or Class 2 product **shall** comply to the microvia contact dimension as described in 3.6.2.12. Breakout, if it occurs, **shall** neither reduce minimum spacing below that specified in 3.5.2, the minimum dielectric spacing specified in 3.6.2.18 and as shown in Figure 3-20, and/or the microvia **shall** comply to the plating thickness in accordance with 3.6.2.1.			3.6.2.9.2
Microvia Target Land Contact Dimension	The microvia target land contact dimension **shall** be greater than 50% of the microvia capture land dimension as defined in Figure 3-36 and Table 3-12 for laser drilled microvias The target land contact dimension minimum is 50% of the microvia hole diameter dimension. When measuring the target land contact dimension, the width of any foreign inclusion or the length of any separation on the target land **shall** be subtracted from the measurement in accordance with Table 3-12 and as shown in Figure 3-37. The microvia contact dimension requirements for mechanically drilled microvias **shall** be as specified in Table 3-13.			3.6.2.12
Microvia Target Land Penetration	When microvia piercing of the target land occurs as shown in Figure 3-38 (unintended piercing) and Figure 3-39 (intentional piercing), dielectric thickness below the target land **shall not** reduce the dielectric spacing below that specified in 3.6.2.18. The area of piercing **shall** meet the requirements of 3.6.2. For laser drilled microvias, the area of piercing **shall not** be evaluated as a reduction in the microvia target land contact dimension.			3.6.2.13
Minimum Internal Layer, Copper Foil Thickness	See Table 3-14.			3.6.2.14
Minimum Surface Conductor Thickness	See Table 3-15. When the overall finished conductor is specified in weight rather than thickness, the minimum conductor thickness **shall** be the Minimum Foil Thickness after Processing from Table 3-14 for that particular copper weight.			3.6.2.15
Moisture and Insulation Resistance	No measling, blistering or delamination in excess of that allowed in 3.3.2; insulation resistance meet requirements of Table 3-18; moisture and insulation resistance testing according to IPC-TM-650, Method 2.6.3.			3.8.4
Nail Heading	Acceptable			3.6.2.21
Negative Etchback	Distance “X” not to exceed 25 µm [984 µin] if etchback not specified on procurement documentation.		Distance “X” not to exceed 13 µm [512 µin] if etchback not specified on procurement documentation.	3.6.2.8 and Figure 3-16
	Distance “Z” not to exceed 37.5 µm [1,476 µin] if etchback not specified on procurement documentation.		Distance “Z” not to exceed 19.5 µm [768 µin] if etchback not specified on procurement documentation.	
	When negative etchback results in folds or inclusions in the copper plating, the copper thickness **shall** meet the minimum requirements as measured from the face of the internal layer as shown in Figure 3-12.			
Nicks and Pinholes in Ground or Voltage Planes	Maximum size 1.5 mm [0.0591 in] with not more than six per side, per 625 cm^2	Maximum size 1.0 mm [0.0394 in] with not more than four per side, per 625 cm^2.		3.5.4.1
Nonfunctional Lands	A fabrication **shall not** remove nonfuctional lands without specific approval of the design activity or unless allowed within the procurement documentation.			3.5.4.10
Nonwetting	For tin, tin/lead reflowed, or solder coated surfaces, not permitted on any conductive surface where a solder connection will be required.			3.5.4.6

Characteristic Inspection	Requirements			Requirement Paragraph
	Class 1	Class 2	Class 3	
Outgassing	Testing in accordance to procurement documentation; not resulting in a weight loss of more than 0.1%.			3.10.1
Overhang	When the surface finish metal is used as the etch resist, overhang will result in the surface finish metal not being supported by the underlying copper and can create slivers as shown in Note 6 of Figure 3-40. The overhang of the conductor **shall not** exceed the total thickness of clad and plated copper when measured laterally.			3.6.2.16
Peel Strength (Foil Laminated Constructions Only)	When tested as specified in IPC-TM-650, Method 2.4.8, Condition A, the surface conductor **shall** yield an average peel strength greater than or equal to the values specified by the applicable base material specification. Unless otherwise specified, the peel strength **shall** correspond to "after thermal stress" condition, and the base material thickness over 0.50 mm 0.0197 in] values specified by the base material specification. For foil types not specified, a value of 60% of the standard profile copper foil after thermal stress, for a base material thickness over 0.50 mm [0.0197 in], **shall** apply. The test samples **shall** have no surface finish.			3.10.13
Pink Ring	Acceptable.			3.3.2.10
Plating Adhesion	No portion of protective plating or conductor pattern foil **shall** be removed. Testing in accordance with IPC-TM-650, Method 2.4.1.			3.3.7
Plating Folds, Inclusions	The minimum copper thickness in Table 3-4 through Table 3-6 **shall** be met. For positive etchback, measurements should follow the topography of the dielectric. When negative etchback results in folds in the copper plating, the copper thickness **shall** meet the minimum requirements as measured from the face of the internal layer (see Figure 3-12); negative etchback limits **shall not** be exceeded.			Table 3-10
Plating Integrity, Plated Holes	Properties specified in Table 3-10. Microanomalies at the interface of plating and foil (excluding interconnects) that do not propagate as a result of thermal stress **shall** be an indicator of process variation but is not a cause for rejection.			3.6.2.1
Plating Thickness, Copper, Through, Blind, Buried Vias > 2 layers	Avg. 20 µm [787 µin] Min. Thin areas 18 µm [709 µin]		Avg. 25 µm [984 µin] Min. Thin areas 20 µm [787 µin]	3.6.2.11, Table 3-4
Plating Thickness, Copper, Blind and Buried Microvias	Avg. 12 µm [472 µin] Min. Thin areas 10 µm [394 µin]			3.6.2.11, Table 3-5
Plating Thickness, Copper, Buried Via Cores (2 layers)	Avg. 13 µm [512 µin] Min. 11 µm [433 µin]	Avg. 15 µm [592 µin] Min. Thin areas 13 µm [512 µin]		3.6.2.11, Table 3-6
Plating and Coating Voids in the Hole (Visual)	Copper: three voids allowed per hole in not more than 10% of holes.	Copper: one void allowed per hole in not more than 5% of holes.	Copper: none allowed.	3.3.3, Table 3-7
	Finished Coating: five voids allowed per hole in not more than 15% of holes.	Finished Coating: three voids allowed per hole in not more than 5% of holes.	Finished Coating: one void allowed per hole in not more than 5% of holes.	
Copper Plating Voids	Meet requirements established in Table 3-10.	• No more than one void per specimen, regardless of length or size. • No plating void in excess of 5% of total printed board thickness. • No plating voids evident at interface of an internal conductive layer and the plated hole wall or microvia wall. • No circumferential plating voids greater than 90°.		3.6.2.2
Repair	AABUS. The repairs **shall** be in accordance with IPC-7711/21.			3.11
Rework	Does not affect functional integrity of printed board.			3.12
Scratches, Dents, and Tool Marks	Do not bridge conductors or expose fibers greater than that allowed in 3.3.2.4 and 3.3.2.5, and do not reduce dielectric spacing below minimum.	3.3.2.7		

Characteristic Inspection	Requirements			Requirement Paragraph
	Class 1	Class 2	Class 3	
Separation Along Vertical Edge of External Land	Allowed at knee (see Figure 3-11), maximum length 130 µm [5, 118 µin].	Allowed provided the separation does not extend beyond the vertical edge of the external copper foil.		Table 3-10
Separation, Inner layer (Separation at the Interface Between Internal Lands and Through-Hole Plating	Allowed on only one side of hole wall at each land location on 20% of each available land.	None allowed.		Table 3-10
Separation, Plating	None allowed.			Table 3-10
Smear Removal	Smear removal **shall** be sufficient to meet the acceptability criteria for inner layer separation per Table 3-10. Smear removal **shall not** exceed 25 µm [984 µin]. The combination of smear removal, drill gouges, random tears, and hole formation **shall not** exceed the dielectric removal limits in Table 3-10 as shown in Figure 3-15. Smear removal is not required of Type 1 or Type 2 printed boards. Measurement for maximum dielectric removal is depicted in Figure 3-15.			3.6.2.7
Solder Mask				3.7
Solder Mask Coverage	Conductors not to be exposed or bridged by blisters in solder mask areas. For exposed dielectric, encroachment on lands, blistering, pits and voids in dielectric areas and printed board edge chipping, see 3.7.1.			3.7.1
Solder Mask Cure and Adhesion	Maximum loss of adhesion after tape test per Table 3-16. No tackiness, delamination or blistering to the following extent: • Class 1 does not bridge between conductors • Class 2 and Class 3, 2 per side, maximum size 250 µm [9,843 µin] in longest dimension, and does not reduce electrical spacing between conductors by more than 25%.			3.7.2
Solderability (Visual)	When required by the procurement documentation, accelerated conditioning for coating durability **shall** be in accordance with J-STD-003. If the accelerated conditioning for coating durability Category is not specified, Category 2 **shall** be used for SnPb and Category A **shall** be used for lead-free. Test coupons or printed boards to be tested **shall** be conditioned, if required, and evaluated for surface and PTH solderability using J-STD-003. Unless otherwise specified, the default test for through-hole **shall** be a solder float of the "S" coupon; the default test for surface mount **shall** be edge-dip of the "M" or "W" coupon. SnPb solder **shall** conform to the contaminant level specified in Table 3-2. NOTE: As per the J-STD-003, edge dip testing **shall** require the use of a mechanical or electromechanical device unless AABUS (e.g., a set of tweezers does not constitute a mechanical device).			3.3.6
Special Requirements (When Specified)	AABUS.			3.10
Structural Integrity	**Shall** meet structural integrity requirements for thermally stressed evaluation coupons specified in 3.6.2.			3.6
Solderable Surface Mount Lands (Rectangular)	Defects along edge of land not > 30%; internal defects not > 20%.	Defects along edge of land not > 20%; internal defects not > 10%.		3.5.4.2.1
	Defects internal to the land remain outside of the central 80% of the land width by 80% of the land length, or pristine area. Electrical test probe "witness" marks within the pristine area for Class 1, Class 2 and Class 3 are considered cosmetic in nature and are acceptable provided the requirements for surface finish are met. Any combination of isolated surface anomalies (e.g., nicks, dents, nodules, dewetting or pinholes) within the pristine area are acceptable provided the final finish requirements are met, that they are within the dimple/protrusion limits of 3.5.4.8 & 3.5.4.9 and do not occupy more than 5% of the pad area.			
Solderable Surface Mount Lands (Round)	Defects along edge of land do not radially extend towards center by more than 10% of the diameter of the land and not extend more than 30% around the circumference of the land.	Defects along edge of land do not radially extend towards center by more than 10% of the diameter of the land and not extend more than 20% of the circumference of the land.		3.5.4.2.2

Characteristic Inspection	Requirements			Requirement Paragraph
	Class 1	Class 2	Class 3	
	Defects internal to the land remain outside of the central 80% of the land width by 80% of the land length, or pristine area. One electrical test probe mark allowed within the pristine area for Class 1, 2 and 3. Electrical test probe "witness" marks within the pristine area for Class 1, Class 2 and Class 3 are considered cosmetic in nature and are acceptable provided the requirements for surface finish are met. Any combination of isolated surface anomalies (e.g., nicks, dents, nodules, dewetting or pinholes) within the pristine area are acceptable provided the final finish requirements are met, that they are within the dimple/protrusion limits of 3.5.4.8 & 3.5.4.9 and do not occupy more than 5% of the pad area.			
Thermal Shock	When specified, testing/evaluation according to IPC-TM-650, Method 2.6.7.2, with temp range between -65 to 125 °C [-85 to 257 °F]. An increase in resistance of 10% or more **shall** be considered a reject and **shall** meet requirements of Table 3-10 after cycling.			3.10.7
Thermal Stress Testing	Test coupons or printed boards **shall** be thermally stressed. Per the applicable criteria listed in 1.3.3, one or more of the following Test Methods **shall** be required: 3.6.1.1 Thermal Stress Testing, Method 2.6.8. 3.6.1.1.1 Thermal Stress Testing, Method 2.6.8 (Microvias) 3.6.1.2 Thermal Stress Testing, Method 2.6.27 (230 °C) 3.6.1.3 Thermal Stress Testing, Method 2.6.27 (260 °C)			3.6.1
Vibration	Printed board **shall** pass test requirements of 3.8.2 after vibration cycling.			3.10.3
Visual	Finished product **shall** be examined, be of uniform quality, and conform to 3.3.1 through 3.3.10. Visual examination for applicable attributes **shall** be conducted at 3 diopters (approx.1.75X). Visual examination of microvia features for applicable dimensional or workmanship attributes **shall** be conducted at 30X minimum. If confirmation of a suspected non-conformance cannot be made at 3 diopters, it should be verified at progressively higher magnifications (up to 40X) to confirm conformance.			3.3
Voids, Laminate	For Class 1 products, voids allowed outside of any thermal zone (see Figure 3-13) **shall not** exceed 150 µm [5,906 µin]. Boundary line voids that overlap into a thermal zone **shall not** be in excess of 150 µm [5,906 µin] for lass 1 products.	For Class 2 and Class 3 products, there **shall** be no laminate voids outside of any thermal zones (see Figure 3-13) in excess of 80 µm [3,150 µin]. Boundary line voids that overlap into a thermal zone **shall not** be in excess of 80 µm [3,150 µin] for Class 2 or Class 3 products.		3.6.2.3
	Voids between conductive patterns that are not electrically common in either the horizontal or vertical direction **shall not** decrease the minimum dielectric spacing.			
Voids in Surface	Surface voids are acceptable provided they do not exceed 0.8 mm [0.031 in] in the longest dimension; bridge conductors; nor can the voids exceed 5% of the total printed board area per side.			3.3.2.8
Weave Exposure	Weave exposure does not reduce the remaining conductor spacing (excluding the area(s) with weave exposure) below the minimum.		No weave exposure.	3.3.2.5
Wire Bond Pads	Final conductor finish as specified in 1.3.4.3 for GWB-1, GWB-2 or ENIG. Surface finish coating per Table 3-3 for applicable coating. Pristine area **shall** have maximum surface roughness of 0.8 µm [32 µin] RMS as measured in accordance with IPC-TM-650, Method 2.4.15. No pits, nodules, scratches, electrical test probe marks within the pristine area that violates RMS requirement.			3.5.4.3
Workmanship	**Shall** be free of defects and of uniform quality – no visual of dirt, foreign matter, oil, fingerprints.			3.3.10

This Page Intentionally Left Blank

ANSI/IPC-T-50 Terms and Definitions for Interconnecting and Packaging Electronic Circuits Definition Submission/Approval Sheet

The purpose of this form is to keep current with terms routinely used in the industry and their definitions. Individuals or companies are invited to comment. Please complete this form and return to:

IPC
3000 Lakeside Drive, Suite 105N
Bannockburn, IL 60015-1249
Fax: 847 615.7105

SUBMITTOR INFORMATION:

Name: _____

Company: _____

City: _____

State/Zip: _____

Telephone: _____

Date: _____

❑ This is a **NEW** term and definition being submitted.
❑ This is an **ADDITION** to an existing term and definition(s).
❑ This is a **CHANGE** to an existing definition.

Term	Definition

If space not adequate, use reverse side or attach additional sheet(s).

Artwork: ❑ Not Applicable ❑ Required ❑ To be supplied
❑ Included: Electronic File Name: _____

Document(s) to which this term applies: _____

Committees affected by this term: _____

Office Use

IPC Office	Committee 2-30
Date Received: _____	Date of Initial Review: _____
Comments Collated: _____	Comment Resolution: _____
Returned for Action: _____	Committee Action: ❑ Accepted ❑ Rejected
Revision Inclusion: _____	❑ Accept Modify

IEC Classification

Classification Code • Serial Number

Terms and Definition Committee Final Approval Authorization:
Committee 2-30 has approved the above term for release in the next revision.

Name: _____ Committee: IPC 2-30 Date: _____

This Page Intentionally Left Blank

Standard Improvement Form

IPC-6012E

The purpose of this form is to provide the Technical Committee of IPC with input from the industry regarding usage of the subject standard.

Individuals or companies are invited to submit comments to IPC. All comments will be collected and dispersed to the appropriate committee(s).

If you can provide input, please complete this form and return to:

IPC
3000 Lakeside Drive, Suite 105N
Bannockburn, IL 60015-1249
Fax: 847 615.7105
E-mail: answers@ipc.org
www.ipc.org/standards-comment

1. I recommend changes to the following:

___ Requirement, paragraph number _____

___ Test Method number _____, paragraph number _____

The referenced paragraph number has proven to be:

___ Unclear ___ Too Rigid ___ In Error

___ Other _____

2. Recommendations for correction:

3. Other suggestions for document improvement:

Submitted by:

Name Telephone

Company E-mail

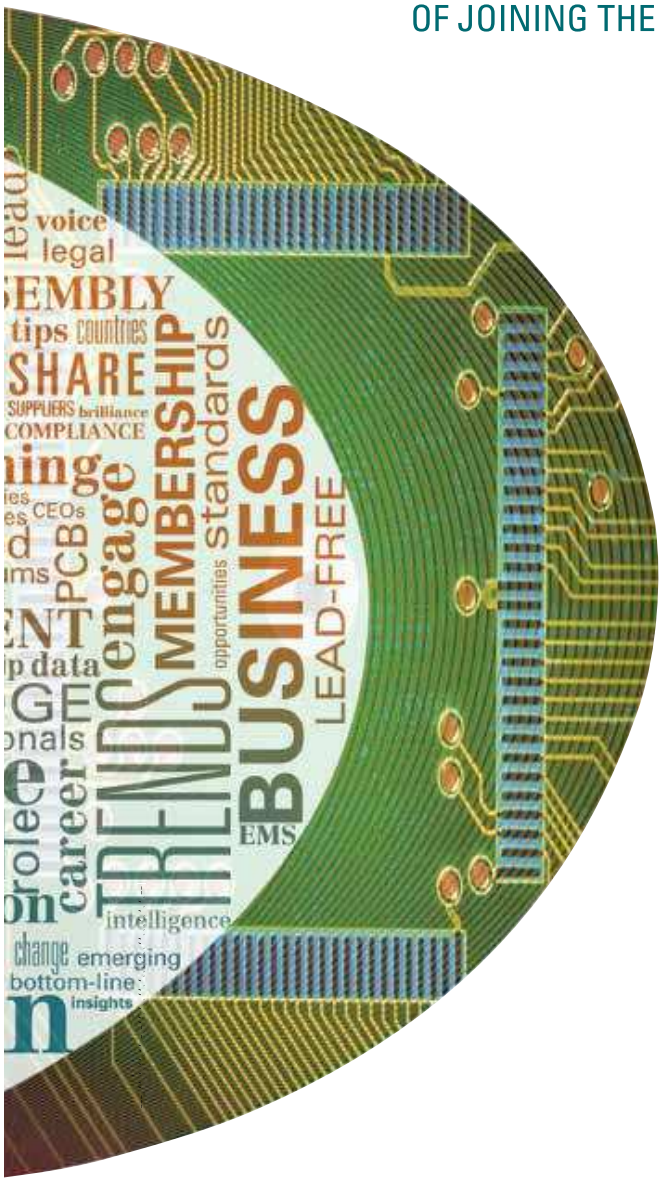
Address

City/State/Zip Date

This Page Intentionally Left Blank

Experience the BENEFITS

OF JOINING THE ELECTRONICS INDUSTRY'S PREMIER ASSOCIATION



Expand your company's resources and influence in the electronics industry.

- Stay Current
- Get Connected
- Shape the Industry
- Train Your Staff
- Contain Costs
- Join the leaders in IPC
- Market Your Business

Learn more about IPC membership and apply online at **www.ipc.org/membership** or contact the Member Success team at **membership@ipc.org**.

Association Connecting Electronics Industries

3000 Lakeside Drive, Suite 105 N
Bannockburn, IL 60015
847-615-7100 **tel**
847-615-7105 **fax**
www.**ipc**.org

ISBN #978-1-951577-09-4