DELTA TAU
Data Systems, Inc.
NEW IDEAS IN MOTION...

USER MANUAL

OPTIONS 4A, 5A, 5B

Enhanced Option CPU Sections

602405-10X (-PC, -VME)

602402-10X (-Lite)

June 1994

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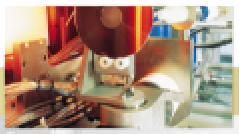

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INTRODUCTION

The new PMAC CPU-section Options 4A, 5A, and 5B (the "Option CPUs") offer several advantages over the standard PMAC CPU section. These advantages include:

1.) Faster operation: The standard CPU section runs at 20 MHz with one-wait-state RAM. Option 4A runs at 20 MHz with zero-wait-state RAM; Option 5A runs at 40 MHz with zero-wait-state RAM; Option 5B runs at 60 MHz with zero-wait-state RAM.

2.) Flash memory: The standard CPU section uses an EPROM to store the firmware, an EEPROM to store the basic setup variables, and a battery to retain user programs and buffers in RAM. The Option CPU sections use a segmented flash EEPROM to retain firmware, setup variables, and user programs and buffers.

3.) Buffered expansion port: With the standard CPU section, the expansion port (JEXP) is unbuffered, limiting the number of accessory boards that can be attached to this port. The limit for the 20 MHz standard CPU section is 2 unbuffered accessory boards; the limit for the 30 MHz standard CPU section is 1 unbuffered accessory board. (ACC-14 and ACC-36 boards past the first ACC-14 or ACC-36 in the series are buffered; all other boards on this port -- Opt 2, ACC-23, ACC-24, ACC-29 -- are unbuffered.) The CPU sections for Options 4A, 5A, and 5B have on-board buffering for the expansion port, which allows the user to put on all possible accessory boards simultaneously.

On PMAC-PC and PMAC-VME, the Option CPU section is a separate "piggyback" circuit board. It is possible to replace the CPU board on an existing PMAC-PC or PMAC-VME, even as a field upgrade. Contact your representative, distributor, or the factory for details on the exchange.

On PMAC-Lite, the Option CPU section is part of the main circuit board. No upgrades are possible. The Option CPU for the PMAC-Lite is not ready for commercial release as of the writing of this manual (May 1994). Contact your representative, distributor, or the factory for availability of this version.

FIELD UPGRADE INSTRUCTIONS

It is possible to change from the standard CPU board to the Option CPU board in the field with the PMAC-PC and PMAC-VME. With the PMAC-Lite, the entire controller must be replaced.

It is important to take proper anti-static protection measures when performing the replacement. If formal protection facilities (wrist straps, conductive table and floor mats) are not available, at least make sure that you are away from charge carriers like carpets, and that you draw charge off yourself by contacting metal before you start the operation.

The replacement procedure is a very simple 4-step process:

1.) Remove the screw that holds the CPU board to the base board.

2.) Gently but firmly pull on the the CPU board to loosen it from the two backside connectors. A slight rocking force along the long axis of the connectors can help. When loose, remove this board and set it aside.

3.) Remove the Option CPU board from its anti-static bag and place it on the main board, pressing carefully to lock it firmly into both backside connectors.

4.) Insert and tighten the holding screw.

OPERATIONAL BEHAVIOR

PMACs with an Option CPU have only two operational differences from PMACs with the standard CPU: in the **SAVE** command, and in the reset cycle. All other operation is identical. The Option CPU also gives the capability to upgrade the firmware without changing any components.

Save Operation

The **SAVE** command with the Option CPU copies all user variables, definitions, programs, and buffers from active memory to the non-volatile flash memory. If there is a EEPROM IC on the PMAC, it is not used. The **SAVE** operation takes about 10 to 20 seconds to execute. The command acknowledgement character (*<LF>* or *<ACK>*) that PMAC sends if I3>0 is not sent back to the host until after the entire **SAVE** operation is completed. Without a battery, nothing is retained in PMAC's memory through a power-down or reset unless it has been saved to the flash memory.

By comparison, with the standard CPU section, only the I-variables, conversion table entries, and bus addresses for DPRAM and VME must explicitly be stored with the **SAVE** command. Other variable values, definitions, programs, and buffers are automatically held by the battery as soon as they are sent to PMAC.

Reset Operation

PMAC's reset cycle can be executed in several ways:

1.) Turning 5V power off, then on.
2.) Taking the INIT/ line low, then high.
3.) For bus interfaces, taking the bus reset line low, then high with E39 ON.
4.) For PC bus interface, writing to {base+10} and {base+12} with E93 or E94 ON.
5.) Sending the **$$$** command.

With the Option CPU section, PMAC copies the contents of the flash memory into active memory during a normal reset cycle (E51 OFF), overwriting any current contents. *This means that anything changed in PMAC's active memory that was not saved to flash memory will be lost.* Even the last saved P-variable and Q-variable values are copied from flash to RAM during the reset cycle.

The reset cycle takes about the same time to execute with the Option CPU as it does with the standard CPU, less than one second.

Re-Initialization and Firmware Upgrade

As in a PMAC with the standard CPU, the **$$$*** ** command will empty all user programs and buffers, and assign factory default values to all I-variables, conversion table settings, and DPRAM and VME bus addresses. It will also recalculate the firmware checksum reference value.

If the jumper E51 is ON when a PMAC with the Option CPU executes its reset cycle, PMAC enters a special re-initialization mode that permits the downloading of new firmware. In this mode, if serial communications is used, it must be at 38,400 baud, regardless of the setting of the baud rate jumpers. Only a very basic "bootstrap" firmware is executing in this mode.

Note: In the earliest Option CPU boards -- those with bootstrap firmware version 1.00 (see below) -- re-initialization communications is only possible over the serial port, so any operational firmware upgrade must be done over the serial port.. In newer versions of the bootstrap firmware (1.01 and grreater), communications is possible over the bus as well.

In this bootstrap mode, there are very few command options. PMAC will respond to any of the status-bit query commands (**?**, **??**, or **???**) with the response ***BOOTSTRAP PROM***. This permits the host to know whether PMAC is in this mode or not. PMAC will respond to the **VERSION** query command with the number of the bootstrap firmware (e.g. ***1.01***) which will probably be different than the operational firmware version.

To bypass the download operation in this mode, send a **<CONTROL-R>** character to PMAC. This puts PMAC in the normal operational mode with the existing firmware. Factory default values for I-variables, conversion table settings, and bus addresses for DPRAM and VME are copied from the firmware section of flash memory into active memory. The saved values of these values are not used, but they are still kept in the user section of flash memory.

Note: Before attempting to upgrade PMAC operational firmware, make sure all of PMAC configuration has been stored to disk. If the new firmware provides a different user memory map, PMAC will clear memory on power-up after new firmware has been loaded. Even if this is not the case, the easiest way to establish a new firmware checksum reference value is to send the **$$$*** ** command, which clears the buffers.

For any change in the operational firmware, the compiled PLCs will have to be re-compiled with the **LIST LINK** file for the new firmware version. It is important to delete all compiled PLCs (**DELETE PLCC n**) *before* attempting to change the operational firmware version. Compiled PLC programs running under a firmware version other than that which they were compiled for can have unpredictable consequences.

To download new operational firmware to the PMAC, send a **<CONTROL-O>** character to PMAC over the serial port. The bootstrap firmware interprets this as a signal to prepare for downloading of new operational firmware. All subsequent bytes received over the serial port will be considered as binary-coded bytes of machine-code firmware, and will be written into the flash memory.

The host computer should wait at least 5 seconds after the **<CONTROL-O>** command before starting to download the operational firmware. This delay ensures that the flash memory is ready to be written to. After downloading, the PMAC should be powered down; no other communications should be attempted with PMAC at this time.

After turning off power to PMAC, the E51 jumper should be removed. When power is re-applied to PMAC, it should operate normally with the new firmware. The user settings stored in other segments of the flash memory with the **SAVE** command are not affected by the downloading of new firmware (unless the new firmware has a different user memory map).

The PMAC Executive program V3.x and newer, when it establishes communications with a PMAC in this re-initialization mode, will automatically notice that PMAC is in this mode. In this mode, the menu selection "Download binary firmware file.." in the File menu can be selected to take a binary file from disk and copy over the serial port to PMAC. The program then forces you to exit to the operating system. At this point, you should turn off power to PMAC and remove the E51 jumper.

With older versions of the PMAC Executive program, or with a terminal emulator program running on a PC, the procedure for downloading new firmware is as follows (remember to back up your PMAC software and delete any compiled PLC programs first):

1.) Establish communications to PMAC over the serial port at 38400 baud. Confirm that PMAC is in this re-initialization mode by seeing that it responds to the **?** command with *BOOTSTRAP PROM*. If you are in the Executive program, make sure that all windows other than the Terminal window (such as the position window) are closed, so no other commands are being sent to PMAC.

2.) Type a **<CONTROL-O>** character in the terminal window and immediately exit to DOS. Do not send any other characters to PMAC here.

3.) Use the binary version (/B) of the DOS `COPY` command to download the file containing the new firmware to PMAC. The command typed at the DOS prompt will look something like

```
COPY/B B:V115A.BIN COM1:
```

where `B:V115A.BIN` is the directory and name of the file containing the operational firmware in binary machine code format, and `COM1:` is the serial port being used for communications.

4.) Shut off power to PMAC and remove the E51 jumper.

5.) Restore power to PMAC and resume normal operation with the new firmware.

6.) If you want to update your firmware checksum reference value so PMAC does not report a firmware checksum error, the easiest method is to send the **$$$***** command, which causes PMAC to compute the new reference value automatically (but it also clears all of your programs and buffers from active memory). As an alternative method, send the command **RHX:$0794** several times. If you get the same value each time, PMAC has stopped its checksum

calculations on an error, and the reported value is the value it calculated for the firmware checksum. Write this value into reference register X:$07B1. For example, if **RHX:$0794** returns *9A3B12* several times, send the command **WX:$07B1,$9A3B12** to PMAC. Remember that for either method, you will need to store this reference value to flash memory with the **SAVE** command.

7.) If you need to re-compile PLC programs, either use the LISTLINK.TXT file that corresponds to the new firmware version, or create this file by sending the **LIST LINK** command to the PMAC with the new firmware and storing the response in a text file of this name.

CLOCK FREQUENCY CONSIDERATIONS

The clock crystal frequency on all of the option CPU sections is 20 MHz (actually 19.6608 MHz). On the Option 5A and 5B sections, this frequency is multiplied with a phase-locked loop inside the CPU. Nothing outside of the CPU sees these higher frequencies directly.

User-Settable Clock Frequencies

The encoder sample clock (SCLK) is derived from the original clock crystal frequency of 19.6608 MHz through one of the jumpers E34 through E38. Users of any of the option CPUs 4A, 5A, or 5B should use the section of the table under the 19.6608 MHz master frequency when selecting one of these jumpers to determine the SCLK frequency.

The clock for the D/A & A/D converters (DCLK) is derived from the original clock crystal frequency of 19.6608 MHz through one of the settings of jumper E98. Users of any of the option CPUs 4A, 5A, or 5B should use the section of the table under the 19.6608 MHz master frequency when selecting the E98 jumper position to determine the DCLK frequency.

The phase clock (PHASE) is derived from the original clock crystal frequency of 19.6608 MHz through one of the jumpers E29 through E33. Users of any of the option CPUs 4A, 5A, or 5B should use the section of the table under the 19.6608 MHz master frequency when selecting one of these jumpers to determine the PHASE frequency.

The servo clock (SERVO) is divided down from the phase clock by a number determined by the settings of jumpers E3 through E6. Since the phase clock is derived from the clock crystal frequency of 19.6608 MHz, users of any of the option CPUs 4A, 5A, or 5B should use this frequency as a starting point as well in all calculations for the servo clock.

Serial Baud Rate

The serial communications baud rate is derived from the CPU's internal clock, which are at a higher frequency in the option 5A and 5B CPUs. To keep the baud rates in the same range, all of the option CPUs divide the CPU's clock twice as much as the standard CPUs for the same setting of baud rate jumpers E44-E47. This means that:

1.) Option 4A (20 MHz CPU): The baud rates for a given E44-E47 setting are half of those listed under the "19.6608 MHz Master Clock" column.

2.) Option 5A (40 MHz CPU): The baud rates for a given E44-E47 are the same as those listed under the "19.6608 MHz Master Clock" column.

3.) Option 5B (60 MHz CPU): The baud rates for a given E44-E47 are the same as those listed under the "29.4912 MHz Master Clock" column.

JUMPER SETTINGS

PMAC-PC, PMAC-VME

The Option CPU exists as a separate piggyback printed circuit board for the PMAC-PC and PMAC-VME. This circuit board has 3 jumpers:

```
E1      * 1             REMOVE JUMPER TO ENABLE
        * 2             WATCHDOG TIMER OPERATION

                        JUMP PINS 1 AND 2 TO DISABLE
                        WATCHDOG TIMER OPERATION
                        (FOR TEST PURPOSES ONLY)

E2      * 1             REMOVE JUMPER FOR USE ON
        * 2             1ST GENERATION PMAC

                        JUMP PINS 1 AND 2 FOR USE ON
                        2ND GENERATION PMAC ("PMAC2")

E3      * 1             REMOVE JUMPER FOR USE ON
        * 2             1ST GENERATION PMAC

                        JUMP PINS 1 AND 2 FOR USE ON
                        2ND GENERATION PMAC ("PMAC2")
```

NOTE: PINS FOR JUMPERS E2 AND E3 MAY NOT BE INSTALLED ON OPTION CPU BOARDS FOR 1ST GENERATION PMACS.

PMAC-Lite

On PMAC-Lite, the Option CPU is a section of the main circuit board, replacing the standard CPU section. The standard CPU section uses 3 jumpers: E103, E104, and E105. The Option CPU section uses only one jumper: E103. It has the same meaning as for the standard CPU section. E104 and E105 are not present on a PMAC-Lite with the Option CPU section.

All PMACs

Jumper E48 is not used on a PMAC with Option 4A (RAM is always zero-wait-state; no clock frequency multiplication can be performed). E48 performs a different function with the Option 5A or 5B than it does for the standard CPU, as explained below.

```
E48      * 1             JUMP PINS 1 AND 2 TO
         * 2             MULTIPLY CRYSTAL FREQUENCY
                         BY 3 INSIDE CPU FOR 60 MHZ
                         OPERATION

                         REMOVE JUMPER TO MULTIPLY
                         CRYSTAL FREQUENCY BY 2
                         INSIDE CPU FOR 40 MHZ
                         OPERATION
```

```
IMPORTANT NOTE: IT MAY BE POSSIBLE TO OPERATE A BOARD WITH 40
MHZ COMPONENTS (OPTION 5A) AT 60 MHZ UNDER SOME CONDITIONS BY
CHANGING THE SETTING OF JUMPER E48.  HOWEVER, THIS OPERATES THE
COMPONENTS OUTSIDE OF THEIR SPECIFIED OPERATING RANGE, AND
PROPER EXECUTION OF PMAC UNDER THESE CONDITIONS IS NOT
GUARANTEED.  PMAC SOFTWARE FAILURE IS POSSIBLE, EVEN PROBABLE,
UNDER THESE CONDITIONS, AND THIS CAN LEAD TO VERY DANGEROUS
MACHINE FAILURE.  OPERATION IN THIS MODE IS DONE COMPLETELY AT
THE USER'S OWN RISK; DELTA TAU CAN ACCEPT NO RESPONSIBILITY FOR
THE OPERATION OF PMAC OR THE MACHINE UNDER THESE CONDITIONS.
```

LED INDICATORS

PMACs with the Option CPU have 3 LED indicators: red, yellow, and green. The red and green LEDs have the same meaning as with the standard CPU: when the green LED is lit, this indicates that power is applied to the +5V input; when the red LED is lit, this indicates that the watchdog timer has tripped and shut down the PMAC.

The new yellow LED located beside the red and green LEDs, when lit, indicates that the phase-locked loop that multiplies the CPU clock frequency from the crystal frequency on the Option CPU is operational and stable. This indicator is for diagnostic purposes only; it may not be present on your board.

COMPUTATIONAL SPEED

One of the main reasons for selecting an Option CPU is to obtain faster computational speed. The faster clock speed of the CPU provides a directly proportionate increase in computational speed. A CPU running at 40 MHz can compute twice as fast as one running at 20 MHz.

The zero-wait-state memory that comes on the Option CPU sections also provides increased computational speed over the standard CPU section with one-wait-state memory in operations that require the CPU to access external memory. Virtually all tasks except the servo and phase updates for motors 1 through 4 require external memory access. In a typical configuration, zero-wait-state memory provides a 15%-20% increase in computational speed over a system with one-wait-state memory operating at the same clock frequency.

In most applications, the speed of user programs -- block rates in motion programs, scan rates in PLC programs -- can be increased substantially more than the increase in raw computational speed, *provided that the servo and phase update rates are not increased proportionately with the clock frequency*. If the servo and phase update rates are not increased with the clock frequency they will execute in a smaller percentage of the processor time. This leaves a higher percentage of processor time for the user programs to execute at a higher speed, providing a double boost to program execution rate.

While it is possible to use the extra processing power of the faster CPU section to increase servo and/or phase update rates, in most applications the extra computational power is allotted for user programs. The servo and phase updates should occur fast enough to obtain the desired dynamic performance, but no faster. Anything faster is a waste of processing time.

As an example of evaluating the increased program execution rates, take a system where the servo and phase updates occupy 50% of processor time on a 20 MHz, 1-wait-state PMAC. On a 40 Mhz, 0-wait-state PMAC, the servo and phase updates would occupy 25% or less of the processor time at the same update rate. The programs now have 75% of processor time to execute, a 1.5 times improvement. The 40 MHz processor doubles their raw execution speed; the 0-wait-state RAM provides a further 20% (of 200%!) increase, yielding 2.4 times faster speed. The net increase in program capability is then 2.4 times 1.5, or a 3.6 times improvement. If 10 msec blocks were the smallest that could be executed before, 3 msec blocks could now be executed.

EXPANSION PORT

The Option CPU provides on-board buffering for the expansion port (JEXP). This permits all useful combinations of expansion-port accessory boards to be used simultaneously on the port. These boards are:

1.) Option 2 Dual-Ported RAM board (for PMAC-PC and PMAC-Lite)
2.) ACC-14D/V Digital I/O Expansion Board
3.) ACC-23P Analog-to-Digital Converter Board (discontinued)*
4.) ACC-24P/V Axis Expansion Board *
5.) ACC-29P/V MLDT Interface Board *
6.) ACC-36P/V Analog-to-Digital Converter Board
* Only one of these boards may be used in a given configuration.

All of these accessory boards have been tested with the Option CPUs, and no problems have been found at any of the processor speeds.

Note: Problems have been reported with third-party accessory boards when operated with the Option CPU boards. Delta Tau Data Systems cannot guarantee the operation of PMAC with these accessory boards.

In all cases, the cable length between any two boards connected on the port shall not exceed 150 mm (6"). Do not leave any unterminated lengths of cable.

With each accessory board, Delta Tau provides a 2-connector cable for connection between it and PMAC, or between it and the "cascade" connector on the previous board. The following boards have "cascade" connectors:

1.) ACC-14D/V
2.) ACC-23P
3.) ACC-36P/V

In some cases, a cable with 3 connectors is required when multiple boards of different sizes and/or without cascade connectors are used on the expansion port. Delta Tau can provide this cable; it comes under several names on the price list, under each board for which it might be:

1.) PMAC-PC/Lite Option 2 Sub-option A
2.) ACC-14D/V Sub-option 7
3.) ACC-24P/V Sub-option 2
4.) ACC-36P/V Sub-option 2