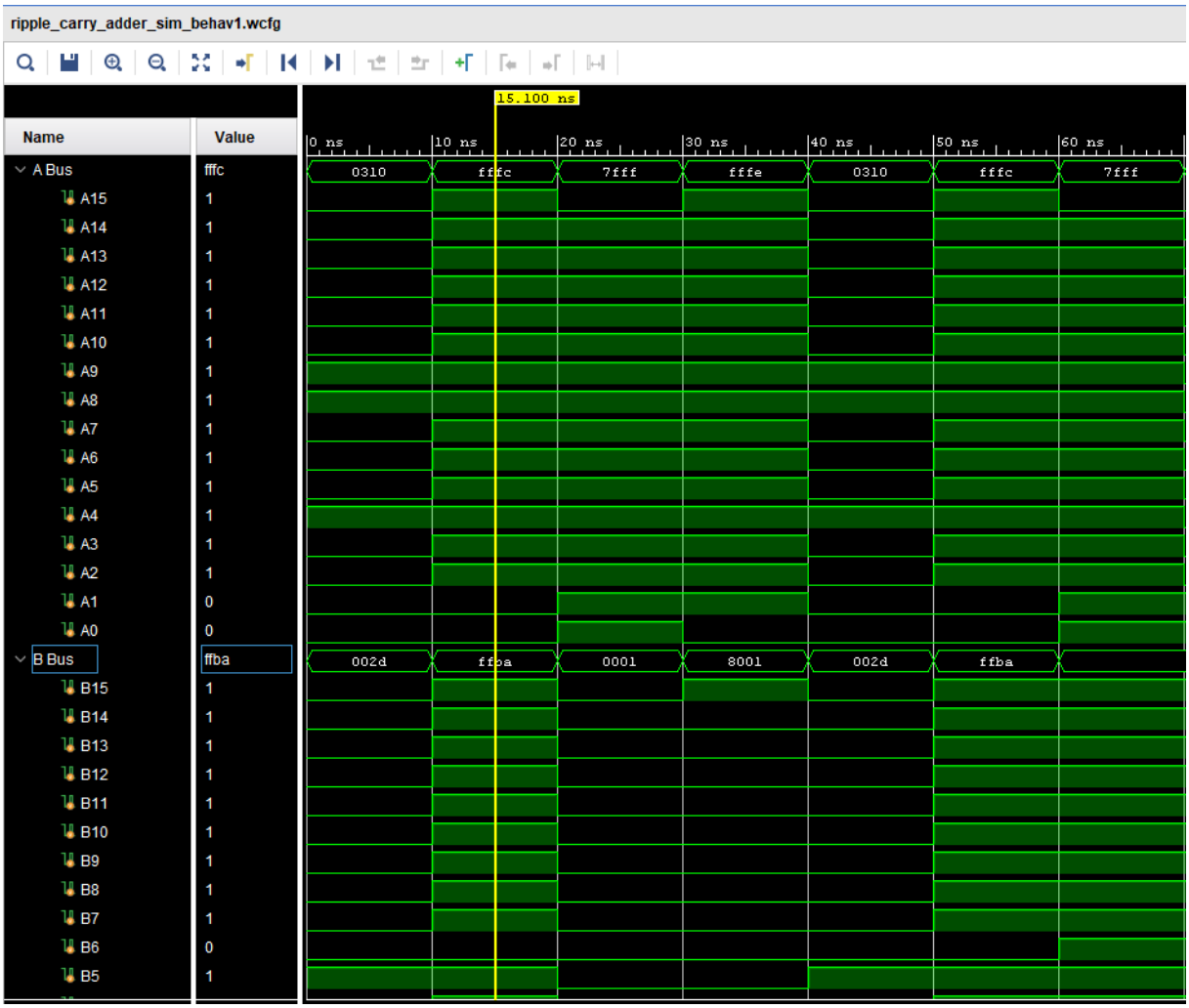
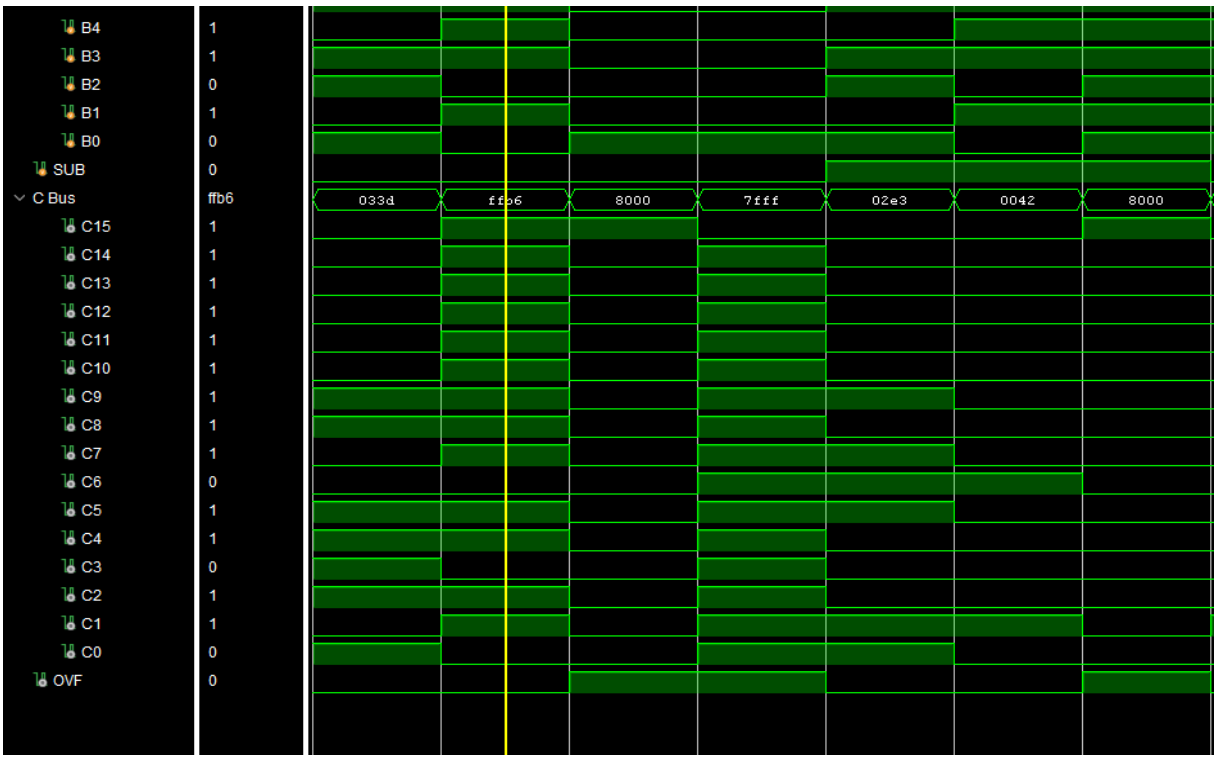
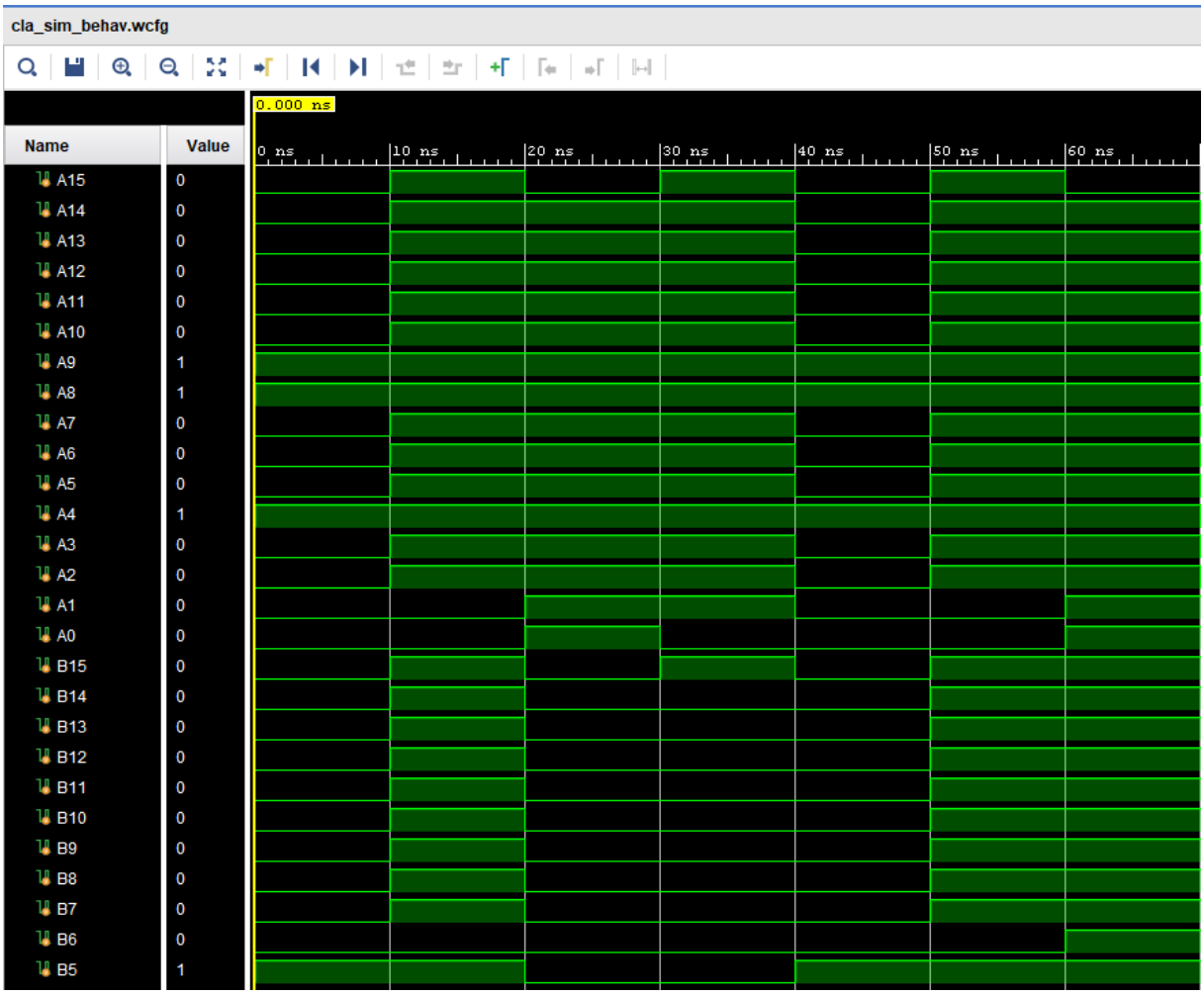
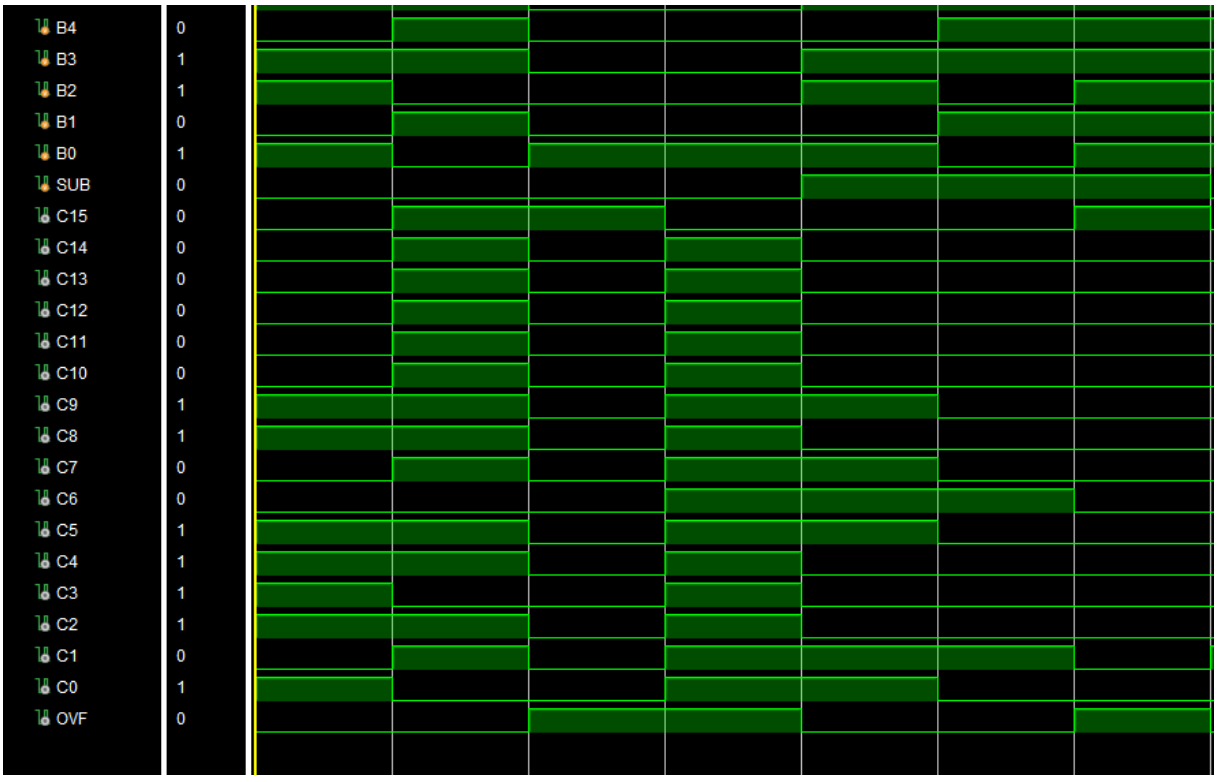
Ripple Carry test results:





CLA:


cla_sim_behav.wcfg
0.000 ns
0 ns
10 ns
20 ns
30 ns
40 ns
50 ns
60 ns
Name
Value
A15 0
A14 0
A13 0
A12 0
A11 0
A10 0
A9 1
A8 1
A7 0
A6 0
A5 0
A4 1
A3 0
A2 0
A1 0
A0 0
B15 0
B14 0
B13 0
B12 0
B11 0
B10 0
B9 0
B8 0
B7 0
B6 0
B5 1


B4 0
B3 1
B2 1
B1 0
B0 1
SUB 0
C15 0
C14 0
C13 0
C12 0
C11 0
C10 0
C9 1
C8 1
C7 0
C6 0
C5 1
C4 1
C3 1
C2 1
C1 0
C0 1
OVF 0

First one is rpa, second is cla, so cla is faster

delays:

Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock
Path 1	∞	10	9	23	SUB	OVF	14.320	4.588	9.732	∞	input port clock
Path 2	∞	10	9	23	SUB	C15	14.096	4.614	9.482	∞	input port clock
Path 3	∞	10	9	23	SUB	C14	13.745	4.609	9.136	∞	input port clock
Path 4	∞	9	8	23	SUB	C13	13.054	4.457	8.597	∞	input port clock
Path 5	∞	9	8	23	SUB	C12	12.969	4.463	8.507	∞	input port clock
Path 6	∞	8	7	23	SUB	C10	12.147	4.351	7.796	∞	input port clock
Path 1	∞	7	6	5	A0	C12	11.956	4.467	7.489	∞	input port clock
Path 2	∞	6	5	5	A0	C9	11.854	4.345	7.510	∞	input port clock
Path 3	∞	7	6	5	A0	OVF	11.740	4.240	7.500	∞	input port clock
Path 4	∞	7	6	5	A0	C13	11.736	4.233	7.503	∞	input port clock
Path 5	∞	7	6	5	A0	C14	11.546	4.261	7.284	∞	input port clock
Path 6	∞	7	6	5	A0	C15	11.271	4.266	7.005	∞	input port clock

rpa

Resource	Estimation	Available	Utilization %
LUT	23	63400	0.04
IO	50	210	23.81

cla

Resource	Utilization	Available	Utilization %
LUT	33	63400	0.05
IO	50	210	23.81

so cla uses more area

Sadi Gürsoy LAB 3:

First case: 784 + 45 → we know 829 fits in 16 bit signed → no overflow

For Ripple carry adder:

(C15, C14, ... C1) = (0000 0011 0011 1101) = 829

So result is correct OVF = 0

For CLA: 784+45

(C15, ... C1) = (0000 0011 0011 0101) = 829

OVF = 0

So result is correct

Second case: -44 - 30 = -74 SUB = 0

Ripple carry:

A = 1111 1111 1111 1100

B = 1111 1111 1011 1010

(C15 ... C1) = 1111 1111 1011 0110 = -74

OVF = 0

So result is correct

CLA:

A - B same

(C15 - C1) = 1111 1111 1011 0110 = -74

OVF = 0

So result is correct

Third case: 32767 + 1 = 32768 → does not fit in range, should give overflow

Ripple: SUB = 0

A = 0111 1111 1111 1111

B = 0000 0000 0000 0001

C = 1000 0000 0000 0000

OVF = 1

} gives overflow test succeed

CLA:

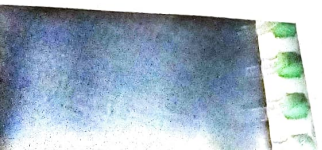
A = 0111 1111 1111 1111

B = 0000 0000 0000 0001

C = 1000 0000 0000 0000

OVF 1

} test succeed



Fourth case: $-2 + -32767 = -32769$ → should be overflow, does not fit in 16 bit signed

Ripple: SUB = 0

A = 1111 1111 1111 1110

B = 1000 0000 0000 0001

C = 0111 1111 1111 1111

OVF = 1

} gives overflow, test succeed

CLA:

C = 0 111 1111 1111 1111

OVF = 1

} gives OVF, wrong

Fifth case: $784 - 45 = 739 \leftrightarrow$ OVF = 0

Ripple carry adder:

SUB = 1

C = 0000 0010 1110 0011 = 739 OVF = 0

Then test succeed

CLA:

C = 0000 0010 1110 0011 = 739, OVF = 0

Then test succeed

Sixth case: $-4 - -70 = 66$ SUB = 1

should fit, no overflow

RCA:

C = 0000 0000 0100 0010 = 66 } test succeed

OVF = 0

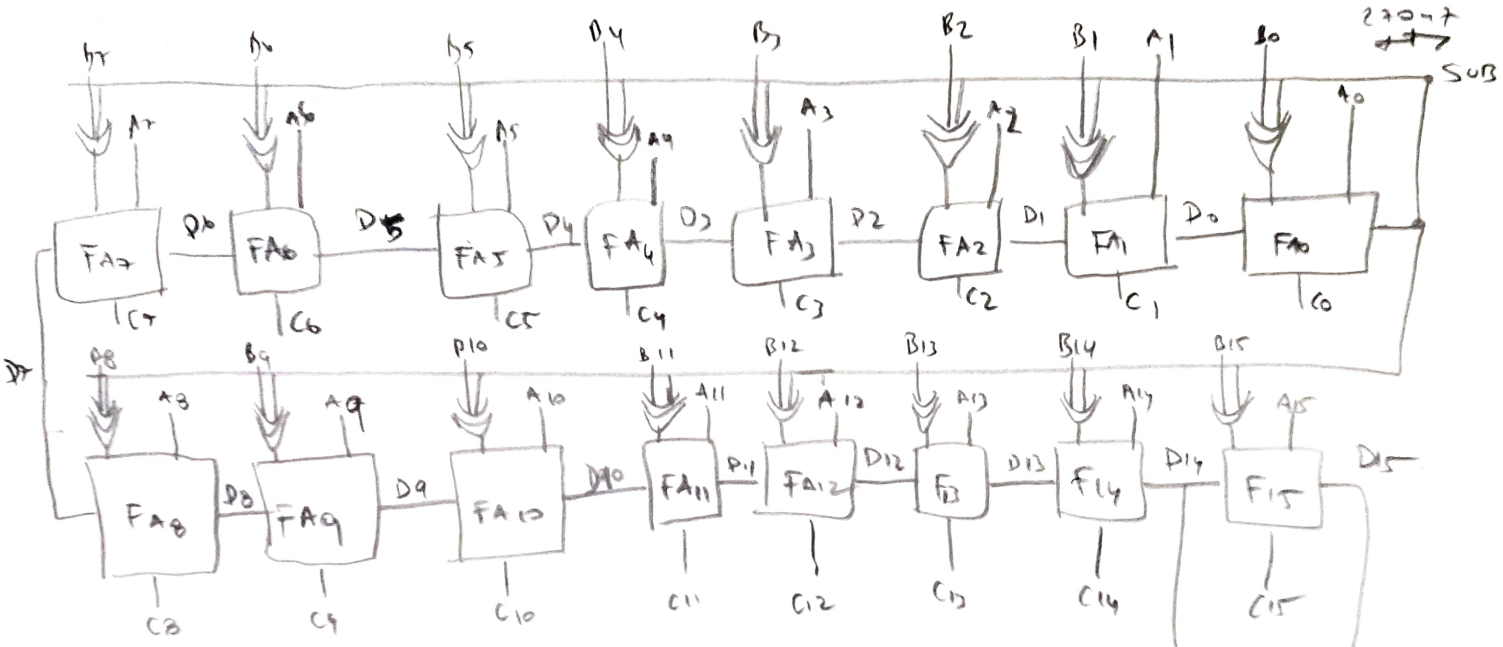
CLA

C = 0000 0000 0100 0010 = 66 } test succeed

OVF = 0

Lab 3:

Sadi Gujjary



FULL ADDER:

So the critical path goes through:

$b_0 \rightarrow XOR_2 \rightarrow XOR_2 \rightarrow AND \rightarrow OR \rightarrow$ Cin as input (15 times, until D15) $\rightarrow XOR \rightarrow OVF$

↓

1 AND + OR

Lab 3

Soal: Gilbert
270417

Then, we found that, delay is:

$T_R = 2T_{XOR} + T_{AND} + T_{OR} + 15(T_{AND} + T_{OR}) + T_{XOR}$

$= 3T_{XOR} + 16T_{AND} + 16T_{OR}$ → All 2 bit inputs.

Area is gate number we use:

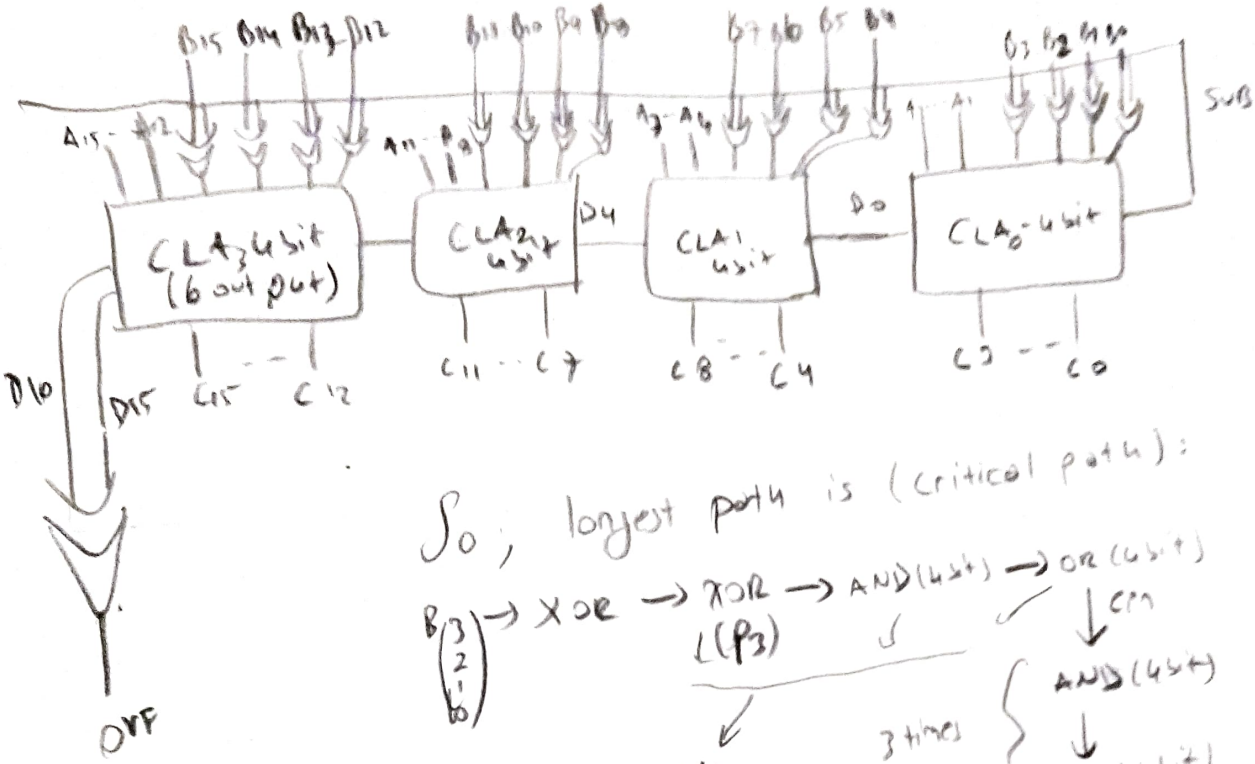
For every bit of B, we use XOR → 16 XOR

FA uses 2 XOR, 2 AND, 1 OR → 30 XOR, 32 AND, 16 OR

OVF → 1 XOR

SUM_R: 49 XOR + 32 AND + 16 OR = 97 gates...

Lab 3:



So, longest path is (critical path):

B(3,2,1,0) → XOR → XOR → AND(4bit) → OR(4bit) → CLA1

L(P3)

CLA1 → CLA2, CLA3 (3 times for every CLA except first one) → AND(4bit) → OR(4bit) → XOR(OVF)

Then:

$T_{CLA16} = 2T_{XOR} + 4T_{AND4bit} + 4T_{OR4bit} + T_{XOR}$

$= 3T_{XOR} + 4T_{AND-4bit} + 4T_{OR-4bit}$

Area: every CLA has: G0 - - G3 → 4 AND
P0 - - P3 → 4 XOR
D0 → 1 OR 1 AND
D1 → 2 OR 3 AND
D2 → 3 OR 6 AND
CARRY → 4 OR 10 AND
SUM0,1,2,3 → 4 XOR

Then, since All B inputs have XOR, and OVF has XOR

→ Gate count = 16 AND + 16 XOR + 4 OR + 30 AND + 16 XOR + 1 XOR = 185 gates

Sadi GULDES

[illegible]

[illegible]

① We see that ripple carry adder/sub uses 97 gates) and CLA uses 185 gates).

So, in terms of area, ripple carry is better

② $T_R = 3T_{XOR} + 16T_{AND} + 16T_{OR}$

$T_{CLA} = 3T_{XOR} + 4T_{AND-4bit} + T_{OR-4bit}$

It can be seen

$T_{CLA} < T_R$

So, CLA is better in terms of time