Ongine 制 品 规 格 书

机 种 名：OPD20 Ongine Projection
机种略号：OPD20M
文件编号：OG-WI-03-011
日　　期：2015/11/26

发注：　　迅达光电（深圳）有限公司

总经理	制造中心		研发中心		
	工厂	品质	承认	审核	作成

受注：

总经理	制造中心		研发中心		
	工厂	品质	承认	审核	作成

备注：本式样书一式__份，签订后各签订部门存档1份.

1、Revision History

Rev	Date	Approved	Description	Notes
ver1.0	2015.05.13	Yao	First Version	
ver2.0	2015.11.26	Yao	General Updata(heat sink\driver board)	
Ver3.0	2016.04.05	Allen	Update input image interface pin37&pin48 power on & power off sequencing	

2、 Optical Engine Function

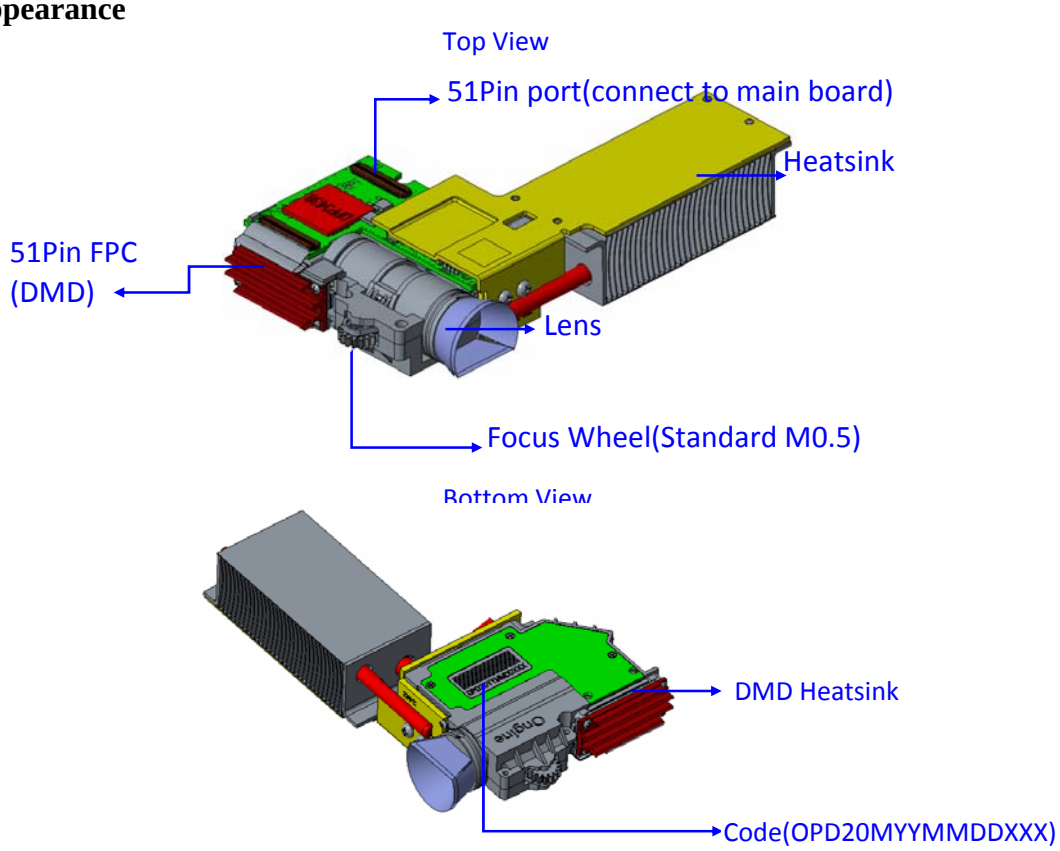
Optical specification

Display Technology	.3 720P DMD(DLP)
Light Source	LED(R,G,B)
Resolution	1280*720
Offset	100%
Foucsing	Manual focus in Rotating adjustment
Throw Ratio	1.66：1(Distance/Width)
Image Size	0.2m---5.5" 1m---27" 3m---81"
Brightness(Typical)	220 Lm @ PAD3000
Contrast (Full on/off)	500 : 1
Distortion(Abs)	<1.0%
Uniformity	>85%
Color Gamma(comparing to NTSC)	>100%
Dimension	44mm*55mm*16.2mm(max)
LED Life	>20,000 hours
System Voltage	12V

NOTE:

DMD IQC spec reference document "DMD Artifact Illustration"for PASS/FAIL.

3、 Appearance



3.1 Module Dimension

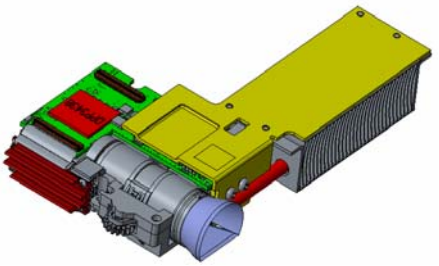


Figure 1

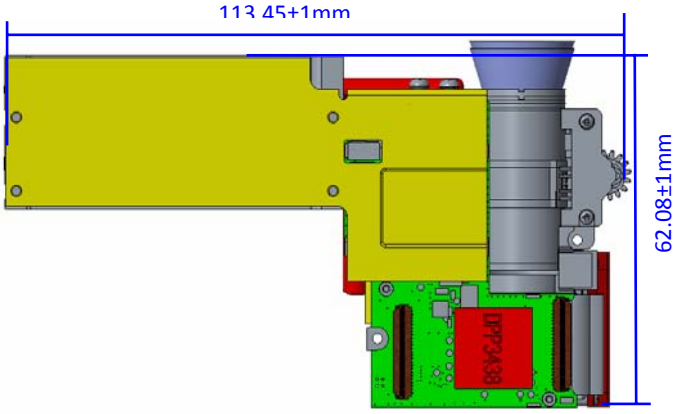


Figure 2

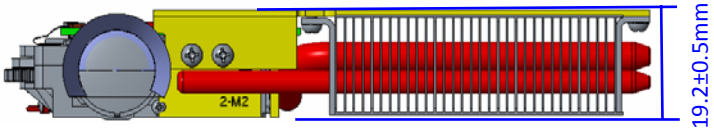


Figure 3

3.2 Module Fasten Screw

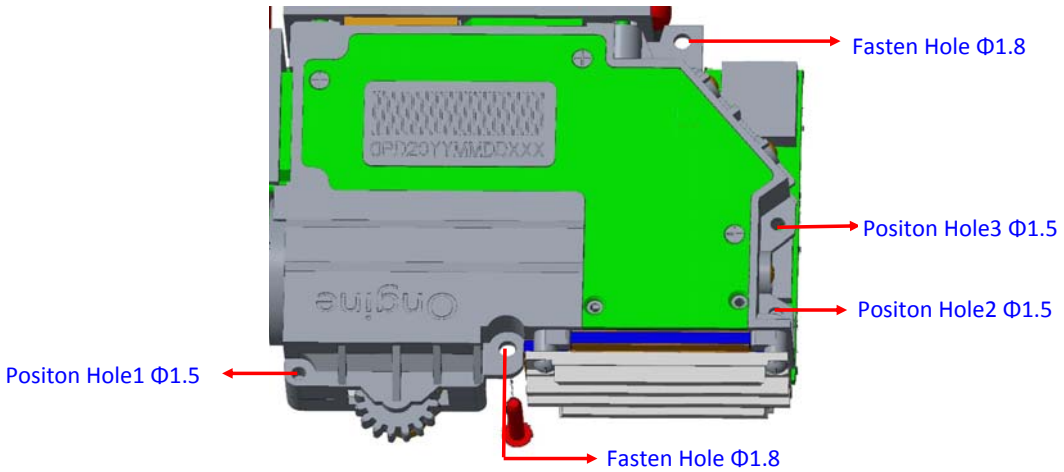


Figure 4

3.3 One-way turnning lens can be moved forward & backward.

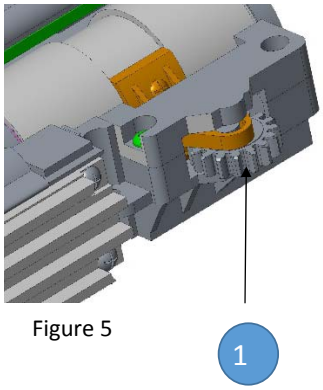


Figure 5

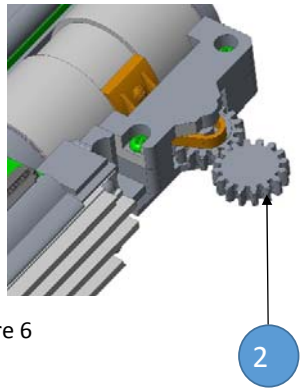


Figure 6

1. Method 1: Use the OE standard wheel to focus
2. Method 2:Use the standard wheel to work together with optical engine wheel to focus

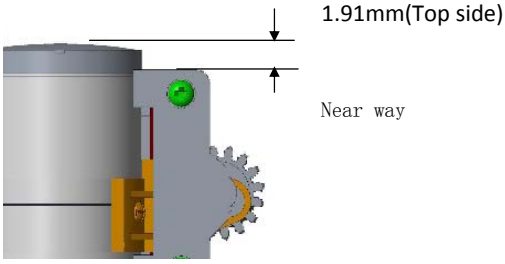


Figure 7

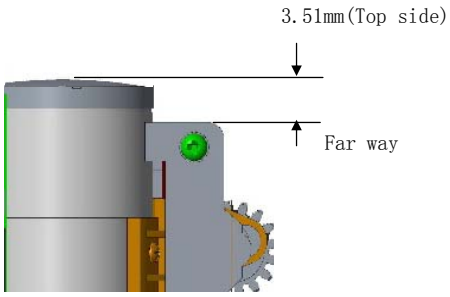


Figure 8

3.4The Rays Cup Design

1. Range Of Effective Rays（Refer to 3D Model）

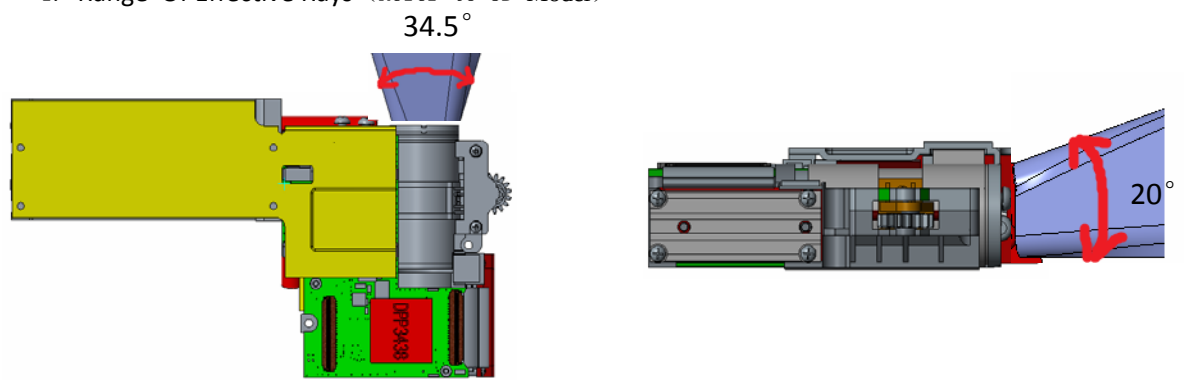


Figure 9

2. Requirement

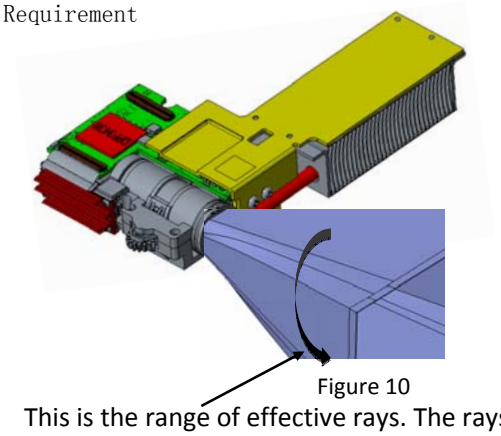
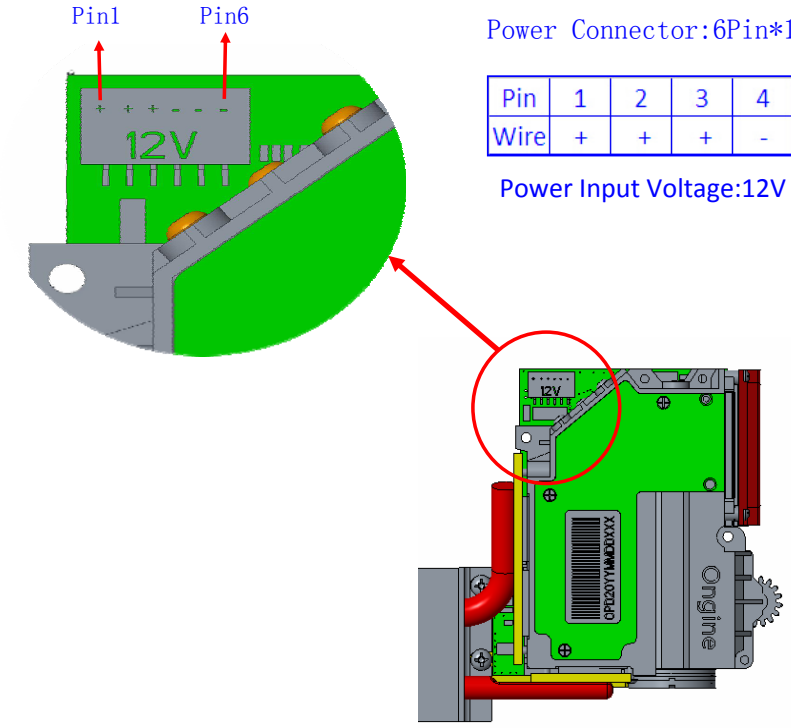


Figure 10

This is the range of effective rays. The rays cup should be to avoid interference the cup internal should use extinction processing

3.5 Connection Port

1)Power Input Support



Power Connector:6Pin*1.0mm

Pin	1	2	3	4	5	6
Wire	+	+	+	-	-	-

Power Input Voltage:12V

Figure 11

2)Drivering board - Main board connection port

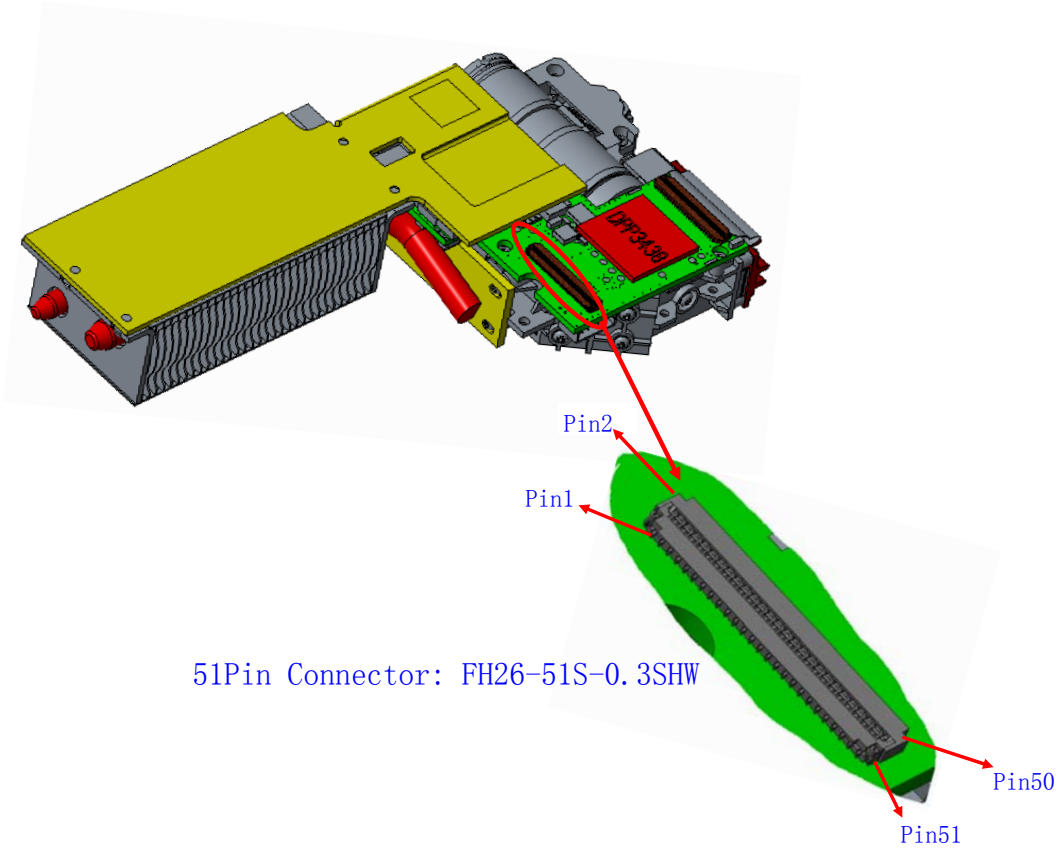


Figure 12

4、Heat Dissipation

4.1 Heat Dissipation, follow the rules as the below:

1. Led and Display chip temperature must meet the spec requirment.
2. Within the acceptance of fan noise and finished product dimension,increase air flow rate and product volume to
3. DMD requires the fan or the design of air passage, the air go through and cool down it.

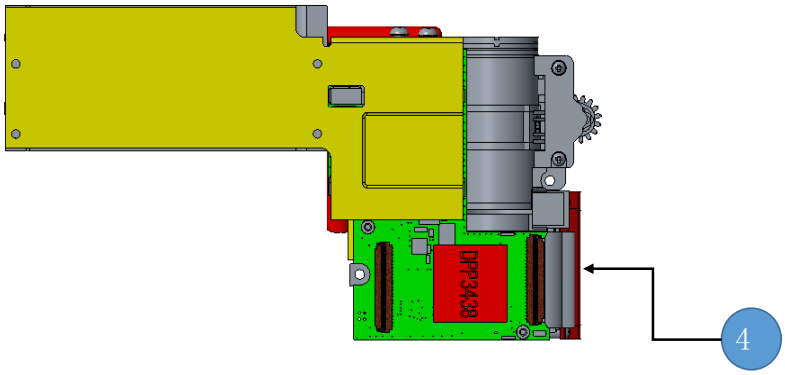


Figure 13

4.2 LED Source thermal testing proint,please let the softwave scan from the Pin37th of 51Pin connector or test it manually.The relation between Voltage&Temperature please reference to the flow table.

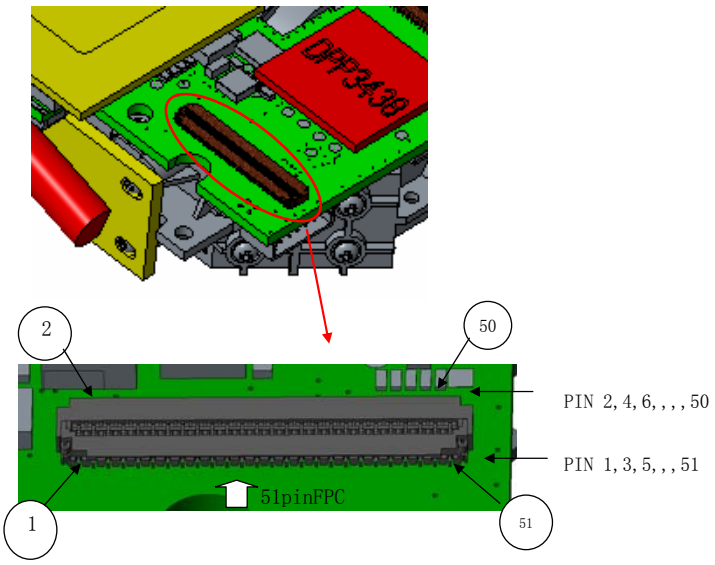
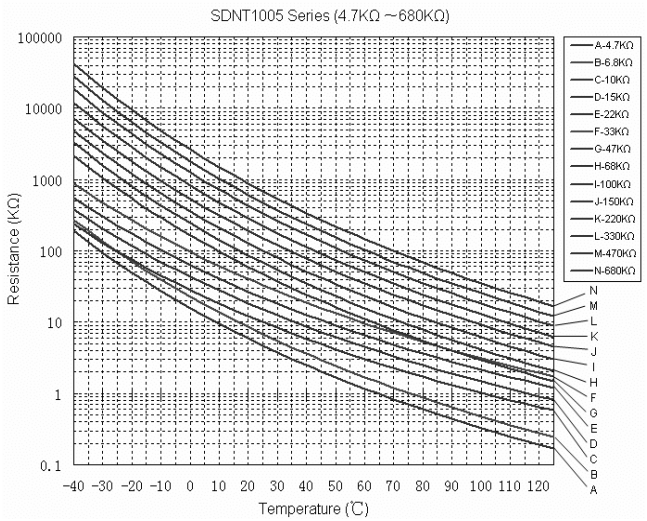


Figure 14

Reference Standard(Spec.):

T-R（10KΩ）



V-T

Voltage(V)	Temperature(°C)
1.7	26.7
1.6	29.7
1.5	32.8
1.4	36.2
1.3	39.6
1.2	43.4
1.1	47.2
1	51.4
0.9	56
0.8	61.8
0.7	66.8
0.6	73.1

4.3 Fan and the Wind Flow suggestion as flow.

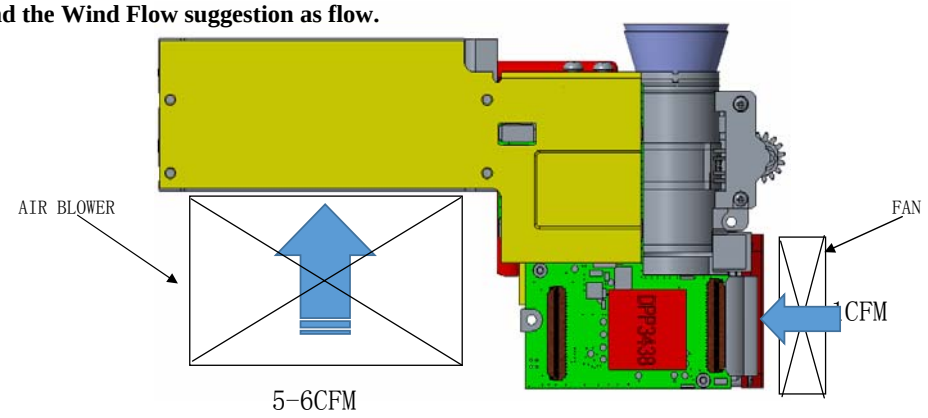


Figure 15

5、Electronic Function

5.1 Block diagram

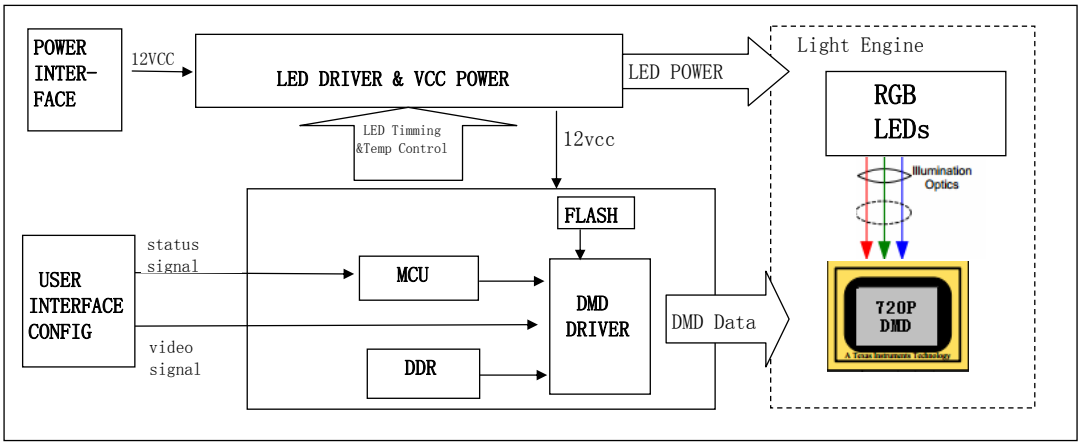


Figure 16. Panel block diagram

6、Electrical Interfaces

6.1 Features

1.Display image resolution:720P (1280*720)

2.Input image bus mode: Parallel bus(RGB888/RGB666/BT656/CPU I/F MODE)

3.Input image sizes: max to 720P (1280*720)

4.Adjustable brightness

5.Support image horizontal and vertical flip

6.Frame rate(60Hz/50Hz)

7.Vsync, Hsync, Pixel clock and DATEN polarity control

8.Temperature control protection by switch Leds status

9. Support Un-packed, Frame Sequential, 3D format

6.2 Input image interface

Parallel bus (RGB 888/RGB666/BT656/CPU I/F MODE) input format

Assignment of User Interface Connector（51pin）

Black font indicates the default input data

User Interface Connector Signal Definitions								
PIN#	PIN NAME	I/O	Description	RGB888	RGB666	BT656	CPU I/F	NOTE
PIN1	CPUVSYNC	I/O	CPU SYNC(CPU I/F)	PullDown	PullDown	PullDown	CPUVSYNC	note1
PIN2	DATEN_CMD	I	Active data	DAT_EN	DAT_EN	DAT_EN	/Command	note2
PIN3	PCLK	I	Pixel Clock	CLK	CLK	CLK	Unused	note2
PIN4	VSYNC_WE	I	Vertical sync. Clk	VSYNC	VSYNC	VSYNC	/Write Enable	note2
PIN5	HSYNC_CS	I	Horizontal sync.Clk	HSYNC	HSYNC	HSYNC	/Chip Select	note2
PIN6	GND	GND	Ground	GND	GND	GND	GND	
PIN7	PDATA0	I	RGB DATA	BLUE_D0	Blue_D0	BT656_Data0	CPU_Data0	note3
PIN8	PDATA1	I	RGB DATA	BLUE_D1	Blue_D1	BT656_Data1	CPU_Data1	
PIN9	PDATA2	I	RGB DATA	BLUE_D2	Blue_D2	BT656_Data2	CPU_Data2	
PIN10	PDATA3	I	RGB DATA	BLUE_D3	Blue_D3	BT656_Data3	CPU_Data3	
PIN11	PDATA4	I	RGB DATA	BLUE_D4	Blue_D4	BT656_Data4	CPU_Data4	
PIN12	PDATA5	I	RGB DATA	BLUE_D5	Blue_D5	BT656_Data5	CPU_Data5	
PIN13	PDATA6	I	RGB DATA	BLUE_D6	GREEN_D0	BT656_Data6	CPU_Data6	
PIN14	PDATA7	I	RGB DATA	BLUE_D7	GREEN_D1	BT656_Data7	CPU_Data7	
PIN15	GND	GND	Ground	GND	GND	GND	GND	
PIN16	PDATA8	I	RGB DATA	GREEN_D0	GREEN_D2	NC	CPU_Data8	
PIN17	PDATA9	I	RGB DATA	GREEN_D1	GREEN_D3	NC	CPU_Data9	
PIN18	PDATA10	I	RGB DATA	GREEN_D2	GREEN_D4	NC	CPU_Data10	
PIN19	PDATA11	I	RGB DATA	GREEN_D3	GREEN_D5	NC	CPU_Data11	
PIN20	PDATA12	I	RGB DATA	GREEN_D4	RED_D0	NC	CPU_Data12	
PIN21	PDATA13	I	RGB DATA	GREEN_D5	RED_D1	NC	CPU_Data13	
PIN22	PDATA14	I	RGB DATA	GREEN_D6	RED_D2	NC	CPU_Data14	
PIN23	PDATA15	I	RGB DATA	GREEN_D7	RED_D3	NC	CPU_Data15	
PIN24	GND	GND	Ground	GND	GND	GND	GND	
PIN25	PDATA16	I	RGB DATA	RED_D0	RED_D4	NC	CPU_Data16	
PIN26	PDATA17	I	RGB DATA	RED_D1	RED_D5	NC	CPU_Data17	
PIN27	PDATA18	I	RGB DATA	RED_D2	NC	NC	CPU_Data18	
PIN28	PDATA19	I	RGB DATA	RED_D3	NC	NC	CPU_Data19	
PIN29	PDATA20	I	RGB DATA	RED_D4	NC	NC	CPU_Data20	
PIN30	PDATA21	I	RGB DATA	RED_D5	NC	NC	CPU_Data21	
PIN31	PDATA22	I	RGB DATA	RED_D6	NC	NC	CPU_Data22	
PIN32	PDATA23	I	RGB DATA	RED_D7	NC	NC	CPU_Data23	
PIN33	GND	GND	Ground	GND				
PIN34	NC	-	NC	NC				
PIN35	NC	-	NC	NC				
PIN36	NC	-	NC	NC				
PIN37	PROJ_ON	I	Control System on/off	1:Open System 0:Close System				
PIN38	NC	-	NC	NC				
PIN39	NC	-	NC	NC				
PIN40	NC	-	NC	NC				
PIN41	NC	-	NC	NC				
PIN42	IIC_SDA	I	IIC SDA	IIC				note5
PIN43	IIC_SCL	I	IIC_SCL	IIC				note5
PIN44	GND	GND	Ground	GND				
PIN45	NC	-	NC	NC				
PIN46	NC	-	NC	NC				
PIN47	TMEP_ERR	O	System Temp Status	ADC OUTPUT				note6
PIN48	LED_CTL	I	contral LED on/off	1:Open Led lamp 0:Close Led lamp				note4
PIN49	NC	-	NC	NC				
PIN50	GND	GND	GROUND	GND				
PIN51	GND	GND	GROUND	GND				

Figure 17. Signal interface diagram

Note：

1. Following by TI DMD Electronic Static requirment, Static Volatage must be under 2000V for the direct static contact to DMD.
2. Due to the optical engine has electronic connection with DMD, OPD21M Optical Eninge must be not more than 2000V static volatge.

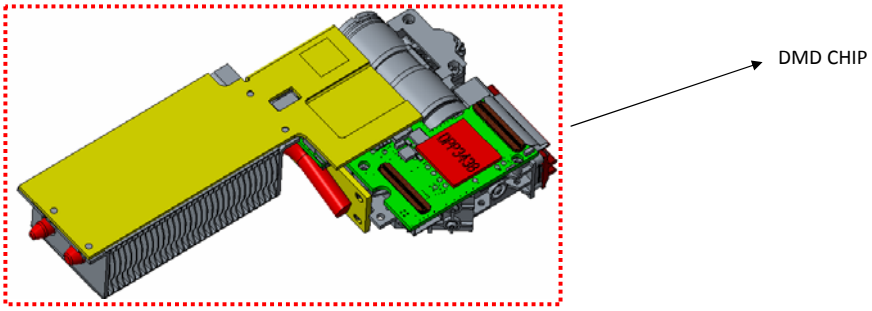


Figure 18

6.3 Notes:

1. CPUVSYNC : the signal be used in CPU I/F mode,other mode please pull down.
2. Video control signals, please pay special attention to the polarity, and see the default settings.
3. PDATA(23:0) bus mapping is pixel format and source mode dependent.
4. Led control signal,we can used to open and close the lamp after system normal.
5. External control functions can be achieved by the IIC, such as image flips,resolution changes, the interface mode.
6. Temperature status indication, TBD.

7、 Input features of RGB888 666

System enter RGB888 interface source mode when power on(default setting)

RGB666 mode source must be setted by iic interface,we described in auxiliary document.

7.1 Parallel Bus Mode

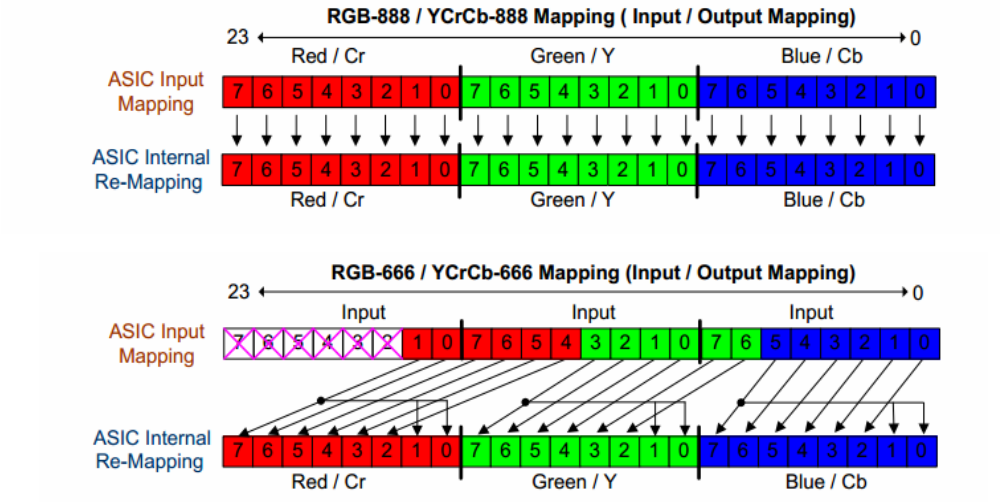


Figure 19

7.2 Parallel Interface(RGB888) Timing

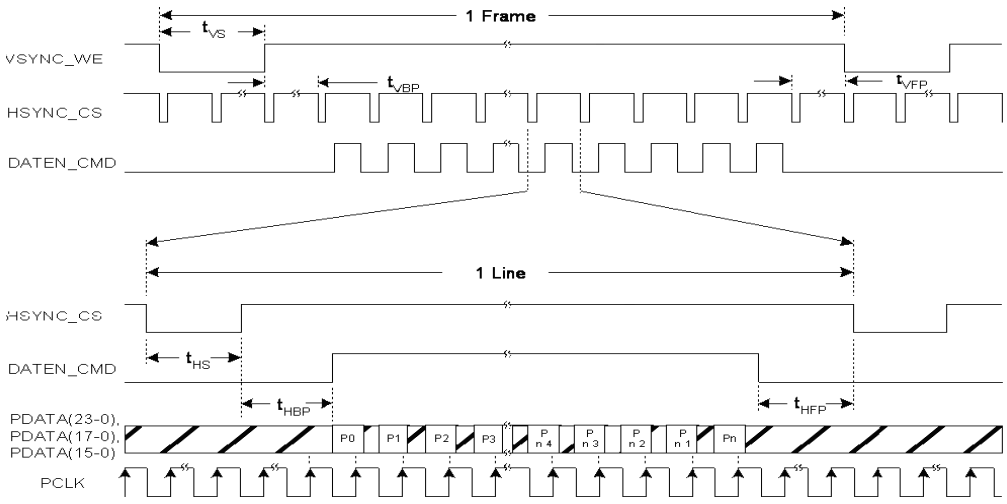


Figure 20

Note:

The description of parameters is according to following signal polarity setting.

(1) Defines the pixel clock edge is sampled on rising edge.

(2) Defines the polarity of the incoming VSYNC signal is Active-low.

(3) Defines the polarity of the incoming HSYNC signal is Active-low.

(4) Defines the polarity of the incoming DATEN_CMD signal is Active-high

8、 Input Features Of BT.656

BT.656 mode source must be setted by iic interface we described in auxiliary document.

8.1 Parallel Bus

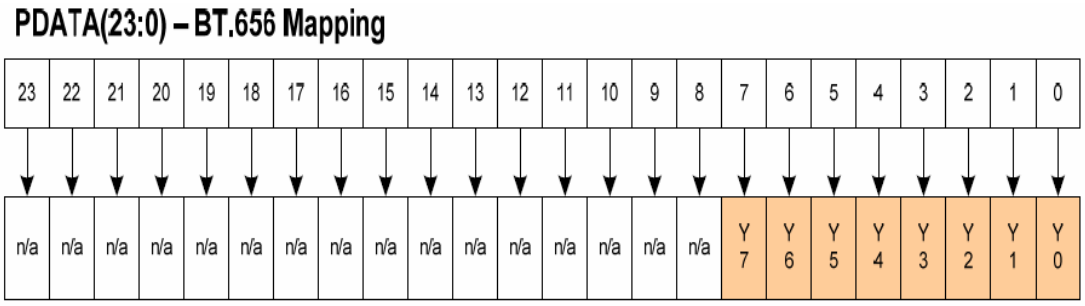


Figure 21.Parallel & BT.656 I/F General Timing

8.2 Parallel & BT.656 I/F General Timing

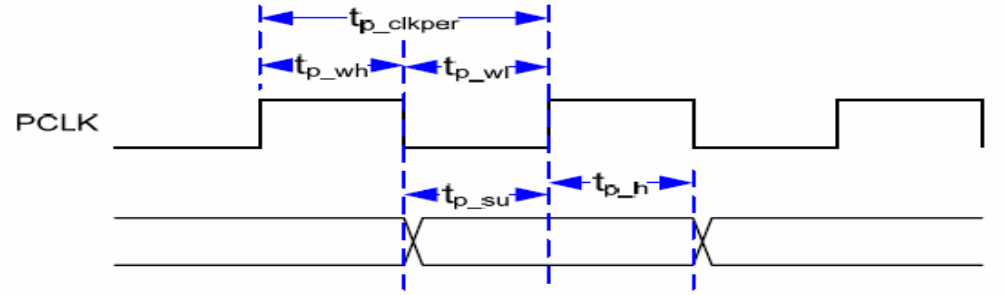


Figure22

BT.656 I/F General Timing Requirements

Parameter	Description	Test Condition	Min	Max	Unit
f_{clock}	Clock Frequency, PCLK		1.0	33.5	MHz
t_{p_clkper}	Clock Period, PCLK	50% reference points	29.85	1,000	ns
t_{p_clkjit}	Clock Jitter, PCLK	Max f_{clock}	See note 1	See note 1	
t_{p_wh}	Pulse Width Low, PCLK	50% reference points	10.0		ns
t_{p_wl}	Pulse Width High, PCLK	50% reference points	10.0		ns
t_{p_su}	Setup Time – PDATA(7:0) before the active edge of PCLK	50% reference points	3.0		ns
t_{p_h}	Hold Time – PDATA(7:0) after the active edge of PCLK	50% reference points	3.0		ns
t_t	Transition Time – all signals	20% to 80% reference points	0.2	4.0	ns

8.3 Notes:

1. This range include the 200ppm of the external reference clock oscillator (PLL_REFCLK)
2. Setup and hold times must be met during clock jitter.
3. Clock jitter should be calculated using this formula: Jitter = [1/ fclock – 28.35ns].

9、 Power and Initialization

9.1 Power On Sequencing

Absolute maximum ratings over recommended operating free-air temperature range (unless otherwise noted)†

Supply voltage range (see Note 1, 2):
- V_{DD} (Core) ..... -0.3 V to 1.21 V
- V_{DDLP12} (DSI-DHY LP I/O) ..... -0.3 V to 1.32 V
- VCC18 (All 1.8 V Power + sub-LVDS) ..... -0.3 V to 1.96 V
- VCC_INTF (Host I/O Power) ..... -0.3 V to 3.60 V
  - VCC_INTF (if 1.8V Power used) ..... -0.3 V to 1.99 V
  - VCC_INTF (if 2.5V Power used) ..... -0.3 V to 2.75 V
  - VCC_INTF (if 3.3V Power used) ..... -0.3 V to 3.60 V
- VCC_FLSH (Flash I/O Power) ..... -0.3 V to 3.60 V
  - VCC_FLSH (if 1.8V Power used) ..... -0.3 V to 1.96 V
  - VCC_FLSH (if 2.5V Power used) ..... -0.3 V to 2.72 V
  - VCC_FLSH (if 3.3V Power used) ..... -0.3 V to 3.58 V
- VDD_PLLM (MCG PLL) ..... -0.3 V to 1.21 V
- VDD_PLLD (1DCG PLL) ..... -0.3 V to 1.21 V

Operating junction temperature range, T_J ..... -30°C to 125°C

Storage temperature range, T_{stg} ..... –40°C to 125°C

Electrostatic discharge voltage using the: Human Body Model ..... +/- 2000 V (3)
Electrostatic discharge voltage using the: Charged Device Model..... +/- 500 V (3)

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:

(1) All voltage values are with respect to GND.

(2) Overlap currents, if allowed to continue flowing unchecked, not only increase total power dissipation in a circuit but degrade the circuit reliability thus shortening its usual operating life.

Recommended operating conditions

	PARAMETER	NOTE	MIN	TYP	MAX	UNIT
VDD	Core Power 1.1V (Main 1.1V)	+/- 5% tolerance	1.045	1.10	1.155	V
VDDLP12	DSI PHY Low Power mode driver supply (1.1V) or (1.2V)	+/- 5% tolerance See Note 2,4,5	1.02 1.12	1.1 1.2	1.18 1.28	V
VCC18	All 1.8V I/O Power: (1.8V power supply for all I/O other than the Host/ Parallel I/F & the SPI Flash I/F. This includes RESETZ, PARKZ LED_SEL, CMP, GPIO, IIC1, TSTPT & JTAG pins)	+/- 8.5% tolerance	1.64	1.8	1.96	V
VCC_INTF	Host / Parallel Interface I/O Power: 1.8 to 3.3V (Includes IIC0, PDATA, Video Syncs & HOST_IRQ pins)	+/- 8.5% tolerance See Note 2	1.64 2.28 3.02	1.8 2.5 3.3	1.96 2.72 3.58	V
VCC_FLSH	Flash Interface I/O Power:1.8 to 3.3V	+/- 8.5% tolerance See Note 2	1.64 2.28 3.02	1.8 2.5 3.3	1.96 2.72 3.58	V
VDD_PLLM	MCG PLL 1.1V power	+/- 9.1% tolerance See Note 3	1.025	1.1	1.155	V
VDD_PLLD	DCG PLL 1.1V power	+/- 9.1% tolerance See Note 3	1.025	1.1	1.155	V
T_A	Operating ambient temperature range		-30		85	°C
T_C	Operating top center case temperature					°C
T_J	Operating junction temperature		-30		105	°C

Notes:

(1) The number inside each parenthesis for the I/O refers to the type defined in the I/O type subscript definition section.

(2) These supplies have multiple valid ranges.

(3) These I/O supply ranges are wider to facilitate additional filtering.

(4) If DSI is not needed, then DSI LP supply (VDDLP12) should be tied to 1.1V core supply. If DSI is needed, then the OEM has the option to run VDDLP12 at 1.1V nominal (and tie it to the VDD supply) or 1.2 V nominal. If 1.1V VDDLP12 is used, then this will meet all MIPI specifications at the host but this is not as explicitly defined by MIPI.

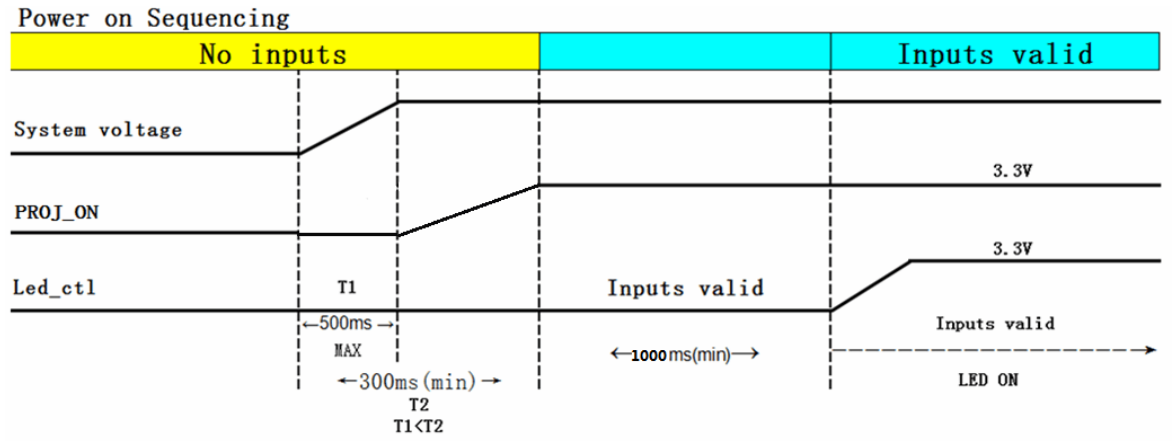
(5) When DSI-PHY LP supply (VDDLP12) is fed from a 1.2V supply, the 1.2V power must sequence ON before the 1.1V core supply

(6) The Operating Ambient temperature range assumes zero forced air flow, a JEDEC JESD51 Junction to Ambient Thermal Resistance value at zero forced air flow (RthetaJA at 0 m/s), a JEDEC JESD51 standard test card and environment, along with min and max estimated power dissipation across process, voltage and temperature. Thermal conditions will vary by application which will impact RthetaJA. Thus maximum operating ambient temperature will vary by application.

- Ta_min = Tj_min - (Pd_min * RthetaJA) = -30C - (0.0W * 30.3 C/W) = -30 C
- Ta_max = Tj_max - (Pd_max * RthetaJA) = +105C - (0.348W * 30.3 C/W) = +94.4 C

Power On Sequencing

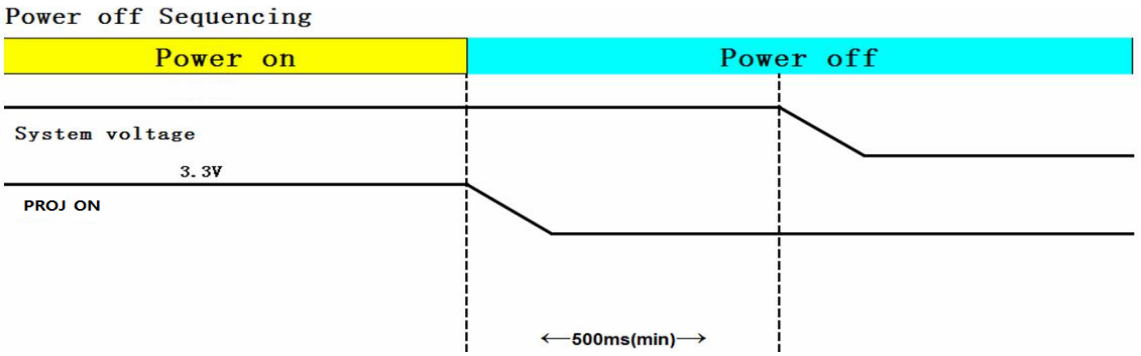
When OPD20M module power on ,system will running normally within 2 seconds,the port LED_CTL can be used to control LED switch time, so we have enough time preper video image singals or switch to the other source mode,resolution,frequery,light,flip mode.We advise to provide the appropriate control signal Based default setting.



Power Off Sequencing

1:Must enter PROJ_ON PIN37 ==> 0

2:Reset System voltage ==> 0



10、 Resolution setting

The default resolution of OPD21M module is 720P. We can change it to other resolution by IIC commands.The setting method is explained in auxiliary document.

Resolution	Pixel Clock	H/V Timing	Frequency	Active	Sync	Back Porch	Front Porch	Total
720P	74.25M	H Timing	45K Hz	1280	40	220	110	1650
		V Timing	60 Hz	720	5	20	5	750

11、 Brightness,Frequency setting and White Balance sequence select.

OPD21M module support 3 mode white balance sequece select:

1. Freq 50-60Hz and High Brightness white balance.
2. Freq 50-60Hz and Low Brightness white balance.
3. 3D Format

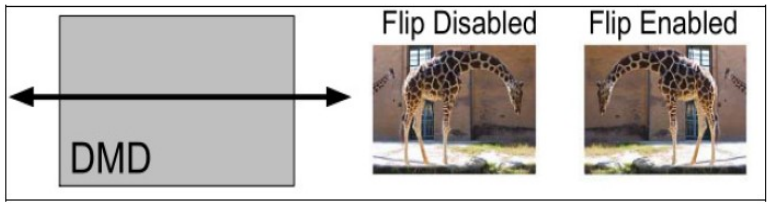
The Control method described in the auxiliary document

12、Long&Short Flip Setting.

OPD20M module support 2 mode flips,long axis flip(HOR.)and short axis flip.

Flip mode can be selected by iic commands,detail in auxiliary document.

Long axis flip means this:



Short axis flip means this:

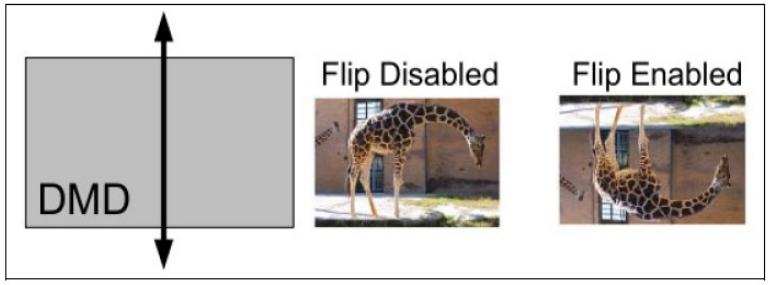


Figure 17

13、Module Default Setting

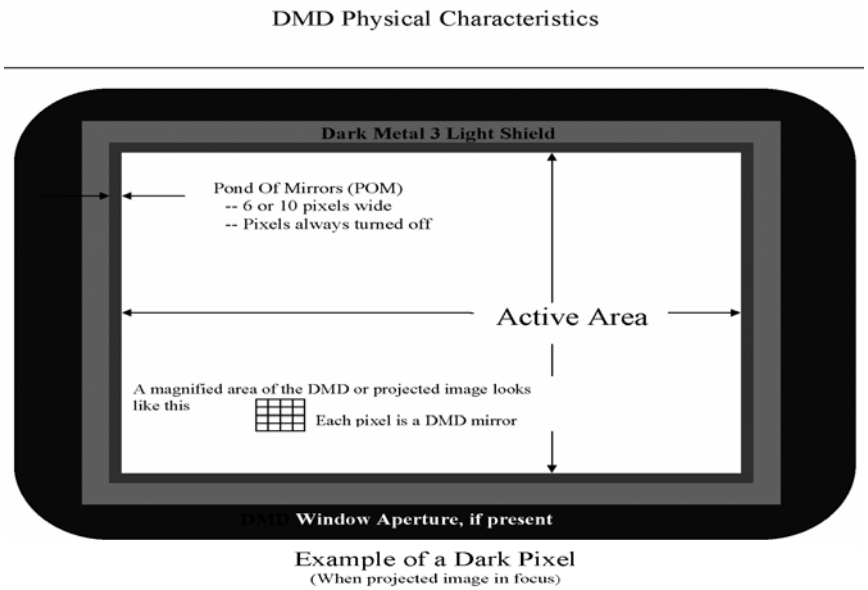
Initial signal status	Factory Default Value
Led power (6PIN Contect)	12V
Input Resolution	854*480
Data Format	RGB888
Vsync,Hsync and Daten Polarity	Vsync,Hsync,Dataen(Low,Low,High)
PWR_ENB(PIN_38)	1 (Power on enable)
LED_CTL(PIN_37)	1 (Open Led lamp)
CURRENT_CTL(PIN_48)	0 (Low Light,Pico projector current 12V/0.38A)
Temperature of Protection	80℃ MAX(RED LED)

14、Electrostatic Discharge Immunity

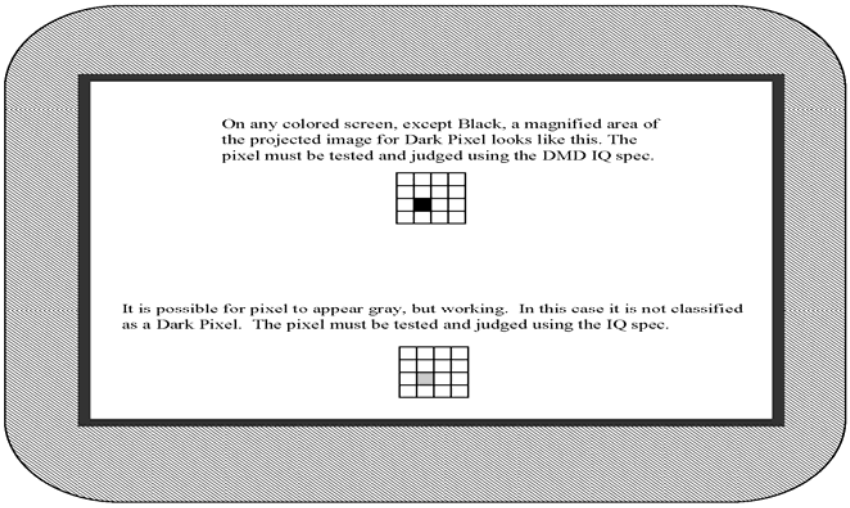
All external signals on the OPD20M module are protected from damage by electrostatic discharge,and are tested inaccordance with JESD22-A114-B Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model(HBM).Add attached file "DMD Artifact Illustration& ESD"for reference.

DMD ESD Protection Limits		
Package Pin Type	Voltage (maximum)	Units
Input	2000	V
Output	2000	V
Power	2000	V

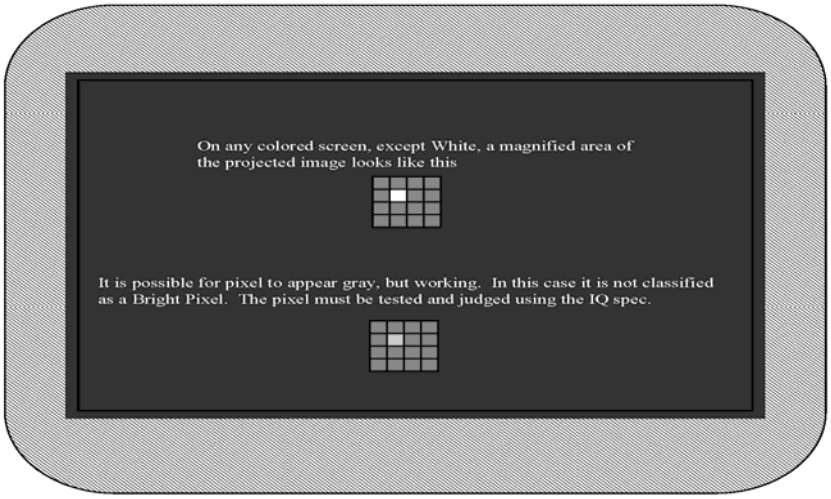
15、DMD Artifact Illustration



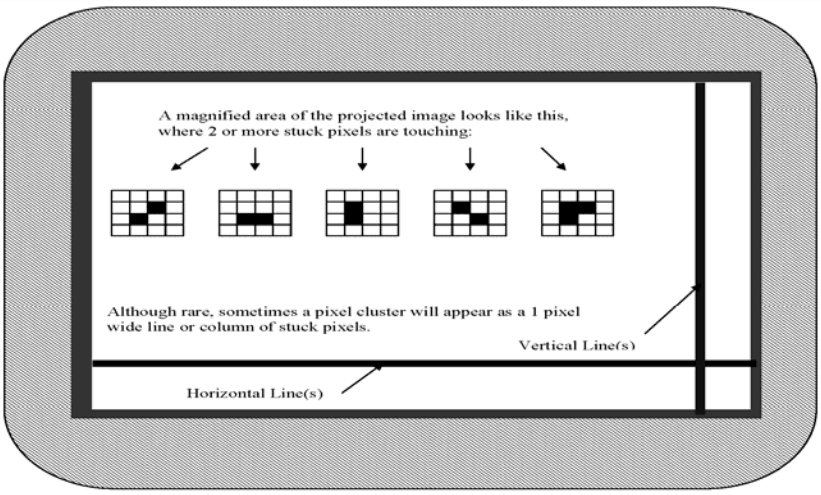
Example of a Dark Pixel
(When projected image in focus)



Example of a Bright Pixel
(When projected image in focus)

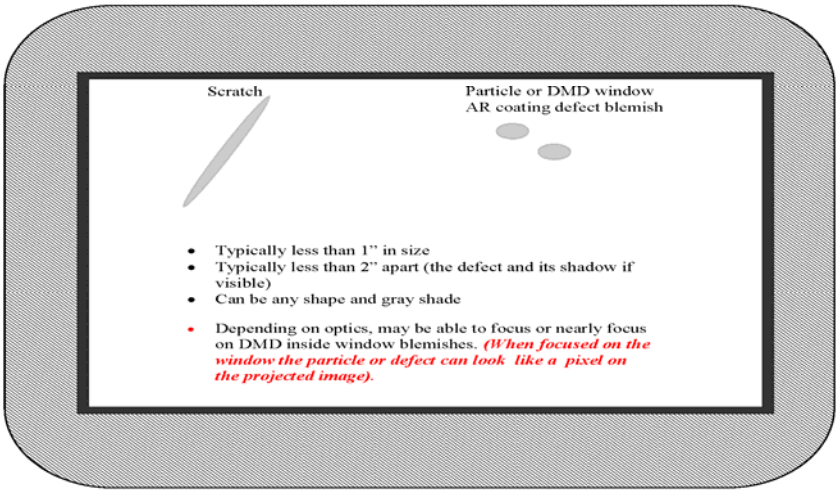


Examples of Adjacent Stuck Pixels
(Also called Clusters)

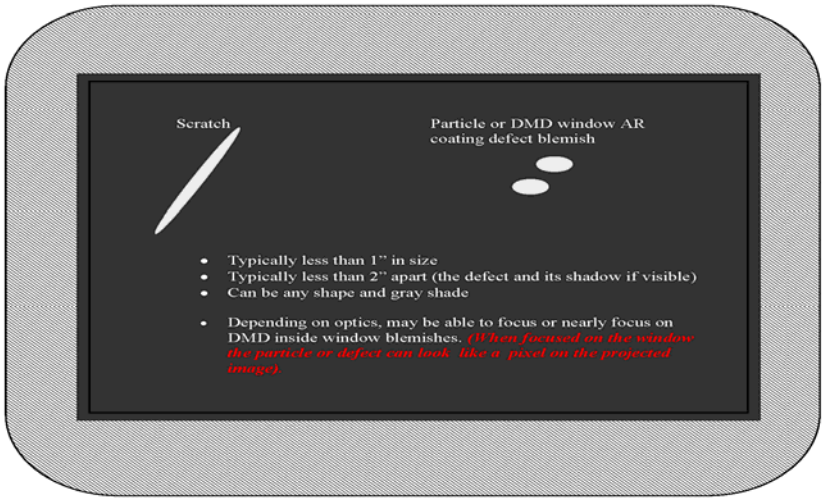


Example of Dark Blemish **Inside the DMD**

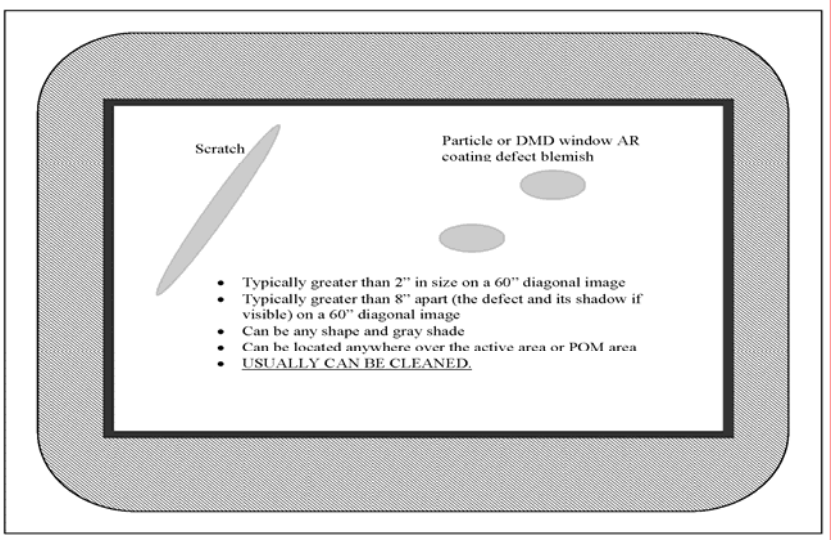
Blemishes can be caused by defects on the DMD window or other surfaces in the optical path to the DMD. Reference the applicable Image Quality spec for the intensity, size, and quantity, for of allowable DMD blemishes.



Example of Light Blemish **Inside the DMD**



Examples of Dark Blemish **Outside the DMD**



If any of the example artifacts are seen,we ask you please do the following:

► Reference IQ spec for PASS/FAIL

1. SCOPE

This document specifies the image quality requirements applicable to the DLP® .3 WVGA Component Sets. The Component Set provides the DLP® .3 WVGA Projector with digital imaging functionality based on Digital Micromirror Device (DMD) technology.

2. Definitions

2.1 Blemish

A blemish is an obstruction, reflection, or refraction of light that is visible, but out of focus in the projected image under specified conditions of inspection (see Table 1). It is caused by a particle, scratch, or other artifact located in the image illumination path.

2.2. Dark pixel

A single pixel or mirror that is stuck in the OFF position and is visibly darker than the surrounding pixels.

2.3. Bright pixel

A single pixel or mirror that is stuck in the ON position and is visibly brighter than the surrounding pixels.

2.4. Unstable pixel

A single pixel or mirror that does not operate in sequence with parameters loaded into memory. The unstable pixel appears to be flickering asynchronously with the image.

2.5. Adjacent pixel

Two or more stuck pixels sharing a common border or common point, also referred to as a cluster.

2.6. Row or Column Defect

Dark or Light column(s) or row(s) are groups of pixels that are not operating or are not operating in sequence with the parameters loaded into memory.

2.7. Pond of Mirrors (POM)

POM is a rectangular array of off-state mirrors surrounding the active area.

2.8. Eyecatcher

Eyecatcher's are blemishes appearing in the area outside of the Active Area. These are due to particles and various DMD window or window aperture “defects” including: digs, voids, and scratches.

2.9. Border Artifacts

Border artifacts are a general category of image artifacts that may show up on screen in the area outside of the active array. Border artifacts include: Exposed Bond Wires, Exposed Metal 2, and Reflective Edge.

2.9.1. Bond Wires

Bond Wires are the electrical connections between the die and the DMD ceramic package. If visible, they will appear as short light parallel lines outside of the Pond of Mirrors (POM).

2.9.2. Exposed Metal 2

Exposed Metal 2 is due to a shift in positioning of either the die or the window aperture, which may allow light to be reflected off of the layer of metal 2 that is below the super structure (mirrors). This defect is located outside of the POM.

2.9.3. Reflective Edge

Reflective Edge is light that may reflect from the edge of the DMD window aperture onto the projection screen. It will appear as a thin diffuse line outside of the POM.

2.10. Gray 10 Screen

All areas of the screen are colored a Microsoft Paintbrush gray 10 (green, red, and blue set at 10).
NOTE: If linear degamma is not used then the Microsoft Paintbrush values must be adjusted to match the degamma table being used in order to generate an equivalent gray level on the test screen image. An equivalent Gray level would be any Gray screen with a lux level $\geq$ 4% of the projectors White screen lux level.

3. ACCEPTANCE REQUIREMENTS

3.1. Conditions of Acceptance

All DMD image quality returns will be evaluated using the following projected image test conditions:

a. Test Set degamma shall be linear.
b. Test Set brightness and contrast settings shall be set to nominal.
c. The diagonal size of the projected image shall be a minimum of 20 inches.
d. The projection screen shall be 1X gain.
e. The projected image shall be inspected from a 38 inch minimum viewing distance.
f. The image shall be in focus during all Table 1 tests.
g. Maximun Lumens on Active Array (mirrors) is 100.

TABLE 1. Image Quality Specification

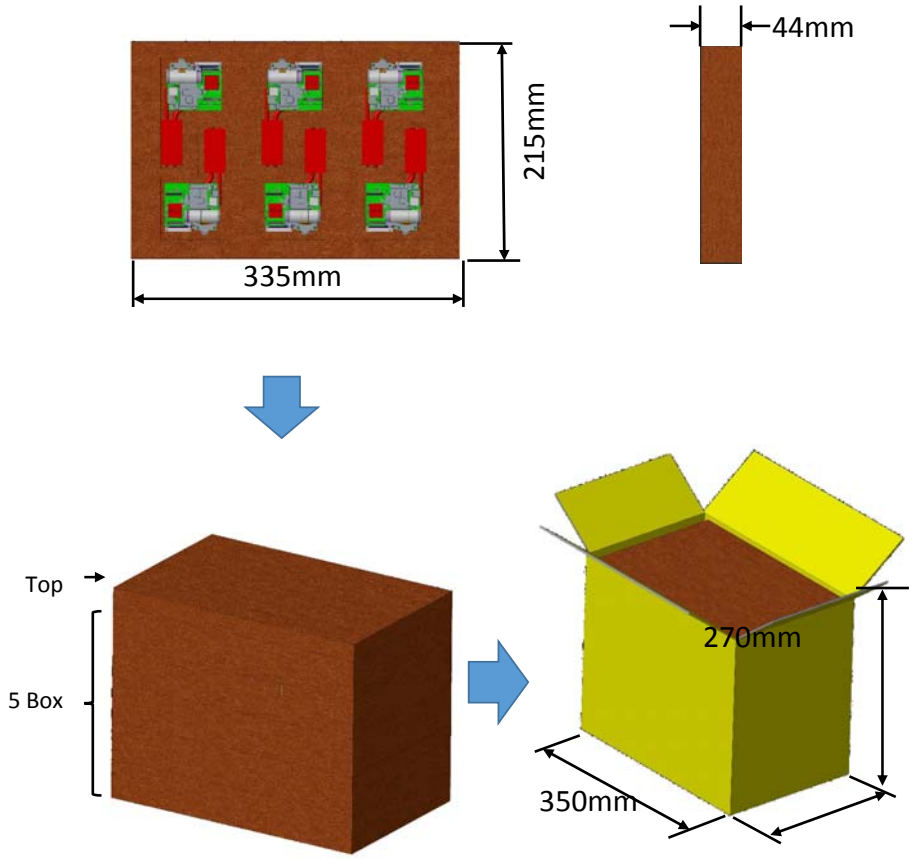
SCREEN	ACCEPTANCE CRITERIA
Gray 10	1. No Bright Pixels in Active Area 2. ≤ 1 Bright Pixels in the POM
White	1. ≤ 4 Dark Pixels in the Active Area
Any screen	1. No Adjacent Pixels/Clusters 2. No Unstable Pixels in Active Area 3. No DMD window aperture shadowing on the Active Area 4. No Row or Column defects 5. Blemishes are allowed 6. Eyecatcher and Border Artifacts are allowed

Notes:

1. Projected blemish numbers include the count for the shadow of the window artifact in addition to the artifact itself.
2. During all Table 1 tests, projected images shall be inspected in accordance with the conditions of inspection specified in Section 3.
3. The rejection basis for all cosmetic DMD defects (scratches, nicks, particles) will be the projected image tests referenced in Table 1.
4. Devices that meet this image quality specification but are deemed undesirable by the customer may not be returned to TI without prior approval by TI.
5. Screens < Gray10 shall not be used as a basis for rejecting a DMD for image quality.

16.Package

Package：6PCS/BOX (335*215*44)
30PCS/BIN(350*230*270)



Package front view