LELEC2660 - Project - Report 2
Design of input and output capacitances and snubber circuit

Delait Louis, **Nachtergaele** Louis

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1 Introduction

This report take place in the design an AC-DC converter made of a **full-bridge single phase diode rectifier** and a **flyback converter** placed in series as shown in Figure 1.

More precisely we will in this second report design the input and output capacitances C_{in} and C_{out} and the snubber circuit (made of R_{sn} and C_{sn}) used in this circuit.

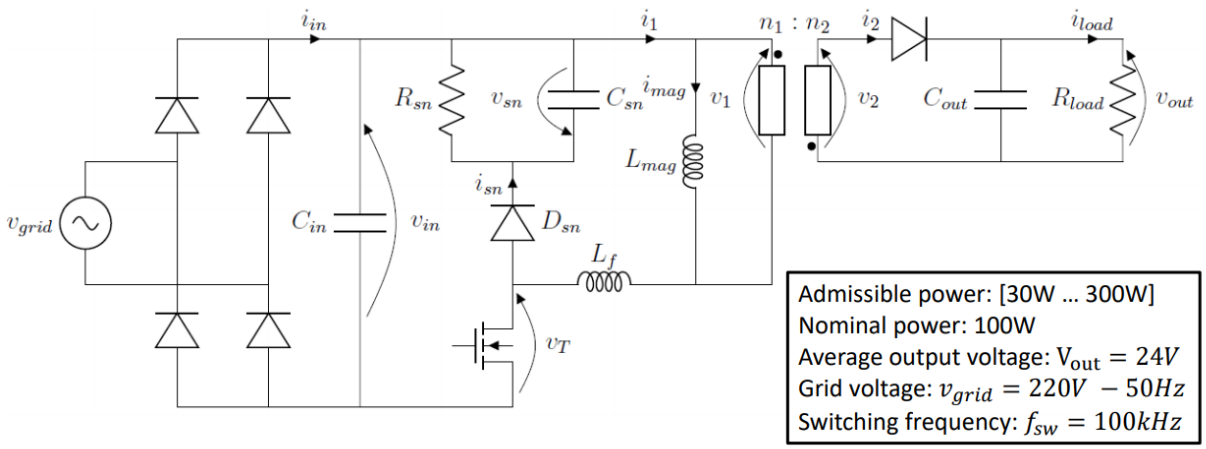

Figure 1: full circuit

2 Input Capacitance Design

2.1 Hypotheses

1. C_{in} must be design so that we can neglect the ripple on V_{in}. We will then assume that ΔV is low compared to V_{in}. We will allow for the design a maximum ripple of 20[V] as in the previous report.
2. The time during which C_{in} is discharging is approximately equal to $T_{grid}/2$.
3. We neglect the ripple on i_1 and only consider its average value. As the left part of the circuit ideally correspond to a DC source.
4. METTRE DESSIN We consider $t_2 \approx T_{grid}/4$, i_{in} being different from 0 from t_1 to t_2
5. For very small arguments x, $sin(x) \approx x$ by Taylor approximation of first order
6. For very small arguments x, $cos(x) \approx 1 + x^2$ by Taylor approximation of second order

2.2 Explanation and computation of value

2.2.1 Minimum value of C_{in}

C_{in} must be design so that we can neglect the ripple on V_{in}. We thus have to find a relation between C_{in} and the ripple ΔV DESSIN de DELTA.
First, by studying the energy stored in C_{in}, ΔU_s (for $t \in [t_1, t_2]$): We know that

$$\Delta U_s = \frac{C_{in}(V_{max}^2 - V_{min}^2)}{2} \tag{1}$$

Using the fact that $V_{in} = V_{max} - \Delta V$ (see figure 2) and the Hypothesis (1):

$$\Delta U_s \approx C_{in} V_{max} \Delta V \tag{2}$$

Using the second Hypothesis, we can write the energy delivered to the flyback converter ΔU_s (for $t \in [t_2, t_1 + T_{grid}/2]$) :

$$\Delta U_d \approx \frac{P_{load} T_{grid}}{2} \tag{3}$$

As the total energy variation during $T_{grid}/2$ on the input capacitor must be equal to 0 we have that:

$$C_{in} = \frac{P_{load}}{2\Delta V V_{max} f_{grid}} \tag{4}$$

We can deduce from this previous equation a minimum value for C_{in} by taking the worst case for each variable. We then find $C_{in,min} = \frac{300}{2 \cdot 20 \cdot 311 \cdot 50} = 483[\mu F]$

2.2.2 Support the current $i_{Cin,RMS}$ at 100Hz

To know if the selected capacitor can handle the current $i_{Cin,RMS}$ at 100Hz, we have to find an expression of this current.

First, the RMS value of i_{Cin} can be expressed as

$$i_{Cin,RMS} = \sqrt{\frac{1}{T_{grid}/2} \int_0^{T_{grid}/2} i_{Cin}^2(t) dt}$$

By applying a Kirchoff current law we have that $i_{Cin} = i_{in} + i_1$. The Hypothesis (3) allow us to write that $i_{1,avg} = i_{1,RMS}$ and the following equation can be rewriten as

$$i_{Cin,RMS}^2 = i_{in,RMS}^2 + i_{1,avg}^2 - 2 i_{1,avg} i_{in,avg} \tag{5}$$

Furthermore as $i_{Cin,avg} = 0 \rightarrow i_{1,avg} = i_{in,avg}$

$$i_{Cin,RMS}^2 = i_{in,RMS}^2 - i_{1,avg}^2 \tag{6}$$

$i_{1,avg}$ is a known value and its expression is $i_{1,avg} = \frac{P_{load}}{V_{in}}$.
In the worst case ($P_{load} = 300[W]$) and as we assume the main value of $v_{in}(t)$ was equal to 300[v], we get $i_{1,avg} = 1[A]$

The RMS value of i_{in} can be computed as followed
we can express the current i_{in} as

$$i_{in} = \begin{cases} i_{Cin} + i_1 & t \in [t_1, t_2] \\ 0 & t \in [t_2, t_1 + T_{grid}/2] \end{cases} \tag{7}$$

With

$$i_{Cin} = C_{in} \frac{dV_{in}}{dt} = C_{in} \sqrt{2} V_{grid} \omega_g cos(\omega_g t)$$

As $cos(x) = sin(\pi/2 - x)$, we can rewrite this as

$$i_{Cin} = C_{in} \sqrt{2} V_{grid} \omega_g sin(\omega_g (\frac{T_{grid}}{4} - t))$$

By using the Hypothesis (5) (we look at the system during a period where t is near from $\frac{T_{grid}}{4}$) we get

$$i_{Cin} = C_{in} \sqrt{2} V_{grid} \omega_g^2 (\frac{T_{grid}}{4} - t) \tag{8}$$

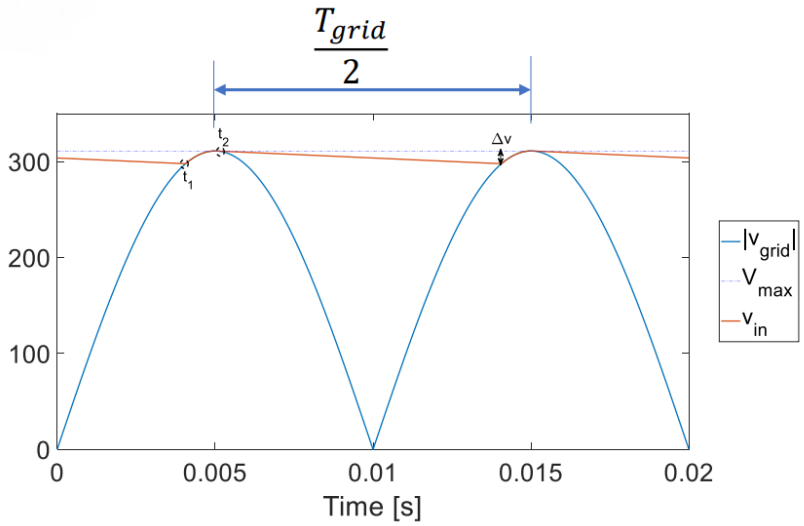

Figure 2: $v(t)$

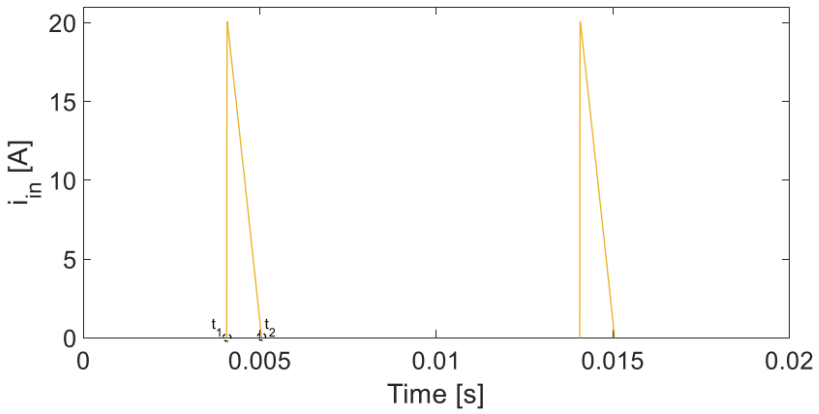

Figure 3: $i_{in}(t)$

That shows the linear dependence between i_{in} and t.

Finally we get for The RMS value of i_{in} by using the previous expression of i_{in} and the definition of the RMS value of a signal

$$i_{in,RMS} = \sqrt{\frac{1}{\Delta t}\int_0^{\Delta t} i_{in}^2(t)dt}$$

$$i_{in,RMS} = I_{peak}\sqrt{\frac{2\Delta t}{3T_{grid}}} = 3.456[A] \tag{9}$$

To find I_{peak} we use the fact that $i_{Cin,avg} = 0 \rightarrow i_{1,avg} = i_{in,avg} = \frac{I_{peak}\Delta t}{T_{grid}}$ by definition of the mean value. Thus

$$I_{peak} = \frac{i_{1,avg}T_{grid}}{\Delta t} = 17.917[A]$$

To find Δt, we start from the definition of the voltage ripple

$$\Delta V = V_{max} - V_{min} = \sqrt{2}V_{grid} - \sqrt{2}V_{grid}sin(\omega_g t_1)$$

$$= \sqrt{2}V_{grid} - \sqrt{2}V_{grid}cos(\omega_g(\frac{T_{grid}}{4} - t_1))$$

$$= \sqrt{2}V_{grid} - \sqrt{2}V_{grid}cos(\omega_g \Delta t)$$

As Δt is close to 0 we can use the Hypothesis (6) and we finally get

$$\Delta t = \frac{1}{\omega_g}\sqrt{\frac{2\Delta V}{\sqrt{2}V_{grid}}} = 1.12[ms] \tag{10}$$

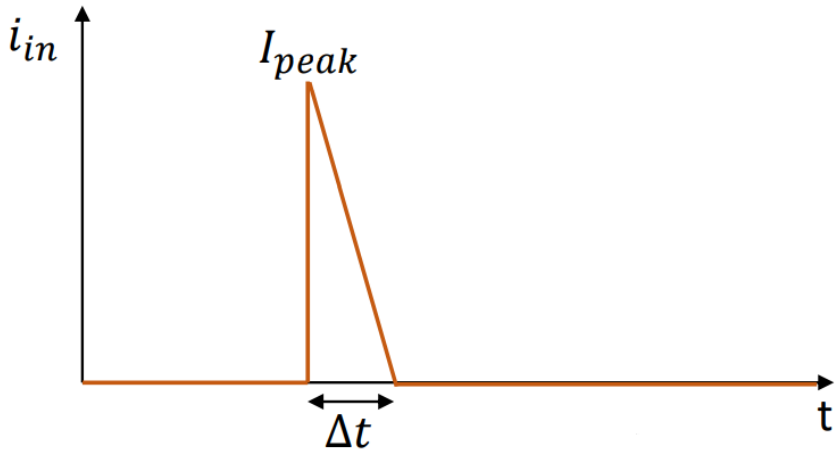

Figure 4: integration of $i_{in}(t)$

We finally find for the current $i_{Cin,RMS}$ at 100Hz that our input capacitor must support the following value :

$$i^2_{Cin,RMS} = i^2_{in,RMS} - i^2_{1,avg} = 2.456[A]$$

2.2.3 ΔV_{ESR} due to the equivalent series resistance (ESR)

By definition the ΔV_{ESR} :

$$\Delta V_{ESR} = ESR \cdot (i_{cin,max} - i_{cin,min})$$

And from equation (7), $i_{cin,max} = I_{peak} - i_{1,avg}$ and $i_{cin,min} = -i_{1,avg}$
Thus

$$\Delta V_{ESR} = ESR \cdot I_{peak}$$

2.2.4 Choice of the device based on datasheet

the criteria our device must respect are :

- Support the applied voltage
- $C > C_{in,min} = 483[\mu F]$
- Support the current $i_{Cin,RMS,max} = 2.456[A]$ at 100HZ
- ΔV due to the equivalent series resistance (ESR) is still negligible

We choosed for the implementation the electrolitycs capacitor **ALS3(1)(2)102KE350** that support à direct voltage of 350[V], has a value of 1[mF], can support a current $i_{C,RMS,max} = 6.1[A]$ at 100[Hz]. Furthermore the ripple to the equivalent series resistance (ESR) is equal to $\Delta V_{ESR} = ESR \cdot I_{peak} = 2.08[V]$ and is still negligible.

3 Output Capacitance Design

3.1 Minimum value of C_{out}

Based on the output impedance criterion : $\Delta V_o \leq 1\% V_o$.
So

$$Z_o \equiv \frac{\Delta V_o}{\Delta I_o} \leq \frac{0.02 V_o^2}{P_o}$$

We take the worst case to find $Z_{o,max} = \frac{0.02\,24^2}{300} = 0.0384[\Omega]$.
Analysing the block diagram scheme we see that Z_o corresponds to the transfer fonction

$$Z_o = \frac{V_o}{I_o} = \frac{1/(Cp)}{1 + PI(p)G_c(p)/(Cp)} \tag{11}$$

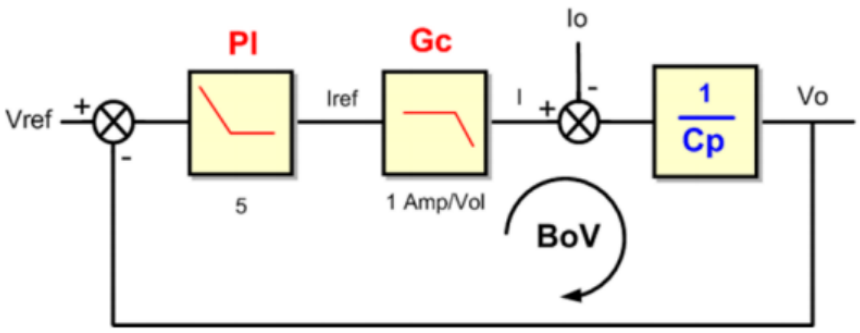

Figure 5: BoV block diagram

Furthermore as we use a PMW control to drive the gate of the transtor, we are under bandwith limitation :

$$f_c \leq \frac{f_{sh}}{\pi}$$

with f_{sh} the switching frequency and f_c the cutoff frequency. As our switching frequency is equal to $100[kHz]$, we use $f_c \leq 30[kHz]$.
The system is controled by 2 loops : 1 for the current control and the other for the voltage control. The frequency of the second one must be lower than the frequency of the first one such that we reduce the frequency in the voltage regulator loop by a factor 10. We get a frequency $f_{BoV} = 3[kHz]$.
At this frequency, we assume the transfer function (EQUATION just avant) is dominated by the term $\frac{1}{Cp}$ as $PI(p)G_c(p)/(Cp)$ is negligible compare to 1.

We finally get the expression

$$Z_o \approx \frac{1}{Cp} = \frac{1}{2\pi C} \leq 0.0384[\Omega]$$

The minimum value of C_{out} is then $1.38[mF]$

3.2 Support the current $i_{Cout,RMS}$ at 100kHz

The current through the output capacitance is given by $i_{cout} = i_2 - i_{load}$ Using the definition of RMS value :

$$i_{cout,RMS} = \sqrt{\frac{1}{T_{sw}} \int_0^{T_{sw}} i_{cout}^2(t)dt}$$

$$\iff i_{cout,RMS} = \sqrt{\frac{1}{T_{sw}} \int_0^{T_{sw}} (i_2 - i_{load})^2(t)dt}$$

$$\iff i_{Cout,RMS}^2 = i_{2,RMS}^2 + i_{load}^2 - 2i_{2,avg}i_{load}$$

Furthermore as $i_{Cout,avg} = 0 \rightarrow i_{2,avg} = i_{load}$

$$i_{Cout,RMS}^2 = i_{2,RMS}^2 - i_{load}^2 \tag{12}$$

The maximum value that $i_{2,RMS}$ can handle is 15.54[A] (see report 1). The minimal value that i_{load} can handle is 1.25 [A]. We thus get

$$i_{Cout,RMSmax} = 15.35[A]$$

3.3 ΔV_{ESR} due to the equivalent series resistance (ESR) negligible

By definition the ΔV_{ESR} :

$$\Delta V_{ESR} = ESR \cdot (i_{cout,max} - i_{cout,min})$$

And

$$i_{cout,max} = i_{2,max} - i_{load} = i_{mag,max}\frac{n_1}{n_2} - i_{load}$$

$$i_{cout,min} = i_{2,min} - i_{load} = -i_{load}$$

Thus

$$\Delta V_{ESR} = ESR \cdot i_{mag,max} \frac{n_1}{n_2}$$

We get the following values from the previous report :

- $n_1 = 135$
- $n_2 = 20$
- $i_{mag,max} = 12.85$[A]

3.4 Choice of the device based on datasheet

The criteria our device must respect are :

- Support the applied voltage
- $C > C_{out,min}$
- Support the current $i_{Cout,RMS}$ at 100[kHz]
- ΔV due to the equivalent series resistance (ESR) is still negligible

A possible choice is to use a big capacitor but it would be oversized as it only has to support 25[V].
We choosed for the implementation the capacitor to put 25 **TAJV107*025NJ** in parallel, each supporting à direct voltage of 25[V]. Each capacitor has a value of 100[μF] we thus get 2500[μF] for the total capacitor and meets our criteria,
Each capacitor can support a current $i_{C,RMS,max} = 0.782[A]$ at 100[kHz] and 85 degres. That meets our criteria because the maximum value of current to support for each capacitor is $15.35/25 = 0.614$[A]. Furthermore the ripple to the equivalent series resistance (ESR) is equal to $\Delta V_{ESR} = ESR \cdot i_{mag,max} \frac{n_1}{n_2}/25 = 1.3878[V]$ and is still negligible.

4 snubber circuit design

4.1 snubber circuit explanation

When the transistor goes off at θT there is a current going through the leakage inductance. If there was no snubber circuit, the current i_{Lf} goign through this leakage inductance would in theory goes instantly to zero meaning an infinite negative $\frac{dI_{Lf}}{dt}$ and because $V_{Lf} = L\frac{dI_{Lf}}{dt}$, this would mean an infinite (negative) value of V_Lf and as $V_{Lf} = V_{in} + \frac{n1}{n2}V_{ou} - V_t$ this lead to a infinite value of v_t. In practise it is not instantly but over a very short time with a high negative value of V_{Lf} so a quick decrease of i_{Lf} and thus provokes a dangerous high voltage on V_t which can destroy the transistor and an electric arc (a current going through a very high resistance). So the role of the snubber circuit is to limit this overvoltage to a voltage $V_{in} + V_{sn}$, V_{sn} being the voltage over the capacitance C_{sn} (we assume it is a constant voltage assuming a large capacitance), once V_t increase until $V_{in} + V_{sn}$ the diode D_{sn} is forward bias and start conducting meaning that $V_{Lf} = \frac{n1}{n2}V_{out} - V_{sn}$ and $v_t = V_{in} + V_{sn}$. Once the current $i_{Lf}(=i_{sn}$ during $t_{sn})$ reaches zero the diode stops conducting and the value of v_t is $V_{in} + \frac{n1}{n2}V_{out}$. The snubber circuit consisting of a resistance R_{sn} and one capacitor C_{sn}in paralelle. The capacitor will charge during the periode t_{sn} where the diode is open and discharge through the resistance the rest of the time.

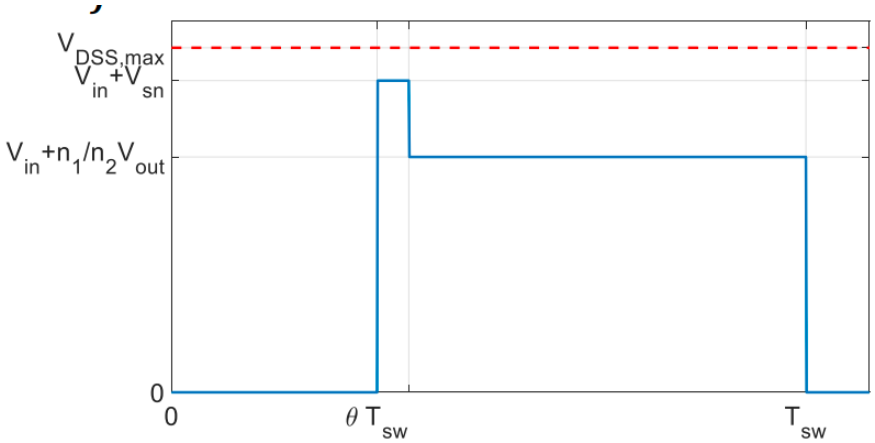

Figure 6: voltage v_t waveform

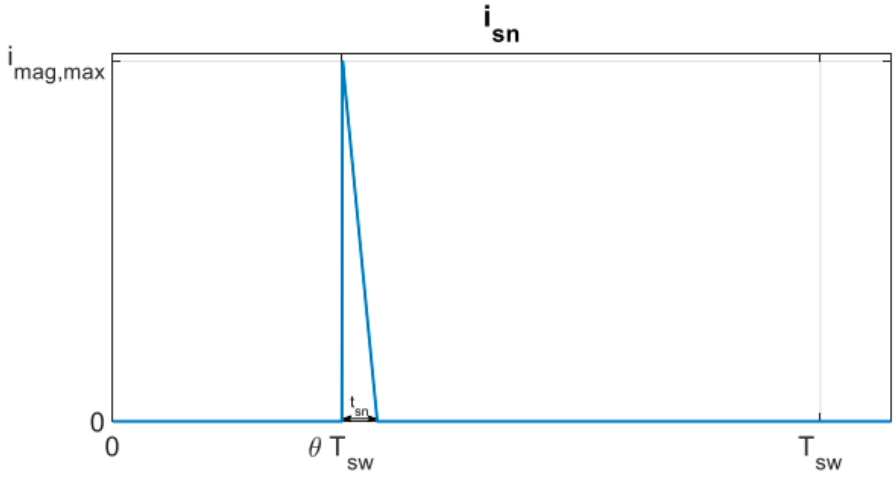

Figure 7: current i_{sn} waveform

We can calculate this time t_{sn} by considering:

$$V_{Lf} = L_f \frac{di_{Lf}}{dt} \tag{13}$$

it implies

$$\frac{di_{Lf}}{dt} = \frac{1}{L_f}(\frac{n1}{n2}V_{out} - V_{sn}) \tag{14}$$

So

$$\int_{\theta T}^{\theta T + t_{sn}} \frac{di_{Lf}(= i_{sn})}{dt} dt = \int_{\theta T}^{\theta T + t_{sn}} \frac{1}{L}(\frac{n1}{n2}V_{out} - V_{sn})dt \tag{15}$$

$$i_{Lf}(\theta T + t_{sn}) - i_{Lf}(\theta T) = 0 - i_{mag,max} = \frac{1}{L}(\frac{n1}{n2}V_{out} - V_{sn})t_{sn} \tag{16}$$

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$$t_{sn} = \frac{L_f \cdot i_{mag,max}}{V_{sn} - \frac{n1}{n2}V_{out}} \tag{17}$$

(Note: $i_{mag,max}$ is the same definition as $i_{mag,peak}$ used in rapport 1, it is the maximum peak current of i_{mag} that occur at θT.)

4.2 dissipated power computation

The power dissipated is equal to:

$$P_{sn} = \frac{V_{sn}^2}{R_{sn}} \tag{18}$$

But this power dissipated is equal to the power coming through the diode during its conduction time t_{sn}:

$$P_{sn} = \frac{1}{T_{sw}} \int_0^{T_{sw}} V_{sn} * i_{sn}(t)dt = \frac{V_{sn}}{T_{sw}} \int_{\theta T}^{\theta T + t_{sn}} i_{sn}(t) = \frac{V_{sn}}{T_{sw}} \int_{\theta T}^{\theta T + t_{sn}} (i_{mag,max} + V_{Lf} \cdot (t - \theta T))dt = V_{sn} \frac{i_{mag,max} \cdot t_{sn}}{2T_{sw}} \tag{19}$$

By equating equation (18), (19) and using (17) we obtain:

$$\frac{V_{sn}^2}{R_{sn}} = V_{sn} \frac{L_f \cdot i_{mag,max}^2}{2 \cdot T_{sw} \cdot (V_{sn} - \frac{n1}{n2}V_{out})} \tag{20}$$

Now we express V_{sn} by solving this second order equation and obtain (keeping the positive solution):

$$V_{sn} = \frac{\frac{n1}{n2}V_{out} + \sqrt{(\frac{n1}{n2}V_{out})^2 + 8T_{sw}R_{sn}L_f i_{mag,max}^2}}{4T_{sw}} \tag{21}$$

With the above expression we can observe that V_{sn} will be maximum when $i_{mag,max}$ will be maximum and we know from rapport 1 that $i_{mag,max} = i_{mag,peak} = \frac{P_{load}}{\theta \cdot V_{in}} + \frac{V_{in} \cdot \theta \cdot T}{2 \cdot L_{mag}}$ so it will be maximum at $P_{load} = P_{load,max}$.

So V_{sn} is maximum at maximum load and by knowing that $V_{sn,max} = \alpha \frac{n1}{n2} V_{out}$, we fix R_{sn} for this value of $V_{sn,max}$ and with $i_{mag,max} = i_{mag,max,Pmax}$ the value of $i_{mag,max}$ when the load is maximum, we have thus using equation (20):

$$R_{sn} = \frac{2T_{sw}\alpha(\alpha-1)(\frac{n1}{n2}V_{out})^2}{L_f i^2_{mag,max,P_{max}}} \tag{22}$$

4.3 Parameter α discussion

Now that we have an expression of R_{sn} in equaytion (22), we insert it in equation (18) and thus we have:

$$P_{sn,max} = \frac{V^2_{sn,max}}{R_{sn}} = \frac{L_f i^2_{mag,max,Pmax}}{2T_{sw}} \frac{\alpha}{\alpha-1} \tag{23}$$

By plotting the function $\frac{\alpha}{\alpha-1}$ for $\alpha \geq 1$ we can observe that it is a decreasing function but it remains almost constant for $\alpha \geq 2$ but has high values for $alpha \leq 1.5$ so we can keep $\alpha = 2$ choosen in rapport 1 to have a low P_{sn}.In our case by computing it gives $P_{sn,max} \approx 18.65$ Watts.

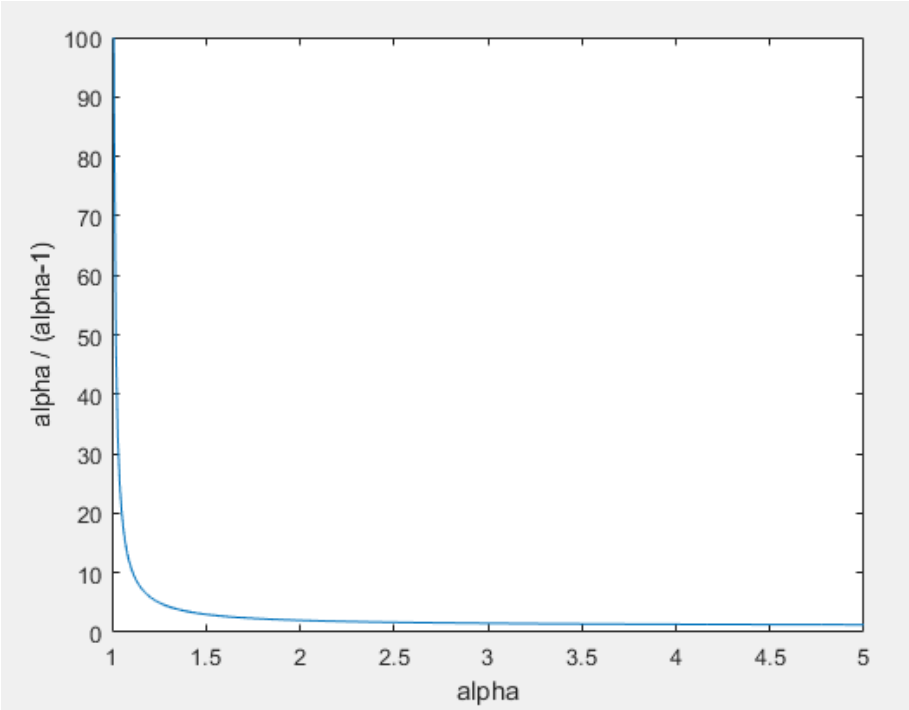

Figure 8: plot of $\frac{\alpha}{\alpha-1}$

4.4 R_{sn} and C_{sn} computation

Now using equation (22) with $i_{mag,max,Pmax} = \frac{P_{load,max}}{\theta \cdot V_{in}} + \frac{V_{in} \cdot \theta \cdot T}{2 \cdot L_{mag}}$ and $V_{Lf} = 1\% L_{mag}$, using the report 1 for thoose values, we obtain:

$$R_{sn} \approx \boxed{5.63k\Omega} \tag{24}$$

Now to compute a minimum value of C_{sn} we will express an approximate value of Δv_{sn}. In steady state V_{sn} will decrease by Δv_{sn} when the diode is not conducting (from $\theta T + t_{sn}$ to $\theta T + T_{sw}$) and increase by Δv_{sn} when the diode is conducting (from θT to $\theta T + t_{sn}$) and we have when the diode is not conducting:

$$i_{Csn}(t) = C_{sn} \frac{dv_{sn}(t)}{dt} \tag{25}$$

So

$$\int_{\theta T + t_{sn}}^{\theta T + T_{sw}} \frac{dv_{sn}(t)}{dt} dt = \frac{1}{C_{sn}} \int_{\theta T + t_{sn}}^{\theta T + T_{sw}} i_{Csn}(t) dt \tag{26}$$

And because when the diode is not conducting $i_{Csn}(t) = -i_{Rsn}(t) \approx \frac{V_{sn}}{R_{sn}}$ so we have:

$$\int_{\theta T+t_{sn}}^{\theta T+T_{sw}} \frac{dv_{sn}(t)}{dt}dt = \frac{1}{C_{sn}} \int_{\theta T+t_{sn}}^{\theta T+T_{sw}} -i_{Rsn}(t)dt \tag{27}$$

Which gives us:

$$v_{sn}(\theta T + T_{sw}) - v_{sn}(\theta T + t_{sn}) = -\Delta v_{sn} \approx -\frac{V_{sn}}{C_{sn}R_{sn}}(T_{sw} - t_{sn}) \tag{28}$$

If we furthermore approximate $T_{sw} - t_{sn} \approx T_{sw} = \frac{1}{f_{sw}}$, we obtain:

$$\Delta v_{sn} \approx \frac{V_{sn}}{C_{sn}R_{sn}f_{sw}} \tag{29}$$

<=>

$$C_{sn} \approx \frac{V_{sn}}{\Delta v_{sn}R_{sn}f_{sw}} \tag{30}$$

So to have a negligible ΔV_{sn} we choose $\Delta V_{sn} \leq 1\% \cdot V_{sn}$, and thus we obtain $C_{sn,min}$:

$$C_{sn} \geq C_{sn,min} \approx \frac{1}{1\% \cdot R_{sn}f_{sw}} \approx \boxed{177.6 \text{ nF}} \tag{31}$$