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1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

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D8 MLB ULTIMATE

LAST_MODIFIED=Mon Aug 27 13:33:38 2012

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
8	0001607319	ENGINEERING RELEASED	2012-08-28

DRAWING

TITLE=K72
ABBREV=DRAWING
LAST_MODIFIED=Mon Aug 27 13:33:38 2012

DRAWING TITLE: SCH,D8,MLB ULTIMATE

Apple Inc.

DRAWING NUMBER: 051-9505 SIZE: D
REVISION: 8.0.0
BRANCH: prefsb
PAGE: 1 OF 144
SHEET: 1 OF 123

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System Block diagram can be found on Kismet

PATH: KISMET > K70/72 > BLOCK DIAGRAMS > K72 BLOCK DIAGRAM

www.qdzbwx.com

PAGE TITLE: System Block Diagram

Apple Inc.

DRAWING NUMBER: 051-9505 SIZE: D

REVISION: 8.0.0

BRANCH: prefsb

PAGE: 2 OF 144

SHEET: 2 OF 123

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Supply Module
AC/DC
Reg G3H 12V
PP12V_ACDC
VD2R
ID2R
PD2R
PP12V_G3H
PP12V_S0_BLC
PP12V_S0
PP12V_S5

U7801
Regulator
Vin
en G3H
Reg G3H 3V42
PP3V42_G3H
SMC, RTC, MojoMux

U7600
Regulator
Vin
en S5
LDO S5 5V
Reg S5 3.3V
en S4
Reg S4 5V
PP5V_S5
PCH, PwrCtl
PP3V3_S5
Bootrom, PCH, SMC, XDP,
SD Card, USB Mux, VRD, PwrCtl
PP3V3_S4
ALS, CAM, BT
USB Hub, SMC, TBT I/O
V3V3
IW0R
PW0R
PP3V3_S4_AP
WIFI
PP3V3_S4_ENET
Ethernet
PP3V3_S0
Audio, LCD TCON, SnsCtl, VRD, PCH
SD Card, DP Mux, DP X-bar
V3V3
IW1R
PH1R
PP3V3_S0_SSD
SSD
PP3V3_TBTLC
TBT Router
PP5V_S4
CAM, USB Ports, VRegCtl
VH05
IH05
PH05
PP5V_S0_HDD
HDD (5V)
PP5V_S0
Audio, PCH
VRegCtl, SnsCtl

U7700
Regulator
Vin
en S3
Reg S3 VDDQ
LDO S3 VTT
en S0
LDO S0 VTT
VM0R
IM0R
PM0R
PPVDDQ_S3_DDR
DIMM (1V5)
PP1V5_S0
Audio
VC0M
IC0M
PC0M
PP1V5_S0_CPU_MEM
CPU (Mem)
PPDDRVTT_S3
DIMM VREF Margining CA
PPDDRVTT_S0
DIMM (VTT)

PPHV_SW_TBTAPWR
TBT Port A
PPHV_SW_TBTBPWR
TBT Port B

U7100
Regulator
Vin
en S0
Reg S0 Core
Reg S0 AXG
VC0C
IC0C
PC0C
PPVCORE_S0_CPU
CPU (Core)
VC0G
IC0G
PC0G
PPVAXG_S0
CPU (AXG)

U7400
Regulator
Vin
en S0
Reg S0 VccIO
VD2R
IC0I
PC0I
PP1V05_S0_CPU
CPU (VccIO)

U7500
Regulator
Vin
en S0
Reg S0 VccSA
VD2R
IC0S
PC0S
PPVCCSA_S0
CPU

UB400
Regulator
Vin
en S0
Reg S0 GPU
VG0C
IG0C
PG0C
PPVCORE_S0_GPU
GPU (Core)

UB750
Regulator
Vin
en S0
Reg S0 GPU
FBVDDQ
VD2R
IG0F
PG0F
PPFBVDDQ_S0_GPU
GPU (FB)

UB700
Regulator
Vin
en S0
Reg S0 1V05
VD2R
IR1R
PR1R
P1V05_S0
GPU (IOVDD, PLLVDD)
VN1R
IN1R
PN1R
P1V05_S0_PCH
PCH (VCC, VccIO)
PP1V05_TBTCIO
TBT Router
PP1V05_TBTLC
TBT Router

Loads
Fan
LCD
GPU
Speaker amps
TBT IO

VD2R
IH02
PH02
PP12V_S0_HDD
HDD (12V)

U7750
Regulator
Vin
en S0
Reg S0 1.8V
PP5V_S0
PP1V8_S0_REG
CPU PLL

High-side Component Total Power Keys

PCTR = 1.176 * (PC0C + PC0G + PC0M) + PC0S + PC0I
PGTR = 1.176 * PG0C + PG0F + 5.7 (GK104/GK107_BLENDED_CONSTANT)
PH0R = PH02 + PH05

SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012
PAGE TITLE
Power Block Diagram
Apple Inc.
DRAWING NUMBER 051-9505
SIZE D
REVISION 8.0.0
BRANCH prefsb
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SHEET 3 OF 123

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-3662	PCBA,MLB,ULTIMATE,3.4G,GTX,SAM,2GB,D8	D8_COMMON,D8,CPU:4C_3P4GHZ,GPU:104GTX,FB:2G_SAMSUNG,EEEE:F0V5
639-3950	PCBA,MLB,ULTIMATE,3.2G,GTX,SAM,2GB,D8	D8_COMMON,D8,CPU:4C_3P2GHZ,GPU:104GTX,FB:2G_SAMSUNG,EEEE:F49R
639-3560	PCBA,MLB,ULTIMATE,3.4G,GT,SAM,1GB,D8	D8_COMMON,D8,CPU:4C_3P4GHZ,GPU:104GT,FB:1G_SAMSUNG,EEEE:DYW3
639-3949	PCBA,MLB,ULTIMATE,3.2G,GT,SAM,1GB,D8	D8_COMMON,D8,CPU:4C_3P2GHZ,GPU:104GT,FB:1G_SAMSUNG,EEEE:F49P
639-4087	PCBA,MLB,ULTIMATE,3.4G,GTX,HYN,2GB,D8	D8_COMMON,D8,CPU:4C_3P4GHZ,GPU:104GTX,FB:2G_HYNIX,EEEE:F64W
639-4091	PCBA,MLB,ULTIMATE,3.2G,GTX,HYN,2GB,D8	D8_COMMON,D8,CPU:4C_3P2GHZ,GPU:104GTX,FB:2G_HYNIX,EEEE:F652
639-4086	PCBA,MLB,ULTIMATE,3.4G,GT,HYN,1GB,D8	D8_COMMON,D8,CPU:4C_3P4GHZ,GPU:104GT,FB:1G_HYNIX,EEEE:F64V
639-4090	PCBA,MLB,ULTIMATE,3.2G,GT,HYN,1GB,D8	D8_COMMON,D8,CPU:4C_3P2GHZ,GPU:104GT,FB:1G_HYNIX,EEEE:F651
085-4435	PCBA,MLB,DEV,D8.ULTIMATE	DEVELOPMENT,D8_DEVEL

Bar Code Labels / EEEE #'s

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-7896	1	LABEL,MLB,2D	EEEE_DYW3	CRITICAL	EEEE:DYW3
825-7896	1	LABEL,MLB,2D	EEEE_F0V5	CRITICAL	EEEE:F0V5
825-7896	1	LABEL,MLB,2D	EEEE_F49P	CRITICAL	EEEE:F49P
825-7896	1	LABEL,MLB,2D	EEEE_F49R	CRITICAL	EEEE:F49R
825-7896	1	LABEL,MLB,2D	EEEE_F4MW	CRITICAL	EEEE:F4MW
825-7896	1	LABEL,MLB,2D	EEEE_F4TY	CRITICAL	EEEE:F4TY
825-7896	1	LABEL,MLB,2D	EEEE_F64W	CRITICAL	EEEE:F64W
825-7896	1	LABEL,MLB,2D	EEEE_F652	CRITICAL	EEEE:F652
825-7896	1	LABEL,MLB,2D	EEEE_F64V	CRITICAL	EEEE:F64V
825-7896	1	LABEL,MLB,2D	EEEE_F651	CRITICAL	EEEE:F651

BOM Groups

BOM GROUP	BOM OPTIONS
D8_COMMON	COMMON,ALTERNATE,D8_COMMON1,D8_PROGPARTS,D8_PRODUCTION
D8_COMMON1	XDP,RSMRST:GATE,SPEAKERID,VREF:CPU,TBTHV:P12V
D8_PROGPARTS	SMC:PROG,BOOTROM:PROG,TBTROM:PROG,CIVROM:PROG,CAMROM:PROG,BLCMCU:PROG
D8_DEVEL	XDP_CONN,LPCPLUS,VREFMRGN:EXT,DEVEL_AUDIO,TEMPSNSDEV
D8_PRODUCTION	VREFMRGN:N,PRODUCTION

CPUs

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S4356	1	IVB,SR0T8,PRQ,N1,3.2,77W,4+1,1.1,6M,LGA	CPU	CRITICAL	CPU:4C_3P2GHZ
337S4247	1	IVB,SR0PK,PRQ,E1,3.4,77W,4+2,1.15,8M,LG	CPU	CRITICAL	CPU:4C_3P4GHZ

ASICs

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S4277	1	IC,PANTHER POINT,C1,SLJC7,PRQ,BDB2Z77	U1800	CRITICAL	
338S1113	1	IC,TBT,CR-4C,B1,PRQ,288 FCBGA,12X12MM	U3600	CRITICAL	
343S0616	1	IC,BCM57766A1,ENET&SD,8X8	U3900	CRITICAL	
337S4333	1	IC, GPU, NV GK104 7-4-PS-A2	UA000	CRITICAL	GPU:104GT
337S4333	1	IC, GPU, NV GK104 7-4-PS-A2	UA000	CRITICAL	GPU:104GT2
337S4332	1	IC, GPU, NV GK104 8-4-PS-A2,	UA000	CRITICAL	GPU:104GTX

Programmable Parts

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION	
341S3672	1	IC,EEPROM,CR,V14.1 (B1),D8	U3690	CRITICAL	TBTROM:PROG	
335S0865	1	IC,EEPROM,SERIAL,8KB,MLP8	U3690	CRITICAL	TBTROM:BLANK	
341S3673	1	IC,PROGRMD,EFI ROM,V00FC,D7/D8	U5110	CRITICAL	BOOTROM:PROG	ALTERNATE:335S0812
335S0807	1	IC,64 MBIT SPI SERIAL FLASH	U5110	CRITICAL	BOOTROM:BLANK	
341S3394	1	IC,PROGRMD,SMC,A3,V2.2A32,D8	U4900	CRITICAL	SMC:PROG	
338S1098	1	IC,SMC,LX4FS1AH5BBCIGA3	U4900	CRITICAL	SMC:BLANK	
341S3675	1	IC,CAMERA FLASH,V7228,D7/D8	U4202	CRITICAL	CAMROM:PROG	
335S0852	1	IC,FLASH,SPI,1MBIT,3V3	U4202	CRITICAL	CAMROM:BLANK	
341S3645	1	IC,ENET 1MBIT, SPI,ROM, V1.13 D8	U3990	CRITICAL	CIVROM:PROG	ALTERNATE:335S0854
335S0862	1	IC,SERIAL FLASH,2MBIT, 2.7V, REF F	U3990	CRITICAL	CIVROM:BLANK	
341S3674	1	IC,BLC,MCU, PRPOGRAMMED, V0204, D8	U9700	CRITICAL	BLCMCU:PROG	
337S3978	1	IC,BLC MCU LPC2132FBD64/01, LQFP64	U9700	CRITICAL	BLCMCU:BLANK	

CPU SOCKET

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
511S0073	1	SOCKET.MOLEX,LGA1155,CPU-LF	U1000	CRITICAL	

CPU SOCKET ALTERNATES

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
511S0071	511S0073		ALL	TYCO SOCKET
511S0072	511S0073		ALL	FOXCONN SOCKET

D8 SCHEMATIC / PCB #'S

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-9505	1	SCH,MLB,D8,ULTIMATE	SCH1	CRITICAL	D8
820-3299	1	PCBF,MLB,D8,ULTIMATE	PCB1	CRITICAL	D8

D8 ALTERNATES

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
377S0147	377S0126		ALL	USB diodes
157S0084	157S0058		ALL	Enet Magnetics
341S3644	341S3645		U3990	CIVROM
376S0975	376S1081		ALL	P/NCH DUAL FET
128S0365	128S0368		ALL	150UF CAPS BLK
138S0803	138S0804		ALL	2.2UF CAPS SOFT
102S0880	102S0879		ALL	0.010 OHM,1%,1206

VRAM Module Parts

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
333S0619	4	IC,SGRAM,GDDR5,32MX32,1.5GHZ,G-DIE,HF	UA300,UA350,UA400,UA450	CRITICAL	FB:1G_SAMSUNG
333S0619	4	IC,SGRAM,GDDR5,32MX32,1.5GHZ,G-DIE,HF	UA500,UA550,UA600,UA650	CRITICAL	FB:1G_SAMSUNG
333S0620	4	IC,GDDR5,32MX32,1.5GHZ,VEGA 44NM,B-DIE	UA300,UA350,UA400,UA450	CRITICAL	FB:1G_HYNIX
333S0620	4	IC,GDDR5,32MX32,1.5GHZ,VEGA 44NM,B-DIE	UA500,UA550,UA600,UA650	CRITICAL	FB:1G_HYNIX
333S0631	4	IC,SGRAM,GDDR5,64MX32,D-DIE	UA300,UA350,UA400,UA450	CRITICAL	FB:2G_SAMSUNG
333S0631	4	IC,SGRAM,GDDR5,64MX32,D-DIE	UA500,UA550,UA600,UA650	CRITICAL	FB:2G_SAMSUNG
333S0630	4	IC,GDDR5,64MX32,A-DIE	UA300,UA350,UA400,UA450	CRITICAL	FB:2G_HYNIX
333S0630	4	IC,GDDR5,64MX32,A-DIE	UA500,UA550,UA600,UA650	CRITICAL	FB:2G_HYNIX

SYNC_MASTER=D8_MLB_ULTIMATE SYNC_DATE=06/15/2012

PAGE TITLE: BOM Configuration

Apple Inc.

DRAWING NUMBER: 051-9505 SIZE: D

REVISION: 8.0.0

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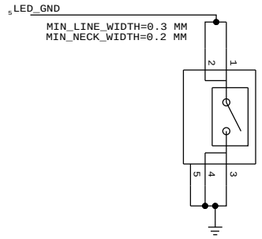
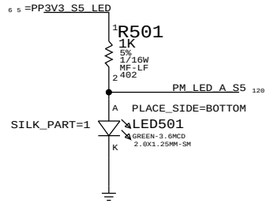
LED GND ISOLATION SWITCH

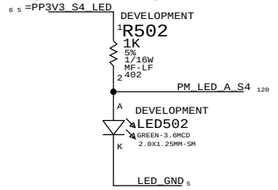


APN: 705S0137

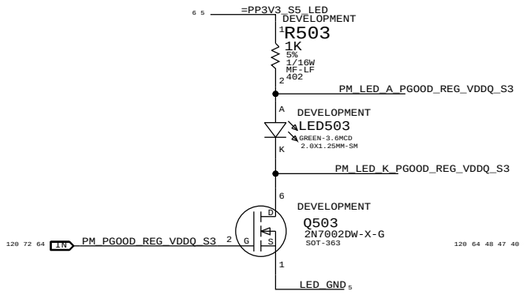
S5 LED



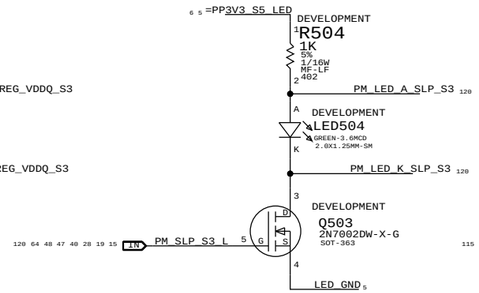
S4 (SLEEP) LED



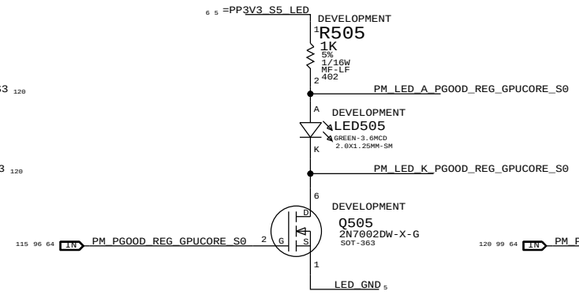
MEM 1V5_S3 LED



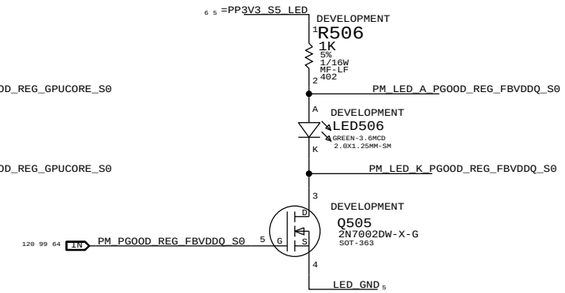
SLP_S3 LED



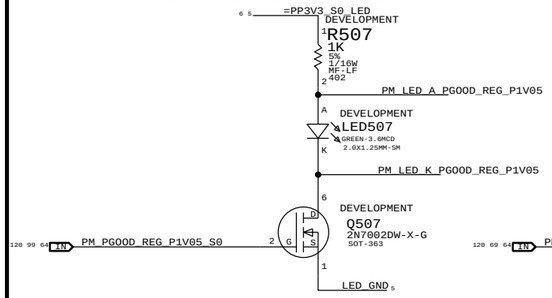
GPU VCORE LED



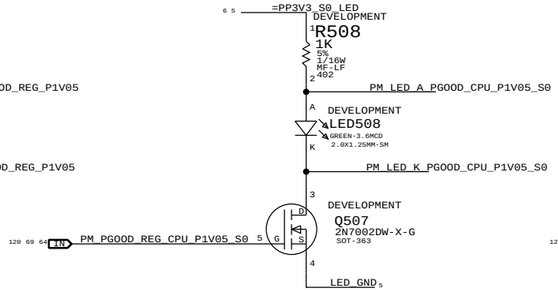
GPU FBVDD LED



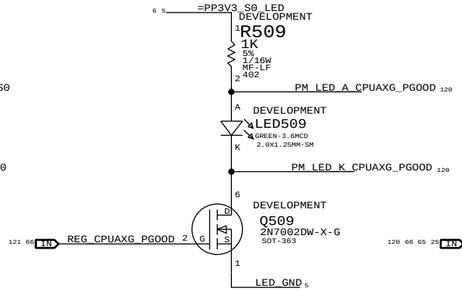
PCH/GPU 1V05 LED



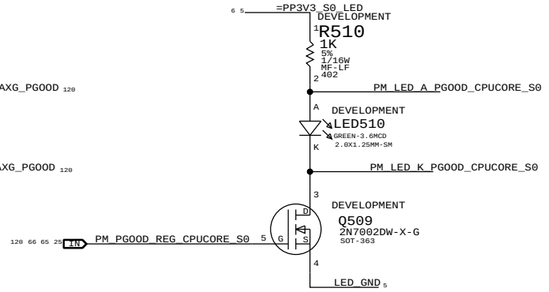
CPU 1V05_S0 LED



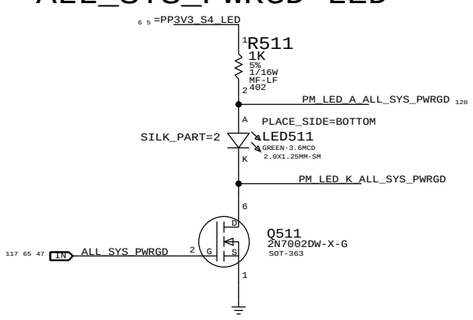
CPU AXG LED



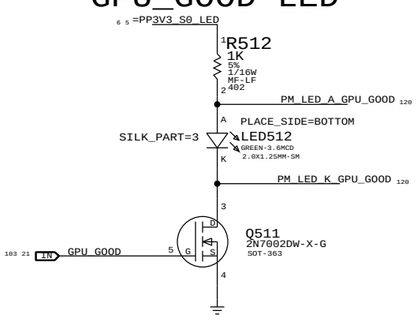
CPU VCORE LED



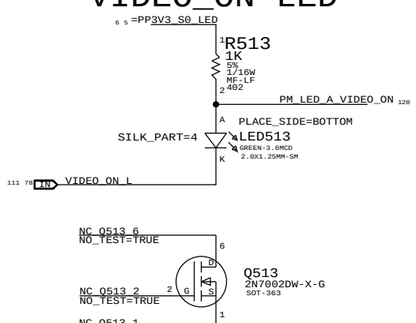
ALL_SYS_PWRGD LED



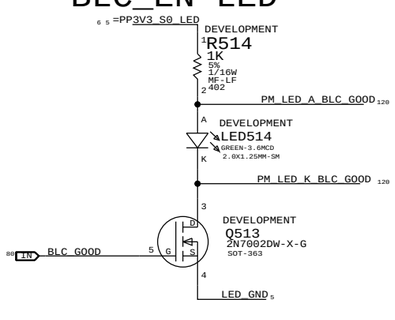
GPU_GOOD LED



VIDEO_ON LED



BLC_EN LED



SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012

PAGE TITLE: DEBUG LEDS

Apple Inc.

DRAWING NUMBER: 051-9505 SIZE: D
REVISION: 8.0.0
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MLB to AC-DC Supplemental Signal Connector

SILK_PART=PWRSIG
J601
504050-0791
M-RT-SM
518S0863

PWR_BTN
PWR_BTN_R
SMC_ACDC_ID_R
TSNS_ACDC_N
TSNS_ACDC_P
BURSTMODE_EN_R_L
BURSTMODE_EN_L
SMC_ACDC_ID

C600 0.1UF 10% 16V X7R-CERM 0402
C605 0.1UF 10% 16V X7R-CERM 0402
C604 0.01UF 20% 16V X7R-CERM 0402
R606 1K 5% 1/16W MF-LF 402
R600 1K 5% 1/16W MF-LF 402
R603 10K 5% 1/16W MF-LF 402
R604 1K 5% 1/16W MF-LF 402
D600 6.8V-100PF 402
D602 6.8V-100PF 402
D601 6.8V-100PF 402

FILTER ADDED TO BURSTMODE_EN_L TO PASS SURGE RDAR://11059712

MLB to AC-DC Connector

CRITICAL
J600
43045-1201
M-RT-TH-1
518-0389

PP12V_G3H_ACDC

C601 10UF 10% 25V XSR 805 — J600.4:10MM
C602 1000PF 5% 25V NP0-C0G 402 — EMC J600.5:10MM
C603 1000PF 5% 25V NP0-C0G 402 — EMC J600.5:10MM

G3 Rails

Always on: Keeps the PCH RTC alive

PP3V3_G3 (MAKE_BASE=TRUE)
- =PP3V3_G3_RTC — 26 121
- =PP3V3_G3_PCH_RTC — 22
- =PP3V3_G3_PCH — 18 19

G3H Rails

On with AC/DC plugged in

PP12V_ACDC (MAKE_BASE=TRUE)
- =PP12V_G3H_ACDC — 6
- =PP12V_G3H_PWR — 51

PP12V_G3H (MAKE_BASE=TRUE)
- =PP12V_G3H_SNS — 51
- =PP12V_G3H_P3V42 — 73
- =PP12V_G3H_FET_P12V_S0 — 74
- =PP12V_G3H_FET_P12V_S5 — 74

PP3V42_G3H (MAKE_BASE=TRUE)
- =PP3V3_G3H_BT — 35
- =PP3V3_G3H_RTC_D — 26
- =PP3V3_G3H_SMC — 47 48 50
- =PP3V3_G3H_SMC_USBMUX — 45
- =PPVIN_G3H_SMCVREF — 48
- =PP3V3_G3H_LPCPLUS — 49

S5 Rails

On when in S5

PP12V_S5 (MAKE_BASE=TRUE)
- =PP12V_S5_FET — 74
- =PP12V_S5_REG_P3V3P5V_S5 — 71
- =PP12V_S5_REG_VDDQ_S3 — 72
- =PP12V_S5_PWRCTL — 64 65 74
- =PPHV_SW_TBTAPWRSW — 77
- =PPHV_SW_TBTBPWRSW — 79
- =PP12V_S5_SNS — 51

PP5V_S5 (MAKE_BASE=TRUE)
- =PP5V_S5_LDO — 71
- =PP5V_S5_PWRCTL — 71
- =PP5V_S5_PCH — 24

PP3V3_S5 (MAKE_BASE=TRUE)
- =PP3V3_S5_REG — 71
- =PP3V3_S5_FET_P3V3_S0 — 74
- =PP3V3_S5_FET_P3V3_S4 — 74
- =PP3V3_S5_SMC — 48
- =PP3V3_S5_LED — 5
- =PP3V3_S5_PCH — 19 24 26
- =PP3V3_S5_PCH_STRAPS — 15
- =PP3V3_S5_PCH_VCCSUS_HDA — 22 24
- =PP3V3_S5_PCH_VCCSUS_USB — 22 24
- =PP3V3_S5_PCH_VCC_DSW — 22 24
- =PP3V3_S5_PCH_VCC_SPI — 22 24
- =PP3V3_S5_PWRCTL — 64 65
- =PP3V3_S5_ROM — 49
- =PP3V3_S5_VRD — 71
- =PP3V3_S5_XDP — 25
- =PP3V3_S5_SMC_USBMUX — 45 46
- =PP3V3_S5_SENSE — 51
- =PP3V3_S5_SDCARD — 41

S4 Rails

Enabled when system has AC and is in run or sleep

PP5V_S4 (MAKE_BASE=TRUE)
- =PP5V_S4_REG — 71
- =PP5V_S4_REG_VDDQ_S3 — 72
- =PP5V_S4_FET_P5V_S0 — 74
- =PP5V_S4_MEMRESET — 28
- =PP5V_S4_USB — 45 46
- =PP5V_S4_CAMERA — 42

PP3V3_S4 (MAKE_BASE=TRUE)
- =PP3V3_S4_FET — 74
- =PP3V3_S4_ALS — 42
- =PP3V3_S4_AP_PWR — 55
- =PP3V3_S4_CAMERA — 42 43
- =PP3V3_S4_ENET — 40
- =PP3V3_S4_LED — 5
- =PP3V3_S4_MEMRESET — 28
- =PP3V3_S4_PM — 28
- =PP3V3_S4_PWRCTL — 65 72 74
- =PP3V3_S4_SENSE — 51
- =PP3V3_S4_SMBUS — 50
- =PP3V3_S4_SMBUS_SMC — 50
- =PP3V3_S4_SMC — 48
- =PP3V3_S4_TBT — 36 37 38 77 79
- =PP3V3_S4_TBTAPWRSW — 48 77
- =PP3V3_S4_TBTBPWRSW — 48 79
- =PP3V3_S4_USB_HUB — 27
- =PP3V3_S4_VREFMRGN — 34
- =PP3V3_S4_AUDIO_DIG — 60

PP3V3_S4_AP (MAKE_BASE=TRUE)
- =PP3V3_S4_AP_SNS — 55
- =PP3V3_S4_AP — 15 35

PP3V3_S4_ENET (MAKE_BASE=TRUE)
- =PP3V3_S4_ENET_FET — 40
- =PP3V3_S4_ENET_SYSCLK — 26
- =PP3V3_S4_ENET_CLK — 26

S3 Rails

Enabled when system is in run or sleep

PPVDDQ_S3 (MAKE_BASE=TRUE) — THIS IS 1.5V RAIL
- =PPVDDQ_S3_REG — 72
- =PPVDDQ_S3_DDR_PWR — 51
- =PPVDDQ_S3_FET_VDDQ_S0 — 74
- =PPVDDQ_S3_LDO_DDRVTT — 72

PPVDDQ_S3_DDR (MAKE_BASE=TRUE) — THIS IS 1.5V RAIL
- =PPVDDQ_S3_DDR_SNS — 51
- =PPVDDQ_S3_DDR_VREF — 34
- =PPVDDQ_S3_MEM_A — 29 30
- =PPVDDQ_S3_MEM_B — 31 32
- =PPVDDQ_S3_MEMRESET — 28

PPDDRVTT_S3 (MAKE_BASE=TRUE) — THIS IS 1.5V RAIL
- =PPDDRVTT_S3_LDO — 72
- =PPDDRVTT_S3_VREFCA — 34

S0 Rails

Enabled when system is in run

PP12V_S0 (MAKE_BASE=TRUE)
- =PP12V_S0_FET — 74
- =PP12V_S0_AUDIO_SPKRAMP — 58 59
- =PP12V_S0_FAN — 54
- =PP12V_S0_FBVDDQ_PWR — 51
- =PP12V_S0_REG_GPUCORE — 96
- =PP12V_S0_HDD_PWR — 51
- =PP12V_S0_LCD — 78
- =PP12V_S0_REG_CPUCORE — 67
- =PP12V_S0_REG_CPU_P1V05_PWR — 55
- =PP12V_S0_REG_CPU_VCCSA_PWR — 55
- =PP12V_S0_REG_P1V05_PWR — 55
- =PP12V_S0_PWRCTL — 65

PP12V_S0_HDD (MAKE_BASE=TRUE)
- =PP12V_S0_HDD_SNS — 51
- =PP12V_S0_HDD — 52

PP12V_S0_BLC (MAKE_BASE=TRUE)
- =PP12V_S0_BLC_FET — 74
- =PP12V_S0_BLC — 82

PP12V_S0_FBVDDQ (MAKE_BASE=TRUE)
- =PP12V_S0_FBVDDQ_SNS — 51
- =PP12V_S0_REG_FBVDDQ — 99

PP12V_S0_CPU_P1V05 (MAKE_BASE=TRUE)
- =PP12V_S0_REG_CPU_P1V05_SNS — 55
- =PP12V_S0_REG_CPU_P1V05 — 69

PP12V_S0_VCCSA (MAKE_BASE=TRUE)
- =PP12V_S0_REG_CPU_VCCSA_SNS — 55
- =PP12V_S0_REG_VCCSA — 70

PP12V_S0_P1V05 (MAKE_BASE=TRUE)
- =PP12V_S0_REG_P1V05_SNS — 55
- =PP12V_S0_REG_P1V05 — 99

PP5V_S0 (MAKE_BASE=TRUE)
- =PP5V_S0_FET — 74
- =PP5V_S0_AUDIO — 56 63
- =PP5V_S0_BLC — 82
- =PP5V_S0_HDD_PWR — 51
- =PP5V_S0_ISENSE — 51
- =PP5V_S0_LPCPLUS — 49
- =PP5V_S0_PCH — 24
- =PP5V_S0_REG_CPUCORE — 66
- =PP5V_S0_REG_CPU_P1V05 — 69
- =PP5V_S0_REG_FBVDDQ — 99
- =PP5V_S0_REG_P1V05 — 99
- =PP5V_S0_REG_P1V8 — 72
- =PP5V_S0_REG_VCCSA — 70
- =PP5V_S0_VRD — 72 96

PP5V_S0_HDD (MAKE_BASE=TRUE)
- =PP5V_S0_HDD_SNS — 51
- =PP5V_S0_HDD — 52

PP3V3_S0 (MAKE_BASE=TRUE)
- =PP3V3_S0_FET — 74
- =PP3V3_S0_GPU_IFPX_PLLVDD — 90
- =PP3V3_S0_GPU_MISC — 92
- =PP3V3_S0_GPU_VDD33 — 91
- =PP3V3_S0_AUDIO — 42 56 58 59 62
- =PP3V3_S0_AUDIO_DIG — 60
- =PP3V3_S0_BLC — 80
- =PP3V3_S0_DP — 76 78
- =PP3V3_S0_ENET — 39
- =PP3V3_S0_FAN — 54
- =PP3V3_S0_GPU — 83 91 92 95 96
- =PP3V3_S0_INTDPMUX — 75
- =PP3V3_S0_LED — 5
- =PP3V3_S0_LED_SATA — 15 44
- =PP3V3_S0_MEM_A_SPD — 29 30
- =PP3V3_S0_MEM_B_SPD — 31 32
- =PP3V3_S0_P3V3TBTFET — 38
- =PP3V3_S0_PCH — 18 21 24
- =PP3V3_S0_PCH_GPIO — 15 19 20 38
- =PP3V3_S0_PCH_PM — 26
- =PP3V3_S0_PCH_STRAPS — 15
- =PP3V3_S0_PCH_VCC — 22 24
- =PP3V3_S0_PCH_VCC_ADAC — 17
- =PP3V3_S0_PCH_VCC_GPIO — 22 24
- =PP3V3_S0_PCH_VCC_HVCMOS — 22 24
- =PP3V3_S0_PCH_VCC_PCI — 22 24
- =PP3V3_S0_PWRCTL — 28 74
- =PP3V3_S0_RSTBUF — 26
- =PP3V3_S0_SDCARD — 41
- =PP3V3_S0_SENSE — 51 52 53 55
- =PP3V3_S0_SMBUS — 50
- =PP3V3_S0_SMBUS_SMC — 50
- =PP3V3_S0_SMBUS_TCON — 50
- =PP3V3_S0_SMC — 48 51 91
- =PP3V3_S0_TBTPWRCTL — 38
- =PP3V3_S0_VRD — 6 66 69 70 72 96 99
- =PP3V3_S0_SSD_PWR — 51

PP3V3_S0_SSD (MAKE_BASE=TRUE)
- =PP3V3_S0_SSD_SNS — 51
- =PP3V3_S0_SSD — 44

PP1V8_S0 (MAKE_BASE=TRUE)
- =PP1V8_S0_REG — 72
- =PP1V8_S0_CPU_PLL — 13 16
- =PP1V8_S0_PCH — 19
- =PP1V8_S0_PCH_VCC_DFTERM — 22 24
- =PP1V8_S0_PCH_VCC_VRM — 24
- =PP1V8_S0_PCH_CLK — 26

PP1V5_S0 (MAKE_BASE=TRUE)
- =PP1V5_S0_FET — 74
- =PP1V5_S0_AUD_DIG — 56
- =PP1V5_S0_CPU_MEM_PWR — 51
- =PP1V5_S0_DP — 75

PP1V5_S0_CPU_MEM (MAKE_BASE=TRUE)
- =PP1V5_S0_CPU_MEM_SNS — 51
- =PP1V5_S0_CPU_MEM — 11 13 16

PPDDRVTT_S0 (MAKE_BASE=TRUE)
- =PPDDRVTT_S0_LDO — 72
- =PPDDRVTT_S0_CLAMP — 28
- =PPDDRVTT_S0_MEM_A — 29 30
- =PPDDRVTT_S0_MEM_B — 31 32

PPDDRVREF_DQ_MEM_A_S3 (MAKE_BASE=TRUE)
- =PPDDRVREF_DQ_MEM_A — 34
- =PPDDRVREF_DQ_MEM_A — 29 30

PPDDRVREF_CA_MEM_A_S3 (MAKE_BASE=TRUE)
- =PPDDRVREF_CA_MEM_A — 34
- =PPDDRVREF_CA_MEM_A — 29 30

PPDDRVREF_DQ_MEM_B_S3 (MAKE_BASE=TRUE)
- =PPDDRVREF_DQ_MEM_B — 34
- =PPDDRVREF_DQ_MEM_B — 31 32

PPDDRVREF_CA_MEM_B_S3 (MAKE_BASE=TRUE)
- =PPDDRVREF_CA_MEM_B — 34
- =PPDDRVREF_CA_MEM_B — 31 32

PP1V05_S0_CPU (MAKE_BASE=TRUE)
- =PP1V05_S0_CPU_REG — 69
- =PPVCCIO_S0_CPU — 10 11 13 16 28 66
- =PPVCCIO_S0_SMC — 48
- =PPVCCIO_S0_XDP — 25

PP1V05_S0 (MAKE_BASE=TRUE)
- =PP1V05_S0_REG — 99
- =PP1V05_S0_PCH_PWR — 51
- =PP1V05_S0_P1V05TBTFET — 38
- =PP1V05_S0_GPU_IFPCD_IOVDD — 90
- =PP1V05_S0_GPU_IFPEF_IOVDD — 90
- =PP1V05_S0_GPU_PEX_PLLVDD — 83 95
- =PP1V05_S0_GPU_PEX_IOVDD — 83

PPVCORE_S0_CPU (MAKE_BASE=TRUE)
- =PPCPUCORE_S0_REG — 67 68
- =PPVCORE_S0_CPU — 13 16 51 66

PPVAXG_S0 (MAKE_BASE=TRUE)
- =PPCPUAXG_S0_REG — 17 68
- =PPVAXG_S0_CPU — 13 17 51 66

PPVCCSA_S0 (MAKE_BASE=TRUE)
- =PPVCCSA_S0_REG — 70
- =PPVCCSA_S0_CPU — 13 16

Thunderbolt Rails (S0)

Enabled when Thunderbolt cable is plugged in

PP3V3_TBTLC (MAKE_BASE=TRUE)
- =PP3V3_TBTLC_FET — 38
- =PP3V3_TBT_PCH_GPIO — 15
- =PP3V3_TBTLC_RTR — 15 36 37 38 50
- =PP3V3_TBT_CLK — 26

PP1V05_TBTLC (MAKE_BASE=TRUE) — 100 38
- =PP1V05_TBTLC_FET — 38
- =PP1V05_TBTLC_RTR — 37

PP1V05_TBTCIO (MAKE_BASE=TRUE)
- =PP1V05_TBTCIO_FET — 38
- =PP1V05_TBTCIO_RTR — 37

Ground/Common

GND (MAKE_BASE=TRUE)

GPU Rails (S0)

Enabled when system is in run

PPVCORE_S0_GPU (MAKE_BASE=TRUE)
- =PPVCORE_S0_GPU — 51 93

PPFBVDDQ_S0_GPU (MAKE_BASE=TRUE)
- =PP1V5R1V35_S0_GPU_REG — 99 115
- =PP1V35_S0_GPU_FBVDDQ — 84 85 86 87 88 89

PP1V05_S0_PCH (MAKE_BASE=TRUE) — 100
- =PP1V05_S0_PCH_SNS — 51
- =PP1V05_S0_PCH — 18
- =PP1V05_S0_PCH_VCCCLKDMI — 22 24
- =PP1V05_S0_PCH_VCCIO_DMI — 22 24
- =PP1V05_S0_PCH_VCCIO_PCIE — 18 19 22 24
- =PP1V05_S0_PCH_VCCIO_SATA — 18 22 24
- =PP1V05_S0_PCH_VCCIO_USB — 22 24
- =PP1V05_S0_PCH_VCC_ADPLL — 17
- =PP1V05_S0_PCH_VCC_ASW — 22 24
- =PP1V05_S0_PCH_VCC_CORE — 22 24
- =PP1V05_S0_PCH_VCC_DIFFCLK — 22 24
- =PP1V05_S0_PCH_VCC_DMI — 22 24
- =PP1V05_S0_PCH_VCC_SSC — 22 24
- =PP1V05_S0_PCH_V_PROC_IO — 22 24

SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012

PAGE TITLE: Power Connectors/Aliases

Apple Inc.

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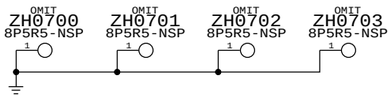
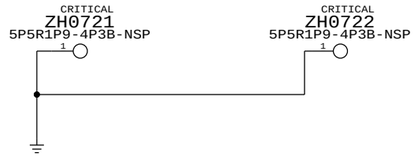
CPU Heatsink

4MM PLATED HOLES (998-4158)



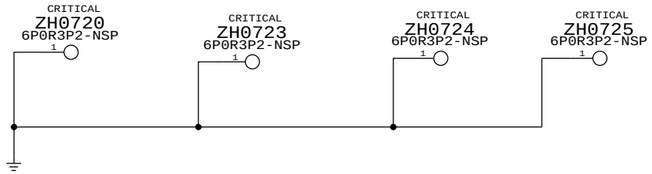
WIRELESS CARD MTG HOLES

998-4938 (PLATED HOLES, 1.9MM INNER DIAMETER, 4.3MM PAD)



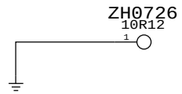
GPU HEATSINK MOUNTING FEATURES

(998-5013. PLATED HOLE, 3.2MM DIA, 6MM PAD TOP/BOT)



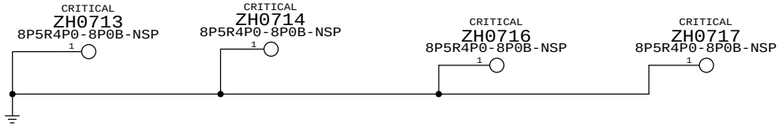
HEATPIPE MTG HOLES

998-4640 (PLATED HOLES, 10MM DIA, 12MM PAD)



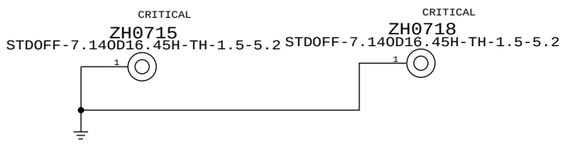
Rear Cover

998-5014 (PLATED HOLES, 4MM DRILL, 8.5MM TOP, 8MM BOT)



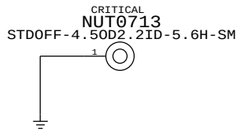
Rear Cover

860-1487 (PCB STANDOFF)



SSD STANDOFF

APN: 860-1461



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PAGE TITLE: Holes/PD parts

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CPU Reserved

10	TP_CPU_RSVD<16..1>	NC_CPU_RSVD<16..1>	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_CPU_RSVD<46..19>	NC_CPU_RSVD<46..19>	MAKE_BASE=TRUE NO_TEST=TRUE
10	CPU_CFG<15..12>	TP_CPU_CFG<15..12>	MAKE_BASE=TRUE

CPU Memory

12	TP_MEM_A_DQ_CB<7..0>	NC_MEM_A_DQ_CB<7..0>	MAKE_BASE=TRUE NO_TEST=TRUE
12	TP_MEM_A_DQS_N<8>	NC_MEM_A_DQSNX<8>	MAKE_BASE=TRUE NO_TEST=TRUE
12	TP_MEM_A_DQS_P<8>	NC_MEM_A_DQSPX<8>	MAKE_BASE=TRUE NO_TEST=TRUE
12	TP_MEM_B_DQ_CB<7..0>	NC_MEM_B_DQ_CB<7..0>	MAKE_BASE=TRUE NO_TEST=TRUE
12	TP_MEM_B_DQS_N<8>	NC_MEM_B_DQSNX<8>	MAKE_BASE=TRUE NO_TEST=TRUE
12	TP_MEM_B_DQS_P<8>	NC_MEM_B_DQSPX<8>	MAKE_BASE=TRUE NO_TEST=TRUE

PCH PCIe

18	TP_PCIE1_D2RN	NC_PCIE1_D2RNX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCIE1_D2RP	NC_PCIE1_D2RPX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCIE1_R2D_CN	NC_PCIE1_R2D_CNX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCIE1_R2D_CP	NC_PCIE1_R2D_CPX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCIE2_D2RN	NC_PCIE2_D2RNX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCIE2_D2RP	NC_PCIE2_D2RPX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCIE2_R2D_CN	NC_PCIE2_R2D_CNX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCIE2_R2D_CP	NC_PCIE2_R2D_PNX	MAKE_BASE=TRUE NO_TEST=TRUE
18	DMI_MIDBUS_CLK100M_N	NC_DMI_MIDBUS_CLK100NX	MAKE_BASE=TRUE NO_TEST=TRUE
18	DMI_MIDBUS_CLK100M_P	NC_DMI_MIDBUS_CLK100PX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCIE_CLK100M_PE0N	NC_PCIE_CLK100M_PE0NX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCIE_CLK100M_PE0P	NC_PCIE_CLK100M_PE0PX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCIE_CLK100M_PE4N	NC_PCIE_CLK100M_PE4NX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCIE_CLK100M_PE4P	NC_PCIE_CLK100M_PE4PX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCIE_CLK100M_PE5N	NC_PCIE_CLK100M_PE5NX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCIE_CLK100M_PE5P	NC_PCIE_CLK100M_PE5PX	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCIE_CLK100M_PE6N	NC_PCIE_CLK100M_PE6NX	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCIE_CLK100M_PE6P	NC_PCIE_CLK100M_PE6PX	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCIE_CLK100M_PE7N	NC_PCIE_CLK100M_PE7NX	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCIE_CLK100M_PE7P	NC_PCIE_CLK100M_PE7PX	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_PE_TX_N<3..0>	NC_PE_TNX<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_PE_TX_P<3..0>	NC_PE_TPX<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_PE_RX_N<3..0>	NC_PE_RNX<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_PE_RX_P<3..0>	NC_PE_RPX<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE

PCH USB

20	USB_PCH_4_N	NC_USB_PCH_4NX	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_PCH_4_P	NC_USB_PCH_4PX	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_PCH_5_N	NC_USB_PCH_5NX	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_PCH_5_P	NC_USB_PCH_5PX	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_PCH_6_N	NC_USB_PCH_6NX	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_PCH_6_P	NC_USB_PCH_6PX	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_PCH_11_N	NC_USB_PCH_11NX	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_PCH_11_P	NC_USB_PCH_11PX	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_PCH_12_N	NC_USB_PCH_12NX	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_PCH_12_P	NC_USB_PCH_12PX	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_PCH_13_N	NC_USB_PCH_13NX	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_PCH_13_P	NC_USB_PCH_13PX	MAKE_BASE=TRUE NO_TEST=TRUE

PCH Clocks

18	TP_PCH_CLKOUT_DPN	NC_PCH_CLKOUT_DPNX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_CLKOUT_DPP	NC_PCH_CLKOUT_DPPX	MAKE_BASE=TRUE NO_TEST=TRUE
18	PCH_CLK25M_XTALOUT	NC_PCH_CLK25M_XTALOUT	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_GPIO64_CLKOUTFLEX0	NC_PCH_GPIO64_CLKOUTFLEX0	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_GPIO65_CLKOUTFLEX1	NC_PCH_GPIO65_CLKOUTFLEX1	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_GPIO66_CLKOUTFLEX2	NC_PCH_GPIO66_CLKOUTFLEX2	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_GPIO67_CLKOUTFLEX3	NC_PCH_GPIO67_CLKOUTFLEX3	MAKE_BASE=TRUE NO_TEST=TRUE

PCH Unused Display

19	TP_CRT_IG_RED	NC_CRT_IG_RED	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_CRT_IG_GREEN	NC_CRT_IG_GREEN	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_CRT_IG_BLUE	NC_CRT_IG_BLUE	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_CRT_IG_HSYNC	NC_CRT_IG_HSYNC	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_CRT_IG_VSYNC	NC_CRT_IG_VSYNC	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_CRT_IG_DDC_CLK	NC_CRT_IG_DDC_CLK	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_CRT_IG_DDC_DATA	NC_CRT_IG_DDC_DATA	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_B_MLN<3..0>	NC_DP_IG_B_MLNX<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_B_MLP<3..0>	NC_DP_IG_B_MLPX<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_B_AUX_N	NC_DP_IG_B_AUXNX	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_B_AUX_P	NC_DP_IG_B_AUXPX	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_B_HPD	NC_DP_IG_B_HPD	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_B_DDC_CLK	NC_DP_IG_B_CTRL_CLK	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_B_DDC_DATA	NC_DP_IG_B_CTRL_DATA	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_C_MLN<3..0>	NC_DP_IG_C_MLNX<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_C_MLP<3..0>	NC_DP_IG_C_MLPX<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_C_AUX_N	NC_DP_IG_C_AUXNX	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_C_AUX_P	NC_DP_IG_C_AUXPX	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_C_HPD	NC_DP_IG_C_HPD	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_C_CTRL_CLK	NC_DP_IG_C_CTRL_CLK	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_C_CTRL_DATA	NC_DP_IG_C_CTRL_DATA	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_D_MLN<3..0>	NC_DP_IG_D_MLNX<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_D_MLP<3..0>	NC_DP_IG_D_MLPX<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_D_AUXN	NC_DP_IG_D_AUXNX	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_D_AUXP	NC_DP_IG_D_AUXPX	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_D_HPD	NC_DP_IG_D_HPD	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_D_CTRL_CLK	NC_DP_IG_D_CTRL_CLK	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_D_CTRL_DATA	NC_DP_IG_D_CTRL_DATA	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_SDVO_TVCLKINN	NC_SDVO_TVCLKINNX	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_SDVO_TVCLKINP	NC_SDVO_TVCLKINPX	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_SDVO_STALLN	NC_SDVO_STALLNX	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_SDVO_STALLP	NC_SDVO_STALLPX	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_SDVO_INTN	NC_SDVO_INTNX	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_SDVO_INTP	NC_SDVO_INTPX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_L_BKLTCTL	NC_PCH_L_BKLTCTL	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_L_BKLTEN	NC_PCH_L_BKLTEN	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_L_VDD_EN	NC_PCH_L_VDD_EN	MAKE_BASE=TRUE NO_TEST=TRUE

PCH SATA

18	TP_SATA_C_R2D_CN	NC_SATA_C_R2D_CNX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_C_R2D_CP	NC_SATA_C_R2D_CPX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_C_D2RN	NC_SATA_C_D2RNX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_C_D2RP	NC_SATA_C_D2RPX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_D_R2D_CN	NC_SATA_D_R2D_CNX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_D_R2D_CP	NC_SATA_D_R2D_CPX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_D_D2RN	NC_SATA_D_D2RNX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_D_D2RP	NC_SATA_D_D2RPX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_E_R2D_CN	NC_SATA_E_R2D_CNX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_E_R2D_CP	NC_SATA_E_R2D_CPX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_E_D2RN	NC_SATA_E_D2RNX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_E_D2RP	NC_SATA_E_D2RPX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_F_R2D_CN	NC_SATA_F_R2D_CNX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_F_R2D_CP	NC_SATA_F_R2D_CPX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_F_D2RN	NC_SATA_F_D2RNX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_F_D2RP	NC_SATA_F_D2RPX	MAKE_BASE=TRUE NO_TEST=TRUE

PCH Reserved

19	TP_PCH_RESERVE_0	NC_PCH_RESERVE_0	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_1	NC_PCH_RESERVE_1	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_2	NC_PCH_RESERVE_2	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_3	NC_PCH_RESERVE_3	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_4	NC_PCH_RESERVE_4	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_5	NC_PCH_RESERVE_5	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_6	NC_PCH_RESERVE_6	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_7	NC_PCH_RESERVE_7	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_8	NC_PCH_RESERVE_8	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_9	NC_PCH_RESERVE_9	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_10	NC_PCH_RESERVE_10	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_11	NC_PCH_RESERVE_11	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_12	NC_PCH_RESERVE_12	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_13	NC_PCH_RESERVE_13	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_14	NC_PCH_RESERVE_14	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_15	NC_PCH_RESERVE_15	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_16	NC_PCH_RESERVE_16	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_17	NC_PCH_RESERVE_17	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_18	NC_PCH_RESERVE_18	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_19	NC_PCH_RESERVE_19	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_20	NC_PCH_RESERVE_20	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_21	NC_PCH_RESERVE_21	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_22	NC_PCH_RESERVE_22	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_23	NC_PCH_RESERVE_23	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_24	NC_PCH_RESERVE_24	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_25	NC_PCH_RESERVE_25	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_26	NC_PCH_RESERVE_26	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_27	NC_PCH_RESERVE_27	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_28	NC_PCH_RESERVE_28	MAKE_BASE=TRUE NO_TEST=TRUE

PCH and CPU FDI

10	TP_CPU_FDI_TX_N<7..0>	NC_CPU_FDI_TNX<7..0>	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_CPU_FDI_TX_P<7..0>	NC_CPU_FDI_TPX<7..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	PCH_FDI_RX_N<7..0>	NC_PCH_FDI_RNX<7..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	PCH_FDI_RX_P<7..0>	NC_PCH_FDI_RPX<7..0>	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_CPU_FDI_FSYNC<1..0>	NC_CPU_FDI_FSYNC<1..0>	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_CPU_FDI_LSYNC<1..0>	NC_CPU_FDI_LSYNC<1..0>	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_CPU_FDI_INT	NC_CPU_FDI_INT	MAKE_BASE=TRUE NO_TEST=TRUE
19	PCH_FDI_FSYNC<1..0>	NC_PCH_FDI_FSYNC<1..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	PCH_FDI_LSYNC<1..0>	NC_PCH_FDI_LSYNC<1..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	PCH_FDI_INT	NC_PCH_FDI_INT	MAKE_BASE=TRUE NO_TEST=TRUE

PCH Test Points

21	TP_PCH_TP1	NC_PCH_TP1	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP2	NC_PCH_TP2	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP3	NC_PCH_TP3	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP4	NC_PCH_TP4	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP5	NC_PCH_TP5	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP6	NC_PCH_TP6	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP7	NC_PCH_TP7	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP8	NC_PCH_TP8	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP9	NC_PCH_TP9	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP10	NC_PCH_TP10	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP11	NC_PCH_TP11	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP12	NC_PCH_TP12	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP13	NC_PCH_TP13	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP14	NC_PCH_TP14	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP15	NC_PCH_TP15	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP16	NC_PCH_TP16	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP17	NC_PCH_TP17	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP18	NC_PCH_TP18	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP19	NC_PCH_TP19	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP20	NC_PCH_TP20	MAKE_BASE=TRUE NO_TEST=TRUE

PCH PCI

20	TP_PCI_AD<31..0>	NC_PCI_AD<31..0>	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_PCI_C_BE_L<3..0>	NC_PCI_C_BE_L<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_PCI_PAR	NC_PCI_PAR	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_PCI_RESET_L	NC_PCI_RESET_L	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_PCH_PCI_GNT0_L	NC_PCI_GNT0_L	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_INIT3V3_L	NC_PCH_INIT3V3_L	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_LPC_DREQ0_L	NC_LPC_DREQ0_L	MAKE_BASE=TRUE NO_TEST=TRUE

PCH Miscellaneous

18	TP_HDA_SDIN1	NC_HDA_SDIN1	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_HDA_SDIN2	NC_HDA_SDIN2	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_HDA_SDIN3	NC_HDA_SDIN3	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_PWM0	NC_PCH_PWM0	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_PWM1	NC_PCH_PWM1	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_PWM2	NC_PCH_PWM2	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_PWM3	NC_PCH_PWM3	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_SST	NC_PCH_SST	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_CL_CLK1	NC_PCH_CL_CLK1	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_CL_DATA1	NC_PCH_CL_DATA1	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_CL_RST1	NC_PCH_CL_RST1	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_PCI_CLK33M_OUT2	NC_PCI_CLK33M_OUT2	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_PCI_CLK33M_OUT3	NC_PCI_CLK33M_OUT3	MAKE_BASE=TRUE NO_TEST=TRUE

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PAGE TITLE

Unused Signal Aliases

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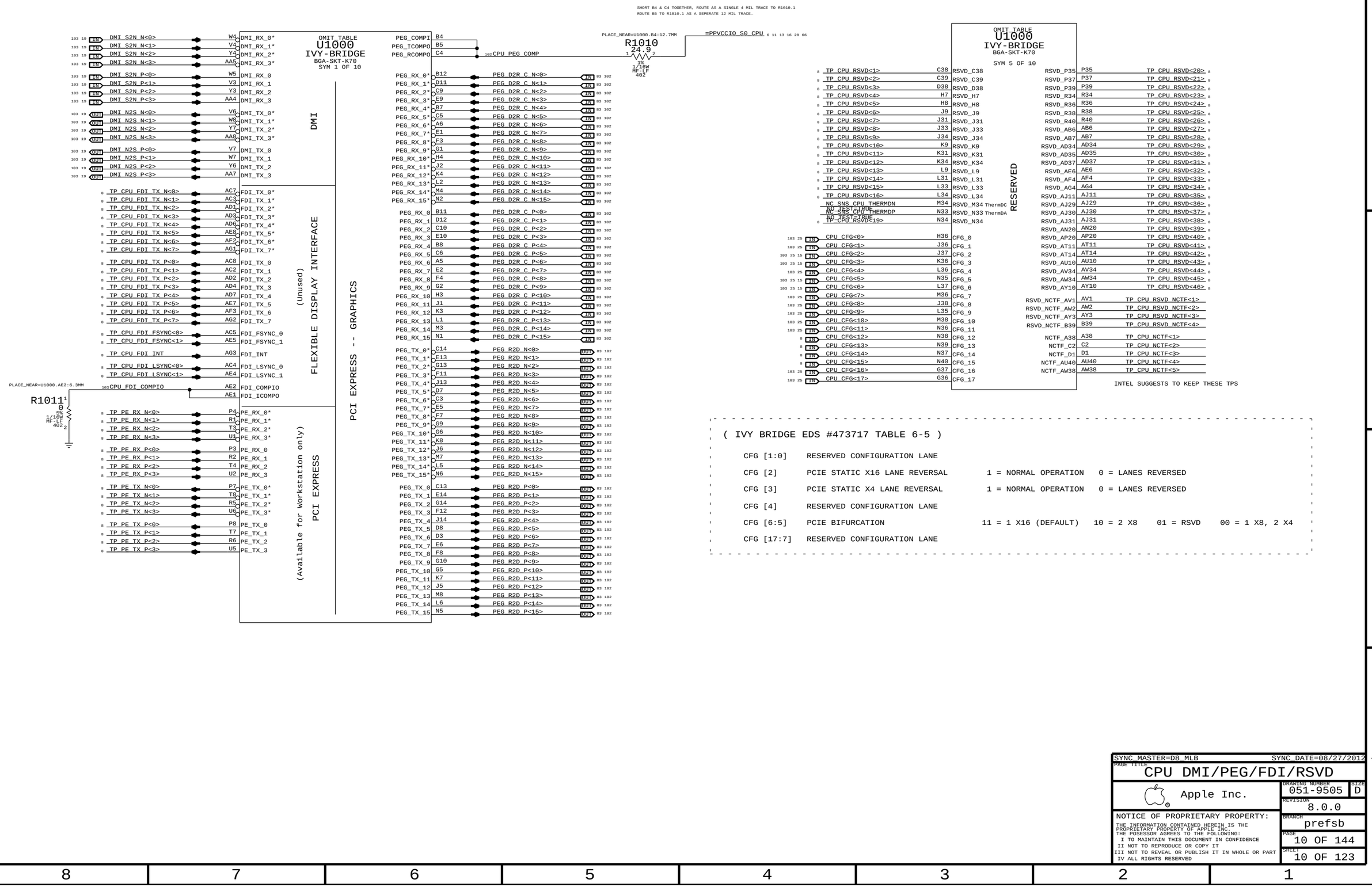

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BASED ON INTEL MOBILE SOLUTION

66 28 16 13 11 10 6 =PPVCCIO_S0_CPU

PLACE_NEAR=U1000.F36:50mm
R1124 75 5% 1/16W MF-LF 402

103 26 IN CPU_RESET_L

R1125 43 5% 1/16W MF-LF 402

103 PLT_RESET_LS1V05_L

16 13 11 6 =PP1V5_S0_CPU_MEM

R1120 200 1% 1/16W MF-LF 402

FROM PCH

103 28 19 IN PM_MEM_PWRGD

R1121 130 1% 1/16W MF-LF 402

103 PM_MEM_PWRGD_R

66 28 16 13 11 10 6 =PPVCCIO_S0_CPU

R1101 51 5% 1/16W MF-LF 402

R1102 0 1/16W MF-LF 5% 402

103 64 OUT CPU_SKTOCC_L
103 19 OUT CPU_PROC_SEL
103 48 OUT CPU_CATERR_L
103 48 47 21 IO CPU_PECI
103 66 48 47 IO CPU_PROCHOT_L
103 48 OUT CPU_THRMTRIP_L
103 19 IN PM_SYNC
103 28 25 21 IN CPU_PWRGD
103 28 OUT CPU_MEM_RESET_L
110 11 CPU_DDR_VREF
110 34 OUT CPU_DIMM_VREF_DAC_B
110 34 OUT CPU_DIMM_VREF_DAC_A

CPU_PROCHOT_R_L

OMIT_TABLE
U1000
IVY-BRIDGE
BGA-SKT-K70
SYM 2 OF 10

AJ33	SKTOCC*	THERMAL
K32	PROC_SEL	
E37	CATERR*	
J35	PECI	
H34	PROCHOT*	
G35	THERMTRIP*	
F36	RESET*	PWR MGMT
E38	PM_SYNC	
J40	UNCOREPWRGOOD	
AJ19	SM_DRAMPWROK	DDR3 MISC
AW18	SM_DRAMRST*	
AJ22	SM_VREF	
AH1	SB_DIMM_VREFDQ	
AH4	SA_DIMM_VREFDQ	

BCLK_ITP	C40	ITPCPU_CLK100M_P	15 103 IN
BCLK_ITP*	D40	ITPCPU_CLK100M_N	15 103 IN
BCLK_0	W2	DMI_CLK100M_CPU_P	18 103 IN
BCLK_0*	W1	DMI_CLK100M_CPU_N	18 103 IN
PRDY*	K38	XDP_CPU_PRDY_L	25 103 OUT
PREQ*	K40	XDP_CPU_PREQ_L	25 103 IN
TCK	M40	XDP_CPU_TCK	25 103 IN
TMS	L38	XDP_CPU_TMS	25 103 IN
TRST*	J39	XDP_CPU_TRST_L	25 103 IN
TDI	L40	XDP_CPU_TDI	25 103 IN
TDO	L39	XDP_CPU_TDO	25 103 OUT
DBR*	E39	XDP_DBRESET_L	25 103 OUT
BPM[0]*	H40	XDP_BPM_L<0>	25 103 BI
BPM[1]*	H38	XDP_BPM_L<1>	25 103 BI
BPM[2]*	G38	XDP_BPM_L<2>	25 103 BI
BPM[3]*	G40	XDP_BPM_L<3>	25 103 BI
BPM[4]*	G39	XDP_BPM_L<4>	25 103 BI
BPM[5]*	F38	XDP_BPM_L<5>	25 103 BI
BPM[6]*	E40	XDP_BPM_L<6>	25 103 BI
BPM[7]*	F40	XDP_BPM_L<7>	25 103 BI

CLOCKS
JTAG & BPM

R1111 1K 5% 1/16W MF-LF 402

16 13 11 6 =PP1V5_S0_CPU_MEM

R1140 1K 1% 1/16W MF-LF 402

CPU_DDR_VREF 11 110

R1141 1K 1% 1/16W MF-LF 402

C1140 0.1UF 10% 16V X7R-CERM 0402

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CPU CLOCK/MISC/JTAG

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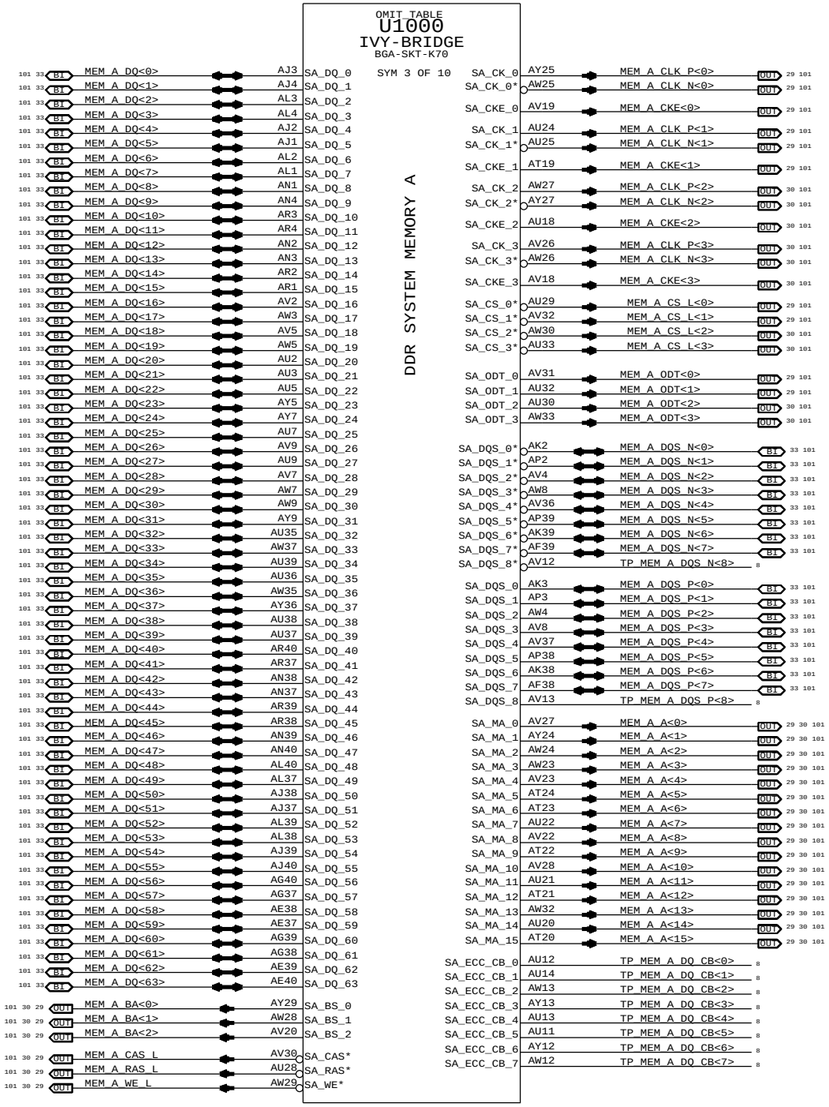

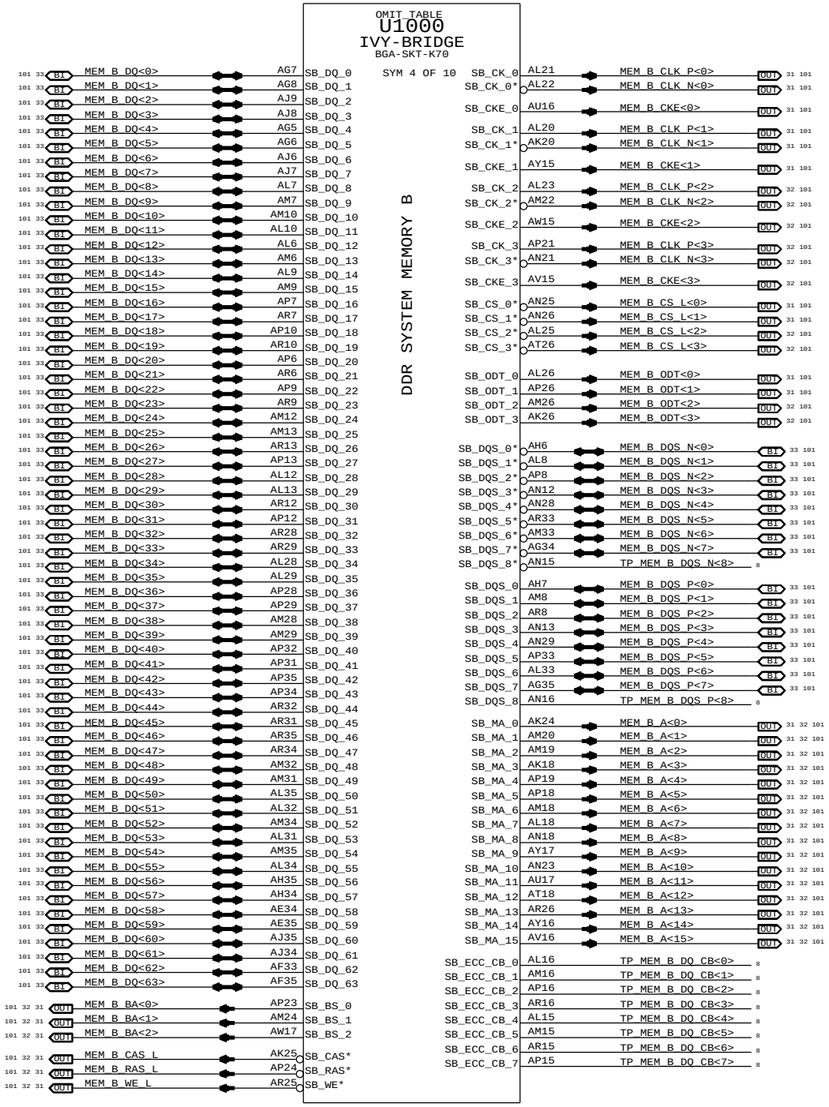

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CPU DDR3 INTERFACES

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66 51 16 13 6 =PPVCORE_S0_CPU

OMIT_TABLE
U1000
IVY-BRIDGE
BGA-SKT-K70
SYM 10 OF 10

POWER
CPU CORE SUPPLY

F16	VCC_071	VCC_131	K22
F18	VCC_072	VCC_132	K24
F19	VCC_073	VCC_133	K25
F21	VCC_074	VCC_134	K27
F22	VCC_075	VCC_135	K28
F24	VCC_076	VCC_136	K30
F25	VCC_077	VCC_137	L13
F27	VCC_078	VCC_138	L14
F28	VCC_079	VCC_139	L15
F30	VCC_080	VCC_140	L16
F31	VCC_081	VCC_141	L18
F32	VCC_082	VCC_142	L19
F33	VCC_083	VCC_143	L21
F34	VCC_084	VCC_144	L22
G15	VCC_085	VCC_145	L24
G16	VCC_086	VCC_146	L25
G18	VCC_087	VCC_147	L27
G19	VCC_088	VCC_148	L28
G21	VCC_089	VCC_149	L30
G22	VCC_090	VCC_150	M14
G24	VCC_091	VCC_151	M15
G25	VCC_092	VCC_152	M16
G27	VCC_093	VCC_153	M18
G28	VCC_094	VCC_154	M19
G30	VCC_095	VCC_155	M21
G31	VCC_096	VCC_156	M22
G32	VCC_097	VCC_157	M24
G33	VCC_098	VCC_158	M25
H13	VCC_099	VCC_159	M27
H14	VCC_100	VCC_160	M28
H15	VCC_101	VCC_161	M30
H16	VCC_102		
H18	VCC_103		
H19	VCC_104		
H21	VCC_105		
H22	VCC_106		
H24	VCC_107		
H25	VCC_108		
H27	VCC_109		
H28	VCC_110		
H30	VCC_111		
H31	VCC_112		
H32	VCC_113		
J12	VCC_114		
J15	VCC_115		
J16	VCC_116		
J18	VCC_117		
J19	VCC_118		
J21	VCC_119		
J22	VCC_120		
J24	VCC_121		
J25	VCC_122		
J27	VCC_123		
J28	VCC_124		
J30	VCC_125		
K15	VCC_126		
K16	VCC_127		
K18	VCC_128		
K19	VCC_129		
K21	VCC_130		

=PPVCCSA_S0_CPU 6 16

VCCSA

VCCSA0	H10		
VCCSA1	H11		
VCCSA2	H12		
VCCSA3	J10		
VCCSA4	K10		
VCCSA5	K11		
VCCSA6	L11		
VCCSA7	L12		
VCCSA8	M10		
VCCSA9	M11		
VCCSA10	M12		

NCTF

VSS_NCTF0	A4		
VSS_NCTF1	B3		
VSS_NCTF2	AV39		
VSS_NCTF3	AY37		

66 51 16 13 6 =PPVCORE_S0_CPU

OMIT_TABLE
U1000
IVY-BRIDGE
BGA-SKT-K70
SYM 6 OF 10

POWER
CPU CORE SUPPLY

A12	VCC_001	VCCIO_01	A11
A13	VCC_002	VCCIO_02	A7
A14	VCC_003	VCCIO_03	AA3
A15	VCC_004	VCCIO_04	AB8
A16	VCC_005	VCCIO_05	AF8
A18	VCC_006	VCCIO_06	AG33
A24	VCC_007	VCCIO_07	AJ16
A25	VCC_008	VCCIO_08	AJ17
A27	VCC_009	VCCIO_09	AJ26
A28	VCC_010	VCCIO_10	AJ28
B15	VCC_011	VCCIO_11	AJ32
B16	VCC_012	VCCIO_12	AK15
B18	VCC_013	VCCIO_13	AK17
B24	VCC_014	VCCIO_14	AK19
B25	VCC_015	VCCIO_15	AK21
B27	VCC_016	VCCIO_16	AK23
B28	VCC_017	VCCIO_17	AK27
B30	VCC_018	VCCIO_18	AK29
B31	VCC_019	VCCIO_19	AK30
B33	VCC_020	VCCIO_20	B9
B34	VCC_021	VCCIO_21	D10
C15	VCC_022	VCCIO_22	D6
C16	VCC_023	VCCIO_23	E3
C18	VCC_024	VCCIO_24	E4
C19	VCC_025	VCCIO_25	G3
C21	VCC_026	VCCIO_26	G4
C22	VCC_027	VCCIO_27	J3
C24	VCC_028	VCCIO_28	J4
C25	VCC_029	VCCIO_29	J7
C27	VCC_030	VCCIO_30	J8
C28	VCC_031	VCCIO_31	L3
C30	VCC_032	VCCIO_32	L4
C31	VCC_033	VCCIO_33	L7
C33	VCC_034	VCCIO_34	M13
C34	VCC_035	VCCIO_35	N3
C36	VCC_036	VCCIO_36	N4
D13	VCC_037	VCCIO_37	N7
D14	VCC_038	VCCIO_38	R3
D15	VCC_039	VCCIO_39	R4
D16	VCC_040	VCCIO_40	R7
D18	VCC_041	VCCIO_41	U3
D19	VCC_042	VCCIO_42	U4
D21	VCC_043	VCCIO_43	U7
D22	VCC_044	VCCIO_44	V8
D24	VCC_045	VCCIO_45	W3
D25	VCC_046		
D27	VCC_047		
D28	VCC_048		
D30	VCC_049		
D31	VCC_050		
D33	VCC_051		
D34	VCC_052		
D35	VCC_053		
D36	VCC_054		
E15	VCC_055		
E16	VCC_056		
E18	VCC_057		
E19	VCC_058		
E21	VCC_059		
E22	VCC_060		
E24	VCC_061		
E25	VCC_062		
E27	VCC_063		
E28	VCC_064		
E30	VCC_065		
E31	VCC_066		
E33	VCC_067		
E34	VCC_068		
E35	VCC_069		
F15	VCC_070		

=PPVCCIO_S0_CPU 6 10 11 13 16 28 66

IO POWER

CPU VIDS

VCCIO_SEL	P33	NC_CPU_VCCIO_VID	NO_TEST=TRUE
VCCSA_VID	P34	NC_CPU_VCCSA_VID	NO_TEST=TRUE
VIDALERT*	A37	109 CPU_VIDALERT_R_L	
VIDSCLK	C37	109 CPU_VIDSCLK_R	
VIDSOUT	B37	109 CPU_VIDSOUT_R	

SENSE LINES

VCCSA_SENSE	T2	SNS_CPU_VCCSA	OUT 70 108
VCC_SENSE	A36	SNS_CPU_VCORE_P	OUT 66 109
VSS_SENSE	B36	SNS_CPU_VCORE_N	OUT 66 109
VCCIO_SENSE	AB4	SNS_CPU_VCCIO_P	OUT 69 108
VSSIO_SENSE	AB3	SNS_CPU_VCCIO_N	OUT 69 108
VCCAXG_SENSE	L32	SNS_CPU_VAXG_P	OUT 66 109
VSSAXG_SENSE	M32	SNS_CPU_VAXG_N	OUT 66 109

PLACE_NEAR=U1000.B37:10mm
R1302 110 1% 1/16W MF-LF 402

PLACE_NEAR=U1000.A37:10mm
R1300 75 1% 1/16W MF-LF 402

=PPVCCIO_S0_CPU 6 10 11 13 16 28 66

R1310 44.2 1% MF-LF 1/16W 402 — CPU_VIDALERT_L IN 66 109

R1311 0 5% MF-LF 1/16W 402 — CPU_VIDSCLK OUT 66 109

R1312 0 5% MF-LF 1/16W 402 — CPU_VIDSOUT BI 66 109

66 51 17 6 =PPVAXG_S0_CPU

OMIT_TABLE
U1000
IVY-BRIDGE
BGA-SKT-K70
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POWER
GRAPHICS

AB33	VCCAXG_01	VCCAXG_21	T37
AB34	VCCAXG_02	VCCAXG_22	T38
AB35	VCCAXG_03	VCCAXG_23	T39
AB36	VCCAXG_04	VCCAXG_24	T40
AB37	VCCAXG_05	VCCAXG_25	U33
AB38	VCCAXG_06	VCCAXG_26	U34
AB39	VCCAXG_07	VCCAXG_27	U35
AB40	VCCAXG_08	VCCAXG_28	U36
AC33	VCCAXG_09	VCCAXG_29	U37
AC34	VCCAXG_10	VCCAXG_30	U38
AC35	VCCAXG_11	VCCAXG_31	U39
AC36	VCCAXG_12	VCCAXG_32	U40
AC37	VCCAXG_13	VCCAXG_33	W33
AC38	VCCAXG_14	VCCAXG_34	W34
AC39	VCCAXG_15	VCCAXG_35	W35
AC40	VCCAXG_16	VCCAXG_36	W36
T33	VCCAXG_17	VCCAXG_37	W37
T34	VCCAXG_18	VCCAXG_38	W38
T35	VCCAXG_19	VCCAXG_39	Y33
T36	VCCAXG_20	VCCAXG_40	Y34
		VCCAXG_41	Y35
		VCCAXG_42	Y36
		VCCAXG_43	Y37
		VCCAXG_44	Y38

=PP1V5_S0_CPU_MEM 6 11 16

DDR3-1.5V RAILS

VDDQ0	AJ13	VDDQ11	AU23
VDDQ1	AJ14	VDDQ12	AU27
VDDQ2	AJ20	VDDQ13	AU31
VDDQ3	AJ23	VDDQ14	AV21
VDDQ4	AJ24	VDDQ15	AV24
VDDQ5	AR20	VDDQ16	AV25
VDDQ6	AR21	VDDQ17	AV29
VDDQ7	AR22	VDDQ18	AV33
VDDQ8	AR23	VDDQ19	AW31
VDDQ9	AR24	VDDQ20	AY23
VDDQ10	AU19	VDDQ21	AY26
		VDDQ22	AY28

=PP1V8_S0_CPU_PLL 6 16

1.8V

VCCPLL0	AK11		
VCCPLL1	AK12		

SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012

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CPU POWER

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OMIT TABLE
U1000
IVY-BRIDGE
BGA-SKT-K70

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VSS

A17	VSS_001	VSS_091	AM27
A23	VSS_002	VSS_092	AM3
A26	VSS_003	VSS_093	AM30
A29	VSS_004	VSS_094	AM36
A35	VSS_005	VSS_095	AM37
AA33	VSS_006	VSS_096	AM38
AA34	VSS_007	VSS_097	AM39
AA35	VSS_008	VSS_098	AM4
AA36	VSS_009	VSS_099	AM40
AA37	VSS_010	VSS_100	AM5
AA38	VSS_011	VSS_101	AN10
AA6	VSS_012	VSS_102	AN11
AB5	VSS_013	VSS_103	AN14
AC1	VSS_014	VSS_104	AN17
AC6	VSS_015	VSS_105	AN19
AD33	VSS_016	VSS_106	AN22
AD36	VSS_017	VSS_107	AN24
AD38	VSS_018	VSS_108	AN27
AD39	VSS_019	VSS_109	AN30
AD40	VSS_020	VSS_110	AN31
AD5	VSS_021	VSS_111	AN32
AD8	VSS_022	VSS_112	AN33
AE3	VSS_023	VSS_113	AN34
AE33	VSS_024	VSS_114	AN35
AE36	VSS_025	VSS_115	AN36
AF1	VSS_026	VSS_116	AN5
AF34	VSS_027	VSS_117	AN6
AF36	VSS_028	VSS_118	AN7
AF37	VSS_029	VSS_119	AN8
AF40	VSS_030	VSS_120	AN9
AF5	VSS_031	VSS_121	AP1
AF6	VSS_032	VSS_122	AP11
AF7	VSS_033	VSS_123	AP14
AG36	VSS_034	VSS_124	AP17
AH2	VSS_035	VSS_125	AP22
AH3	VSS_036	VSS_126	AP25
AH33	VSS_037	VSS_127	AP27
AH36	VSS_038	VSS_128	AP30
AH37	VSS_039	VSS_129	AP36
AH38	VSS_040	VSS_130	AP37
AH39	VSS_041	VSS_131	AP4
AH40	VSS_042	VSS_132	AP40
AH5	VSS_043	VSS_133	AP5
AH8	VSS_044	VSS_134	AR11
AJ12	VSS_045	VSS_135	AR14
AJ15	VSS_046	VSS_136	AR17
AJ18	VSS_047	VSS_137	AR18
AJ21	VSS_048	VSS_138	AR19
AJ25	VSS_049	VSS_139	AR27
AJ27	VSS_050	VSS_140	AR30
AJ36	VSS_051	VSS_141	AR36
AJ5	VSS_052	VSS_142	AR5
AK1	VSS_053	VSS_143	AT1
AK10	VSS_054	VSS_144	AT10
AK13	VSS_055	VSS_145	AT12
AK14	VSS_056	VSS_146	AT13
AK16	VSS_057	VSS_147	AT15
AK22	VSS_058	VSS_148	AT16
AK28	VSS_059	VSS_149	AT17
AK31	VSS_060	VSS_150	AT2
AK32	VSS_061	VSS_151	AT25
AK33	VSS_062	VSS_152	AT27
AK34	VSS_063	VSS_153	AT28
AK35	VSS_064	VSS_154	AT29
AK36	VSS_065	VSS_155	AT3
AK37	VSS_066	VSS_156	AT30
AK4	VSS_067	VSS_157	AT31
AK40	VSS_068	VSS_158	AT32
AK5	VSS_069	VSS_159	AT33
AK6	VSS_070	VSS_160	AT34
AK7	VSS_071	VSS_161	AT35
AK8	VSS_072	VSS_162	AT36
AK9	VSS_073	VSS_163	AT37
AL11	VSS_074	VSS_164	AT38
AL14	VSS_075	VSS_165	AT39
AL17	VSS_076	VSS_166	AT4
AL19	VSS_077	VSS_167	AT40
AL24	VSS_078	VSS_168	AT5
AL27	VSS_079	VSS_169	AT6
AL30	VSS_080	VSS_170	AT7
AL36	VSS_081	VSS_171	AT8
AL5	VSS_082	VSS_172	AT9
AM1	VSS_083	VSS_173	AU1
AM11	VSS_084	VSS_174	AU15
AM14	VSS_085	VSS_175	AU26
AM17	VSS_086	VSS_176	AU34
AM2	VSS_087	VSS_177	AU4
AM21	VSS_088	VSS_178	AU6
AM23	VSS_089	VSS_179	AU8
AM25	VSS_090	VSS_180	AV10

OMIT TABLE
U1000
IVY-BRIDGE
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VSS

AV11	VSS_181	VSS_271	G8
AV14	VSS_182	VSS_272	H1
AV17	VSS_183	VSS_273	H17
AV3	VSS_184	VSS_274	H2
AV35	VSS_185	VSS_275	H20
AV38	VSS_186	VSS_276	H23
AV6	VSS_187	VSS_277	H26
AW10	VSS_188	VSS_278	H29
AW11	VSS_189	VSS_279	H33
AW14	VSS_190	VSS_280	H35
AW16	VSS_191	VSS_281	H37
AW36	VSS_192	VSS_282	H39
AW6	VSS_193	VSS_283	H5
AY11	VSS_194	VSS_284	H6
AY14	VSS_195	VSS_285	H9
AY18	VSS_196	VSS_286	J11
AY35	VSS_197	VSS_287	J17
AY4	VSS_198	VSS_288	J20
AY6	VSS_199	VSS_289	J23
AY8	VSS_200	VSS_290	J26
B10	VSS_201	VSS_291	J29
B13	VSS_202	VSS_292	J32
B14	VSS_203	VSS_293	K1
B17	VSS_204	VSS_294	K12
B23	VSS_205	VSS_295	K13
B26	VSS_206	VSS_296	K14
B29	VSS_207	VSS_297	K17
B32	VSS_208	VSS_298	K2
B35	VSS_209	VSS_299	K20
B38	VSS_210	VSS_300	K23
B6	VSS_211	VSS_301	K26
C11	VSS_212	VSS_302	K29
C12	VSS_213	VSS_303	K33
C17	VSS_214	VSS_304	K35
C20	VSS_215	VSS_305	K37
C23	VSS_216	VSS_306	K39
C26	VSS_217	VSS_307	K5
C29	VSS_218	VSS_308	K6
C32	VSS_219	VSS_309	L10
C35	VSS_220	VSS_310	L17
C7	VSS_221	VSS_311	L20
C8	VSS_222	VSS_312	L23
D17	VSS_223	VSS_313	L26
D2	VSS_224	VSS_314	L29
D20	VSS_225	VSS_315	L8
D23	VSS_226	VSS_316	M1
D26	VSS_227	VSS_317	M17
D29	VSS_228	VSS_318	M2
D32	VSS_229	VSS_319	M20
D37	VSS_230	VSS_320	M23
D39	VSS_231	VSS_321	M26
D4	VSS_232	VSS_322	M29
D5	VSS_233	VSS_323	M33
D9	VSS_234	VSS_324	M35
E11	VSS_235	VSS_325	M37
E12	VSS_236	VSS_326	M39
E17	VSS_237	VSS_327	M5
E20	VSS_238	VSS_328	M6
E23	VSS_239	VSS_329	M9
E26	VSS_240	VSS_330	N8
E29	VSS_241	VSS_331	P1
E32	VSS_242	VSS_332	P2
E36	VSS_243	VSS_333	P36
E7	VSS_244	VSS_334	P38
E8	VSS_245	VSS_335	P40
F1	VSS_246	VSS_336	P5
F10	VSS_247	VSS_337	P6
F13	VSS_248	VSS_338	R33
F14	VSS_249	VSS_339	R35
F17	VSS_250	VSS_340	R37
F2	VSS_251	VSS_341	R39
F20	VSS_252	VSS_342	R8
F23	VSS_253	VSS_343	T1
F26	VSS_254	VSS_344	T5
F29	VSS_255	VSS_345	T6
F35	VSS_256	VSS_346	U8
F37	VSS_257	VSS_347	V1
F39	VSS_258	VSS_348	V2
F5	VSS_259	VSS_349	V33
F6	VSS_260	VSS_350	V34
F9	VSS_261	VSS_351	V35
G11	VSS_262	VSS_352	V36
G12	VSS_263	VSS_353	V37
G17	VSS_264	VSS_354	V38
G20	VSS_265	VSS_355	V39
G23	VSS_266	VSS_356	V40
G26	VSS_267	VSS_357	V5
G29	VSS_268	VSS_358	W6
G34	VSS_269	VSS_359	Y5
G7	VSS_270	VSS_360	Y8

SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012

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CPU GROUNDS

Apple Inc.

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REVISION 8.0.0

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=PP3V3_S5_PCH_STRAPS
R1501 10K 5% 1/16W MF-LF 402 — SMC_WAKE_SCI_L
R1502 10K 5% 1/16W MF-LF 402 — TBT_GO2SX_BIDIR
R1504 10K 5% 1/16W MF-LF 402 — PCH_SUSWARN_L
R1563 10K 5% 1/16W MF-LF 402 — PCH_GPIO72
R1564 4.7K 5% 1/16W MF-LF 402 — PM_PWRBTN_L
R1505 10K 5% 1/16W MF-LF 402 — AP_PWR_EN
R1591 10K 5% 1/16W MF-LF 402 — PCH_SMBALERT_L

=PP3V3_S0_LED_SATA
R1556 10K 5% 1/16W MF-LF 402 — PCH_SATALED_L

=PP3V3_S5_PCH_STRAPS
R1520 10K 5% 1/16W MF-LF 402 — SDCONN_STATE_CHANGE
R1519 10K 5% 1/16W MF-LF 402 — USB_EXTA_OC_L
R1518 10K 5% 1/16W MF-LF 402 — USB_EXTB_OC_L
R1517 10K 5% 1/16W MF-LF 402 — USB_EXTC_OC_L
R1516 10K 5% 1/16W MF-LF 402 — USB_EXTD_OC_L
R1536 1K 5% 1/16W MF-LF 402 — USB_EXTB_OC_EHCI_L
R1537 1K 5% 1/16W MF-LF 402 — USB_EXTD_OC_EHCI_L

=PP3V3_S0_PCH_GPIO
R1558 10K 5% 1/16W MF-LF 402 — BT_PWR_RST_L
R1557 10K 5% 1/16W MF-LF 402 — TBT_PWR_REQ_L

NOSTUFF R1553 0 5% 1/16W MF-LF 402 — ITPXDP_CLK100M_N — ITPCPU_CLK100M_N
NOSTUFF R1554 0 5% 1/16W MF-LF 402 — ITPXDP_CLK100M_P — ITPCPU_CLK100M_P

HDA_SYNC — R1514 1K 5% 1/16W MF-LF 402

=PP3V3_S5_PCH_STRAPS
SPI_DESCRIPTOR_OVERRIDE_L — Q1500 NTR1P02L SOT23-3-HF (G, S, D)

PLACE_NEAR=R1805.1:3MM
SPI_DESCRIPTOR_OVERRIDE_R — R1552 330 5% 1/16W MF-LF 402 — HDA_SDOUT_R

=PP3V3_S0_PCH_STRAPS
R1590 10K 5% 1/16W MF-LF 402
CRITICAL Q1509 SSM3K15AMFVAPE VESM (D, G, S)
DP_AUXCH_ISOL

=PP3V3_S0_PCH_GPIO
U1501.5:3MM C1501 0.1UF 10% 16V X7R-CERM 0402
U1501 74LVC1G08GW SOT353
DP_AUXCH_ISOL_EN
PM_PCH_PWROK
DP_AUXIO_EN

DP_AUXCH_ISOL IS ACTIVE LOW!

DP_AUXIO_EN Inversion
Inverts PCH GPIO DP_AUXCH_ISOL to drive DP_AUXIO_EN for external DP

DP_AUXIO_EN GLITCHES ON S0/S3 TRANSITIONS RDAR://11085566

=PP3V3_S0_PCH_STRAPS
R1509 10K 5% 1/16W MF-LF 402 — DP_AUXCH_ISOL
R1510 10K 5% 1/16W MF-LF 402 — PCH_GPIO1
R1511 10K 5% 1/16W MF-LF 402 — PCH_GPIO48

=PP3V3_S5_PCH_STRAPS
R1540 10K 5% 1/16W MF-LF 402 — TBT_PCH_CLKREQ_L
R1539 10K 5% 1/16W MF-LF 402 — ENET_CLKREQ_L
R1541 10K 5% 1/16W MF-LF 402 — SSD_CLKREQ_L
R1538 10K 5% 1/16W MF-LF 402 — AP_CLKREQ_L

=PP3V3_TBT_PCH_GPIO
NOSTUFF R1565 10K 5% 1/16W MF-LF 402 — TBT_SW_RESET_R_L

AP CLKREQ# ISOLATION

=PP3V3_S4_AP
R1587 10K 5% 1/16W MF-LF 402
Q1550 SSM3K15FV SOD-VESM-HF (G, D, S)
AP_CLKREQ_L (OUT) — AP_CLKREQ_L_ISO

ISOLATION FET TO PREVENT LEAKAGE ON AP_PWR_EN AND AP_CLKREQ_L RDAR://11068662

AP PWR_EN ISOLATION

=PP3V3_S4_AP
R1588 10K 5% 1/16W MF-LF 402
Q1560 SSM3K15FV SOD-VESM-HF (G, D, S)
AP_PWR_EN (OUT) — AP_PWR_EN_ISO

IVB PCIe Straps configuration:

CFG[5:6] = Sel PCIe Cfg
11 = 1x16 (default)
10 = 2x8
00 = 1x8,2x4

CFG[3]=Direct/Rev for X4
1 = DIR
0 = REV

CFG[2]= Direct/Rev for x16
1 = DIR
0 = REV

=PP3V3_S0_PCH_STRAPS
4.7K 5% 1/16W MF-LF 402 — R1529 PCH_SPKR
10K 5% 1/16W MF-LF 402 — R1528 SATARDRVR_EN
10K 5% 1/16W MF-LF 402 — R1542 SMC_RUNTIME_SCI_L
10K 5% 1/16W MF-LF 402 — R1508 PEG_CLKREQ_L

10K 5% 1/16W MF-LF 402 — R1527 PCH_CAM_EXT_BOOT_L
10K 5% 1/16W MF-LF 402 — R1526 PCH_CAM_RESET
2.0K 1% 1/16W MF-LF 402 — R1525 PCH_BLC_MCU_RESET_R
2.0K 1% 1/16W MF-LF 402 — R1524 PCH_BLC_EXT_BOOT_R

=PP3V3_S0_PCH_GPIO
R1595 10K 5% 1/16W MF-LF 402
CRITICAL Q1540 SSM6N15AFE SOT563
JTAG_TBT_TDO
=PP3V3_TBT_PCH_GPIO
R1562 10K 5% 1/16W MF-LF 402
JTAG_TBT_TDO_ISOL
NOSTUFF R1598 0 5% 1/16W MF-LF 402

=PP3V3_S0_PCH_GPIO
R1597 10K 5% 1/16W MF-LF 402
Q1530 SSM3K15FV SOD-VESM-HF (G, D, S)
JTAG_TBT_TMS
=PP3V3_TBT_PCH_GPIO
R1594 10K 5% 1/16W MF-LF 402
JTAG_TBT_TMS_ISOL
NOSTUFF R1500 0 5% 1/16W MF-LF 402

=PP3V3_S0_PCH_GPIO
R1596 10K 5% 1/16W MF-LF 402
CRITICAL Q1540 SSM6N15AFE SOT563
JTAG_TBT_TDI
=PP3V3_TBT_PCH_GPIO
R1561 10K 5% 1/16W MF-LF 402
JTAG_TBT_TDI_ISOL
NOSTUFF R1599 0 5% 1/16W MF-LF 402

=PP3V3_S0_PCH_GPIO
U1500.5:3MM C1500 0.1UF 10% 16V X7R-CERM 0402
U1500 74LVC1G08GW SOT353
JTAG_TBT_TCK
JTAG_TBT_TCK_ISOL
=PP3V3_TBT_PCH_GPIO
R1586 10K 5% 1/16W MF-LF 402
NOSTUFF R1585 0 5% 1/16W MF-LF 402 — TBT_PWR_EN — TBT_PWR_EN_R
R1593 10K 5% 1/16W MF-LF 402

TBT JTAG_TCK ISOLATION

D8: ISOLATION FET TO PREVENT TBT 3V3_TBTLC LEAKAGE RDAR://10885566

D7/D7I: CHECK CACTUSRIDGE POWER SEQUENCING & LEAKAGE RDAR://10739300

NOSTUFF R1584 0 5% 1/16W MF-LF 402
D1521 BAT54XV2T1 SOD-523 (A, K)
TBT_CIO_PLUG_EVENT_ISOL — TBT_CIO_PLUG_EVENT
R1583 10K 5% 1/16W MF-LF 402
R1521 10K 5% 1/16W MF-LF 402

CPU_CFG<5> — 1K 5% 1/16W MF-LF 402 — NOSTUFF R1512 — PLACE_NEAR=U1000.N35:20MM
CPU_CFG<6> — 1K 5% 1/16W MF-LF 402 — NOSTUFF R1513 — PLACE_NEAR=U1000.L37:20MM
CPU_CFG<3> — 1K 5% 1/16W MF-LF 402 — NOSTUFF R1523 — PLACE_NEAR=U1000.K36:20MM
CPU_CFG<2> — 1K 5% 1/16W MF-LF 402 — R1522 — PLACE_NEAR=U1000.J37:20MM

PM_SLP_S3_L — 100K 5% 1/16W MF-LF 402 — R1571
PM_SLP_S4_L — 100K 5% 1/16W MF-LF 402 — R1570
PM_SLP_S5_L — 100K 5% 1/16W MF-LF 402 — R1535
ENET_LOW_PWR_PCH — 10K 5% 1/16W MF-LF 402 — R1534
PCH_GPIO22 — 10K 5% 1/16W MF-LF 402 — R1533
PCH_GPIO6 — 20K 5% 1/16W MF-LF 402 — R1532
ENET_MEDIA_SENSE — 10K 5% 1/16W MF-LF 402 — R1531
WOL_EN — 10K 5% 1/16W MF-LF 402 — R1530
PCH_GPIO29 — 10K 5% 1/16W MF-LF 402 — R1555

UNUSED clock terminations for FCIM MODE

PCH_CLKIN_GND1 — 10K 5% 1/16W MF-LF 402 — R1551
PCH_CLKIN_GND0 — 10K 5% 1/16W MF-LF 402 — R1550
PCH_CLK14P3M_REFCLK — 10K 5% 1/16W MF-LF 402 — R1549
PCH_CLK100M_DMIN — 10K 5% 1/16W MF-LF 402 — R1548 — PLACE_NEAR=U1800.P33:5mm
PCH_CLK100M_DMIP — 10K 5% 1/16W MF-LF 402 — R1547 — PLACE_NEAR=U1800.R33:5mm
PCH_CLK100M_SATAN — 10K 5% 1/16W MF-LF 402 — R1546 — PLACE_NEAR=U1800.AF55:6MM
PCH_CLK100M_SATAP — 10K 5% 1/16W MF-LF 402 — R1545 — PLACE_NEAR=U1800.AG56:5mm
PCH_CLK96M_DOTN — 10K 5% 1/16W MF-LF 402 — R1544 — PLACE_NEAR=U1800.BD38:5mm
PCH_CLK96M_DOTP — 10K 5% 1/16W MF-LF 402 — R1543 — PLACE_NEAR=U1800.BF38:5mm

TBT CLKREQ# ISOLATION

=PP3V3_TBTLC_RTR
R1592 10K 5% 1/16W MF-LF 402
Q1510 SSM3K15FV SOD-VESM-HF (G, D, S)
TBT_PCH_CLKREQ_L (OUT) — TBT_CLKREQ_L

SYNC_MASTER=D8_MLB — SYNC_DATE=08/27/2012
PAGE TITLE: STRAPS, PULL UPS, PULL DOWNS FOR PCH AND CPU

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CPU VCORE DECOUPLING

14x 22UF,0805 INTEL RECOMMENDATION 18X 22UF 0805 (14 Inside cavity and 4 North of processor)

PLACEMENT_NOTE (C1600-C1613): REPLACED WITH 603 PER RDAR://10700439

16 13 6 66 51 =PPVCORE_S0_CPU

C1600 C1601 C1602 C1603 C1604 C1605 C1606 C1607 C1608 C1609
22UF 20% 6.3V X5R-CERM2 0603

C1610 C1611 C1612 C1613
22UF 20% 6.3V X5R-CERM2 0603

BULK CAPS ON CPU VREG PAGE 72

10x 10UF and 10x 1UF CAPACITORS

66 51 16 13 6 =PPVCORE_S0_CPU

Place inside socket cavity

C1620 C1621 C1622 C1623 C1624 C1625 C1626 C1627 C1628 C1629
10UF 20% 6.3V X5R 603

C1630 C1631 C1632 C1633 C1634 C1635 C1636 C1637 C1638 C1639
1UF 10% 16V X5R 402

CPU VCCIO DECOUPLING

8X 22UF 0805, 6X 10UF 0805 INTEL RECOMMENDATION 9X22UF 0805,16X 0805 placeholders

13 11 10 6 66 28 =PPVCCIO_S0_CPU

PLACEMENT_NOTE (C1650-C1657):

C1650 C1651 C1652 C1653 C1654 C1655 C1656 C1657
22UF 20% 6.3V X5R-CERM2 0603

PLACEMENT_NOTE (C1660-C1665):

Place at edge of socket.

C1660 C1661 C1662 C1663 C1664 C1665
10UF 20% 6.3V X5R 603

BULK CAPS ON CPU VREG PAGE 74

CRITICAL
C1670
330UF-0.0045OHM 20% 6V POLY CASE-D2-SM

CPU VCCSA DECOUPLING

2x 10uF 0603. INTEL RECOMMENDATION 2X 10uF 0805

13 6 =PPVCCSA_S0_CPU

C1666 C1667
10UF 20% 6.3V X6S 603

Bulk decoupling is on VCCSA reg page 75

Memory (CPU VCCDDR) DECOUPLING

13 11 6 =PP1V5_S0_CPU_MEM

C1676 C1677 C1678 C1679 C1680 C1681 C1682 C1683 C1684 C1685 C1686
22UF 20% 6.3V X5R-CERM2 0603
1UF 20% 6.3V X6S 0201

CRITICAL
NOSTUFF
C1687
330UF-0.0045OHM 20% 6V POLY CASE-D2-SM

PLL (CPU VCCSFR) DECOUPLING

2x 47uF, 1x 22uF 0805, 1x 10uF 0603, 1x 4.7uF 0603, 1x 2.2uF 0402, 2x 1uF 0402. INTEL RECOMMENDATION 1x 10uF 0805

13 6 =PP1V8_S0_CPU_PLL

C1693 C1694 C1692 C1691 C1695 C1690 C1696 C1697
1UF 10% 16V X5R 402
2.2UF 10% 6.3V X6S 402
4.7UF 10% 6.3V X5R-CERM 603
10UF 20% 6.3V X6S 603
22UF 20% 6.3V X5R-CERM2 0603
47UF 20% 6.3V X5R 0805

BULK CAPS ON VTT REG PAGE 77

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CPU NON-GFX DECOUPLING

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VAXG DECOUPLING

INTEL RECOMMENDATION 4X22UF 0805,3X 4.7UF

PLACEMENT_NOTE (C1704-C1709):

Place inside socket cavity

AXG BULK CAPS

68 6 PPCPUAXG_S0_REG

C1788 CRITICAL 330UF-0.006OHM 20% 2V POLY CASE-D2-SM
C1789 CRITICAL 330UF-0.006OHM 20% 2V POLY CASE-D2-SM
C1790 CRITICAL 330UF-0.006OHM 20% 2V POLY CASE-D2-SM
C1791 CRITICAL 330UF-0.006OHM 20% 2V POLY CASE-D2-SM
C1792 CRITICAL 330UF-0.006OHM 20% 2V POLY CASE-D2-SM
C1793 CRITICAL 330UF-0.006OHM 20% 2V POLY CASE-D2-SM
C1794 10UF 20% 10V X5R 603
C1795 10UF 20% 10V X5R 603

66 51 13 6 =PPVAXG_S0_CPU

C1704 22UF 20% 6.3V X5R-CERM2 0603
C1705 22UF 20% 6.3V X5R-CERM2 0603
C1706 22UF 20% 6.3V X5R-CERM2 0603
C1707 22UF 20% 6.3V X5R-CERM2 0603
C1708 22UF 20% 6.3V X5R-CERM2 0603
C1709 22UF 20% 6.3V X5R-CERM2 0603

C1710 4.7UF 10% 6.3V X5R-CERM 603
C1711 4.7UF 10% 6.3V X5R-CERM 603
C1712 4.7UF 10% 6.3V X5R-CERM 603

6 =PP3V3_S0_PCH_VCC_ADAC — R1720 0 5% 1/16W MF-LF 402 — PP3V3_S0_PCH_VCCA_DAC_F 22 121
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V

6 =PP1V05_S0_PCH_VCC_ADPLL — R1730 0 5% 1/16W MF-LF 402 — PP1V05_S0_PCH_VCCADPLLA_F 22 120
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=1.05V

C1731 1UF 10% 6.3V CERM 402 PLACE C1731 AT BALL U1800.AB1

R1740 0 5% 1/16W MF-LF 402 — PP1V05_S0_PCH_VCCADPLLB_F 22 120
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=1.05V

C1741 1UF 10% 6.3V CERM 402 PLACE C1741 AT BALL U1800.AC2

SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012

PAGE TITLE: GFX DECOUPLING & PCH PWR ALIAS

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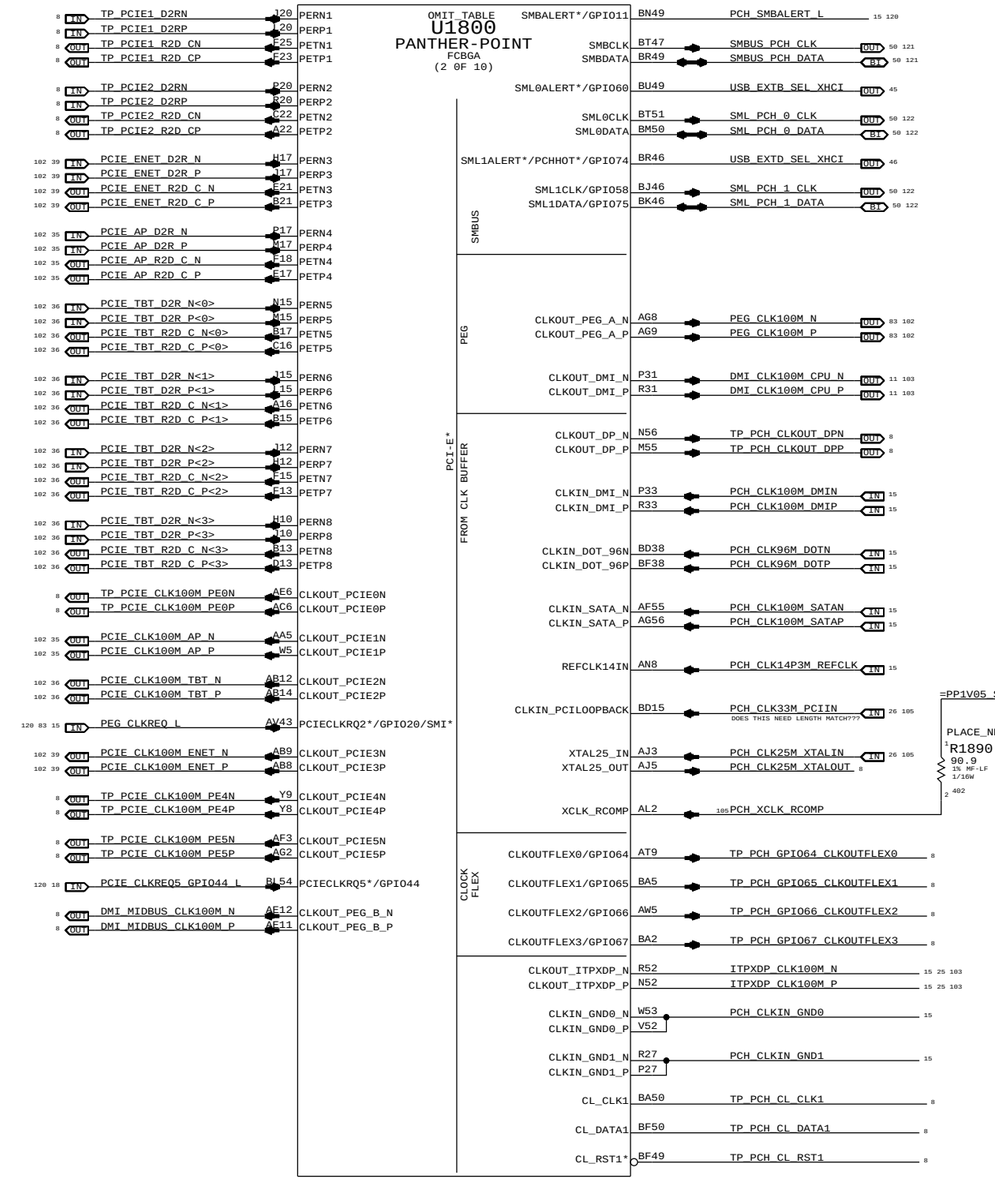

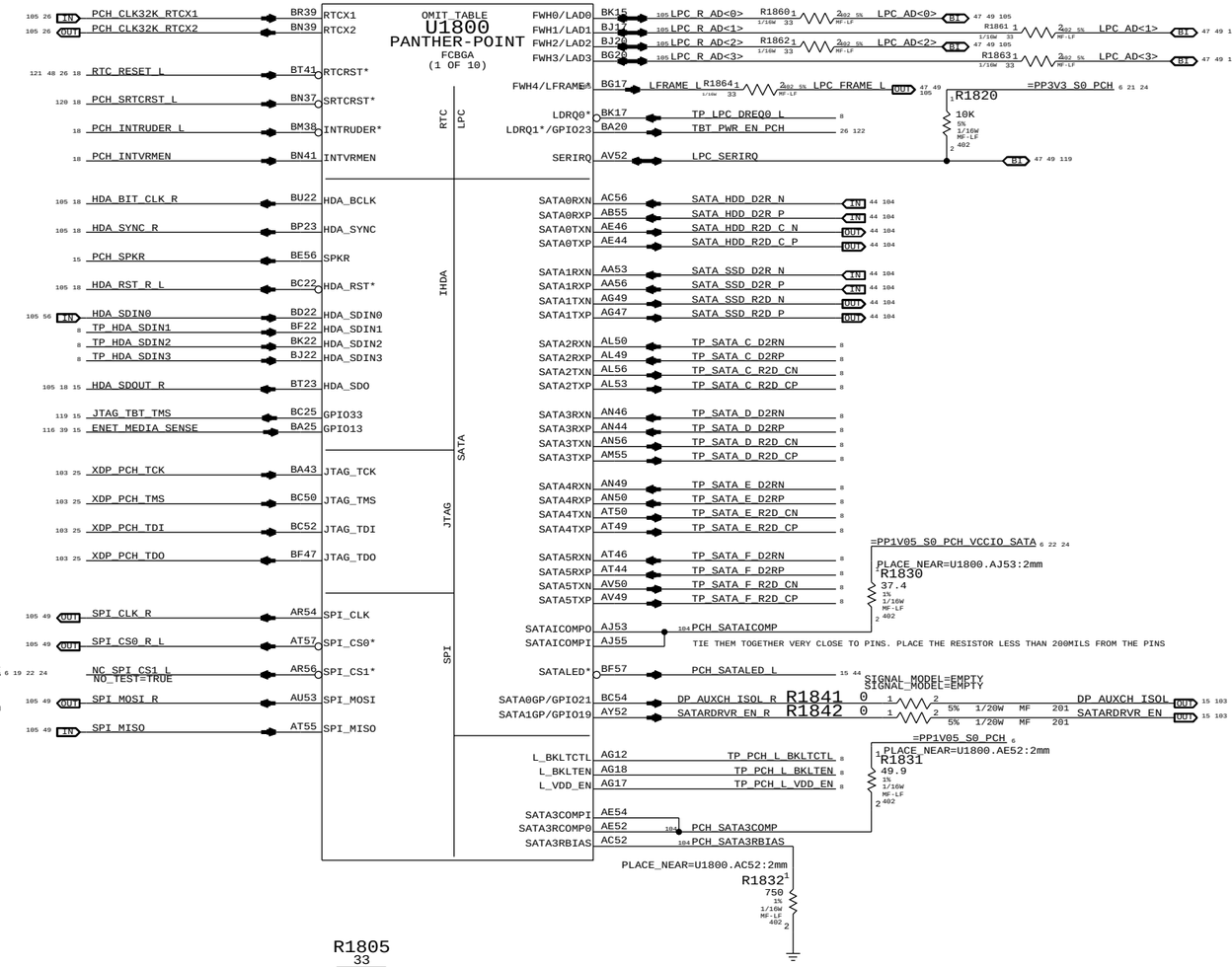

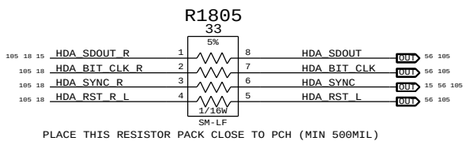

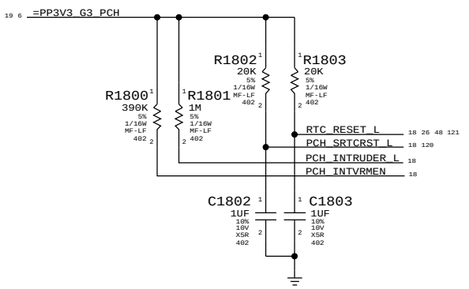

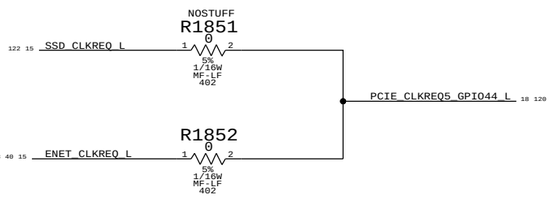

SYNC_MASTER=D8_MLB	SYNC_DATE=08/27/2012
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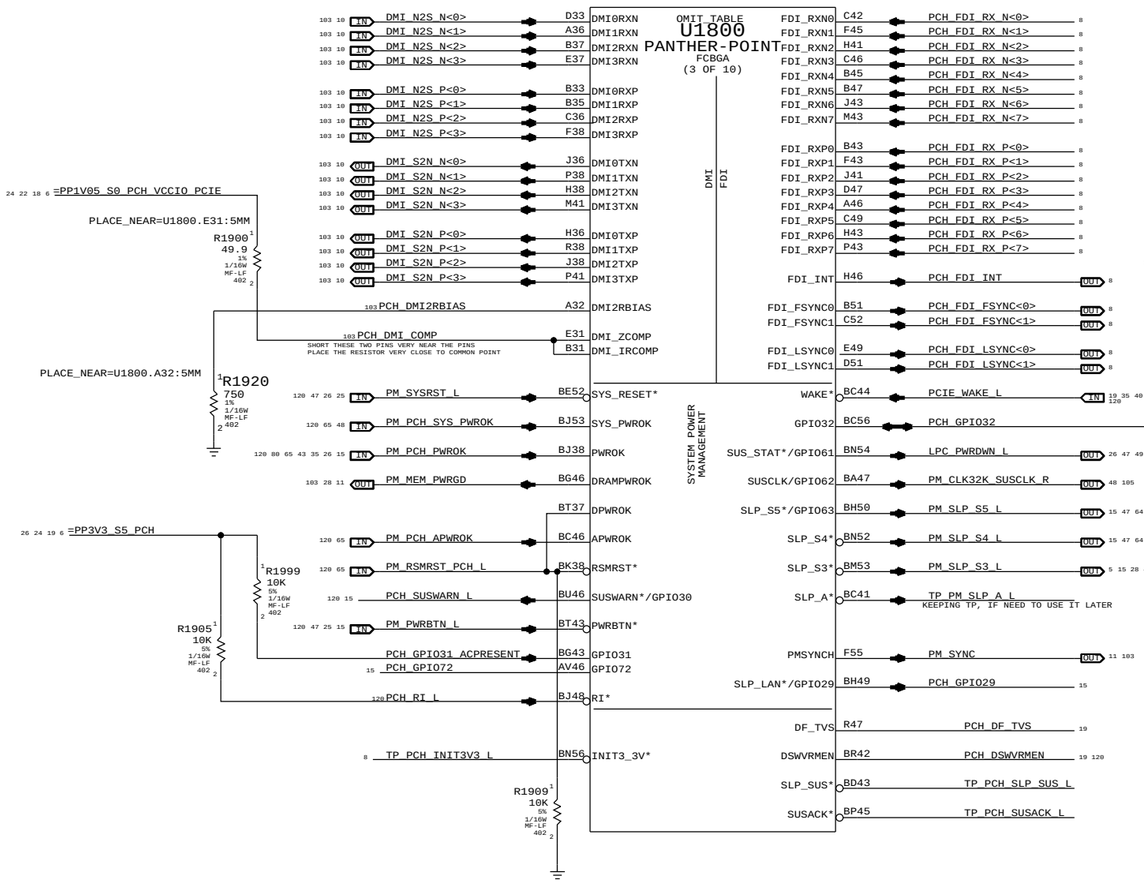

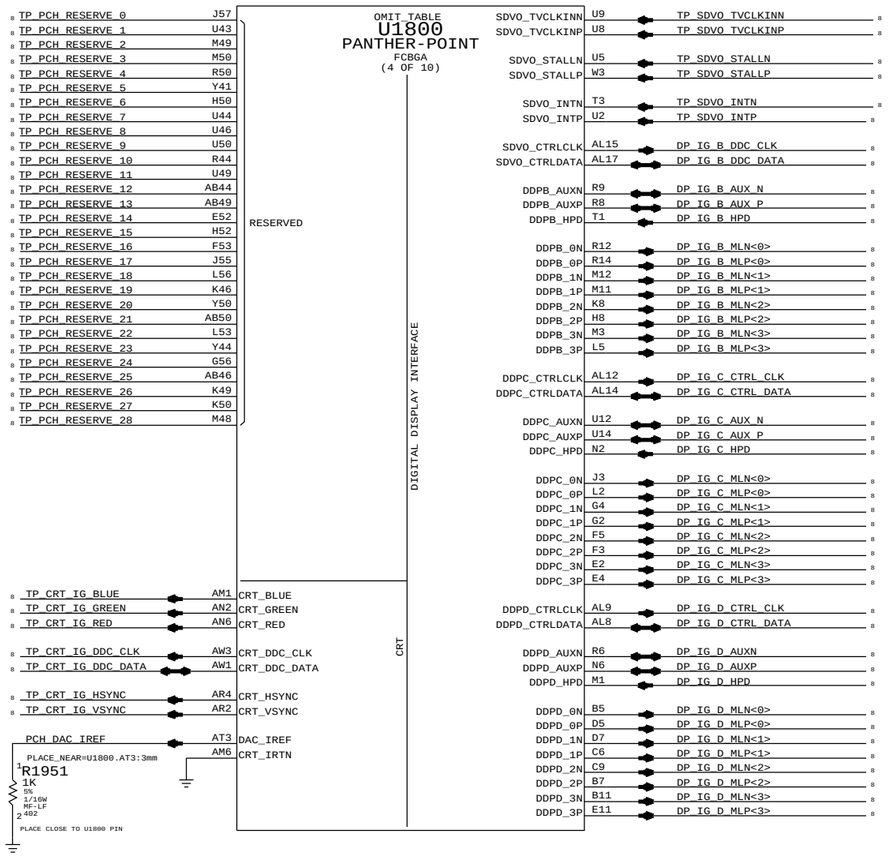

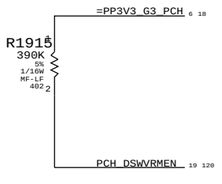

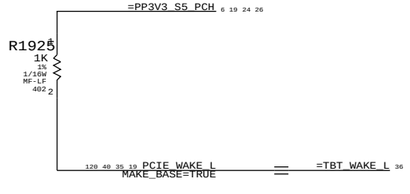

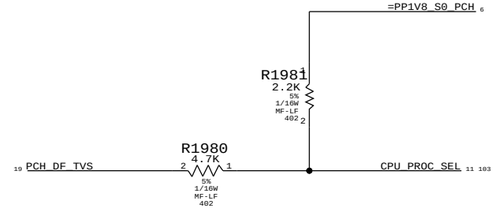

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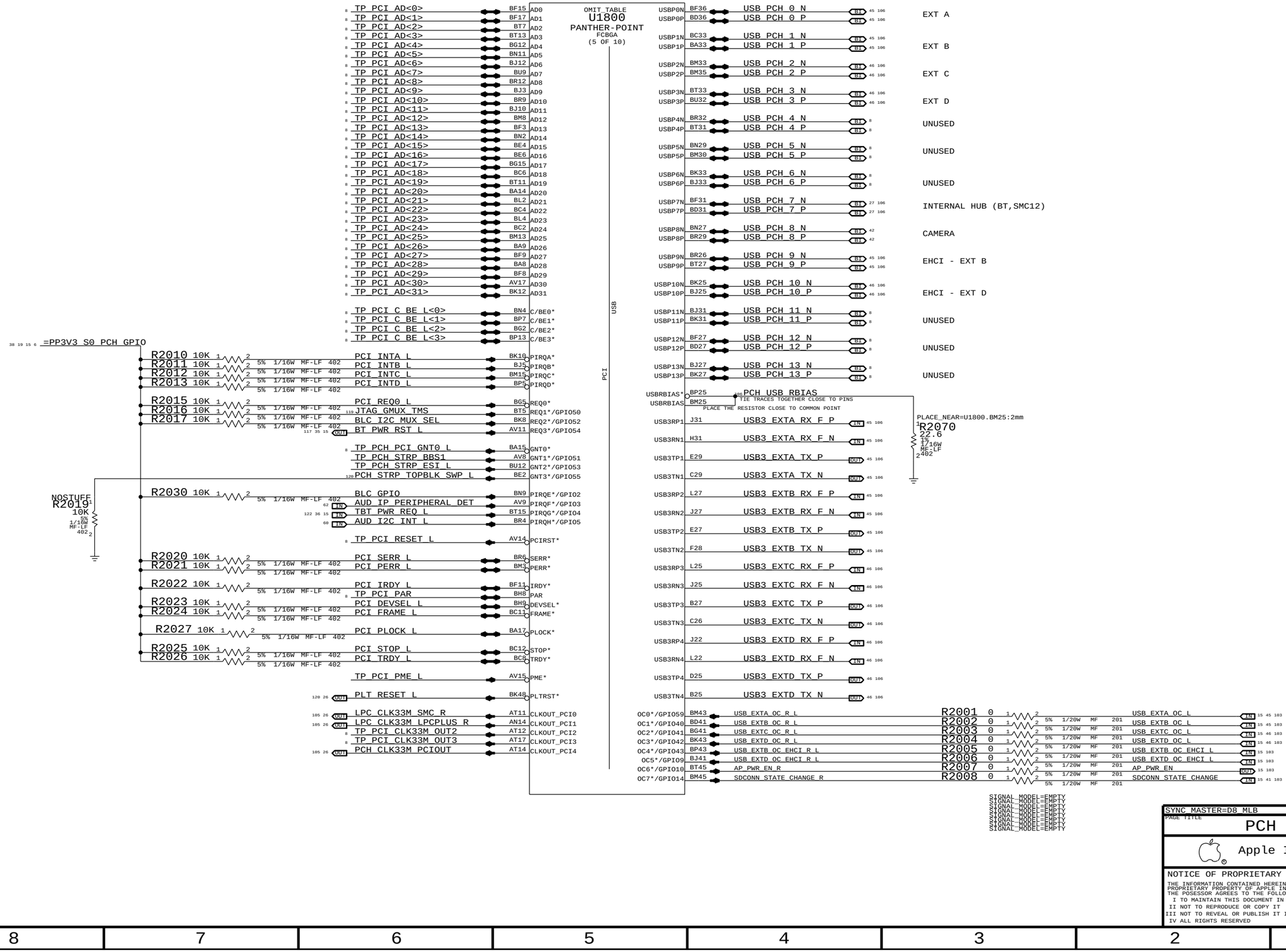

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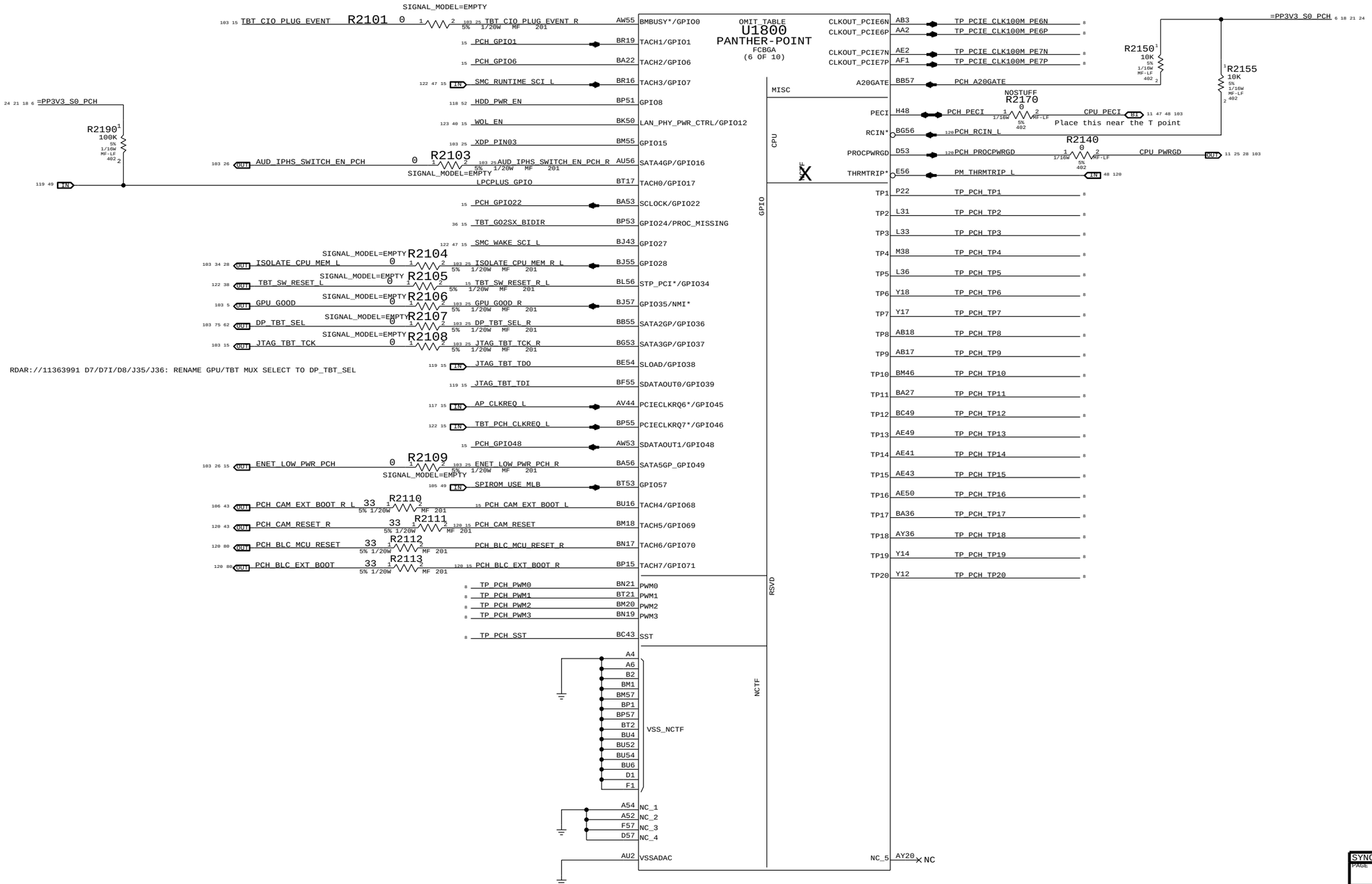

RDAR://11363991 D7/D7I/D8/J35/J36: RENAME GPU/TBT MUX SELECT TO DP_TBT_SEL

SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012

PAGE TITLE: PCH MISC

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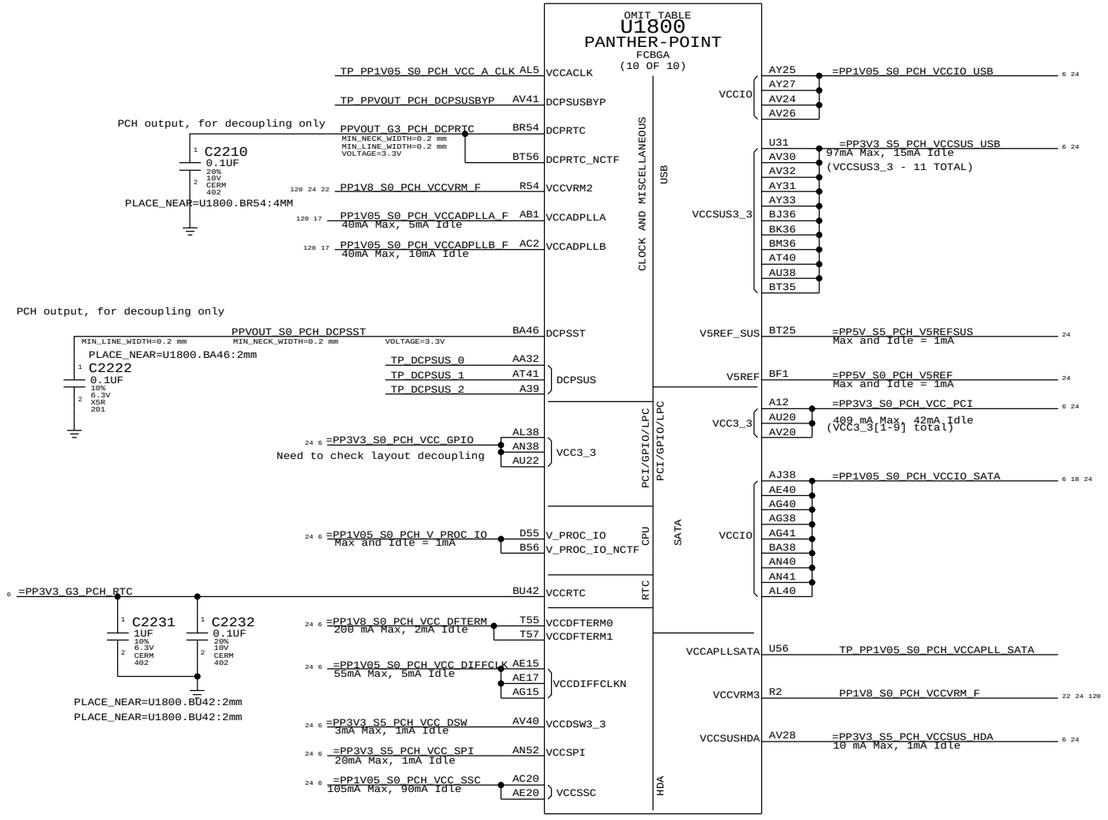

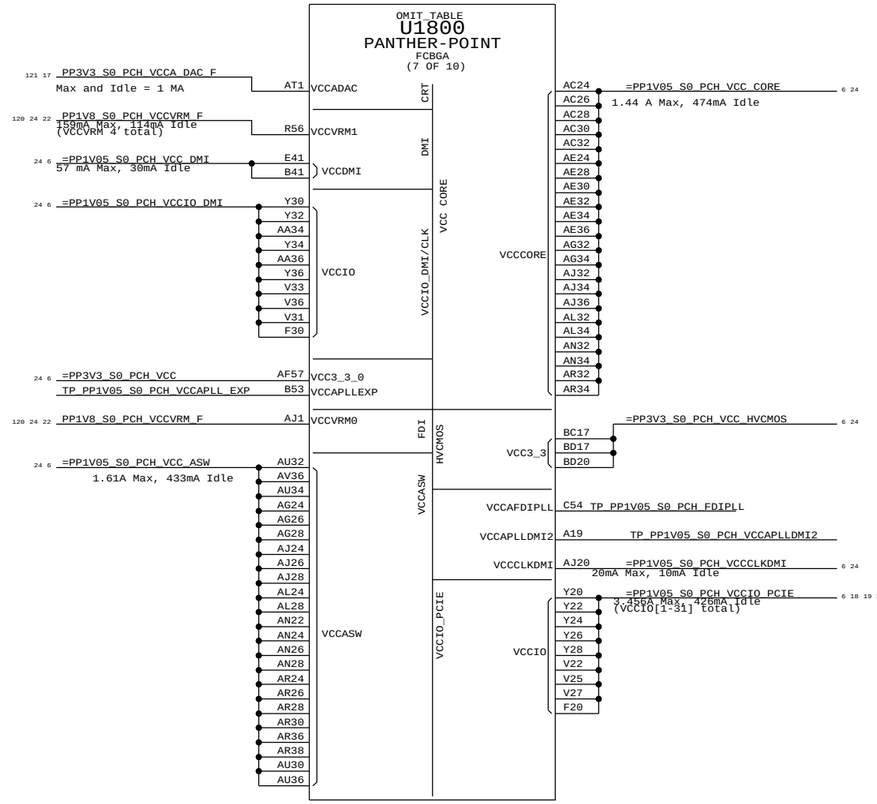

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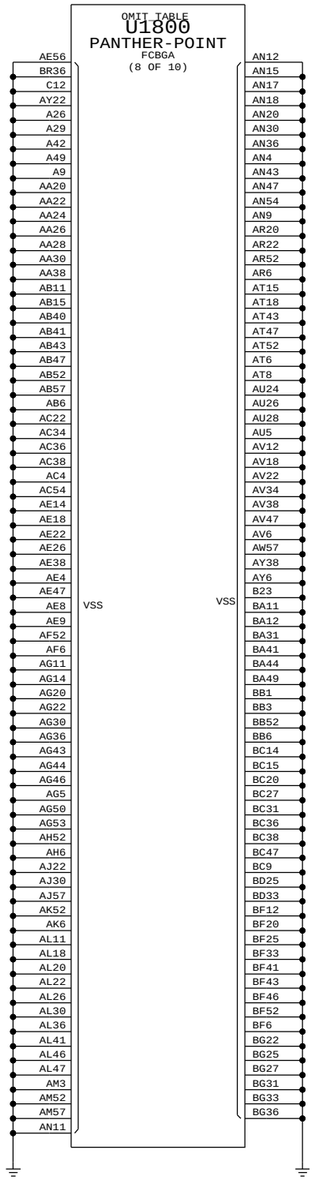

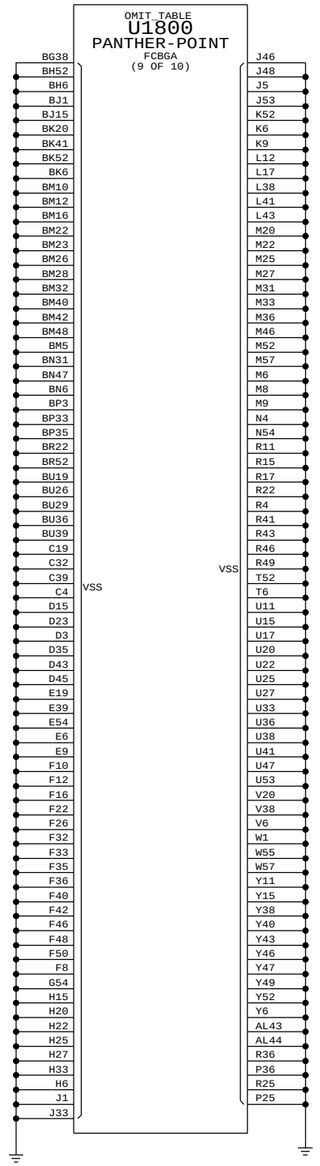

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=PP1V8_S0_PCH_VCC_VRM

R2400 0 5% 1/16W MF-LF 402
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=1.8V
MAKE_BASE=TRUE

=PP1V8_S0_PCH_VCCVRM_F

C2447 0.1UF 10% 16V X7R-CERM 0402
C2436 1UF 10% 6.3V CERM 402
C2443 1UF 10% 6.3V CERM 402
C2445 10UF 20% 6.3V CERM 805-1

PLACEMENT_NOTES:
PLACE C2436 AT BALL R54
PLACE C2443 AT BALL AJ1
PLACE C2445 AT BALL R2

PCH VCCSUS3_3 BYPASS
(PCH SUSPEND USB 3.3V PWR)

=PP3V3_S5_PCH_VCCSUS_USB

C2484 0.1UF 10% 16V X7R-CERM 0402
C2455 2.2UF 10% 6.3V X5R 402
C2413 0.1UF 10% 16V X7R-CERM 0402
C2412 2.2UF 10% 6.3V X5R 402
C2490 0.1UF 10% 16V X7R-CERM 0402

PLACEMENT_NOTES:
PLACE C2412 AT BALL AV30
PLACE C2412 AT BALL AT40

INTEL PDG: 2X 0.1UF AND 1X 2.2UF

=PP1V8_S0_PCH_VCC_DFTERM

C2440 0.1UF 20% 10V CERM 402

PLACEMENT_NOTE:
PLACE C2440 AT BALL T55
INTEL PDG: 1X 0.1UF

PCH VCCSUSHDA BYPASS
(PCH HD Audio 3.3V/1.5V PWR)

=PP3V3_S5_PCH_VCCSUS_HDA

C2441 0.1UF 20% 10V CERM 402

PLACEMENT_NOTE:
PLACE C2441 AT BALL AV28
INTEL PDG: 1X 0.1UF

=PP1V05_S0_PCH_VCCIO_SATA

C2444 1UF 10% 6.3V CERM 402
C2452 1UF 10% 6.3V CERM 402
C2453 1UF 10% 6.3V CERM 402

PLACEMENT_NOTES:
PLACE C2452 AT BALL AG38
PLACE C2453 AT BALL AJ38
PLACE C2444 AT BALL BA38
INTEL PDG: 2X 1UF

=PP1V05_S0_PCH_VCC_SSC

C2475 1UF 10% 6.3V CERM 402
C2480 10UF 20% 6.3V CERM 805-1

PLACEMENT_NOTES:
PLACE C2475 AT BALL AE20
PLACE C2480 AT BALL AC20

=PP1V05_S0_PCH_V_PROC_IO

C2416 4.7UF 20% 6.3V X5R 402
C2417 0.1UF 10% 16V X7R-CERM 0402
C2430 0.1UF 10% 16V X7R-CERM 0402

PLACEMENT_NOTES (all 3):
PLACE C2416 AT BALL D55

INTEL PDG: 2X 0.1UF AND 1X 4.7UF

=PP3V3_S5_PCH_VCC_SPI

C2442 1UF 10% 6.3V CERM 402

PLACEMENT_NOTE:
PLACE C2442 AT BALL AN52
INTEL PDG: 1X 1UF

=PP1V05_S0_PCH_VCC_DIFFCLK

C2434 1UF 10% 6.3V CERM 402
C2435 1UF 10% 6.3V CERM 402
C2437 10UF 20% 6.3V CERM 805-1

PLACEMENT_NOTES:
PLACE C2434 AT BALL AE15
PLACE C2435 AT BALL AE17
PLACE C2437 AT BALL AE15

FOR PCH_VCC_DIFFCLK AND PCH_VCC_CORE
INTEL PDG: 4X 1UF AND 2X 10UF

PCH VCCIO BYPASS
(PCH DMI 1.05V PWR)

=PP1V05_S0_PCH_VCC_DMI

PLACEMENT_NOTE:
PLACE C2419 AT BALL B41
PLACE C2487 AT BALL E41

C2419 1UF 10% 6.3V CERM 402
C2487 1UF 10% 6.3V CERM 402

PCH VCC3_3 BYPASS
(PCH PCI 3.3V PWR)

=PP3V3_S5_PCH_VCC_DSW

C2499 0.1UF 20% 10V CERM 402

PLACEMENT_NOTE:
PLACE C2499 AT BALL AV40
INTEL PDG: 1X 0.1UF

PCH VCCCORE BYPASS
(PCH 1.05V CORE PWR)

=PP1V05_S0_PCH_VCC_CORE

C2481 1UF 10% 6.3V CERM 402
C2482 1UF 10% 6.3V CERM 402
C2483 1UF 10% 6.3V CERM 402
C2460 10UF 20% 6.3V CERM 805-1
C2461 10UF 20% 6.3V CERM 805-1

PLACEMENT_NOTES:
PLACE C2482 AT BALL AC24
PLACE C2481 AT BALL AB32
PLACE C2483 AT BALL AC32
PLACE C2460 AT BALL AJ34
PLACE C2483 AT BALL AL34

=PP3V3_S0_PCH_VCC

C2423 0.1UF 10% 16V X7R-CERM 0402

PLACEMENT_NOTES:

=PP1V05_S0_PCH_VCCIO_PCIE

C2429 1UF 10% 6.3V CERM 402
C2414 1UF 10% 6.3V CERM 402
C2407 1UF 10% 6.3V CERM 402
C2463 1UF 10% 6.3V CERM 402
C2401 10UF 20% 6.3V CERM 805
C2410 10UF 20% 6.3V CERM 805-1
C2415 10UF 20% 6.3V CERM 805-1

PLACEMENT_NOTES:
PLACE C2410 AT BALL Y20
PLACE C2415 AT BALL F20
PLACE C2429 AT BALL Y24
PLACE C2414 AT BALL Y26
PLACE C2407 AT BALL Y28
PLACE C2401 AT BALL V22
PLACE C2463 AT BALL V25

=PP1V05_S0_PCH_VCCCLKDMI

C2411 1UF 10% 16V XSR 402

PLACE C2411 AT BALL AJ20

=PP3V3_S0_PCH_VCC_GPIO

C2486 0.1UF 10% 25V X5R 402
C2485 0.1UF 10% 25V X5R 402

PLACEMENT_NOTE:
PLACE C2485 AT BALL AL38
PLACE C2486 AT BALL AD22

PCH VCCIO BYPASS
(PCH USB 1.05V PWR)

=PP1V05_S0_PCH_VCCIO_USB

C2446 1UF 10% 6.3V CERM 402
C2449 1UF 10% 6.3V CERM 402
C2450 1UF 10% 6.3V CERM 402

PLACEMENT_NOTES:
PLACE C2446 AT BALL AV25
PLACE C2449 AT BALL AV27
PLACE C2450 AT BALL AV26

=PP3V3_S0_PCH
=PP5V_S0_PCH
1 mA

PCH V5REF Filter & Follower
(PCH Reference for 5V Tolerance on PCI)

R2405 100 5% 1/16W MF-LF 402
NC
D2400 BAT54DW-X-G SOT-363
PP5V_S0_PCH_V5REF
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=5V
MAKE_BASE=TRUE
<1 MA
=PP5V_S0_PCH_V5REF

C2439 1UF 10% 16V XSR 402

PLACEMENT_NOTE:
PLACE C2439 AT BALL BF1

=PP3V3_S0_PCH_VCC_PCI

C2421 0.1UF 10% 16V X7R-CERM 0402
C2422 1UF 10% 6.3V CERM 402

PLACEMENT_NOTES:
PLACE C2422 AT BALL AU20

=PP1V05_S0_PCH_VCC_ASW

C2426 1UF 10% 6.3V CERM 402
C2456 1UF 10% 6.3V CERM 402
C2496 1UF 10% 6.3V CERM 402
C2498 1UF 10% 6.3V CERM 402
C2418 10UF 20% 6.3V CERM 805-1
C2420 10UF 20% 6.3V CERM 805-1
C2428 10UF 20% 6.3V CERM 805-1

PLACEMENT_NOTES:
PLACE C2420 AT BALL AU32
PLACE C2428 AT BALL AJ24
PLACE C2426 AT BALL AU30
PLACE C2456 AT BALL AR28
PLACE C2496 AT BALL AR26
PLACE C2498 AT BALL AR22
PLACE C2418 AT BALL AN22
PLACE C2498 AT BALL AR24

=PP1V05_S0_PCH_VCCIO_DMI

C2470 1UF 10% 6.3V CERM 402
C2469 1UF 10% 6.3V CERM 402
C2473 10UF 20% 6.3V CERM 805-1
C2472 10UF 20% 6.3V CERM 805-1
C2471 10UF 20% 6.3V CERM 805-1

PLACEMENT_NOTES:
PLACE C2469 AT BALL V36
PLACE C2474 AT BALL AA34
PLACE C2470 AT BALL Y32
PLACE C2472 AT BALL Y34
PLACE C2473 AT BALL F30

=PP3V3_S5_PCH
=PP5V_S5_PCH
1 mA S0-S5

PCH V5REF_SUS Filter & Follower
(PCH Reference for 5V Tolerance on USB)

R2404 10 5% 1/16W MF-LF 402
NC
D2400 BAT54DW-X-G SOT-363
PP5V_S5_PCH_V5REFSUS
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=5V
MAKE_BASE=TRUE
<1 MA S0-S5
=PP5V_S5_PCH_V5REFSUS

C2438 0.1UF 20% 10V CERM 402

PLACEMENT_NOTE:
PLACE C2438 AT BALL BT25

=PP3V3_S0_PCH_VCC_HVCMOS

C2424 0.1UF 10% 16V X7R-CERM 0402
C2425 1UF 10% 6.3V CERM 402
C2427 1UF 10% 6.3V CERM 402

PLACEMENT_NOTES:
PLACE C2425 AT BALL BD20
PLACE C2427 AT BALL BD17

SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012

PAGE TITLE
PCH DECOUPLING

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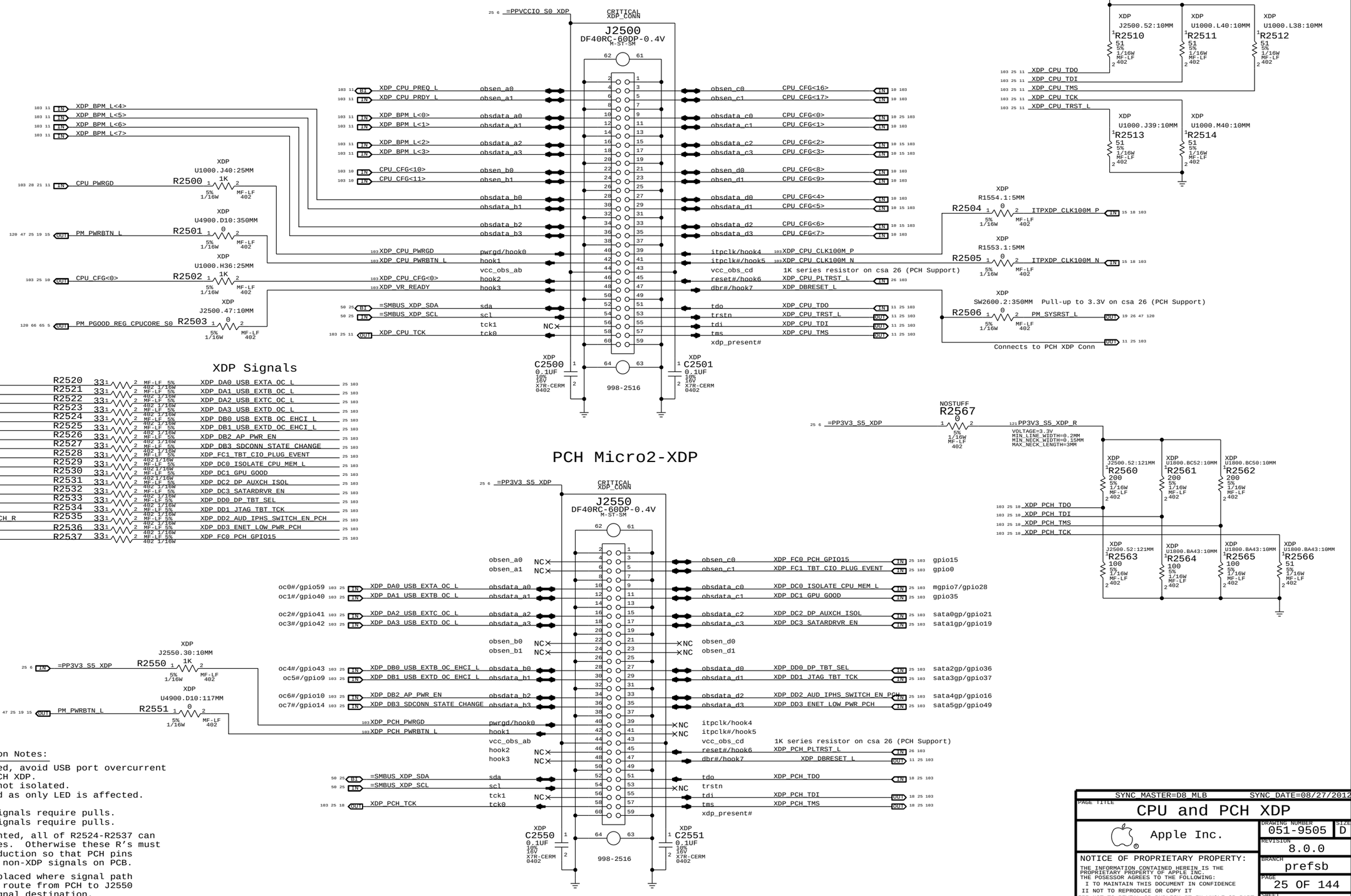
CPU Micro2-XDP



PCH Signals

USB_EXTA_OC_R_L	R2520	33	XDP_DA0_USB_EXTA_OC_L
USB_EXTB_OC_R_L	R2521	33	XDP_DA1_USB_EXTB_OC_L
USB_EXTC_OC_R_L	R2522	33	XDP_DA2_USB_EXTC_OC_L
USB_EXTD_OC_R_L	R2523	33	XDP_DA3_USB_EXTD_OC_L
USB_EXTB_OC_EHCI_R_L	R2524	33	XDP_DB0_USB_EXTB_OC_EHCI_L
USB_EXTD_OC_EHCI_R_L	R2525	33	XDP_DB1_USB_EXTD_OC_EHCI_L
AP_PWR_EN_R	R2526	33	XDP_DB2_AP_PWR_EN
SDCONN_STATE_CHANGE_R	R2527	33	XDP_DB3_SDCONN_STATE_CHANGE
TBT_CIO_PLUG_EVENT_R	R2528	33	XDP_FC1_TBT_CIO_PLUG_EVENT
ISOLATE_CPU_MEM_R_L	R2529	33	XDP_DC0_ISOLATE_CPU_MEM_L
GPU_GOOD_R	R2530	33	XDP_DC1_GPU_GOOD
DP_AUXCH_ISOL_R	R2531	33	XDP_DC2_DP_AUXCH_ISOL
SATARDRVR_EN_R	R2532	33	XDP_DC3_SATARDRVR_EN
DP_TBT_SEL_R	R2533	33	XDP_DD0_DP_TBT_SEL
JTAG_TBT_TCK_R	R2534	33	XDP_DD1_JTAG_TBT_TCK
AUD_IPHS_SWITCH_EN_PCH_R	R2535	33	XDP_DD2_AUD_IPHS_SWITCH_EN_PCH
ENET_LOW_PWR_PCH_R	R2536	33	XDP_DD3_ENET_LOW_PWR_PCH
XDP_PIN03	R2537	33	XDP_FC0_PCH_GPIO15

XDP Signals

PCH Micro2-XDP

PCH/XDP Signal Isolation Notes:

- USB OC#'s not isolated, avoid USB port overcurrent events while using PCH XDP.
- Unused GPIOs 0 & 15 not isolated.
- MXM_GOOD not isolated as only LED is affected.
- For isolated GPIOs:
  - 'Output' non-XDP signals require pulls.
  - 'Output' PCH/XDP signals require pulls.

If PCH XDP not implemented, all of R2524-R2537 can be replaced with aliases. Otherwise these R's must be stuffed even in production so that PCH pins connect to appropriate non-XDP signals on PCB.

R2524-R2537 should be placed where signal path needs to split between route from PCH to J2550 and path to non-XDP signal destination.

SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012

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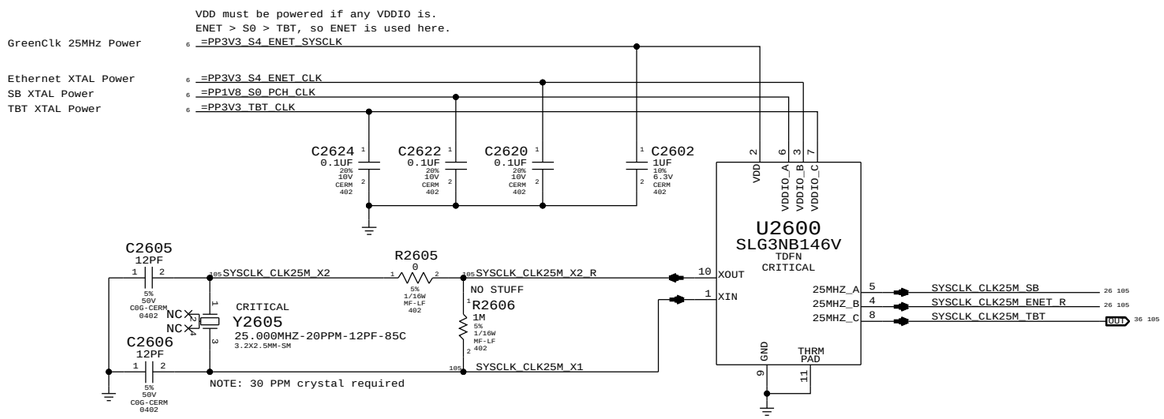
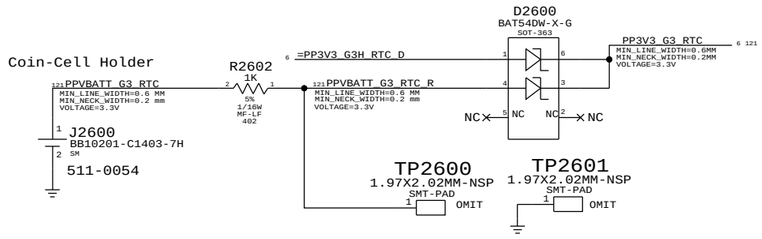
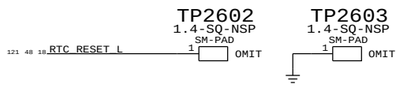
System 25MHz Clock Generator



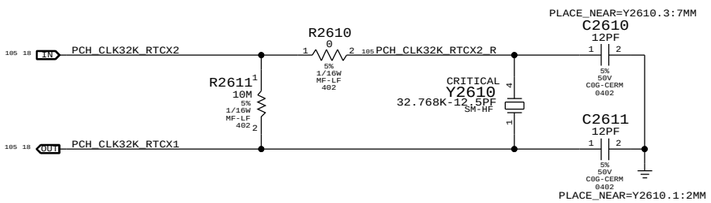
RTC Power Sources



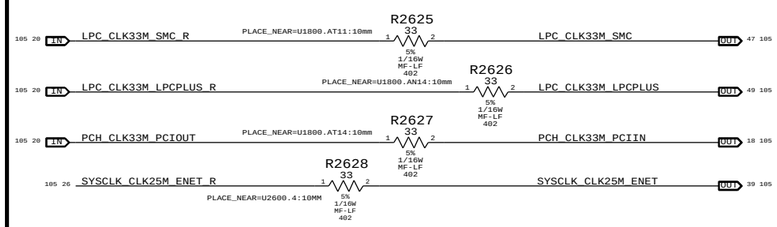
RDAR://11218892 TESTPOINT TO RESET RTC FOR APPLE CARE



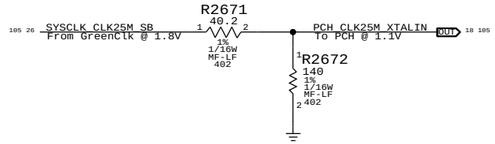
PCH RTC Crystal



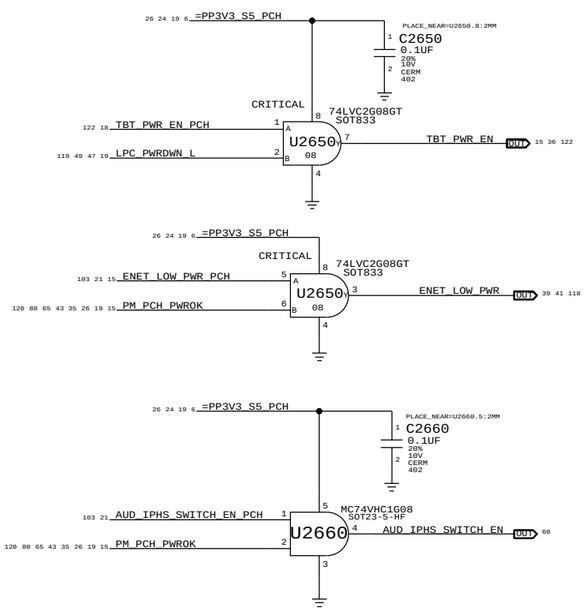
Clock series termination



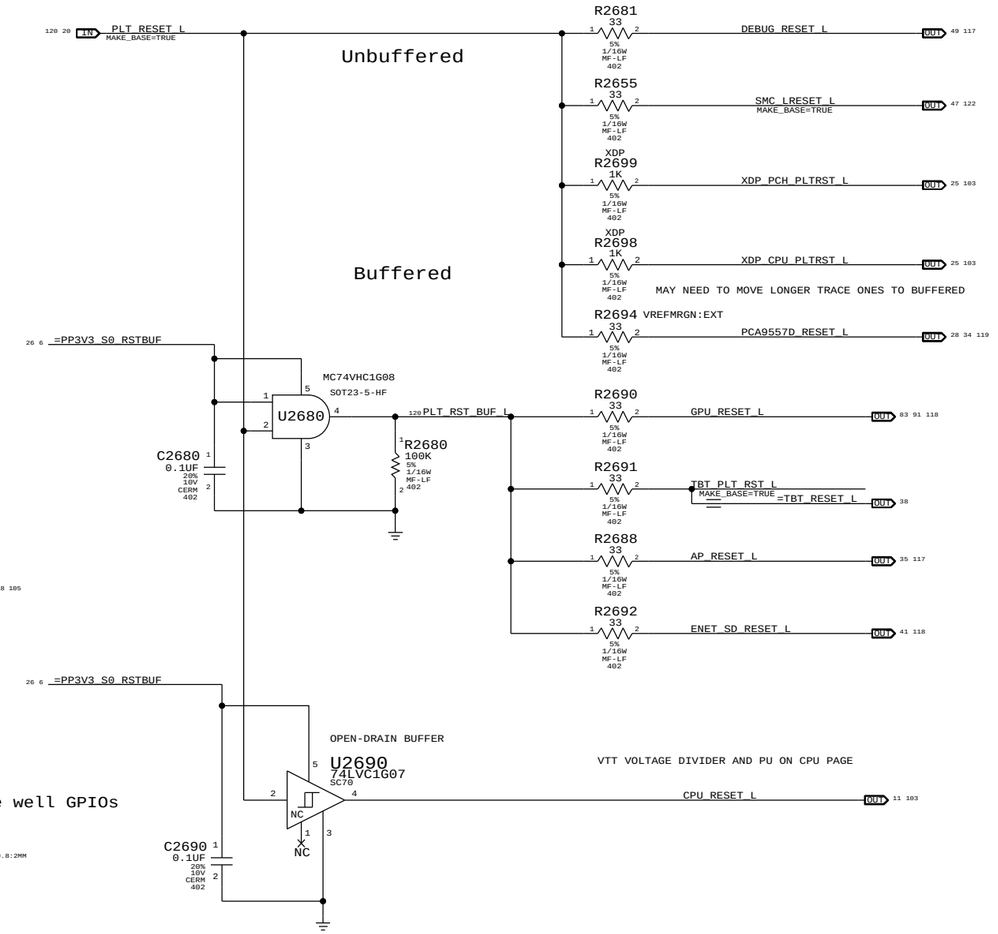
PCH 25MHZ CLOCK



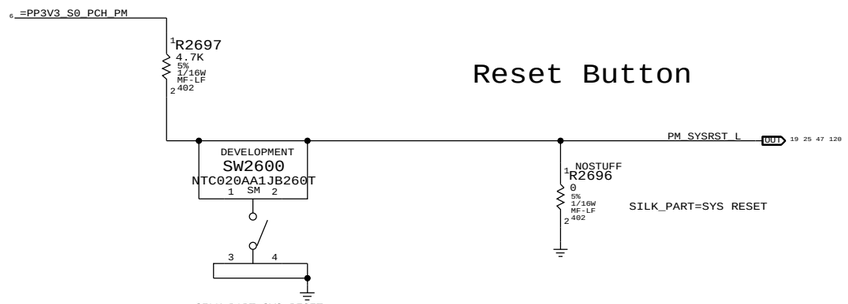
GPIO Isolation to prevent glitches on critical core well GPIOs



Platform Reset Connections



Reset Button



SYNC_MASTER=D8_MLB	SYNC_DATE=08/27/2012
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155S0220
L2700
FERR-120-OHM-1.5A
=PP3V3_S4_USB_HUB
50mV P-P spec @ 100k-1MHz
0402
PP3V3_S4_USB_HUB_VDD
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.25MM
MAX_NECK_LENGTH=3MM

C2708 1UF 10% 16V X5R 402
C2709 0.1UF 10% 16V X7R-CERM 0402
C2710 0.1UF 10% 16V X7R-CERM 0402
C2711 0.1UF 10% 16V X7R-CERM 0402
C2707 0.1UF 10% 16V X7R-CERM 0402
C2705 4.7UF 10% 6.3V X5R-CERM 603
C2706 0.1UF 10% 16V X7R-CERM 0402

PP1V2_USB_HUB_CRFILT
VOLTAGE=1.2V
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
MAX_NECK_LENGTH=3MM
PP1V2_USB_HUB_PLLFILT
VOLTAGE=1.2V
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
MAX_NECK_LENGTH=3MM

C2703 0.1UF 10% 16V X7R-CERM 0402
C2704 0.1UF 10% 16V X7R-CERM 0402

NON_REM 0 and 1 are used to indicate whether the downstream ports are removable or captive
NON_REM[1:0] = 00 ---> ports 1 and 2 are removable
NON_REM[1:0] = 01 ---> port 1 is non-removable
NON_REM[1:0] = 1x ---> ports 1 and 2 are non-removable

=PP3V3_S4_USB_HUB
R2704 100K 5% 1/16W MF-LF 402
R2705 100K 5% 1/16W MF-LF 402

=PP3V3_S4_USB_HUB
R2703 10K 5% 1/16W MF-LF 402

U2700
USB2412-DZK
QFN
CRITICAL
338S1076

VDD33	4		
VDD33	10		
VDD33	14		
VDD33	20		
VDD33	27		
CRFILT	9		
PLLFILT	25		
VBUS_DET	18	USB_HUB_VBUS_DET	106
USBDP_UP	22	USB_PCH_7_P	106 20
USBDM_UP	21	USB_PCH_7_N	106 20
USBDP_DN1	1	USB_BT_P	106 35
USBDM_DN1	28	USB_BT_N	106 35
USBDP_DN2	3	USB_HUB_2P	106
USBDM_DN2	2	USB_HUB_2N	106
PRTPWR1	7	NC	
PRTPWR2	11	NC	
OCS1*	8	NC	
OCS2*	12	NC	
RBIAS	26	USB_HUB_RBIAS	106
SUSP_IND/NON_REM0	19	USB_HUB_NON_REM0	106
NON_REM1	13	USB_HUB_NON_REM1	106
HS_IND	16	USB_HUB_HS_IND	106
RESET*	17	USB_HUB_RESET_L	106
TEST	6		
XTALIN/CLKIN	24	USB_HUB_XTAL1	106
XTALOUT	23	USB_HUB_XTAL2	106
NC	5	NC	
TEST1	15		
EPAD	29		

ePad needs a minimum of 3x3 via array to GND

R2711 4.7K 5% 1/20W MF 201
R2710 4.7K 5% 1/20W MF 201
R2707 12K 1% 1/16W MF 402
PLACE_NEAR=U2700.26:2MM

R2708 100K 5% 1/16W MF-LF 402
C2712 0.01UF 10% 16V CERM 402
R2712 1K 5% 1/16W MF-LF 402
PM_PGOOD_P3V3_S4_FET
R2709 0 5% 1/16W MF-LF 402
R2706 1M 5% 1/16W MF-LF 402
C2701 18PF 5% 50V C0G-CERM 0402
CRITICAL
Y2700 24.000M-50PPM-16PF 5X3.2X1.5-SM
C2702 18PF 5% 50V C0G-CERM 0402
USB_HUB_XTAL2_R

SYNC_MASTER=D8_MLB	SYNC_DATE=08/27/2012
PAGE TITLE	USB 2.0 HUB (BT/SMC)
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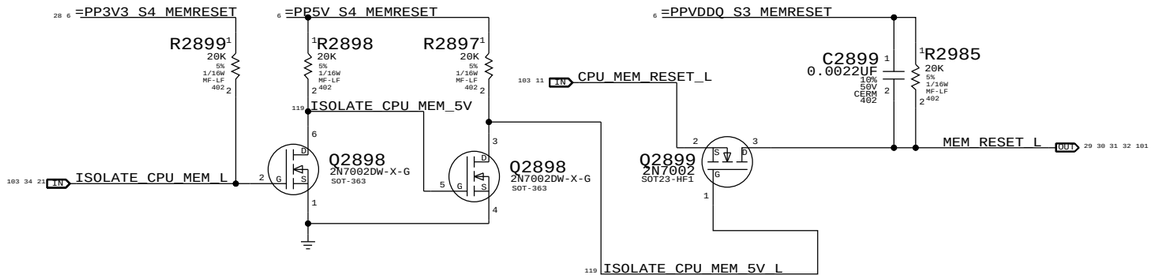
MEM_RESET_L Generator

The circuits below handle MEMVTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behaviour of signals.
WHEN HIGH: MEM_RESET_L NOT ISOLATED.
WHEN LOW: MEM_RESET_L IS ISOLATED.
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L (Block CPU from driving MEM_RESET_L in S3)

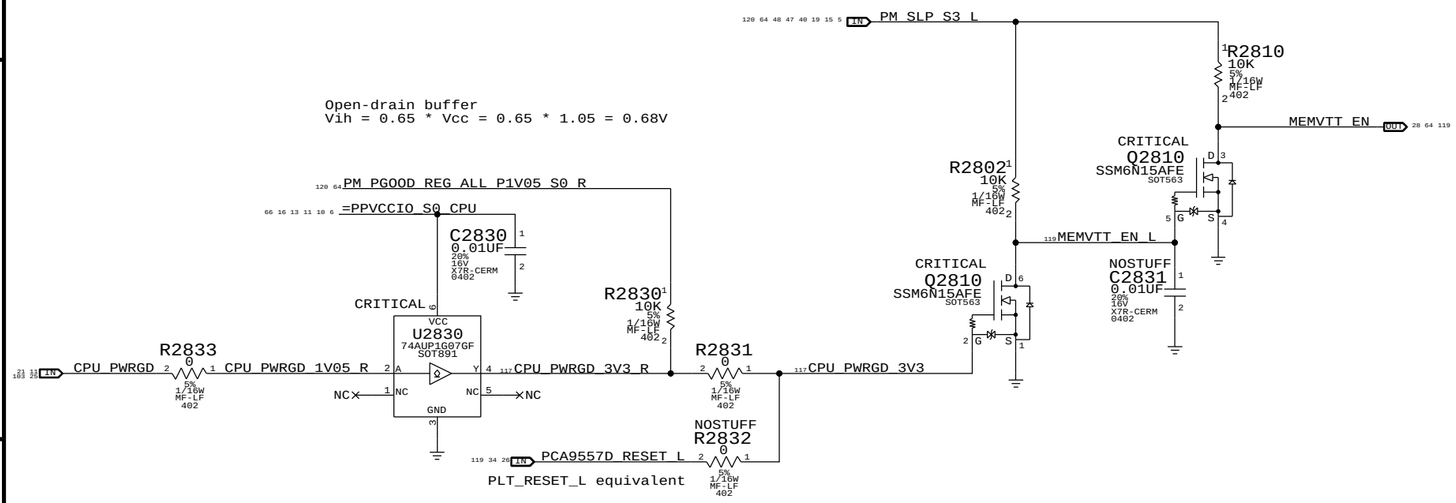


MEMVTT_EN Generator

rdar://11117167

Enables MEMVTT when PCH drives CPU PWRGD.

CPU does not drive MEM_CKE until VCCORE activated but CPU 1V5 (VDDQ) leaks into it.
Clamping MEMVTT will keep the MEM_CKE low until CPU actively controls it.
MEMVTT Clamp actively holds MEMVTT rail low until MEMVTT is enabled.
MEMVTT_EN = CPU_PWRGD * PM_SLP_S3_L (VTT is enabled when PCH tells CPU to enable VCCORE)



	Step	ISOLATE_CPU_MEM_L	PM_SLP_S3_L	CPU_PWRGD	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN
S0	0	1	1	1	CPU_MEM_RESET_L	1	1
to	1	0	1	1	1	1	1
S3	2	0	1	1	1	1	1
	3	0	0	0	X	1	0
	4	0	0	0	X	1	0
to	5	0	1	1	0 (*)	1	1
S0	6	0	1	1	1	1	1
	7	1	1	1	CPU_MEM_RESET_L	1	1

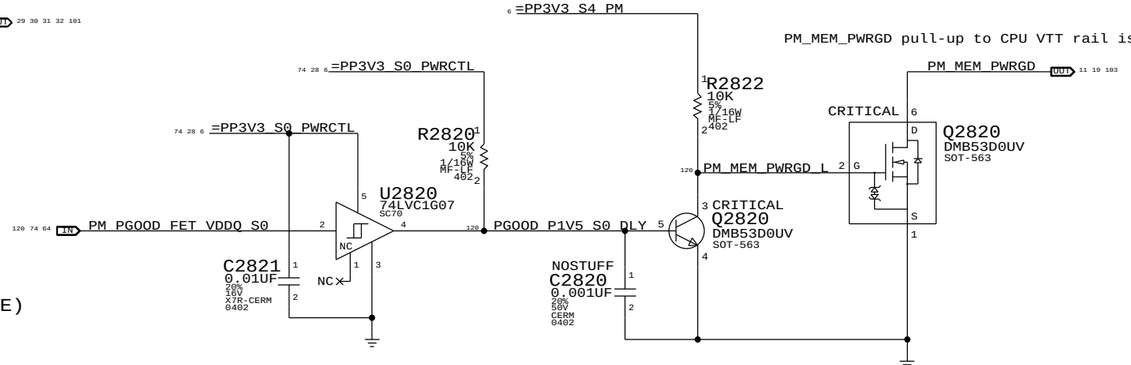
(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: On a S5->S0 transition, ISOLATE_CPU_MEM_L will default low.
Rails will power-up as if from S3, but MEM_RESET_L now needs to be asserted in S0. Software must de-assert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

1V5 S0 "PGOOD" for CPU

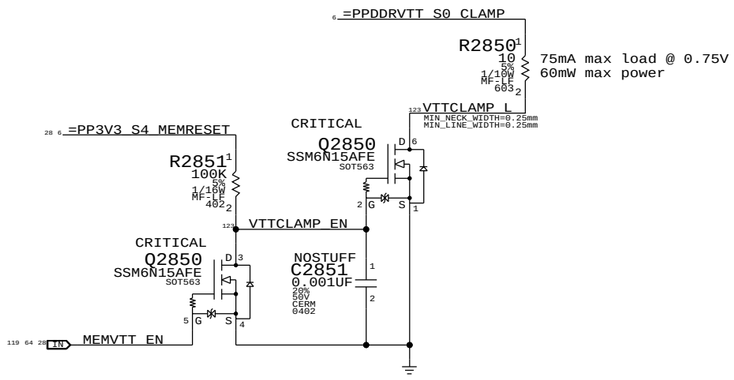
With optional delay from 1V5 S0 PGOOD

PM_MEM_PWRGD pull-up to CPU VTT rail is on CPU page



MEMVTT Clamp

Ensures CKE signals are held low in S3 and in S0 before CPU PWRGD



SYNC_MASTER=D8_MLB	SYNC_DATE=08/27/2012
PAGE TITLE	CPU Memory S3 Support
Apple Inc.	DRAWING NUMBER 051-9505 SIZE D
	REVISION 8.0.0
	BRANCH prefsb
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	SHEET 28 OF 123

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Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_A
- =PPVDDQ_S3_MEM_A
- =PPDDRVTT_S0_MEM_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

=PPDDRVREF_DQ_MEM_A

C2930 2.2UF 20% 6.3V CERM 402-LF
C2931 0.1UF 20% 10V CERM 402

DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

=PPVDDQ_S3_MEM_A

C2910 0.1UF 20% 10V CERM 402
C2911 0.1UF 20% 10V CERM 402
C2912 0.1UF 20% 10V CERM 402
C2913 0.1UF 20% 10V CERM 402
C2914 0.1UF 20% 10V CERM 402
C2915 0.1UF 20% 10V CERM 402
C2916 0.1UF 20% 10V CERM 402
C2917 0.1UF 20% 10V CERM 402

C2900 10UF 20% 6.3V X5R 603
C2901 10UF 20% 6.3V X5R 603
C2918 0.1UF 20% 10V CERM 402
C2919 0.1UF 20% 10V CERM 402
C2920 0.1UF 20% 10V CERM 402
C2921 0.1UF 20% 10V CERM 402
C2922 0.1UF 20% 10V CERM 402
C2923 0.1UF 20% 10V CERM 402

MEM_DIMM0_SA<1>
MEM_DIMM0_SA<0>
=PP3V3_S0_MEM_A_SPD

C2940 2.2UF 20% 6.3V CERM 402-LF
R2940 10K 5% 1/16W MF-LF 402
R2941 10K 5% 1/16W MF-LF 402

=PPDDRVTT_S0_MEM_A

J2900 F-ANG-SM-2 SODIMM-P0.60-D8 SYM 1 OF 2

1	VREFDQ	VSS_0	2
3	VSS_1	DQ4	4
5	DQ0	DQ5	6
7	DQ1	VSS_2	8
9	VSS_3	DQS0*	10
11	DM0	DQS0	12
13	VSS_4	VSS_5	14
15	DQ2	DQ6	16
17	DQ3	DQ7	18
19	VSS_6	VSS_7	20
21	DQ8	DQ12	22
23	DQ9	DQ13	24
25	VSS_8	VSS_9	26
27	DQS1*	DM1	28
29	DQS1	RESET*	30
31	VSS_10	VSS_11	32
33	DQ10	DQ14	34
35	DQ11	DQ15	36
37	VSS_12	VSS_13	38
39	DQ16	DQ20	40
41	DQ17	DQ21	42
43	VSS_14	VSS_15	44
45	DQS2*	DM2	46
47	DQS2	VSS_16	48
49	VSS_17	DQ22	50
51	DQ18	DQ23	52
53	DQ19	VSS_18	54
55	VSS_19	DQ28	56
57	DQ24	DQ29	58
59	DQ25	VSS_20	60
61	VSS_21	DQS3*	62
63	DM3	DQS3	64
65	VSS_22	VSS_23	66
67	DQ26	DQ30	68
69	DQ27	DQ31	70
71	VSS_24	VSS_25	72
KEY			
73	CKE0	CKE1	74
75	VDD_0	VDD_1	76
77	NC_0	A15	78
79	BA2	A14	80
81	VDD_2	VDD_3	82
83	A12/BC*	A11	84
85	A9	A7	86
87	VDD_4	VDD_5	88
89	A8	A6	90
91	A5	A4	92
93	VDD_6	VDD_7	94
95	A3	A2	96
97	A1	A0	98
99	VDD_8	VDD_9	100
101	CK0	CK1	102
103	CK0*	CK1*	104
105	VDD_10	VDD_11	106
107	A10_AP	BA1	108
109	BA0	RAS*	110
111	VDD_12	VDD_13	112
113	WE*	S0*	114
115	CAS*	ODT0	116
117	VDD_14	VDD_15	118
119	A13	ODT1	120
121	S1*	NC_1	122
123	VDD_16	VDD_17	124
125	TEST	VREFCA	126
127	VSS_26	VSS_27	128
129	DQ32	DQ36	130
131	DQ33	DQ37	132
133	VSS_28	VSS_29	134
135	DQS4*	DM4	136
137	DQS4	VSS_30	138
139	VSS_31	DQ38	140
141	DQ34	DQ39	142
143	DQ35	VSS_32	144
145	VSS_33	DQ44	146
147	DQ40	DQ45	148
149	DQ41	VSS_34	150
151	VSS_35	DQS5*	152
153	DM5	DQS5	154
155	VSS_36	VSS_37	156
157	DQ42	DQ46	158
159	DQ43	DQ47	160
161	VSS_38	VSS_39	162
163	DQ48	DQ52	164
165	DQ49	DQ53	166
167	VSS_40	VSS_41	168
169	DQS6*	DM6	170
171	DQS6	VSS_42	172
173	VSS_43	DQ54	174
175	DQ50	DQ55	176
177	DQ51	VSS_44	178
179	VSS_45	DQ60	180
181	DQ56	DQ61	182
183	DQ57	VSS_46	184
185	VSS_47	DQS7*	186
187	DM7	DQS7	188
189	VSS_48	VSS_49	190
191	DQ58	DQ62	192
193	DQ59	DQ63	194
195	VSS_50	VSS_51	196
197	SA0	EVENT*	198
199	VDDSPD	SDA	200
201	SA1	SCL	202
203	VTT_0	VTT_1	204

J2900 SODIMM-P0.60-D8 F-ANG-SM-2 SYM 2 OF 2

205	MTG HOLE
206	
207	
208	
209	

P/N: 516S1030

=PPDDRVREF_CA_MEM_A

C2935 2.2UF 20% 6.3V CERM 402-LF
C2936 0.1UF 20% 10V CERM 402

=PPDDRVTT_S0_MEM_A

C2950 1UF 10% 10V X5R 402
C2951 1UF 10% 10V X5R 402
C2952 1UF 10% 10V X5R 402
C2953 1UF 10% 10V X5R 402

SYNC_MASTER=D8_MLB	SYNC_DATE=08/27/2012
PAGE TITLE	DDR3 SO-DIMM Connector A Slot0
Apple Inc.	DRAWING NUMBER 051-9505 SIZE D
	REVISION 8.0.0
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Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_A
- =PPVDDQ_S3_MEM_A
- =PPDDRVTT_S0_MEM_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

=PPDDRVREF_DQ_MEM_A

C3030 2.2UF 20% 6.3V CERM 402-LF
C3031 0.1UF 20% 10V CERM 402

P/N: 516S1030

J3000
SODIMM-P0.60-D8
F-ANG-SM-2
SYM 2 OF 2
MTG HOLE

J3000
SODIMM-P0.60-D8
F-ANG-SM-2
SYM 1 OF 2

1	VREFDQ	VSS_0	2
3	VSS_1	DQ4	4
5	DQ0	DQ5	6
7	DQ1	VSS_2	8
9	VSS_3	DQS0*	10
11	DM0	DQS0	12
13	VSS_4	VSS_5	14
15	DQ2	DQ6	16
17	DQ3	DQ7	18
19	VSS_6	VSS_7	20
21	DQ8	DQ12	22
23	DQ9	DQ13	24
25	VSS_8	VSS_9	26
27	DQS1*	DM1	28
29	DQS1	RESET*	30
31	VSS_10	VSS_11	32
33	DQ10	DQ14	34
35	DQ11	DQ15	36
37	VSS_12	VSS_13	38
39	DQ16	DQ20	40
41	DQ17	DQ21	42
43	VSS_14	VSS_15	44
45	DQS2*	DM2	46
47	DQS2	VSS_16	48
49	VSS_17	DQ22	50
51	DQ18	DQ23	52
53	DQ19	VSS_18	54
55	VSS_19	DQ28	56
57	DQ24	DQ29	58
59	DQ25	VSS_20	60
61	VSS_21	DQS3*	62
63	DM3	DQS3	64
65	VSS_22	VSS_23	66
67	DQ26	DQ30	68
69	DQ27	DQ31	70
71	VSS_24	VSS_25	72
	KEY		
73	CKE0	CKE1	74
75	VDD_0	VDD_1	76
77	NC_0	A15	78
79	BA2	A14	80
81	VDD_2	VDD_3	82
83	A12/BC*	A11	84
85	A9	A7	86
87	VDD_4	VDD_5	88
89	A8	A6	90
91	A5	A4	92
93	VDD_6	VDD_7	94
95	A3	A2	96
97	A1	A0	98
99	VDD_8	VDD_9	100
101	CK0	CK1	102
103	CK0*	CK1*	104
105	VDD_10	VDD_11	106
107	A10_AP	BA1	108
109	BA0	RAS*	110
111	VDD_12	VDD_13	112
113	WE*	S0*	114
115	CAS*	ODT0	116
117	VDD_14	VDD_15	118
119	A13	ODT1	120
121	S1*	NC_1	122
123	VDD_16	VDD_17	124
125	TEST	VREFCA	126
127	VSS_26	VSS_27	128
129	DQ32	DQ36	130
131	DQ33	DQ37	132
133	VSS_28	VSS_29	134
135	DQS4*	DM4	136
137	DQS4	VSS_30	138
139	VSS_31	DQ38	140
141	DQ34	DQ39	142
143	DQ35	VSS_32	144
145	VSS_33	DQ44	146
147	DQ40	DQ45	148
149	DQ41	VSS_34	150
151	VSS_35	DQS5*	152
153	DM5	DQS5	154
155	VSS_36	VSS_37	156
157	DQ42	DQ46	158
159	DQ43	DQ47	160
161	VSS_38	VSS_39	162
163	DQ48	DQ52	164
165	DQ49	DQ53	166
167	VSS_40	VSS_41	168
169	DQS6*	DM6	170
171	DQS6	VSS_42	172
173	VSS_43	DQ54	174
175	DQ50	DQ55	176
177	DQ51	VSS_44	178
179	VSS_45	DQ60	180
181	DQ56	DQ61	182
183	DQ57	VSS_46	184
185	VSS_47	DQS7*	186
187	DM7	DQS7	188
189	VSS_48	VSS_49	190
191	DQ58	DQ62	192
193	DQ59	DQ63	194
195	VSS_50	VSS_51	196
197	SA0	EVENT*	198
199	VDDSPD	SDA	200
201	SA1	SCL	202
203	VTT_0	VTT_1	204

MEM_A_DQ<0>, MEM_A_DQ<1>, MEM_A_DQ<2>, MEM_A_DQ<3>, MEM_A_DQ<8>, MEM_A_DQ<9>, MEM_A_DQS_N<1>, MEM_A_DQS_P<1>, MEM_A_DQ<10>, MEM_A_DQ<11>, MEM_A_DQ<16>, MEM_A_DQ<17>, MEM_A_DQS_N<2>, MEM_A_DQS_P<2>, MEM_A_DQ<18>, MEM_A_DQ<19>, MEM_A_DQ<24>, MEM_A_DQ<25>, MEM_A_DQ<26>, MEM_A_DQ<27>, MEM_A_DQ<32>, MEM_A_DQ<33>, MEM_A_DQS_N<4>, MEM_A_DQS_P<4>, MEM_A_DQ<34>, MEM_A_DQ<35>, MEM_A_DQ<40>, MEM_A_DQ<41>, MEM_A_DQ<42>, MEM_A_DQ<43>, MEM_A_DQ<48>, MEM_A_DQ<49>, MEM_A_DQS_N<6>, MEM_A_DQS_P<6>, MEM_A_DQ<50>, MEM_A_DQ<51>, MEM_A_DQ<56>, MEM_A_DQ<57>, MEM_A_DQ<58>, MEM_A_DQ<59>, MEM_DIMM1_SA<0>, =PP3V3_S0_MEM_A_SPD, MEM_DIMM1_SA<1>

MEM_A_DQ<4>, MEM_A_DQ<5>, MEM_A_DQS_N<0>, MEM_A_DQS_P<0>, MEM_A_DQ<6>, MEM_A_DQ<7>, MEM_A_DQ<12>, MEM_A_DQ<13>, MEM RESET L, MEM_A_DQ<14>, MEM_A_DQ<15>, MEM_A_DQ<20>, MEM_A_DQ<21>, MEM_A_DQ<22>, MEM_A_DQ<23>, MEM_A_DQ<28>, MEM_A_DQ<29>, MEM_A_DQS_N<3>, MEM_A_DQS_P<3>, MEM_A_DQ<30>, MEM_A_DQ<31>, MEM A CKE<3>, MEM_A_DQ<36>, MEM_A_DQ<37>, MEM_A_DQ<38>, MEM_A_DQ<39>, MEM_A_DQ<44>, MEM_A_DQ<45>, MEM_A_DQS_N<5>, MEM_A_DQS_P<5>, MEM_A_DQ<46>, MEM_A_DQ<47>, MEM_A_DQ<52>, MEM_A_DQ<53>, MEM_A_DQ<54>, MEM_A_DQ<55>, MEM_A_DQ<60>, MEM_A_DQ<61>, MEM_A_DQS_N<7>, MEM_A_DQS_P<7>, MEM_A_DQ<62>, MEM_A_DQ<63>, MEM_EVENT_L, =I2C_SODIMMA_SDA, =I2C_SODIMMA_SCL

MEM A CKE<2>, MEM A BA<2>, MEM_A_A<12>, MEM_A_A<9>, MEM_A_A<8>, MEM_A_A<5>, MEM_A_A<3>, MEM_A_A<1>, MEM_A_CLK_P<2>, MEM_A_CLK_N<2>, MEM_A_A<10>, MEM_A_BA<0>, MEM A WE L, MEM A CAS L, MEM_A_A<13>, MEM A CS L<3>, MEM A CKE<0>, MEM A CKE<1>, MEM_A_A<15>, MEM_A_A<14>, MEM_A_A<11>, MEM_A_A<7>, MEM_A_A<6>, MEM_A_A<4>, MEM_A_A<2>, MEM_A_A<0>, MEM_A_CLK_P<3>, MEM_A_CLK_N<3>, MEM_A_BA<1>, MEM_A_RAS_L, MEM A CS L<2>, MEM A ODT<2>, MEM A ODT<3>

=PPVDDQ_S3_MEM_A

DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

C3010 C3011 C3012 C3013 C3014 C3015 C3016 C3017 0.1UF 20% 10V X5R 402

C3000 10UF 20% 6.3V X5R 603
C3001 10UF 20% 6.3V X5R 603
C3018 C3019 C3020 C3021 C3022 C3023 0.1UF 20% 10V CERM 402

=PP3V3_S0_MEM_A_SPD
R3040 10K 5% 1/16W ME-LF 402
R3041 10K 5% 1/16W ME-LF 402
C3040 2.2UF 20% 6.3V CERM 402-LF

=PPDDRVTT_S0_MEM_A

=PPDDRVREF_CA_MEM_A
C3035 2.2UF 20% 6.3V CERM 402-LF
C3036 0.1UF 20% 10V CERM 402

=PPDDRVTT_S0_MEM_A
C3050 C3051 C3052 C3053 1UF 20% 10V X5R 402

SYNC_MASTER=D8_MLB
SYNC_DATE=08/27/2012
PAGE TITLE: DDR3 SO-DIMM Connector A Slot1
Apple Inc.
DRAWING NUMBER: 051-9505
SIZE: D
REVISION: 8.0.0
BRANCH: prefsb
PAGE: 30 OF 144
SHEET: 30 OF 123

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Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PPVDDQ_S3_MEM_B
- =PPDDRVTT_S0_MEM_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

P/N: 516S1030

=PPDDRVREF_DQ_MEM_B

C3130 2.2UF 20% 6.3V CERM 402-LF
C3131 0.1UF 20% 10V CERM 402

J3100
SODIMM-P0.60-D8
F-ANG-SM-2
SYM 1 OF 2

1	VREFDQ	VSS_0	2
3	VSS_1	DQ4	4
5	DQ0	DQ5	6
7	DQ1	VSS_2	8
9	VSS_3	DQS0*	10
11	DM0	DQS0	12
13	VSS_4	VSS_5	14
15	DQ2	DQ6	16
17	DQ3	DQ7	18
19	VSS_6	VSS_7	20
21	DQ8	DQ12	22
23	DQ9	DQ13	24
25	VSS_8	VSS_9	26
27	DQS1*	DM1	28
29	DQS1	RESET*	30
31	VSS_10	VSS_11	32
33	DQ10	DQ14	34
35	DQ11	DQ15	36
37	VSS_12	VSS_13	38
39	DQ16	DQ20	40
41	DQ17	DQ21	42
43	VSS_14	VSS_15	44
45	DQS2*	DM2	46
47	DQS2	VSS_16	48
49	VSS_17	DQ22	50
51	DQ18	DQ23	52
53	DQ19	VSS_18	54
55	VSS_19	DQ28	56
57	DQ24	DQ29	58
59	DQ25	VSS_20	60
61	VSS_21	DQS3*	62
63	DM3	DQS3	64
65	VSS_22	VSS_23	66
67	DQ26	DQ30	68
69	DQ27	DQ31	70
71	VSS_24	VSS_25	72
KEY			
73	CKE0	CKE1	74
75	VDD_0	VDD_1	76
NCX 77	NC_0	A15	78
79	BA2	A14	80
81	VDD_2	VDD_3	82
83	A12/BC*	A11	84
85	A9	A7	86
87	VDD_4	VDD_5	88
89	A8	A6	90
91	A5	A4	92
93	VDD_6	VDD_7	94
95	A3	A2	96
97	A1	A0	98
99	VDD_8	VDD_9	100
101	CK0	CK1	102
103	CK0*	CK1*	104
105	VDD_10	VDD_11	106
107	A10_AP	BA1	108
109	BA0	RAS*	110
111	VDD_12	VDD_13	112
113	WE*	S0*	114
115	CAS*	ODT0	116
117	VDD_14	VDD_15	118
119	A13	ODT1	120
121	S1*	NC_1 NCX	122
123	VDD_16	VDD_17	124
NCX 125	TEST	VREFCA	126
127	VSS_26	VSS_27	128
129	DQ32	DQ36	130
131	DQ33	DQ37	132
133	VSS_28	VSS_29	134
135	DQS4*	DM4	136
137	DQS4	VSS_30	138
139	VSS_31	DQ38	140
141	DQ34	DQ39	142
143	DQ35	VSS_32	144
145	VSS_33	DQ44	146
147	DQ40	DQ45	148
149	DQ41	VSS_34	150
151	VSS_35	DQS5*	152
153	DM5	DQS5	154
155	VSS_36	VSS_37	156
157	DQ42	DQ46	158
159	DQ43	DQ47	160
161	VSS_38	VSS_39	162
163	DQ48	DQ52	164
165	DQ49	DQ53	166
167	VSS_40	VSS_41	168
169	DQS6*	DM6	170
171	DQS6	VSS_42	172
173	VSS_43	DQ54	174
175	DQ50	DQ55	176
177	DQ51	VSS_44	178
179	VSS_45	DQ60	180
181	DQ56	DQ61	182
183	DQ57	VSS_46	184
185	VSS_47	DQS7*	186
187	DM7	DQS7	188
189	VSS_48	VSS_49	190
191	DQ58	DQ62	192
193	DQ59	DQ63	194
195	VSS_50	VSS_51	196
197	SA0	EVENT*	198
199	VDDSPD	SDA	200
201	SA1	SCL	202
203	VTT_0	VTT_1	204

SODIMM-P0.60-D8 SYM 1 OF 2

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SODIMM-P0.60-D8
F-ANG-SM-2
SYM 2 OF 2

205	MTG HOLE
206	
207	
208	
209	

DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

=PPVDDQ_S3_MEM_B
C3110 0.1UF 20% 10V CERM 402
C3111 0.1UF 20% 10V CERM 402
C3112 0.1UF 20% 10V CERM 402
C3113 0.1UF 20% 10V CERM 402
C3114 0.1UF 20% 10V CERM 402
C3115 0.1UF 20% 10V CERM 402
C3116 0.1UF 20% 10V CERM 402
C3117 0.1UF 20% 10V CERM 402
C3100 10UF 20% 6.3V X5R 603
C3101 10UF 20% 6.3V X5R 603
C3118 0.1UF 20% 10V CERM 402
C3119 0.1UF 20% 10V CERM 402
C3120 0.1UF 20% 10V CERM 402
C3121 0.1UF 20% 10V CERM 402
C3122 0.1UF 20% 10V CERM 402
C3123 0.1UF 20% 10V CERM 402

=PP3V3_S0_MEM_B_SPD
R3141 10K 5% 1/16W MF-LF 402
MEM_DIMM2_SA<1>
MEM_DIMM2_SA<0>
=PP3V3_S0_MEM_B_SPD
C3140 2.2UF 20% 6.3V CERM 402-LF
R3140 10K 5% 1/16W MF-LF 402

=PPDDRVTT_S0_MEM_B
C3150 1UF 10% 10V X5R 402
C3151 1UF 10% 10V X5R 402
C3152 1UF 10% 10V X5R 402
C3153 1UF 10% 10V X5R 402

=PPDDRVREF_CA_MEM_B
C3135 2.2UF 20% 6.3V CERM 402-LF
C3136 0.1UF 20% 10V CERM 402

SYNC_MASTER=D8_MLB	SYNC_DATE=08/27/2012
PAGE TITLE	DDR3 SO-DIMM CONNECTOR B SLOT0
	Apple Inc.
DRAWING NUMBER	051-9505
SIZE	D
REVISION	8.0.0
BRANCH	prefsb
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SHEET	31 OF 123

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Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PPVDDQ_S3_MEM_B
- =PPDDRVTT_S0_MEM_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

P/N: 516S1030

=PPDDRVREF_DQ_MEM_B
C3230 2.2UF 20% 6.3V CERM 402-LF
C3231 0.1UF 20% 10V CERM 402

J3200 SODIMM-P0.60-D8 F-ANG-SM-2 SYM 1 OF 2

1	VREFDQ	VSS_0	2
3	VSS_1	DQ4	4
5	DQ0	DQ5	6
7	DQ1	VSS_2	8
9	VSS_3	DQS0*	10
11	DM0	DQS0	12
13	VSS_4	VSS_5	14
15	DQ2	DQ6	16
17	DQ3	DQ7	18
19	VSS_6	VSS_7	20
21	DQ8	DQ12	22
23	DQ9	DQ13	24
25	VSS_8	VSS_9	26
27	DQS1*	DM1	28
29	DQS1	RESET*	30
31	VSS_10	VSS_11	32
33	DQ10	DQ14	34
35	DQ11	DQ15	36
37	VSS_12	VSS_13	38
39	DQ16	DQ20	40
41	DQ17	DQ21	42
43	VSS_14	VSS_15	44
45	DQS2*	DM2	46
47	DQS2	VSS_16	48
49	VSS_17	DQ22	50
51	DQ18	DQ23	52
53	DQ19	VSS_18	54
55	VSS_19	DQ28	56
57	DQ24	DQ29	58
59	DQ25	VSS_20	60
61	VSS_21	DQS3*	62
63	DM3	DQS3	64
65	VSS_22	VSS_23	66
67	DQ26	DQ30	68
69	DQ27	DQ31	70
71	VSS_24	VSS_25	72
KEY			
73	CKE0	CKE1	74
75	VDD_0	VDD_1	76
NCX 77	NC_0	A15	78
79	BA2	A14	80
81	VDD_2	VDD_3	82
83	A12/BC*	A11	84
85	A9	A7	86
87	VDD_4	VDD_5	88
89	A8	A6	90
91	A5	A4	92
93	VDD_6	VDD_7	94
95	A3	A2	96
97	A1	A0	98
99	VDD_8	VDD_9	100
101	CK0	CK1	102
103	CK0*	CK1*	104
105	VDD_10	VDD_11	106
107	A10_AP	BA1	108
109	BA0	RAS*	110
111	VDD_12	VDD_13	112
113	WE*	S0*	114
115	CAS*	ODT0	116
117	VDD_14	VDD_15	118
119	A13	ODT1	120
121	S1*	NC_1 XNC 122	
123	VDD_16	VDD_17	124
NCX 125	TEST	VREFCA	126
127	VSS_26	VSS_27	128
129	DQ32	DQ36	130
131	DQ33	DQ37	132
133	VSS_28	VSS_29	134
135	DQS4*	DM4	136
137	DQS4	VSS_30	138
139	VSS_31	DQ38	140
141	DQ34	DQ39	142
143	DQ35	VSS_32	144
145	VSS_33	DQ44	146
147	DQ40	DQ45	148
149	DQ41	VSS_34	150
151	VSS_35	DQS5*	152
153	DM5	DQS5	154
155	VSS_36	VSS_37	156
157	DQ42	DQ46	158
159	DQ43	DQ47	160
161	VSS_38	VSS_39	162
163	DQ48	DQ52	164
165	DQ49	DQ53	166
167	VSS_40	VSS_41	168
169	DQS6*	DM6	170
171	DQS6	VSS_42	172
173	VSS_43	DQ54	174
175	DQ50	DQ55	176
177	DQ51	VSS_44	178
179	VSS_45	DQ60	180
181	DQ56	DQ61	182
183	DQ57	VSS_46	184
185	VSS_47	DQS7*	186
187	DM7	DQS7	188
189	VSS_48	VSS_49	190
191	DQ58	DQ62	192
193	DQ59	DQ63	194
195	VSS_50	VSS_51	196
197	SA0	EVENT*	198
199	VDDSPD	SDA	200
201	SA1	SCL	202
203	VTT_0	VTT_1	204

SODIMM-P0.60-D8 SYM 1 OF 2

=MEM_B_DQ<0>, =MEM_B_DQ<1>, =MEM_B_DQ<2>, =MEM_B_DQ<3>, =MEM_B_DQ<8>, =MEM_B_DQ<9>, =MEM_B_DQS_N<1>, =MEM_B_DQS_P<1>, =MEM_B_DQ<10>, =MEM_B_DQ<11>, =MEM_B_DQ<16>, =MEM_B_DQ<17>, =MEM_B_DQS_N<2>, =MEM_B_DQS_P<2>, =MEM_B_DQ<18>, =MEM_B_DQ<19>, =MEM_B_DQ<24>, =MEM_B_DQ<25>, =MEM_B_DQ<26>, =MEM_B_DQ<27>, MEM_B_CKE<2>, MEM_B_BA<2>, MEM_B_A<12>, MEM_B_A<9>, MEM_B_A<8>, MEM_B_A<5>, MEM_B_A<3>, MEM_B_A<1>, MEM_B_CLK_P<2>, MEM_B_CLK_N<2>, MEM_B_A<10>, MEM_B_BA<0>, MEM_B_WE_L, MEM_B_CAS_L, MEM_B_A<13>, MEM_B_CS_L<3>, =MEM_B_DQ<32>, =MEM_B_DQ<33>, =MEM_B_DQS_N<4>, =MEM_B_DQS_P<4>, =MEM_B_DQ<34>, =MEM_B_DQ<35>, =MEM_B_DQ<40>, =MEM_B_DQ<41>, =MEM_B_DQ<42>, =MEM_B_DQ<43>, =MEM_B_DQ<48>, =MEM_B_DQ<49>, =MEM_B_DQS_N<6>, =MEM_B_DQS_P<6>, =MEM_B_DQ<50>, =MEM_B_DQ<51>, =MEM_B_DQ<56>, =MEM_B_DQ<57>, =MEM_B_DQ<58>, =MEM_B_DQ<59>, MEM_DIMM3_SA<0>, =PP3V3_S0_MEM_B_SPD, MEM_DIMM3_SA<1>

SODIMM-P0.60-D8 SYM 2 OF 2

=MEM_B_DQ<4>, =MEM_B_DQ<5>, =MEM_B_DQS_N<0>, =MEM_B_DQS_P<0>, =MEM_B_DQ<6>, =MEM_B_DQ<7>, =MEM_B_DQ<12>, =MEM_B_DQ<13>, MEM_RESET_L, =MEM_B_DQ<14>, =MEM_B_DQ<15>, =MEM_B_DQ<20>, =MEM_B_DQ<21>, =MEM_B_DQ<22>, =MEM_B_DQ<23>, =MEM_B_DQ<28>, =MEM_B_DQ<29>, =MEM_B_DQS_N<3>, =MEM_B_DQS_P<3>, =MEM_B_DQ<30>, =MEM_B_DQ<31>, MEM_B_CKE<3>, MEM_B_A<15>, MEM_B_A<14>, MEM_B_A<11>, MEM_B_A<7>, MEM_B_A<6>, MEM_B_A<4>, MEM_B_A<2>, MEM_B_A<0>, MEM_B_CLK_P<3>, MEM_B_CLK_N<3>, MEM_B_BA<1>, MEM_B_RAS_L, MEM_B_CS_L<2>, MEM_B_ODT<2>, MEM_B_ODT<3>, =PPDDRVREF_CA_MEM_B, =MEM_B_DQ<36>, =MEM_B_DQ<37>, =MEM_B_DQ<38>, =MEM_B_DQ<39>, =MEM_B_DQ<44>, =MEM_B_DQ<45>, =MEM_B_DQS_N<5>, =MEM_B_DQS_P<5>, =MEM_B_DQ<46>, =MEM_B_DQ<47>, =MEM_B_DQ<52>, =MEM_B_DQ<53>, =MEM_B_DQ<54>, =MEM_B_DQ<55>, =MEM_B_DQ<60>, =MEM_B_DQ<61>, =MEM_B_DQS_N<7>, =MEM_B_DQS_P<7>, =MEM_B_DQ<62>, =MEM_B_DQ<63>, MEM_EVENT_L, =I2C_SODIMMB_SDA, =I2C_SODIMMB_SCL

J3200 SODIMM-P0.60-D8 F-ANG-SM-2 SYM 2 OF 2

205	MTG HOLE
206	
207	
208	
209	

DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

=PPVDDQ_S3_MEM_B
C3210 0.1UF 20% 10V CERM 402
C3211 0.1UF 20% 10V CERM 402
C3212 0.1UF 20% 10V CERM 402
C3213 0.1UF 20% 10V CERM 402
C3214 0.1UF 20% 10V CERM 402
C3215 0.1UF 20% 10V CERM 402
C3216 0.1UF 20% 10V CERM 402
C3217 0.1UF 20% 10V CERM 402
C3200 10UF 20% 6.3V X6S 603
C3201 10UF 20% 6.3V X6S 603
C3218 0.1UF 20% 10V CERM 402
C3219 0.1UF 20% 10V CERM 402
C3220 0.1UF 20% 10V CERM 402
C3221 0.1UF 20% 10V CERM 402
C3222 0.1UF 20% 10V CERM 402
C3223 0.1UF 20% 10V CERM 402

=PP3V3_S0_MEM_B_SPD
R3241 10K 5% 1/16W MF-LF 402
R3240 10K 5% 1/16W MF-LF 402
MEM_DIMM3_SA<1>
MEM_DIMM3_SA<0>
=PP3V3_S0_MEM_B_SPD
C3240 2.2UF 20% 6.3V CERM 402-LF

=PPDDRVTT_S0_MEM_B
C3250 1UF 10% 10V X5R 402
C3251 1UF 10% 10V X5R 402
C3252 1UF 10% 10V X5R 402
C3253 1UF 10% 10V X5R 402

C3235 2.2UF 20% 6.3V CERM 402-LF
C3236 0.1UF 20% 10V CERM 402

=PPVDDQ_S3_MEM_B

SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012

PAGE TITLE: DDR3 SO-DIMM CONNECTOR B SLOT1

Apple Inc.

DRAWING NUMBER: 051-9505 SIZE: D
REVISION: 8.0.0
BRANCH: prefsb
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MEM_A_DQS_N<0>	MAKE_BASE=TRUE		=MEM_A_DQS_N<0>
MEM_A_DQS_P<0>	MAKE_BASE=TRUE		=MEM_A_DQS_P<0>
MEM_A_DQ<7>	MAKE_BASE=TRUE		=MEM_A_DQ<7>
MEM_A_DQ<6>	MAKE_BASE=TRUE		=MEM_A_DQ<6>
MEM_A_DQ<5>	MAKE_BASE=TRUE		=MEM_A_DQ<4>
MEM_A_DQ<4>	MAKE_BASE=TRUE		=MEM_A_DQ<1>
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MEM_A_DQ<2>	MAKE_BASE=TRUE		=MEM_A_DQ<2>
MEM_A_DQ<1>	MAKE_BASE=TRUE		=MEM_A_DQ<5>
MEM_A_DQ<0>	MAKE_BASE=TRUE		=MEM_A_DQ<0>
MEM_A_DQS_N<1>	MAKE_BASE=TRUE		=MEM_A_DQS_N<1>
MEM_A_DQS_P<1>	MAKE_BASE=TRUE		=MEM_A_DQS_P<1>
MEM_A_DQ<15>	MAKE_BASE=TRUE		=MEM_A_DQ<15>
MEM_A_DQ<14>	MAKE_BASE=TRUE		=MEM_A_DQ<14>
MEM_A_DQ<13>	MAKE_BASE=TRUE		=MEM_A_DQ<13>
MEM_A_DQ<12>	MAKE_BASE=TRUE		=MEM_A_DQ<12>
MEM_A_DQ<11>	MAKE_BASE=TRUE		=MEM_A_DQ<11>
MEM_A_DQ<10>	MAKE_BASE=TRUE		=MEM_A_DQ<10>
MEM_A_DQ<9>	MAKE_BASE=TRUE		=MEM_A_DQ<9>
MEM_A_DQ<8>	MAKE_BASE=TRUE		=MEM_A_DQ<8>
MEM_A_DQS_N<2>	MAKE_BASE=TRUE		=MEM_A_DQS_N<2>
MEM_A_DQS_P<2>	MAKE_BASE=TRUE		=MEM_A_DQS_P<2>
MEM_A_DQ<23>	MAKE_BASE=TRUE		=MEM_A_DQ<23>
MEM_A_DQ<22>	MAKE_BASE=TRUE		=MEM_A_DQ<22>
MEM_A_DQ<21>	MAKE_BASE=TRUE		=MEM_A_DQ<21>
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MEM_A_DQ<19>	MAKE_BASE=TRUE		=MEM_A_DQ<18>
MEM_A_DQ<18>	MAKE_BASE=TRUE		=MEM_A_DQ<19>
MEM_A_DQ<17>	MAKE_BASE=TRUE		=MEM_A_DQ<17>
MEM_A_DQ<16>	MAKE_BASE=TRUE		=MEM_A_DQ<16>
MEM_A_DQS_N<3>	MAKE_BASE=TRUE		=MEM_A_DQS_N<3>
MEM_A_DQS_P<3>	MAKE_BASE=TRUE		=MEM_A_DQS_P<3>
MEM_A_DQ<31>	MAKE_BASE=TRUE		=MEM_A_DQ<31>
MEM_A_DQ<30>	MAKE_BASE=TRUE		=MEM_A_DQ<30>
MEM_A_DQ<29>	MAKE_BASE=TRUE		=MEM_A_DQ<29>
MEM_A_DQ<28>	MAKE_BASE=TRUE		=MEM_A_DQ<28>
MEM_A_DQ<27>	MAKE_BASE=TRUE		=MEM_A_DQ<27>
MEM_A_DQ<26>	MAKE_BASE=TRUE		=MEM_A_DQ<26>
MEM_A_DQ<25>	MAKE_BASE=TRUE		=MEM_A_DQ<25>
MEM_A_DQ<24>	MAKE_BASE=TRUE		=MEM_A_DQ<24>
MEM_A_DQS_N<4>	MAKE_BASE=TRUE		=MEM_A_DQS_N<4>
MEM_A_DQS_P<4>	MAKE_BASE=TRUE		=MEM_A_DQS_P<4>
MEM_A_DQ<39>	MAKE_BASE=TRUE		=MEM_A_DQ<39>
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MEM_A_DQ<37>	MAKE_BASE=TRUE		=MEM_A_DQ<32>
MEM_A_DQ<36>	MAKE_BASE=TRUE		=MEM_A_DQ<37>
MEM_A_DQ<35>	MAKE_BASE=TRUE		=MEM_A_DQ<35>
MEM_A_DQ<34>	MAKE_BASE=TRUE		=MEM_A_DQ<34>
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MEM_A_DQ<32>	MAKE_BASE=TRUE		=MEM_A_DQ<36>
MEM_A_DQS_N<5>	MAKE_BASE=TRUE		=MEM_A_DQS_N<5>
MEM_A_DQS_P<5>	MAKE_BASE=TRUE		=MEM_A_DQS_P<5>
MEM_A_DQ<47>	MAKE_BASE=TRUE		=MEM_A_DQ<47>
MEM_A_DQ<46>	MAKE_BASE=TRUE		=MEM_A_DQ<46>
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MEM_A_DQ<43>	MAKE_BASE=TRUE		=MEM_A_DQ<43>
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MEM_A_DQ<40>	MAKE_BASE=TRUE		=MEM_A_DQ<40>
MEM_A_DQS_N<6>	MAKE_BASE=TRUE		=MEM_A_DQS_N<6>
MEM_A_DQS_P<6>	MAKE_BASE=TRUE		=MEM_A_DQS_P<6>
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MEM_A_DQ<54>	MAKE_BASE=TRUE		=MEM_A_DQ<54>
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MEM_A_DQ<52>	MAKE_BASE=TRUE		=MEM_A_DQ<52>
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MEM_A_DQ<48>	MAKE_BASE=TRUE		=MEM_A_DQ<48>
MEM_A_DQS_N<7>	MAKE_BASE=TRUE		=MEM_A_DQS_N<7>
MEM_A_DQS_P<7>	MAKE_BASE=TRUE		=MEM_A_DQS_P<7>
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MEM_A_DQ<60>	MAKE_BASE=TRUE		=MEM_A_DQ<60>
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MEM_A_DQ<58>	MAKE_BASE=TRUE		=MEM_A_DQ<59>
MEM_A_DQ<57>	MAKE_BASE=TRUE		=MEM_A_DQ<57>
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MEM_B_DQS_P<0>	MAKE_BASE=TRUE		=MEM_B_DQS_P<0>
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MEM_B_DQ<3>	MAKE_BASE=TRUE		=MEM_B_DQ<7>
MEM_B_DQ<2>	MAKE_BASE=TRUE		=MEM_B_DQ<2>
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MEM_B_DQS_N<1>	MAKE_BASE=TRUE		=MEM_B_DQS_N<1>
MEM_B_DQS_P<1>	MAKE_BASE=TRUE		=MEM_B_DQS_P<1>
MEM_B_DQ<15>	MAKE_BASE=TRUE		=MEM_B_DQ<11>
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MEM_B_DQ<13>	MAKE_BASE=TRUE		=MEM_B_DQ<13>
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MEM_B_DQ<11>	MAKE_BASE=TRUE		=MEM_B_DQ<15>
MEM_B_DQ<10>	MAKE_BASE=TRUE		=MEM_B_DQ<14>
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MEM_B_DQS_N<2>	MAKE_BASE=TRUE		=MEM_B_DQS_N<2>
MEM_B_DQS_P<2>	MAKE_BASE=TRUE		=MEM_B_DQS_P<2>
MEM_B_DQ<23>	MAKE_BASE=TRUE		=MEM_B_DQ<22>
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MEM_B_DQ<21>	MAKE_BASE=TRUE		=MEM_B_DQ<21>
MEM_B_DQ<20>	MAKE_BASE=TRUE		=MEM_B_DQ<20>
MEM_B_DQ<19>	MAKE_BASE=TRUE		=MEM_B_DQ<23>
MEM_B_DQ<18>	MAKE_BASE=TRUE		=MEM_B_DQ<19>
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MEM_B_DQ<16>	MAKE_BASE=TRUE		=MEM_B_DQ<16>
MEM_B_DQS_N<3>	MAKE_BASE=TRUE		=MEM_B_DQS_N<3>
MEM_B_DQS_P<3>	MAKE_BASE=TRUE		=MEM_B_DQS_P<3>
MEM_B_DQ<31>	MAKE_BASE=TRUE		=MEM_B_DQ<31>
MEM_B_DQ<30>	MAKE_BASE=TRUE		=MEM_B_DQ<30>
MEM_B_DQ<29>	MAKE_BASE=TRUE		=MEM_B_DQ<29>
MEM_B_DQ<28>	MAKE_BASE=TRUE		=MEM_B_DQ<28>
MEM_B_DQ<27>	MAKE_BASE=TRUE		=MEM_B_DQ<27>
MEM_B_DQ<26>	MAKE_BASE=TRUE		=MEM_B_DQ<26>
MEM_B_DQ<25>	MAKE_BASE=TRUE		=MEM_B_DQ<25>
MEM_B_DQ<24>	MAKE_BASE=TRUE		=MEM_B_DQ<24>
MEM_B_DQS_N<4>	MAKE_BASE=TRUE		=MEM_B_DQS_N<4>
MEM_B_DQS_P<4>	MAKE_BASE=TRUE		=MEM_B_DQS_P<4>
MEM_B_DQ<39>	MAKE_BASE=TRUE		=MEM_B_DQ<39>
MEM_B_DQ<38>	MAKE_BASE=TRUE		=MEM_B_DQ<38>
MEM_B_DQ<37>	MAKE_BASE=TRUE		=MEM_B_DQ<37>
MEM_B_DQ<36>	MAKE_BASE=TRUE		=MEM_B_DQ<36>
MEM_B_DQ<35>	MAKE_BASE=TRUE		=MEM_B_DQ<35>
MEM_B_DQ<34>	MAKE_BASE=TRUE		=MEM_B_DQ<34>
MEM_B_DQ<33>	MAKE_BASE=TRUE		=MEM_B_DQ<33>
MEM_B_DQ<32>	MAKE_BASE=TRUE		=MEM_B_DQ<32>
MEM_B_DQS_N<5>	MAKE_BASE=TRUE		=MEM_B_DQS_N<5>
MEM_B_DQS_P<5>	MAKE_BASE=TRUE		=MEM_B_DQS_P<5>
MEM_B_DQ<47>	MAKE_BASE=TRUE		=MEM_B_DQ<47>
MEM_B_DQ<46>	MAKE_BASE=TRUE		=MEM_B_DQ<46>
MEM_B_DQ<45>	MAKE_BASE=TRUE		=MEM_B_DQ<45>
MEM_B_DQ<44>	MAKE_BASE=TRUE		=MEM_B_DQ<44>
MEM_B_DQ<43>	MAKE_BASE=TRUE		=MEM_B_DQ<43>
MEM_B_DQ<42>	MAKE_BASE=TRUE		=MEM_B_DQ<42>
MEM_B_DQ<41>	MAKE_BASE=TRUE		=MEM_B_DQ<41>
MEM_B_DQ<40>	MAKE_BASE=TRUE		=MEM_B_DQ<40>
MEM_B_DQS_N<6>	MAKE_BASE=TRUE		=MEM_B_DQS_N<6>
MEM_B_DQS_P<6>	MAKE_BASE=TRUE		=MEM_B_DQS_P<6>
MEM_B_DQ<55>	MAKE_BASE=TRUE		=MEM_B_DQ<55>
MEM_B_DQ<54>	MAKE_BASE=TRUE		=MEM_B_DQ<54>
MEM_B_DQ<53>	MAKE_BASE=TRUE		=MEM_B_DQ<52>
MEM_B_DQ<52>	MAKE_BASE=TRUE		=MEM_B_DQ<53>
MEM_B_DQ<51>	MAKE_BASE=TRUE		=MEM_B_DQ<51>
MEM_B_DQ<50>	MAKE_BASE=TRUE		=MEM_B_DQ<50>
MEM_B_DQ<49>	MAKE_BASE=TRUE		=MEM_B_DQ<48>
MEM_B_DQ<48>	MAKE_BASE=TRUE		=MEM_B_DQ<49>
MEM_B_DQS_N<7>	MAKE_BASE=TRUE		=MEM_B_DQS_N<7>
MEM_B_DQS_P<7>	MAKE_BASE=TRUE		=MEM_B_DQS_P<7>
MEM_B_DQ<63>	MAKE_BASE=TRUE		=MEM_B_DQ<63>
MEM_B_DQ<62>	MAKE_BASE=TRUE		=MEM_B_DQ<58>
MEM_B_DQ<61>	MAKE_BASE=TRUE		=MEM_B_DQ<60>
MEM_B_DQ<60>	MAKE_BASE=TRUE		=MEM_B_DQ<61>
MEM_B_DQ<59>	MAKE_BASE=TRUE		=MEM_B_DQ<59>
MEM_B_DQ<58>	MAKE_BASE=TRUE		=MEM_B_DQ<62>
MEM_B_DQ<57>	MAKE_BASE=TRUE		=MEM_B_DQ<56>
MEM_B_DQ<56>	MAKE_BASE=TRUE		=MEM_B_DQ<57>

SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012

PAGE TITLE
DDR3 ALIASES AND BITSWAPS

Apple Inc.

DRAWING NUMBER 051-9505 SIZE D

REVISION 8.0.0

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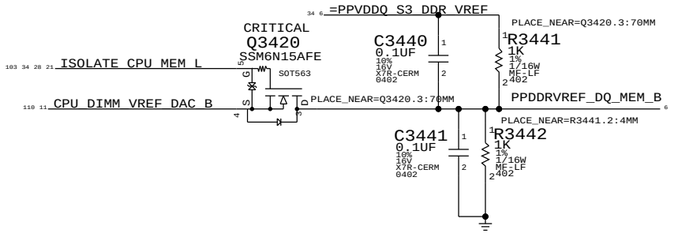
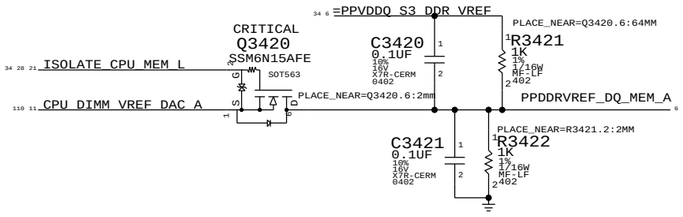
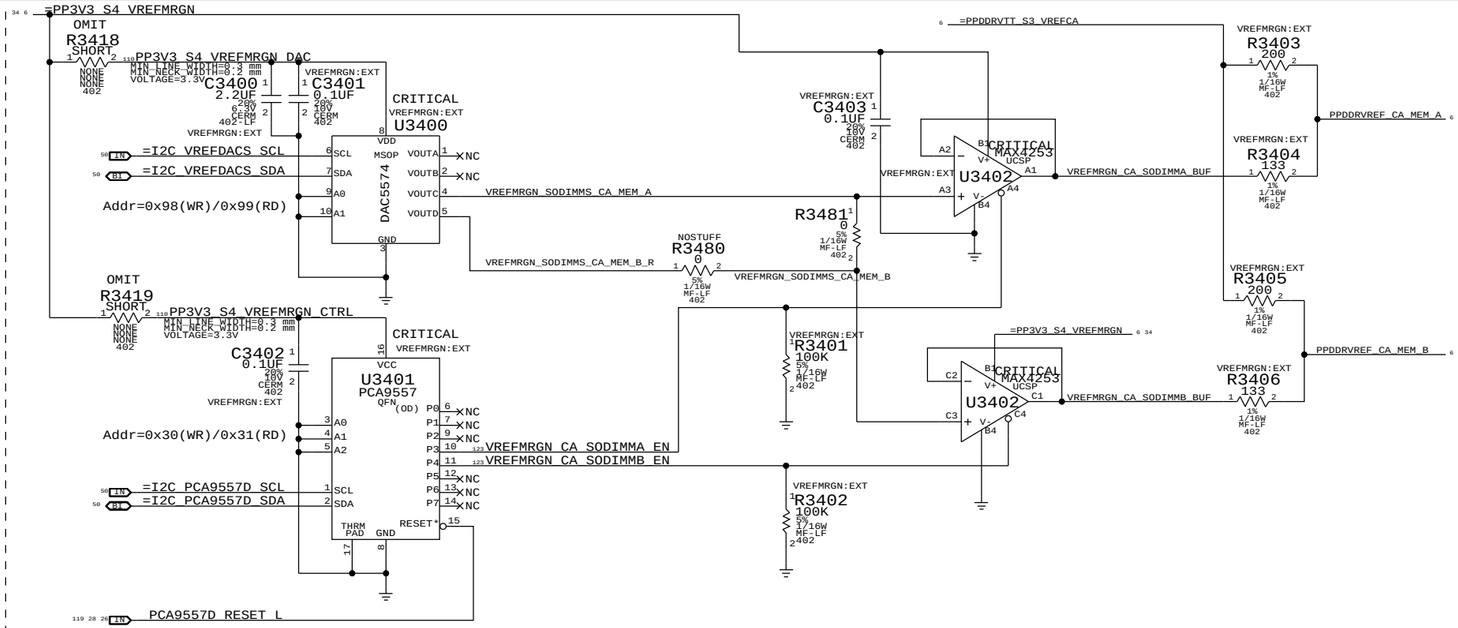
VRef DQ

Driven by CPU

NOTE: CPU DAC output step sizes:
DDR3 (1.5V) 7.70mV per step







RST* on 'platform reset' so that system watchdog will disable margining.

NOTE: MEMVREG and FRAMEBUF share a DAC output, cannot enable both at the same time!

NOTE: Margining will be disabled across all soft-resets and sleep/wake cycles.

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S0004	2	RES,MTL FLM,0,5%,402,SM,LF	R3403,R3405		VREFMRGN:N

	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% VRef)
DAC Channel:	C	C	D	D
PCA9557D Pin:	3	4	5	6
Nominal value	0.75V (DAC: 0x3A)		1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:	0.300V - 1.200V (+/- 450mV)		1.000V - 2.000V (+/- 500mV)	1.056V - 1.442V (+/- 180mV)
DAC range:	0.000V - 1.501V (0x00 - 0x74)		0.000V - 3.000V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xFF)
VRef current:	+3.4mA - -3.4mA (- = sourced)		+61uA - -61uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:	7.69mV / step @ output		8.59mV / step @ output	1.51mV / step @ output

SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012

PAGE TITLE
DDR3/FRAMEBUF VREF MARGINING

Apple Inc.

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AIRPORT BLUETOOTH

WI-FI POWER CONSUMPTION: RDAR://10174119

=PP3V3_S4_AP
AP_PWR_EN_ISO
U3502 TPS22924B CSP
=PP3V3_S4_AP_FET
PP3V3_S4_AP_FET
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
L3502 FERR-220-OHM-2.5A 0603
C3502 0.1UF 10% 16V X7R-CERM 0402
C3503 0.1UF 10% 16V X7R-CERM 0402
C3504 10UF 20% 6.3V X5R 603
PP3V3_S4_AP_FLT
NET_PHYSICAL_TYPE=POWER_PHY
J3500 SSD-K99 F-RT-SM1
AP_EVENT_L
PCIE_AP_R2D_C_N
PCIE_AP_R2D_C_P
C3505 0.1UF 10% X5R 6.3V 201
C3506 0.1UF 10% X5R 6.3V 201
PCIE_AP_R2D_N
PCIE_AP_R2D_P
PCIE_CLK100M_AP_N
PCIE_CLK100M_AP_P
PCIE_AP_D2R_P
PCIE_AP_D2R_N
AP_WAKE_L
AP_RESET_CONN_L
AP_CLKREQ_Q_L
USB_BT_MUX_N
USB_BT_MUX_P
PP3V3_G3H_BT_FLT
SMC_S4_WAKESRC_EN
Q3543 DMC2400UV SOT563 P-CH
BT_PWR_RST_L_Q
BT_PWR_RST_L
PM_PCH_PWROK
R3542 10K 5% 1/16W MF-LF 402
=PP3V3_G3H_BT
U3503 TPS22924B CSP
PP3V3_G3H_BT_FET
L3501 FERR-220-OHM-2.5A 0603
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2MM
C3507 0.1UF 10% 16V X7R-CERM 0402
C3508 10UF 20% 6.3V X5R 603
BT_PWR_EN
BT_PWR_RST_L_Q
R3543 10K 5% 1/16W MF-LF 402
N-CH

SUPERVISOR & CLKREG # ISOLATION
DELAY = 130 MS +/- 20%

=PP3V3_S4_AP_FET
=PP3V3_S4_AP
R3530 100K 1% 1/16W MF-LF 402
R3531 232K 1% 1/16W MF-LF 402
C3530 0.1uF 20% 10V CERM 402
U3530 SLG4AP041V TDFN
P3V3AP_VMON
AP_RESET_CONN_L
AP_CLKREQ_Q_L
AP_RESET_L
AP_PWR_EN_ISO
AP_CLKREQ_L_ISO
R3532 100K 1% 1/16W MF-LF 402

SMC_PME_S4_WAKE_L
Q3501 SSM3K15FV SOD-VESM-HF
C3531 0.1uF 10% 16V X7R-CERM 402
U3501 USB3740 DFN
USB_BT_P
USB_BT_N
USB_ACT_DET
PM_PGOOD_P3V3_S4_FET
USB_BT_MUX_P
USB_BT_MUX_N
R3599 15K 1% 1/20W MF 201
SIGNAL_MODEL=SWI_USB3740_DFN_USB3740_MOJO

Q3570 SSM3K15FV SOD-VESM-HF
PCIE_WAKE_L
R3570 10K 5% 1/16W MF-LF 402

SYNC_MASTER=D8_MLB	SYNC_DATE=08/27/2012
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Apple Inc.	DRAWING NUMBER 051-9505 SIZE D
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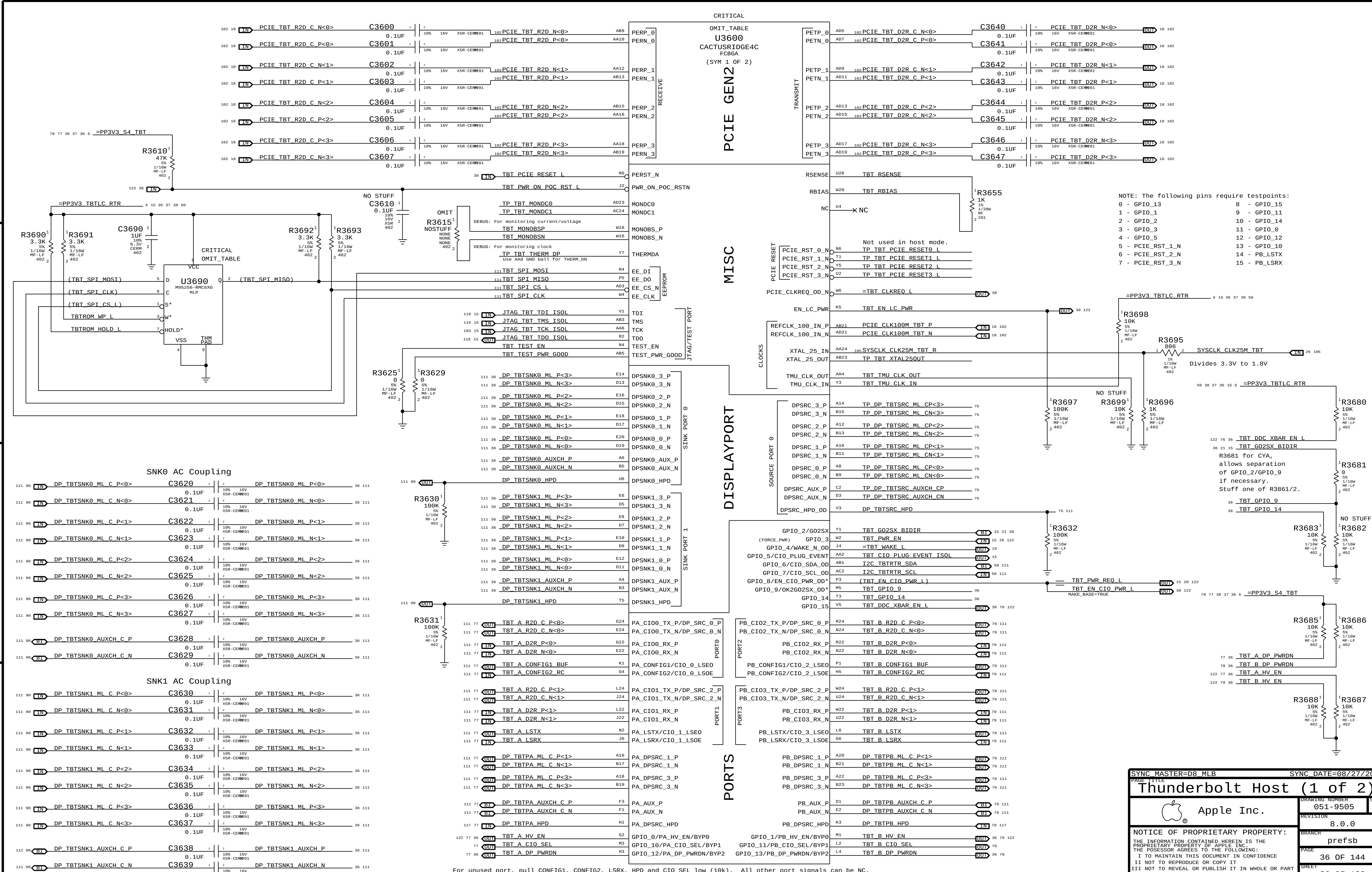

SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012

PAGE TITLE: Thunderbolt Host (1 of 2)

Apple Inc.

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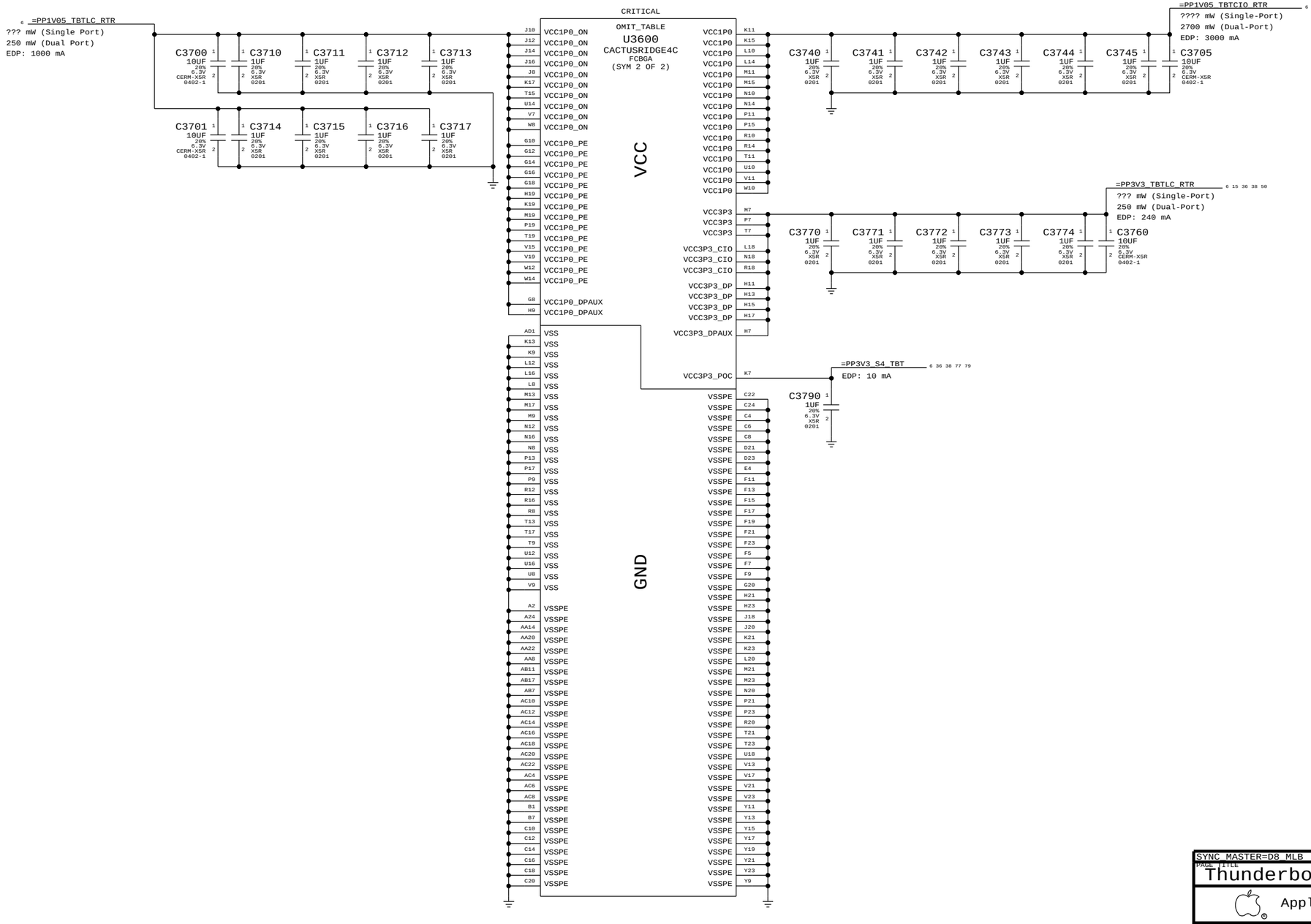

EDP current / power consumption figures from CR DG v0.57, IBL doc #472455.

SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012

PAGE TITLE: Thunderbolt Host (2 of 2)

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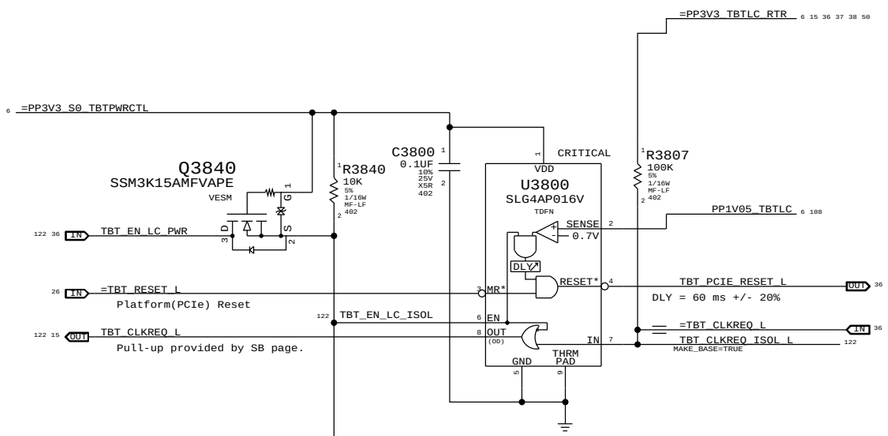
Page Notes

Power aliases required by this page:
- =PPVIN_SW_TBTBST (8-13V Boost Input)
- =PP15V_TBT_REG (15V Boost Output)
- =PP3V3_TBT_P3V3TBTFET (3.3V FET Input)
- =PP3V3_TBT_FET (3.3V FET Output)
- =PP3V3_S0_TBTPWRCTL
- =PP1V05_TBT_P1V05TBTFET (1.05V FET Input)
- =PP1V05_TBT_FET (1.05V FET Output)

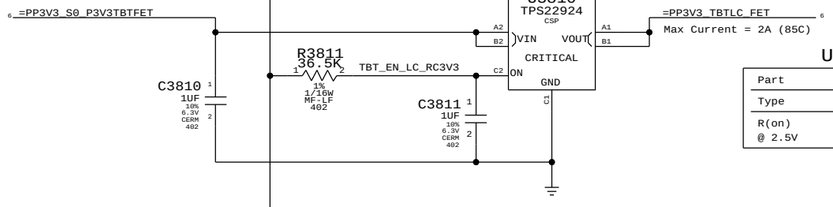
Signal aliases required by this page:
- =TBT_CLKREQ_L
- =TBT_RESET_L

BOM options provided by this page:
TBTBST:Y - Stuffs 15V boost circuitry.

Supervisor & CLKREQ# Isolation



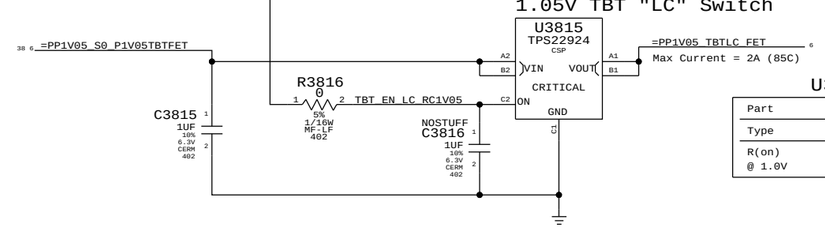
3.3V TBT "LC" Switch



U3810

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max

1.05V TBT "LC" Switch

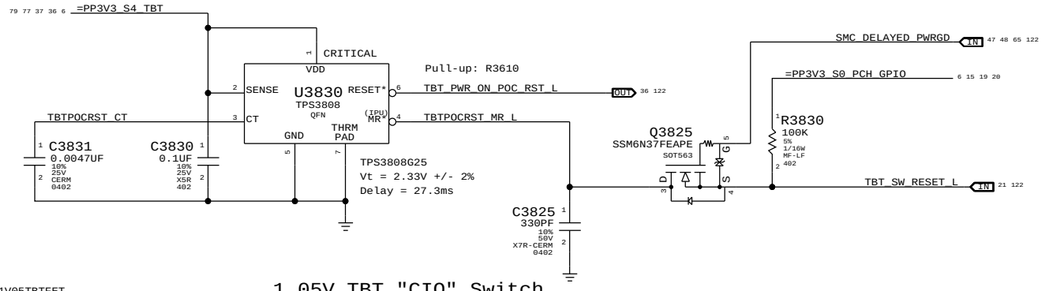


U3815

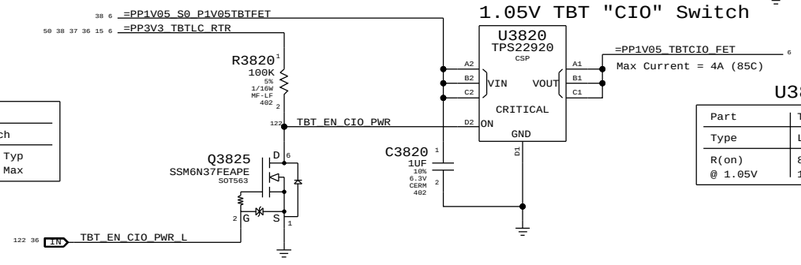
Part	TPS22924C
Type	Load Switch
R(on) @ 1.0V	20.3 mOhm Typ 28.6 mOhm Max

TBT "POC" Power-up Reset

Intel investigating whether RC is sufficient.



1.05V TBT "CIO" Switch



U3820

Part	TPS22920
Type	Load Switch
R(on) @ 1.05V	8 mOhm Typ 11.5 mOhm Max

SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012

PAGE TITLE
Thunderbolt Power Support

Apple Inc.

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BCM57765 ENET SR pins are internal 1.2V switching regulator. See note for SR_DISABLE below.
If disabled: Okay to float VDD, VDDP & LX pin. VFB must always connect to =PP1V2_S3_ENET_PHY.
If enabled: VDD/VDDP connect to =PP3V3_S3_ENET_PHY (add bypassing), LX connects to inductor.
Special Star routing needed on these pins. Decoupling on Pg 37.

=PP3V3_S4_ENET_FET
281mA (1000base-T max power, Caesar IV)

R3901 0 5% 1/16W MF-LF 402

PP3V3_S4_ENET_FET_SRVDD
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

C3979 4.7UF 20% 6.3V X5R-CERM 402
C3996 0.1UF 10% 16V X5R-CERM 0201
C3997 0.1UF 10% 16V X5R-CERM 0201

=PP3V3R1V8_CR_IOPWR_OUT
VDD for Card Reader I/O

CRITICAL
L3900
FERR-600-OHM-300MA-0.85OHM 0402

PP3V3_S4_ENET_FET_XTALVDDH
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

C3900 0.1UF 10% 16V X5R-CERM 0201

CRITICAL
L3905
FERR-600-OHM-300MA-0.85OHM 0402

PP3V3_S4_ENET_FET_BIASVDDH
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

C3905 0.1UF 10% 16V X5R-CERM 0201

CRITICAL
L3910
FERR-600-OHM-300MA-0.85OHM 0402

PP3V3_S4_ENET_FET_AVDDH
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

R3910 4.7K 5% 1/16W MF-LF 402
C3910 0.1UF 10% 16V X5R-CERM 0201
C3911 0.1UF 10% 16V X5R-CERM 0201
C3912 1.0UF 10% 6.3V X5R-CERM 0201

C3915 4.7UF 20% 6.3V X5R-CERM 402
C3999 0.1UF 10% 16V X5R-CERM 0201
C3998 0.1UF 10% 16V X5R-CERM 0201
C3916 0.1UF 10% 16V X5R-CERM 0201

R3940 4.7K 5% 1/16W MF-LF 402
R3941 4.7K 5% 1/16W MF-LF 402

=PP3V3_S0_ENET
Current Limiting Resistor
R3942 1K 5% 1/16W MF-LF 402

C3950 0.1UF 10% 16V X5R-CERM 0201
C3951 0.1UF 10% 16V X5R-CERM 0201
C3955 0.1UF 10% 16V X5R-CERM 0201
C3956 0.1UF 10% 16V X5R-CERM 0201

PCIE_ENET_D2R_N
PCIE_ENET_D2R_P
PCIE_ENET_D2R_C_P
PCIE_ENET_D2R_C_N

ENET_VMAIN_PRSNT
PCIE_ENET_D2R_C_N
PCIE_ENET_D2R_C_P
PCIE_ENET_R2D_P
PCIE_ENET_R2D_N
PCIE_CLK100M_ENET_P
PCIE_CLK100M_ENET_N
ENET_RESET_L
ENET_CLKREQ_L_Q
ENET_LOW_PWR
SMB_ENET_SCL
SMB_ENET_SDA
ENET_SCLK
ENET_MISO
ENET_MOSI
ENET_CS_L
TP_ENET_CR_3V3_EN_L
ENET_TRAFFICLED_L
SYSCLK_CLK25M_ENET
ENET_RDAC

=ENET_WAKE_L
(See note)

WAKE#
Must isolate from PCIe WAKE# if PHY is powered-down in S3/S5. Standard N-channel FET isolation suggested.
If PHY is always powered then alias =ENET_WAKE_L to PCIE_WAKE_L.

ENET_SR_LX
ENET_SR_VFB
Internal 1.2V Switching Regulator pins.

=PP1V2_S4_ENET_PHY
396mA (1000base-T, Caesar II)

CRITICAL
L3920
FERR-600-OHM-300MA-0.85OHM 0402

PP1V2_S4_ENET_PHY_AVDDL
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V

C3921 0.1UF 10% 16V X5R-CERM 0201
C3920 4.7UF 20% 6.3V X5R-CERM1 402
C3913 1.0UF 10% 6.3V X5R-CERM 0201

CRITICAL
L3925
FERR-600-OHM-0.5A SM

PP1V2_S4_ENET_PHY_PCIEPLL
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V

C3926 0.1UF 10% 16V X5R-CERM 0201
C3925 4.7UF 20% 6.3V X5R-CERM1 402

CRITICAL
L3930
FERR-600-OHM-300MA-0.85OHM 0402

PP1V2_S4_ENET_PHY_GPHYPLL
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.2V

C3931 0.1UF 10% 16V X5R-CERM 0201
C3930 4.7UF 20% 6.3V X5R-CERM1 402

C3936 0.1UF 10% 16V X5R-CERM 0201
C3935 10UF 20% 6.3V X5R 603

LR_OUT/GPIO1 is used as a 3.3V/1.8V internal LDO out for the card reader on-chip I/O.
Connect only to U3900 pin 20.

OMIT_TABLE
U3900
BCM57765
QFN-8X8

AVDDH BIASVDDH XTALVDDH VDDO SR_VDD SR_VDDP SR_LX SR_VFB AVDDL PCIE_PLLVDDL GPHY_PLLVDDL VDDC

TRD0_P TRD0_N TRD1_P TRD1_N TRD2_P TRD2_N TRD3_P TRD3_N
ENETCONN_MDI P<0>
ENETCONN_MDI N<0>
ENETCONN_MDI P<1>
ENETCONN_MDI N<1>
ENETCONN_MDI P<2>
ENETCONN_MDI N<2>
ENETCONN_MDI P<3>
ENETCONN_MDI N<3>

GPIO_0
GPIO_1/CR_BUS_PWR
RE*/GPIO_2
TP_ENET_CR_1V8_EN
PP3V3R1V8_ENET_LR_OUT_REG
ENET_MEDIA_SENSE

MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3R1V8_CR_IOPWR_OUT

NOTE: "IPx" == Programmable pull-up/down

SD_DETECT/WE*
ENET_SD_DETECT_L
SD_DETECT can only be used active low due to errata.

CR_CMD/CLE
CR_CLK/RY_BY*
CR_DATA0 CR_DATA1 CR_DATA2 CR_DATA3 CR_DATA4 CR_DATA5 CR_DATA6 CR_DATA7
CE*/MS_INS*
CR_LED/ALE
CR_WP*/XD_WP*
XD_DETECT

ENET_SD_CMD R3961 33 5% 1/20W MF 201 SDCONN_CMD
ENET_SD_CLK R3979 33 5% 1/20W MF 201 SDCONN_CLK
ENET_CR_DATA<0> R3971 33 5% 1/20W MF 201 SDCONN_DATA<0>
ENET_CR_DATA<1> R3972 33 5% 1/20W MF 201 SDCONN_DATA<1>
ENET_CR_DATA<2> R3973 33 5% 1/20W MF 201 SDCONN_DATA<2>
ENET_CR_DATA<3> R3974 33 5% 1/20W MF 201 SDCONN_DATA<3>
ENET_CR_DATA<4> R3975 33 5% 1/20W MF 201 SDCONN_DATA<4>
ENET_CR_DATA<5> R3976 33 5% 1/20W MF 201 SDCONN_DATA<5>
ENET_CR_DATA<6> R3977 33 5% 1/20W MF 201 SDCONN_DATA<6>
ENET_CR_DATA<7> R3978 33 5% 1/20W MF 201 SDCONN_DATA<7>

NC_ENET_CE_L_MS_INS_L NO_TEST=TRUE
No MS (Memory Stick) Insert feature needed.
ENET_CR_PWREN
Control signal to light LED or control SD bus power.
SDCONN_WP
ENET_SR_DISABLE R3981 1K 5% 1/16W MF-LF 402

ENET supports both active-levels for WP.

ENET_CR Signals
BCM requests SD CR[0:7], CMD, CLK termination.

ENET_SR_DISABLE
IF ENET SWITCHING REGULATOR IS USED, THIS PIN SHOULD HAVE A 1K PD TO GND

THRM_PAD

R3965 1.24K 1% 1/16W MF-LF 402

PHY Non-Volatile Memory

ROM contains MAC address, PCIe config info as well as code for Bonjour proxy. Avoids need for EFI to program at startup.
(Required ROM size 1 Mbit)

=PP3V3_S4_ENET_FET
C3990 0.1UF 10% 16V X5R-CERM 0201
U3990
AT45DB011D
SOIC-8S1
OMIT_TABLE
VCC SCK CS* WP* RESET* SI SO GND
ENET_SCLK
ENET_CS_L
ENET_MOSI
ENET_MISO
NOSTUFF
R3990 4.7K 5% 1/16W MF-LF 402
R3997 4.7K 5% 1/16W MF-LF 402

NOTE: Pull-down on SO plus internal pull-ups on other 3 SPI pins configures ENET for the Atmel AT45DB011D (1Mbit) ROM. If a different ROM is used then the straps must change.
NOTE: ENETM requires SI pull-down instead of SO.

SYNC MASTER=D8_MLB
SYNC_DATE=08/27/2012
PAGE TITLE
ETHERNET PHY (CAESAR IV+)

Apple Inc.

DRAWING NUMBER 051-9505
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REVISION 8.0.0
BRANCH prefsb
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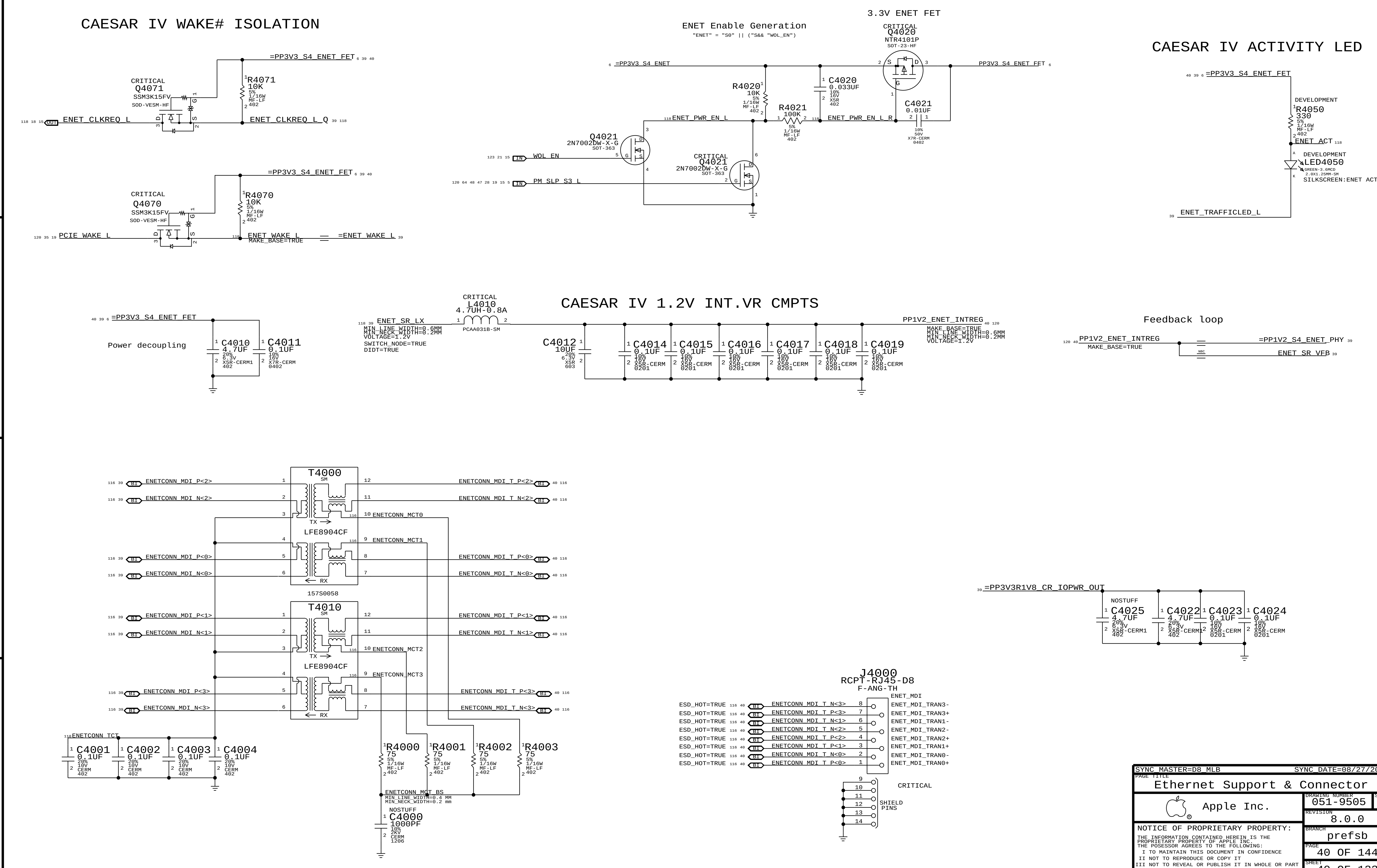
CAESAR IV WAKE# ISOLATION
=PP3V3_S4_ENET_FET
CRITICAL
Q4071
SSM3K15FV
SOD-VESM-HF
R4071
10K
5%
1/16W
MF-LF
402
ENET_CLKREQ_L
ENET_CLKREQ_L_Q
CRITICAL
Q4070
SSM3K15FV
SOD-VESM-HF
R4070
10K
PCIE_WAKE_L
ENET_WAKE_L
MAKE_BASE=TRUE
=ENET_WAKE_L
ENET Enable Generation
"ENET" = "S0" || ("S&& "WOL_EN")
3.3V ENET FET
CRITICAL
Q4020
NTR4101P
SOT-23-HF
=PP3V3_S4_ENET
PP3V3_S4_ENET_FET
R4020
10K
C4020
0.033UF
10%
16V
X5R
402
R4021
100K
C4021
0.01UF
10%
50V
X7R-CERM
0402
ENET_PWR_EN_L
ENET_PWR_EN_L_R
Q4021
2N7002DW-X-G
SOT-363
CRITICAL
Q4021
2N7002DW-X-G
SOT-363
WOL_EN
PM_SLP_S3_L
CAESAR IV ACTIVITY LED
=PP3V3_S4_ENET_FET
DEVELOPMENT
R4050
330
5%
1/16W
MF-LF
402
ENET_ACT
DEVELOPMENT
LED4050
GREEN-3.6MCD
2.0X1.25MM-SM
SILKSCREEN:ENET ACT
ENET_TRAFFICLED_L
CAESAR IV 1.2V INT.VR CMPTS
=PP3V3_S4_ENET_FET
Power decoupling
C4010
4.7UF
20%
6.3V
X5R-CERM1
402
C4011
0.1UF
10%
16V
X7R-CERM
0402
CRITICAL
L4010
4.7UH-0.8A
PCAA031B-SM
ENET_SR_LX
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=1.2V
SWITCH_NODE=TRUE
DIDT=TRUE
PP1V2_ENET_INTREG
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=1.2V
C4012
10UF
20%
6.3V
X5R
603
C4014
0.1UF
C4015
0.1UF
C4016
0.1UF
C4017
0.1UF
C4018
0.1UF
C4019
0.1UF
10%
16V
X5R-CERM
0201
Feedback loop
PP1V2_ENET_INTREG
MAKE_BASE=TRUE
=PP1V2_S4_ENET_PHY
ENET_SR_VFB
T4000
SM
LFE8904CF
157S0058
T4010
SM
LFE8904CF
TX
RX
ENETCONN_MDI_P<2>
ENETCONN_MDI_N<2>
ENETCONN_MDI_P<0>
ENETCONN_MDI_N<0>
ENETCONN_MDI_P<1>
ENETCONN_MDI_N<1>
ENETCONN_MDI_P<3>
ENETCONN_MDI_N<3>
ENETCONN_MDI_T_P<2>
ENETCONN_MDI_T_N<2>
ENETCONN_MDI_T_P<0>
ENETCONN_MDI_T_N<0>
ENETCONN_MDI_T_P<1>
ENETCONN_MDI_T_N<1>
ENETCONN_MDI_T_P<3>
ENETCONN_MDI_T_N<3>
ENETCONN_MCT0
ENETCONN_MCT1
ENETCONN_MCT2
ENETCONN_MCT3
ENETCONN_TCT
C4001
0.1UF
C4002
0.1UF
C4003
0.1UF
C4004
0.1UF
20%
10V
CERM
402
R4000
75
R4001
75
R4002
75
R4003
75
5%
1/16W
MF-LF
402
ENETCONN_MCT_BS
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 mm
NOSTUFF
C4000
1000PF
10%
2KV
CERM
1206
=PP3V3R1V8_CR_IOPWR_OUT
NOSTUFF
C4025
4.7UF
20%
6.3V
X5R-CERM1
402
C4022
4.7UF
C4023
0.1UF
10%
16V
X5R-CERM
0201
C4024
0.1UF
J4000
RCPT-RJ45-D8
F-ANG-TH
ENET_MDI
ESD_HOT=TRUE
ENET_MDI_TRAN3-
ENET_MDI_TRAN3+
ENET_MDI_TRAN1-
ENET_MDI_TRAN2-
ENET_MDI_TRAN2+
ENET_MDI_TRAN1+
ENET_MDI_TRAN0-
ENET_MDI_TRAN0+
CRITICAL
SHIELD
PINS

SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012

PAGE TITLE
Ethernet Support & Connector

Apple Inc.

DRAWING NUMBER 051-9505 SIZE D

REVISION 8.0.0

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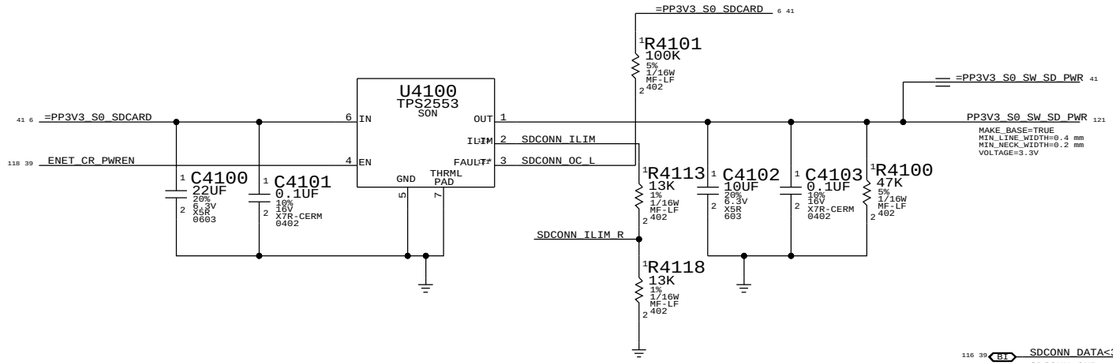
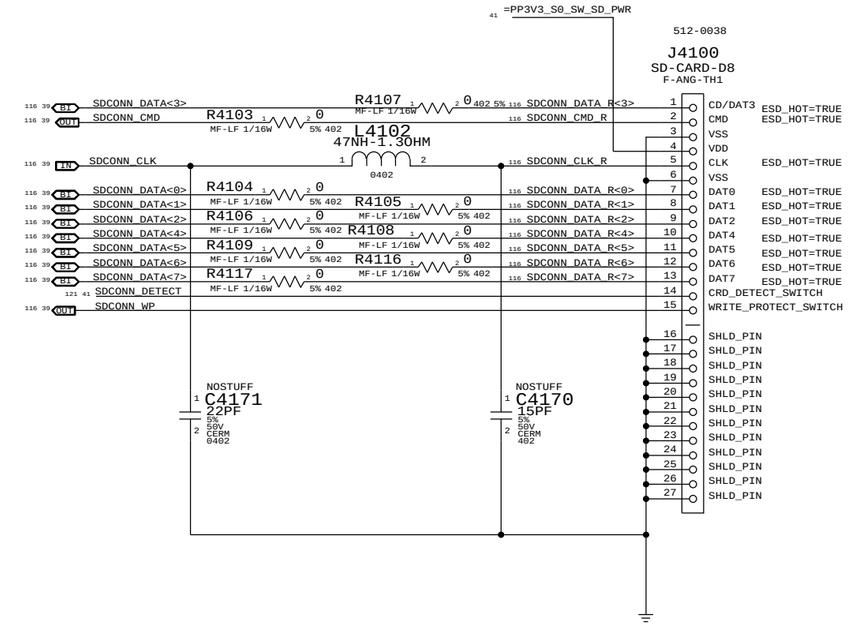
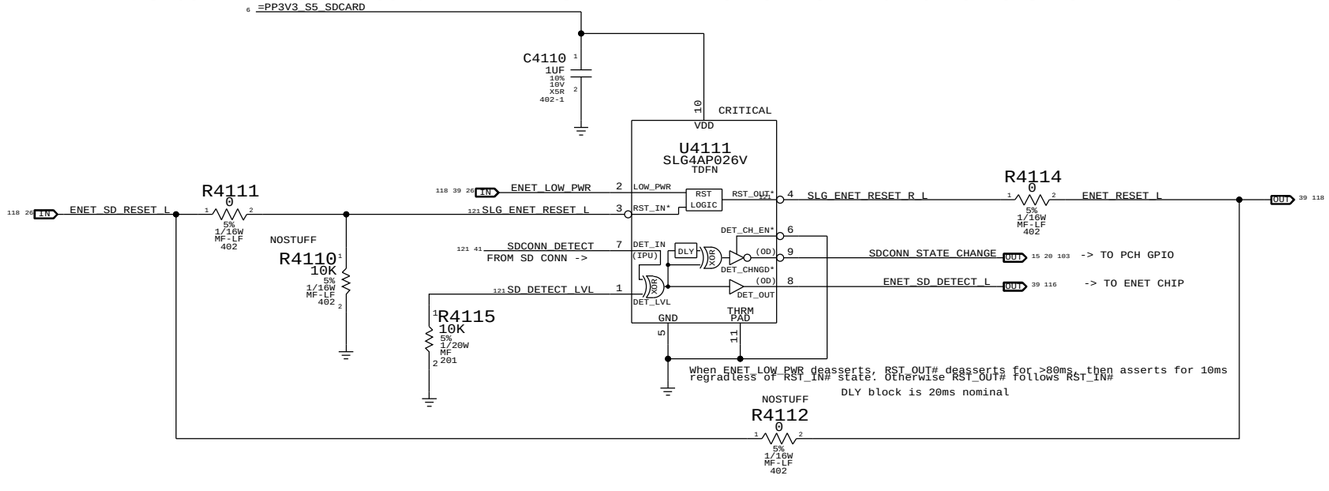
SD CARD 3.3V OVERCURRENT PROTECTION





SDCONN DETECT DEBOUNCE. ENET_RESET AND DETECT-CHANGED PCH GPIO PULSE GENERATION.



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SD READER CONNECTOR

Apple Inc.

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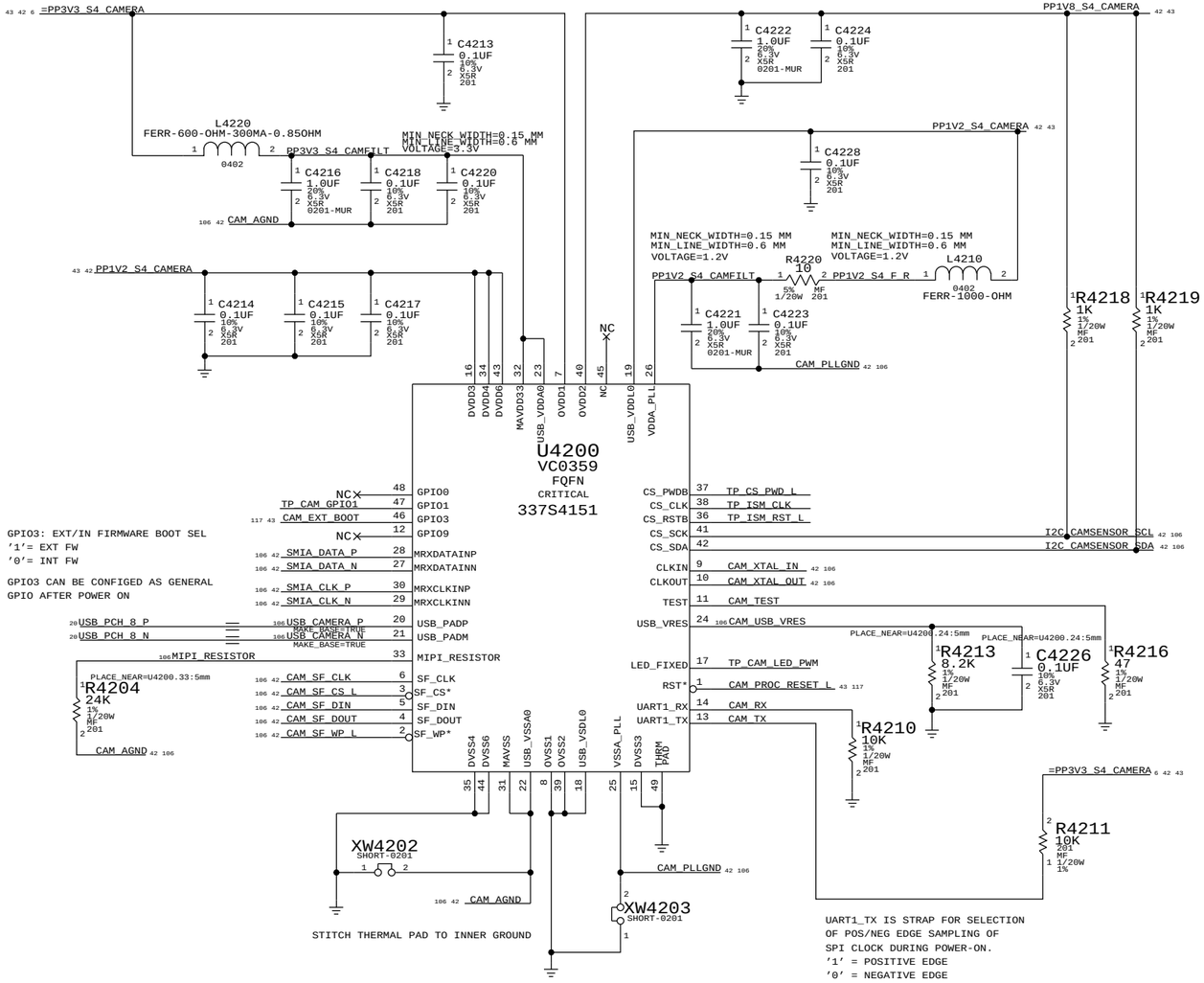
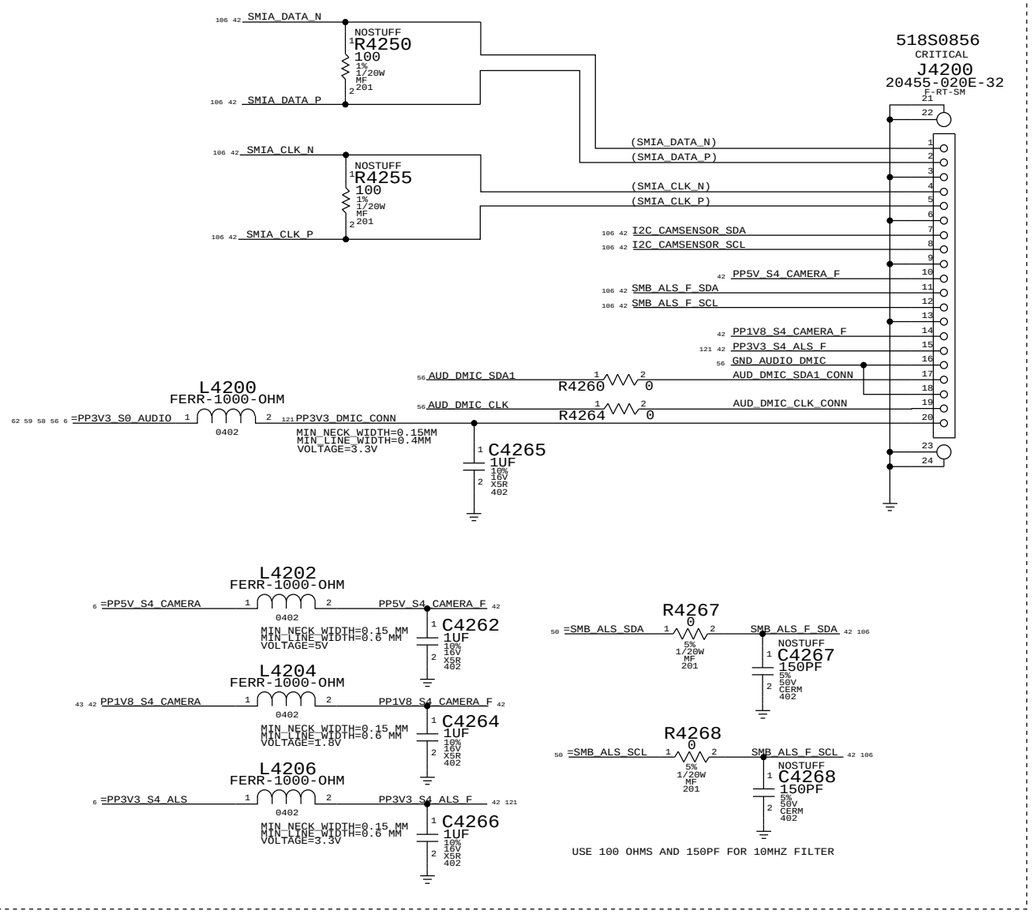
USB CAMERA CONTROLLER



CAMERA/ALS/DMIC CONNECTOR



SYNC_MASTER=D8_MLB	SYNC_DATE=08/27/2012
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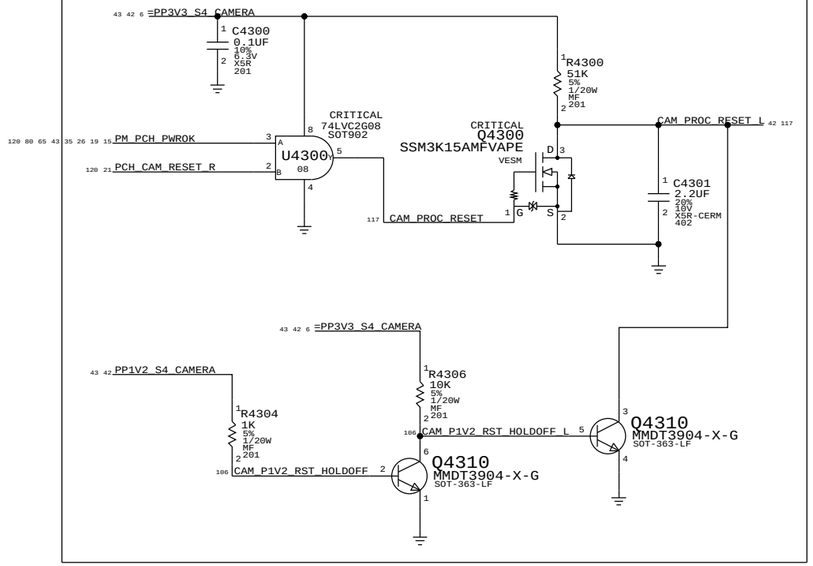
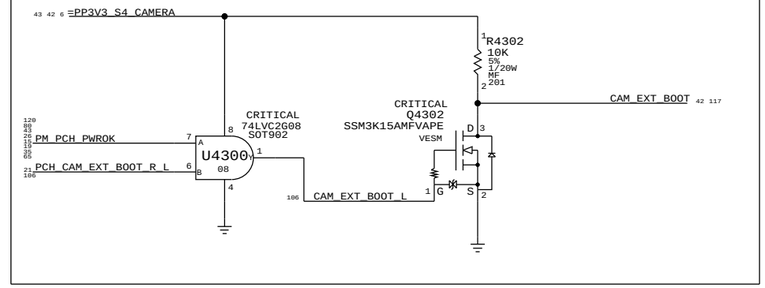
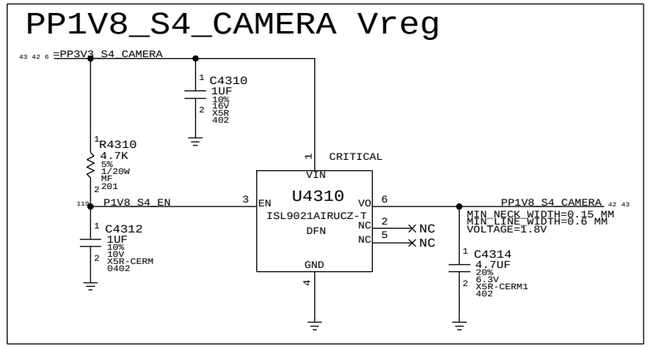
Camera Processor Reset



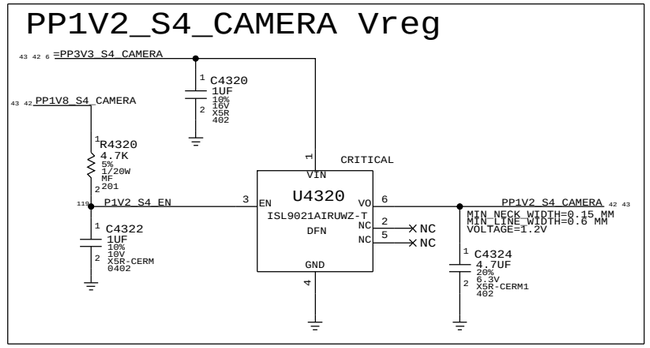
Camera Processor ExtBoot Cntl



PP1V8_S4_CAMERA Vreg



PP1V2_S4_CAMERA Vreg



SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012

PAGE TITLE
Camera Controller Support

Apple Inc.

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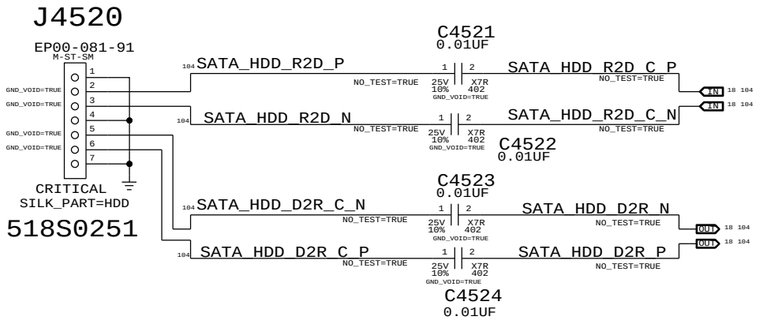
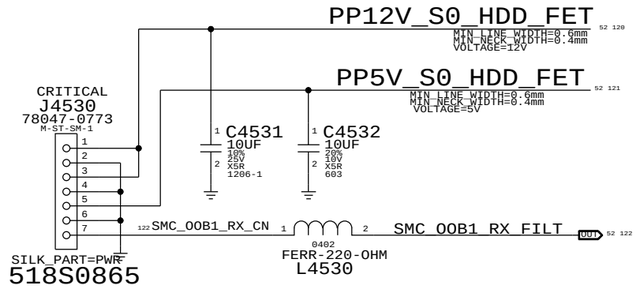
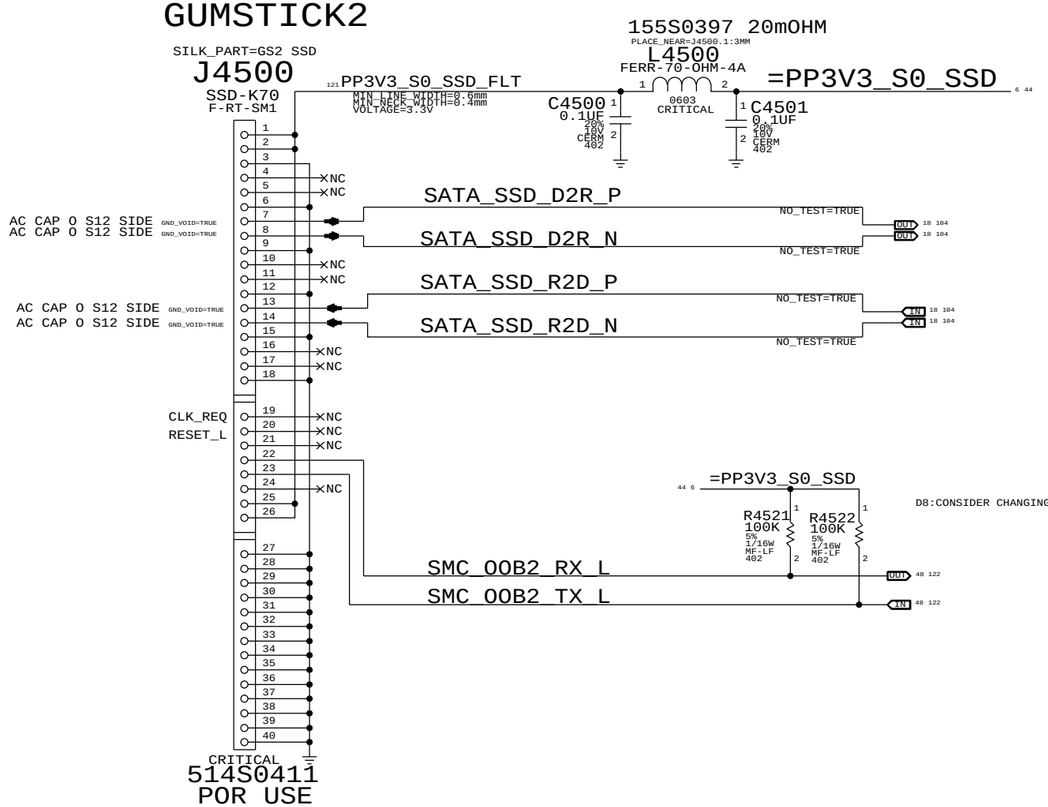
HDD DATA



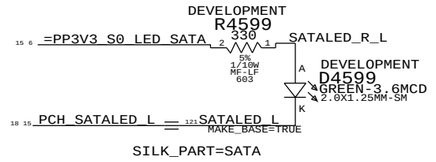
HDD POWER



GUMSTICK2



SATA Activity LED



D8:CONSIDER CHANGING SMC_OOB2_RX/TX_L PULL-UP TO 100K (FROM 10K) RDAR://10817697

SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012

PAGE TITLE: SATA Connectors

Apple Inc.

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USB/SMC DEBUG MUX

EXTERNAL USB PORTS A & B

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=PP5V_S4_USB
C4702 330UF-25MOHM 20% 6.3V TANT CASE-D2E
C4701 0.1UF 20% 10V CERM 402
PLACE_NEAR=U4700.2:2MM

353S3052 CRITICAL
U4700 TPS2561DR SON
IN_0 IN_1 OUT1 OUT2 FAULT1* FAULT2* EN1 EN2 ILIM THRM PAD GND

44 mOHM
3ms Rise Time

USB_EXTD_OC_L
USB_EXTC_OC_L
PM_EN_USB_PWR
USB_EXTCD_ILIM
PLACE_NEAR=U4700.7:2MM
R4702 11.5K 1% 1/16W MF-LF 402
USB_EXTCD_ILIM_R
PLACE_NEAR=R4702.2:2MM
R4703 11.5K 1% 1/16W MF-LF 402
23.2K (1%)
=> 2.19A MIN
=> 2.63A MAX
2x ILIM resistors rdar://11104691

PP5V_S4_EXTD
VOLTAGE=5V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NOSTUFF C4713 10UF 20% 10V X5R 603

=PP3V3_S5_SMC_USBMUX
C4716 0.1UF 20% 10V CERM 402
R4715 10K 5% 1/10W MF-LF 402

U4730 USB3740 DFN 353S3603 CRITICAL
VDD DP_2 DM_2 DP_1 DM_1 OE* S GND DP DM

XHCI
USB_PCH_3_P
USB_PCH_3_N
EHCI
USB_PCH_10_P
USB_PCH_10_N
USB_EXTD_SEL_XHCI
PCH GPIO74

USB2_EXTD_MUXED_P
USB2_EXTD_MUXED_N
NO_TEST=TRUE

155S0367 L4711 FERR-120-OHM-3A 0603
BLM18S121: 25 mOHM
C4715 0.01UF 20% 16V X7R-CERM 0402
C4717 0.1UF 20% 10V CERM 402

PP5V_S4_EXTD_F
VOLTAGE=5V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM

377S0126 CRITICAL
SLP1210N6 RCLAMP0582N D4711
GND VBUS NC D+ D- NC GND

155S0430 CRITICAL L4712 120-OHM-90MA DLP0NS

377S0104 CRITICAL D4712 ESD0P2RF-02LS TSSLP-2-1
377S0104 CRITICAL D4713 ESD0P2RF-02LS TSSLP-2-1

155S0721 CRITICAL L4713 80OHM-25%-100MA L2 L1 0504
155S0721 CRITICAL L4714 80OHM-25%-100MA L2 L1 0504

USB3_EXTD_RX_F_N
USB3_EXTD_RX_F_P
USB3_EXTD_TX_C_N
USB3_EXTD_TX_C_P
USB3_EXTD_TX_N
USB3_EXTD_TX_P
C4718 0.1UF X5R 10% 6.3V 201
C4719 0.1UF X5R 10% 6.3V 201
GND_VOID=TRUE

377S0104 CRITICAL D4714 ESD0P2RF-02LS TSSLP-2-1
377S0104 CRITICAL D4715 ESD0P2RF-02LS TSSLP-2-1

USB3_EXTD_RX_N
USB3_EXTD_RX_P
USB3_EXTD_TX_F_N
USB3_EXTD_TX_F_P
USB2_EXTD_MUXED_F_N
USB2_EXTD_MUXED_F_P

EXT PORT D
514-0842 CRITICAL
J4710 USB-NO4-T86-D8 F-ANG-TH
VBUS D- D+ GND STDA_SSRX- STDA_SSRX+ GND_DRAIN STDA_SSTX- STDA_SSTX+ SHIELD

155S0367 L4701 FERR-120-OHM-3A 0603
BLM18S121: 25 mOHM
C4705 0.01UF 20% 16V X7R-CERM 0402
C4707 0.1UF 20% 10V CERM 402

PP5V_S4_EXTC
VOLTAGE=5V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NOSTUFF C4703 10UF 20% 10V X5R 603

PP5V_S4_EXTC_F
VOLTAGE=5V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM

377S0126 CRITICAL
SLP1210N6 RCLAMP0582N D4701
GND VBUS NC D+ D- NC GND

155S0430 CRITICAL L4702 120-OHM-90MA DLP0NS

377S0104 CRITICAL D4702 ESD0P2RF-02LS TSSLP-2-1
377S0104 CRITICAL D4703 ESD0P2RF-02LS TSSLP-2-1

155S0721 CRITICAL L4703 80OHM-25%-100MA L2 L1 0504
155S0721 CRITICAL L4704 80OHM-25%-100MA L2 L1 0504

USB_PCH_2_P
USB_PCH_2_N
USB3_EXTC_RX_F_N
USB3_EXTC_RX_F_P
USB3_EXTC_TX_C_N
USB3_EXTC_TX_C_P
USB3_EXTC_TX_N
USB3_EXTC_TX_P
C4708 0.1UF X5R 10% 6.3V 201
C4709 0.1UF X5R 10% 6.3V 201
GND_VOID=TRUE

377S0104 CRITICAL D4704 ESD0P2RF-02LS TSSLP-2-1
377S0104 CRITICAL D4705 ESD0P2RF-02LS TSSLP-2-1

USB3_EXTC_RX_N
USB3_EXTC_RX_P
USB3_EXTC_TX_F_N
USB3_EXTC_TX_F_P
USB2_EXTC_F_N
USB2_EXTC_F_P
NO_TEST=TRUE

EXT PORT C
514-0841 CRITICAL
J4700 USB-NO3-T86-D8 F-ANG-TH
VBUS D- D+ GND STDA_SSRX- STDA_SSRX+ GND_DRAIN STDA_SSTX- STDA_SSTX+ SHIELD

SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012
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EXTERNAL USB PORTS C & D
Apple Inc.
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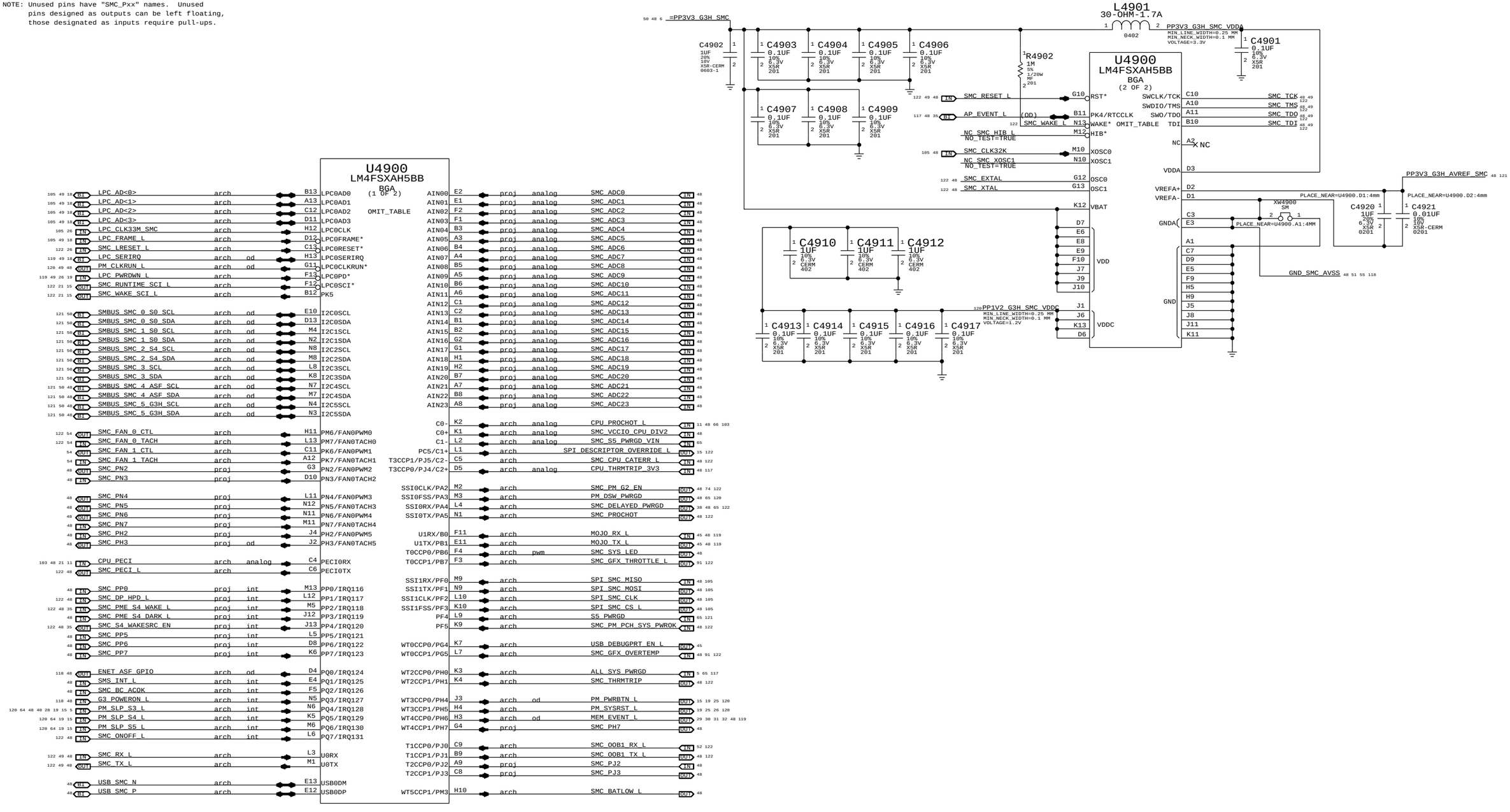
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.



SYNC_MASTER=D8_MLB	SYNC_DATE=08/27/2012
PAGE TITLE	SMC
Apple Inc.	DRAWING NUMBER 051-9505 · SIZE D
	REVISION 8.0.0
	BRANCH prefsb
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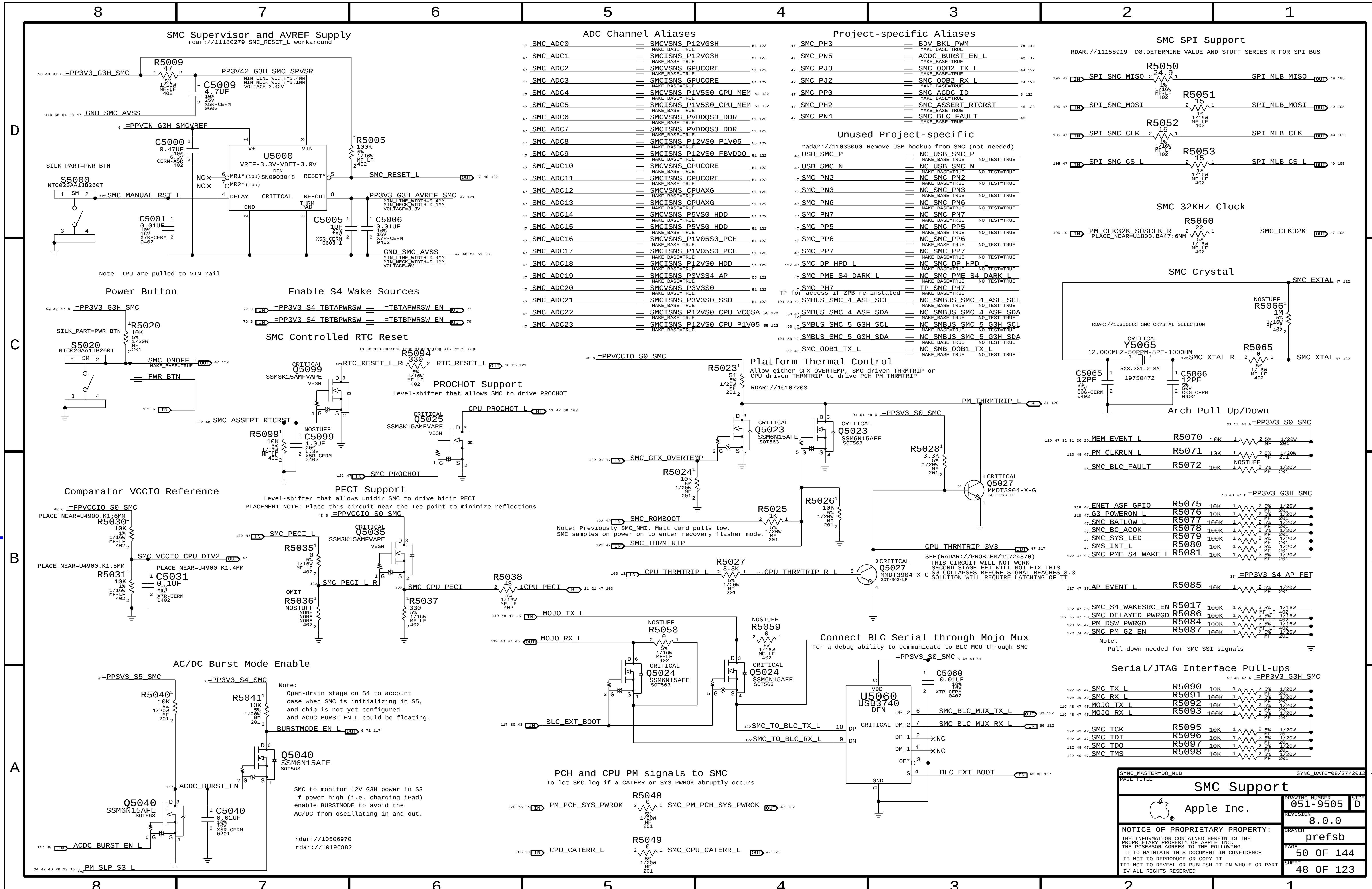

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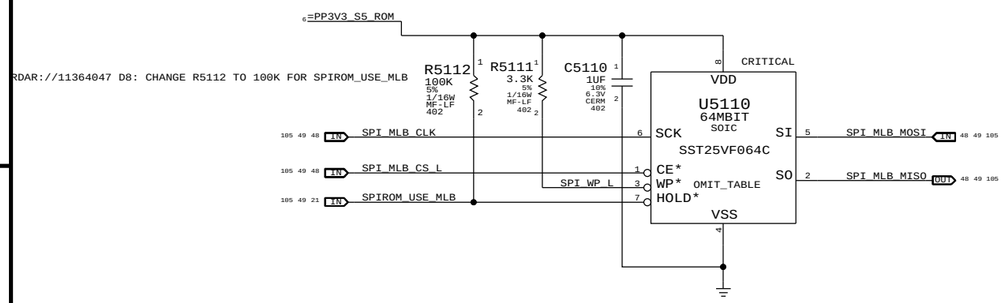
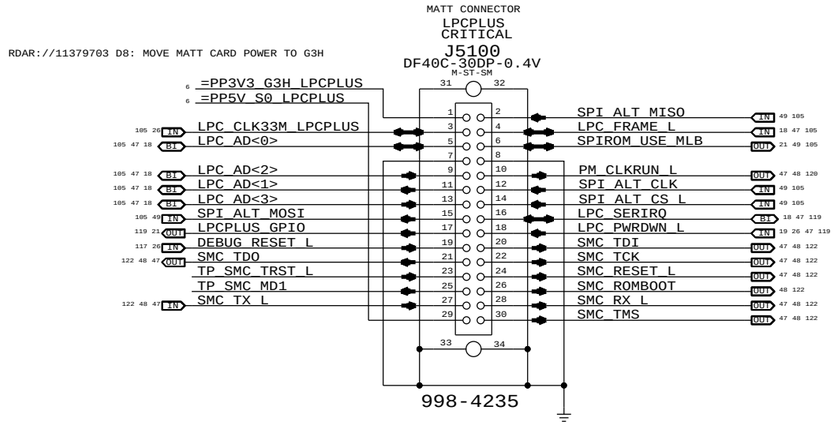
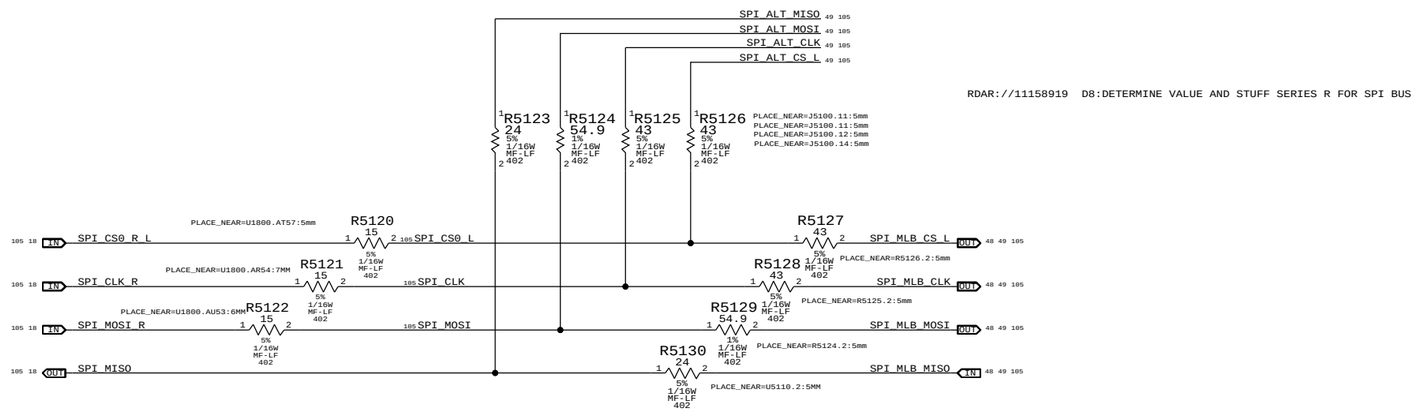
SPI BootROM



LPC+SPI Connector



SPI Series Termination



SYNC_MASTER=D8_MLB	SYNC_DATE=08/27/2012
PAGE TITLE	SPI and Debug Connector
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=PP3V3_S0_SMBUS_SMC

R5200 2.2K 5% 1/16W MF-LF 402
R5201 2.2K 5% 1/16W MF-LF 402

U4900
SMC (SMBus 0)
SMBUS_SMC_0_S0_SCL MAKE_BASE=TRUE
SMBUS_SMC_0_S0_SDA MAKE_BASE=TRUE

U5500
Temp Sensors "T1"
=SMB_SNS1_SCL
=SMB_SNS1_SDA
U5500 EMC1414-1: 0x98 Write 0x99 Read

GK107:U8000 / GK104:UA000
GPU die temp
GPU_SMB_CLK_R
GPU_SMB_DAT_R
0x9E Write 0x9F Read

U5590
LCD remote IR temp
=SMB_SNS3_SCL
=SMB_SNS3_SDA
0x8A Write 0x8B Read

R5202 0 5% 1/16W MF-LF 402
R5203 0 5% 1/16W MF-LF 402

U1800
PCH (SMLink 1)
SML_PCH_1_CLK
SML_PCH_1_DATA
0x88 Write 0x89 Read
PCH PECI sensor data

=PP3V3_S0_SMBUS_SMC

R5210 2.2K 5% 1/16W MF-LF 402
R5211 2.2K 5% 1/16W MF-LF 402

U4900
SMC (SMBus 1)
SMBUS_SMC_1_S0_SCL MAKE_BASE=TRUE
SMBUS_SMC_1_S0_SDA MAKE_BASE=TRUE

U5550
Temp Sensors "T2"
=SMB_SNS2_SCL
=SMB_SNS2_SDA
U5550 EMC1428-7: 0x92 Write 0x93 Read

J9500
Display TCon slave
=I2C_TCON_SLA_SCL
=I2C_TCON_SLA_SDA
TMP421: 0x9E Write 0x9F Read
Panel/Vendor ID: 0x1A Write 0x1B Read

=PP3V3_S4_SMBUS_SMC

R5220 2.2K 5% 1/16W MF-LF 402
R5221 2.2K 5% 1/16W MF-LF 402

U4900
SMC (SMBus 2)
SMBUS_SMC_2_S4_SCL MAKE_BASE=TRUE
SMBUS_SMC_2_S4_SDA MAKE_BASE=TRUE

J4200
Ambient Light Sensor
=SMB_ALS_SCL
=SMB_ALS_SDA
0x52 Write 0x53 Read

=PP3V3_S0_SMBUS_SMC

NOSTUFF R5230 4.7K 5% 1/16W MF-LF 402
NOSTUFF R5231 4.7K 5% 1/16W MF-LF 402

U4900
SMC (SMBus 3)
SMBUS_SMC_3_SCL
SMBUS_SMC_3_SDA

NOSTUFF R5232 0 5% MF-LF 402 1/16W
NOSTUFF R5233 0 5% MF-LF 402 1/16W

SMC SMBus 3 is reserved for SMC/PCH multi-master experiment

=PP3V3_S0_SMBUS_SMC

NOSTUFF R5240 4.7K 5% 1/16W MF-LF 402
NOSTUFF R5241 4.7K 5% 1/16W MF-LF 402

U4900
SMC (SMBus 4)
SMBUS_SMC_4_ASF_SCL
SMBUS_SMC_4_ASF_SDA

SMC SMBus 4 is unused (reserved for ethernet LOM)

=PP3V3_G3H_SMC

NOSTUFF R5250 4.7K 5% 1/16W MF-LF 402
NOSTUFF R5251 4.7K 5% 1/16W MF-LF 402

U4900
SMC (SMBus 5)
SMBUS_SMC_5_G3H_SCL
SMBUS_SMC_5_G3H_SDA

SMC SMBus 5 is unused

=PP3V3_S0_SMBUS_TCON

R5280 2.2K 5% 1/16W MF-LF 402
R5281 2.2K 5% 1/16W MF-LF 402

J9500
Display TCon master
I2C_TCON_MAS_SCL
I2C_TCON_MAS_SDA

R5282 0 5% MF-LF 402 1/16W
R5283 0 5% MF-LF 402 1/16W

U9700
Backlight Controller
SMB_TCON_BLC_SCL
SMB_TCON_BLC_SDA
0x6E Write 0x6F Read

D8 TCon has 2.2K pullup
K62 TCon has 4.7K pullup

=PP3V3_S0_SMBUS

R5260 2.2K 5% 1/16W MF-LF 402
R5261 2.2K 5% 1/16W MF-LF 402

U1800
PCH (SMBus)
SMBUS_PCH_CLK MAKE_BASE=TRUE
SMBUS_PCH_DATA MAKE_BASE=TRUE

J2900 & J3000
Memory Channel A
=I2C_SODIMMA_SCL
=I2C_SODIMMA_SDA
DIMM 0: 0xA0 Write 0xA1 Read
DIMM 2: 0xA2 Write 0xA3 Read

J3100 & J3200
Memory Channel B
=I2C_SODIMMB_SCL
=I2C_SODIMMB_SDA
DIMM 1: 0xA4 Write 0xA5 Read
DIMM 3: 0xA6 Write 0xA7 Read

U3400
VRef DACs
=I2C_VREFDACS_SCL
=I2C_VREFDACS_SDA
0x98 Write 0x99 Read

U3401
Vref Control
=I2C_PCA9557D_SCL
=I2C_PCA9557D_SDA
0x30 Write 0x31 Read

U6500
China Headset
=I2C_CHS_SCL
=I2C_CHS_SDA
0x76 Write 0x77 Read

U6551
Mikey
=I2C_MIKEY_SCL
=I2C_MIKEY_SDA
0x72 Write 0x73 Read

=PP3V3_S4_SMBUS

R5270 8.2K 5% 1/16W MF-LF 402
R5271 8.2K 5% 1/16W MF-LF 402

U1800
PCH (SMLink 0)
SML_PCH_0_CLK
SML_PCH_0_DATA
PCH SMLink 0 is unused

=PP3V3_TBTLC_RTR

radar://11669665

TBT I2C will not be used in D8
0-ohm not stuffed and pullups stuffed
addresses in 0b11111XXX are "reserved"

R5268 3.3K 5% 1/16W MF-LF 402
R5269 3.3K 5% 1/16W MF-LF 402

U3600
Thunderbolt Router
I2C_TBTRTR_SCL
I2C_TBTRTR_SDA
0xFF Write 0xFE Read
I2C can be used as alternative to JTAG

NOSTUFF R5266 0 5% MF-LF 402 1/16W
NOSTUFF R5267 0 5% MF-LF 402 1/16W

=PP3V3_S0_SMBUS

NOSTUFF R5264 0 5% 1/16W MF-LF 402
NOSTUFF R5265 0 5% 1/16W MF-LF 402
NOSTUFF R5274 2.2K 5% 1/16W MF-LF 402
NOSTUFF R5275 2.2K 5% 1/16W MF-LF 402

J2500 & J2550
XDP
SMBUS_PCH_CLK_R MAKE_BASE=TRUE
SMBUS_PCH_DATA_R MAKE_BASE=TRUE
=SMBUS_XDP_SCL
=SMBUS_XDP_SDA
0x94 Write 0x95 Read

radar://11710650
XDP disconnected from I2C bus to reduce load

SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012

PAGE TITLE
SMBus Connections

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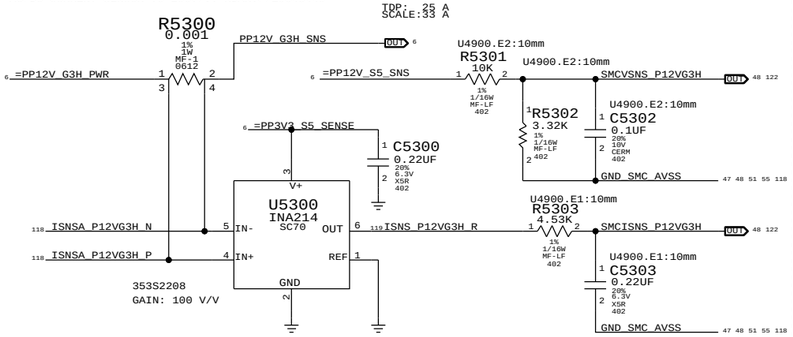
ADC 0/1 12V G3H (ID2R/VD2R)

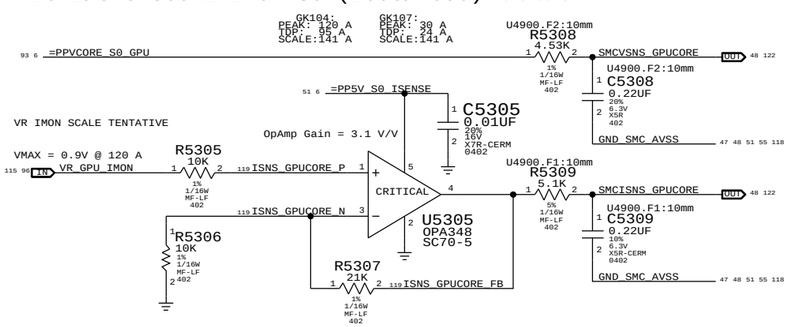
AC/DC lowside sense (System total)

AC/DC CURRENT SENSOR TO 100V/V: RDAR://10645440



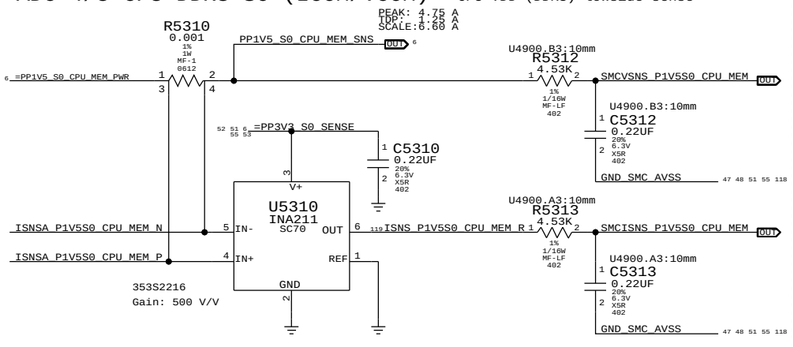
ADC 2/3 GPUCORE IMON S0 (IG0C/VG0C)

GPU Core



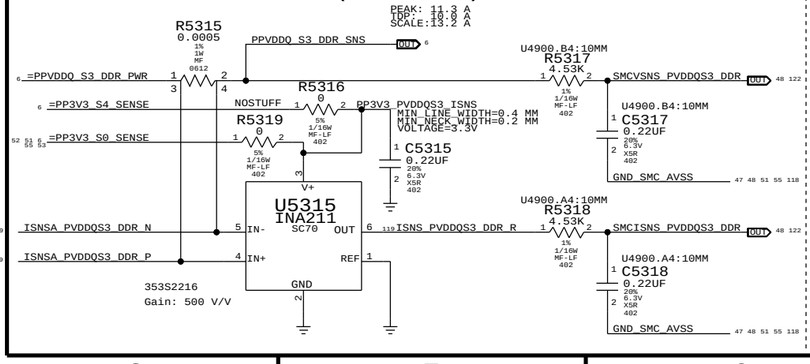
ADC 4/5 CPU DDR3 S0 (IC0M/VC0M)

CPU VDD (DDR3) lowside sense



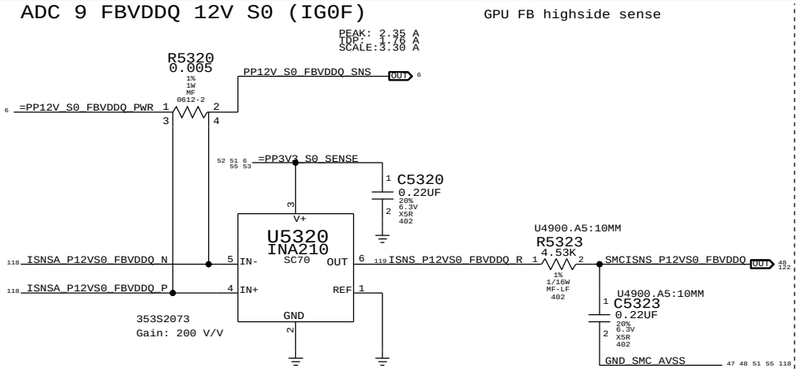
ADC 6/7 SODIMM DDR3 S3 (IM0R/VM0R)

DIMM 1.5V lowside sense



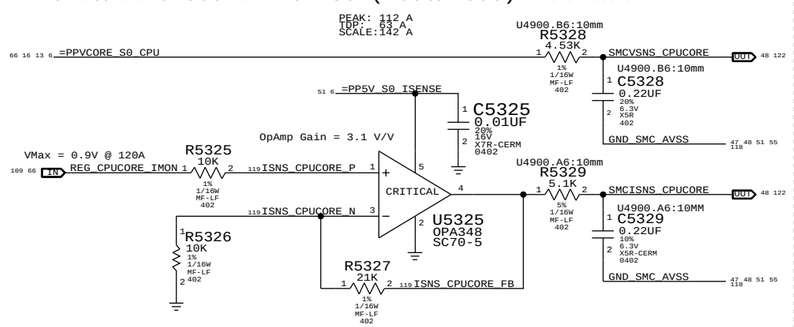
ADC 9 FBVDDQ 12V S0 (IG0F)

GPU FB highside sense



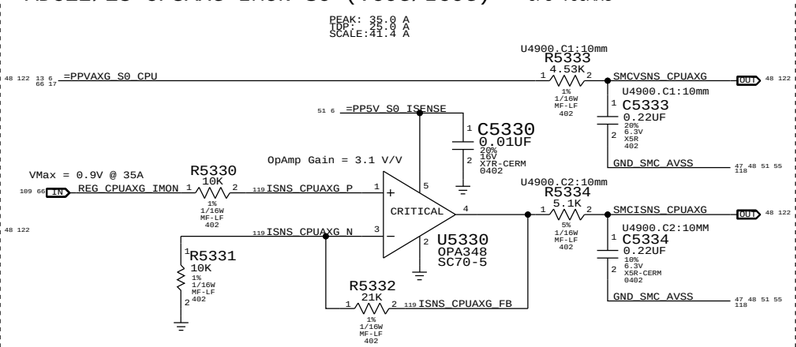
ADC 10/11 CPUCORE IMON S0 (VC0C/IC0C)

CPU VCCore



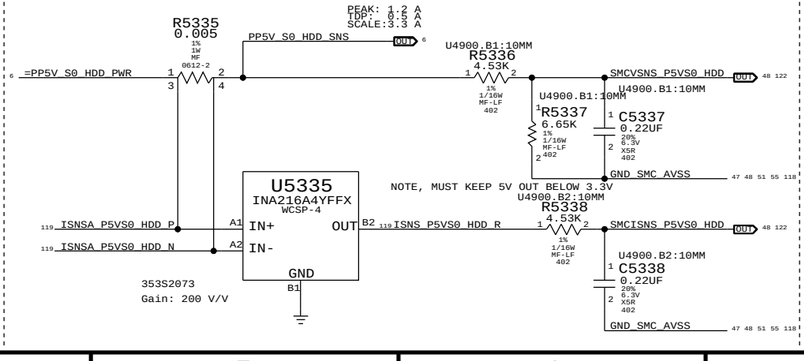
ADC12/13 CPUAXG IMON S0 (VC0G/IC0G)

CPU VCCAXG



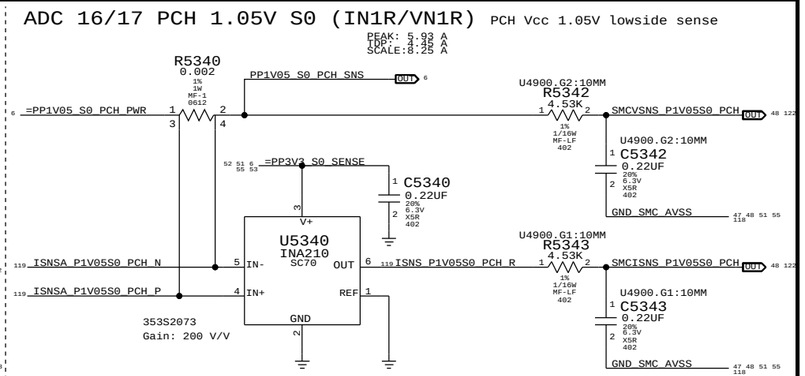
ADC14/15 HDD 5V S0 (VH05/IH05)

Highside sense for HDD 5V



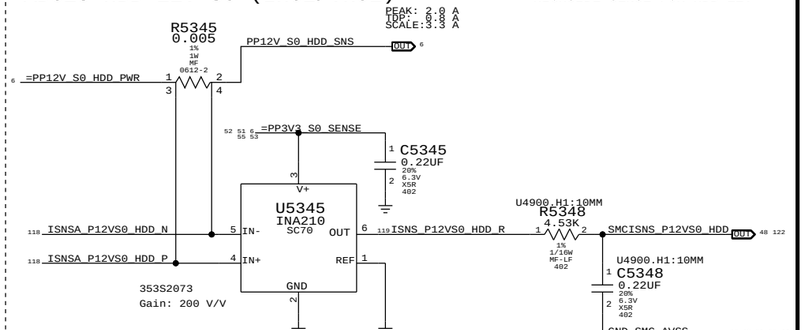
ADC 16/17 PCH 1.05V S0 (IN1R/VN1R)

PCH Vcc 1.05V lowside sense



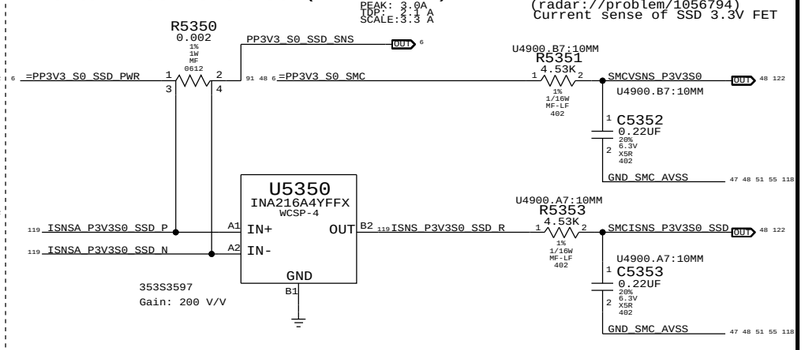
ADC18 HDD 12V S0 (IH02/VH02)

HIGHSIDE SENSE FOR HDD 12V



ADC20/21 SSD 3.3V S0 (IH1R/VR3R)

Voltage sense of 3.3V S0
(radar://problem/1056794)
Current sense of SSD 3.3V FET



SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012

PAGE TITLE: I and V Sense 1

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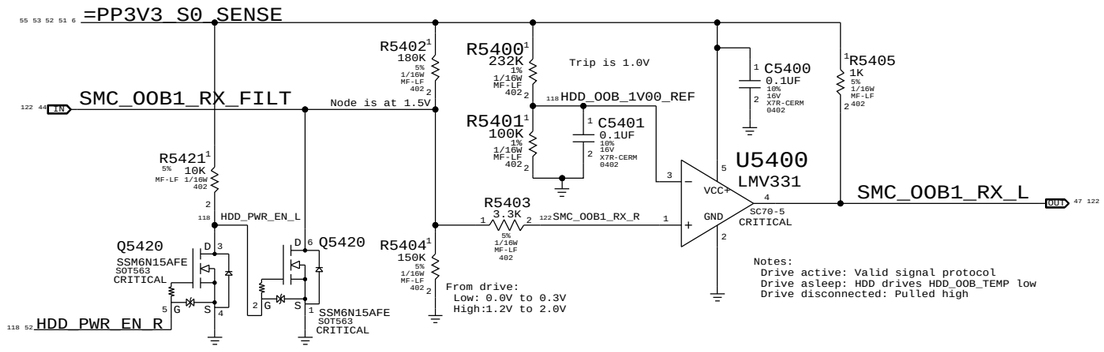
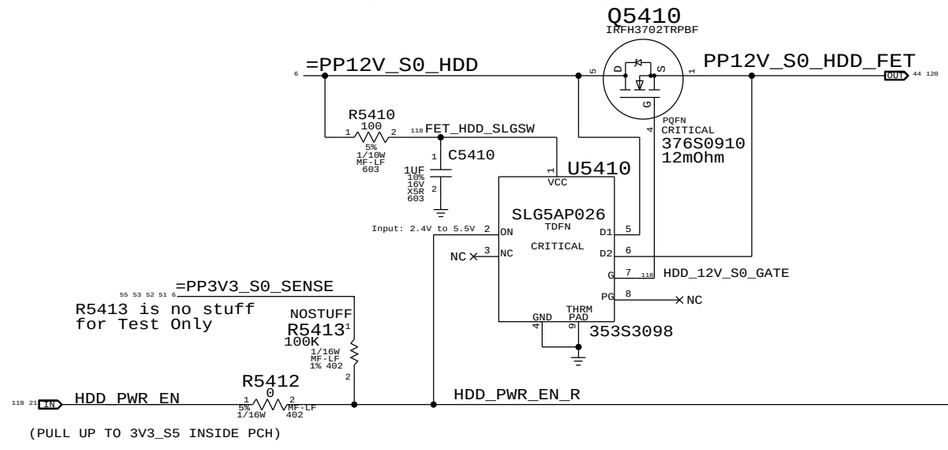
HDD Out-of-Band Temp Sensing

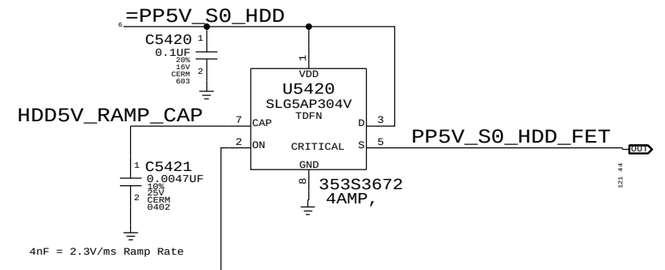
Temperature read from SATA power connecter pin 11



HDD 12V_S0 FET (max 2.8A,ave 0.6A)



HDD 5V_S0 FET (max 0.7A,ave 0.3A)



REMOVE R5413 AND SHORT R5412 AFTER HDD_PWR_EN WORKS

SYNC-MASTER=D8-MLB- - - - - - - - - - - - SYNC-DATE=08/27/2012

PAGE TITLE: HDD/SSD Temp Sense

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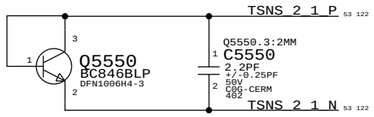
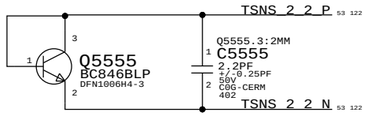
Temperature Sensor T2 EMC1428: Near GPU VR

GPU Proximity



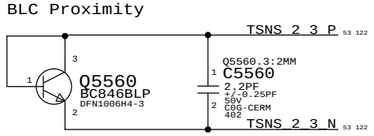
PLACEMENT_NOTE=Place Q5550 near GPU and GDDR5

Ambient



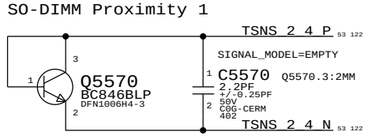
PLACEMENT_NOTE=Place Q5555 near bottom of board

BLC Proximity



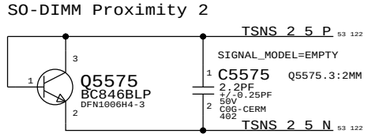
PLACEMENT_NOTE=Place Q5560 near BLC VR

SO-DIMM Proximity 1



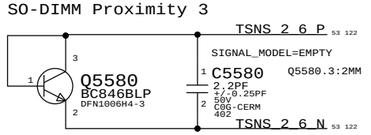
PLACEMENT_NOTE=Place Q5570 near SO-DIMM connectors (top left)

SO-DIMM Proximity 2



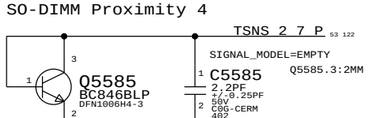
PLACEMENT_NOTE=Place Q5575 near SO-DIMM connectors (top right)

SO-DIMM Proximity 3



PLACEMENT_NOTE=Place Q5580 near SO-DIMM connectors (bottom left)

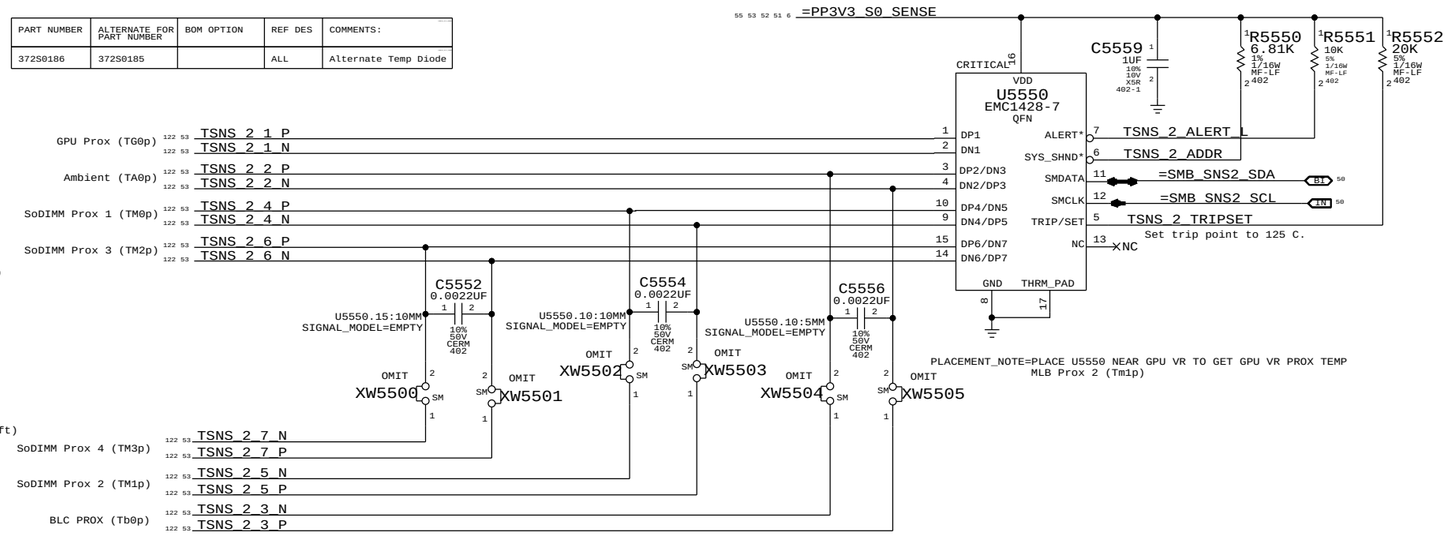
SO-DIMM Proximity 4



PLACEMENT_NOTE=Place Q5585 near SO-DIMM connectors (bottom right)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
372S0186	372S0185		ALL	Alternate Temp Diode

SNS T2: TEMP SENSOR IC

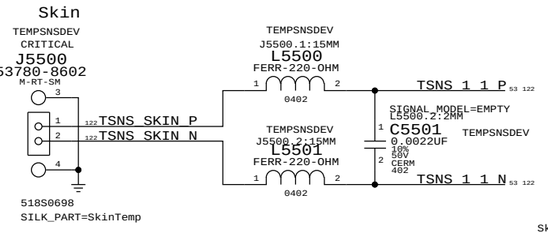


PLACEMENT_NOTE=PLACE U5550 NEAR GPU VR TO GET GPU VR PROX TEMP
MLB Prox 2 (Tm1p)

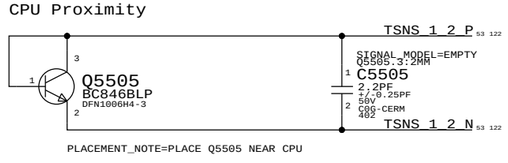
EMC1428-7: 6.8K PULL UP: I2C ADDRESS: WRITE: 0x92, READ: 0x93

Temperature Sensor T1 EMC1414: Near PSU Conn

Skin



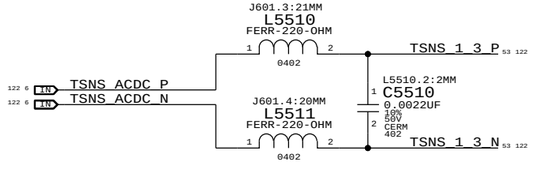
CPU Proximity

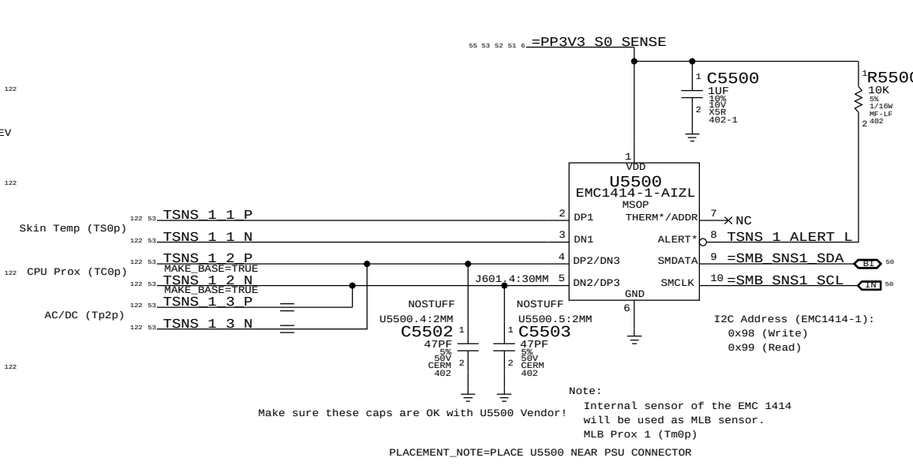


PLACEMENT_NOTE=PLACE Q5505 NEAR CPU

AC/DC

Via connector to diode inside PSU





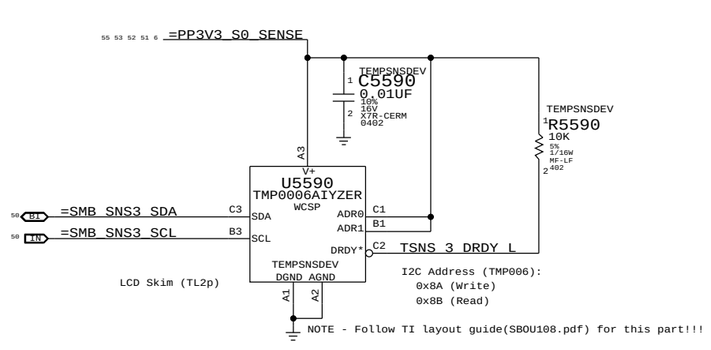
I2C Address (EMC1414-1):
0x98 (Write)
0x99 (Read)

Make sure these caps are OK with U5500 Vendor!

Note:
Internal sensor of the EMC 1414
will be used as MLB sensor.
MLB Prox 1 (Tm0p)

PLACEMENT_NOTE=PLACE U5500 NEAR PSU CONNECTOR

Temperature Sensor T3: LCD Remote Sensor(Dev4Now)



I2C Address (TMP006):
0x8A (Write)
0x8B (Read)

NOTE - Follow TI layout guide(SBOU108.pdf) for this part!!!

SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012

PAGE TITLE: Temperature Sensors

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DRAWING NUMBER: 051-9505 SIZE: D
REVISION: 8.0.0
BRANCH: prefsb
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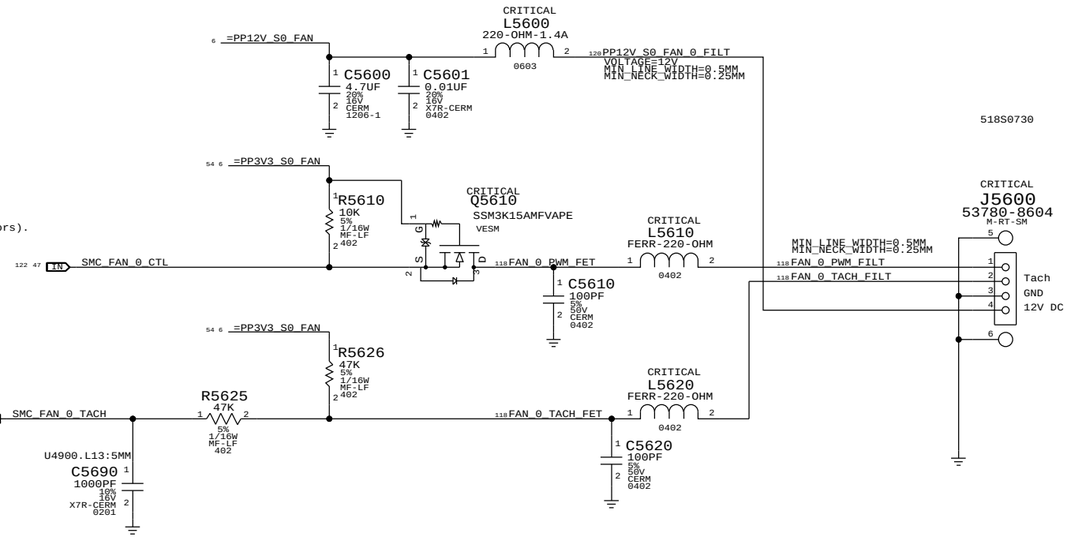
SMC Fan 0 (System)

Note:
The circuit for the PWM input to the fan acts as a non-inverting level-shifter to protect the SMC. It is assumed there is a pull-up to 5V/12V inside the fan, otherwise when the SMC PWM goes low and Q5610 turns on, there would be 5V/12V present on the SMC pin! Then by definition, the drain of Q5610 is at common and the SMC sinks current when Q5610 is on.

This resembles an open-drain if there is a pull-up, going to a Hi-Z FET input.

Otherwise, this is simply a pass-FET.
See RADAR: 10565825- D7: Need scematic and PCB file of fan(All Vendors).



SMC Fan 1 (Unused)

47 IN SMC_FAN_1_CTL — NC_SMC_FAN_1_CTL
MAKE_BASE=TRUE NO_TEST=TRUE

47 OUT SMC_FAN_1_TACH — NC_SMC_FAN_1_TACH
MAKE_BASE=TRUE NO_TEST=TRUE

SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012

PAGE TITLE
System Fan

Apple Inc.

DRAWING NUMBER 051-9505 SIZE D
REVISION 8.0.0
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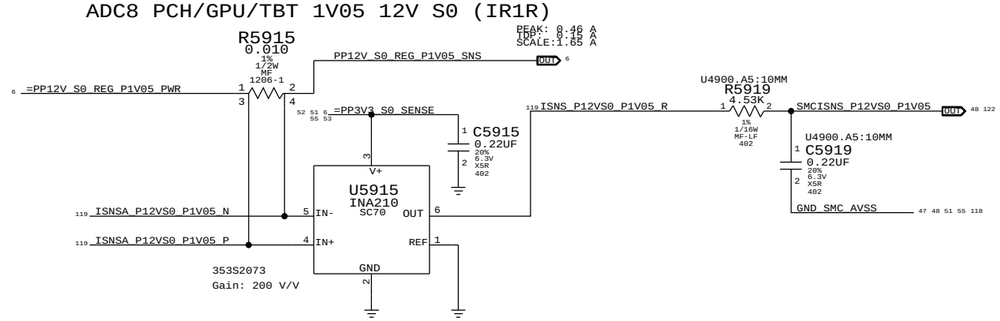
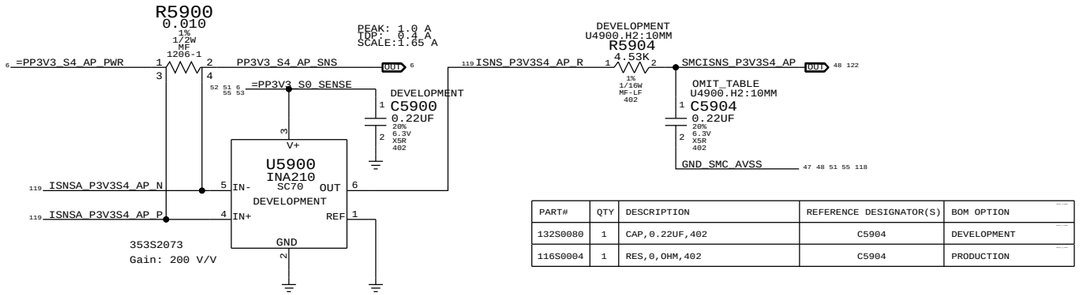
ADC8 PCH/GPU/TBT 1V05 12V S0 (IR1R)



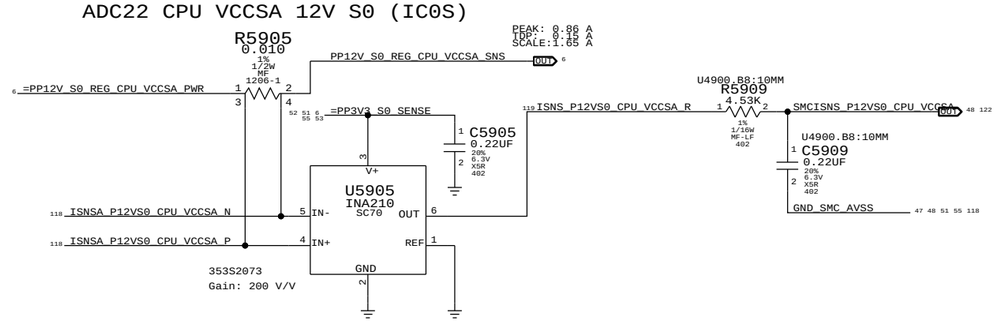
ADC19 AP 3.3V S4 (IW0R)

Current sense of AP 3.3V FET

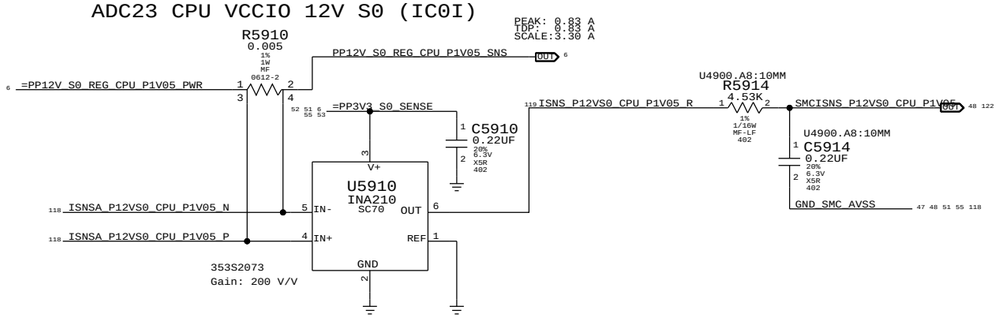


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
132S0080	1	CAP,0.22UF,402	C5904	DEVELOPMENT
116S0004	1	RES,0,OHM,402	C5904	PRODUCTION

ADC22 CPU VCCSA 12V S0 (IC0S)



ADC23 CPU VCCIO 12V S0 (IC0I)



SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012

PAGE TITLE: I and V Sense 2

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DRAWING NUMBER: 051-9505 SIZE: D

REVISION: 8.0.0

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AUDIO CODEC

APPLE P/N 353S2592

PLACE C6200 AS CLOSE TO PIN 9 AS POSSIBLE

VD MUST BE LESS THAN OR EQUAL TO VL_HD

=PP1V5_S0_AUD_DIG

C6101 4.7UF 20% 4V X5R-1 402

C6100 0.47UF 10% 10V X5R 0402

C6108 10UF 20% 16V POLY-TANT CASE-B2-SM

GND_AUDIO_CODEC

PP4V5_AUDIO_ANALOG

R6100 2.67K 1% 1/16W MF-LF 402

C6109 2.2UF 20% 6.3V CERM 402-LF

C6110 2.2UF 20% 6.3V CERM 402-LF

VBIAS_DAC

CS4206_FP

CS4206_FN

C6102 0.47UF 10% 10V X5R 0402

C6103 10UF 20% 16V POLY-TANT CASE-B2-SM

C6105 1UF 10% 10V X5R 402-1

C6104 0.47UF 10% 10V X5R 0402

C6106 0.47UF 10% 10V X5R 0402

CRITICAL C6107 10UF 20% 10V X5R-CERM 0402-1

PP5V_AUDIO_HPAMP

=PP3V3_S0_AUDIO

PP4V5_AUDIO_ANALOG

GND_AUDIO_CODEC

R6105 0 5% 1/16W MF-LF 402

CRITICAL U6101 CS4206B QFN

VD	9				
VA_REF	24				
VA_HP	46				
VA	25				
VBIAS_DAC	29				
VHP_FILT+	44				
VHP_FILT-	41				
GPIO0/DMIC_SDA1	2	LINEOUT_L1+	35	AUD_LO1_L_P	
GPIO1/DMIC_SDA2/SPDIF_OUT2	12	LINEOUT_L1-	34	AUD_LO1_L_N	
GPIO2	14	LINEOUT_R1+	36	AUD_LO1_R_P	
GPIO3	15	LINEOUT_R1-	37	AUD_LO1_R_N	
SENSE_A	13	LINEOUT_L2+	31	AUD_LO2_L_P	
		LINEOUT_L2-	30	AUD_LO2_L_N	
		LINEOUT_R2+	32	AUD_LO2_R_P	
		LINEOUT_R2-	33	AUD_LO2_R_N	
FLYP	45				
FLYC	43				
FLYN	42				
VL_HD	3				
VL_IF	1				
BITCLK	6				
SYNC	10				
SDI	8				
SDO	5				
RESET*	11				
SPDIF_IN	47				
SPDIF_OUT	48				
DGND	7				
THRM_PAD	49				
AGND	26				
HPOUT_L	38	MIN_LINE_WIDTH=0.1MM MIN_NECK_WIDTH=0.1MM		TP_AUD_HP_L	NC
HPOUT_R	40	MIN_LINE_WIDTH=0.1MM MIN_NECK_WIDTH=0.1MM		TP_AUD_HP_R	NC
HPREF	39	MIN_LINE_WIDTH=0.2MM MIN_NECK_WIDTH=0.1MM		CS4206_HPREF	
MICBIAS	16			AUD_CODEC_MICBIAS	
VCOM	28	CS4206_VCOM MIN_LINE_WIDTH=0.20MM MIN_NECK_WIDTH=0.15MM			
LINEIN_L+	21	NO_TEST=TRUE		NC_AUD_LI_P_L	NC
LINEIN_C-	22	NO_TEST=TRUE		NC_AUD_LI_COM	NC
LINEIN_R+	23	NO_TEST=TRUE		NC_AUD_LI_P_R	NC
MICIN_L+	18			AUD_MIC_INL_P	
MICIN_L-	17			AUD_MIC_INL_N	
MICIN_R+	19	NO_TEST=TRUE		NC_AUD_MIC_INP_R	NC
MICIN_R-	20	NO_TEST=TRUE		NC_AUD_MIC_INN_R	NC
VREF+_ADC	27	CS4206_VREF_ADC NC MIN_LINE_WIDTH=0.20MM MIN_NECK_WIDTH=0.15MM			
DMIC_SCL	4			CS4206_DMIC_SCL	

HP AMP/LINE OUT

TWEETERS

RESERVE SPACE FOR POSSIBLE LATCH CIRCUIT

WOOFERS

DMICS 1 & 2 — AUD_DMIC_SDA1

HP AMP CNTRL — AUD_GPIO_2

NC — TP_AUD_GPIO_1

MAC SPKR AMP CNTRL — AUD_CODEC_MICBIAS

D6100 SOD-523 BAT54XV2T1

WIN SPKR AMP CNTRL — AUD_GPIO_3

AUD_SENSE_A

CS4206_FLYP

CS4206_FLYC

C6111 2.2UF 20% 6.3V CERM 402-LF

C6112 2.2UF 20% 6.3V CERM 402-LF

CS4206_FLYN

PLACE TP FOR ALL HDA SIGNALS NEAR CODEC

HDA_BIT_CLK

HDA_SYNC

HDA_SDIN0

R6101 22 5% 1/16W MF-LF 402 — AUD_SDI_R

HDA_SDOUT

HDA_RST_L

DP_INT_SPDIF_AUDIO

AUD_SPDIF_OUT

R6102 22 5% 1/16W MF-LF 402 — AUD_SPDIF_CHIP

R6103 100K 1% 1/16W MF-LF 402

DMICS SHOULD HAVE OWN GND ON CONNECTOR SHARED WITH CAMERA

XW6100

GND_AUDIO_DMIC MIN_LINE_WIDTH=0.20MM MIN_NECK_WIDTH=0.15MM VOLTAGE=0V

GND_AUDIO_CODEC

R6104 22 5% 1/16W MF-LF 402 — AUD_DMIC_CLK

CRITICAL C6113 1UF 10% 25V TANT CASE-P3-HF

CRITICAL C6114 10UF 20% 16V POLY-TANT CASE-B2-SM

C6115 0.47UF 10% 10V X5R 0402

DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
127S0134	127S0111		C6113	THAILAND ALTERNATE

DEVEL_AUDIO CRITICAL Q6170 DMC2400UV SOT563

Q6170_P_S — R6170 0 5% 1/16W MF-LF 402 — Q6170_P_G

Q6170_N_G — R6171 0 5% 1/16W MF-LF 402 — Q6170_N_S

DEVEL_AUDIO CRITICAL Q6171 DMC2400UV SOT563

Q6171_P_S — R6172 0 5% 1/16W MF-LF 402 — Q6171_P_G

Q6171_N_G — R6173 0 5% 1/16W MF-LF 402 — Q6171_N_S

APPLE P/N 353S2456
4.5V POWER SUPPLY FOR CODEC

L6111 FERR-220-OHM 0402 — MIN_LINE_WIDTH=0.40MM MIN_NECK_WIDTH=0.20MM VOLTAGE=5V — PP5V_AUDIO_HPAMP

L6110 FERR-220-OHM 0402 — MIN_LINE_WIDTH=0.40MM MIN_NECK_WIDTH=0.20MM VOLTAGE=5V — =PP5V_S0_AUDIO

VR6101 TPS71745 CRITICAL

IN	6		
SON			
OUT	1		PP4V5_AUDIO_ANALOG MIN_LINE_WIDTH=0.40MM MIN_NECK_WIDTH=0.15MM VOLTAGE=4.5V
4V5_REG_IN			
4V5_REG_EN	4	EN	
NR/FB	3	4V5_NR	
GND	2		
NC	5		

=PP3V3_S0_AUDIO

R6120 0 5% 1/16W MF-LF 402

C6122 1UF 10% 16V X5R 402-1

XW6110 SM

C6123 0.1UF 10% 16V X7R-CERM 0402

C6124 1UF 10% 16V X5R 402-1

GND_AUDIO_CODEC MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.2MM VOLTAGE=0V

XW6111 SM

GND_AUDIO_HPAMP MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.2MM VOLTAGE=0V

PLACE XW6110 BENEATH U6101, BETWEEN PINS 2 & 5

SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012

PAGE TITLE: AUDIO: CODEC/REGULATORS

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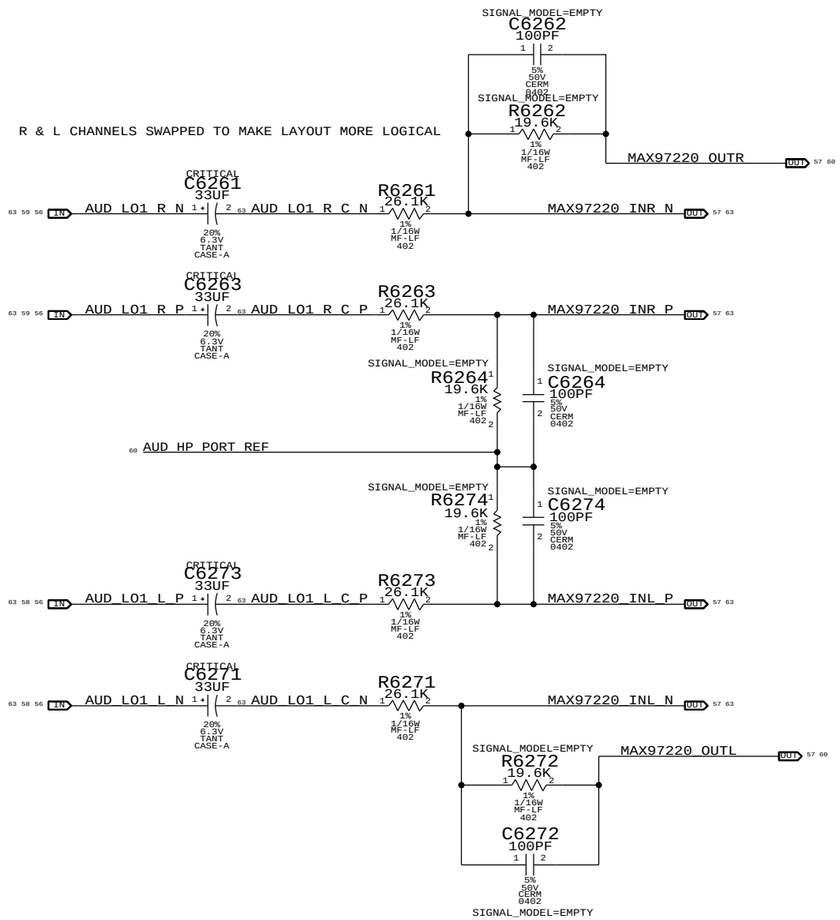

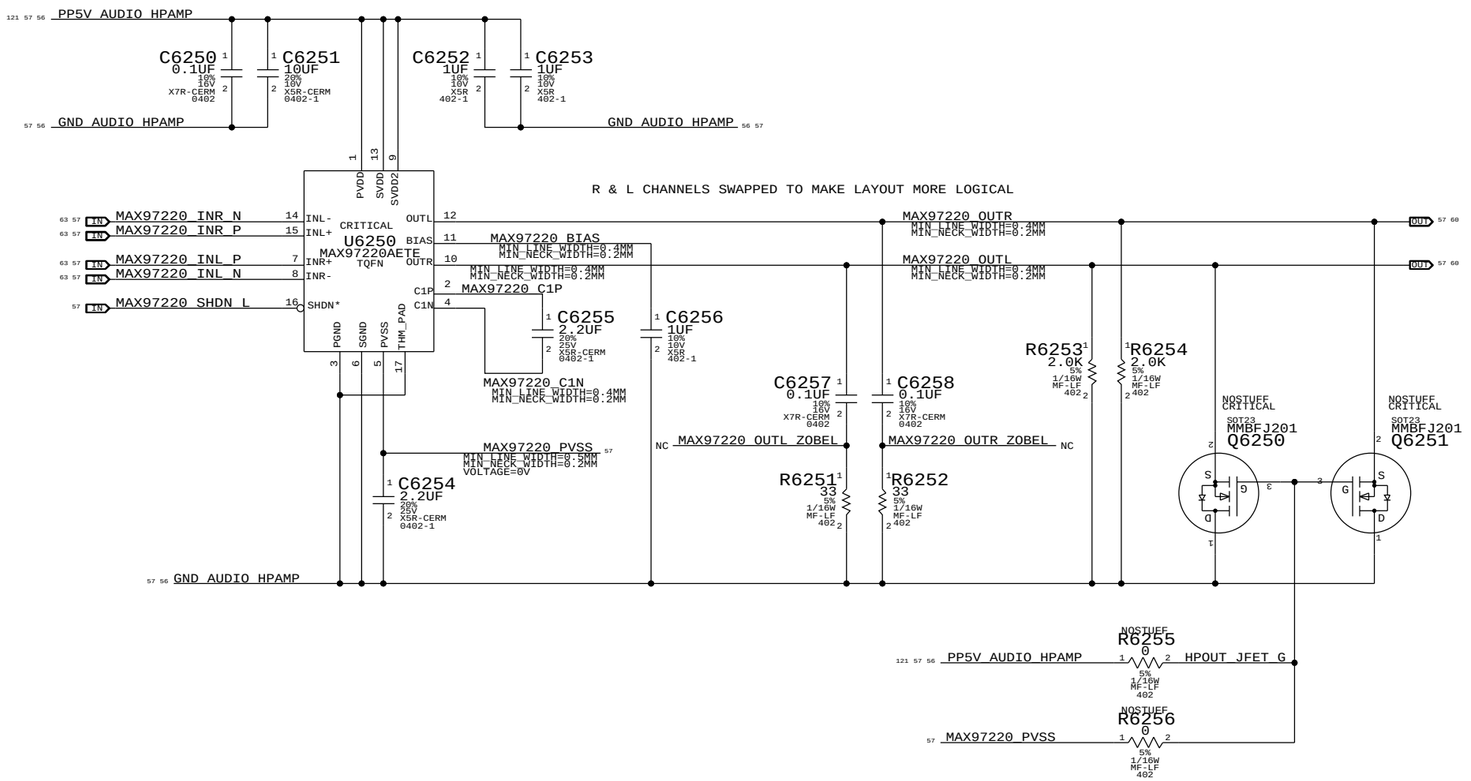

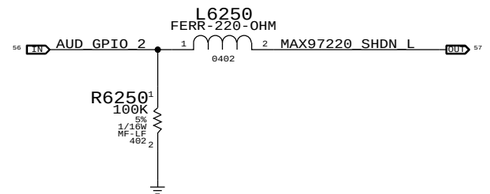

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
127S0135	127S0120		C6261	THAILAND ALTERNATE
127S0135	127S0120		C6263	THAILAND ALTERNATE
127S0135	127S0120		C6271	THAILAND ALTERNATE
127S0135	127S0120		C6273	THAILAND ALTERNATE

SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012

PAGE TITLE: AUDIO: HEADPHONE AMP

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LEFT CH SPEAKER AMP
APPLE P/N 353S3163

SPEAKER AMP GAIN = +9 DB
SPEAKER AMP RIN = 40K NOMINAL
FC_HPF, TWEETERS = ~847 HZ (4700 PF)
FC_HPF, WOOFERS = ~4 HZ (1.0 UF)

=PP12V_S0_AUDIO_SPKRAMP
C6300 10UF 10% 25V X5R 805
C6301 10UF 10% 25V X5R 805
C6302 0.1UF 10% 25V X5R 402
C6303 1UF 10% 25V X5R 603-1
C6304 0.1UF 10% 25V X5R 402
C6305 1UF 10% 25V X5R 603-1
CRITICAL C6306 220UF 20% 16V ELEC SM-CASE-C1-HF
CRITICAL C6307 220UF 20% 16V ELEC SM-CASE-C1-HF

INPUT POLARITY FLIP OK -- TRUE DIFF INPUTS

L6300 FERR-1000-OHM 0402
L6301 FERR-1000-OHM 0402
L6302 FERR-1000-OHM 0402
L6303 FERR-1000-OHM 0402
C6308 1UF 10% 25V X5R 0402
C6309 1UF 10% 25V X5R 0402
C6310 4700PF 5% 50V NPO-C0G-CERM 0805
C6311 4700PF 5% 50V NPO-C0G-CERM 0805

AUD_LO2_L_N
AUD_LO2_L_P
AUD_LO1_L_P
AUD_LO1_L_N
AUD_LAMP_RINC_P
AUD_LAMP_RIN_P
AUD_LAMP_RINC_N
AUD_LAMP_RIN_N
AUD_LAMP_LINC_P
AUD_LAMP_LIN_P
AUD_LAMP_LINC_N
AUD_LAMP_LIN_N

CRITICAL U6300 SSM3302 LFCSP

20	INR+		
19	INR-		
22	SDNR*	AUD_SPKRAMP_WIN_SHDN_L	ONLY WOOFERS ON UNDER WINDOWS
16	MONO	AUD_LAMP_MONO	
9	SDNL*	AUD_SPKRAMP_MAC_SHDN_L	WOOFERS & TWEETERS ON UNDER MAC OS
11	INL+		
12	INL-		
21	GAIN	AUD_LAMP_GAIN	
8	VREG/AVDD	AUD_LAMP_AVDD (MIN_LINE_WIDTH=0.20MM, MIN_NECK_WIDTH=0.15MM, VOLTAGE=5V)	
23	REGEN	=PP3V3_S0_AUDIO	
34,35,36,37	PVDD		
7,24,41	AGND		
31,32,33,38,39,40	PGND		
17	THERM	TP_AUD_LAMP_THERM NC	
30	BOOTR+	AUD_LAMP_BOOTRP	
28,29	OUTR+		
26,27	OUTR-		
25	BOOTR-	AUD_LAMP_BOOTRN	
10	EDGE	AUD_LAMP_EDGE	
1	BOOTL+	AUD_LAMP_BOOTLP	
2,3	OUTL+		
4,5	OUTL-		
6	BOOTL-	AUD_LAMP_BOOTLN	
18	NC	NC	
13	NC	NC	
14,15	TEST		

C6313 0.22UF 20% 25V X5R 603
C6314 0.22UF 20% 25V X5R 603
C6315 0.22UF 20% 25V X5R 603
C6316 0.22UF 20% 25V X5R 603
C6317 2.2UF 20% 10V X5R-CERM 402

OUTPUT POLARITY FLIP TO MAKE LAYOUT MORE LOGICAL

AUD_LAMP_OUTPR
AUD_LAMP_OUTNR
AUD_LAMP_OUTPL
AUD_LAMP_OUTNL
MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM

SIGNAL_MODEL=EMPTY
CRITICAL L6305 110-OHM-3A DLY5ATN111SQ2
CRITICAL L6307 110-OHM-3A DLY5ATN111SQ2

AUD_SPKR_LWFR_OUT_P
AUD_SPKR_LWFR_OUT_N
AUD_SPKR_LTWT_OUT_P
AUD_SPKR_LTWT_OUT_N

CRITICAL C6323 1000PF 5% 25V NP0-C0G 402
CRITICAL C6324 1000PF 5% 25V NP0-C0G 402
CRITICAL C6319 1000PF 5% 25V NP0-C0G 402
CRITICAL C6320 1000PF 5% 25V NP0-C0G 402
CRITICAL C6321 1000PF 5% 25V NP0-C0G 402
CRITICAL C6322 1000PF 5% 25V NP0-C0G 402

PINS 14 & 15 ARE TEST PINS AND SHOULD BE TIED TO GND

L6308 FERR-1000-OHM 0402
AUD_CODEC_MICBIAS
AUD_SPKRAMP_MAC_SHDN_L
R6301 100K 5% 1/16W MF-LF 402
NOSTUFF C6312 100PF 5% 50V CERM 402

R6308 0 5% 1/16W MF-LF 402
AUD_GPIO_3
AUD_SPKRAMP_WIN_SHDN_L
R6309 100K 5% 1/16W MF-LF 402
NOSTUFF C6318 100PF 5% 50V CERM 402

EDGE RATE CONTROL	R6304	R6305
ON	0 OHM	NOSTUFF
OFF	NOSTUFF	0 OHM

AUD_RAMP_MONO NET:
HIGH = MONO OPERATION
LOW = STEREO OPERATION

GAIN	R6306	R6307
+9 DB	NOSTUFF	0 OHM
+12 DB	NOSTUFF	47 KOHM
+15 DB	NOSTUFF	NOSTUFF
+18 DB	47 KOHM	NOSTUFF
+24 DB	0 OHM	NOSTUFF

AUD_LAMP_AVDD
R6304 0 5% 1/16W MF-LF 402
NOSTUFF R6306 0 5% 1/16W MF-LF 402
AUD_LAMP_EDGE
AUD_LAMP_MONO
AUD_LAMP_GAIN
NOSTUFF R6305 0 5% 1/16W MF-LF 402
R6303 0 5% 1/16W MF-LF 402
R6307 47K 5% 1/16W MF-LF 402

SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012
PAGE TITLE: AUDIO: LEFT SPKR AMP
Apple Inc.
DRAWING NUMBER: 051-9505 SIZE: D
REVISION: 8.0.0
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PAGE: 63 OF 144
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RIGHT CH SPEAKER AMP
APPLE P/N 353S3163

SPEAKER AMP GAIN = +9 DB
SPEAKER AMP RIN = 40K NOMINAL
FC_HPF, TWEETERS = ~847 HZ (4700 PF)
FC_HPF, WOOFERS = ~4 HZ (1.0 UF)

INPUT POLARITY FLIP OK -- TRUE DIFF INPUTS

OUTPUT POLARITY FLIP TO MAKE LAYOUT MORE LOGICAL

ONLY WOOFERS ON UNDER WINDOWS

WOOFERS & TWEETERS ON UNDER MAC OS

PINS 14 & 15 ARE TEST PINS AND SHOULD BE TIED TO GND

EDGE RATE CONTROL	R6404	R6405
ON	0 OHM	NOSTUFF
OFF	NOSTUFF	0 OHM

AUD_RAMP_MONO NET:
HIGH = MONO OPERATION
LOW = STEREO OPERATION

GAIN	R6406	R6407
+9 DB	NOSTUFF	0 OHM
+12 DB	NOSTUFF	47 KOHM
+15 DB	NOSTUFF	NOSTUFF
+18 DB	47 KOHM	NOSTUFF
+24 DB	0 OHM	NOSTUFF

SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012

PAGE TITLE: AUDIO: RIGHT SPKR AMP

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DRAWING NUMBER 051-9505 SIZE D
REVISION 8.0.0
BRANCH prefsb
PAGE 64 OF 144
SHEET 59 OF 123

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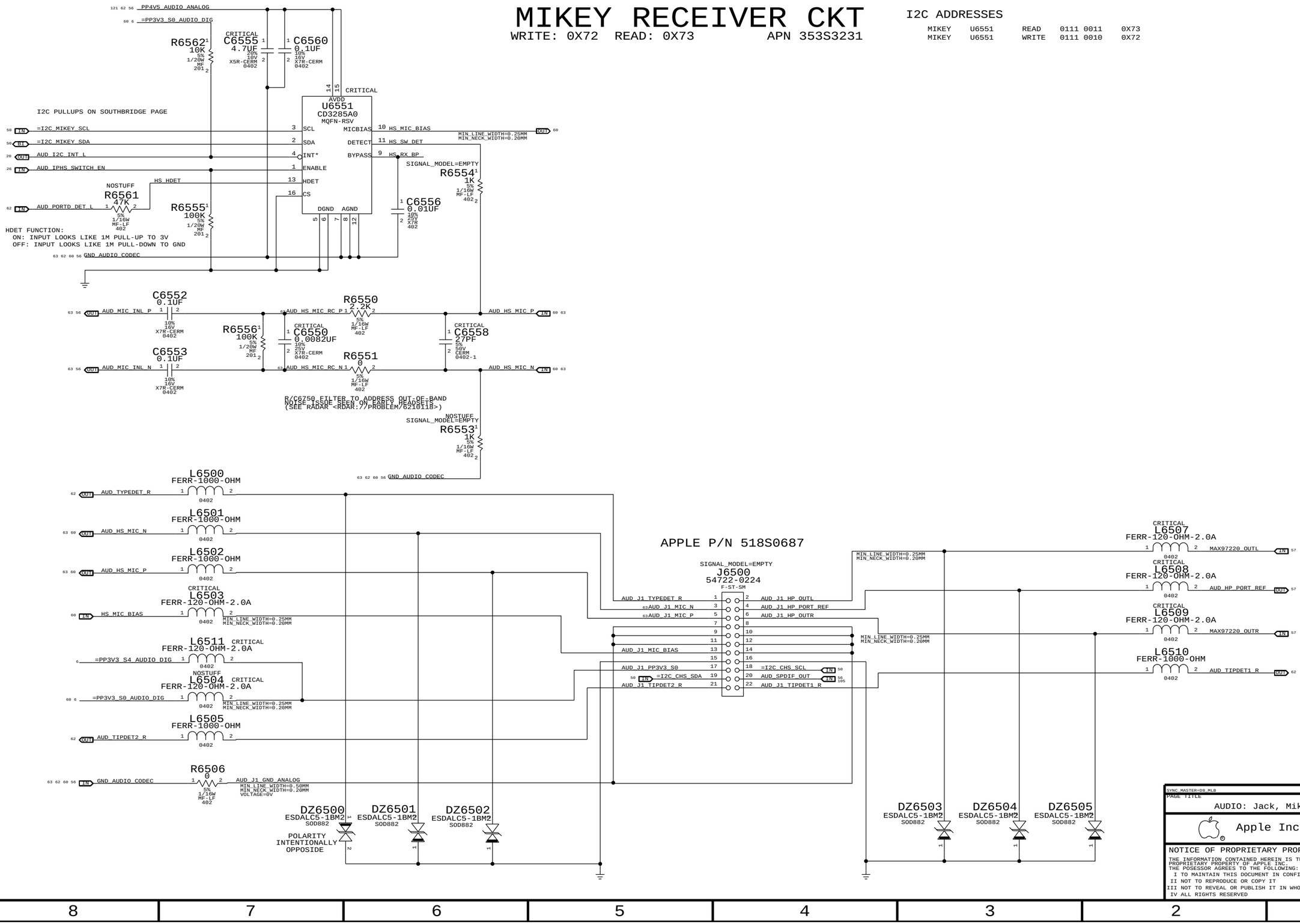
MIKEY RECEIVER CKT

WRITE: 0X72 READ: 0X73 APN 353S3231

I2C ADDRESSES

MIKEY	U6551	READ	0111 0011	0X73
MIKEY	U6551	WRITE	0111 0010	0X72



SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012

PAGE TITLE: AUDIO: Jack, Mikey, CHS Switch

Apple Inc.

DRAWING NUMBER: 051-9505 SIZE: D

REVISION: 8.0.0

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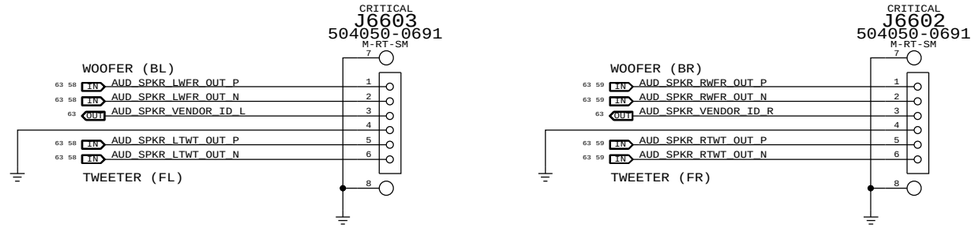
SPEAKER CABLE CONNECTORS

APPLE P/N 518S0862



SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012

PAGE TITLE: Audio: Spkr/Mic Conn.

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DRAWING NUMBER: 051-9505 SIZE: D

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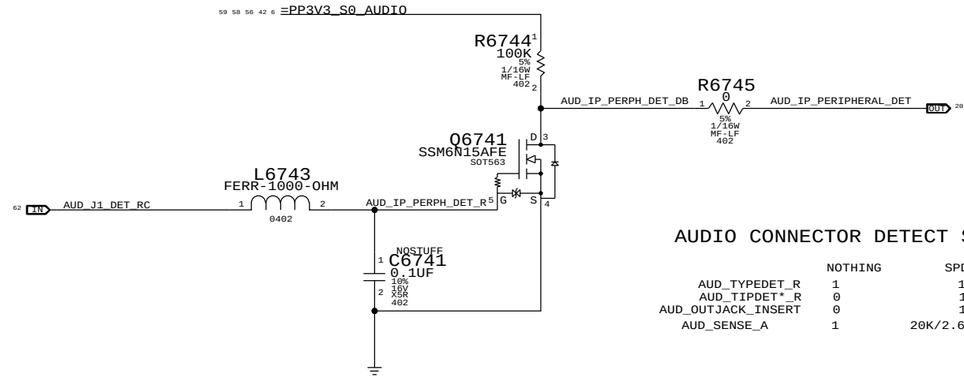
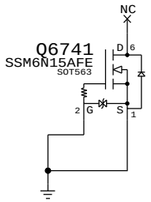
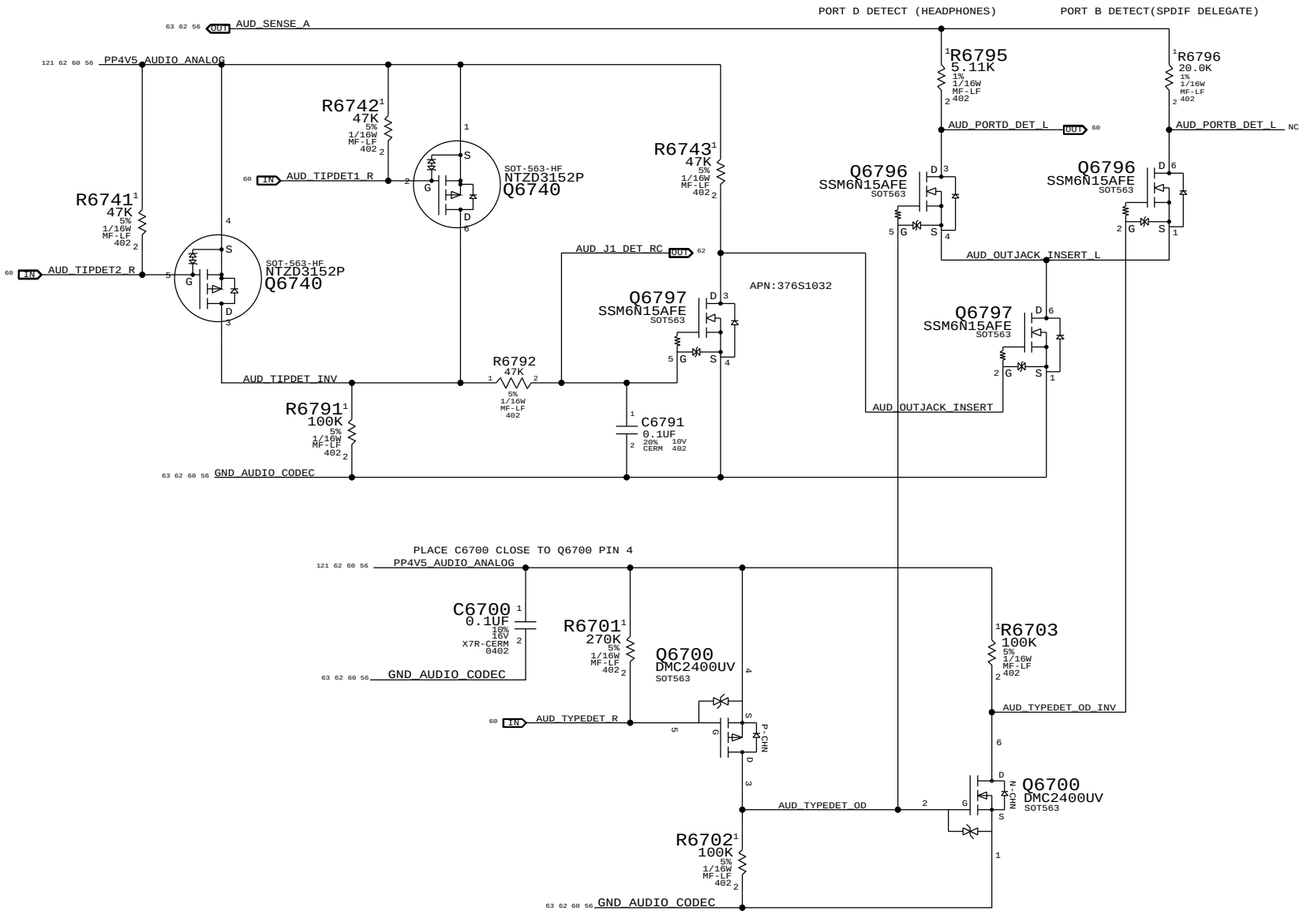
IPHS HS Detect Debounce CKT



AUDIO CONNECTOR DETECT STATES

	NOTHING	SPDIF	HEADPHONE
AUD_TYPEDET_R	1	1	0
AUD_TIPDET*_R	0	1	1
AUD_OUTJACK_INSERT	0	1	1
AUD_SENSE_A	1	20K/2.67K RDIV	5.11K/2.67K RDIV





LI Insert Detect (DETECT A)

SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012

PAGE TITLE: AUDIO: Detects/Grounding

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CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME/MUTE	CONVERTER	PIN COMPLEX	MAC SHDN	WIN SHDN	DET ASSIGNMENT
HP/LINE OUT	0X03 (3)	0X03 (3)	0X0A (10,D)	GPIO_2	GPIO_2	0X0A (DET D)
PRIMARY SPKRS (WFR)	0X04 (4)	0X04 (4)	0X0B (11)	MICBIAS	GPIO_3	N/A
SECONDARY SPKRS (TWT)	0X03 (3)	0X03 (3)	0X0A (10,V24)	MICBIAS	N/A	N/A
SPDIF OUT	N/A	0X08 (8)	0x10 (16)	N/A	N/A	0X0D (DET B)

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	ENABLE/CONTROL	DET ASSIGNMENT
SPDIF IN	0X07 (7)	0x0F (15)	N/A	0X09 (DET A)
INTERNAL MIC ARRAY	0X06 (6) 0X05 (5)	0x0E (14,LEFT & RIGHT) 0x12 (18,LEFT)	N/A	N/A
EXTERNAL MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	PANTHER POINT GPIO 16	PANTHER POINT GPIO 5 (RCVR INT) PANTHER POINT GPIO 3 (PERIPH DET)

OTHER DETECT

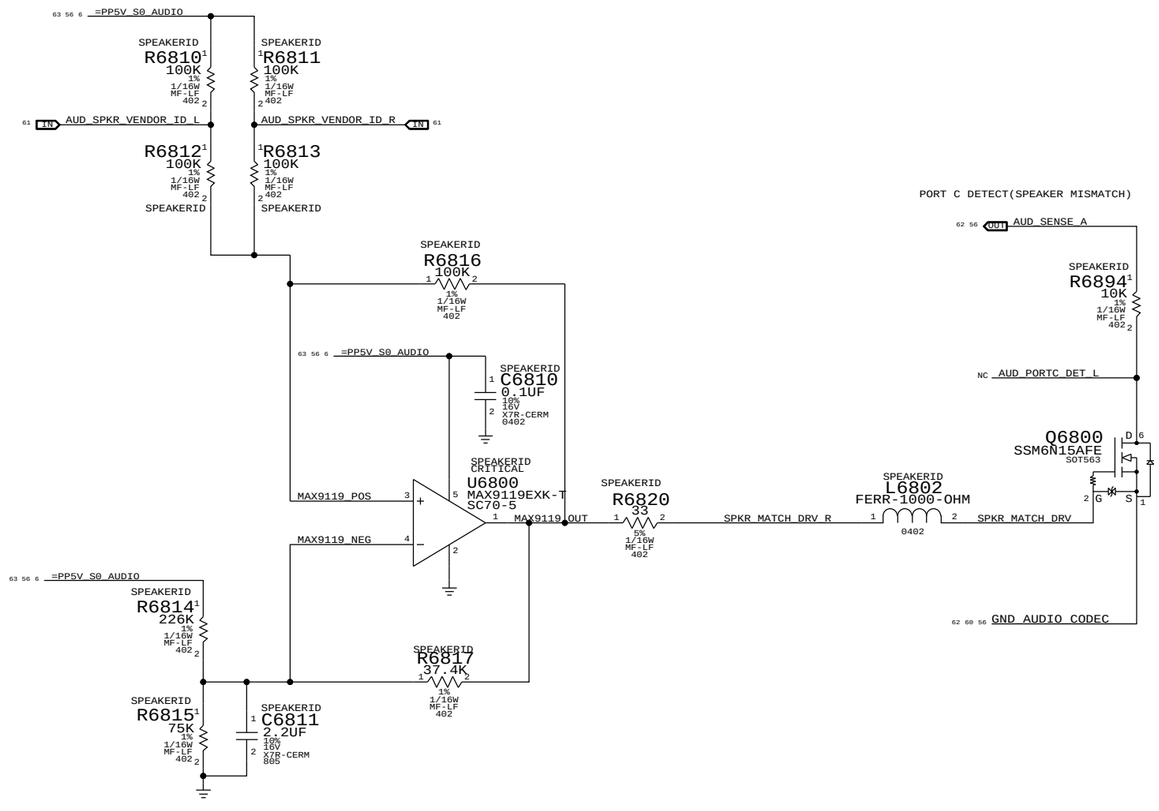
FUNCTION	CONVERTER	PIN COMPLEX	ENABLE/CONTROL	DET ASSIGNMENT
MULTIPLE SPKR VENDORS	N/A	N/A	N/A	0X0C (DET C)

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
AUDIO	*	0.1 MM	?
SPKROUT	*	0.2 MM	?

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
AUDIODIFF	*	AUDIODIFF
SPKROUTDIFF	*	SPKROUTDIFF

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
AUDIODIFF	*	Y	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM
SPKROUTDIFF	*	Y	0.6 MM	0.25 MM	10 MM	0.2 MM	0.2 MM

CIRCUIT THEORY OF OPERATION AVAILABLE IN <RDAR://PROBLEM/9776522>



ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
I2S0	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_P 56 57 58
I2S0	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_N 56 57 58
I2S0	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_C_P 57
I2S0	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_C_N 57
I2S1	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_P 56 57 59
I2S1	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_N 56 57 59
I2S1	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_C_P 57
I2S1	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_C_N 57
I2S0	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_P 56 58
I2S0	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_N 56 58
I2S1	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_P 56 59
I2S1	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_N 56 59
I2S0	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LINC_P 59
I2S0	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LINC_N 59
I2S0	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RINC_P 59
I2S0	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RINC_N 59
I2S2	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LIN_P 59
I2S2	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LIN_N 59
I2S2	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RIN_P 59
I2S2	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RIN_N 59
I2S0	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LINC_P 58
I2S0	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LINC_N 58
I2S0	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RINC_P 58
I2S0	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RINC_N 58
I2S2	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LIN_P 58
I2S2	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LIN_N 58
I2S2	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RIN_P 58
I2S2	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RIN_N 58
I2S0	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	MAX9722D_INL_P 57
I2S0	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	MAX9722D_INL_N 57
I2S1	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	MAX9722D_INR_P 57
I2S1	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	MAX9722D_INR_N 57
I2S0	SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RWFR_OUT_P 59 61
I2S0	SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RWFR_OUT_N 59 61
I2S0	SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RTWT_OUT_P 59 61
I2S0	SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RTWT_OUT_N 59 61
I2S0	SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LWFR_OUT_P 58 61
I2S0	SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LWFR_OUT_N 58 61
I2S0	SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LTWT_OUT_P 58 61
I2S0	SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LTWT_OUT_N 58 61
I2S0	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_INL_P 56 60
I2S0	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_INL_N 56 60
I2S0	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HS_MIC_RC_P 60
I2S0	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HS_MIC_RC_N 60
I2S0	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HS_MIC_P 60
I2S0	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HS_MIC_N 60
I2S0	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_J1_MIC_P 60
I2S0	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_J1_MIC_N 60

SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012

PAGE TITLE: AUDIO: Speaker ID

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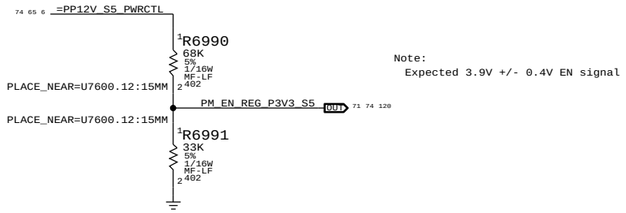
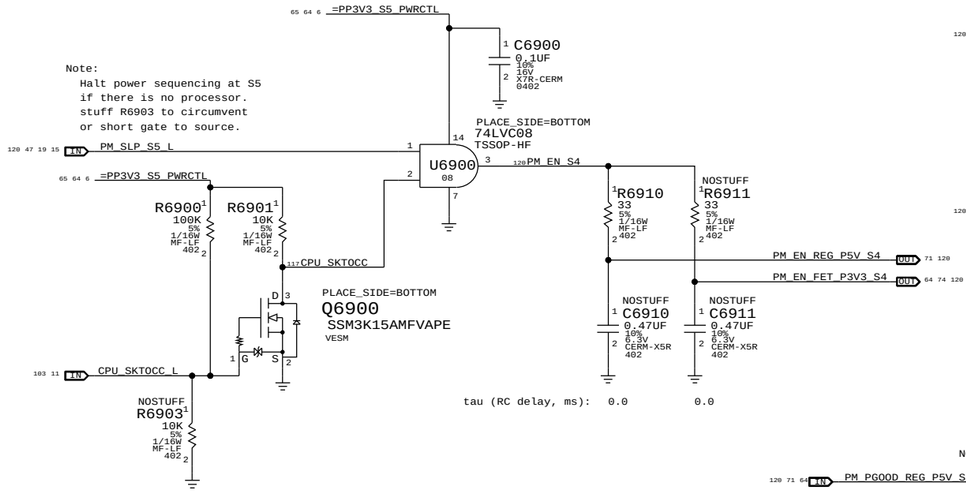
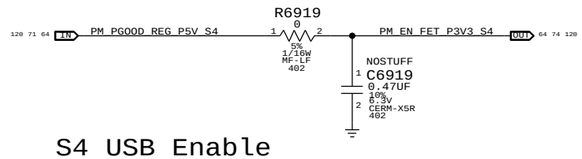
S5 3V3 Soft Enable



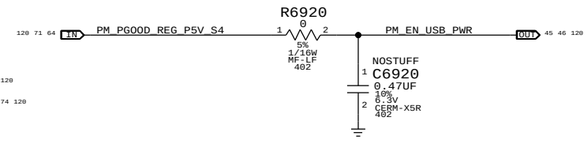
S4 5V Enable



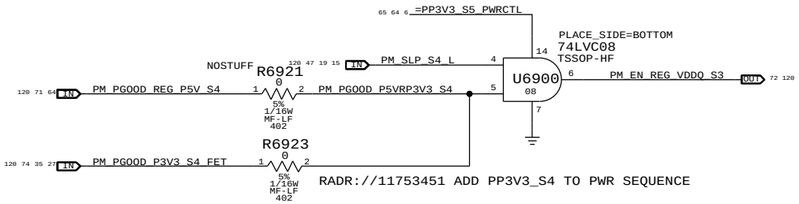
S4 3V3 Enable



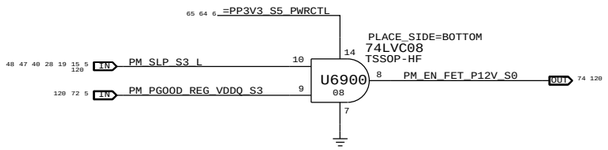
S4 USB Enable



S3 1V5 Reg (S0/S3) Enable



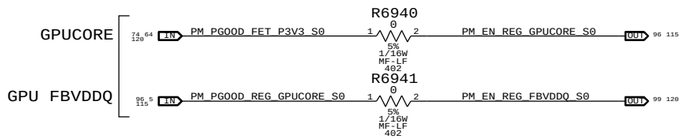
S0 12V Enable



S0 Platform Parallel Sequence Enable

CPU/PCH Sequencing

GPU Sequencing



Rail definitions

Platform: All processor non-Core and non-Graphics (5 V, 3.3 V, 1.8 V 1.5 V, PCH Core/PLL/VRM)
Uncore: VccSA, VDDQ, VccA (1.8 V), VccIO (VccSA, VccA, and VccIO must ramp within 50 ms of each other)

Notes on sequencing requirements

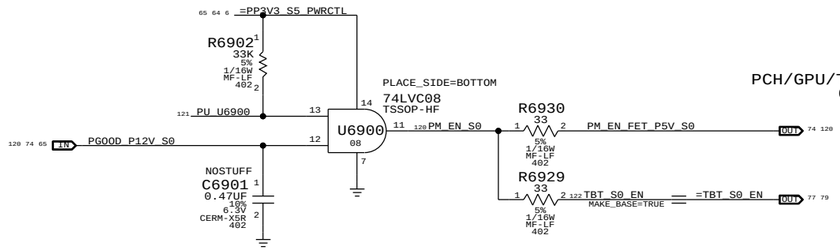
Intel:

1. No hard specification on platform rails
2. SMC guarantees timing on PCH DPWROK and PWROK
3. CPU VDDQ must ramp before MEMVTT and vice versa on power down. It has no relationship to any other rails.

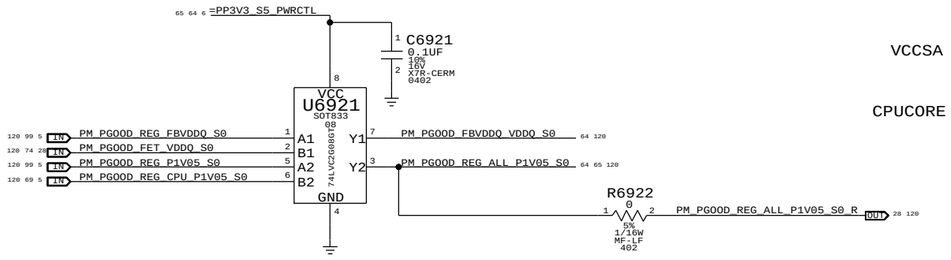
NVIDIA GFX:

1. VDD33 (our 3V3_S0)
2. IFPA/B_IOVDD (1.8 V) with or after 3V3_S0 (unused in our implementation)
3. NVVDD (our GPUCORE) after IFPA/B_IOVDD
4. FBVDDQ (our GPU_VDDQ) after NVVDD
5. PEX_VDD (our GPU_1V05) after FBVDDQ
6. IFPC/D/E/F_IOVDD (1.05V) wit or after PEX_VDD
7. The ramp time for any rail must be more than 40 uS
8. All rails must be powered off within 10 ms from first rail powering off

S0 5V and TBT Enable



Parallel Enable PGOOD combinator



SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012

PAGE TITLE
PM Regulator Enables

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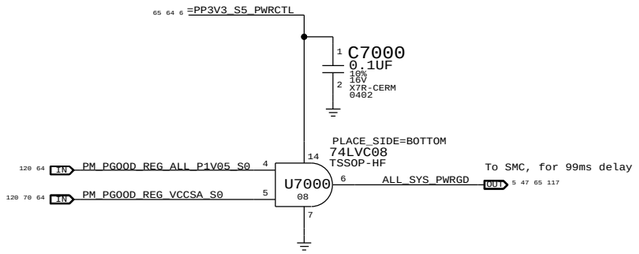
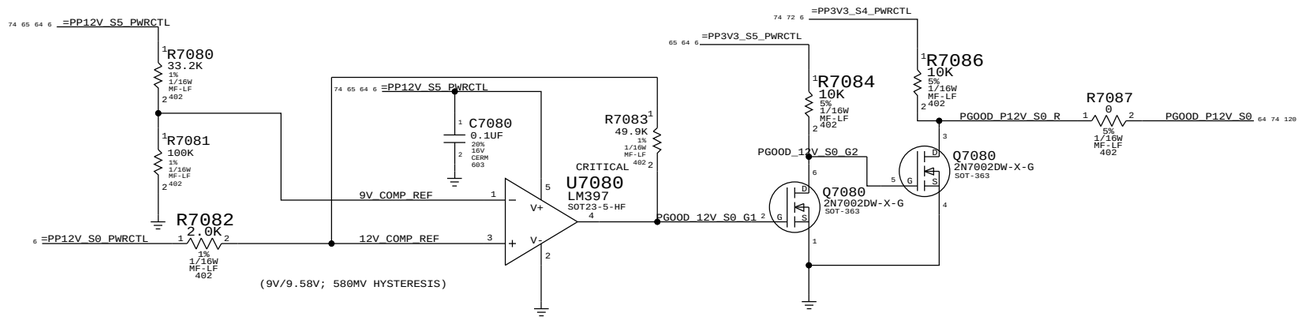
Platform Power Good

Derive SMC ALL_SYS_PWRGD

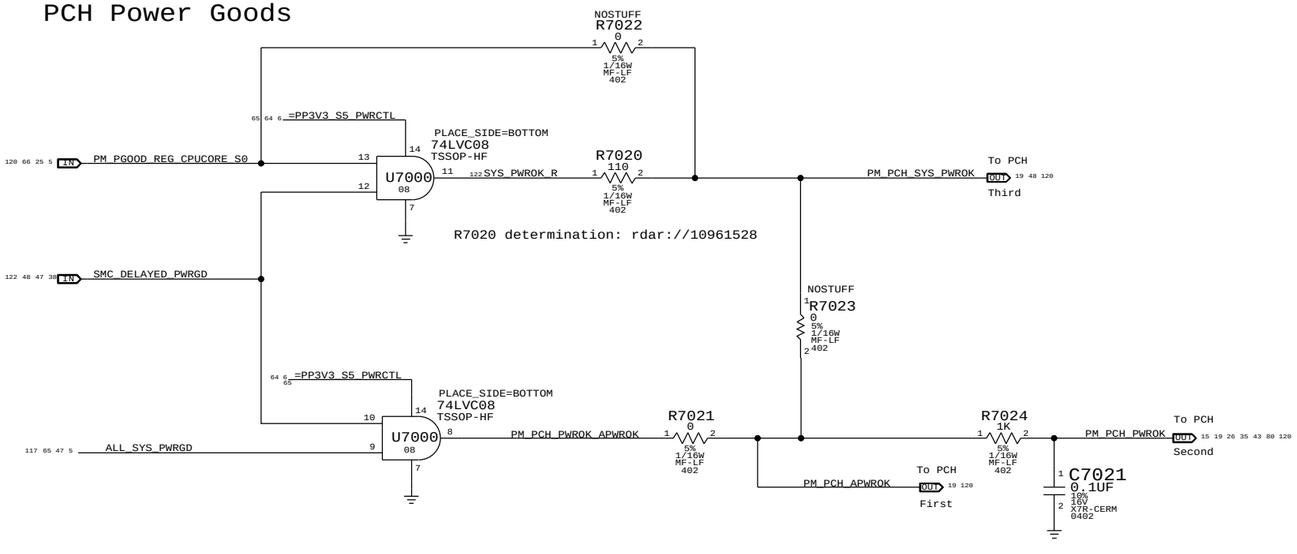
The end of the power sequence for S0 rails except CPU CORE.



PGOOD COMPARATORS FOR PP12V_S0



PCH Power Goods



radar://11043352 Need AND Gate to deassert PM_PCH_PWROK to PCH when unexpected power loss happens

Resume Reset

Intel Doc# 29517 Maho Bay PDG, Section 22.13
Intel Doc# 29562 Panther Point EDS, Section 8.7 and 8.8

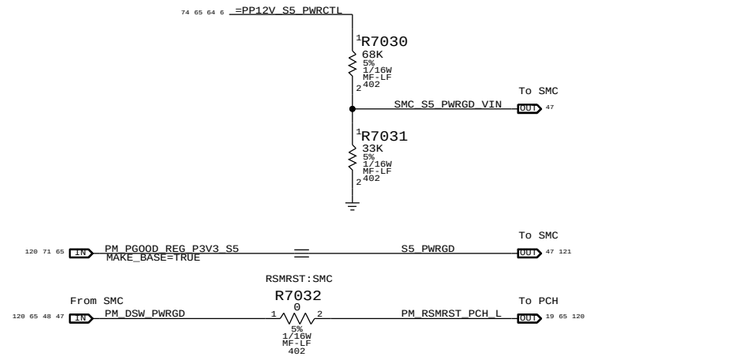
Note:
The iMac K70K72 designs does not support Deep Sx modes so both DPWROK and RSMRST# signals are shorted together

Requirements:
Power on:
Asserted at least 10 ms after all suspend well power is valid
Power off or loss of AC:
Transition to 0.8V or less before VccSUS3_3 drops to 2.90 V to allow PCH to switch suspend well to battery without excessive loading

Primary method:
The SMC guarantees proper assertion and de-assertion of RSMRST# for normal operation.

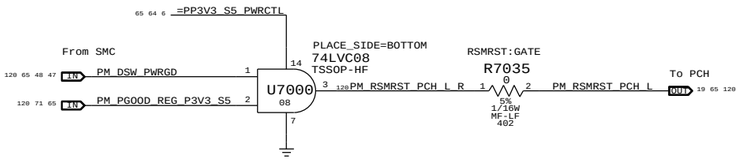
SMC de-asserts RSMRST# (PM_DSW_PWRGD) when S5_PWRGD input is asserted and SMC_S5_PWRGD_VIN input is above comparator input level of 1.5 V.

SMC asserts RSMRST# (PM_DSW_PWRGD) when SMC_S5_PWRGD_VIN input drops from 1.8 V to 1.5 V (as implemented) when 12 V S5 rail drops to 10 V.



Secondary method:
The SMC guarantees proper assertion and de-assertion of RSMRST# for normal operation via PM_DSW_PWRGD.

RSMRST# is asserted when power good from regulator is de-asserted in the event AC is lost. Power good de-assertion should happen quickly enough to meet Intel spec.



SYNC_MASTER=D8_MLB	SYNC_DATE=08/27/2012
PAGE TITLE: PM Power Good	
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	REVISION: 8.0.0
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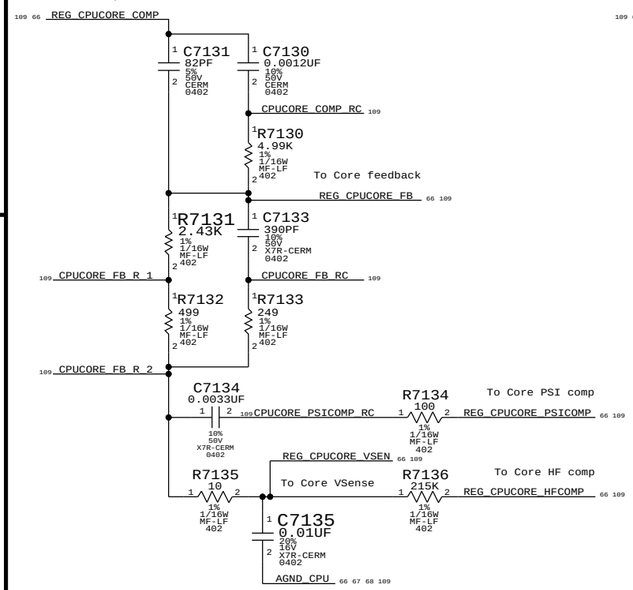
CPU Core S0 Regulator

Max avg current: 63 A (BUDGET)
Max peak current: 110 A (BUDGET)
OC trip point: ? A (nom)/? A (min)
Switching freq: 290 kHz

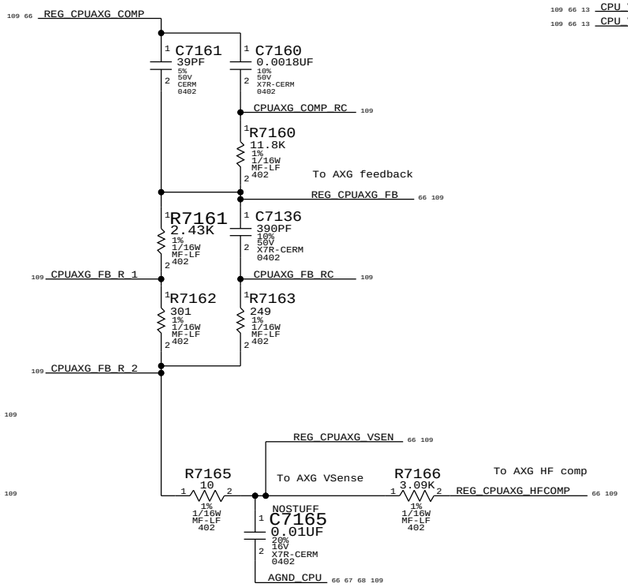
Core compensation and feedback



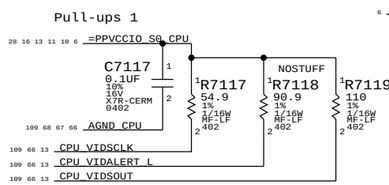
CPU AXG S0 Regulator

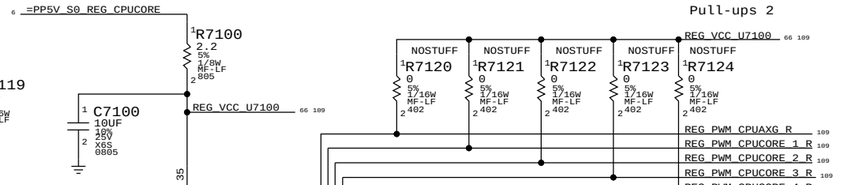
Max avg current: 12.7 A (BUDGET)
Max peak current: 30.0 A (BUDGET)
OC trip point: ? A (nom)/? A (min)
Switching freq: 290 kHz

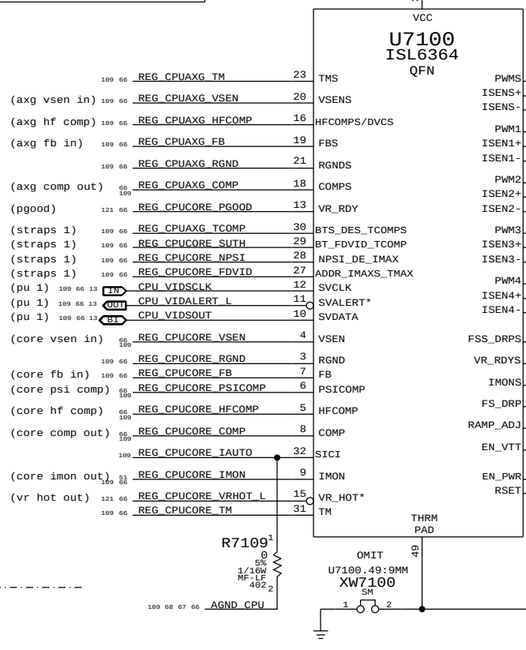
AXG compensation and feedback

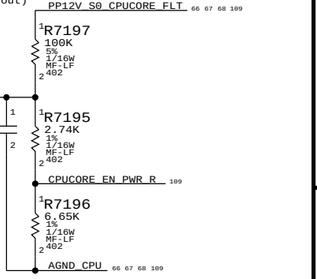


Pull-ups 1

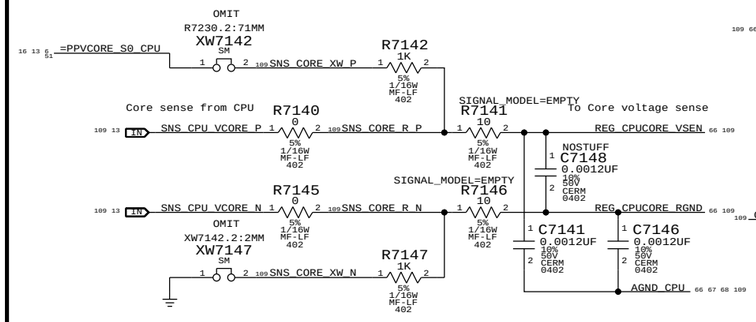




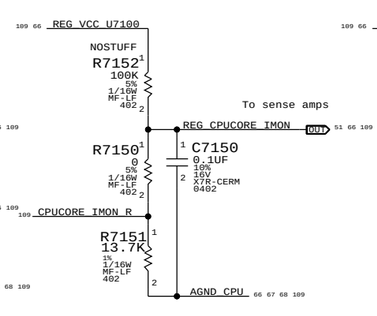




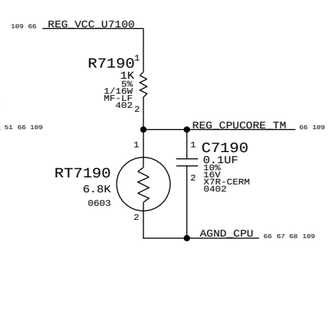
Core voltage sense input



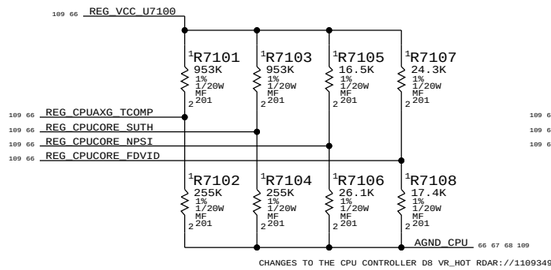
Core IMON output



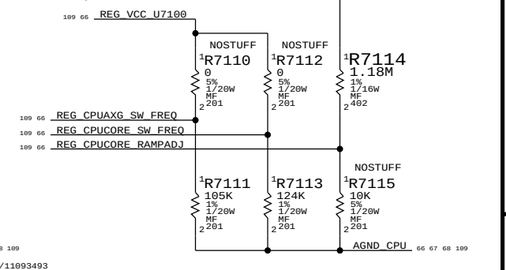
Core temp measurement



Straps 1

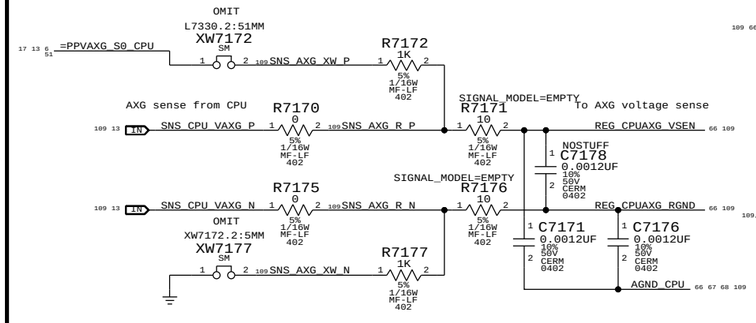


Straps 2

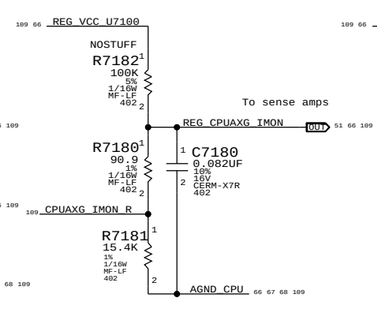


CHANGES TO THE CPU CONTROLLER D8 VR_HOT RDAR://11093493

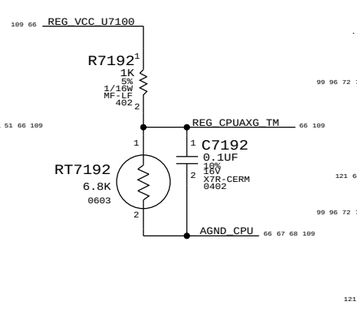
AXG voltage sense input



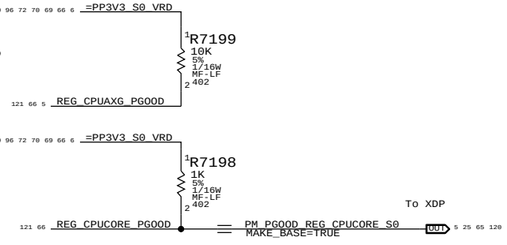
AXG IMON output



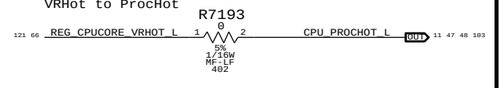
AXG temp measurement



Power goods



VRHot to ProcHot



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VReg CPU Core/AXG Cntl

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8 7 6 5 4 3 2 1

D C B A

109 68 67 66 PP12V_S0_CPUCORE_FLT

CPU Phase 1

C7225 1.0UF 10% 16V X7R 0603
C7226 1.0UF 10% 16V X7R 0603
C7227 1.0UF 10% 16V X7R 0603
109 REG_LVCC_U7210

U7210
ISL6622
DFN
CRITICAL
VCC UVCC LVCC
GDSEL
PWM
BOOT
UGATE
PHASE
LGATE
GND
THRML PAD
NC
109 66 TP REG_PWM_CPUCORE_1
109 REG_BOOT_CPUCORE_1
109 REG_UGATE_CPUCORE_1
109 REG_PHASE_CPUCORE_1
109 REG_LGATE_CPUCORE_1

109 REG_BOOT_CPUCORE_1_RC
R7216 0 5% 1/10W MF-LF 603
C7216 0.22UF 10% 25V X7R 0603

109 68 67 66 PP12V_S0_CPUCORE_FLT

CRITICAL Q7210 IRF6802SDTRPBF DIRECTFET-SA
CRITICAL Q7211 IRF6893MTRPBF DIRECTFET-MX

CRITICAL C7291 180UF 20% 16V POLY TH1
CRITICAL C7212 10UF 20% 16V X6S-CERM 0603
CRITICAL C7213 10UF 20% 16V X6S-CERM 0603
EMC C7214 1UF 10% 16V X6S-CERM 0402
EMC C7215 1UF 10% 16V X6S-CERM 0402

CRITICAL L7210 0.24UH-30A-0.35MOHM SDP110808M-TH
109 PPCPUCORE_S0_SENSE_1

NOSTUFF C7217 0.001UF 10% 50V X7R-CERM 0402
REG_SNUBBER_CPUCORE_1 109
NOSTUFF R7217 2.2 5% 1/8W MF-LF 805

CRITICAL R7210 0.0005 1% 1W MF 0612
PPCPUCORE_S0_REG OUT 6 67 68
REG_ISENCORE_1_P OUT 66 109
SIGNAL_MODEL=EMPTY
C7221 220PF 10% 50V X7R-CERM 0402
SIGNAL_MODEL=EMPTY
R7221 1.02K 1% 1/16W MF-LF 402
109 REG_ISENCORE_1_N
REG_ISENCORE_1_NR OUT 66 109
C7220 0.1UF 10% 16V X7R-CERM 0402
AGND_CPU 66 67 68 109

109 68 67 66 PP12V_S0_CPUCORE_FLT

R7247 10 5% 1/10W MF-LF 603

CPU Phase 2

C7245 1.0UF 10% 16V X7R 0603
109 REG_LVCC_U7230
C7247 1.0UF 10% 16V X7R 0603

U7230
ISL6612
QFN1
CRITICAL
VCC PVCC
PWM
BOOT
UGATE
PHASE
LGATE
GND
THRML PAD
NC
109 66 TP REG_PWM_CPUCORE_2
109 REG_BOOT_CPUCORE_2
109 REG_UGATE_CPUCORE_2
109 REG_PHASE_CPUCORE_2
109 REG_LGATE_CPUCORE_2

109 REG_BOOT_CPUCORE_2_RC
R7236 0 5% 1/10W MF-LF 603
C7236 0.22UF 10% 25V X7R 0603

CRITICAL Q7210 IRF6802SDTRPBF DIRECTFET-SA
CRITICAL Q7231 IRF6893MTRPBF DIRECTFET-MX

CRITICAL C7292 180UF 20% 16V POLY TH1
CRITICAL C7293 180UF 20% 16V POLY TH1
CRITICAL C7232 10UF 20% 16V X6S-CERM 0603
CRITICAL C7233 10UF 20% 16V X6S-CERM 0603
EMC C7234 1UF 10% 16V X6S-CERM 0402
EMC C7235 1UF 10% 16V X6S-CERM 0402

CRITICAL L7230 0.24UH-30A-0.35MOHM SDP110808M-TH
109 PPCPUCORE_S0_SENSE_2

NOSTUFF C7237 0.001UF 10% 50V X7R-CERM 0402
REG_SNUBBER_CPUCORE_2 109
NOSTUFF R7237 2.2 5% 1/8W MF-LF 805

CRITICAL R7230 0.0005 1% 1W MF 0612
PPCPUCORE_S0_REG OUT 6 67 68
REG_ISENCORE_2_P OUT 66 109
SIGNAL_MODEL=EMPTY
C7241 220PF 10% 50V X7R-CERM 0402
SIGNAL_MODEL=EMPTY
R7241 1.02K 1% 1/16W MF-LF 402
109 REG_ISENCORE_2_N
REG_ISENCORE_2_NR OUT 66 109
C7240 0.1UF 10% 16V X7R-CERM 0402
AGND_CPU 66 67 68 109

109 68 67 66 PP12V_S0_CPUCORE_FLT

R7267 10 5% 1/10W MF-LF 603

CPU Phase 3

C7265 1.0UF 10% 16V X7R 0603
109 REG_LVCC_U7250
C7267 1.0UF 10% 16V X7R 0603

U7250
ISL6612
QFN1
CRITICAL
VCC PVCC
PWM
BOOT
UGATE
PHASE
LGATE
GND
THRML PAD
NC
109 66 TP REG_PWM_CPUCORE_3
109 REG_BOOT_CPUCORE_3
109 REG_UGATE_CPUCORE_3
109 REG_PHASE_CPUCORE_3
109 REG_LGATE_CPUCORE_3

109 REG_BOOT_CPUCORE_3_RC
R7256 0 5% 1/10W MF-LF 603
C7256 0.22UF 10% 25V X7R 0603

CRITICAL Q7250 IRF6802SDTRPBF DIRECTFET-SA
CRITICAL Q7251 IRF6893MTRPBF DIRECTFET-MX

CRITICAL C7294 180UF 20% 16V POLY TH1
CRITICAL C7295 180UF 20% 16V POLY TH1
CRITICAL C7251 10UF 20% 16V X6S-CERM 0603
CRITICAL C7253 10UF 20% 16V X6S-CERM 0603
EMC C7254 1UF 10% 25V X6S-CERM 0402
EMC C7255 1UF 10% 25V X6S-CERM 0402

CRITICAL L7250 0.24UH-30A-0.35MOHM SDP110808M-TH
109 PPCPUCORE_S0_SENSE_3

NOSTUFF C7257 0.001UF 10% 50V X7R-CERM 0402
REG_SNUBBER_CPUCORE_3 109
NOSTUFF R7257 2.2 5% 1/8W MF-LF 805

CRITICAL R7250 0.0005 1% 1W MF 0612
PPCPUCORE_S0_REG OUT 6 67 68
REG_ISENCORE_3_P OUT 66 109
SIGNAL_MODEL=EMPTY
C7261 220PF 10% 50V X7R-CERM 0402
SIGNAL_MODEL=EMPTY
R7261 1.02K 1% 1/16W MF-LF 402
109 REG_ISENCORE_3_N
REG_ISENCORE_3_NR OUT 66 109
C7260 0.1UF 10% 16V X7R-CERM 0402
AGND_CPU 66 67 68 109

CPU Output Decoupling

68 67 6 PPCPUCORE_S0_REG

CRITICAL C7280 270UF-0.006OHM 20% 2V TANT CASE-D2
CRITICAL C7281 270UF-0.006OHM 20% 2V TANT CASE-D2
CRITICAL C7282 270UF-0.006OHM 20% 2V TANT CASE-D2
CRITICAL C7283 270UF-0.006OHM 20% 2V TANT CASE-D2
CRITICAL C7284 270UF-0.006OHM 20% 2V TANT CASE-D2
CRITICAL C7285 270UF-0.006OHM 20% 2V TANT CASE-D2

Filtered 12V Rail

CRITICAL L7200 0.36UH-30A-0.6MOHM SDP110808MR36MF-TH
6 =PP12V_S0_REG_CPUCORE
PP12V_S0_CPUCORE_FLT 66 67 68 109

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VReg CPU Core Phases

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CPU Phase 4

AXG Phase

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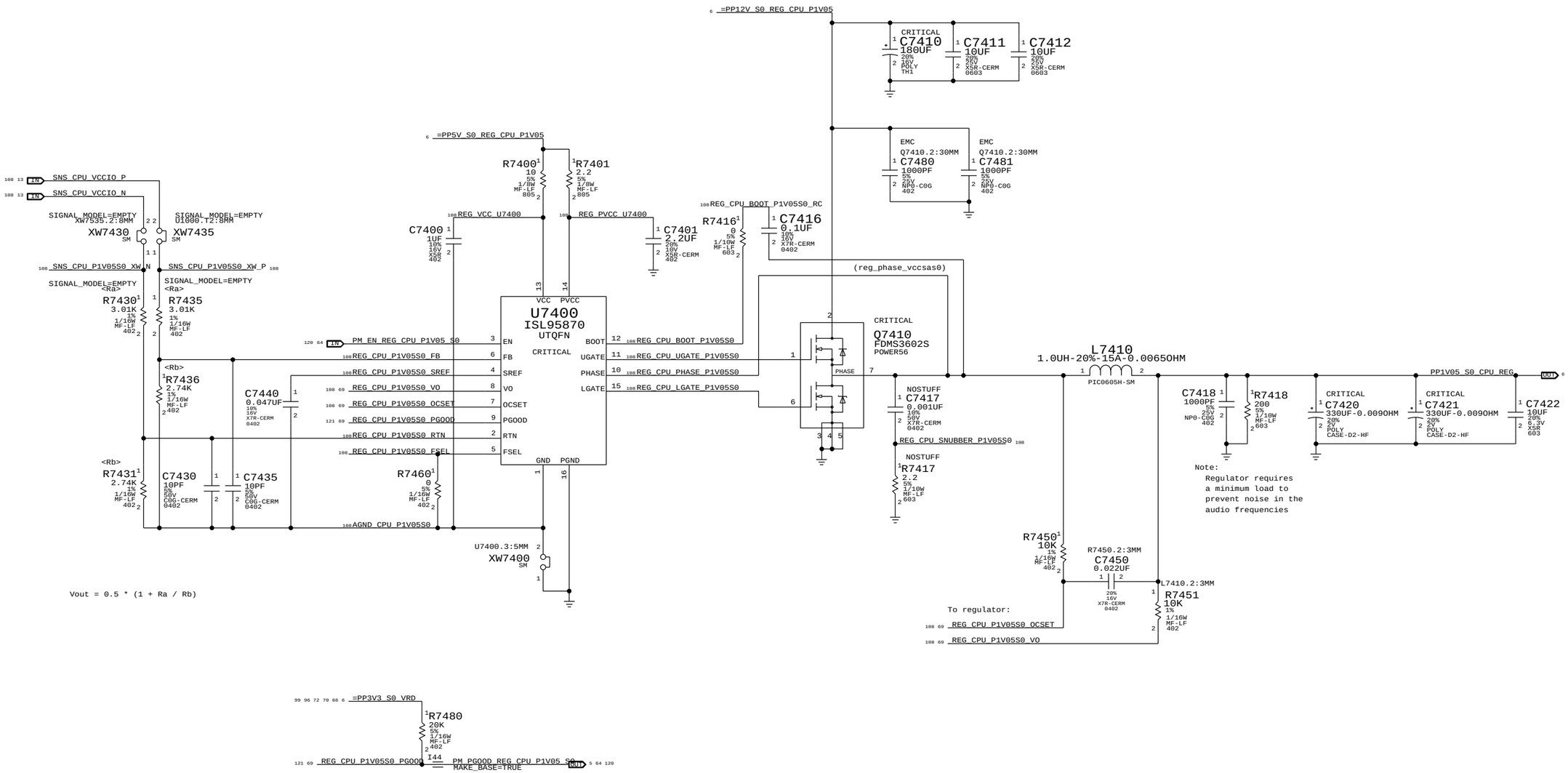
CPU VccIO (1.05V) S0 Regulator

Max avg current: 8.10 A (BUDGET)
Max peak current: 8.50 A (BUDGET)
OC trip point: ? A (min)/? A (max)
Switching freq: 500 kHz



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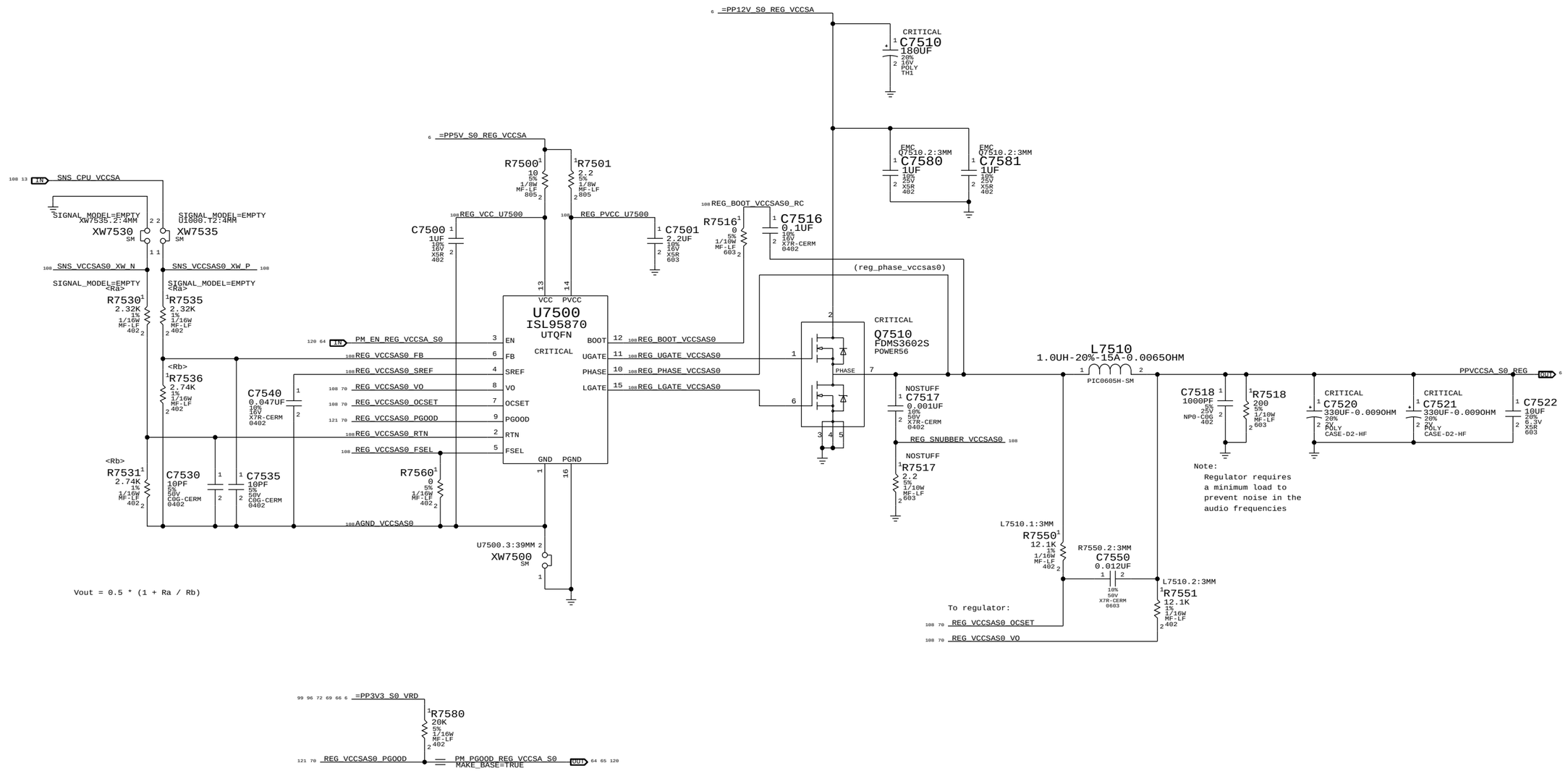
CPU VccSA (0.925V) S0 Regulator

Max avg current: 12.07 A (BUDGET)
Max peak current: 30 A (BUDGET)
OC trip point: ? A (min)/? A (max)
Switching freq: 500 kHz



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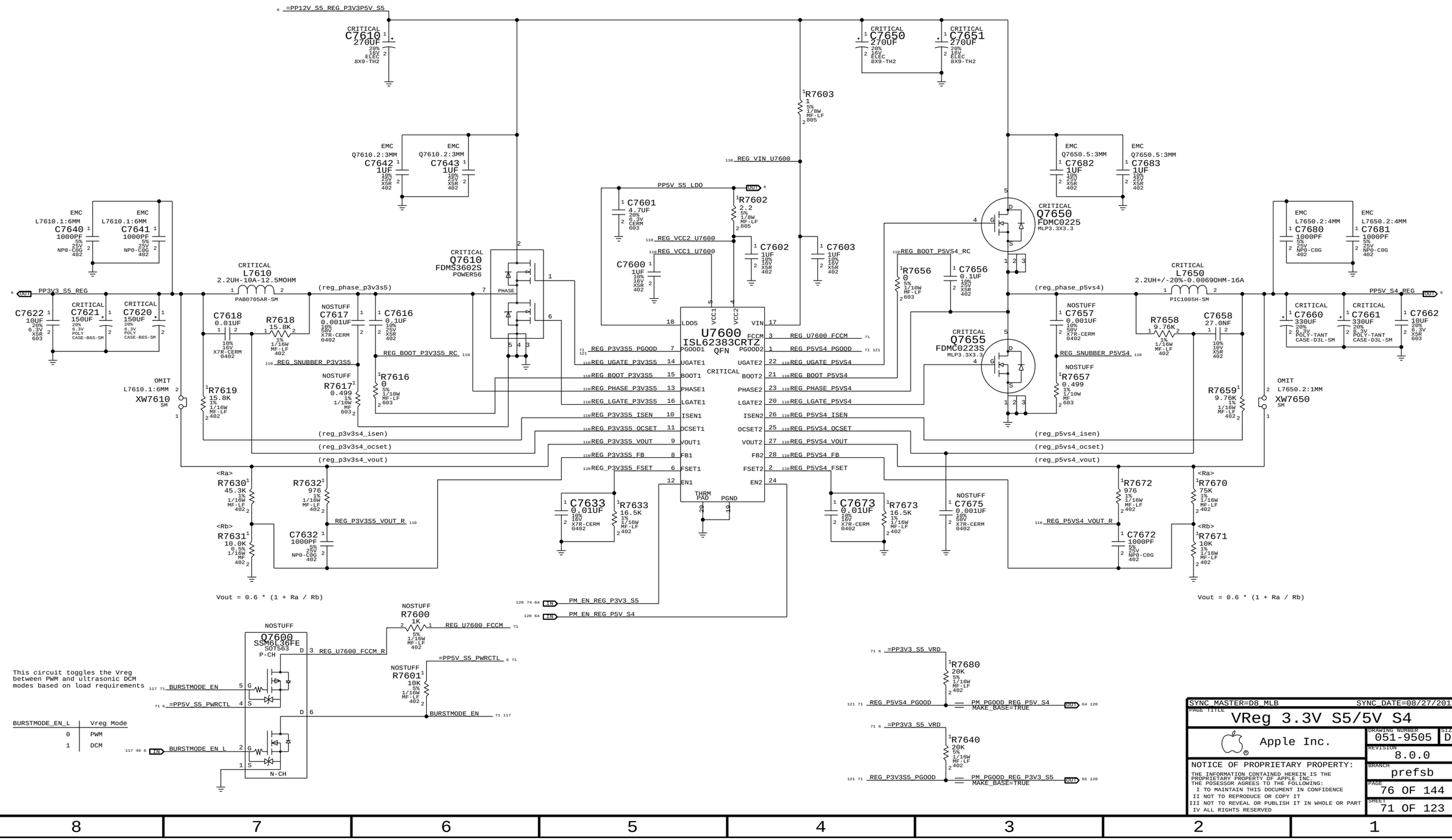
3.3V S5 Regulator

Max avg current: 6 A (design)/ 4.85 A (budget)
Max peak current: ? A (design)/ 6.6 A (budget)
OC trip point: ? A (nom)/? A (min)
Switching freq: 350 kHz

5V S4 Regulator

Max avg current: 10 A (design)/ 6.08 A (budget)
Max peak current: ? A (design)/ 6.9 A (budget)
OC trip point: ? A (nom)/? A (min)
Switching freq: 350 kHz



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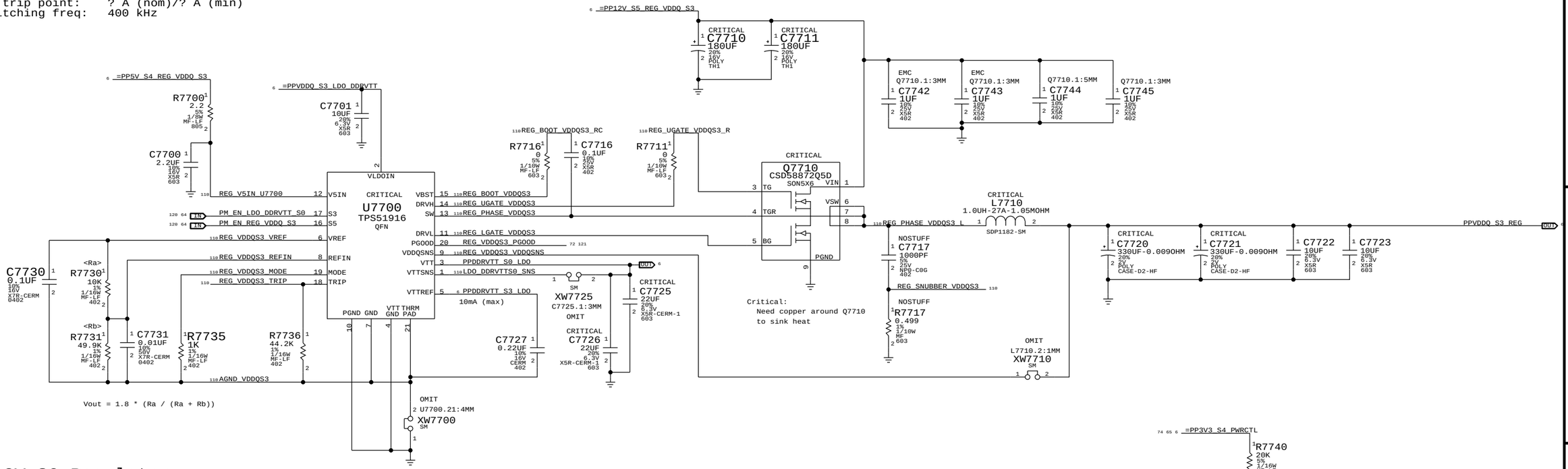
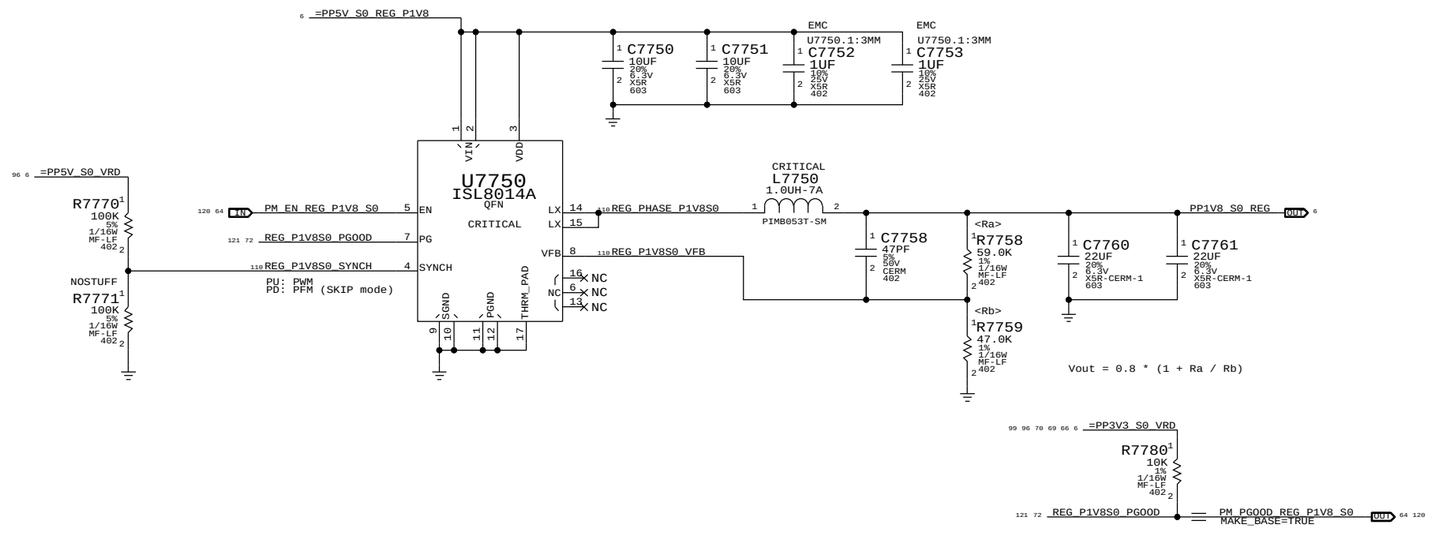
VDDQ (1.5V) S3 Regulator

Max avg current: 9.0 A (BUDGET)
Max peak current: 11.3 A (BUDGET)
OC trip point: ? A (nom)/? A (min)
Switching freq: 400 kHz



1.8V S0 Regulator

Max avg current: 0.6 A (BUDGET)
Max peak current: 1.7 A (BUDGET)
OC trip point: ? A (nom)/? A (min)
Switching freq: ? kHz



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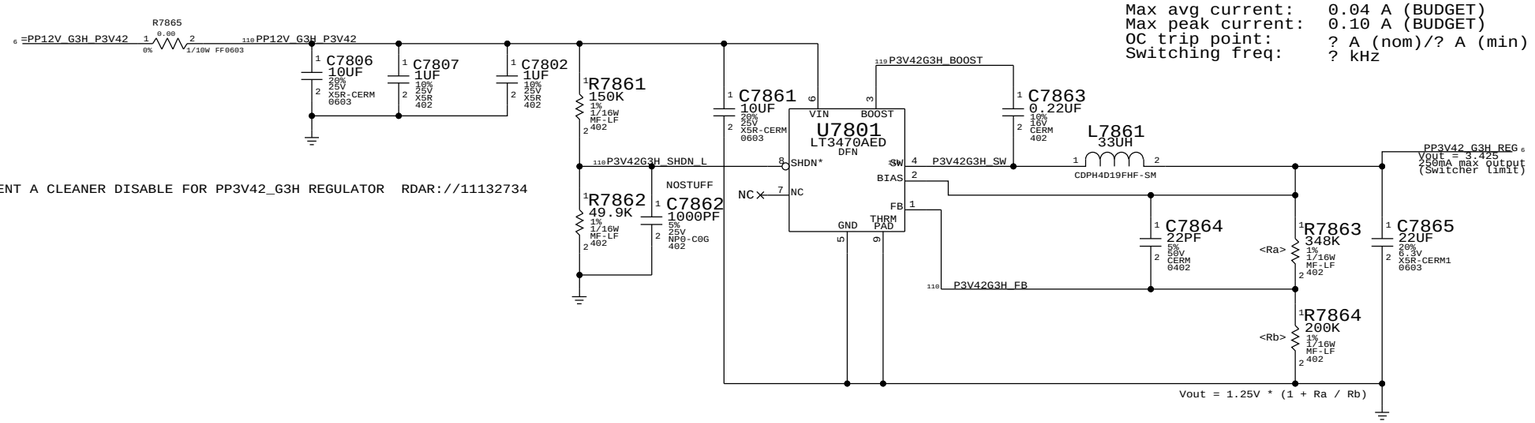
D8:CONTROLLER CHANGE FOR 3.42V SMC SUPPLY RDAR://11003901

D7/D7I: IMPLEMENT A CLEANER DISABLE FOR PP3V42_G3H REGULATOR RDAR://11132734



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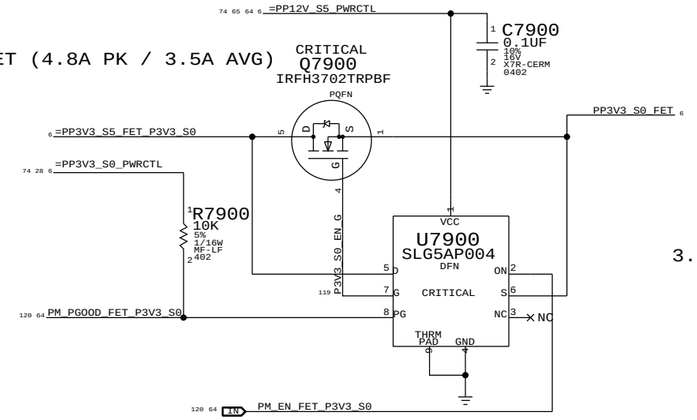
3.3V S0 FET (4.8A PK / 3.5A AVG)



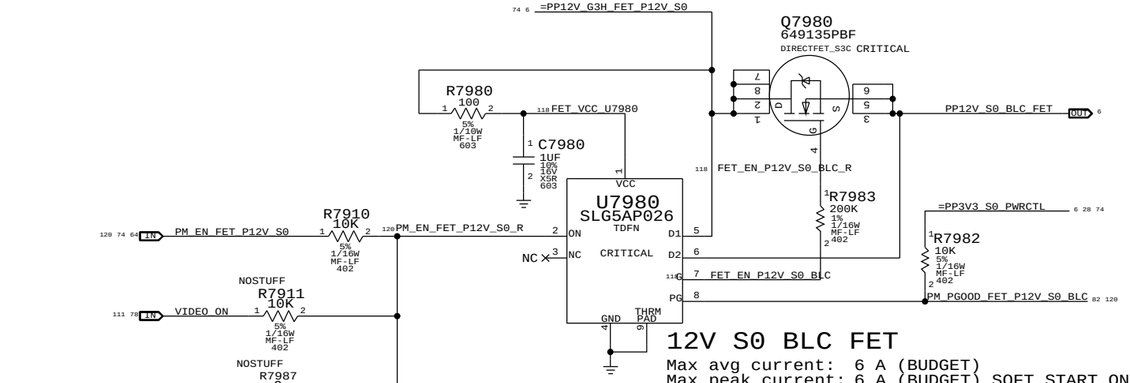
12V S0 FET

Max avg current: 20.4 A (BUDGET)
Max peak current: 24.1 A (BUDGET)

RADAR://11420274 NEW MOSFET Q7950 TO AVOID 50A 100US PULSE ON 12V S0.

12V S0 BLC FET

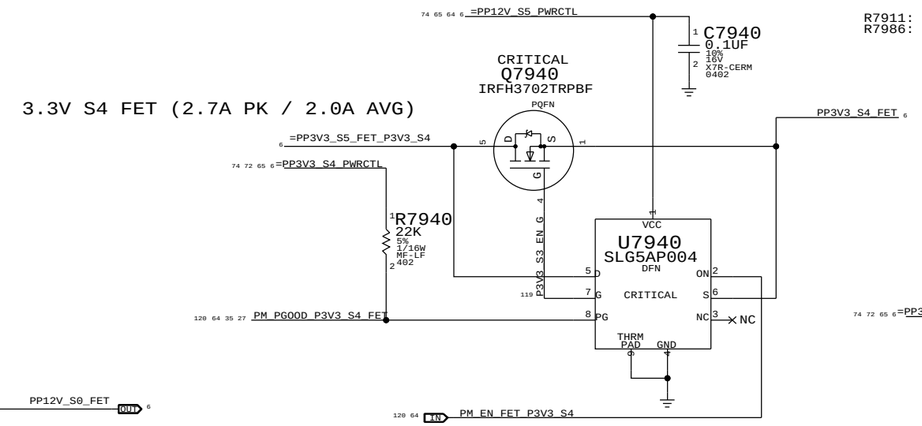
Max avg current: 6 A (BUDGET)
Max peak current: 6 A (BUDGET) SOFT START ON BLC



BLC12V BYPASS STUFFING OPTION

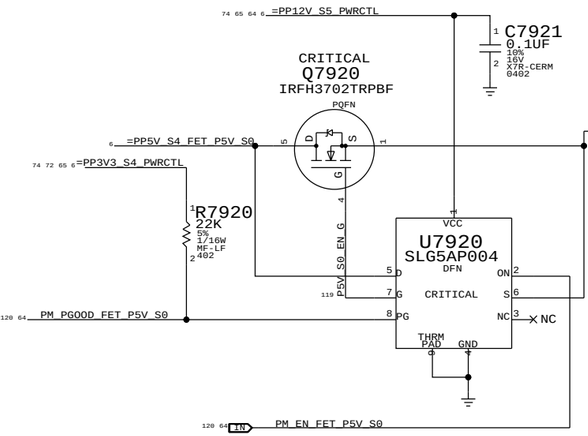
	BYPASS	NO BYPASS
R7911:	STUFF	NOSTUFF
R7986:	STUFF	NOSTUFF

3.3V S4 FET (2.7A PK / 2.0A AVG)



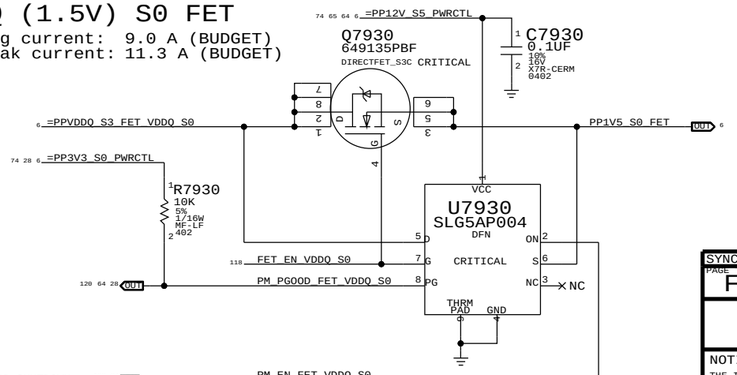
5V S0 FET

Max avg current: 2.7 A (BUDGET)
Max peak current: 3.9 A (BUDGET)



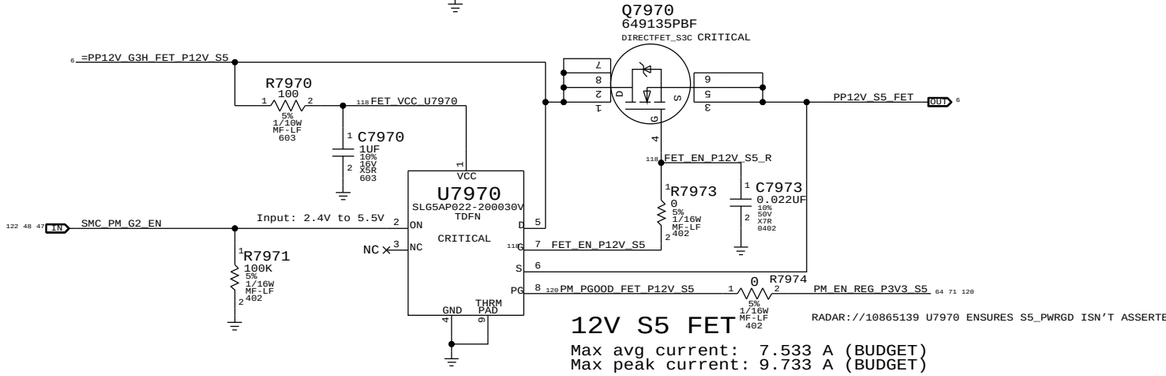
VDDQ (1.5V) S0 FET

Max avg current: 9.0 A (BUDGET)
Max peak current: 11.3 A (BUDGET)



12V S5 FET

Max avg current: 7.533 A (BUDGET)
Max peak current: 9.733 A (BUDGET)



RADAR://10865139 U7970 ENSURES S5_PWRGD ISN'T ASSERTED AFTER HARD SHUTDOWN.

SYNC_MASTER=D8_MLB	SYNC_DATE=08/27/2012
PAGE TITLE	FET-Controlled S0 and S4
Apple Inc.	DRAWING NUMBER 051-9505 SIZE D
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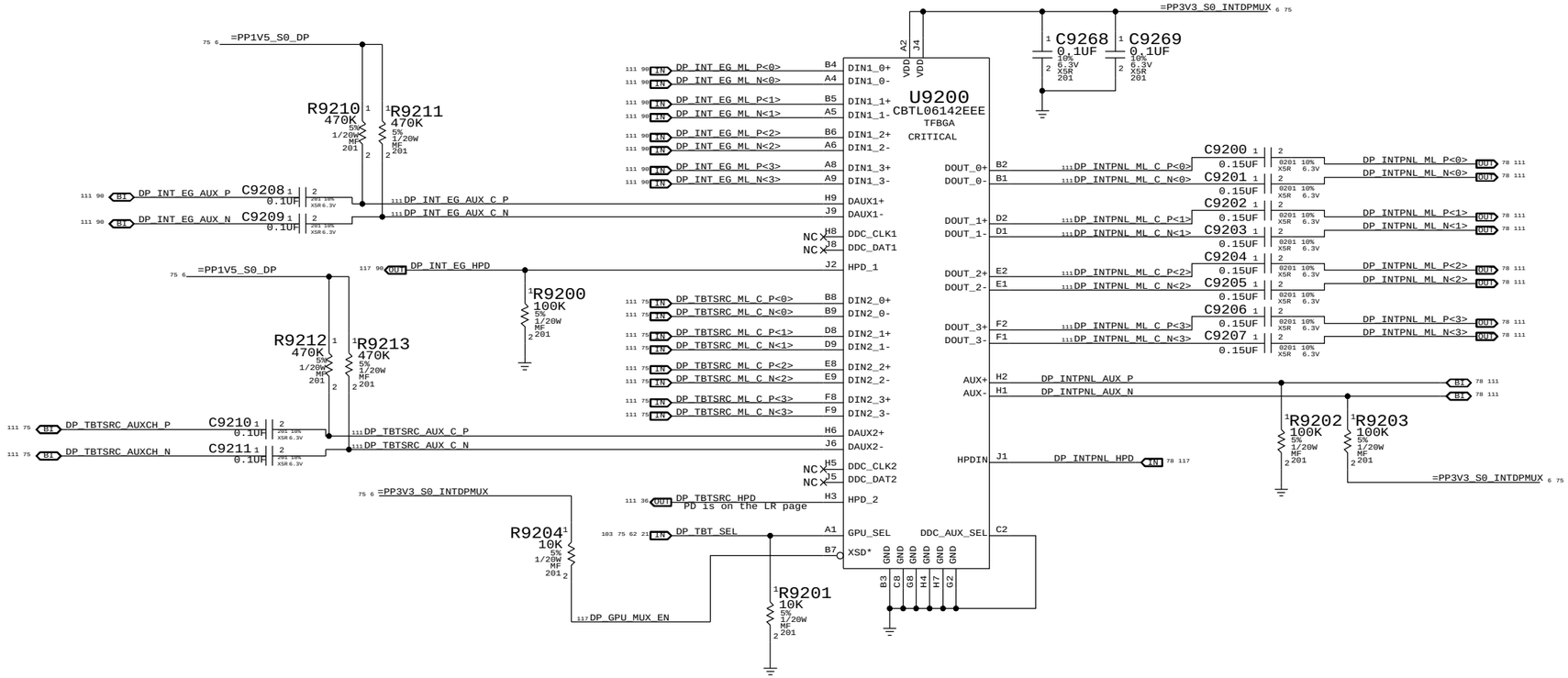
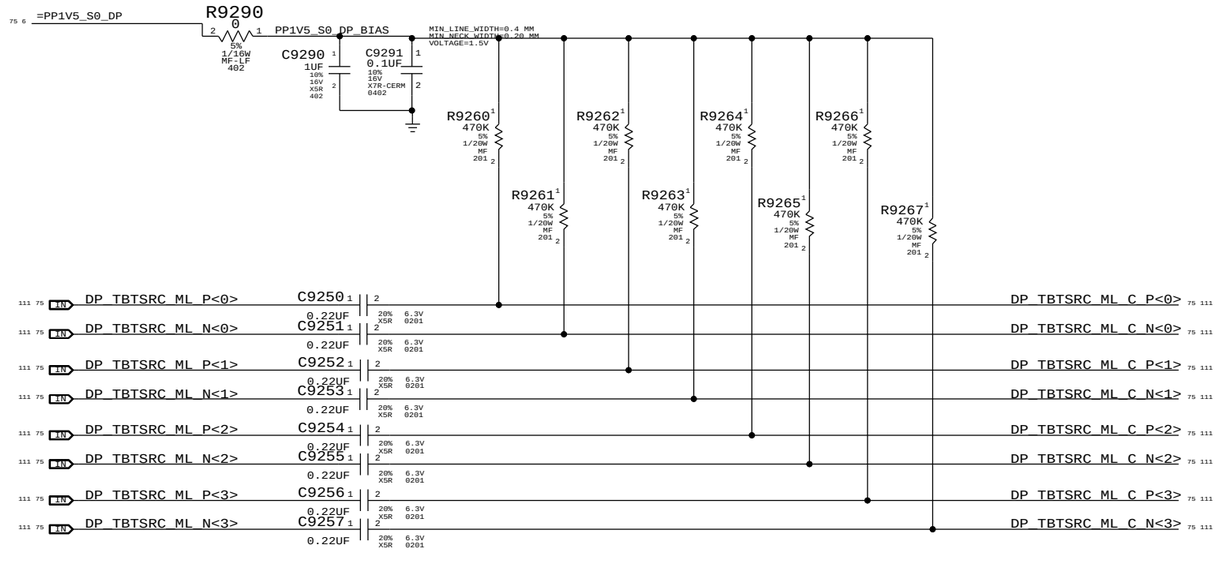
TP to DP aliases

TP_DP_TBTSRC_ML_CP<0>	=	DP_TBTSRC_ML_P<0>
TP_DP_TBTSRC_ML_CN<0>	=	DP_TBTSRC_ML_N<0>
TP_DP_TBTSRC_ML_CP<1>	=	DP_TBTSRC_ML_P<1>
TP_DP_TBTSRC_ML_CN<1>	=	DP_TBTSRC_ML_N<1>
TP_DP_TBTSRC_ML_CP<2>	=	DP_TBTSRC_ML_P<2>
TP_DP_TBTSRC_ML_CN<2>	=	DP_TBTSRC_ML_N<2>
TP_DP_TBTSRC_ML_CP<3>	=	DP_TBTSRC_ML_P<3>
TP_DP_TBTSRC_ML_CN<3>	=	DP_TBTSRC_ML_N<3>
TP_DP_TBTSRC_AUXCH_CP	=	DP_TBTSRC_AUXCH_P
TP_DP_TBTSRC_AUXCH_CN	=	DP_TBTSRC_AUXCH_N

All: MAKE_BASE=TRUE





SYNC_MASTER=D8_MLB	SYNC_DATE=08/27/2012
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Apple Inc.	DRAWING NUMBER 051-9505 · SIZE D
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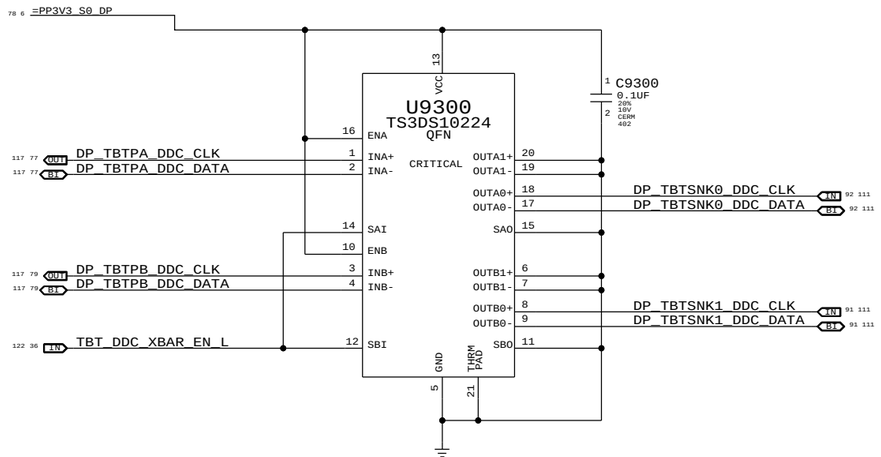
Dual-Port Host DDC Crossbar



SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012

PAGE TITLE

TBT DDC Crossbar

Apple Inc.

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3.3V/HV Power MUX

V3P3 must be S4 to support
wake from Thunderbolt devices.

	Nominal	Min	Max
IV3P3	1100mA	1030mA	1200mA
IHVS0	890mA	830mA	930mA (assumes 15V, 12W minimum)
IHVS3	890mA	830mA	930mA (assumes 3S, 9-12.6V, 7.5-11.7W)

=PP3V3_S4_TBTAPWRSW
CRITICAL C9487 100UF 20% 6.3V POLY-TANT CASE-B2-SM
CRITICAL C9480 22UF 20% 6.3V X5R-CERM-1 603
C9481 0.1UF 20% 10V CERM 402
=PPHV_SW_TBTAPWRSW 18.9V Max
C9415 4.7UF 10% 25V X5R-CERM 0603
C9410 0.1UF 10% 50V X7R 603-1
U9410 CRITICAL CD3210A0RGP QFN
V3P3OUT, NC, VHV, OUT, RSVD, EN, HV_EN, S0, ISET_V3P3, ISET_S0, ISET_S3, GND, THRM PAD
PPHV_SW_TBTAPWR MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=12V
C9411 0.1UF 10% 50V X7R 603-1
=TBTAPWRSW_EN
TBT_A_HV_EN
=TBT_S0_EN
TBTAPWRSW_ISET_V3P3
TBTAPWRSW_ISET_S0
TBTAPWRSW_ISET_S3
TBTHV:P15V
R9410 22.6K 1% 1/16W MF-LF 402
R9411 22.6K 1% 1/16W MF-LF 402
12V: See below
R9412 36.5K 1% 1/16W MF-LF 402
TBTAPWRSW_ISET_S3_R
TBTAPWRSW_ISET_S0_R
R9413 22.6K 1% 1/16W MF-LF 402
R9414 22.6K 1% 1/16W MF-LF 402
Two Rs in series required by CD3210 for single-fault protection(S0,S3 only)

For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0338	2	RES,MTL FILM,1/16W,17.8K,1,0402,SMD,LF	R9410,R9413		TBTHV:P12V
114S0338	2	RES,MTL FILM,1/16W,17.8K,1,0402,SMD,LF	R9411,R9414		TBTHV:P12V

	Nominal	Min	Max
IHVS0/S3	1120mA	1090mA	1170mA (12W minimum)

Thunderbolt Connector A

=PP3V3_S4_TBT
C9420 0.1UF 10% 6.3V X5R 201
C9421 0.1UF 10% 6.3V X5R 201
R9427 10K 5% 1/20W MF 201
R9429 100K 5% 1/20W MF 201
VDD
CRITICAL U9420 CBTL05023 HVQFN
TBT_A_BIAS VOLTAGE=3.3V
C9425 0.1UF 10% 6.3V X5R 201
TBT_A_CIO_SEL
DP_A_AUXIO_EN
DP_TBTPA_AUXCH_C_N
DP_TBTPA_AUXCH_C_P
C9430 0.1UF 10% 6.3V X5R 201
C9431 0.1UF 10% 6.3V X5R 201
DP_TBTPA_AUXCH_N
DP_TBTPA_AUXCH_P
DP_TBTPA_DDC_DATA
DP_TBTPA_DDC_CLK
TBT_A_CONFIG1_BUF
DP_TBTPA_ML_C_P<1>
DP_TBTPA_ML_C_N<1>
C9432 0.22UF 20% 6.3V X5R 0201
C9433 0.22UF 20% 6.3V X5R 0201
DP_TBTPA_ML_P<1>
DP_TBTPA_ML_N<1>
TBT_A_LSTX
TBT_A_LSRX_UNBUF
TBT_A_DP_PWRDN
DP_TBTPA_HPD
=PP3V3_S4_TBT
CRITICAL U9460 74AUP1T97 SOT891
TBT_A_LSRX
C9460 0.1UF 10% 16V X5R-CERM 0201
BIASIN, AUXIO_EN, AUX-, AUX+, DDC_DAT, DDC_CLK, CA_DETOUT, DP+, DP-, LSTX, LSRX, DP_PD, HPDOUT
BIASOUT, AUXIO-, AUXIO+, CA_DET, DPMLO+, DPMLO-, HPD, GND_THMPAD
DP_A_AUXCH_DDC_N
DP_A_AUXCH_DDC_P
TBT: RX_1 Bias Sink
TBT_A_CONFIG1_RC
DP_A_LSX_ML_P<1>
DP_A_LSX_ML_N<1>
TBT: LSX_A_R2P/P2R (P/N)
TBT_A_HPD
R9426 1M 5% 1/20W MF 201
R9428 100K 5% 1/20W MF 201

L9400 FERR-120-OHM-3A 0603
PP3V3RHV_SW_TBTAPWR MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=12V
C9400 0.01UF 10% 50V X7R-CERM 0402
TBTACONN_20_RC MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=18V
R9401 12 5% 1/20W MF 201
C9401 0.01UF 10% 50V X7R-CERM 0402
TBT Dir DP Dir

C9405 0.01UF 10% 25V X5R-CERM 0201
TBTACONN_1_C MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=18.9V
(0-18.9V)
DP Dir TBT Dir
TBT_A_R2D_P<0>
TBT_A_R2D_N<0>
TBT: TX_0
C9470 0.22UF 20% 6.3V X5R 0201
C9471 0.22UF 20% 6.3V X5R 0201
GND_VOID=TRUE (Both C's)
TBT_A_R2D_C_P<0>
TBT_A_R2D_C_N<0>
R9470 470K 5% 1/20W MF 201
R9471 470K 5% 1/20W MF 201

C9406 0.01UF 10% 25V X5R-CERM 0201
TBTACONN_7_C MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=18.9V
(0-18.9V)
DP_A_LSX_ML_P<1>
DP_A_LSX_ML_N<1>
TBT: LSX_R2P/P2R (P/N)

CRITICAL J9400 DUAL-MDP-D8 SHLD
F-ANG-TH
HPD, CONFIG1, CONFIG2, GND2, ML_LANE3P, ML_LANE3N, GND4, AUX_CHP, AUX_CHN, DP_PWR
GND0, ML_LANE0P, ML_LANE0N, GND1, ML_LANE1P, ML_LANE1N, GND3, ML_LANE2P, ML_LANE2N, RETURN
PORT A SHLD
514-0831

NOTE: Polarity Swapped for layout!
C9474 0.47UF 20% 4V CERM-X5R-1
C9475 0.47UF 20% 4V CERM-X5R-1
TBT_A_D2R_N<0>
TBT_A_D2R_P<0>
TBT_A_D2R_C_P<0>
TBT_A_D2R_C_N<0>
R9494 1K 5% 1/20W MF 201
R9495 1K 5% 1/20W MF 201
SIGNAL_MODEL=EMPTY
C9478 0.22UF 20% 6.3V X5R 0201
C9479 0.22UF 20% 6.3V X5R 0201
DP_TBTPA_ML_C_P<3>
DP_TBTPA_ML_C_N<3>
TBT: Terminated
R9478 470K 5% 1/20W MF 201
R9479 470K 5% 1/20W MF 201
TBT_A_BIAS
R9498 2.2K 5% 1/20W MF 201
R9499 2.2K 5% 1/20W MF 201
NOTE: Polarity Swapped for layout!
C9476 0.47UF 20% 4V CERM-X5R-1
C9477 0.47UF 20% 4V CERM-X5R-1
TBT_A_D2R_N<1>
TBT_A_D2R_P<1>
TBT_A_D2R_C_P<1>
TBT_A_D2R_C_N<1>
CRITICAL D9498 BAR90-02LRH TSLP-2-7
CRITICAL D9499 BAR90-02LRH TSLP-2-7
TBT_A_D2R1_AUXDDC_P
TBT_A_D2R1_AUXDDC_N
CRITICAL L9498 650NH-5%-0.430MA-0.52OHM 0603
CRITICAL L9499 650NH-5%-0.430MA-0.52OHM 0603
DP_A_AUXCH_DDC_P
DP_A_AUXCH_DDC_N
C9498 30PF 5% 50V C0G-NP0 0402
C9499 30PF 5% 50V C0G-NP0 0402
TBT_A_HPD
TBT_A_CONFIG1_RC
TBT_A_CONFIG2_RC
R9452 1M 5% 1/20W MF 201
R9451 1M 5% 1/20W MF 201
C9494 330PF 10% 16V X7R-CERM 0201
C9495 330PF 10% 16V X7R-CERM 0201
R9441 100K 5% 1/20W MF 201
C9402 0.01UF 10% 25V X5R-CERM 0201

DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

NOTE: Polarity Swapped for layout!
C9472 0.22UF 20% 6.3V X5R 0201
C9473 0.22UF 20% 6.3V X5R 0201
TBT_A_R2D_C_N<1>
TBT_A_R2D_C_P<1>
R9472 470K 5% 1/20W MF 201
R9473 470K 5% 1/20W MF 201
470k R's for ESD protection on AC-coupled signals.

SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012
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Apple Inc.
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INTERNAL DP (STRAIGHT)

518S0852 CRITICAL

J9500
20525-140E-01
F-RT-SM

L9500
FERR-120-OHM-3A
0603
155S0367

78 6 =PP12V_S0_LCD — 1 — 2 — 120 PP12V_LCD
VOLTAGE=12V
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.1 mm

C9520 10UF 10% 16V X5R-CERM 0805
C9501 0.001UF 20% 50V CERM 0402

Display TCon Master
- 118 50 BI I2C_TCON_MAS_SDA
- 118 50 OUT I2C_TCON_MAS_SCL

Display TCon Slave
- 50 IN =I2C_TCON_SLA_SDA
- 50 BI =I2C_TCON_SLA_SCL

- 111 56 OUT DP_INT_SPDIF_AUDIO
- 117 75 OUT DP_INTPNL_HPD
- 111 75 BI DP_INTPNL_AUX_N
- 111 75 BI DP_INTPNL_AUX_P
- 111 75 IN DP_INTPNL_ML_P<0>
- 111 75 IN DP_INTPNL_ML_N<0>
- 111 75 IN DP_INTPNL_ML_P<1>
- 111 75 IN DP_INTPNL_ML_N<1>
- 111 75 IN DP_INTPNL_ML_P<2>
- 111 75 IN DP_INTPNL_ML_N<2>
- 111 75 IN DP_INTPNL_ML_P<3>
- 111 75 IN DP_INTPNL_ML_N<3>
- 111 78 74 OUT VIDEO_ON
- 117 80 OUT BLC_VSYNC

K6X BACKLIGHT CONTROL SUPPORT

guarantee backlight is
only on when Panel has valid video

78 76 6 =PP3V3_S0_DP — C9502 0.1UF 20% 10V CERM 402

U9501 74AUP2G14GM SOT886
111 78 74 VIDEO_ON — 1
VIDEO_ON_K6X — 6
2

R9505 0 5% 1/16W MF-LF 402 — used by diag LED
VIDEO_ON_L OUT 5 78 111

D9501 SOT23 BAT54XG
R9503 20.0K 1% 1/10W MF-LF 402

78 76 6 =PP3V3_S0_DP — C9503 10UF 10% 16V X5R-CERM 0805 — C9504 0.1UF 20% 10V CERM 402

U9502 74AUP2G14GM SOT886
VIDEO_ON_L_DLY — 3
LCD_BKL_ON_DLY — 4
2

R9504 47 5% 1/10W MF-LF 402
BLC_EN OUT 78 80 81 117

Backlight Control

U9500 OUTPUT Y2 IS A NON-INVERTED, DELAYED VERSION OF INPUT A
The delay applies only on a L->H transition on A. This guarantees video is valid before the backlight is enabled.
On a H->L transition of A, Y2 follows with standard logic propagation delay. This ensures the backlight is off immediately after loss of video
Y1 is simply an inverted version of A, with no delay

78 76 6 =PP3V3_S0_DP — NOSTUFF C9506 0.1UF 20% 10V CERM 402

U9500 SN1105002 SC70 CRITICAL
1 VCC
111 78 74 IN VIDEO_ON — 3 A
NC — 6 NC
ipd
GND — 2
Y1 — 5
Y2 — 4 — 117 BLC_EN_DELAY

NOSTUFF R9506 0 5% 1/16W MF-LF 402
VIDEO_ON_D8_L — 1 — 2 — VIDEO_ON_L OUT 5 78 111
TO DIAGS LED

NOSTUFF R9502 0 5% 1/16W MF-LF 402
1 — 2 — BLC_EN — To BLC OUT 78 80 81 117

NOSTUFF R9501 0 5% 1/16W MF-LF 402
1 — 2

78 76 6 =PP3V3_S0_DP

U9501 74AUP2G14GM SOT886
3 — NC
2

U9502 74AUP2G14GM SOT886
1 — NC
2

DEVELOPMENT
L9520
FERR-250-OHM
SM
78 6 =PP12V_S0_LCD — 1 — 2 — 120 PP12V_LCD_EXT
VOLTAGE=12V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM

C9530 10UF 10% 16V X5R-CERM 0805 — DEVELOPMENT
C9531 0.001UF 20% 50V CERM 0402 — DEVELOPMENT

518S0778
DEVELOPMENT
CRITICAL
J9520
53780-8606
M-RT-SM
7
1 2 3 4 5 6 8

SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012

PAGE TITLE
Internal DP Support

Apple Inc.

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3.3V/HV Power MUX

V3P3 must be S4 to support
wake from Thunderbolt devices.

=PP3V3_S4_TBTBPWRSW

	Nominal	Min	Max
IV3P3	1100mA	1030mA	1200mA
IHVS0	890mA	830mA	930mA (assumes 15V, 12W minimum)
IHVS3	890mA	830mA	930mA (assumes 3S, 9-12.6V, 7.5-11.7W)

CRITICAL C9687 100UF 20% 6.3V POLY-TANT CASE-B2-SM
CRITICAL C9680 22UF 20% 6.3V X5R-CERM-1 603
C9681 0.1UF 20% 10V CERM 402

=PPHV_SW_TBTBPWRSW
18.9V Max
C9615 4.7UF 10% 25V X5R-CERM 0603
C9610 0.1UF 10% 50V X7R 603-1

CRITICAL U9610 CD3210A0RGP QFN
V3P3 (19,20) V3P3OUT (18) NC
VHV (6,7) OUT (12,14) PPHV_SW_TBTBPWR (21)
MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=12V
C9611 0.1UF 10% 50V X7R 603-1
RSVD (16) RSVD (15)
EN (5) ISET_V3P3 (8) TBTBPWRSW_ISET_V3P3
HV_EN (11) ISET_S0 (10) TBTBPWRSW_ISET_S0
S0 (17) ISET_S3 (9) TBTBPWRSW_ISET_S3
GND (1,2,3,4,13,21) THRM PAD

=TBTBPWRSW_EN
TBT_B_HV_EN
=TBT_S0_EN

TBTHV:P15V
R9610 22.6K 1% 1/16W MF-LF 402
R9611 22.6K 1% 1/16W MF-LF 402
R9612 36.5K 1% 1/16W MF-LF 402
12V: See below
TBTBPWRSW_ISET_S3_R
TBTBPWRSW_ISET_S0_R
TBTHV:P15V
R9613 22.6K 1% 1/16W MF-LF 402
R9614 22.6K 1% 1/16W MF-LF 402
Two Rs in series required by CD3210 for single-fault protection(S0,S3 only)

For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0338	2	RES,MTL FILM,1/16W,17.8K,1,0402,SMD,LF	R9610,R9613		TBTHV:P12V
114S0338	2	RES,MTL FILM,1/16W,17.8K,1,0402,SMD,LF	R9611,R9614		TBTHV:P12V

	Nominal	Min	Max
IHVS0/S3	1120mA	1090mA	1170mA (12W minimum)

Thunderbolt Connector B

=PP3V3_S4_TBT

C9620 0.1UF 10% 6.3V X5R 201
C9621 0.1UF 10% 6.3V X5R 201
R9627 10K 5% 1/20W MF 201
R9629 100K 5% 1/20W MF 201

CRITICAL U9620 CBTL05023 HVQFN
VDD (15)

TBT_B_CIO_SEL	1	BIASIN	BIASOUT 24
DP_AUXIO_EN	2	AUXIO_EN	
DP_TBTPB_AUXCH_C_N	7	AUX-	AUXIO- 23
DP_TBTPB_AUXCH_C_P	8	AUX+	AUXIO+ 22
DP_TBTPB_DDC_DATA	4	DDC_DAT	
DP_TBTPB_DDC_CLK	5	DDC_CLK	
TBT_B_CONFIG1_BUF	16	CA_DETOUT	CA_DET 18
DP_TBTPB_ML_C_P<1>	11	DP+	
DP_TBTPB_ML_C_N<1>	10	DP-	DPMLO+ 19
TBT_B_LSTX	14	LSTX	DPMLO- 20
TBT_B_LSRX_UNBUF	13	LSRX	
TBT_B_DP_PWRDN	6	DP_PD	
DP_TBTPB_HPD	12	HPDOUT	HPD 17

GND_THMPAD (9,21,25)

TBT_B_BIAS (VOLTAGE=3.3V)
C9625 0.1UF 10% 6.3V X5R 201

DP_B_AUXCH_DDC_N
DP_B_AUXCH_DDC_P
TBT: RX_1 Bias Sink
TBT_B_CONFIG1_RC
DP_B_LSX_ML_P<1>
DP_B_LSX_ML_N<1>
TBT: LSX_A_R2P/P2R (P/N)
TBT_B_HPD

C9630 0.1UF 10% 6.3V X5R 201
C9631 0.1UF 10% 6.3V X5R 201
C9632 0.22UF 20% 6.3V X5R 0201
C9633 0.22UF 20% 6.3V X5R 0201

R9626 1M 5% 1/20W MF 201
R9628 100K 5% 1/20W MF 201

CRITICAL U9660 74AUP1T97 SOT891
TBT_B_LSRX
C9660 0.1UF 10% 16V X5R-CERM 0201

L9600 FERR-120-OHM-3A 0603
PP3V3RHV_SW_TBTBPWR
MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=12V
C9600 0.01UF 10% 50V X7R-CERM 0402
C9601 0.01UF 10% 50V X7R-CERM 0402
R9601 12 5% 1/20W MF 201

TBTBCONN_20_RC
MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=18V

TBT Dir DP Dir

C9605 0.01UF 10% 25V X5R-CERM 0201
TBTBCONN_1_C MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=18.9V
(0-18.9V)
DP Dir TBT Dir
TBT_B_R2D_P<0>
TBT_B_R2D_N<0>
TBT: TX_0

C9606 0.01UF 10% 25V X5R-CERM 0201
TBTBCONN_7_C MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=18.9V
(0-18.9V)
DP_B_LSX_ML_P<1>
DP_B_LSX_ML_N<1>
TBT: LSX_R2P/P2R (P/N)
TBT_B_R2D_P<1>
TBT_B_R2D_N<1>
TBT: TX_1

GND_VOID=TRUE (Both C's)
C9670 0.22UF 20% 6.3V X5R 0201
C9671 0.22UF 20% 6.3V X5R 0201
R9670 470K 5% 1/20W MF 201
R9671 470K 5% 1/20W MF 201
TBT_B_R2D_C_P<0>
TBT_B_R2D_C_N<0>

CRITICAL J9400 DUAL-MDP-D8 F-ANG-TH
SHLD (58,57,56,55,54,53)
PORT B SHLD (65,64,63,62,61,60,59)

HPD	22	GND0	21
CONFIG1	24	ML_LANE0P	23
CONFIG2	26	ML_LANE0N	25
GND2	28	GND1	27
ML_LANE3P	30	ML_LANE1P	29
ML_LANE3N	32	ML_LANE1N	31
GND4	34	GND3	33
AUX_CHP	36	ML_LANE2P	35
AUX_CHN	38	ML_LANE2N	37
DP_PWR	40	RETURN	39

514-0831

GND_VOID=TRUE (Both C's)
C9672 0.22UF 20% 6.3V X5R 0201
C9673 0.22UF 20% 6.3V X5R 0201
R9672 470K 5% 1/20W MF 201
R9673 470K 5% 1/20W MF 201
TBT_B_R2D_C_N<1>
TBT_B_R2D_C_P<1>

NOTE: Polarity Swapped for Layout!

470k R's for ESD protection on AC-coupled signals.

GND_VOID=TRUE (Both C's)
C9674 0.47UF 20% 4V CERM-X5R-1
C9675 0.47UF 20% 4V CERM-X5R-1
TBT_B_D2R_N<0>
TBT_B_D2R_P<0>
TBT_B_D2R_C_P<0>
TBT_B_D2R_C_N<0>

NOTE: Polarity Swapped for Layout!

R9694 1K 5% 1/20W MF 201 SIGNAL_MODEL=EMPTY
R9695 1K 5% 1/20W MF 201 SIGNAL_MODEL=EMPTY

C9678 0.22UF 20% 6.3V X5R 0201
C9679 0.22UF 20% 6.3V X5R 0201
DP_TBTPB_ML_C_P<3>
DP_TBTPB_ML_C_N<3>
TBT: Terminated

R9678 470K 5% 1/20W MF 201
R9679 470K 5% 1/20W MF 201

R9698 2.2K 5% 1/20W MF 201
R9699 2.2K 5% 1/20W MF 201

GND_VOID=TRUE (Both C's)
C9676 0.47UF 20% 4V CERM-X5R-1
C9677 0.47UF 20% 4V CERM-X5R-1
TBT_B_D2R_N<1>
TBT_B_D2R_P<1>
TBT_B_D2R_C_P<1>
TBT_B_D2R_C_N<1>

NOTE: Polarity Swapped for Layout!

CRITICAL GND_VOID=TRUE (Both D's)
D9698 BAR90-02LRH TSLP-2-7
D9699 BAR90-02LRH TSLP-2-7
TBT_B_D2R1_AUXDDC_P
TBT_B_D2R1_AUXDDC_N

CRITICAL L9698 650NH-5%-0.430MA-0.52OHM 0603 GND_VOID=TRUE SIGNAL_MODEL=EMPTY
CRITICAL L9699 650NH-5%-0.430MA-0.52OHM 0603 GND_VOID=TRUE SIGNAL_MODEL=EMPTY

DP_B_AUXCH_DDC_P
DP_B_AUXCH_DDC_N

C9698 30PF 5% 50V C0G-NP0 0402
C9699 30PF 5% 50V C0G-NP0 0402

TBT_B_HPD
TBT_B_CONFIG1_RC
TBT_B_CONFIG2_RC

R9652 1M 5% 1/20W MF 201
R9651 1M 5% 1/20W MF 201
C9694 330PF 10% 16V X7R-CERM 0201
C9695 330PF 10% 16V X7R-CERM 0201
R9641 100K 5% 1/20W MF 201

C9602 0.01UF 10% 25V X5R-CERM 0201

DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

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Apple Inc.
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14V BLC PRE-REGULATOR

L9703 1KOHM-25%-0.6A 0603 — BLC_P3V3S
L9704 1KOHM-25%-0.6A 0603 — BLC_P3V3A
NOSTUFF L9702 1KOHM-25%-0.6A 0603 — BLC_P3V3_REF
=PP3V3_S0_BLC — R9701 0.100 0.1% 1/4W MF 1206 — PP3V3_S0_BLC_R
C9735 2.2UF 10% 16V X5R 603
C9733 1000PF 5% 25V C0G CERM 603
C9734 2.2UF 10% 16V X5R 603

PP12V_S0_BLC_VINP — R9752 0.001 1% 1W MF-LF 2512 — L9740 12UH-7A-0.02OHM PIMB136T-SM NOSTUFF — BOOST_FET_DRAIN
D9740 T0277A SS12P4S
Q9741 NOSTUFF FDMS6681Z POWER56
PRE_REG_OUT
C9748 10UF 10% 35V X5R 1210
C9749 470UF 20% 25V ELEC 10X10.8-SM
C9747 0.068UF 10% 50V X7R-CERM 0603

PRE_BOOST:Y R9743 330K 5% 1/10W MF-LF 603 — C9742 270PF 5% 50V CERM 603 — C9743 1.0UF 10% 50V X7R 0805 — R9744 10 1% 1/8W MF-LF 805 — BOOST_VDD
BOOST_EN_L
BOOST_COMP_C — C9741 0.1UF 10% 50V X7R 603-1
PRE_REG_OUT — R9740 0 5% 1/10W MF-LF 603 — PRE_REG_OUT_R
R9742 10K 1% 1/10W MF-LF 603 — C9740 1500PF 10% 50V CERM 603
R9741 22K 5% 1/10W MF-LF 603

U9740 TPS40210 MSOP
VDD
DIS/EN* — BOOST_BP — BOOST_GDRV — ISNS
COMP — FB — SS — RC — GND — THRM_PAD
BOOST_COMP — BOOST_FB — BOOST_SS — BOOST_RC

R9747 30.1 1% 1/10W MF-LF 603 — BOOST_GDRV_R
Q9740 CSD16412Q5A MLP5X6-LFPAK-Q5A
R9751 49.9K 1% 1/10W MF-LF 603
BOOST_BYPASS_GATE
R9750 49.9K 1% 1/10W MF-LF 603 — BOOST_BYPASS
R9748 1.0K 1% 1/10W MF-LF 603 — BOOST_ISNS_R
R9749 0.010 1% 1W MF 2010
R9745 1.10K 1% 1/8W MF-LF 805
C9746 0.1UF 10% 50V X7R 603-1
C9744 1.0UF 10% 50V X7R 0805
C9745 390PF 10% 50V X7R-CERM 0402

BLC_P3V3S — C9790 0.1UF 10% 16V X7R-CERM 0402
BLC_BL — U9780 74LVC1G08GW SOT353 — BLC_ENA1
BLC_ENA — R9780 100K 1% 1/10W MF-LF 603

PM_PCH_PWROK — U9710 74LVC2G08 SOT902 — PCH_BLC_EXT_BOOT
CRITICAL Q9711 SSM3K15AMFVAPE VESM
NOSTUFF R9711 100K 5% 1/16W MF-LF 402 — BLC_EXT_BOOT_L
BLC_EXT_BOOT — 0 R9712 — SMB_PCH_BLC_SDA

D8:SUOPERTEX GPIOS FOR BLC ISP RDAR://10987156

PM_PCH_PWROK — U9710 74LVC2G08 SOT902 — PCH_BLC_MCU_RESET
CRITICAL Q9710 SSM3K15AMFVAPE VESM
NOSTUFF R9710 100K 5% 1/16W MF-LF 402 — BLC_MCU_RESET_R_L
BLC_MCU_RESET — 0 R9713 — BLC_MCU_RESET_L
C9710 0.1UF 10% 6.3V X5R 201

NOSTUFF R9732 10K 5% 1/16W MF-LF 402
R9733 10K 5% 1/16W MF-LF 402
SMC_BLC_MUX_RX_L — 0 R9730 — BLC_MCU_TXD0
SMC_BLC_MUX_TX_L — 0 R9731 — BLC_MCU_RXD0

MCU ISP PROG AND TEST CONNECTOR

DEVELOPMENT J9700 CF20151D0R0-NH F-RT-SM — APN 998-3605
=PP3V3_S0_BLC
(WAS BLC_BLON)
BLC_EN
LCD_BKLT_PWM
BLC_VSYNC
BLC_MCU_TXD0
BLC_MCU_RXD0
BLC_MCU_B_SDA_CONN
BLC_MCU_RESET_L
BLC_MCU_TRST
BLC_MCU_TDI
BLC_MCU_TMS
BLC_MCU_TCK
BLC_MCU_RTCK
BLC_MCU_TDO
SMB_PCH_BLC_SDA
NOSTUFF J9701 HB3902U-L M-ST-TH

BLC_UVLO — R9726 0 5% 1/16W MF-LF 402
BLC_VSYNC — R9702 1K 5% 1/16W MF-LF 402 — R9703 100K 5% 1/16W MF-LF 402
SMB_PCH_BLC_SCL
TP_BLC_MCU_TP_2
SMB_PCH_BLC_SDA
FLAG_V — R9797 0 1/16W MF-LF 402
STRCLK_R1 — R9705 10K 5% 1/16W MF-LF 402
LCD_BKLT_PWM — R9706 1K 1% 1/16W MF-LF 402 — R9707 100K 5% 1/16W MF-LF 402
BLC_DIM_MCU
LED_DRIVER_OVP1P
LED_DRIVER_OVP2P
LED_DRIVER_OVP3P

BLC_P3V3S — C9701 1000PF 5% 50V C0G-CERM 603
C9702 1000PF 5% 50V C0G-CERM 603
C9703 1000PF 5% 50V C0G-CERM 603
C9704 0.1UF 10% 16V X7R-CERM 0402
C9708 0.1UF 10% 16V X7R-CERM 0402
C9709 1000PF 5% 50V C0G-CERM 603

NOSTUFF R9720 4.7K 5% 1/16W MF-LF 402
NOSTUFF R9721 4.7K 5% 1/16W MF-LF 402
NOSTUFF R9718 4.7K 5% 1/16W MF-LF 402
NOSTUFF R9719 4.7K 5% 1/16W MF-LF 402

U9700 LPC2132FBD64 LQFP
VDD — VDDA VREF VBAT OMIT_TABLE

BLC_MCU_TXD0 — P0.0/TXD0/PWM1
BLC_MCU_RXD0 — P0.1/RXD0/PWM3/EINT0
SMB_TCON_BLC_SCL — P0.2/SCL0/CAP0.0
SMB_TCON_BLC_SDA — P0.3/SDA0/MAT0.0/EINT1
BLC_GOOD — P0.4/SCK0/CAP0.1/AD0.6
BLC_MCU_UVLO — P0.5/MISO0/MAT0.1/AD0.7
BLC_VSYNC_R — P0.6/MOSI0/CAP0.2
BLC_PWM_1_R — P0.7/SSEL0/PWM2/EINT2
BLC_PWM_2_R — P0.8/TXD1/PWM4
BLC_PWM_3_R — P0.9/RXD1/PWM6/EINT3
P0.10/CAP1.0
P0.11/CAP1.1/SCL1
P0.12/MAT1.0
P0.13/MAT1.1
P0.14/EINT1/SDA1
P0.15/EINT2
P0.16/EINT0/MAT0.2/CAP0.2
BLC_ENA — P0.17/CAP1.2/SCK1/MAT1.2
P0.18/CAP1.3/MISO1/MAT1.3
P0.19/MAT1.2/MOSI1/CAP1.2
BLC_MCU_FLAG_V — P0.20/MAT1.3/SSEL1/EINT3
BLC_MCU_PWM5 — P0.21/PWM5/CAP1.3
P0.22/CAP0.0/MAT0.0
P0.23
P0.25/AD0.4/AOUT
P0.26/AD0.5
P0.27/AD0.0/CAP0.1/MAT0.1
P0.28/AD0.1/CAP0.2/MAT0.2
P0.29/AD0.2/CAP0.3/MAT0.3
P0.30/AD0.3/EINT3/CAP0.0
P0.31

P1.16/TRACEPKT0 — TP_PCH_GPIO6_TACH2
P1.17/TRACEPKT1 — BLC_EN_R
P1.18/TRACEPKT2 — NC
P1.19/TRACEPKT3 — NC
P1.20/TRACESYNC — NC
P1.21/PIPESTAT0 — NC
P1.22/PIPESTAT1 — NC
P1.23/PIPESTAT2 — NC
P1.24/TRACECLK — NC
P1.25/EXTIN0 — NC
P1.26/RTCK — BLC_MCU_RTCK
P1.27/TDO — BLC_MCU_TDO
P1.28/TDI — BLC_MCU_TDI
P1.29/TCK — BLC_MCU_TCK
P1.30/TMS — BLC_MCU_TMS
P1.31/TRST* (IPU) — BLC_MCU_TRST

(WAS BLC_GPIO)
R9727 10K 5% 1/16W MF-LF 402 — C9725 1000PF 5% 50V C0G-CERM 603
R9728 1K 5% 1/16W MF-LF 402 — BLC_EN
BLC_EN IS DRIVEN BY TCON (CSA95)

RESET* — BLC_MCU_RESET_L
XTALI — BLC_MCU_XTAL_IN
XTALO — BLC_MCU_XTAL_OUT_R
RTCX1 — NC
RTCX2 — NC
BLC_MCU_XTAL_OUT
R9716 0 5% 1/16W MF-LF 402
R9717 10M 5% 1/16W MF-LF 402
CRITICAL Y9705 3.2X2.5MM-SM 12.000MHZ-30PPM-10PF-85C
C9706 18PF 5% 50V C0G-CERM 0402
C9707 18PF 5% 50V C0G-CERM 0402
C9705 1UF 10% 16V X5R 402

D9700 BAS316DG SOD323-SM — BLC_P3V3S
R9715 10K 5% 1/16W MF-LF 402
R9781 100K 5% 1/16W MF-LF 402 — FLAG_V

VSS — VSSA

BLC MCU

U9770 L78M08ABDT DPAK — PP12V_S0_BLC_VIN2 — PP8V_BLC
353S3748
C9770 4.7UF 10% 16V X5R-CERM 0603
C9771 2.2UF 10% 25V X5R-CERM 603

BLC_BST — R9791 10K 5% 1/16W MF-LF 402 — BLC_BST_R
R9790 10K 5% 1/16W MF-LF 402
BLC_P_ON — U9790 74LVC1G08GW SOT353 — BOOST_EN_GATE
C9791 0.1UF 10% 16V X7R-CERM 0402
C9792 0.1UF 10% 16V X7R-CERM 0402
Q9701 2N7002 SOT23-HF1
R9793 10K 5% 1/16W MF-LF 402 — BOOST_EN_L
PP5V_S0_BLC_R — R9792 10K 5% 1/16W MF-LF 402

PP5V_S0_BLC_R — R9725 10K 1% 1/10W MF-LF 603 — BLC_MCU_BV
Q9700 BSH111DG SOT23-3
BLC_MCU_PWM5_R — R9724 10K 1% 1/10W MF-LF 603
C9722 1000PF 5% 50V C0G-CERM 603
R9722 0 5% 1/16W MF-LF 402

U9720 REF3333 SOT23-3
PP5V_S0_BLC_R — C9720 2.2UF 10% 16V X5R 603 — BLC_P3V3_REF
C9721 4.7UF 10% 6.3V X5R-CERM 603

D8 PROTO 2 BLC ADDING 3.3V VOLTAGE REFERENCE RDAR://11280328

SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012
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Apple Inc.
DRAWING NUMBER 051-9505 SIZE D
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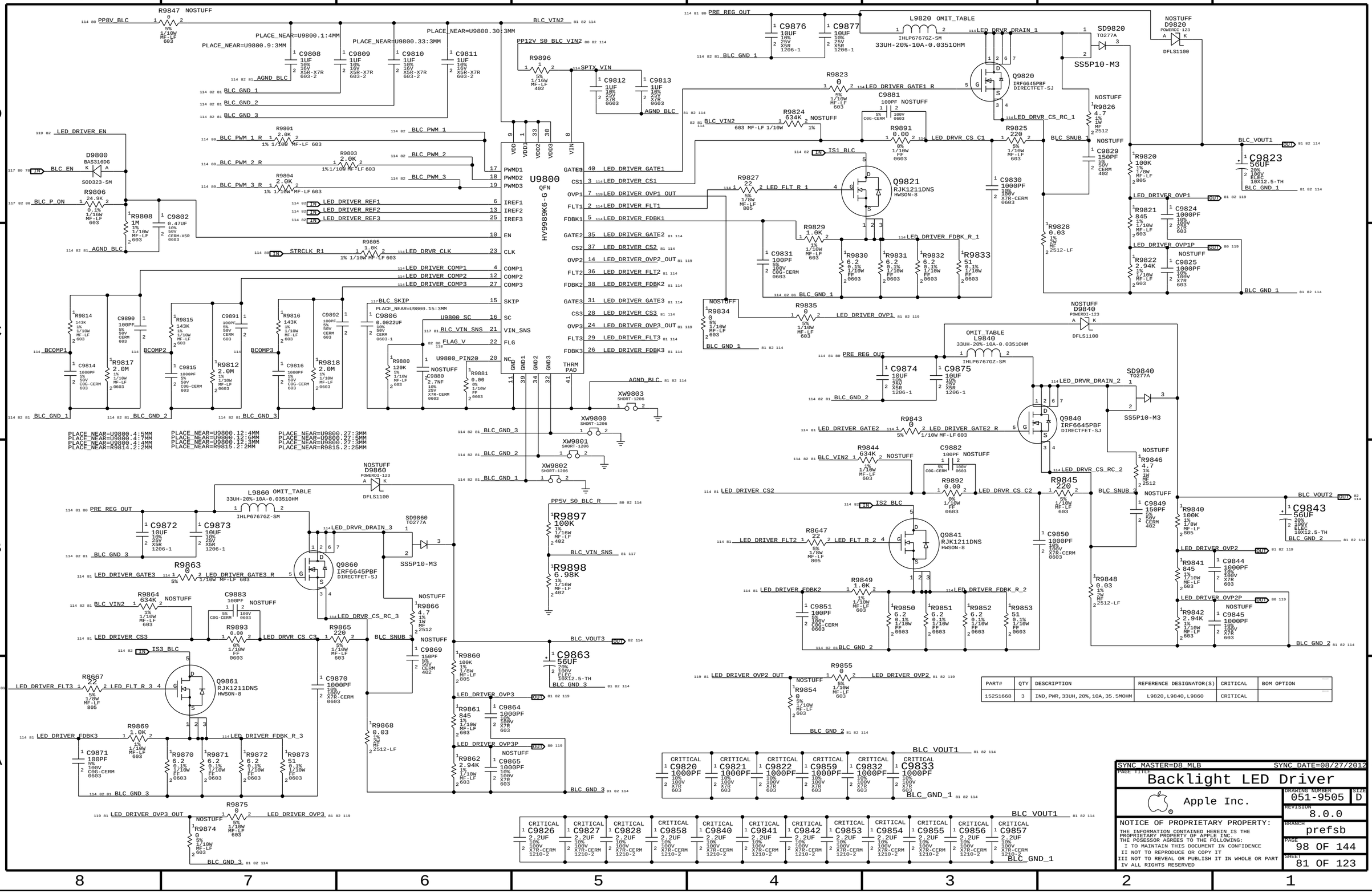

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
152S1668	3	IND,PWR,33UH,20%,10A,35.5MOHM	L9820,L9840,L9860	CRITICAL	

SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012

PAGE TITLE

Backlight LED Driver

Apple Inc.

DRAWING NUMBER 051-9505 SIZE D

REVISION 8.0.0

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Output Current Adjustment

IN-RUSH CURRENT LIMITER

OVP PROTECTION

Backlight Connector

BLC12V BYPASS STUFFING OPTION

	BYPASS	NO BYPASS
R9998:	STUFF	NOSTUFF
R9995:	NOSTUFF	STUFF
R9999:	STUFF	NOSTUFF
R9994:	NOSTUFF	STUFF
R9976:	STUFF	NOSTUFF

UVP PROTECTION

PWM <= 50% -> TURN ON BOOST
PWM > 50% -> TURN OFF BOOST

UVLO VIN2 BLC_BL

2.5V @12V = "1"
2.0V @10V = "0" (SHUTDOWN)

SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012

PAGE TITLE: Backlight Controller

Apple Inc.

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GPU PEX_IOVDD/Q 3300MA

UA000
BGA
SYM 1 OF 14
PCI_EXPRESS
GK104 GPU

NC	BJ21	PEX_WAKE*
GPU_RESET_L	BE20	PEX_RST*
PEG_CLKREQ_L	BB20	PEX_CLKREQ*
PEG_CLK100M_P	BD20	PEX_REFCLK
PEG_CLK100M_N	BC20	PEX_REFCLK*
PEG_D2R_P<0>	BC21	PEX_TX0
PEG_D2R_N<0>	BD21	PEX_TX0*
PEG_R2D_C_P<0>	BH21	PEX_RX0
PEG_R2D_C_N<0>	BG21	PEX_RX0*
PEG_D2R_P<1>	BE22	PEX_TX1
PEG_D2R_N<1>	BE23	PEX_TX1*
PEG_R2D_C_P<1>	BG23	PEX_RX1
PEG_R2D_C_N<1>	BH23	PEX_RX1*
PEG_D2R_P<2>	BD23	PEX_TX2
PEG_D2R_N<2>	BC23	PEX_TX2*
PEG_R2D_C_P<2>	BJ23	PEX_RX2
PEG_R2D_C_N<2>	BJ24	PEX_RX2*
PEG_D2R_P<3>	BC24	PEX_TX3
PEG_D2R_N<3>	BD24	PEX_TX3*
PEG_R2D_C_P<3>	BH24	PEX_RX3
PEG_R2D_C_N<3>	BG24	PEX_RX3*
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PEG_R2D_C_P<4>	BG26	PEX_RX4
PEG_R2D_C_N<4>	BH26	PEX_RX4*
PEG_D2R_P<5>	BD26	PEX_TX5
PEG_D2R_N<5>	BC26	PEX_TX5*
PEG_R2D_C_P<5>	BJ26	PEX_RX5
PEG_R2D_C_N<5>	BJ27	PEX_RX5*
PEG_D2R_P<6>	BC27	PEX_TX6
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PEG_R2D_C_P<6>	BH27	PEX_RX6
PEG_R2D_C_N<6>	BG27	PEX_RX6*
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PEG_R2D_C_P<7>	BG29	PEX_RX7
PEG_R2D_C_N<7>	BH29	PEX_RX7*
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PEG_D2R_N<8>	BC29	PEX_TX8*
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PEG_R2D_C_N<8>	BJ30	PEX_RX8*
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PEG_D2R_N<9>	BD30	PEX_TX9*
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PEG_R2D_C_N<9>	BG30	PEX_RX9*
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PEG_R2D_C_P<10>	BG32	PEX_RX10
PEG_R2D_C_N<10>	BH32	PEX_RX10*
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PEG_D2R_N<11>	BC32	PEX_TX11*
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PEG_R2D_C_N<11>	BJ33	PEX_RX11*
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PEG_D2R_N<12>	BD33	PEX_TX12*
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PEG_R2D_C_N<12>	BG33	PEX_RX12*
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PEG_D2R_N<13>	BE35	PEX_TX13*
PEG_R2D_C_P<13>	BG35	PEX_RX13
PEG_R2D_C_N<13>	BH35	PEX_RX13*
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PEG_D2R_N<14>	BC35	PEX_TX14*
PEG_R2D_C_P<14>	BJ35	PEX_RX14
PEG_R2D_C_N<14>	BJ36	PEX_RX14*
PEG_D2R_P<15>	BC36	PEX_TX15
PEG_D2R_N<15>	BD36	PEX_TX15*
PEG_R2D_C_P<15>	BH36	PEX_RX15
PEG_R2D_C_N<15>	BG36	PEX_RX15*

OMIT_TABLE

PLACE_NEAR=UA000.AY33:20MM
PLACE_NEAR=UA000.AY32:3.8MM
PLACE_NEAR=UA000.AW33:3.8MM

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PEX_IOVDD	AY32	
PEX_IOVDD	AY33	
PEX_IOVDD	AY35	
PEX_IOVDD	BA33	
PEX_IOVDD	BA35	
PEX_IOVDD	BB33	

NEAR GPU
CA001 1UF 10% 6.3V X7R 0402
CA002 1UF 10% 6.3V X7R 0402
CA003 4.7UF 20% 6.3V X6S 0402
CA004 22UF 20% 4V X6S-CERM 0603
CA005 22UF 20% 4V X6S-CERM 0603
CA006 10UF 20% 4V X6S 0402
CA007 10UF 20% 4V X6S 0402
UNDER GPU

PLACE_NEAR=UA000.AY26:20MM
PLACE_NEAR=UA000.AY26:3.8MM
PLACE_NEAR=UA000.AY24:3.8MM

PEX_IOVDDQ	AY24	
PEX_IOVDDQ	AY26	
PEX_IOVDDQ	AY27	
PEX_IOVDDQ	AY29	
PEX_IOVDDQ	AY30	
PEX_IOVDDQ	BA24	
PEX_IOVDDQ	BA26	
PEX_IOVDDQ	BA27	
PEX_IOVDDQ	BA29	
PEX_IOVDDQ	BA30	
PEX_IOVDDQ	BA32	
PEX_IOVDDQ	BB24	
PEX_IOVDDQ	BB27	
PEX_IOVDDQ	BB30	

NEAR GPU
CA008 1UF 10% 6.3V X7R 0402
CA009 1UF 10% 6.3V X7R 0402
CA010 4.7UF 20% 6.3V X6S 0402
CA011 22UF 20% 4V X6S-CERM 0603
CA012 22UF 20% 4V X6S-CERM 0603
CA013 10UF 20% 4V X6S 0402
CA014 10UF 20% 4V X6S 0402
UNDER GPU

GPU PLL_HVDD/PEX_SVVD 210MA

PLACE_NEAR=UA000.AW30:20MM
PLACE_NEAR=UA000.AW32:20MM
PLACE_NEAR=UA000.AW30:3.8MM
PLACE_NEAR=UA000.AW32:3.8MM

PEX_PLL_HVDD	AW30	=PP3V3_S0_GPU 6 91 92 95 96
PEX_SVDD_3V3	AW32	

PLACE NEAR GPU
CA092 4.7UF 20% 6.3V X6S 0402
CA093 4.7UF 20% 6.3V X6S 0402
CA094 0.1UF 10% 6.3V X6S 0201
CA095 0.1UF 10% 6.3V X6S 0201
PLACE NEAR GPU
ESR = 0.31OHM

RA002
200 1% 1/20W MF 201
NOSTUFF

PEX_TSTCLK_OUT	BH38	112 PEX_TSTCLK_O_PL
PEX_TSTCLK_OUT*	BG38	112 PEX_TSTCLK_O_NG

GPU PEX_PLLVDD 150MA

PEX_PLLVDD	AW26	PLACE_NEAR=UA000.AW26:20MM PLACE_NEAR=UA000.AW26:20MM =PP1V05_S0_GPU_PEX_PLLVDD 6 95

Place near GPU
CA087 4.7UF 20% 6.3V X6S 0402
CA088 1UF 10% 6.3V X7R 0402
CA089 0.1UF 10% 6.3V X6S 0201
PLACE_NEAR=UA000.AW26:3.8MM
PLACE UNDER GPU

TESTMODE	BA23	GPU_TESTMODE

RA006
10K 5% 1/16W MF-LF 402

PEX_TERMP	BJ38	PLACE_NEAR=UA000.BJ38:5MM

RA005
2.49K 1% 1/20W MF 201
112 GPU_PEX_TERMP

ALL LANES ARE REVERSED AND LANES 10,8,7,6,5,3,2,1 ARE POLARITY SWAPPED

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PEG_R2D_P<12>	CA026 0.22UF	PEG_R2D_C_P<3>
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PEG_R2D_P<9>	CA032 0.22UF	PEG_R2D_C_P<6>
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PEG_R2D_N<8>	CA034 0.22UF	PEG_R2D_C_P<7>
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ALL LANES ARE REVERSED AND LANES 15,14,13,11,10,8,7,6,5,2,0 ARE POLARITY SWAPPED

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Page Notes

Power aliases required by this page:
- =PP1V05_S0_GPU_PEX_IOVDD
- =PP3V3_S0_GPU
- =PP1V05_S0_GPU_PEX_PLLVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

SYNC_MASTER=D8_YAN
SYNC_DATE=04/09/2013
PAGE TITLE
KEPLER PCI-E

Apple Inc.

DRAWING NUMBER 051-9505
SIZE D
REVISION 8.0.0
BRANCH prefsb
PAGE 100 OF 144
SHEET 83 OF 123

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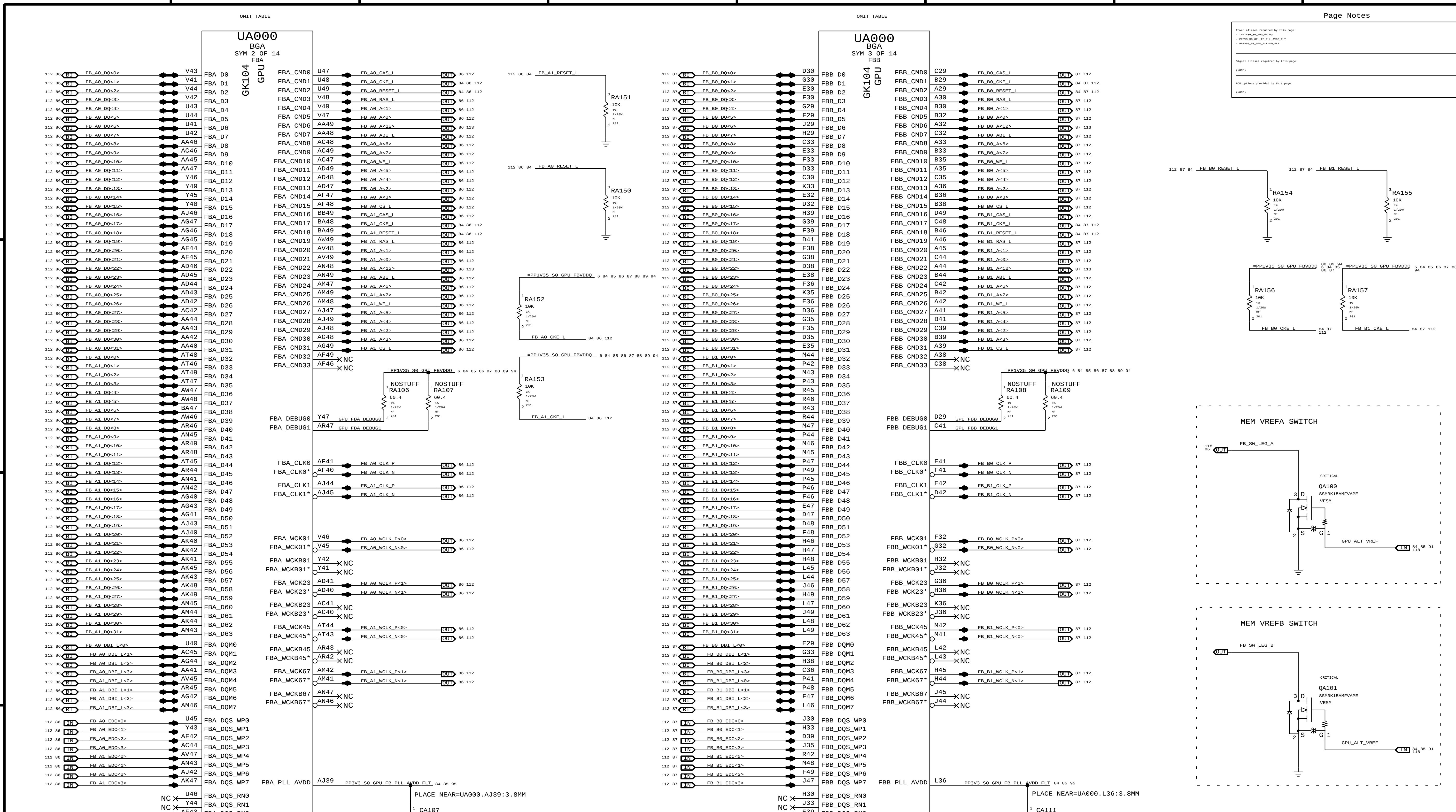

SYNC_MASTER=D8_YAN SYNC_DATE=04/09/2012

PAGE TITLE

KEPLER FRAME BUFFER A/B

Apple Inc.

DRAWING NUMBER 051-9505 SIZE D

REVISION 8.0.0

BRANCH prefsb

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SHEET 84 OF 123

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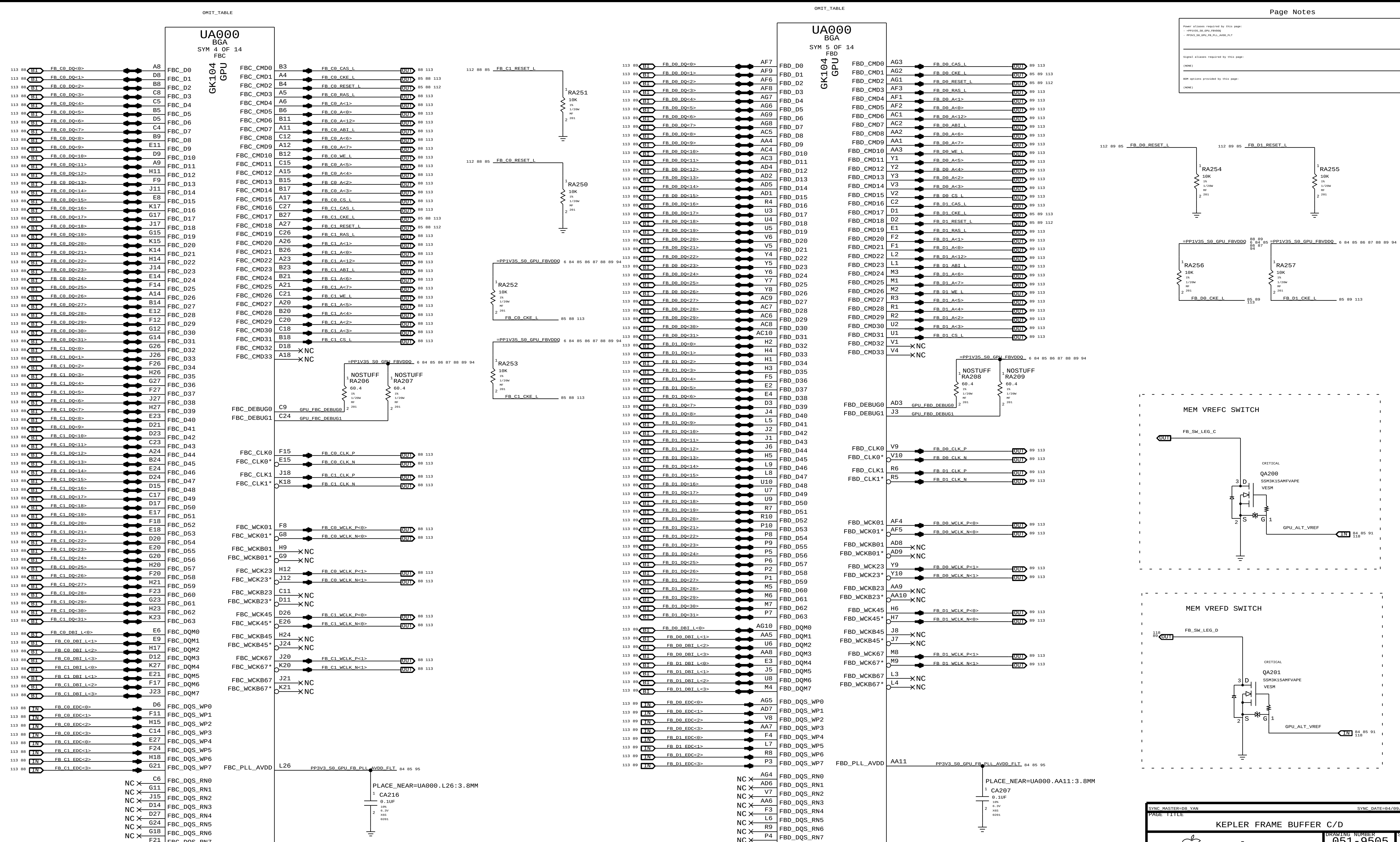

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SYNC_MASTER=D8_YAN SYNC_DATE=04/09/2012

PAGE TITLE

KEPLER FRAME BUFFER C/D

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Page Notes

Power aliases required by this page:

- =PP1V35_S0_GPU_FBVDD

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

CK TERMINATION - A0

RA301 40.2 1% 1/20W MF 201 — FB_A0_CLK_P — FB_A0_CK_MID
RA302 40.2 1% 1/20W MF 201 — FB_A0_CK_MID — FB_A0_CLK_N
CA390 0.01UF 10% 10V X5R-CERM 0201

CK TERMINATION - A1

RA351 40.2 1% 1/20W MF 201 — FB_A1_CLK_P — FB_A1_CK_MID
RA352 40.2 1% 1/20W MF 201 — FB_A1_CK_MID — FB_A1_CLK_N
CA391 0.01UF 10% 10V X5R-CERM 0201

RA300 120 1% 1/20W MF 201
RA304 1K 1% 1/20W MF 201
RA303 1K 1% 1/20W MF 201

MIRRORED

UA300 32MX32-1.5GHZ-MFH
BGA
K4G10325FG-HC03
(1 OF 2)

FB_A0_A<2>	K11	BA0/A2	
FB_A0_A<5>	H10	BA1/A5	
FB_A0_A<4>	H11	BA2/A4	
FB_A0_A<3>	K10	BA3/A3	
FB_A0_A<7>	H4	A8/A7	
FB_A0_A<1>	K5	A9/A1	
FB_A0_A<0>	K4	A10/A0	
FB_A0_A<6>	H5	A11/A6	
FB_A0_CKE_L	J3	CKE*	
FB_A0_CLK_P	J12	CK	
FB_A0_CLK_N	J11	CK*	
FB_A0_CS_L	L12	CS*	
FB_A0_WE_L	G12	WE*	
FB_A0_CAS_L	G3	CAS*	
FB_A0_RAS_L	L3	RAS*	
FB_A0_ZQ	J13	ZQ	
FB_A0_MF	J1	MF (MF=1)	
FB_A0_SEN	J10	SEN	
FB_A0_RESET_L	J2	RESET*	
FB_A0_ABI_L	J4	ABI*	
FB_A0_EDC<0>	R2	EDC0	
FB_A0_EDC<1>	R13	EDC1	
FB_A0_EDC<2>	C13	EDC2	
FB_A0_EDC<3>	C2	EDC3	
FB_A0_WCLK_P<0>	P4	WCK01	
FB_A0_WCLK_N<0>	P5	WCK01*	
FB_A0_WCLK_P<1>	D4	WCK23	
FB_A0_WCLK_N<1>	D5	WCK23*	

OMIT_TABLE

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OMIT_TABLE

UA300 32MX32-1.5GHZ-MFH
BGA
K4G10325FG-HC03
(2 OF 2)

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VDDQ	B1 E10 F1 F3 F12 F14 G2 G13 H3 H12 K3 B3 K12 L2 L13 M1 M3 M12 M14 N5 N10 P1 B12 P3 P12 P14 T1 T3 T12 T14 B14 D1 D3 D12 D14 E5	
VSS	B5 L5 L10 P10 T5 T10 B10 D10 G5 G10 H1 H14 K1 K14	
VSSQ	A1 C14 E1 E3 E12 E14 F5 F10 H2 H13 K2 A3 K13 M5 M10 N1 N3 N12 N14 R1 R3 R4 A12 R11 R12 R14 U1 U3 U12 U14 A14 C1 C3 C4 C11 C12	
VREFC	J14	FB_A0_VREFC
VREFD	A10 U10	FB_A0_VREFD

PLACE CLOSE TO UA300

RA330 549 1% 1/20W MF 201 — =PP1V35_S0_GPU_FBVDDQ
RA331 1.33K 1% 1/20W MF 201 — FB_A0_VREFC — MIN_LINE_WIDTH=0.25 MM, MIN_NECK_WIDTH=0.1 mm
RA334 931 1% 1/20W MF 201 — FB_SW_LEG_A
CA331 820PF 10% 50V CERM 0402

RA332 549 1% 1/20W MF 201 — =PP1V35_S0_GPU_FBVDDQ
RA333 1.33K 1% 1/20W MF 201 — FB_A0_VREFC — MIN_LINE_WIDTH=0.25 MM, MIN_NECK_WIDTH=0.1 mm
RA335 931 1% 1/20W MF 201 — FB_SW_LEG_A
CA340 820PF 10% 50V CERM 0402
CA333 820PF 10% 50V CERM 0402

CA300 10UF 20% 6.3V X5R 603-3
CA301 10UF 20% 6.3V X5R 603-3
CA303 4.7UF 20% 6.3V X5R 402
CA304 4.7UF 20% 6.3V X5R 402
CA306 1UF 20% 6.3V X5R 0201
CA307 1UF 20% 6.3V X5R 0201
CA308 1UF 20% 6.3V X5R 0201
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CA319 0.1UF 10% 6.3V X5R 201
CA320 0.1UF 10% 6.3V X5R 201
CA321 0.1UF 10% 6.3V X5R 201
CA322 0.1UF 10% 6.3V X5R 201
CA323 0.1UF 10% 6.3V X5R 201
CA324 0.1UF 10% 6.3V X5R 201
CA325 0.1UF 10% 6.3V X5R 201

CA350 10UF 20% 6.3V X5R 603-3
CA351 10UF 20% 6.3V X5R 603-3
CA353 4.7UF 20% 6.3V X5R 402
CA354 4.7UF 20% 6.3V X5R 402
CA356 1UF 20% 6.3V X5R 0201
CA357 1UF 20% 6.3V X5R 0201
CA358 1UF 20% 6.3V X5R 0201
CA359 1UF 20% 6.3V X5R 0201
CA360 1UF 20% 6.3V X5R 0201
CA361 1UF 20% 6.3V X5R 0201
CA362 1UF 20% 6.3V X5R 0201
CA363 1UF 20% 6.3V X5R 0201
CA364 1UF 20% 6.3V X5R 0201
CA365 1UF 20% 6.3V X5R 0201
CA366 0.1UF 10% 6.3V X5R 201
CA367 0.1UF 10% 6.3V X5R 201
CA368 0.1UF 10% 6.3V X5R 201
CA369 0.1UF 10% 6.3V X5R 201
CA370 0.1UF 10% 6.3V X5R 201
CA371 0.1UF 10% 6.3V X5R 201
CA372 0.1UF 10% 6.3V X5R 201
CA373 0.1UF 10% 6.3V X5R 201
CA374 0.1UF 10% 6.3V X5R 201
CA375 0.1UF 10% 6.3V X5R 201

NORMAL

UA350 32MX32-1.5GHZ-MFL
BGA
K4G10325FG-HC03
(1 OF 2)

FB_A1_A<2>	H11	BA0/A2	
FB_A1_A<5>	K10	BA1/A5	
FB_A1_A<4>	K11	BA2/A4	
FB_A1_A<3>	H10	BA3/A3	
FB_A1_A<7>	K4	A8/A7	
FB_A1_A<1>	H5	A9/A1	
FB_A1_A<0>	H4	A10/A0	
FB_A1_A<6>	K5	A11/A6	
FB_A1_CKE_L	J3	CKE*	
FB_A1_CLK_P	J12	CK	
FB_A1_CLK_N	J11	CK*	
FB_A1_CS_L	G12	CS*	
FB_A1_WE_L	L12	WE*	
FB_A1_CAS_L	L3	CAS*	
FB_A1_RAS_L	G3	RAS*	
FB_A1_ZQ	J13	ZQ	
FB_A1_MF	J1	MF (MF=0)	
FB_A1_SEN	J10	SEN	
FB_A1_RESET_L	J2	RESET*	
FB_A1_ABI_L	J4	ABI*	
FB_A1_EDC<0>	C2	EDC0	
FB_A1_EDC<1>	C13	EDC1	
FB_A1_EDC<2>	R13	EDC2	
FB_A1_EDC<3>	R2	EDC3	
FB_A1_WCLK_P<0>	D4	WCK01	
FB_A1_WCLK_N<0>	D5	WCK01*	
FB_A1_WCLK_P<1>	P4	WCK23	
FB_A1_WCLK_N<1>	P5	WCK23*	

OMIT_TABLE

DBI0*	D2	FB_A1_DBI_L<0>	
DBI1*	D13	FB_A1_DBI_L<1>	
DBI2*	P13	FB_A1_DBI_L<2>	
DBI3*	P2	FB_A1_DBI_L<3>	
DQ0	A4	FB_A1_DQ<0>	
DQ1	A2	FB_A1_DQ<1>	
DQ2	B4	FB_A1_DQ<2>	
DQ3	B2	FB_A1_DQ<3>	
DQ4	E4	FB_A1_DQ<4>	
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DQ13	E13	FB_A1_DQ<13>	
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DQ16	U11	FB_A1_DQ<16>	
DQ17	U13	FB_A1_DQ<17>	
DQ18	T11	FB_A1_DQ<18>	
DQ19	T13	FB_A1_DQ<19>	
DQ20	N11	FB_A1_DQ<20>	
DQ21	N13	FB_A1_DQ<21>	
DQ22	M11	FB_A1_DQ<22>	
DQ23	M13	FB_A1_DQ<23>	
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DQ29	N2	FB_A1_DQ<29>	
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DQ31	M2	FB_A1_DQ<31>	
NC	A5	NC	
A12/RFU/NC	J5	FB_A1_A<12>	
NC	U5	NC	

UA350 32MX32-1.5GHZ-MFL
BGA
K4G10325FG-HC03
(2 OF 2)

VDD	C5 C10 D11 G1 G4 G11 G14 L1 L4 L11 L14 P11 R5 R10	
VDDQ	B1 B3 B12 B14 D1 D3 D12 D14 E5 E10 F1 F3 F12 F14 G2 G13 H3 H12 K3 K12 L2 L13 M1 M3 M12 M14 N5 N10 P1 P3 P12 P14 T1 T3 T12 T14	
VSS	B5 B10 D10 G5 G10 H1 H14 K1 K14 L5 L10 P10 T5 T10	
VSSQ	A1 A3 A12 A14 C1 C3 C4 C11 C12 C14 E1 E3 E12 E14 F5 F10 H2 H13 K2 K13 M5 M10 N1 N3 N12 N14 R1 R3 R4 R11 R12 R14 U1 U3 U12 U14	
VREFC	J14	FB_A1_VREFC
VREFD	A10 U10	FB_A1_VREFD

RA336 549 1% 1/20W MF 201 — =PP1V35_S0_GPU_FBVDDQ
RA337 1.33K 1% 1/20W MF 201 — FB_A1_VREFC — MIN_LINE_WIDTH=0.25 MM, MIN_NECK_WIDTH=0.1 mm
RA338 931 1% 1/20W MF 201 — FB_SW_LEG_A
CA381 820PF 10% 50V CERM 0402

RA339 549 1% 1/20W MF 201 — =PP1V35_S0_GPU_FBVDDQ
RA340 1.33K 1% 1/20W MF 201 — FB_A1_VREFD — MIN_LINE_WIDTH=0.25 MM, MIN_NECK_WIDTH=0.1 mm
RA341 931 1% 1/20W MF 201 — FB_SW_LEG_A
CA341 820PF 10% 50V CERM 0402
CA383 820PF 10% 50V CERM 0402

RA350 120 1% 1/20W MF 201
RA354 1K 1% 1/20W MF 201
RA353 1K 1% 1/20W MF 201

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PAGE TITLE	GDDR5 Frame Buffer A
Apple Inc.	DRAWING NUMBER 051-9505 SIZE D
	REVISION 8.0.0
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	PAGE 103 OF 144
	SHEET 86 OF 123

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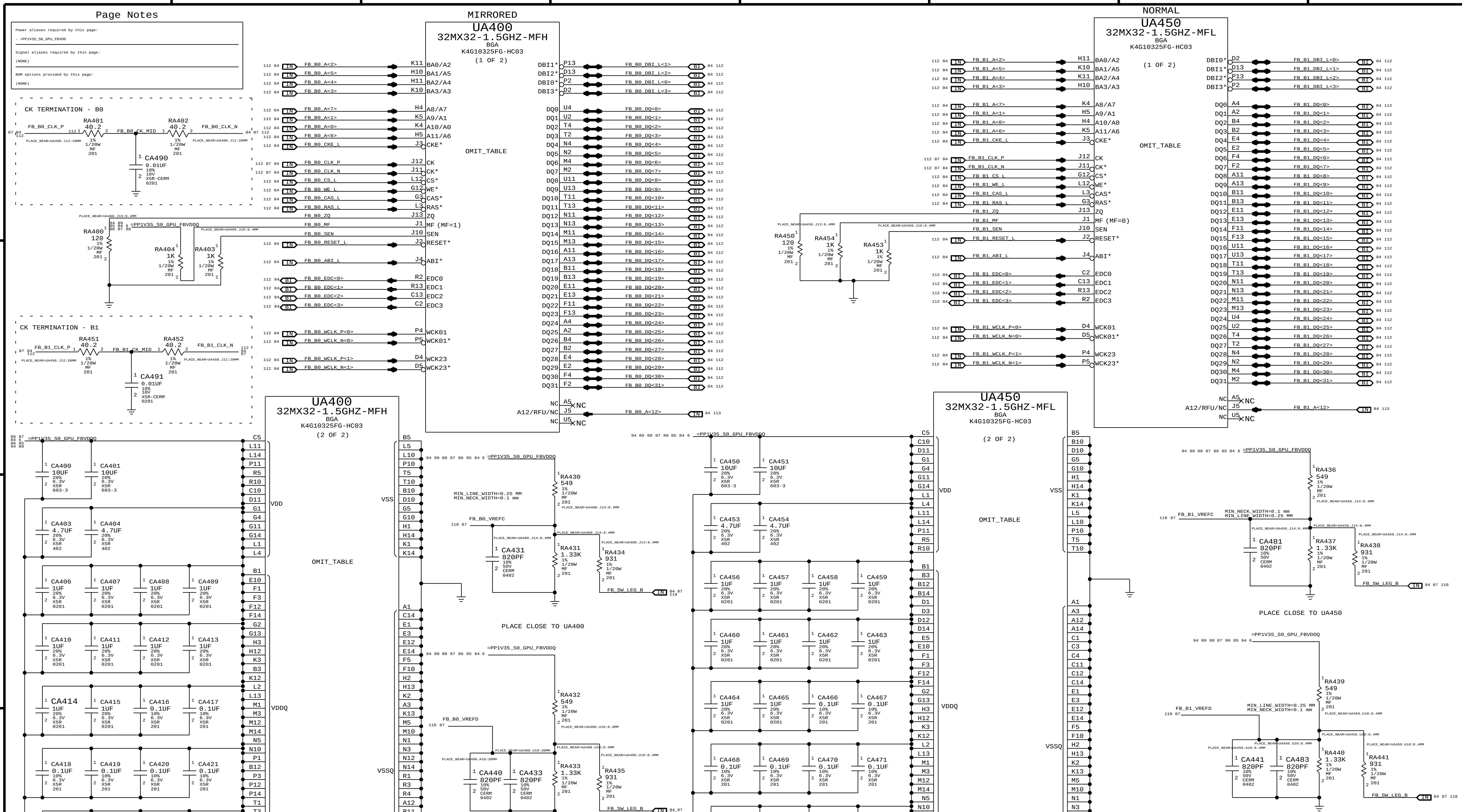

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SYNC_MASTER=D8_YAN SYNC_DATE=04/09/2012

PAGE TITLE

GDDR5 Frame Buffer B

Apple Inc.

DRAWING NUMBER 051-9505 SIZE D

REVISION 8.0.0

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Page Notes

Power aliases required by this page:

- =PP1V35_S0_GPU_FBVDD

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

CK TERMINATION - C0

FB_C0_CLK_P — RA501 40.2 1% 1/20W MF 201 — FB_C0_CK_MID — RA502 40.2 1% 1/20W MF 201 — FB_C0_CLK_N

PLACE_NEAR=UA500.J12:20MM, PLACE_NEAR=UA500.J11:20MM

CA590 0.01UF 10% 10V X5R-CERM 0201

CK TERMINATION - C1

FB_C1_CLK_P — RA551 40.2 1% 1/20W MF 201 — FB_C1_CK_MID — RA552 40.2 1% 1/20W MF 201 — FB_C1_CLK_N

PLACE_NEAR=UA550.J12:20MM, PLACE_NEAR=UA550.J11:20MM

CA591 0.01UF 10% 10V X5R-CERM 0201

MIRRORED

UA500 32MX32-1.5GHZ-MFH

BGA
K4G10325FG-HC03
(1 OF 2)

OMIT_TABLE

FB_C0_A<2>	K11	BA0/A2	
FB_C0_A<5>	H10	BA1/A5	
FB_C0_A<4>	H11	BA2/A4	
FB_C0_A<3>	K10	BA3/A3	
FB_C0_A<7>	H4	A8/A7	
FB_C0_A<1>	K5	A9/A1	
FB_C0_A<0>	K4	A10/A0	
FB_C0_A<6>	H5	A11/A6	
FB_C0_CKE_L	J3	CKE*	
FB_C0_CLK_P	J12	CK	
FB_C0_CLK_N	J11	CK*	
FB_C0_CS_L	L12	CS*	
FB_C0_WE_L	G12	WE*	
FB_C0_CAS_L	G3	CAS*	
FB_C0_RAS_L	L3	RAS*	
FB_C0_ZQ	J13	ZQ	
FB_C0_MF	J1	MF (MF=1)	
FB_C0_SEN	J10	SEN	
FB_C0_RESET_L	J2	RESET*	
FB_C0_ABI_L	J4	ABI*	
FB_C0_EDC<0>	R2	EDC0	
FB_C0_EDC<1>	R13	EDC1	
FB_C0_EDC<2>	C13	EDC2	
FB_C0_EDC<3>	C2	EDC3	
FB_C0_WCLK_P<0>	P4	WCK01	
FB_C0_WCLK_N<0>	P5	WCK01*	
FB_C0_WCLK_P<1>	D4	WCK23	
FB_C0_WCLK_N<1>	D5	WCK23*	

DBI1*	P13		FB_C0_DBI_L<1>
DBI2*	D13		FB_C0_DBI_L<2>
DBI0*	P2		FB_C0_DBI_L<0>
DBI3*	D2		FB_C0_DBI_L<3>
DQ0	U4		FB_C0_DQ<0>
DQ1	U2		FB_C0_DQ<1>
DQ2	T4		FB_C0_DQ<2>
DQ3	T2		FB_C0_DQ<3>
DQ4	N4		FB_C0_DQ<4>
DQ5	N2		FB_C0_DQ<5>
DQ6	M4		FB_C0_DQ<6>
DQ7	M2		FB_C0_DQ<7>
DQ8	U11		FB_C0_DQ<8>
DQ9	U13		FB_C0_DQ<9>
DQ10	T11		FB_C0_DQ<10>
DQ11	T13		FB_C0_DQ<11>
DQ12	N11		FB_C0_DQ<12>
DQ13	N13		FB_C0_DQ<13>
DQ14	M11		FB_C0_DQ<14>
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DQ16	A11		FB_C0_DQ<16>
DQ17	A13		FB_C0_DQ<17>
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DQ22	F11		FB_C0_DQ<22>
DQ23	F13		FB_C0_DQ<23>
DQ24	A4		FB_C0_DQ<24>
DQ25	A2		FB_C0_DQ<25>
DQ26	B4		FB_C0_DQ<26>
DQ27	B2		FB_C0_DQ<27>
DQ28	E4		FB_C0_DQ<28>
DQ29	E2		FB_C0_DQ<29>
DQ30	F4		FB_C0_DQ<30>
DQ31	F2		FB_C0_DQ<31>
NC	A5		
A12/RFU/NC	J5		FB_C0_A<12>
NC	U5		

UA500 32MX32-1.5GHZ-MFH

BGA
K4G10325FG-HC03
(2 OF 2)

OMIT_TABLE

=PP1V35_S0_GPU_FBVDDQ	C5	
	L11	
	L14	
	P11	
	R5	
	R10	
	C10	
VDD	D11	
	G1	
	G4	
	G11	
	G14	
	L1	
	L4	
	B1	
	E10	
	F1	
	F3	
	F12	
	F14	
	G2	
	G13	
	H3	
	H12	
	K3	
	B3	
	K12	
	L2	
	L13	
VDDQ	M1	
	M3	
	M12	
	M14	
	N5	
	N10	
	P1	
	B12	
	P3	
	P12	
	P14	
	T1	
	T3	
	T12	
	T14	
	B14	
	D1	
	D3	
	D12	
	D14	
	E5	
FB_C0_VREFC	J14	VREFC
FB_C0_VREFD	A10	VREFD
	U10	

	B5	
	L5	
	L10	
	P10	
	T5	
	B10	
	D10	
	G5	
VSS	G10	
	H1	
	H14	
	K1	
	K14	
	A1	
	C14	
	E1	
	E3	
	E12	
	E14	
	F5	
	F10	
	H2	
	H13	
	K2	
	A3	
	K13	
	M5	
	M10	
	N1	
	N3	
	N12	
VSSQ	N14	
	R1	
	R3	
	R4	
	A12	
	R11	
	R12	
	R14	
	U1	
	U3	
	U12	
	U14	
	A14	
	C1	
	C3	
	C4	
	C11	
	C12	

PLACE CLOSE TO UA500

MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.1 mm

NORMAL

UA550 32MX32-1.5GHZ-MFL

BGA
K4G10325FG-HC03
(1 OF 2)

OMIT_TABLE

FB_C1_A<2>	H11	BA0/A2	
FB_C1_A<5>	K10	BA1/A5	
FB_C1_A<4>	K11	BA2/A4	
FB_C1_A<3>	H10	BA3/A3	
FB_C1_A<7>	K4	A8/A7	
FB_C1_A<1>	H5	A9/A1	
FB_C1_A<0>	H4	A10/A0	
FB_C1_A<6>	K5	A11/A6	
FB_C1_CKE_L	J3	CKE*	
FB_C1_CLK_P	J12	CK	
FB_C1_CLK_N	J11	CK*	
FB_C1_CS_L	G12	CS*	
FB_C1_WE_L	L12	WE*	
FB_C1_CAS_L	L3	CAS*	
FB_C1_RAS_L	G3	RAS*	
FB_C1_ZQ	J13	ZQ	
FB_C1_MF	J1	MF (MF=0)	
FB_C1_SEN	J10	SEN	
FB_C1_RESET_L	J2	RESET*	
FB_C1_ABI_L	J4	ABI*	
FB_C1_EDC<0>	C2	EDC0	
FB_C1_EDC<1>	C13	EDC1	
FB_C1_EDC<2>	R13	EDC2	
FB_C1_EDC<3>	R2	EDC3	
FB_C1_WCLK_P<0>	D4	WCK01	
FB_C1_WCLK_N<0>	D5	WCK01*	
FB_C1_WCLK_P<1>	P4	WCK23	
FB_C1_WCLK_N<1>	P5	WCK23*	

DBI1*	D2		FB_C1_DBI_L<0>
DBI2*	D13		FB_C1_DBI_L<1>
DBI0*	P13		FB_C1_DBI_L<2>
DBI3*	P2		FB_C1_DBI_L<3>
DQ0	A4		FB_C1_DQ<0>
DQ1	A2		FB_C1_DQ<1>
DQ2	B4		FB_C1_DQ<2>
DQ3	B2		FB_C1_DQ<3>
DQ4	E4		FB_C1_DQ<4>
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DQ18	T11		FB_C1_DQ<18>
DQ19	T13		FB_C1_DQ<19>
DQ20	N11		FB_C1_DQ<20>
DQ21	N13		FB_C1_DQ<21>
DQ22	M11		FB_C1_DQ<22>
DQ23	M13		FB_C1_DQ<23>
DQ24	U4		FB_C1_DQ<24>
DQ25	U2		FB_C1_DQ<25>
DQ26	T4		FB_C1_DQ<26>
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DQ29	N2		FB_C1_DQ<29>
DQ30	M4		FB_C1_DQ<30>
DQ31	M2		FB_C1_DQ<31>
NC	A5		
A12/RFU/NC	J5		FB_C1_A<12>
NC	U5		

UA550 32MX32-1.5GHZ-MFL

BGA
K4G10325FG-HC03
(2 OF 2)

OMIT_TABLE

=PP1V35_S0_GPU_FBVDDQ	C5	
	C10	
	D11	
	G1	
	G4	
	G11	
	G14	
VDD	L1	
	L4	
	L11	
	L14	
	P11	
	R5	
	R10	
	B1	
	B3	
	B12	
	B14	
	D1	
	D3	
	D12	
	D14	
	E5	
	E10	
	F1	
	F3	
	F12	
	F14	
	G2	
	G13	
	H3	
	H12	
	K3	
	K12	
	L2	
	L13	
VDDQ	M1	
	M3	
	M12	
	M14	
	N5	
	N10	
	P1	
	P3	
	P12	
	P14	
	T1	
	T3	
	T12	
	T14	
FB_C1_VREFC	J14	VREFC
FB_C1_VREFD	A10	VREFD
	U10	

	B5	
	B10	
	D10	
	G5	
	G10	
	H1	
	H14	
VSS	K1	
	K14	
	L5	
	L10	
	P10	
	T5	
	T10	
	A1	
	A3	
	A12	
	A14	
	C1	
	C3	
	C4	
	C11	
	C12	
	C14	
	E1	
	E3	
	E12	
	E14	
	F5	
	F10	
	H2	
	H13	
	K2	
	K13	
	M5	
	M10	
	N1	
	N3	
	N12	
VSSQ	N14	
	R1	
	R3	
	R4	
	R11	
	R12	
	R14	
	U1	
	U3	
	U12	
	U14	

MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.1 mm

SYNC_MASTER=D8_YAN
SYNC_DATE=04/09/2012

PAGE TITLE

GDDR5 FRAME BUFFER C

Apple Inc.

DRAWING NUMBER 051-9505
SIZE D
REVISION 8.0.0
BRANCH prefsb
PAGE 105 OF 144
SHEET 88 OF 123

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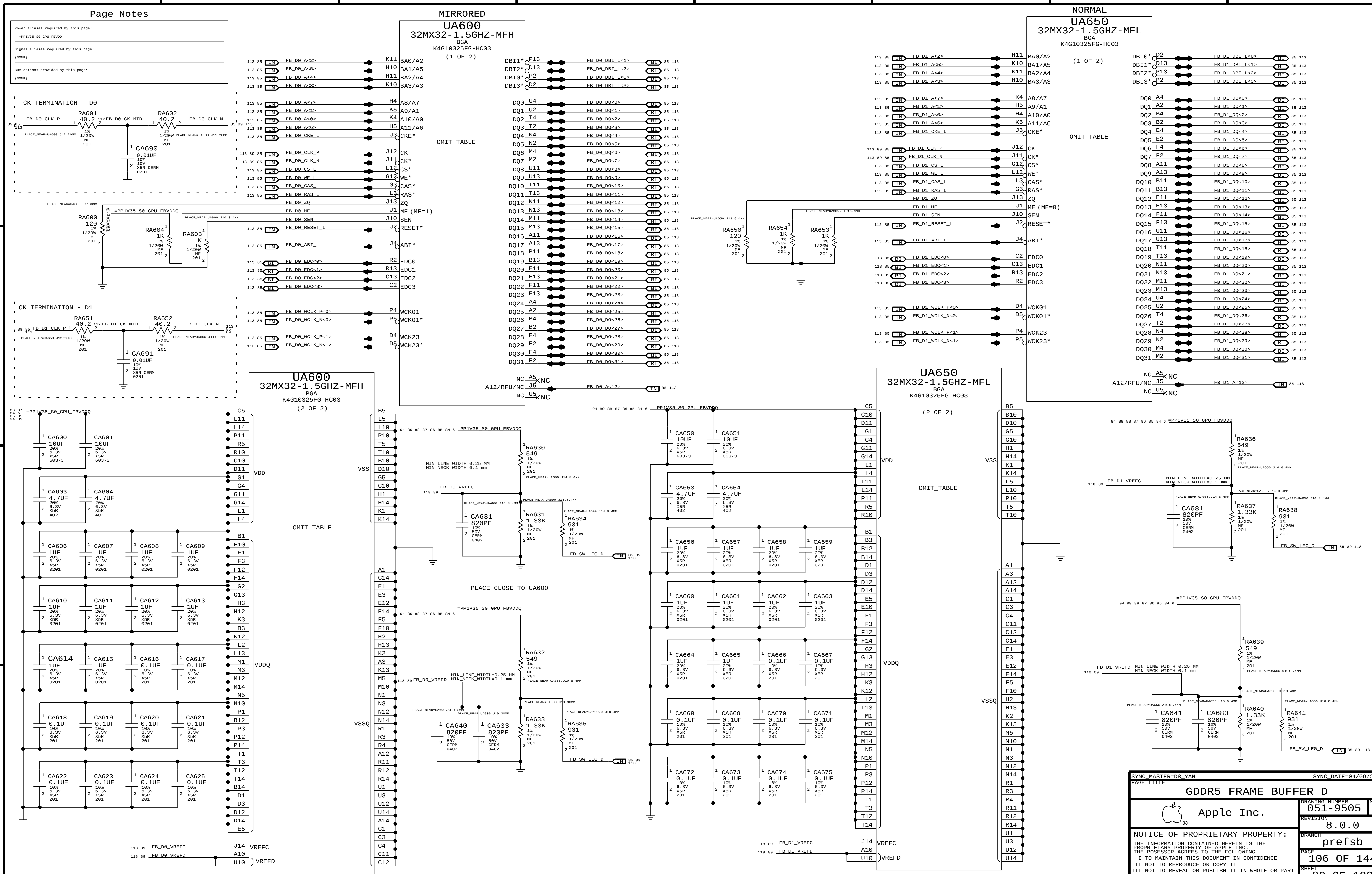

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SYNC_MASTER=D8_YAN SYNC_DATE=04/09/2012

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GDDR5 FRAME BUFFER D

Apple Inc.

DRAWING NUMBER 051-9505 SIZE D

REVISION 8.0.0

BRANCH prefsb

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DISABLE PHYS A, B & C FOR D8

OMIT_TABLE
CRITICAL

UA000
BGA
SYM 6 OF 14
GK104 GPU

NC BE18 IFPAB_RSET
118 GPU_IFPAB_PLLVDD BB15 IFPAB_PLLVDD
RA704 10K 1% 1/20W MF 201
118 GPU_IFPA_IOVDD BB17 BA17 IFPA_IOVDD
RA701 10K 1% 1/20W MF 201
118 GPU_IFPB_IOVDD BA18 BB18 IFPB_IOVDD
RA702 10K 1% 1/20W MF 201
NC BB14 IFPC_RSET
118 GPU_IFPC_PLLVDD BB12 IFPC_PLLVDD
RA719 10K 1% 1/20W MF 201
118 GPU_IFPC_IOVDD BA11 BA12 IFPC_IOVDD
RA703 10K 1% 1/20W MF 201
118 IFPD_RSET BE12 IFPD_RSET
RA706 1K 1% 1/20W MF 201
PLACE_NEAR=UA000.BE12:5MM
99 PP3V3_GPU_IFPX_PLLVDD_FLT BB11 IFPD_PLLVDD
PD FOR RSET
PLACE_NEAR=UA000.BF11:5MM
118 IFPEF_RSET BF11 IFPEF_RSET
RA707 1K 1% 1/20W MF 201
90 PP3V3_GPU_IFPX_PLLVDD_FLT BB9 IFPEF_PLLVDD

IFPA_TXC* BD18 → NC
IFPA_TXC BC18 → NC
IFPA_TXD0* BG14 → NC
IFPA_TXD0 BH14 → NC
IFPA_TXD1* BC15 → NC
IFPA_TXD1 BD15 → NC
IFPA_TXD2* BE17 → NC
IFPA_TXD2 BF17 → NC
IFPA_TXD3* BC17 → NC
IFPA_TXD3 BD17 → NC
IFPB_TXC* BG18 → NC
IFPB_TXC BH18 → NC
IFPB_TXD4* BJ14 → NC
IFPB_TXD4 BJ15 → NC
IFPB_TXD5* BH15 → NC
IFPB_TXD5 BG15 → NC
IFPB_TXD6* BG17 → NC
IFPB_TXD6 BH17 → NC
IFPB_TXD7* BJ18 → NC
IFPB_TXD7 BJ17 → NC
IFPAB GPIO14 AW5 → NC
IFPC_AUX_I2CW_SDA* BF2 → NC
IFPC_AUX_I2CW_SCL BG2 → NC
IFPC
IFPC_L3* BE11 → NC
IFPC_L3 BD11 → NC
IFPC_L2* BC12 → NC
IFPC_L2 BD12 → NC
IFPC_L1* BE14 → NC
IFPC_L1 BF14 → NC
IFPC_L0* BD14 → NC
IFPC_L0 BC14 → NC
GPIO15 AV6 → NC
IFPD_AUX_I2CX_SDA* BF4 → DP_INT_EG_AUX_N B1 75 90 111
IFPD_AUX_I2CX_SCL BG4 → DP_INT_EG_AUX_P B1 75 90 111
IFPD
IFPD_L3* BH9 → DP_INT_EG_ML_N<3> OUT 75 111
IFPD_L3 BG9 → DP_INT_EG_ML_P<3> OUT 75 111
IFPD_L2* BG11 → DP_INT_EG_ML_N<2> OUT 75 111
IFPD_L2 BH11 → DP_INT_EG_ML_P<2> OUT 75 111
IFPD_L1* BJ11 → DP_INT_EG_ML_N<1> OUT 75 111
IFPD_L1 BJ12 → DP_INT_EG_ML_P<1> OUT 75 111
IFPD_L0* BH12 → DP_INT_EG_ML_N<0> OUT 75 111
IFPD_L0 BG12 → DP_INT_EG_ML_P<0> OUT 75 111
GPIO17 AW6 → DP_INT_EG_HPD 75 117
IFPEF_AUX_I2CY_SDA* BH3 → DP_TBTSNK0_EG_AUXCH_N B1 90
IFPEF_AUX_I2CY_SCL BG3 → DP_TBTSNK0_EG_AUXCH_P B1 90
IFPEF
IFPE_L3* BE5 → DP_TBTSNK0_ML_C_N<3> OUT 36 111
IFPE_L3 BD5 → DP_TBTSNK0_ML_C_P<3> OUT 36 111
IFPE_L2* BE6 → DP_TBTSNK0_ML_C_N<2> OUT 36 111
IFPE_L2 BD6 → DP_TBTSNK0_ML_C_P<2> OUT 36 111
IFPE_L1* BG6 → DP_TBTSNK0_ML_C_N<1> OUT 36 111
IFPE_L1 BF6 → DP_TBTSNK0_ML_C_P<1> OUT 36 111
IFPE_L0* BF8 → DP_TBTSNK0_ML_C_N<0> OUT 36 111
IFPE_L0 BE8 → DP_TBTSNK0_ML_C_P<0> OUT 36 111
GPIO18 AW3 → DP_TBTSNK0_HPD 36 111
IFPF_AUX_I2CZ_SDA* BH4 → DP_TBTSNK1_EG_AUXCH_N B1 90
IFPF_AUX_I2CZ_SCL BJ4 → DP_TBTSNK1_EG_AUXCH_P B1 90
IFPF_L3* BH6 → DP_TBTSNK1_ML_C_N<3> OUT 36 111
IFPF_L3 BJ6 → DP_TBTSNK1_ML_C_P<3> OUT 36 111
IFPF_L2* BG8 → DP_TBTSNK1_ML_C_N<2> OUT 36 111
IFPF_L2 BH8 → DP_TBTSNK1_ML_C_P<2> OUT 36 111
IFPF_L1* BJ8 → DP_TBTSNK1_ML_C_N<1> OUT 36 111
IFPF_L1 BJ9 → DP_TBTSNK1_ML_C_P<1> OUT 36 111
IFPF_L0* BE9 → DP_TBTSNK1_ML_C_N<0> OUT 36 111
IFPF_L0 BF9 → DP_TBTSNK1_ML_C_P<0> OUT 36 111
GPIO16 AW2 → DP_TBTSNK1_HPD 36 111

PD FOR AUX CHANNELS (FOR NVIDIA)
111 90 75 DP_INT_EG_AUX_P
111 90 75 DP_INT_EG_AUX_N
RA714 100K 1% 1/20W MF 201
RA713 100K 1% 1/20W MF 201

90 DP_TBTSNK0_EG_AUXCH_P
90 DP_TBTSNK0_EG_AUXCH_N
RA715 100K 1% 1/20W MF 201
RA716 100K 1% 1/20W MF 201

90 DP_TBTSNK1_EG_AUXCH_P
90 DP_TBTSNK1_EG_AUXCH_N
RA717 100K 1% 1/20W MF 201
RA718 100K 1% 1/20W MF 201

IFP CD IOVDD

6 =PP3V3_S0_GPU_IFPX_PLLVDD IFPX PLLVDD
CRITICAL
LA704 330-OHM-1.2A 0603
PP3V3_GPU_IFPX_PLLVDD_FLT 90
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

PLACE BELOW GPU NEAR DISPLAY SECTION
PLACE_NEAR=UA000.BB11:20MM
PLACE_NEAR=UA000.BB9:20MM
PLACE_NEAR=UA000.BB11:3.8MM
PLACE_NEAR=UA000.BB9:3.8MM
Place near GPU
CA719 4.7UF 20% 6.3V X6S 0402
CA715 1UF 10% 6.3V X7R 0402
Place under GPU
CA718 0.1UF 10% 6.3V X6S 0201
CA712 0.1UF 10% 6.3V X6S 0201

PLACE_NEAR=UA000.BA14:20MM
6 =PP1V05_S0_GPU_IFPCD_IOVDD
LA705 FERR-220-OHM-2A 0603
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2mm
VOLTAGE=1.05V
CRITICAL
ESR = 0.05OHM
PP1V05_GPU_IFPD_IOVDD_FLT
BA14 BA15 IFPD_IOVDD
PLACE_NEAR=UA000.BA14:20MM
PLACE_NEAR=UA000.BA14:3.8MM
PLACE_NEAR=UA000.BA15:3.8MM
Place near GPU
CA725 4.7UF 20% 6.3V X6S 0402
CA756 1UF 10% 6.3V X7R 0402
Place under GPU
CA757 0.1UF 10% 6.3V X6S 0201
CA758 0.1UF 10% 6.3V X6S 0201

IFP EF IOVDD

PLACE_NEAR=UA000.BC8:20MM
LA706 FERR-220-OHM-2A 0603
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2mm
VOLTAGE=1.05V
CRITICAL
ESR = 0.05OHM
6 =PP1V05_S0_GPU_IFPEF_IOVDD
PP1V05_GPU_IFPEF_IOVDD_FLT
BC8 BD8 IFPE_IOVDD
BC9 BD9 IFPF_IOVDD
PLACE_NEAR=UA000.BC8:20MM
PLACE_NEAR=UA000.BD8:20MM
PLACE_NEAR=UA000.BD9:20MM
PLACE_NEAR=UA000.BD9:3.8MM
PLACE_NEAR=UA000.BC8:5MM
PLACE_NEAR=UA000.BD8:5MM
PLACE_NEAR=UA000.BC9:5MM
PLACE_NEAR=UA000.BD9:3.8MM
Place near GPU
CA733 4.7UF 20% 6.3V X6S 0402
CA734 4.7UF 20% 6.3V X6S 0402
CA735 1.0UF 20% 4V X6S 0201
CA736 1.0UF 20% 4V X6S 0201
Place under GPU
CA737 0.1UF 10% 6.3V X6S 0201
CA738 0.1UF 10% 6.3V X6S 0201
CA731 0.1UF 10% 6.3V X6S 0201
CA732 0.1UF 10% 6.3V X6S 0201

90 DP_TBTSNK0_EG_AUXCH_P = DP_TBTSNK0_AUXCH_C_P 36 111 MAKE_BASE=TRUE
90 DP_TBTSNK0_EG_AUXCH_N = DP_TBTSNK0_AUXCH_C_N 36 111 MAKE_BASE=TRUE
90 DP_TBTSNK1_EG_AUXCH_P = DP_TBTSNK1_AUXCH_C_P 36 111 MAKE_BASE=TRUE
90 DP_TBTSNK1_EG_AUXCH_N = DP_TBTSNK1_AUXCH_C_N 36 111 MAKE_BASE=TRUE

SYNC_MASTER=D8_YAN SYNC_DATE=04/09/2012

PAGE TITLE
KEPLER EDP/DP/GPIO

Apple Inc.

DRAWING NUMBER 051-9505 SIZE D
REVISION 8.0.0
BRANCH prefsb
PAGE 107 OF 144
SHEET 90 OF 123

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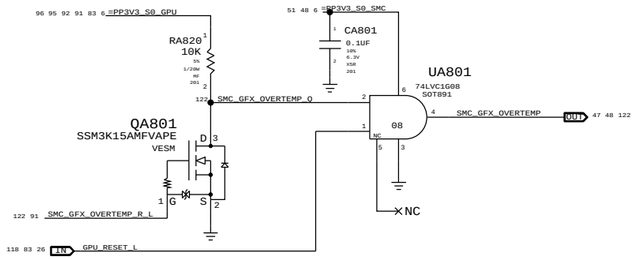
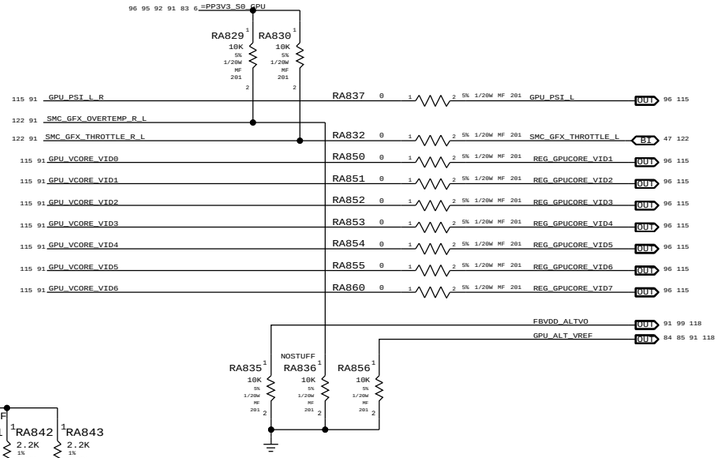
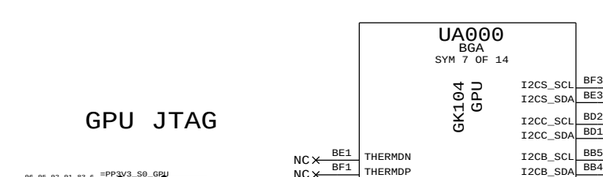
GPU overtemp masking

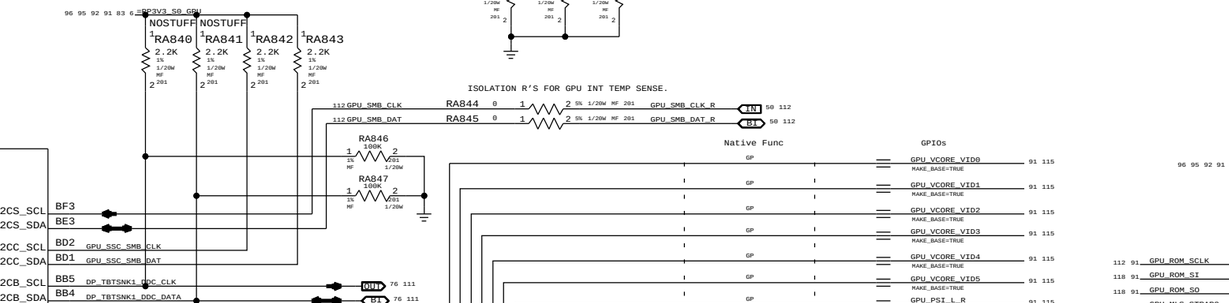


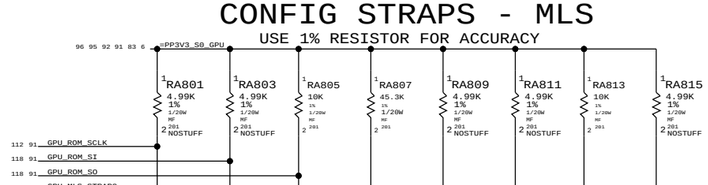


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0175	1	RES,MF,20KOHM,1,1/20W,0201	RA804		FB:1G_SAMSUNG
118S0105	1	RES,MF,15KOHM,1,1/20W,0201	RA804		FB:1G_HYNIX
118S0385	1	RES,MF,45.3KOHM,1,1/20W,0201	RA804		FB:2G_SAMSUNG
118S0315	1	RES,MF,34.8KOHM,1,1/20W,0201	RA804		FB:2G_HYNIX
118S0175	1	RES,MF,20KOHM,1,1/20W,0201	RA812		GPU:104GTX
118S0105	1	RES,MF,15KOHM,1,1/20W,0201	RA812		GPU:104GT
118S0105	1	RES,MF,15KOHM,1,1/20W,0201	RA812		GPU:104GT2

GPU JTAG







CONFIG STRAPS - MLS

USE 1% RESISTOR FOR ACCURACY

SYNC_MASTER=D8_YAN
SYNC_DATE=07/27/2012
PAGE TITLE
KEPLER GPIO/STRAPPING
Apple Inc.
DRAWING NUMBER 051-9505
SIZE D
REVISION 8.0.0
BRANCH prefsb
PAGE 108 OF 144
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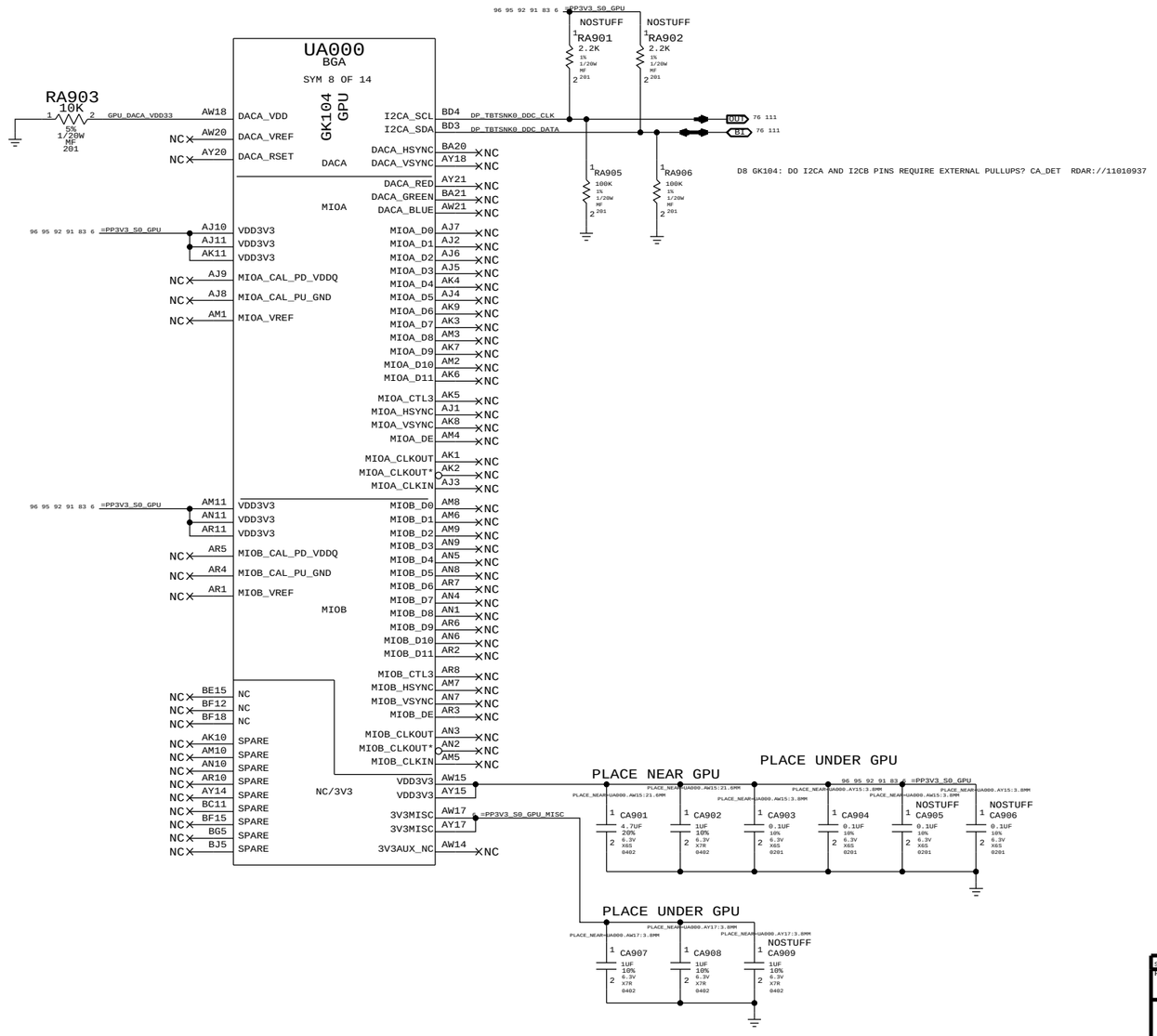

SYNC_MASTER=D8_YAN SYNC_DATE=04/09/2012

PAGE TITLE

KEPLER MISC

Apple Inc.

DRAWING NUMBER 051-9505 SIZE D

REVISION 8.0.0

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GPU NVVDD DECOUPLING I(EDP)=95A

Page Notes

Power aliases required by this page:

- =PPVCORE_S0_GPU

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

93 51 6 =PPVCORE_S0_GPU

UA000 BGA SYM 10 OF 14 VDD 1/2 GK104-GPU

BA39	VDD	VDD	BH48
BA42	VDD	VDD	BH49
BA43	VDD	VDD	BJ39
BA44	VDD	VDD	BJ41
BA45	VDD	VDD	BJ42
BA46	VDD	VDD	BJ44
BB37	VDD	VDD	BJ45
BB38	VDD	VDD	BJ46
BB39	VDD	VDD	BJ47
BB40	VDD	VDD	BJ48
BB41	VDD	VDD	P15
BB42	VDD	VDD	P17
BB43	VDD	VDD	P19
BB44	VDD	VDD	P21
BB45	VDD	VDD	P23
BB46	VDD	VDD	P25
BB47	VDD	VDD	P27
BC38	VDD	VDD	P29
BC39	VDD	VDD	P31
BC41	VDD	VDD	R14
BC42	VDD	VDD	R16
BC45	VDD	VDD	R18
BC46	VDD	VDD	R20
BD38	VDD	VDD	R22
BD39	VDD	VDD	R24
BD41	VDD	VDD	R26
BD42	VDD	VDD	R28
BD44	VDD	VDD	R30
BD45	VDD	VDD	R32
BD46	VDD	VDD	T15
BD47	VDD	VDD	T17
BD48	VDD	VDD	T19
BD49	VDD	VDD	T21
BE38	VDD	VDD	T23
BE39	VDD	VDD	T25
BE40	VDD	VDD	T27
BE41	VDD	VDD	T29
BE42	VDD	VDD	T31
BE43	VDD	VDD	U14
BE44	VDD	VDD	U16
BE45	VDD	VDD	U18
BE46	VDD	VDD	U20
BE47	VDD	VDD	U22
BE48	VDD	VDD	U24
BE49	VDD	VDD	U26
BF38	VDD	VDD	U28
BF39	VDD	VDD	U30
BF40	VDD	VDD	U32
BF41	VDD	VDD	V15
BF42	VDD	VDD	V17
BF43	VDD	VDD	V19
BF44	VDD	VDD	V21
BF45	VDD	VDD	V23
BF46	VDD	VDD	V25
BF47	VDD	VDD	V27
BF48	VDD	VDD	V29
BF49	VDD	VDD	V31
BG39	VDD	VDD	W14
BG41	VDD	VDD	W16
BG42	VDD	VDD	W18
BG44	VDD	VDD	W20
BG45	VDD	VDD	W22
BG46	VDD	VDD	W24
BG47	VDD	VDD	W26
BG48	VDD	VDD	W28
BG49	VDD	VDD	W30
BH39	VDD	VDD	W32
BH40	VDD	VDD	Y15
BH41	VDD	VDD	Y17
BH42	VDD	VDD	Y19
BH43	VDD	VDD	Y21
BH44	VDD	VDD	Y23
BH45	VDD	VDD	Y25
BH46	VDD	VDD	Y27
BH47	VDD	VDD	Y29

UA000 BGA SYM 9 OF 14 VDD 1/2 GK104-GPU

AA14	VDD	VDD	AH31
AA16	VDD	VDD	AJ14
AA18	VDD	VDD	AJ16
AA20	VDD	VDD	AJ18
AA22	VDD	VDD	AJ20
AA24	VDD	VDD	AJ22
AA26	VDD	VDD	AJ24
AA28	VDD	VDD	AJ26
AA30	VDD	VDD	AJ28
AA32	VDD	VDD	AJ30
AB15	VDD	VDD	AJ32
AB17	VDD	VDD	AK15
AB19	VDD	VDD	AK17
AB21	VDD	VDD	AK19
AB23	VDD	VDD	AK21
AB25	VDD	VDD	AK23
AB27	VDD	VDD	AK25
AB29	VDD	VDD	AK27
AB31	VDD	VDD	AK29
AC14	VDD	VDD	AK31
AC16	VDD	VDD	AL14
AC18	VDD	VDD	AL16
AC20	VDD	VDD	AL18
AC22	VDD	VDD	AL20
AC24	VDD	VDD	AL22
AC26	VDD	VDD	AL24
AC28	VDD	VDD	AL26
AC30	VDD	VDD	AL28
AC32	VDD	VDD	AL30
AD15	VDD	VDD	AL32
AD17	VDD	VDD	AM15
AD19	VDD	VDD	AM17
AD21	VDD	VDD	AM19
AD23	VDD	VDD	AM21
AD25	VDD	VDD	AM23
AD27	VDD	VDD	AM25
AD29	VDD	VDD	AM27
AD31	VDD	VDD	AM29
AE14	VDD	VDD	AM31
AE16	VDD	VDD	AM32
AE18	VDD	VDD	AN39
AE20	VDD	VDD	AP39
AE22	VDD	VDD	AR39
AE24	VDD	VDD	AR40
AE26	VDD	VDD	AR41
AE28	VDD	VDD	AT39
AE30	VDD	VDD	AT40
AE32	VDD	VDD	AT41
AF15	VDD	VDD	AU39
AF17	VDD	VDD	AU41
AF19	VDD	VDD	AU42
AF21	VDD	VDD	AV41
AF23	VDD	VDD	AV42
AF25	VDD	VDD	AV43
AF27	VDD	VDD	AV44
AF29	VDD	VDD	AW35
AF31	VDD	VDD	AW36
AG14	VDD	VDD	AW37
AG16	VDD	VDD	AW41
AG18	VDD	VDD	AW42
AG20	VDD	VDD	AW43
AG22	VDD	VDD	AW44
AG24	VDD	VDD	AW45
AG26	VDD	VDD	AY36
AG28	VDD	VDD	AY42
AG30	VDD	VDD	AY45
AG32	VDD	VDD	BA36
AH15	VDD	VDD	BA37
AH17	VDD	VDD	BA38
AH19	VDD	VDD	Y31
AH21	VDD		
AH23	VDD		
AH25	VDD		
AH27	VDD		
AH29	VDD		

VDD_SENSE AY23
GND_SENSE AW23

=PPVCORE_S0_GPU 6 51 93

NOSTUFF
RB101 100 5% 1/20W MF 201

NOSTUFF
RB102 100 5% 1/20W MF 201

MIN_LINE_WIDTH=0.41 MM
MIN_NECK_WIDTH=0.10 MM
VOLTAGE=1.0V
VSNS_GPU_VDD → 96 115
VSNS_GPU_VSS → 96 115
MIN_LINE_WIDTH=0.41MM
MIN_NECK_WIDTH=0.10 MM
VOLTAGE=0V

PLACE UNDER GPU

CB101 4.7UF 20% 6.3V X6S 0402
CB102 4.7UF 20% 6.3V X6S 0402
CB103 4.7UF 20% 6.3V X6S 0402
CB104 4.7UF 20% 6.3V X6S 0402
CB105 4.7UF 20% 6.3V X6S 0402
CB106 4.7UF 20% 6.3V X6S 0402
CB107 4.7UF 20% 6.3V X6S 0402
CB108 4.7UF 20% 6.3V X6S 0402
CB109 4.7UF 20% 6.3V X6S 0402
CB110 4.7UF 20% 6.3V X6S 0402
CB111 4.7UF 20% 6.3V X6S 0402
CB112 4.7UF 20% 6.3V X6S 0402
CB113 4.7UF 20% 6.3V X6S 0402
CB114 4.7UF 20% 6.3V X6S 0402
CB115 4.7UF 20% 6.3V X6S 0402
CB116 4.7UF 20% 6.3V X6S 0402
CB117 4.7UF 20% 6.3V X6S 0402
CB118 4.7UF 20% 6.3V X6S 0402
CB119 4.7UF 20% 6.3V X6S 0402
CB120 4.7UF 20% 6.3V X6S 0402

PLACE UNDER GPU

CB121 4.7UF 20% 6.3V X6S 0402
CB122 4.7UF 20% 6.3V X6S 0402
CB123 4.7UF 20% 6.3V X6S 0402
CB124 4.7UF 20% 6.3V X6S 0402
CB125 4.7UF 20% 6.3V X6S 0402
CB126 4.7UF 20% 6.3V X6S 0402
CB127 4.7UF 20% 6.3V X6S 0402
CB128 4.7UF 20% 6.3V X6S 0402
CB129 4.7UF 20% 6.3V X6S 0402
CB130 4.7UF 20% 6.3V X6S 0402
CB131 4.7UF 20% 6.3V X6S 0402
CB132 4.7UF 20% 6.3V X6S 0402
CB133 4.7UF 20% 6.3V X6S 0402
CB134 4.7UF 20% 6.3V X6S 0402
CB135 4.7UF 20% 6.3V X6S 0402
CB136 4.7UF 20% 6.3V X6S 0402
CB137 4.7UF 20% 6.3V X6S 0402
CB138 4.7UF 20% 6.3V X6S 0402
CB139 4.7UF 20% 6.3V X6S 0402
CB140 4.7UF 20% 6.3V X6S 0402

PLACE UNDER GPU

CB141 1.0UF 20% 4V X6S 0201
CB142 1.0UF 20% 4V X6S 0201
CB143 1.0UF 20% 4V X6S 0201
CB144 1.0UF 20% 4V X6S 0201
CB145 1.0UF 20% 4V X6S 0201
CB146 1.0UF 20% 4V X6S 0201
CB147 1.0UF 20% 4V X6S 0201
CB148 1.0UF 20% 4V X6S 0201
CB149 1.0UF 20% 4V X6S 0201
CB150 1.0UF 20% 4V X6S 0201
CB151 1.0UF 20% 4V X6S 0201
CB152 1.0UF 20% 4V X6S 0201
CB153 1.0UF 20% 4V X6S 0201
CB154 1.0UF 20% 4V X6S 0201
CB155 1.0UF 20% 4V X6S 0201
CB156 1.0UF 20% 4V X6S 0201
CB157 1.0UF 20% 4V X6S 0201
CB158 1.0UF 20% 4V X6S 0201
CB159 1.0UF 20% 4V X6S 0201
CB160 1.0UF 20% 4V X6S 0201

PLACE UNDER GPU

CB161 10UF 20% 4V X6S 0402
CB162 10UF 20% 4V X6S 0402
CB163 10UF 20% 4V X6S 0402
CB164 10UF 20% 4V X6S 0402
CB171 22UF 20% 4V X6S-CERM 0603
CB172 22UF 20% 4V X6S-CERM 0603
CB173 22UF 20% 4V X6S-CERM 0603
CB174 22UF 20% 4V X6S-CERM 0603
CB175 22UF 20% 4V X6S-CERM 0603
CB176 22UF 20% 4V X6S-CERM 0603
CB177 22UF 20% 4V X6S-CERM 0603
CB178 22UF 20% 4V X6S-CERM 0603
CB179 22UF 20% 4V X6S-CERM 0603
CB180 22UF 20% 4V X6S-CERM 0603
CB181 22UF 20% 4V X6S-CERM 0603
CB191 47UF 20% 4V X6S 0805
CB192 47UF 20% 4V X6S 0805
CB193 47UF 20% 4V X6S 0805
CB194 47UF 20% 4V X6S 0805

PLACE NEAR GPU W/ 35MM FROM GPU CENTER

PLACE_NEAR=UA000.AT40:35MM
CRITICAL
CB165 330UF-0.006OHM 20% 2V POLY CASE-D2-SM

PLACE_NEAR=UA000.AT40:35MM
CRITICAL
CB166 330UF-0.006OHM 20% 2V POLY CASE-D2-SM

PLACE_NEAR=UA000.AT40:42MM
CRITICAL
CB167 330UF-0.006OHM 20% 2V POLY CASE-D2-SM

PLACE_NEAR=UA000.AT40:38MM
CRITICAL
CB168 330UF-0.006OHM 20% 2V POLY CASE-D2-SM

SYNC_MASTER=D8_YAN SYNC_DATE=04/09/2012

PAGE TITLE: KEPLER CORE POWER

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GPU FBVDD/Q DECOUPLING I(EDP PEAK)=26A

Page Notes

Power aliases required by this page:

- +PP1V35_GPU_FBVDDQ

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

PLACE UNDER GPU

CB201 0.1UF 10% 6.3V X6S 0201
CB202 0.1UF 10% 6.3V X6S 0201
CB203 0.1UF 10% 6.3V X6S 0201
CB204 0.1UF 10% 6.3V X6S 0201
CB205 0.1UF 10% 6.3V X6S 0201
CB206 0.1UF 10% 6.3V X6S 0201
CB207 0.1UF 10% 6.3V X6S 0201
CB208 0.1UF 10% 6.3V X6S 0201

PLACE UNDER GPU

CB211 1UF 10% 6.3V X7R 0402
CB212 1UF 10% 6.3V X7R 0402
CB213 1UF 10% 6.3V X7R 0402
CB214 1UF 10% 6.3V X7R 0402
CB215 1UF 10% 6.3V X7R 0402
CB216 1UF 10% 6.3V X7R 0402
CB217 1UF 10% 6.3V X7R 0402
CB218 1UF 10% 6.3V X7R 0402

PLACE UNDER GPU

CB221 4.7UF 20% 6.3V X6S 0402
CB222 4.7UF 20% 6.3V X6S 0402
CB223 4.7UF 20% 6.3V X6S 0402
CB224 4.7UF 20% 6.3V X6S 0402
CB225 4.7UF 20% 6.3V X6S 0402
CB226 4.7UF 20% 6.3V X6S 0402
CB227 4.7UF 20% 6.3V X6S 0402
CB228 4.7UF 20% 6.3V X6S 0402
NOSTUFF CB229 4.7UF 20% 6.3V X6S 0402
NOSTUFF CB230 4.7UF 20% 6.3V X6S 0402
NOSTUFF CB231 4.7UF 20% 6.3V X6S 0402
NOSTUFF CB232 4.7UF 20% 6.3V X6S 0402
NOSTUFF CB233 4.7UF 20% 6.3V X6S 0402
NOSTUFF CB234 4.7UF 20% 6.3V X6S 0402
NOSTUFF CB235 4.7UF 20% 6.3V X6S 0402
NOSTUFF CB236 4.7UF 20% 6.3V X6S 0402

PLACE UNDER GPU

CB240 22UF 20% 4V X6S-CERM 0603
CB241 22UF 20% 4V X6S-CERM 0603
CB242 22UF 20% 4V X6S-CERM 0603
CB243 22UF 20% 4V X6S-CERM 0603
NOSTUFF CB244 22UF 20% 4V X6S-CERM 0603
NOSTUFF CB245 22UF 20% 4V X6S-CERM 0603
CB246 10UF 20% 4V X6S 0402
CB247 10UF 20% 4V X6S 0402
CB248 10UF 20% 4V X6S 0402
CB249 10UF 20% 4V X6S 0402
NOSTUFF CB250 10UF 20% 4V X6S 0402
NOSTUFF CB251 10UF 20% 4V X6S 0402

94 89 88 87 86 85 84 6 +PP1V35_S0_GPU_FBVDDQ

UA000 BGA SYM 11 OF 14 FBVDDQ GK104 GPU

AA39	FBVDDQ	FBVDDQ	J43
AC11	FBVDDQ	FBVDDQ	K24
AD10	FBVDDQ	FBVDDQ	K26
AD39	FBVDDQ	FBVDDQ	K29
AF11	FBVDDQ	FBVDDQ	K30
AF39	FBVDDQ	FBVDDQ	K32
AG39	FBVDDQ	FBVDDQ	L14
AK39	FBVDDQ	FBVDDQ	L15
AM39	FBVDDQ	FBVDDQ	L17
AM40	FBVDDQ	FBVDDQ	L18
AN40	FBVDDQ	FBVDDQ	L20
B47	FBVDDQ	FBVDDQ	L23
C45	FBVDDQ	FBVDDQ	L24
C46	FBVDDQ	FBVDDQ	L27
C47	FBVDDQ	FBVDDQ	L29
D44	FBVDDQ	FBVDDQ	L30
D45	FBVDDQ	FBVDDQ	L32
D46	FBVDDQ	FBVDDQ	L33
E44	FBVDDQ	FBVDDQ	L35
E45	FBVDDQ	FBVDDQ	L41
F42	FBVDDQ	FBVDDQ	P11
F44	FBVDDQ	FBVDDQ	P39
F45	FBVDDQ	FBVDDQ	R11
G41	FBVDDQ	FBVDDQ	R40
G42	FBVDDQ	FBVDDQ	U11
H41	FBVDDQ	FBVDDQ	U39
H42	FBVDDQ	FBVDDQ	V11
H43	FBVDDQ	FBVDDQ	V39
J38	FBVDDQ	FBVDDQ	V40
J39	FBVDDQ	FBVDDQ	Y11
J42	FBVDDQ	FBVDDQ	Y40

FBVDDQ_SENSE R49 115 FBVDDQ_SENSE_R
FB_CLAMP BB48 FB_CLAMP
FB_VREF R39 118 FB_VREF_GPU
PROBE_FBVDDQ AG11 FB_PROBE_VDDQ
PROBE_FB_GND AF10 FB_PROBE_GND
FB_CAL_PD_VDDQ P40 112 FB_CAL_PD_VDDQ
FB_CAL_PU_GND R48 112 FB_CAL_PU_GND
FB_CALTERM_GND R47 112 FB_CAL_TERM_GND

PLACE_NEAR=UA000.P40:3.8MM
PLACE_NEAR=UA000.R49:3.8MM
PLACE_NEAR=UA000.R39:6MM
PLACE_NEAR=UA000.R48:5MM
PLACE_NEAR=UA000.R47:5.5MM
PLACE_NEAR=UA000.R39:7MM
PLACE_NEAR=UA000.R39:8MM

RB202 40.2 1% 1/20W MF 201
NOSTUFF RB201 60.4 1% 1/20W MF 201
NOSTUFF RB208 1.33K 1% 1/20W MF 201
RB203 0 5% 1/20W MF 201
RB204 60.4 1% 1/20W MF 201
RB205 40.2 1% 1/20W MF 201
NOSTUFF RB206 60.4 1% 1/20W MF 201
RB207 10K 5% 1/20W MF 201
NOSTUFF RB209 1.33K 1% 1/20W MF 201
NOSTUFF CB252 0.1UF 10% 16V X7R-CERM 402

XWB201 SM SIGNAL_MODEL=EMPTY VSNS_FBVDDQ_P OUT1 99 115
XWB200 SM SIGNAL_MODEL=EMPTY VSNS_FBVDDQ_N OUT1 99 115

SYNC_MASTER=D8_YAN SYNC_DATE=04/09/2013

PAGE TITLE: KEPLER FBVDD/Q POWER

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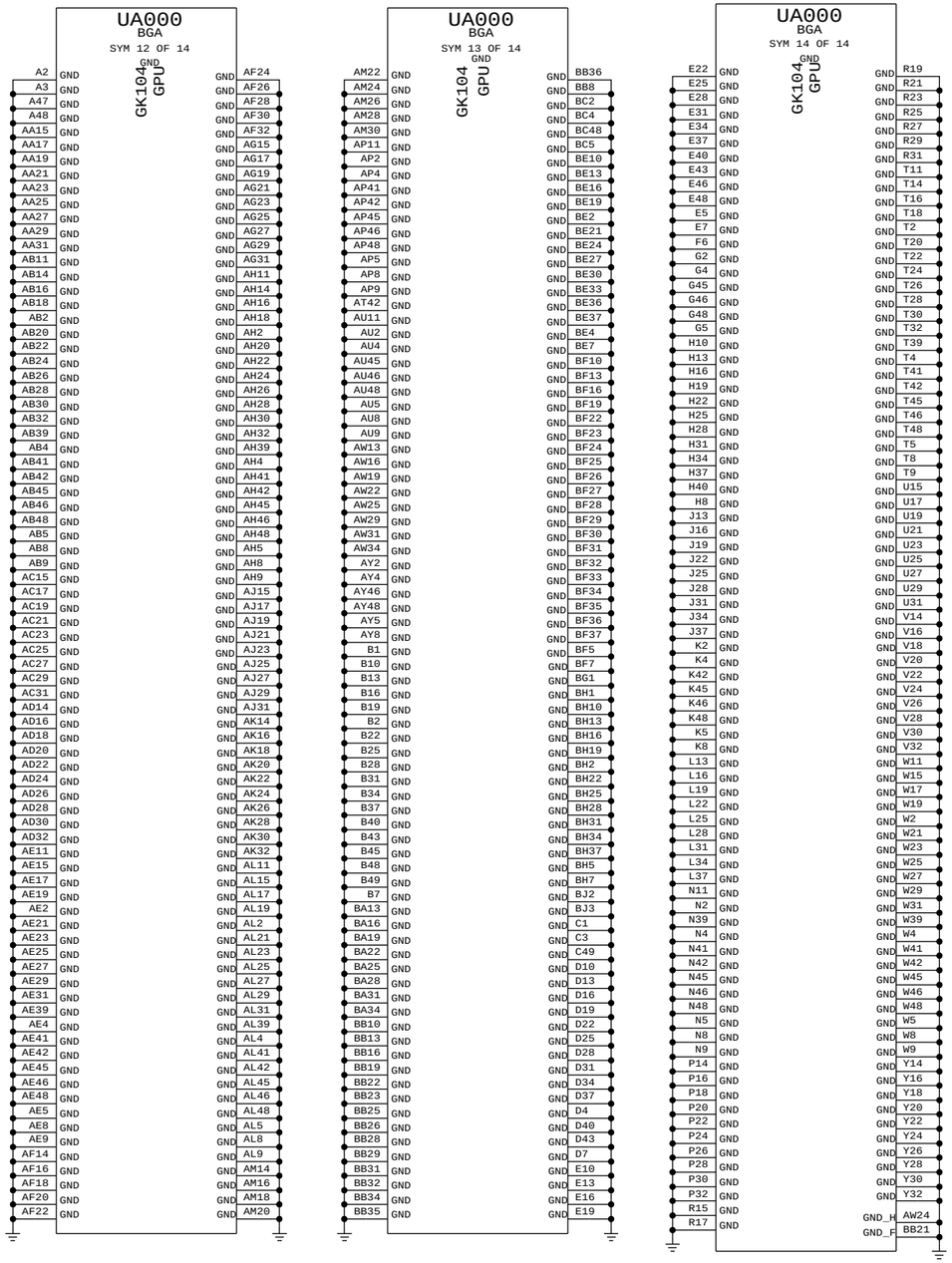


Page Notes

Power aliases required by this page:

- +PP3V3_GPU_VDD33
- +PP1V05_GPU_PEX_IOVDD
- +PP1V05_GPU_PEX_PLLVDD

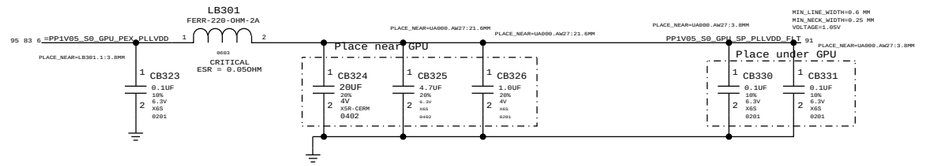
Signal aliases required by this page:

(NONE)

BOM options provided by this page:

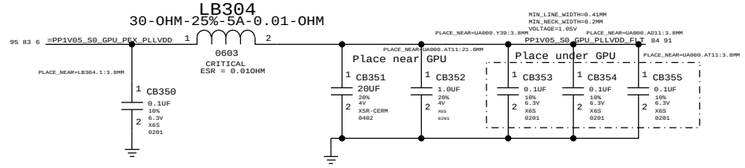
(NONE)

GPU SP_PLLVDD/VID_PLLVDD 47MA+41MA

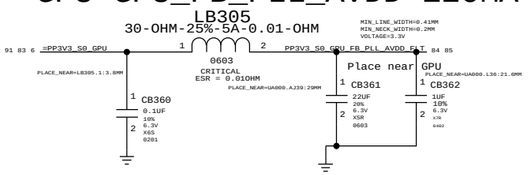


RDAR://11427653 D8: REPLACE 138S0682 WITH 138S0802

GPU GPC_PLLAVDD/LXS_PLLVDD/FB_DLL_AVDD 52MA+39MA+50MA



GPU GPU_FB_PLL_AVDD 120MA X 4 = 480MA



SYNC_MASTER=D8_YAN SYNC_DATE=04/09/2012

PAGE TITLE: KEPLER PEX PWR/GNDS

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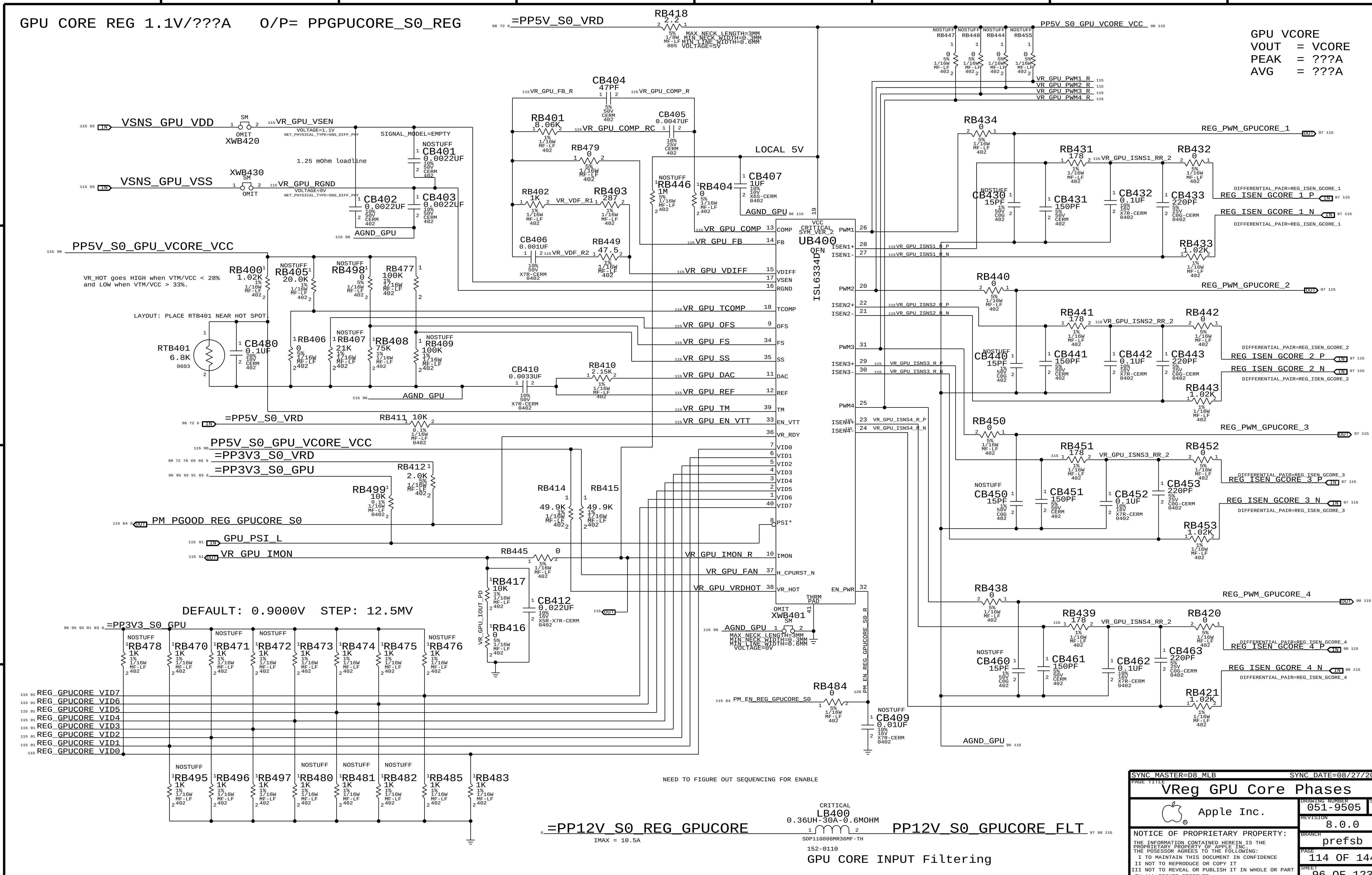

SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012

PAGE TITLE: VReg GPU Core Phases

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GPU Phase 1

115 98 97 96 PP12V_S0_GPUCORE_FLT

RB528 0 5% 1/10W MF-LF 603

NOSTUFF RB527 10 5% 1/10W MF-LF 603

115 REG_UVCC_UB510

115 REG_LVCC_UB510

CB525 1.0UF 10% 16V X7R 0603

CB526 1.0UF 10% 16V X7R 0603

CB527 1.0UF 10% 16V X7R 0603

115 REG_BOOT_GPUCORE_1_RC

RB516 0 5% 1/10W MF-LF 603

CB516 0.22UF 10% 25V X7R 0603

UB510 ISL6622 DFN

VCC UVCC LVCC

GDSEL NC

BOOT 115 REG_BOOT_GPUCORE_1

UGATE 115 REG_UGATE_GPUCORE_1

PHASE 115 REG_PHASE_GPUCORE_1

LGATE 115 REG_LGATE_GPUCORE_1

115 96 IN REG_PWM_GPUCORE_1

PWM

GND THRML PAD

CRITICAL

115 98 97 96 PP12V_S0_GPUCORE_FLT

CRITICAL QB510 IRF6811STRPBF SQ

NC NC

CRITICAL QB511 IRF6893MTRPBF DIRECTFET-MX

NC NC

CRITICAL LB510 0.24UH-30A-0.35MOHM SDP110808M-TH

115 PPGPUCORE_S0_SENSE_1

CRITICAL RB510 0.0005 1% 1W MF 0612

PPGPUCORE_S0_REG OUT 6 97 98

REG_ISEN_GCORE_1_P OUT 96 115

REG_ISEN_GCORE_1_N OUT 96 115

NOSTUFF CB517 0.001UF 10% 50V X7R-CERM 0402

REG_SNUBBER_GPUCORE_1 115

NOSTUFF RB517 2.2 5% 1/8W MF-LF 805

CRITICAL CB510 180UF 20% 16V POLY TH1

CRITICAL CB511 180UF 20% 16V POLY TH1

CRITICAL CB512 10UF 10% 25V X6S 0805

CRITICAL CB513 10UF 10% 25V X6S 0805

EMC CB514 1UF 10% 25V X6S-CERM 0402

EMC CB515 1UF 10% 25V X6S-CERM 0402

GPU Phase 2

115 98 97 96 PP12V_S0_GPUCORE_FLT

RB547 10 5% 1/10W MF-LF 603

115 REG_LVCC_UB530

CB545 1.0UF 10% 16V X7R 0603

CB547 1.0UF 10% 16V X7R 0603

115 REG_BOOT_GPUCORE_2_RC

RB536 0 5% 1/10W MF-LF 603

CB536 0.22UF 10% 25V X7R 0603

UB530 ISL6612 QFN1

VCC PVCC

PWM 115 96 IN REG_PWM_GPUCORE_2

BOOT 115 REG_BOOT_GPUCORE_2

UGATE 115 REG_UGATE_GPUCORE_2

PHASE 115 REG_PHASE_GPUCORE_2

LGATE 115 REG_LGATE_GPUCORE_2

NC NC

NC NC

GND THRML PAD

CRITICAL

CRITICAL QB512 IRF6811STRPBF SQ

NC NC

CRITICAL QB531 IRF6893MTRPBF DIRECTFET-MX

NC NC

CRITICAL LB530 0.24UH-30A-0.35MOHM SDP110808M-TH

115 PPGPUCORE_S0_SENSE_2

CRITICAL RB530 0.0005 1% 1W MF 0612

PPGPUCORE_S0_REG OUT 6 97 98

REG_ISEN_GCORE_2_P OUT 96 115

REG_ISEN_GCORE_2_N OUT 96 115

NOSTUFF CB537 0.001UF 10% 50V X7R-CERM 0402

REG_SNUBBER_GPUCORE_2 115

NOSTUFF RB537 2.2 5% 1/8W MF-LF 805

CRITICAL CB530 180UF 20% 16V POLY TH1

CRITICAL CB531 180UF 20% 16V POLY TH1

CRITICAL CB532 10UF 10% 25V X6S 0805

CRITICAL CB533 10UF 10% 25V X6S 0805

EMC CB534 1UF 10% 25V X6S-CERM 0402

EMC CB535 1UF 10% 25V X6S-CERM 0402

GPU Phase 3

115 98 97 96 PP12V_S0_GPUCORE_FLT

RB529 0 5% 1/10W MF-LF 603

RB531 0 5% 1/10W MF-LF 603

NOSTUFF RB567 10 5% 1/10W MF-LF 603

115 REG_UVCC_UB550

115 REG_VCC_UB550

115 REG_LVCC_UB550

CB565 1.0UF 10% 16V X7R 0603

CB566 1.0UF 10% 16V X7R 0603

CB567 1.0UF 10% 16V X7R 0603

115 REG_BOOT_GPUCORE_3_RC

RB556 0 5% 1/10W MF-LF 603

CB556 0.22UF 10% 25V X7R 0603

UB550 ISL6622 DFN

VCC UVCC LVCC

GDSEL NC

BOOT 115 REG_BOOT_GPUCORE_3

UGATE 115 REG_UGATE_GPUCORE_3

PHASE 115 REG_PHASE_GPUCORE_3

LGATE 115 REG_LGATE_GPUCORE_3

115 96 IN REG_PWM_GPUCORE_3

PWM

GND THRML PAD

CRITICAL

CRITICAL QB514 IRF6811STRPBF SQ

NC NC

CRITICAL QB551 IRF6893MTRPBF DIRECTFET-MX

NC NC

CRITICAL LB550 0.24UH-30A-0.35MOHM SDP110808M-TH

115 PPGPUCORE_S0_SENSE_3

CRITICAL RB550 0.0005 1% 1W MF 0612

PPGPUCORE_S0_REG OUT 6 97 98

REG_ISEN_GCORE_3_P OUT 96 115

REG_ISEN_GCORE_3_N OUT 96 115

NOSTUFF CB557 0.001UF 10% 50V X7R-CERM 0402

REG_SNUBBER_GPUCORE_3 115

NOSTUFF RB557 2.2 5% 1/8W MF-LF 805

CRITICAL CB595 180UF 20% 16V POLY TH1

CRITICAL CB552 10UF 10% 25V X6S 0805

CRITICAL CB553 10UF 10% 25V X6S 0805

EMC CB554 1UF 10% 25V X6S-CERM 0402

EMC CB555 1UF 10% 25V X6S-CERM 0402

GPU Output Decoupling

98 97 6 PPGPUCORE_S0_REG

CRITICAL CB580 330UF-0.006OHM 20% 2V POLY CASE-D2-SM

CRITICAL CB581 330UF-0.006OHM 20% 2V POLY CASE-D2-SM

CRITICAL CB582 330UF-0.006OHM 20% 2V POLY CASE-D2-SM

CRITICAL CB583 330UF-0.006OHM 20% 2V POLY CASE-D2-SM

CRITICAL CB584 330UF-0.006OHM 20% 2V POLY CASE-D2-SM

CRITICAL CB585 330UF-0.006OHM 20% 2V POLY CASE-D2-SM

SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012

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VReg GPU Core Phases

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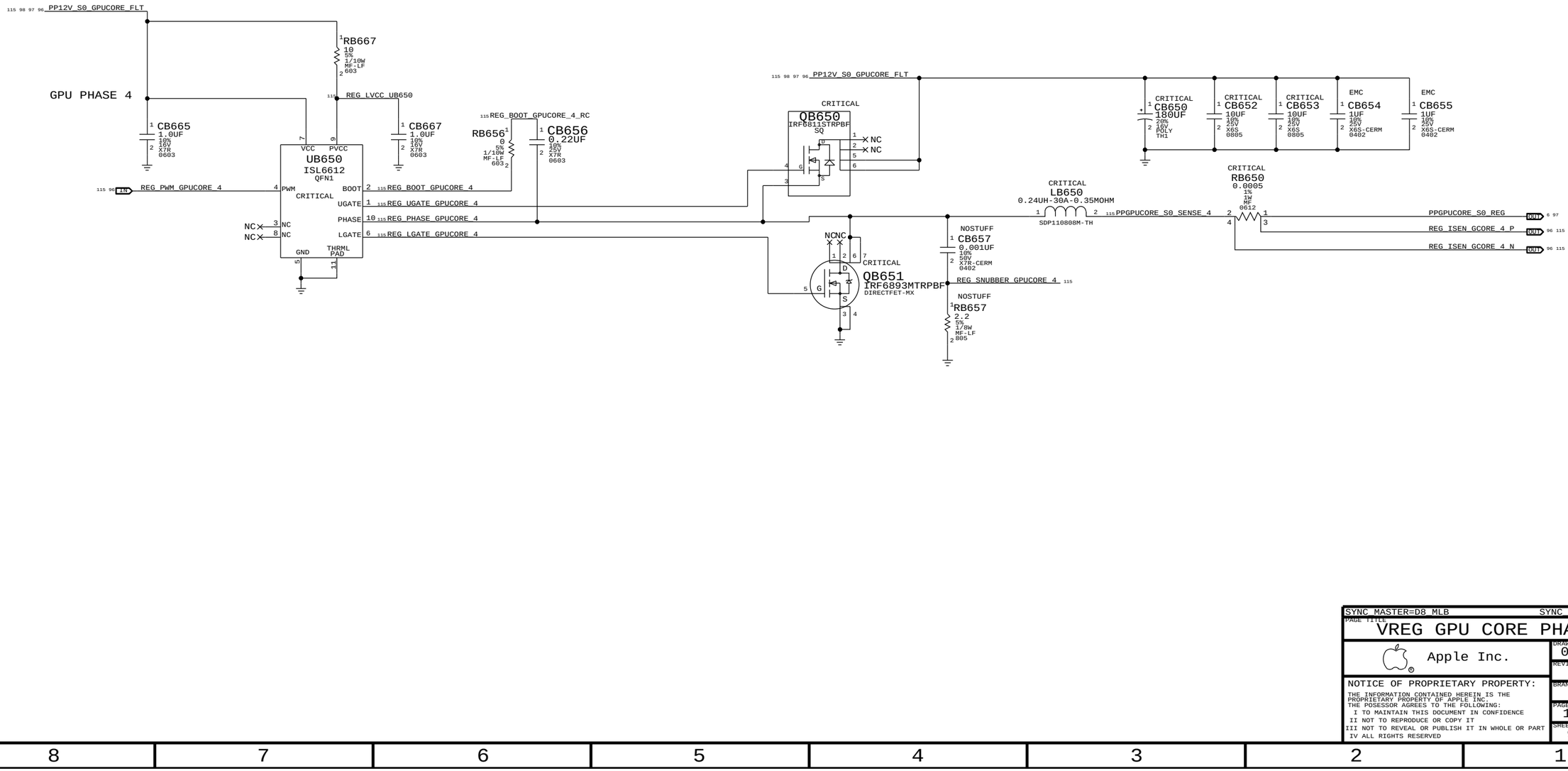

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GPU VDDQ SUPPLY

VOUT = 1.5V / 1.35V

??? A MAX OUTPUT

F = ??? KHZ

GPIO_16	VID 1	VID 0	GPU VDDQ
	0	0	1.5 V
	1	0	1.35 V

Vout = 0.5 * (1 + Ra / Rb)

Note:
Regulator requires a minimum load to prevent noise in the audio frequencies

GPU/PCH/TBT 1V05 SUPPLY

VOUT = 1.05V

5.3A MAX OUTPUT

F = 500 KHZ

Vout = 0.5V * (1 + Ra / Rb)

SYNC_MASTER=D8_MLB	SYNC_DATE=08/27/2012
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D8 BOARD SPECIFIC PHYSICAL AND SPACING CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL OF MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA,BGA_TBT	MM	16.2

General Physical Rule Definitions

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	0.1 MM	=50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
34_OHM_SE	*	Y	0.185 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
34_OHM_SE	ISL5,ISL8	Y	0.205 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
34_OHM_SE	TOP,BOTTOM	Y	0.220 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
39_OHM_SE	*	Y	0.150 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
39_OHM_SE	ISL5,ISL8	Y	0.165 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
39_OHM_SE	TOP,BOTTOM	Y	0.175 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
42_OHM_SE	*	Y	0.130 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
42_OHM_SE	ISL5,ISL8	Y	0.145 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
42_OHM_SE	TOP,BOTTOM	Y	0.155 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	*	Y	0.115 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
45_OHM_SE	ISL5,ISL8	Y	0.126 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
45_OHM_SE	TOP,BOTTOM	Y	0.135 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	*	Y	0.090 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
50_OHM_SE	ISL5,ISL8	Y	0.100 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
50_OHM_SE	TOP,BOTTOM	Y	0.105 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	*	Y	0.075 MM	0.075 MM	=STANDARD	=STANDARD	=STANDARD
55_OHM_SE	ISL5,ISL8	Y	0.080 MM	0.080 MM	=STANDARD	=STANDARD	=STANDARD
55_OHM_SE	TOP,BOTTOM	Y	0.085 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
68_OHM_DIFF	*	Y	0.171 MM	0.085 MM	=STANDARD	0.130 MM	0.1 MM
68_OHM_DIFF	TOP,BOTTOM	Y	0.185 MM	0.085 MM	=STANDARD	0.150 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	Y	0.136 MM	0.085 MM	=STANDARD	0.190 MM	0.1 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.141 MM	0.085 MM	=STANDARD	0.185 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	Y	0.121 MM	0.085 MM	=STANDARD	0.190 MM	0.1 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.085 MM	=STANDARD	0.190 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	Y	0.109 MM	0.085 MM	=STANDARD	0.200 MM	0.1 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.111 MM	0.085 MM	=STANDARD	0.200 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	Y	0.086 MM	0.085 MM	=STANDARD	0.200 MM	0.1 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.090 MM	0.085 MM	=STANDARD	0.230 MM	0.1 MM

Compensation Physical Rule Definition

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
COMP_SE	*	Y	0.305 MM	0.105 MM	3 MM	=STANDARD	=STANDARD

NOTE: line width based on 12 mil recommendation
NOTE: neck width based on 4 mil recommendation

General Spacing Definitions

Default

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?

Fixed and Dielectric

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.1 MM	?
1X_DIELECTRIC	TOP,BOTTOM	0.071 MM	?
1X_DIELECTRIC	ISL3,ISL10	0.101 MM	?
1X_DIELECTRIC	*	0.076 MM	?

BGA

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BGA_P1MM	*	=STANDARD	?

Power and Common

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_ISO	*	=STANDARD	8000
GND_P2MM	*	=2:1_SPACING	1000
PWR_P2MM	*	=2:1_SPACING	1100

GENERIC

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GENERIC_ISO	*	=1:1_SPACING	?
PM_ISO	*	=1:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PM	*	*	PM_ISO
PM	GND	*	DEFAULT

BGA Area Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM

Board Stack-up

FINISHED BOARD THICKNESS: 1.94 MM

Top	Signal	0.5 oz (Cu plated)	
	Prepreg	0.071 MM	
2	Plane	1 oz	
	Core	0.101 MM	
3	Signal	0.5 oz	
	Prepreg	0.115 MM	
4	Plane	1 oz	
	Core	0.076 MM	
5	Signal	0.5 oz	
	Prepreg	0.380 MM	
6	Plane	1 oz	
	Core	0.076 MM	
7	Plane	1 oz	
	Prepreg	0.380 MM	
8	Signal	0.5 oz	
	Core	0.076 MM	
9	Plane	1 oz	
	Prepreg	0.115 MM	
10	Signal	0.5 oz	
	Core	0.101 MM	
11	Plane	1 oz	
	Prepreg	0.071 MM	
Btm	Signal	0.5 oz (Cu plated)	

SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012

PAGE TITLE: D8 RULE DEFINITIONS

Apple Inc.

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DDR3

DDR3-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DDR_34S	*	=34_OHM_SE	=34_OHM_SE	=34_OHM_SE	=34_OHM_SE	=STANDARD	=STANDARD
DDR_34S	BOTTOM	=34_OHM_SE	=34_OHM_SE	=34_OHM_SE	2.0 MM	=STANDARD	=STANDARD
DDR_39S	*	=39_OHM_SE	=39_OHM_SE	=39_OHM_SE	=39_OHM_SE	=STANDARD	=STANDARD
DDR_42S	*	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=STANDARD	=STANDARD
DDR_42S	BOTTOM	=42_OHM_SE	=55_OHM_SE	=55_OHM_SE	2.0 MM	=STANDARD	=STANDARD
DDR_42S	ISL5,ISL8	=42_OHM_SE	=55_OHM_SE	=55_OHM_SE	2.0 MM	=STANDARD	=STANDARD
DDR_42S_D	*	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	0.1016 MM	0.1016 MM
DDR_42S_D	BOTTOM	=42_OHM_SE	=55_OHM_SE	=55_OHM_SE	2.0 MM	0.1016 MM	0.1016 MM
DDR_42S_D	ISL5,ISL8	=42_OHM_SE	=55_OHM_SE	=55_OHM_SE	2.0 MM	0.1016 MM	0.1016 MM
DDR_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
DDR_68D	*	=68_OHM_DIFF	=68_OHM_DIFF	=68_OHM_DIFF	=68_OHM_DIFF	=68_OHM_DIFF	=68_OHM_DIFF

Minimum diff spacing is 4 mil
Table 3-5, Intel Doc# 473718

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
POWER_DDR_P4MM	*	Y	0.400 MM	0.100 MM	3.0 MM	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
POWER_DDR_PHY	*	POWER_DDR_P4MM
DDR_CLK_PHY	*	DDR_68D
DDR_CTRL_PHY	*	DDR_39S
DDR_CMD_PHY	*	DDR_34S
DDR_DQ_PHY	*	DDR_42S
DDR_DQS_PHY	*	DDR_42S_D

DDR3-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DDR_CLK_ISO	TOP,BOTTOM	=5.5X_DIELECTRIC	?
DDR_CLK_ISO	ISL3,ISL10	=4.9X_DIELECTRIC	?
DDR_CLK_ISO	*	=6.5X_DIELECTRIC	?
DDR_CTRL_ISO	TOP,BOTTOM	=4.5X_DIELECTRIC	?
DDR_CTRL_ISO	ISL3,ISL10	=4.0X_DIELECTRIC	?
DDR_CTRL_ISO	*	=5.3X_DIELECTRIC	?
DDR_CTRL2CTRL	TOP,BOTTOM	=3.0X_DIELECTRIC	?
DDR_CTRL2CTRL	ISL3,ISL10	=2.6X_DIELECTRIC	?
DDR_CTRL2CTRL	*	=3.5X_DIELECTRIC	?
DDR_CMD_ISO	TOP,BOTTOM	=4.5X_DIELECTRIC	?
DDR_CMD_ISO	ISL3,ISL10	=4.0X_DIELECTRIC	?
DDR_CMD_ISO	*	=5.3X_DIELECTRIC	?
DDR_CMD2CMD	TOP,BOTTOM	=2.3X_DIELECTRIC	?
DDR_CMD2CMD	ISL3,ISL10	=2.0X_DIELECTRIC	?
DDR_CMD2CMD	*	=2.7X_DIELECTRIC	?
DDR_DATA_ISO	TOP,BOTTOM	=4.5X_DIELECTRIC	?
DDR_DATA_ISO	ISL3,ISL10	=4.0X_DIELECTRIC	?
DDR_DATA_ISO	*	=5.3X_DIELECTRIC	?
DDR_DQ2DQ	TOP,BOTTOM	=3.2X_DIELECTRIC	900
DDR_DQ2DQ	ISL3,ISL10	=2.8X_DIELECTRIC	900
DDR_DQ2DQ	*	=3.8X_DIELECTRIC	900
DDR_DQ2DQS	TOP,BOTTOM	=3.7X_DIELECTRIC	?
DDR_DQ2DQS	ISL3,ISL10	=3.3X_DIELECTRIC	?
DDR_DQ2DQS	*	=4.4X_DIELECTRIC	?
DDR_BL2BL	TOP,BOTTOM	=4.5X_DIELECTRIC	?
DDR_BL2BL	ISL3,ISL10	=4.0X_DIELECTRIC	?
DDR_BL2BL	*	=5.3X_DIELECTRIC	?
DDR_CH2CH	TOP,BOTTOM	=9.1X_DIELECTRIC	?
DDR_CH2CH	ISL3,ISL10	=8.2X_DIELECTRIC	?
DDR_CH2CH	*	=10.9X_DIELECTRIC	?
CMD2DATA_ISO	TOP,BOTTOM	=7X_DIELECTRIC	?
CMD2DATA_ISO	ISL3,ISL10	=5X_DIELECTRIC	?
CMD2DATA_ISO	*	=5X_DIELECTRIC	?

DDR3 Power-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
POWER_DDR_ISO	*	=4.3X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
POWER_DDR	*	*	POWER_DDR_ISO

Constraints

Clocks: CK[3:0], CK#[3:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DDR_CLK	*	*	DDR_CLK_ISO

Control: CS#[3:0], CKE[3:0], ODT[3:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DDR_CTRL	*	*	DDR_CTRL_ISO
DDR_CTRL	DDR_CTRL	*	DDR_CTRL2CTRL

Command: MA[15:0], RAS#, CAS#, WE# BS[2:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DDR_CMD	*	*	DDR_CMD_ISO
DDR_CMD	DDR_CMD	*	DDR_CMD2CMD
DDR_CMD	DDR_A_DQ_BYTE*	*	CMD2DATA_ISO
DDR_CMD	DDR_A_DQS*	*	CMD2DATA_ISO
DDR_CMD	DDR_B_DQ_BYTE*	*	CMD2DATA_ISO
DDR_CMD	DDR_B_DQS*	*	CMD2DATA_ISO

Data: DQS[7:0], DQS#[7:0], DQ[63:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET	
DDR_A_DQ_BYTE*	*	*	DDR_DATA_ISO	
DDR_A_DQS*	*	*	DDR_DATA_ISO	
DDR_B_DQ_BYTE*	*	*	DDR_DATA_ISO	
DDR_B_DQS*	*	*	DDR_DATA_ISO	
DDR_*_DQ_BYTE*	=SAME	*	DDR_DQ2DQ	See Note (3)
DDR_A_DQ_BYTE*	DDR_A_DQS*	*	DDR_DQ2DQS	See Note (1)
DDR_A_DQ_BYTE*	DDR_A_DQ_BYTE*	*	DDR_BL2BL	See Note (3)
DDR_B_DQ_BYTE*	DDR_B_DQS*	*	DDR_DQ2DQS	See Note (1)
DDR_B_DQ_BYTE*	DDR_B_DQ_BYTE*	*	DDR_BL2BL	
DDR_A_*	DDR_B_*	*	DDR_CH2CH	See Note (2)

Note (1):
Deliberately set DQ to DQS spacing to 3:1 to avoid adding complexity to contraints, even though it can be less. Only one rule per channel is needed by trading off a little space.

Note (2):
Intel suggests 25 mil (0.65 mm) spacing for via to channel, and via to pad to two different channels. DDR3 draws about 20 mA per trace with edge rates in the 100s of ps. The main coupling mechanism is capacitive. A 0.65 mm spacing is used for power nets, which draw far more current (inductive coupling however). These rules are far too conservative. To meet these rules, the spacing must be applied to the net.

Note (3):
In order for the constraints DDR_*_DQ_BYTE* to =SAME to win out over DDR_{A,B}_DQ_BYTE* to DDR_{A,B}_DQ_BYTE* so that the small intra-bytelane spacing is used, the spacing rule DDR_DQ2DQ must have a weight greater than DDR_BL2BL.

DDR3

Electrical Contraint Set	Physical	Spacing		
Channel A				
A17 DDR_A_CLK0	DDR_CLK_PHY	DDR_CLK	MEM_A_CLK_P<1..0>	12 29
A17 DDR_A_CLK0	DDR_CLK_PHY	DDR_CLK	MEM_A_CLK_N<1..0>	12 29
A25 DDR_A_CLK1	DDR_CLK_PHY	DDR_CLK	MEM_A_CLK_P<3..2>	12 30
A25 DDR_A_CLK1	DDR_CLK_PHY	DDR_CLK	MEM_A_CLK_N<3..2>	12 30
A16 DDR_A_CTRL0	DDR_CTRL_PHY	DDR_CTRL	MEM_A_CKE<1..0>	12 29
A16 DDR_A_CTRL0	DDR_CTRL_PHY	DDR_CTRL	MEM_A_CS_L<1..0>	12 29
A16 DDR_A_CTRL0	DDR_CTRL_PHY	DDR_CTRL	MEM_A_ODT<1..0>	12 29
A24 DDR_A_CTRL1	DDR_CTRL_PHY	DDR_CTRL	MEM_A_CKE<3..2>	12 30
A24 DDR_A_CTRL1	DDR_CTRL_PHY	DDR_CTRL	MEM_A_CS_L<3..2>	12 30
A24 DDR_A_CTRL1	DDR_CTRL_PHY	DDR_CTRL	MEM_A_ODT<3..2>	12 30
A18 DDR_A_CMD	DDR_CMD_PHY	DDR_CMD	MEM_A_A<15..0>	12 29 30
A18 DDR_A_CMD	DDR_CMD_PHY	DDR_CMD	MEM_A_BA<2..0>	12 29 30
A18 DDR_A_CMD	DDR_CMD_PHY	DDR_CMD	MEM_A_RAS_L	12 29 30
A18 DDR_A_CMD	DDR_CMD_PHY	DDR_CMD	MEM_A_CAS_L	12 29 30
A18 DDR_A_CMD	DDR_CMD_PHY	DDR_CMD	MEM_A_WE_L	12 29 30
A19 DDR_A_DQ_BYTE0	DDR_DQ_PHY	DDR_A_DQ_BYTE0	MEM_A_DQ<7..0>	12 33
A15 DDR_A_DQ_BYTE1	DDR_DQ_PHY	DDR_A_DQ_BYTE1	MEM_A_DQ<15..8>	12 33
A13 DDR_A_DQ_BYTE2	DDR_DQ_PHY	DDR_A_DQ_BYTE2	MEM_A_DQ<23..16>	12 33
A12 DDR_A_DQ_BYTE3	DDR_DQ_PHY	DDR_A_DQ_BYTE3	MEM_A_DQ<31..24>	12 33
A10 DDR_A_DQ_BYTE4	DDR_DQ_PHY	DDR_A_DQ_BYTE4	MEM_A_DQ<39..32>	12 33
A10 DDR_A_DQ_BYTE5	DDR_DQ_PHY	DDR_A_DQ_BYTE5	MEM_A_DQ<47..40>	12 33
A10 DDR_A_DQ_BYTE6	DDR_DQ_PHY	DDR_A_DQ_BYTE6	MEM_A_DQ<55..48>	12 33
A10 DDR_A_DQ_BYTE7	DDR_DQ_PHY	DDR_A_DQ_BYTE7	MEM_A_DQ<63..56>	12 33
A19 DDR_A_DQS0	DDR_DQS_PHY	DDR_A_DQS0	MEM_A_DQS_P<0>	12 33
A17 DDR_A_DQS0	DDR_DQS_PHY	DDR_A_DQS0	MEM_A_DQS_N<0>	12 33
A15 DDR_A_DQS1	DDR_DQS_PHY	DDR_A_DQS1	MEM_A_DQS_P<1>	12 33
A13 DDR_A_DQS1	DDR_DQS_PHY	DDR_A_DQS1	MEM_A_DQS_N<1>	12 33
A26 DDR_A_DQS2	DDR_DQS_PHY	DDR_A_DQS2	MEM_A_DQS_P<2>	12 33
A28 DDR_A_DQS2	DDR_DQS_PHY	DDR_A_DQS2	MEM_A_DQS_N<2>	12 33
A28 DDR_A_DQS3	DDR_DQS_PHY	DDR_A_DQS3	MEM_A_DQS_P<3>	12 33
A26 DDR_A_DQS3	DDR_DQS_PHY	DDR_A_DQS3	MEM_A_DQS_N<3>	12 33
A24 DDR_A_DQS4	DDR_DQS_PHY	DDR_A_DQS4	MEM_A_DQS_P<4>	12 33
A22 DDR_A_DQS4	DDR_DQS_PHY	DDR_A_DQS4	MEM_A_DQS_N<4>	12 33
A20 DDR_A_DQS5	DDR_DQS_PHY	DDR_A_DQS5	MEM_A_DQS_P<5>	12 33
A20 DDR_A_DQS5	DDR_DQS_PHY	DDR_A_DQS5	MEM_A_DQS_N<5>	12 33
A20 DDR_A_DQS6	DDR_DQS_PHY	DDR_A_DQS6	MEM_A_DQS_P<6>	12 33
A20 DDR_A_DQS6	DDR_DQS_PHY	DDR_A_DQS6	MEM_A_DQS_N<6>	12 33
A21 DDR_A_DQS7	DDR_DQS_PHY	DDR_A_DQS7	MEM_A_DQS_P<7>	12 33
A21 DDR_A_DQS7	DDR_DQS_PHY	DDR_A_DQS7	MEM_A_DQS_N<7>	12 33
Channel B				
A21 DDR_B_CLK0	DDR_CLK_PHY	DDR_CLK	MEM_B_CLK_P<1..0>	12 31
A21 DDR_B_CLK0	DDR_CLK_PHY	DDR_CLK	MEM_B_CLK_N<1..0>	12 31
A25 DDR_B_CLK1	DDR_CLK_PHY	DDR_CLK	MEM_B_CLK_P<3..2>	12 32
A25 DDR_B_CLK1	DDR_CLK_PHY	DDR_CLK	MEM_B_CLK_N<3..2>	12 32
A21 DDR_B_CTRL0	DDR_CTRL_PHY	DDR_CTRL	MEM_B_CKE<1..0>	12 31
A21 DDR_B_CTRL0	DDR_CTRL_PHY	DDR_CTRL	MEM_B_CS_L<1..0>	12 31
A21 DDR_B_CTRL0	DDR_CTRL_PHY	DDR_CTRL	MEM_B_ODT<1..0>	12 31
A25 DDR_B_CTRL1	DDR_CTRL_PHY	DDR_CTRL	MEM_B_CKE<3..2>	12 32
A25 DDR_B_CTRL1	DDR_CTRL_PHY	DDR_CTRL	MEM_B_CS_L<3..2>	12 32
A25 DDR_B_CTRL1	DDR_CTRL_PHY	DDR_CTRL	MEM_B_ODT<3..2>	12 32
A21 DDR_B_CMD	DDR_CMD_PHY	DDR_CMD	MEM_B_A<15..0>	12 31 32
A21 DDR_B_CMD	DDR_CMD_PHY	DDR_CMD	MEM_B_BA<2..0>	12 31 32
A21 DDR_B_CMD	DDR_CMD_PHY	DDR_CMD	MEM_B_RAS_L	12 31 32
A22 DDR_B_CMD	DDR_CMD_PHY	DDR_CMD	MEM_B_CAS_L	12 31 32
A22 DDR_B_CMD	DDR_CMD_PHY	DDR_CMD	MEM_B_WE_L	12 31 32
A22 DDR_B_DQ_BYTE0	DDR_DQ_PHY	DDR_B_DQ_BYTE0	MEM_B_DQ<7..0>	12 33
A22 DDR_B_DQ_BYTE1	DDR_DQ_PHY	DDR_B_DQ_BYTE1	MEM_B_DQ<15..8>	12 33
A22 DDR_B_DQ_BYTE2	DDR_DQ_PHY	DDR_B_DQ_BYTE2	MEM_B_DQ<23..16>	12 33
A22 DDR_B_DQ_BYTE3	DDR_DQ_PHY	DDR_B_DQ_BYTE3	MEM_B_DQ<31..24>	12 33
A22 DDR_B_DQ_BYTE4	DDR_DQ_PHY	DDR_B_DQ_BYTE4	MEM_B_DQ<39..32>	12 33
A22 DDR_B_DQ_BYTE5	DDR_DQ_PHY	DDR_B_DQ_BYTE5	MEM_B_DQ<47..40>	12 33
A22 DDR_B_DQ_BYTE6	DDR_DQ_PHY	DDR_B_DQ_BYTE6	MEM_B_DQ<55..48>	12 33
A22 DDR_B_DQ_BYTE7	DDR_DQ_PHY	DDR_B_DQ_BYTE7	MEM_B_DQ<63..56>	12 33
A23 DDR_B_DQS0	DDR_DQS_PHY	DDR_B_DQS0	MEM_B_DQS_P<0>	12 33
A23 DDR_B_DQS0	DDR_DQS_PHY	DDR_B_DQS0	MEM_B_DQS_N<0>	12 33
A23 DDR_B_DQS1	DDR_DQS_PHY	DDR_B_DQS1	MEM_B_DQS_P<1>	12 33
A23 DDR_B_DQS1	DDR_DQS_PHY	DDR_B_DQS1	MEM_B_DQS_N<1>	12 33
A23 DDR_B_DQS2	DDR_DQS_PHY	DDR_B_DQS2	MEM_B_DQS_P<2>	12 33
A23 DDR_B_DQS2	DDR_DQS_PHY	DDR_B_DQS2	MEM_B_DQS_N<2>	12 33
A23 DDR_B_DQS3	DDR_DQS_PHY	DDR_B_DQS3	MEM_B_DQS_P<3>	12 33
A23 DDR_B_DQS3	DDR_DQS_PHY	DDR_B_DQS3	MEM_B_DQS_N<3>	12 33
A23 DDR_B_DQS4	DDR_DQS_PHY	DDR_B_DQS4	MEM_B_DQS_P<4>	12 33
A23 DDR_B_DQS4	DDR_DQS_PHY	DDR_B_DQS4	MEM_B_DQS_N<4>	12 33
A24 DDR_B_DQS5	DDR_DQS_PHY	DDR_B_DQS5	MEM_B_DQS_P<5>	12 33
A24 DDR_B_DQS5	DDR_DQS_PHY	DDR_B_DQS5	MEM_B_DQS_N<5>	12 33
A24 DDR_B_DQS6	DDR_DQS_PHY	DDR_B_DQS6	MEM_B_DQS_P<6>	12 33
A24 DDR_B_DQS6	DDR_DQS_PHY	DDR_B_DQS6	MEM_B_DQS_N<6>	12 33
A24 DDR_B_DQS7	DDR_DQS_PHY	DDR_B_DQS7	MEM_B_DQS_P<7>	12 33
A24 DDR_B_DQS7	DDR_DQS_PHY	DDR_B_DQS7	MEM_B_DQS_N<7>	12 33
Reset				
A24	DDR_50S	CPU	MEM_RESET_L	28 29 30 31 32

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PCI EXPRESS

PCIe-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
PCIE_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
PCIE_PHY	*	PCIE_80D
CLK_PCIE_PHY	*	PCIE_90D
COMP_PCIE_PHY	*	COMP_SE

PCIe-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_ISO	TOP,BOTTOM	=5X_DIELECTRIC	?
PCIE_ISO	*	=4X_DIELECTRIC	?
CLK_PCIE_ISO	*	=5:1_SPACING	?
COMP_PCIE_ISO	*	=4:1_SPACING	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE	*	*	PCIE_ISO
CLK_PCIE	*	*	CLK_PCIE_ISO
COMP_PCIE	*	*	COMP_PCIE_ISO

PCIe Min Spacing Rules (mils) (Maho Bay PDG, Intel Doc# 473718)

Section	Imp	Design	Iso	Design	Comments
4.2.1	80	85	16	15.75	PCIe Gen2, PCIe Gen3, DMI

PCIe and DMI Compensation Rules (mils)

Table	Imp	Design	Iso	Design	Comments
4-5	50	50	15	15.75	PCIe. Impedance inferred from Table 4-7.
4-7	50	50	8	15.75	DMI. Numbers based on Intel stack-up.

PCIe (PCH)

Electrical Contraint Set	Physical	Spacing		
x1 AirPort				
J69 PCIE_GEN2_R2D_CONN_AP	PCIE_PHY	PCIE	PCIE_AP_R2D_P	NO_TEST=TRUE 35
J68 PCIE_GEN2_R2D_CONN_AP	PCIE_PHY	PCIE	PCIE_AP_R2D_N	NO_TEST=TRUE 35
J69	PCIE_PHY	PCIE	PCIE_AP_R2D_C_P	NO_TEST=TRUE 18 35
J68	PCIE_PHY	PCIE	PCIE_AP_R2D_C_N	NO_TEST=TRUE 18 35
J66 PCIE_GEN2_D2R_CONN_AP	PCIE_PHY	PCIE	PCIE_AP_D2R_P	NO_TEST=TRUE 18 35
J66 PCIE_GEN2_D2R_CONN_AP	PCIE_PHY	PCIE	PCIE_AP_D2R_N	NO_TEST=TRUE 18 35
J67 PCIE_REF_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_AP_P	18 35
J68 PCIE_REF_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_AP_N	18 35
x1 Caesar IV				
J61 PCIE_GEN2_R2D	PCIE_PHY	PCIE	PCIE_ENET_R2D_P	NO_TEST=TRUE 39
J60 PCIE_GEN2_R2D	PCIE_PHY	PCIE	PCIE_ENET_R2D_N	NO_TEST=TRUE 39
J61	PCIE_PHY	PCIE	PCIE_ENET_R2D_C_P	NO_TEST=TRUE 18 39
J61	PCIE_PHY	PCIE	PCIE_ENET_R2D_C_N	NO_TEST=TRUE 18 39
J62 PCIE_GEN2_D2R	PCIE_PHY	PCIE	PCIE_ENET_D2R_P	NO_TEST=TRUE 18 39
J63 PCIE_GEN2_D2R	PCIE_PHY	PCIE	PCIE_ENET_D2R_N	NO_TEST=TRUE 18 39
J63	PCIE_PHY	PCIE	PCIE_ENET_D2R_C_P	NO_TEST=TRUE 39
J63	PCIE_PHY	PCIE	PCIE_ENET_D2R_C_N	NO_TEST=TRUE 39
J67 PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_ENET_P	18 39
J61 PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_ENET_N	18 39

PCIE (PCH - TBT)

Electrical Contraint Set	Physical	Spacing		
x4 Thunderbolt				
J57 PCIE_GEN2_R2D_PINV	PCIE_PHY	PCIE	PCIE_TBT_R2D_P<2..0>	NO_TEST=TRUE 36
J57 PCIE_GEN2_R2D_PINV	PCIE_PHY	PCIE	PCIE_TBT_R2D_N<2..0>	NO_TEST=TRUE 36
J62 PCIE_GEN2_R2D	PCIE_PHY	PCIE	PCIE_TBT_R2D_P<3>	NO_TEST=TRUE 36
J61 PCIE_GEN2_R2D	PCIE_PHY	PCIE	PCIE_TBT_R2D_N<3>	NO_TEST=TRUE 36
J57	PCIE_PHY	PCIE	PCIE_TBT_R2D_C_P<3..0>	NO_TEST=TRUE 18 36
J57	PCIE_PHY	PCIE	PCIE_TBT_R2D_C_N<3..0>	NO_TEST=TRUE 18 36
J59	PCIE_PHY	PCIE	PCIE_TBT_D2R_P<3..0>	NO_TEST=TRUE 18 36
J59	PCIE_PHY	PCIE	PCIE_TBT_D2R_N<3..0>	NO_TEST=TRUE 18 36
J67 PCIE_GEN2_D2R_PINV	PCIE_PHY	PCIE	PCIE_TBT_D2R_C_P<1..0>	NO_TEST=TRUE 36
J67 PCIE_GEN2_D2R_PINV	PCIE_PHY	PCIE	PCIE_TBT_D2R_C_N<1..0>	NO_TEST=TRUE 36
J62 PCIE_GEN2_D2R	PCIE_PHY	PCIE	PCIE_TBT_D2R_C_P<2>	NO_TEST=TRUE 36
J63 PCIE_GEN2_D2R	PCIE_PHY	PCIE	PCIE_TBT_D2R_C_N<2>	NO_TEST=TRUE 36
J62 PCIE_GEN2_D2R_PINV	PCIE_PHY	PCIE	PCIE_TBT_D2R_C_P<3>	NO_TEST=TRUE 36
J62 PCIE_GEN2_D2R_PINV	PCIE_PHY	PCIE	PCIE_TBT_D2R_C_N<3>	NO_TEST=TRUE 36
J57 PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_TBT_P	18 36
J68 PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_TBT_N	18 36

PCIe (CPU)

Electrical Contraint Set	Physical	Spacing		
x16 Graphics				
T64 PCIE_GEN3_R2D	PCIE_PHY	PCIE	PEG_R2D_P<15>	NO_TEST=TRUE 10 83
T63 PCIE_GEN3_R2D	PCIE_PHY	PCIE	PEG_R2D_N<15>	NO_TEST=TRUE 10 83
T64	PCIE_PHY	PCIE	PEG_R2D_C_P<15>	NO_TEST=TRUE 83
T63	PCIE_PHY	PCIE	PEG_R2D_C_N<15>	NO_TEST=TRUE 83
T60 PCIE_GEN3_D2R_PINV	PCIE_PHY	PCIE	PEG_D2R_P<15>	NO_TEST=TRUE 83
T61 PCIE_GEN3_D2R_PINV	PCIE_PHY	PCIE	PEG_D2R_N<15>	NO_TEST=TRUE 83
T60	PCIE_PHY	PCIE	PEG_D2R_C_P<15>	NO_TEST=TRUE 10 83
T61	PCIE_PHY	PCIE	PEG_D2R_C_N<15>	NO_TEST=TRUE 10 83
T55 PCIE_GEN3_R2D	PCIE_PHY	PCIE	PEG_R2D_P<14>	NO_TEST=TRUE 10 83
T56 PCIE_GEN3_R2D	PCIE_PHY	PCIE	PEG_R2D_N<14>	NO_TEST=TRUE 10 83
T55	PCIE_PHY	PCIE	PEG_R2D_C_P<14>	NO_TEST=TRUE 83
T56	PCIE_PHY	PCIE	PEG_R2D_C_N<14>	NO_TEST=TRUE 83
T58 PCIE_GEN3_D2R_PINV	PCIE_PHY	PCIE	PEG_D2R_P<14>	NO_TEST=TRUE 83
T59 PCIE_GEN3_D2R_PINV	PCIE_PHY	PCIE	PEG_D2R_N<14>	NO_TEST=TRUE 83
T58	PCIE_PHY	PCIE	PEG_D2R_C_P<14>	NO_TEST=TRUE 10 83
T59	PCIE_PHY	PCIE	PEG_D2R_C_N<14>	NO_TEST=TRUE 10 83
T55 PCIE_GEN3_R2D	PCIE_PHY	PCIE	PEG_R2D_P<13>	NO_TEST=TRUE 10 83
T46 PCIE_GEN3_R2D	PCIE_PHY	PCIE	PEG_R2D_N<13>	NO_TEST=TRUE 10 83
T47	PCIE_PHY	PCIE	PEG_R2D_C_P<13>	NO_TEST=TRUE 83
T47	PCIE_PHY	PCIE	PEG_R2D_C_N<13>	NO_TEST=TRUE 83
T45 PCIE_GEN3_D2R_PINV	PCIE_PHY	PCIE	PEG_D2R_P<13>	NO_TEST=TRUE 83
T45 PCIE_GEN3_D2R_PINV	PCIE_PHY	PCIE	PEG_D2R_N<13>	NO_TEST=TRUE 83
T45	PCIE_PHY	PCIE	PEG_D2R_C_P<13>	NO_TEST=TRUE 10 83
T45	PCIE_PHY	PCIE	PEG_D2R_C_N<13>	NO_TEST=TRUE 10 83
T46 PCIE_GEN3_R2D	PCIE_PHY	PCIE	PEG_R2D_P<12>	NO_TEST=TRUE 10 83
T47 PCIE_GEN3_R2D	PCIE_PHY	PCIE	PEG_R2D_N<12>	NO_TEST=TRUE 10 83
T47	PCIE_PHY	PCIE	PEG_R2D_C_P<12>	NO_TEST=TRUE 83
T47	PCIE_PHY	PCIE	PEG_R2D_C_N<12>	NO_TEST=TRUE 83
T42 PCIE_GEN3_D2R	PCIE_PHY	PCIE	PEG_D2R_P<12>	NO_TEST=TRUE 83
T43 PCIE_GEN3_D2R	PCIE_PHY	PCIE	PEG_D2R_N<12>	NO_TEST=TRUE 83
T42	PCIE_PHY	PCIE	PEG_D2R_C_P<12>	NO_TEST=TRUE 10 83
T43	PCIE_PHY	PCIE	PEG_D2R_C_N<12>	NO_TEST=TRUE 10 83
T42 PCIE_GEN3_R2D	PCIE_PHY	PCIE	PEG_R2D_P<11>	NO_TEST=TRUE 10 83
T43 PCIE_GEN3_R2D	PCIE_PHY	PCIE	PEG_R2D_N<11>	NO_TEST=TRUE 10 83
T43	PCIE_PHY	PCIE	PEG_R2D_C_P<11>	NO_TEST=TRUE 83
T43	PCIE_PHY	PCIE	PEG_R2D_C_N<11>	NO_TEST=TRUE 83
T39 PCIE_GEN3_D2R_PINV	PCIE_PHY	PCIE	PEG_D2R_P<11>	NO_TEST=TRUE 83
T40 PCIE_GEN3_D2R_PINV	PCIE_PHY	PCIE	PEG_D2R_N<11>	NO_TEST=TRUE 83
T39	PCIE_PHY	PCIE	PEG_D2R_C_P<11>	NO_TEST=TRUE 10 83
T39	PCIE_PHY	PCIE	PEG_D2R_C_N<11>	NO_TEST=TRUE 10 83
T33 PCIE_GEN3_R2D_PINV	PCIE_PHY	PCIE	PEG_R2D_P<10>	NO_TEST=TRUE 10 83
T34 PCIE_GEN3_R2D_PINV	PCIE_PHY	PCIE	PEG_R2D_N<10>	NO_TEST=TRUE 10 83
T33	PCIE_PHY	PCIE	PEG_R2D_C_P<10>	NO_TEST=TRUE 83
T33	PCIE_PHY	PCIE	PEG_R2D_C_N<10>	NO_TEST=TRUE 83
T36 PCIE_GEN3_D2R_PINV	PCIE_PHY	PCIE	PEG_D2R_P<10>	NO_TEST=TRUE 83
T37 PCIE_GEN3_D2R_PINV	PCIE_PHY	PCIE	PEG_D2R_N<10>	NO_TEST=TRUE 83
T36	PCIE_PHY	PCIE	PEG_D2R_C_P<10>	NO_TEST=TRUE 10 83
T37	PCIE_PHY	PCIE	PEG_D2R_C_N<10>	NO_TEST=TRUE 10 83
T40 PCIE_GEN3_R2D	PCIE_PHY	PCIE	PEG_R2D_P<9>	NO_TEST=TRUE 10 83
T41 PCIE_GEN3_R2D	PCIE_PHY	PCIE	PEG_R2D_N<9>	NO_TEST=TRUE 10 83
T42	PCIE_PHY	PCIE	PEG_R2D_C_P<9>	NO_TEST=TRUE 83
T42	PCIE_PHY	PCIE	PEG_R2D_C_N<9>	NO_TEST=TRUE 83
T44 PCIE_GEN3_D2R	PCIE_PHY	PCIE	PEG_D2R_P<9>	NO_TEST=TRUE 83
T45 PCIE_GEN3_D2R	PCIE_PHY	PCIE	PEG_D2R_N<9>	NO_TEST=TRUE 83
T44	PCIE_PHY	PCIE	PEG_D2R_C_P<9>	NO_TEST=TRUE 10 83
T45	PCIE_PHY	PCIE	PEG_D2R_C_N<9>	NO_TEST=TRUE 10 83
T40 PCIE_GEN3_R2D_PINV	PCIE_PHY	PCIE	PEG_R2D_P<8>	NO_TEST=TRUE 10 83
T40 PCIE_GEN3_R2D_PINV	PCIE_PHY	PCIE	PEG_R2D_N<8>	NO_TEST=TRUE 10 83
T40	PCIE_PHY	PCIE	PEG_R2D_C_P<8>	NO_TEST=TRUE 83
T40	PCIE_PHY	PCIE	PEG_R2D_C_N<8>	NO_TEST=TRUE 83
T62 PCIE_GEN3_D2R_PINV	PCIE_PHY	PCIE	PEG_D2R_P<8>	NO_TEST=TRUE 83
T62 PCIE_GEN3_D2R_PINV	PCIE_PHY	PCIE	PEG_D2R_N<8>	NO_TEST=TRUE 83
T62	PCIE_PHY	PCIE	PEG_D2R_C_P<8>	NO_TEST=TRUE 10 83
T62	PCIE_PHY	PCIE	PEG_D2R_C_N<8>	NO_TEST=TRUE 10 83

PCIe (CPU)

Electrical Contraint Set	Physical	Spacing		
x16 Graphics				
T64 PCIE_GEN3_R2D_PINV	PCIE_PHY	PCIE	PEG_R2D_P<7>	NO_TEST=TRUE 10 83
T63 PCIE_GEN3_R2D_PINV	PCIE_PHY	PCIE	PEG_R2D_N<7>	NO_TEST=TRUE 10 83
T64	PCIE_PHY	PCIE	PEG_R2D_C_P<7>	NO_TEST=TRUE 83
T63	PCIE_PHY	PCIE	PEG_R2D_C_N<7>	NO_TEST=TRUE 83
T60 PCIE_GEN3_D2R_PINV	PCIE_PHY	PCIE	PEG_D2R_P<7>	NO_TEST=TRUE 83
T61 PCIE_GEN3_D2R_PINV	PCIE_PHY	PCIE	PEG_D2R_N<7>	NO_TEST=TRUE 83
T60	PCIE_PHY	PCIE	PEG_D2R_C_P<7>	NO_TEST=TRUE 10 83
T61	PCIE_PHY	PCIE	PEG_D2R_C_N<7>	NO_TEST=TRUE 10 83
T55 PCIE_GEN3_R2D_PINV	PCIE_PHY	PCIE	PEG_R2D_P<6>	NO_TEST=TRUE 10 83
T56 PCIE_GEN3_R2D_PINV	PCIE_PHY	PCIE	PEG_R2D_N<6>	NO_TEST=TRUE 10 83
T55	PCIE_PHY	PCIE	PEG_R2D_C_P<6>	NO_TEST=TRUE 83
T56	PCIE_PHY	PCIE	PEG_R2D_C_N<6>	NO_TEST=TRUE 83
T58 PCIE_GEN3_D2R_PINV	PCIE_PHY	PCIE	PEG_D2R_P<6>	NO_TEST=TRUE 83
T59 PCIE_GEN3_D2R_PINV	PCIE_PHY	PCIE	PEG_D2R_N<6>	NO_TEST=TRUE 83
T58	PCIE_PHY	PCIE	PEG_D2R_C_P<6>	NO_TEST=TRUE 10 83
T59	PCIE_PHY	PCIE	PEG_D2R_C_N<6>	NO_TEST=TRUE 10 83
T54 PCIE_GEN3_R2D_PINV	PCIE_PHY	PCIE	PEG_R2D_P<5>	NO_TEST=TRUE 10 83
T53 PCIE_GEN3_R2D_PINV	PCIE_PHY	PCIE	PEG_R2D_N<5>	NO_TEST=TRUE 10 83
T54	PCIE_PHY	PCIE	PEG_R2D_C_P<5>	NO_TEST=TRUE 83
T53	PCIE_PHY	PCIE	PEG_R2D_C_N<5>	NO_TEST=TRUE 83
T50 PCIE_GEN3_D2R_PINV	PCIE_PHY	PCIE	PEG_D2R_P<5>	NO_TEST=TRUE 83
T51 PCIE_GEN3_D2R_PINV	PCIE_PHY	PCIE	PEG_D2R_N<5>	NO_TEST=TRUE 83
T50	PCIE_PHY	PCIE	PEG_D2R_C_P<5>	NO_TEST=TRUE 10 83
T51	PCIE_PHY	PCIE	PEG_D2R_C_N<5>	NO_TEST=TRUE 10 83
T46 PCIE_GEN3_R2D	PCIE_PHY	PCIE	PEG_R2D_P<4>	NO_TEST=TRUE 10 83
T47 PCIE_GEN3_R2D	PCIE_PHY	PCIE	PEG_R2D_N<4>	NO_TEST=TRUE 10 83
T46	PCIE_PHY	PCIE	PEG_R2D_C_P<4>	NO_TEST=TRUE 83
T47	PCIE_PHY	PCIE	PEG_R2D_C_N<4>	NO_TEST=TRUE 83
T42 PCIE_GEN3_D2R	PCIE_PHY	PCIE	PEG_D2R_P<4>	NO_TEST=TRUE 83
T43 PCIE_GEN3_D2R	PCIE_PHY	PCIE	PEG_D2R_N<4>	NO_TEST=TRUE 83
T42	PCIE_PHY	PCIE	PEG_D2R_C_P<4>	NO_TEST=TRUE 10 83
T43	PCIE_PHY	PCIE	PEG_D2R_C_N<4>	NO_TEST=TRUE 10 83
T39 PCIE_GEN3_R2D_PINV	PCIE_PHY	PCIE	PEG_R2D_P<3>	NO_TEST=TRUE 10 83
T40 PCIE_GEN3_R2D_PINV	PCIE_PHY	PCIE	PEG_R2D_N<3>	NO_TEST=TRUE 10 83
T39	PCIE_PHY	PCIE	PEG_R2D_C_P<3>	NO_TEST=TRUE 83
T39	PCIE_PHY	PCIE	PEG_R2D_C_N<3>	NO_TEST=TRUE 83
T36 PCIE_GEN3_D2R	PCIE_PHY	PCIE	PEG_D2R_P<3>	NO_TEST=TRUE 83
T37 PCIE_GEN3_D2R	PCIE_PHY	PCIE	PEG_D2R_N<3>	NO_TEST=TRUE 83
T36	PCIE_PHY	PCIE	PEG_D2R_C_P<3>	NO_TEST=TRUE 10 83
T37	PCIE_PHY	PCIE	PEG_D2R_C_N<3>	NO_TEST=TRUE 10 83
T33 PCIE_GEN3_R2D_PINV	PCIE_PHY	PCIE	PEG_R2D_P<2>	NO_TEST=TRUE 10 83
T34 PCIE_GEN3_R2D_PINV	PCIE_PHY	PCIE	PEG_R2D_N<2>	NO_TEST=TRUE 10 83
T33	PCIE_PHY	PCIE	PEG_R2D_C_P<2>	NO_TEST=TRUE 83
T33	PCIE_PHY	PCIE	PEG_R2D_C_N<2>	NO_TEST=TRUE 83
T36 PCIE_GEN3_D2R_PINV	PCIE_PHY	PCIE	PEG_D2R_P<2>	NO_TEST=TRUE 83
T37 PCIE_GEN3_D2R_PINV	PCIE_PHY	PCIE	PEG_D2R_N<2>	NO_TEST=TRUE 83
T36	PCIE_PHY	PCIE	PEG_D2R_C_P<2>	NO_TEST=TRUE 10 83
T37	PCIE_PHY	PCIE	PEG_D2R_C_N<2>	NO_TEST=TRUE 10 83
T40 PCIE_GEN3_R2D_PINV	PCIE_PHY	PCIE	PEG_R2D_P<1>	NO_TEST=TRUE 10 83
T41 PCIE_GEN3_R2D_PINV	PCIE_PHY	PCIE	PEG_R2D_N<1>	NO_TEST=TRUE 10 83
T40	PCIE_PHY	PCIE	PEG_R2D_C_P<1>	NO_TEST=TRUE 83
T41	PCIE_PHY	PCIE	PEG_R2D_C_N<1>	NO_TEST=TRUE 83
T39 PCIE_GEN3_D2R	PCIE_PHY	PCIE	PEG_D2R_P<1>	NO_TEST=TRUE 83
T40 PCIE_GEN3_D2R	PCIE_PHY	PCIE	PEG_D2R_N<1>	NO_TEST=TRUE 83
T39	PCIE_PHY	PCIE	PEG_D2R_C_P<1>	NO_TEST=TRUE 10 83
T40	PCIE_PHY	PCIE	PEG_D2R_C_N<1>	NO_TEST=TRUE 10 83
T66 PCIE_GEN3_R2D	PCIE_PHY	PCIE	PEG_R2D_P<0>	NO_TEST=TRUE 10 83
T66 PCIE_GEN3_R2D	PCIE_PHY	PCIE	PEG_R2D_N<0>	NO_TEST=TRUE 10 83
T66	PCIE_PHY	PCIE	PEG_R2D_C_P<0>	NO_TEST=TRUE 83
T66	PCIE_PHY	PCIE	PEG_R2D_C_N<0>	NO_TEST=TRUE 83
T64 PCIE_GEN3_D2R_PINV	PCIE_PHY	PCIE	PEG_D2R_P<0>	NO_TEST=TRUE 83
T65 PCIE_GEN3_D2R_PINV	PCIE_PHY	PCIE	PEG_D2R_N<0>	NO_TEST=TRUE 83
T64	PCIE_PHY	PCIE	PEG_D2R_C_P<0>	NO_TEST=TRUE 10 83
T65	PCIE_PHY	PCIE	PEG_D2R_C_N<0>	NO_TEST=TRUE 10 83
CPU PCIe Clocks				
T48 PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PEG_CLK100M_P	NO_TEST=TRUE 18 83
T49 PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PEG_CLK100M_N	NO_TEST=TRUE 18 83
CPU PCIe Compensation				
T68	COMP_PCIE_PHY	COMP_PCIE	CPU_PEG_COMP	10

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DMI

DMI-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DMI_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
DMI_PHY	*	DMI_85D

CPU Misc / FDI

CPU-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
COMP_FDI_SE	*	Y	0.3 MM	0.25 MM	3 MM	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
CPU_PHY	*	CPU_50S
COMP_FDI_PHY	*	COMP_FDI_SE

CPU-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_ISO	*	=3:1_SPACING	?
COMP_FDI_ISO	*	=4:1_SPACING	?

FDI Compensation Rules (mils) (Maho Bay PDG, Intel Doc# 473718)

Table	Trace	Design	Iso	Design	Comments
6-4	10	11.81	-	15.75	Using PCIe guidelines

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU	*	*	CPU_ISO
COMP_FDI	*	*	COMP_FDI_ISO

XDP

XDP-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
XDP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
XDP_PHY	*	XDP_50S

XDP-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
XDP_ISO	*	=2:1_SPACING	?
XDP_CLK_ISO	*	=4:1_SPACING	?

Desktop Debug Design Guide (Intel Doc# 430883)

Section	Imp	Design	Iso	Design	Comments
1.5	45-65	50	-	15.75	Isolation is for JTAG clocks. All signals default are 50 Ohm SE.

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
XDP	*	*	XDP_ISO
CLK_JTAG	*	*	XDP_CLK_ISO
OBS_STROBE	*	*	XDP_CLK_ISO

DMI

Electrical Contraint Set	Physical	Spacing		
DMI				
U16 DMI_N2S	DMI_PHY	PCIE	DMI_N2S_P<3..0> NO_TEST=TRUE	10 19
U16 DMI_N2S	DMI_PHY	PCIE	DMI_N2S_N<3..0> NO_TEST=TRUE	10 19
U16 DMI_S2N	DMI_PHY	PCIE	DMI_S2N_P<3..0> NO_TEST=TRUE	10 19
U16 DMI_S2N	DMI_PHY	PCIE	DMI_S2N_N<3..0> NO_TEST=TRUE	10 19
U28 PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	DMI_CLK100M_CPU_P	11 18
U28 PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	DMI_CLK100M_CPU_N	11 18
DMI Compensation				
U17	COMP_PCIE_PHY	COMP_PCIE	PCH_DMI_COMP	19
U22	COMP_PCIE_PHY	COMP_PCIE	PCH_DMI2RBIAS	19

CPU Misc.

Electrical Contraint Set	Physical	Spacing		
CPU Misc.				
U24	CPU_PHY	CPU	CPU_SKTOCC_L	11 64
U24	CPU_PHY	CPU	CPU_PROC_SEL	11 19
U26	CPU_PHY	CPU	CPU_CATERR_L	11 48
U25	CPU_PHY	CPU	CPU_PECI	11 21 47 48
U25	CPU_PHY	CPU	CPU_PROCHOT_L	11 47 48 66
U26	CPU_PHY	CPU	CPU_PROCHOT_R_L	11
U24	CPU_PHY	CPU	CPU_THRMTRIP_L	11 48
U24	CPU_PHY	CPU	CPU_RESET_L	11 26
U24	CPU_PHY	CPU	PLT_RESET_LS1V05_L	11
U25	CPU_PHY	CPU	PM_SYNC	11 19
U25	CPU_PHY	CPU	CPU_PWRGD	11 21 25 28
U26	CPU_PHY	CPU	PM_MEM_PWRGD	11 19 28
U25	CPU_PHY	CPU	PM_MEM_PWRGD_R	11
U25	CPU_PHY	CPU	CPU_MEM_RESET_L	11 28

FDI

Electrical Contraint Set	Physical	Spacing		
FDI Compensation				
U26	COMP_FDI_PHY	COMP_FDI	CPU_FDI_COMPIO	10

XDP

Electrical Contraint Set	Physical	Spacing		
XDP MISC.				
U17 XDP_BPM_L	XDP_PHY	XDP	XDP_BPM_L<7..0>	11 25
U17	XDP_PHY	XDP	CPU_CFG<17..16>	10 25
U25	XDP_PHY	XDP	CPU_CFG<11..0>	10 15 25
U26	XDP_PHY	XDP	XDP_DBRESET_L	11 25
U26	XDP_PHY	XDP	XDP_CPU_PWRGD	25
U25	XDP_PHY	XDP	XDP_CPU_PWRBTN_L	25
U26	XDP_PHY	XDP	XDP_CPU_CFG<0>	25
U25	XDP_PHY	XDP	XDP_VR_READY	25
U27	XDP_PHY	XDP	XDP_CPU_PLTRST_L	25 26
U26	XDP_PHY	XDP	XDP_PCH_PWRGD	25
U26	XDP_PHY	XDP	XDP_PCH_PWRBTN_L	25
U27	XDP_PHY	XDP	XDP_PCH_PLTRST_L	25 26
U17	CLK_PCIE_PHY	CLK_PCIE	ITPCPU_CLK100M_P	11 15
U17	CLK_PCIE_PHY	CLK_PCIE	ITPCPU_CLK100M_N	11 15
U17 ITP_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE	ITPXDP_CLK100M_P	15 18 25
U18 ITP_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE	ITPXDP_CLK100M_N	15 18 25
U17	CLK_PCIE_PHY	CLK_PCIE	XDP_CPU_CLK100M_P	25
U18	CLK_PCIE_PHY	CLK_PCIE	XDP_CPU_CLK100M_N	25
CPU JTAG				
U18	XDP_PHY	CLK_JTAG	XDP_CPU_TCK	11 25
U18	XDP_PHY	XDP	XDP_CPU_TMS	11 25
U18	XDP_PHY	XDP	XDP_CPU_TDI	11 25
U18	XDP_PHY	XDP	XDP_CPU_TDO	11 25
U19	XDP_PHY	XDP	XDP_CPU_TRST_L	11 25
U25	XDP_PHY	XDP	XDP_CPU_PRDY_L	11 25
U25	XDP_PHY	XDP	XDP_CPU_PREQ_L	11 25
PCH JTAG				
U18	XDP_PHY	CLK_JTAG	XDP_PCH_TCK	18 25
U18	XDP_PHY	XDP	XDP_PCH_TMS	18 25
U18	XDP_PHY	XDP	XDP_PCH_TDI	18 25
U18	XDP_PHY	XDP	XDP_PCH_TDO	18 25

Chipset Test Interface

Electrical Contraint Set	Physical	Spacing		
OBS PCH Side				
U19 XDP_PCH_OBS	XDP_PHY	XDP	USB_EXTA_OC_R_L	20 25
U19 XDP_PCH_OBS	XDP_PHY	XDP	USB_EXTB_OC_R_L	20 25
U19 XDP_PCH_OBS	XDP_PHY	XDP	USB_EXTC_OC_R_L	20 25
U19 XDP_PCH_OBS	XDP_PHY	XDP	USB_EXTD_OC_R_L	20 25
U19 XDP_PCH_OBS	XDP_PHY	XDP	USB_EXTB_OC_EHCI_R_L	20 25
U19 XDP_PCH_OBS	XDP_PHY	XDP	USB_EXTD_OC_EHCI_R_L	20 25
U19 XDP_PCH_OBS	XDP_PHY	XDP	AP_PWR_EN_R	20 25
U19 XDP_PCH_OBS	XDP_PHY	XDP	SDCONN_STATE_CHANGE_R	20 25
U19 XDP_PCH_OBS	XDP_PHY	OBS_STROBE	TBT_CIO_PLUG_EVENT_R	21 25
U19 XDP_PCH_OBS	XDP_PHY	XDP	ISOLATE_CPU_MEM_R_L	21 25
U19 XDP_PCH_OBS	XDP_PHY	XDP	GPU_GOOD_R	21 25
U19 XDP_PCH_OBS	XDP_PHY	XDP	DP_AUXCH_ISOL_R	18 25
U19 XDP_PCH_OBS	XDP_PHY	XDP	SATARDRVR_EN_R	18 25
U19 XDP_PCH_OBS	XDP_PHY	XDP	DP_TBT_SEL_R	21 25
U19 XDP_PCH_OBS	XDP_PHY	XDP	JTAG_TBT_TCK_R	21 25
U19 XDP_PCH_OBS	XDP_PHY	XDP	AUD_IPHS_SWITCH_EN_PCH_R	21 25
U19 XDP_PCH_OBS	XDP_PHY	XDP	ENET_LOW_PWR_PCH_R	21 25
U19 XDP_PCH_OBS_UNUSED	XDP_PHY	OBS_STROBE	XDP_PIN03	21 25
OBS XDP Side				
U19	XDP_PHY	XDP	XDP_DA0_USB_EXTA_OC_L	25
U19	XDP_PHY	XDP	XDP_DA1_USB_EXTB_OC_L	25
U19	XDP_PHY	XDP	XDP_DA2_USB_EXTC_OC_L	25
U19	XDP_PHY	XDP	XDP_DA3_USB_EXTD_OC_L	25
U19	XDP_PHY	XDP	XDP_DB0_USB_EXTB_OC_EHCI_L	25
U19	XDP_PHY	XDP	XDP_DB1_USB_EXTD_OC_EHCI_L	25
U19	XDP_PHY	XDP	XDP_DB2_AP_PWR_EN	25
U19	XDP_PHY	XDP	XDP_DB3_SDCONN_STATE_CHANGE	25
U19	XDP_PHY	OBS_STROBE	XDP_FC1_TBT_CIO_PLUG_EVENT	25
U19	XDP_PHY	XDP	XDP_DC0_ISOLATE_CPU_MEM_L	25
U19	XDP_PHY	XDP	XDP_DC1_GPU_GOOD	25
U19	XDP_PHY	XDP	XDP_DC2_DP_AUXCH_ISOL	25
U19	XDP_PHY	XDP	XDP_DC3_SATARDRVR_EN	25
U19	XDP_PHY	XDP	XDP_DD0_DP_TBT_SEL	25
U19	XDP_PHY	XDP	XDP_DD1_JTAG_TBT_TCK	25
U19	XDP_PHY	XDP	XDP_DD2_AUD_IPHS_SWITCH_EN_PCH	25
U19	XDP_PHY	XDP	XDP_DD3_ENET_LOW_PWR_PCH	25
U19	XDP_PHY	OBS_STROBE	XDP_FC0_PCH_GPIO15	25
Standard usage branch off from OBS				
U19	XDP_PHY	XDP	USB_EXTA_OC_L	15 20 45
U19	XDP_PHY	XDP	USB_EXTB_OC_L	15 20 45
U19	XDP_PHY	XDP	USB_EXTC_OC_L	15 20 46
U19	XDP_PHY	XDP	USB_EXTD_OC_L	15 20 46
U19	XDP_PHY	XDP	USB_EXTB_OC_EHCI_L	15 20
U19	XDP_PHY	XDP	USB_EXTD_OC_EHCI_L	15 20
U19	XDP_PHY	XDP	AP_PWR_EN	15 20
U19	XDP_PHY	XDP	SDCONN_STATE_CHANGE	15 20 41
U19	XDP_PHY	OBS_STROBE	TBT_CIO_PLUG_EVENT	15 21
U19	XDP_PHY	XDP	ISOLATE_CPU_MEM_L	21 28 34
U19	XDP_PHY	XDP	GPU_GOOD	5 21
U19	XDP_PHY	XDP	DP_AUXCH_ISOL	15 18
U19	XDP_PHY	XDP	SATARDRVR_EN	15 18
U19	XDP_PHY	XDP	DP_TBT_SEL	21 62 75
U19	XDP_PHY	XDP	JTAG_TBT_TCK	15 21
U19	XDP_PHY	XDP	JTAG_TBT_TCK_ISOL	15 36
U19	XDP_PHY	XDP	AUD_IPHS_SWITCH_EN_PCH	21 26
U19	XDP_PHY	XDP	ENET_LOW_PWR_PCH	15 21 26
U19	XDP_PHY	XDP	DP_AUXCH_ISOL_EN	15

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SATA

SATA-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SATA_PHY	*	SATA_90D
COMP_SATA_PHY	*	SATA_50S

SATA-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_ISO	*	=7.2X_DIELECTRIC	?
COMP_SATA_ISO	*	=5.4X_DIELECTRIC	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SATA	*	*	SATA_ISO
COMP_SATA	*	*	COMP_SATA_ISO

SATA Min Spacing Rules (mils) (Maho Bay PDG, Intel Doc# 473718)

Section	Imp	Design	Iso	Design	Comments
15.2.1	90	95	20	23.62	SATA Gen2, SATA Gen3

SATA Compensation Rules (mils)

Table	Imp	Design	Iso	Design	Comments
15-3	50	50	15	15.75	SATA Gen2, SATA Gen3

SATA

Electrical Contraint Set	Physical	Spacing		
PCH SATA Port 0 (HDD)				
180 SATA_R2D	SATA_PHY	SATA	SATA_HDD_R2D_P	44
182 SATA_R2D	SATA_PHY	SATA	SATA_HDD_R2D_N	44
183	SATA_PHY	SATA	SATA_HDD_R2D_C_P	18 44
189	SATA_PHY	SATA	SATA_HDD_R2D_C_N	18 44
184 SATA_D2R	SATA_PHY	SATA	SATA_HDD_D2R_P	18 44
185 SATA_D2R	SATA_PHY	SATA	SATA_HDD_D2R_N	18 44
181	SATA_PHY	SATA	SATA_HDD_D2R_C_P	44
183	SATA_PHY	SATA	SATA_HDD_D2R_C_N	44
PCH SATA Port 1 (SSD)				
187 SATA_R2D_MUX_SSD	SATA_PHY	SATA	SATA_SSD_R2D_P	18 44
189 SATA_R2D_MUX_SSD	SATA_PHY	SATA	SATA_SSD_R2D_N	18 44
186 SATA_D2R_MUX_SSD	SATA_PHY	SATA	SATA_SSD_D2R_P	18 44
182 SATA_D2R_MUX_SSD	SATA_PHY	SATA	SATA_SSD_D2R_N	18 44
PCH SATA Compensation				
180	COMP_SATA_PHY	COMP_SATA	PCH_SATA1COMP	18
180	COMP_SATA_PHY	COMP_SATA	PCH_SATA3COMP	18
180	COMP_SATA_PHY	COMP_SATA	PCH_SATA3RBIAS	18

Unused

Electrical Contraint Set	Physical	Spacing

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PCH

PCH-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CLK_PCH_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

PCH-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCH_ISO	*	=6.5X_DIELECTRIC	?
COMP_PCH_ISO	*	=2:1_SPACING	?
PCH_ISO	*	=3:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCH	*	*	CLK_PCH_ISO
COMP_PCH	*	*	COMP_PCH_ISO
PCH	*	*	PCH_ISO

PCI

PCI-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CLK_PCI_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

PCI-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCI_ISO	*	=3.6X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCI	*	*	CLK_PCI_ISO

LPC

LPC-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

LPC-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC_ISO	*	=1.5:1_SPACING	?
CLK_LPC_ISO	*	=3.6X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LPC	*	*	LPC_ISO
CLK_LPC	*	*	CLK_LPC_ISO

HDA

HDA-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

HDA-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA_ISO	*	=2X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
HDA	*	*	HDA_ISO

Crystal

Crystal-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_XTAL	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

Crystal-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
XTAL_ISO	*	=4X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
XTAL	*	*	XTAL_ISO

SPI

SPI-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPI-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI_ISO	*	=2X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SPI	*	*	SPI_ISO

PCI

Electrical Contraint Set	Physical	Spacing		
PCI Clock				
H33	CLK_PCI_50S	CLK_PCI	PCH_CLK33M_PCIIN	18 26
H32	CLK_PCI_50S	CLK_PCI	PCH_CLK33M_PCIOUT	20 26

LPC

Electrical Contraint Set	Physical	Spacing		
LPC				
H36	LPC_50S	LPC	LPC_AD<3..0>	18 47 49
H35	LPC_50S	LPC	LPC_R_AD<3..0>	18
H33	LPC_50S	LPC	LPC_FRAME_L	18 47 49
H37	LPC_50S	LPC	LFRAME_L	18
LPC Clocks				
H38	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_LPCPLUS	26 49
H34	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_LPCPLUS_R	20 26
H31	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC	26 47
H32	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC_R	20 26

PCH Clocks

Electrical Contraint Set	Physical	Spacing		
PCH Reference Clock				
H38	CLK_PCH_50S	CLK_PCH	SYSCLK_CLK25M_SB	26
H40	CLK_PCH_50S	CLK_PCH	PCH_CLK25M_XTALIN	18 26
PCH Ref Clock Comp				
H44	PCH_50S	COMP_PCH	PCH_XCLK_RCOMP	18
PCH RTC 32K				
H43	CLK_XTAL	XTAL	PCH_CLK32K_RTCX1	18 26
H41	CLK_XTAL	XTAL	PCH_CLK32K_RTCX2	18 26
H52	CLK_XTAL	XTAL	PCH_CLK32K_RTCX2_R	26
SMC 32K				
H24	CLK_PCH_50S	CLK_PCH	PM_CLK32K_SUSCLK_R	19 48
F50	CLK_PCH_50S	CLK_PCH	SMC_CLK32K	47 48

25 MHz Reference Clocks

Electrical Contraint Set	Physical	Spacing		
25M Reference Crystal				
H42	CLK_XTAL	XTAL	SYSCLK_CLK25M_X1	26
H39	CLK_XTAL	XTAL	SYSCLK_CLK25M_X2	26
H38	CLK_XTAL	XTAL	SYSCLK_CLK25M_X2_R	26
25M Reference Clocks				
H46	CLK_PCH_50S	CLK_PCH	SYSCLK_CLK25M_ENET	26 39
H45	CLK_PCH_50S	CLK_PCH	SYSCLK_CLK25M_ENET_R	26
H48	CLK_PCH_50S	CLK_PCH	SYSCLK_CLK25M_TBT	26 36
H49	CLK_PCH_50S	CLK_PCH	SYSCLK_CLK25M_TBT_R	36

HDA

Electrical Contraint Set	Physical	Spacing		
HDA				
H55	HDA_50S	HDA	HDA_BIT_CLK	18 56
H54	HDA_50S	HDA	HDA_BIT_CLK_R	18
H56	HDA_50S	HDA	HDA_RST_L	18 56
H53	HDA_50S	HDA	HDA_RST_R_L	18
H46	HDA_50S	HDA	HDA_SDOUT	18 56
H57	HDA_50S	HDA	HDA_SDOUT_R	15 18
H60	HDA_50S	HDA	HDA_SYNC	15 18 56
H58	HDA_50S	HDA	HDA_SYNC_R	18
H59	HDA_50S	HDA	HDA_SDIN0	18 56
H50	HDA_50S	HDA	AUD_SDI_R	56
H47	HDA_50S	HDA	SPI_DESCRIPTOR_OVERRIDE_R	15
SPDIF				
H72		HDA	AUD_SPDIF_CHIP	56
H73		HDA	AUD_SPDIF_OUT	56 60

SPI Bootrom

Electrical Contraint Set	Physical	Spacing		
SPI ROM				
H91	SPI_50S	SPI	SPI_CLK_R	18 49
H92	SPI_50S	SPI	SPI_CLK	49
H93	SPI_50S	SPI	SPI_ALT_CLK	49
H40	SPI_50S	SPI	SPI_SMC_CLK	47 48
H49	SPI_50S	SPI	SPI_MLB_CLK	48 49
H90	SPI_50S	SPI	SPI_CS0_R_L	18 49
H89	SPI_50S	SPI	SPI_CS0_L	49
H39	SPI_50S	SPI	SPI_ALT_CS_L	49
H40	SPI_50S	SPI	SPI_SMC_CS_L	47 48
H97	SPI_50S	SPI	SPI_MLB_CS_L	48 49
H95	SPI_50S	SPI	SPI_MOSI_R	18 49
H46	SPI_50S	SPI	SPI_MOSI	49
H41	SPI_50S	SPI	SPI_ALT_MOSI	49
H43	SPI_50S	SPI	SPI_SMC_MOSI	47 48
H48	SPI_50S	SPI	SPI_MLB_MOSI	48 49
H96	SPI_50S	SPI	SPI_MISO	18 49
H40	SPI_50S	SPI	SPI_ALT_MISO	49
H42	SPI_50S	SPI	SPI_SMC_MISO	47 48
H45	SPI_50S	SPI	SPI_MLB_MISO	48 49
H40	SPI_50S	SPI	SPIROM_USE_MLB	21 49

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USB

USB-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
USB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
USB2_PHY	*	USB_90D
USB3_PHY	*	USB_85D
USB_HUB_PHY	*	USB_50S

USB Min Spacing Rules (mils) (Maho Bay PDG, Intel Doc# 473718)

Section	Imp	Design	Iso	Comments
12.2.1	90	90	12/2.8 mils = 4.29:1	USB 2.0
13.3.1	85	85	20/2.8 mils = 7.14:1	USB 3.0
			50/2.8 mils = 17.9:1	USB 2.0/3.0

SMSC Hub Application Note 15.17
Single-ended impedance range from 45-80 ohm is acceptable

USB 2.0 Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB2_ISO	*	=4.4X_DIELECTRIC	?
USB2_ISO	TOP,BOTTOM	=4.4X_DIELECTRIC	?
USB2_CLK_ISO	*	=18X_DIELECTRIC	?
USB2_CLK_ISO	TOP,BOTTOM	=18X_DIELECTRIC	?
USB_HUB_ISO	*	=2:1_SPACING	?

USB 3.0 Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_ISO	*	=7.3X_DIELECTRIC	?
USB3_ISO	TOP,BOTTOM	=7.3X_DIELECTRIC	?
USB3_CLK_ISO	*	=18X_DIELECTRIC	?
USB3_CLK_ISO	TOP,BOTTOM	=18X_DIELECTRIC	?
USB3_USB3_ISO	*	=7.3X_DIELECTRIC	?
USB3_USB3_ISO	TOP,BOTTOM	=7.3X_DIELECTRIC	?
USB3_USB3_ISO	ISL10	=5X_DIELECTRIC	?

USB 2.0 Spacing Rules

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB2	*	*	USB2_ISO
USB2	*CLK*	*	USB2_CLK_ISO
USB2	DISPLAYPORT	*	USB2_CLK_ISO
USB2	*TBT*	*	USB2_CLK_ISO
USB2	*ENET*	*	USB2_CLK_ISO
USB2	*SD*	*	USB2_CLK_ISO
USB3	PCIE	*	USB3_CLK_ISO
USB3	SATA	*	USB3_CLK_ISO
USB_HUB	*	*	USB_HUB_ISO

USB 3.0 Spacing Rules

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB3	*	*	USB3_ISO
USB3	*CLK*	*	USB3_CLK_ISO
USB3	DISPLAYPORT	*	USB3_CLK_ISO
USB3	*TBT*	*	USB3_CLK_ISO
USB3	*ENET*	*	USB3_CLK_ISO
USB3	*SD*	*	USB3_CLK_ISO
USB3	PCIE	*	USB3_CLK_ISO
USB3	SATA	*	USB3_CLK_ISO
USB3	USB3	*	USB3_USB3_ISO

CAMERA CONTROLLER

Camera Controller's SMIA Interface & MISC. Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMIA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CAM_SE	*	Y	0.2 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SMIA_DIFF_PHY	*	SMIA_100D
CAM_PHY	*	CAM_SE

Camera Controller's SMIA Interface & MISC. Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMIA_DIFF_ISO	*	=6:1_SPACING	?
SMIA_DIFF2DIFF	*	=3:1_SPACING	?
CAM_ISO	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SMIA_DIFF	*	*	SMIA_DIFF_ISO
SMIA_DIFF	SMIA_DIFF	*	SMIA_DIFF2DIFF
CAM	*	*	CAM_ISO

USB 3.0 and USB 2.0 Trixies Muxing

Electrical Contraint Set	Physical	Spacing		
External Port A (J4600)				
USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTA_RX_P	45
USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTA_RX_N	45
	USB3_PHY	USB3	USB3_EXTA_RX_F_P	20 45
	USB3_PHY	USB3	USB3_EXTA_RX_F_N	20 45
USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTA_TX_P	20 45
USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTA_TX_N	20 45
	USB3_PHY	USB3	USB3_EXTA_TX_F_P	45
	USB3_PHY	USB3	USB3_EXTA_TX_F_N	45
	USB3_PHY	USB3	USB3_EXTA_TX_C_P	45
	USB3_PHY	USB3	USB3_EXTA_TX_C_N	45
USB2_MUXED_MOJO_CONN	USB2_PHY	USB2	USB_PCH_0_P	20 45
USB2_MUXED_MOJO_CONN	USB2_PHY	USB2	USB_PCH_0_N	20 45
	USB2_PHY	USB2	USB2_EXTA_MUXED_P	45
	USB2_PHY	USB2	USB2_EXTA_MUXED_N	45
	USB2_PHY	USB2	USB2_EXTA_MUXED_F_P	45
	USB2_PHY	USB2	USB2_EXTA_MUXED_F_N	45
External Port B (J4610)				
USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTB_RX_P	45
USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTB_RX_N	45
	USB3_PHY	USB3	USB3_EXTB_RX_F_P	20 45
	USB3_PHY	USB3	USB3_EXTB_RX_F_N	20 45
USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTB_TX_P	20 45
USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTB_TX_N	20 45
	USB3_PHY	USB3	USB3_EXTB_TX_F_P	45
	USB3_PHY	USB3	USB3_EXTB_TX_F_N	45
	USB3_PHY	USB3	USB3_EXTB_TX_C_P	45
	USB3_PHY	USB3	USB3_EXTB_TX_C_N	45
USB2_MUXED_CONN	USB2_PHY	USB2	USB_PCH_1_P	20 45
USB2_MUXED_CONN	USB2_PHY	USB2	USB_PCH_1_N	20 45
	USB2_PHY	USB2	USB_PCH_9_P	20 45
	USB2_PHY	USB2	USB_PCH_9_N	20 45
	USB2_PHY	USB2	USB2_EXTB_MUXED_P	45
	USB2_PHY	USB2	USB2_EXTB_MUXED_N	45
	USB2_PHY	USB2	USB2_EXTB_MUXED_F_P	45
	USB2_PHY	USB2	USB2_EXTB_MUXED_F_N	45
External Port C (J4700)				
USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTC_RX_P	46
USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTC_RX_N	46
	USB3_PHY	USB3	USB3_EXTC_RX_F_P	20 46
	USB3_PHY	USB3	USB3_EXTC_RX_F_N	20 46
USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTC_TX_P	20 46
USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTC_TX_N	20 46
	USB3_PHY	USB3	USB3_EXTC_TX_F_P	46
	USB3_PHY	USB3	USB3_EXTC_TX_F_N	46
	USB3_PHY	USB3	USB3_EXTC_TX_C_P	46
	USB3_PHY	USB3	USB3_EXTC_TX_C_N	46
USB2_CONN	USB2_PHY	USB2	USB_PCH_2_P	20 46
USB2_CONN	USB2_PHY	USB2	USB_PCH_2_N	20 46
	USB2_PHY	USB2	USB2_EXTC_F_P	46
	USB2_PHY	USB2	USB2_EXTC_F_N	46
External Port D (J4710)				
USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTD_RX_P	46
USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTD_RX_N	46
	USB3_PHY	USB3	USB3_EXTD_RX_F_P	20 46
	USB3_PHY	USB3	USB3_EXTD_RX_F_N	20 46
USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTD_TX_P	20 46
USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTD_TX_N	20 46
	USB3_PHY	USB3	USB3_EXTD_TX_F_P	46
	USB3_PHY	USB3	USB3_EXTD_TX_F_N	46
	USB3_PHY	USB3	USB3_EXTD_TX_C_P	46
	USB3_PHY	USB3	USB3_EXTD_TX_C_N	46
USB2_MUXED_CONN	USB2_PHY	USB2	USB_PCH_3_P	20 46
USB2_MUXED_CONN	USB2_PHY	USB2	USB_PCH_3_N	20 46
	USB2_PHY	USB2	USB_PCH_10_P	20 46
	USB2_PHY	USB2	USB_PCH_10_N	20 46
	USB2_PHY	USB2	USB2_EXTD_MUXED_P	46
	USB2_PHY	USB2	USB2_EXTD_MUXED_N	46
	USB2_PHY	USB2	USB2_EXTD_MUXED_F_P	46
	USB2_PHY	USB2	USB2_EXTD_MUXED_F_N	46
Camera (U4200)				
USB2_CONN_INT	USB2_PHY	USB2	USB_CAMERA_P	42
USB2_CONN_INT	USB2_PHY	USB2	USB_CAMERA_N	42
PCH USB Compensation				
	PCH_50S	COMP_PCH	PCH_USB_RBIAS	20

Electrical Contraint Set	Physical	Spacing	Voltage	
Camera Controller Local Ground				
	GND_PHY	GND	0V	CAM_AGND 42
	GND_PHY	GND	0V	CAM_PLLGND 42

USB Hub

Electrical Contraint Set	Physical	Spacing		
USB 2.0 Hub				
USB2_HUB_PCH	USB2_PHY	USB2	USB_PCH_7_P	20 27
USB2_HUB_PCH	USB2_PHY	USB2	USB_PCH_7_N	20 27
USB2_HUB_BT	USB2_PHY	USB2	USB_BT_P	27 35
USB2_HUB_BT	USB2_PHY	USB2	USB_BT_N	27 35
USB2_HUB_BT	USB2_PHY	USB2	USB_BT_MUX_P	35
USB2_HUB_BT	USB2_PHY	USB2	USB_BT_MUX_N	35
	USB_HUB_PHY	USB_HUB	USB_HUB_2P	27
	USB_HUB_PHY	USB_HUB	USB_HUB_2N	27
USB 2.0 Hub Misc.				
	USB_HUB_PHY	USB_HUB	USB_HUB_RESET_L	27
	USB_HUB_PHY	USB_HUB	USB_HUB_VBUS_DET	27
	USB_HUB_PHY	USB_HUB	USB_HUB_NON_REM0	27
	USB_HUB_PHY	USB_HUB	USB_HUB_NON_REM1	27
	USB_HUB_PHY	USB_HUB	USB_HUB_HS_IND	27
USB 2.0 Hub Compensation				
	PCH_50S	COMP_PCH	USB_HUB_RBIAS	27
USB 2.0 Hub Crystal				
	CLK_XTAL	XTAL	USB_HUB_XTAL1	27
	CLK_XTAL	XTAL	USB_HUB_XTAL2	27
	CLK_XTAL	XTAL	USB_HUB_XTAL2_R	27

Camera Controller

Electrical Contraint Set	Physical	Spacing		
SMIA				
SMIA_DATA	SMIA_DIFF_PHY	SMIA_DIFF	SMIA_DATA_P	42
SMIA_DATA	SMIA_DIFF_PHY	SMIA_DIFF	SMIA_DATA_N	42
SMIA_CLK	SMIA_DIFF_PHY	SMIA_DIFF	SMIA_CLK_P	42
SMIA_CLK	SMIA_DIFF_PHY	SMIA_DIFF	SMIA_CLK_N	42
MISC				
	SPI_50S	SPI	CAM_SF_CLK	42
	SPI_50S	SPI	CAM_SF_CLK_R	42
	SPI_50S	SPI	CAM_SF_DIN	42
	SPI_50S	SPI	CAM_SF_DIN_R	42
	SPI_50S	SPI	CAM_SF_CS_L	42
	SPI_50S	SPI	CAM_SF_WP_L	42
	SPI_50S	SPI	CAM_SF_DOUT	42
	SPI_50S	SPI	CAM_SF_DOUT_R	42
	SPI_50S	SPI	CAM_SF_HOLD_L	42
	CAM_PHY	CAM	CAM_USB_VRES	42
	CAM_PHY	CAM	MIPI_RESISTOR	42
		PM	CAM_EXT_BOOT_L	43
		PM	PCH_CAM_EXT_BOOT_R_L	21 43
		PM	CAM_P1V2_RST_HOLDOFF	43
		PM	CAM_P1V2_RST_HOLDOFF_L	43
I2C				
	SMB_PHY	SMB	I2C_CAMSENSOR_SDA	42
	SMB_PHY	SMB	I2C_CAMSENSOR_SCL	42
	SMB_PHY	SMB	SMB_ALS_F_SDA	42
	SMB_PHY	SMB	SMB_ALS_F_SCL	42
Camera Controller Crystal				
	CLK_XTAL	XTAL	CAM_XTAL_IN	42
	CLK_XTAL	XTAL	CAM_XTAL_OUT	42
	CLK_XTAL	XTAL	CAM_XTAL_OUT_R	42

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SMBus

SMBus-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SMB_PHY	*	SMB_55S

SMBus-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB_ISO	*	=2x_DIELECTRIC	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SMB	*	*	SMB_ISO

Sensor

Sensor-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.085 MM
SNS_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SNS_DIFF_PHY	*	1:1_DIFFPAIR
SNS_PHY	*	SNS_50S

Sensor-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE_ISO	*	=4:1_SPACING	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SENSE	*	*	SENSE_ISO
SENSE	POWER	*	PWR_P2MM
SENSE	GND	*	GND_P2MM

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DC-DC

Power-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GND_P3MM	*	Y	0.300 MM	0.200 MM	3.0 MM	=STANDARD	=STANDARD
GND_P5MM	*	Y	0.500 MM	0.200 MM	3.0 MM	=STANDARD	=STANDARD
POWER_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
POWER_P3MM	*	Y	0.300 MM	0.200 MM	3.0 MM	=STANDARD	=STANDARD
POWER_P6MM	*	Y	0.600 MM	0.200 MM	3.0 MM	=STANDARD	=STANDARD
POWER_P5MM	*	Y	0.500 MM	0.200 MM	3.0 MM	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
VR_CTL_PHY	*	POWER_P5MM
VR_CTL_PHY	BGA	STANDARD
VR_VID_PHY	*	POWER_50S
POWER_PHY	*	POWER_P6MM
GND_PHY	*	GND_P5MM

Constraints
Power and Common

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
POWER	*	*	POWER_ISO
GND	*	*	GND_ISO

Power-specific Spacing Definitions
Power and Common

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
POWER_ISO	*	=STANDARD	?

DC-DC Baddies

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
VR_SWITCH	*	*	SWNODE_ISO
VR_SWITCH	*	BGA	BGA_P1MM
VR_SWITCH	VR_SWITCH	*	SWNODE_SW2SW
VR_SWITCH	POWER	*	SWNODE_SW2PWR
VR_SWITCH	GND	*	SWNODE_SW2GND
VR_LGATE	*	*	SWNODE_ISO
VR_LGATE	VR_SWITCH	*	SWNODE_LG2SW

DC-DC Baddies

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SWNODE_ISO	*	=8:1_SPACING	1000
SWNODE_SW2SW	*	=1:1_SPACING	?
SWNODE_SW2PWR	*	=2:1_SPACING	?
SWNODE_SW2GND	*	=2:1_SPACING	?
SWNODE_LG2SW	*	=3:1_SPACING	?

DC-DC Control

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
VR_CTL	*	*	VR_CTL_ISO
VR_VID	*	*	VR_VID_ISO

DC-DC Control

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
VR_CTL_ISO	*	=3:1_SPACING	?
VR_VID_ISO	*	=4X_DIELECTRIC	?

CPU VccSA

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST	
Input Bus						
J24	POWER_PHY	POWER	5V			REG_VCC_U7500 70
J25	POWER_PHY	POWER	5V			REG_PVCC_U7500 70
Local Ground						
J26	GND_PHY	GND	0V			AGND_VCCSAS0 70
VCCIO						
J27	POWER_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_VCCSAS0 70
J28	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_VCCSAS0 70
J29	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_VCCSAS0_RC 70
J31	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_VCCSAS0 70
J30	VR_CTL_PHY	VR_LGATE	12V	TRUE		REG_LGATE_VCCSAS0 70
J33	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_SNUBBER_VCCSAS0 70
J32	VR_CTL_PHY	VR_CTL				REG_VCCSAS0_OCSET 70
J35	VR_CTL_PHY	VR_CTL				REG_VCCSAS0_VO 70
J34		SENSE				SNS_CPU_VCCSA 13 70
J37	VSNS_CPU_VCCSA	SNS_DIFF_PHY	SENSE			SNS_VCCSAS0_XW_P 70
J36	VSNS_CPU_VCCSA	SNS_DIFF_PHY	SENSE			SNS_VCCSAS0_XW_N 70
J38		SENSE				REG_VCCSAS0_FB 70
J39		SENSE				REG_VCCSAS0_RTN 70
J40	VR_CTL_PHY	VR_CTL				REG_VCCSAS0_SREF 70
J41	VR_CTL_PHY	VR_CTL				REG_VCCSAS0_FSEL 70
Output Bus						
J42	POWER_PHY	POWER	0.925V			PPVCCSA_S0 6

CPU VccIO PCH 1.05V S0

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST	
Input Bus						
J1	POWER_PHY	POWER	5V			REG_VCC_U7400 69
J2	POWER_PHY	POWER	5V			REG_PVCC_U7400 69
Local Ground						
J3	GND_PHY	GND	0V			AGND_CPU_P1V05S0 69
1.05V S0						
J5	POWER_PHY	VR_SWITCH	12V	TRUE		REG_CPU_PHASE_P1V05S0 69
J7	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_CPU_BOOT_P1V05S0 69
J6	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_CPU_BOOT_P1V05S0_RC 69
J8	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_CPU_UGATE_P1V05S0 69
J9	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_CPU_UGATE_P1V05S0_R
J10	VR_CTL_PHY	VR_LGATE	12V	TRUE		REG_CPU_LGATE_P1V05S0 69
J12	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_CPU_SNUBBER_P1V05S0 69
J11	VR_CTL_PHY	VR_CTL				REG_CPU_P1V05S0_OCSET 69
J14	VR_CTL_PHY	VR_CTL				REG_CPU_P1V05S0_VO 69
J13	VSNS_CPU_VCCIO	SNS_DIFF_PHY	SENSE			SNS_CPU_VCCIO_P 13 69
J15	VSNS_CPU_VCCIO	SNS_DIFF_PHY	SENSE			SNS_CPU_VCCIO_N 13 69
J16		SNS_DIFF_PHY	SENSE			SNS_CPU_P1V05S0_XW_P 69
J17		SNS_DIFF_PHY	SENSE			SNS_CPU_P1V05S0_XW_N 69
J19			SENSE			REG_CPU_P1V05S0_FB 69
J18			SENSE			REG_CPU_P1V05S0_RTN 69
J21	VR_CTL_PHY	VR_CTL				REG_CPU_P1V05S0_SREF 69
J20	VR_CTL_PHY	VR_CTL				REG_CPU_P1V05S0_FSEL 69
Output Bus						
J22	POWER_PHY	POWER	1.05V			PP1V05_S0_CPU 6

PCH/GPU/TBT 1.05V S0

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST	
Input Bus						
J44	POWER_PHY	POWER	5V			REG_VCC_UB700 99
Local Ground						
J45	GND_PHY	GND	0V			P1V05_AGND 99
1.05V S0						
J47	POWER_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_P1V05S0 99
J48	POWER_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_P1V05S0_L 99
J49	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_P1V05S0 99
J50	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_P1V05S0_RC 99
J51	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_P1V05S0 99
J52	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_P1V05S0_R 99
J53	VR_CTL_PHY	VR_LGATE	12V	TRUE		REG_LGATE_P1V05S0 99
J54	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_SNUBBER_P1V05S0 99
J55	VR_CTL_PHY	VR_CTL				REG_P1V05S0_OCSET 99
J56	VR_CTL_PHY	VR_CTL				REG_P1V05S0_VO 99
J72	POWER_PHY	VR_SWITCH	12V			REG_P1V05S0_VO_R 99
J73	POWER_PHY	VR_SWITCH	12V			P1V05_OCSET_R 99
J61		SENSE				REG_P1V05S0_FB 99
J62		SENSE				REG_P1V05S0_RTN 99
J63	VR_CTL_PHY	VR_CTL				REG_P1V05S0_SREF 99
J64	VR_CTL_PHY	VR_CTL				REG_P1V05S0_FSEL 99
Output Bus						
J68	POWER_PHY	POWER	1.05V			PP1V05_S0_PCH 6
J66	POWER_PHY	POWER	1.05V			PP1V05_S0 6
FET Switched						
J67	POWER_PHY	POWER	1.05V			PP1V05_TBTLC 6 38
J69	POWER_PHY	POWER	1.05V			PP1V05_TBTCIO 6

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CPU Core Phases

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST	
Input Bus						
H10	POWER_PHY	POWER	12V			PP12V_S0_CPUCORE_FLT 66 67 68
H11	POWER_PHY	POWER	5V			REG_VCC_U7100 66
Local Ground						
H20	GND_PHY	GND	0V			AGND_CPU 66 67 68
Phase 1						
H83	POWER_PHY	POWER	12V			REG_LVCC_U7210 67
H85	VR_CTL_PHY	VR_CTL				REG_PWM_CPUCORE_1 66 67
H86	VR_CTL_PHY	VR_CTL				REG_PWM_CPUCORE_1_R 66
H87	POWER_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_CPUCORE_1 67
H88	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_CPUCORE_1 67
H89	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_CPUCORE_1_RC 67
H90	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_CPUCORE_1 67
H91	VR_CTL_PHY	VR_LGATE	12V	TRUE		REG_LGATE_CPUCORE_1 67
H92	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_SNUBBER_CPUCORE_1 67
H93	POWER_PHY	POWER	1.1V			PPCPUCORE_S0_SENSE_1 67
H94	ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE			REG_ISENCORE_1_P 66 67
H95	ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE			REG_ISENCORE_1_N 67
H96			SENSE			REG_ISENCORE_1_NR 66 67
Phase 2						
H113	POWER_PHY	POWER	12V			REG_LVCC_U7230 67
H114	VR_CTL_PHY	VR_CTL				REG_PWM_CPUCORE_2 66 67
H115	VR_CTL_PHY	VR_CTL				REG_PWM_CPUCORE_2_R 66
H116	POWER_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_CPUCORE_2 67
H117	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_CPUCORE_2 67
H118	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_CPUCORE_2_RC 67
H119	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_CPUCORE_2 67
H120	VR_CTL_PHY	VR_LGATE	12V	TRUE		REG_LGATE_CPUCORE_2 67
H121	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_SNUBBER_CPUCORE_2 67
H122	POWER_PHY	POWER	1.1V			PPCPUCORE_S0_SENSE_2 67
H123	ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE			REG_ISENCORE_2_P 66 67
H124	ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE			REG_ISENCORE_2_N 67
H125			SENSE			REG_ISENCORE_2_NR 66 67
Phase 3						
H138	POWER_PHY	POWER	12V			REG_LVCC_U7250 67
H140	VR_CTL_PHY	VR_CTL				REG_PWM_CPUCORE_3 66 67
H141	VR_CTL_PHY	VR_CTL				REG_PWM_CPUCORE_3_R 66
H142	POWER_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_CPUCORE_3 67
H143	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_CPUCORE_3 67
H144	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_CPUCORE_3_RC 67
H145	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_CPUCORE_3 67
H146	VR_CTL_PHY	VR_LGATE	12V	TRUE		REG_LGATE_CPUCORE_3 67
H147	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_SNUBBER_CPUCORE_3 67
H148	POWER_PHY	POWER	1.1V			PPCPUCORE_S0_SENSE_3 67
H149	ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE			REG_ISENCORE_3_P 66 67
H150	ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE			REG_ISENCORE_3_N 67
H151			SENSE			REG_ISENCORE_3_NR 66 67
Phase 4						
H168	POWER_PHY	POWER	12V			REG_LVCC_U7310 68
H170	VR_CTL_PHY	VR_CTL				REG_PWM_CPUCORE_4 66 68
H171	VR_CTL_PHY	VR_CTL				REG_PWM_CPUCORE_4_R 66
H172	POWER_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_CPUCORE_4 68
H173	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_CPUCORE_4 68
H174	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_CPUCORE_4_RC 68
H175	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_CPUCORE_4 68
H176	VR_CTL_PHY	VR_LGATE	12V	TRUE		REG_LGATE_CPUCORE_4 68
H177	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_SNUBBER_CPUCORE_4 68
H178	POWER_PHY	POWER	1.1V			PPCPUCORE_S0_SENSE_4 68
H179	ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE			REG_ISENCORE_4_P 66 68
H180	ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE			REG_ISENCORE_4_N 68
H181			SENSE			REG_ISENCORE_4_NR 66 68
H420	ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE			SNS_CORE_XW_P 66
H421	ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE			SNS_CORE_XW_N 66
H422	ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE			SNS_CORE_R_P 66
H423	ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE			SNS_CORE_R_N 66
H424	ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE			SNS_CPU_VAXG_P 13 66
H425	ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE			SNS_CPU_VAXG_N 13 66
H426	ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE			SNS_CPU_VCORE_P 13 66
H427	ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE			SNS_CPU_VCORE_N 13 66
H428	ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE			SNS_P1V05_IOVDD_XW_P 99
H429	ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE			SNS_P1V05_IOVDD_XW_N 99

CPU AXG Phase and Core Controller

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST	
AXG						
H110	POWER_PHY	POWER	12V			REG_LVCC_U7330 68
H183	VR_CTL_PHY	VR_CTL				REG_PWM_CPUAXG 66 68
H184	VR_CTL_PHY	VR_CTL				REG_PWM_CPUAXG_R 66
H185	POWER_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_CPUAXG 68
H186	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_CPUAXG 68
H187	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_CPUAXG_RC 68
H188	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_CPUAXG 68
H189	VR_CTL_PHY	VR_LGATE	12V	TRUE		REG_LGATE_CPUAXG 68
H190	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_SNUBBER_CPUAXG 68
H191	POWER_PHY	POWER	1.1V			PPCPUAXG_S0_SENSE 68
H192	ISNS_CPU_AXG	SNS_DIFF_PHY	SENSE			REG_ISENAXG_P 68
H193	ISNS_CPU_AXG	SNS_DIFF_PHY	SENSE			REG_ISENAXG_N 68
H194			SENSE			REG_ISENAXG_PR 66 68
H195			SENSE			REG_ISENAXG_NR 66 68
H227	ISNS_CPU_AXG	SNS_DIFF_PHY	SENSE			SNS_AXG_R_P 66
H228	ISNS_CPU_AXG	SNS_DIFF_PHY	SENSE			SNS_AXG_R_N 66
H229	ISNS_CPU_AXG	SNS_DIFF_PHY	SENSE			SNS_AXG_XW_P 66
H230	ISNS_CPU_AXG	SNS_DIFF_PHY	SENSE			SNS_AXG_XW_N 66
ISL6364						
H196	VR_CTL_PHY	VR_CTL				REG_CPUCORE_COMP 66
H197	VR_CTL_PHY	VR_CTL				CPUCORE_COMP_RC 66
H198	VR_CTL_PHY	VR_CTL				REG_CPUCORE_FB 66
H199	VR_CTL_PHY	VR_CTL				CPUCORE_FB_RC 66
H200	VR_CTL_PHY	VR_CTL				CPUCORE_FB_R_1 66
H201	VR_CTL_PHY	VR_CTL				CPUCORE_FB_R_2 66
H202	VR_CTL_PHY	VR_CTL				CPUCORE_PSICOMP_RC 66
H203	VR_CTL_PHY	VR_CTL				REG_CPUCORE_PSICOMP 66
H204	VR_CTL_PHY	VR_CTL				REG_CPUCORE_HFCOMP 66
H205		SENSE				REG_CPUCORE_VSEN 66
H206		SENSE				REG_CPUCORE_RGND 66
H207	VR_CTL_PHY	VR_CTL				REG_CPUCORE_IMON 51 66
H208	VR_CTL_PHY	VR_CTL				CPUCORE_IMON_R 66
H209	VR_CTL_PHY	VR_CTL				REG_CPUCORE_TM 66
H210	VR_CTL_PHY	VR_CTL				REG_CPUCORE_SUTH 66
H211	VR_CTL_PHY	VR_CTL				REG_CPUCORE_NPSI 66
H212	VR_CTL_PHY	VR_CTL				REG_CPUCORE_FDVID 66
H213	VR_CTL_PHY	VR_CTL				REG_CPUCORE_IAUTO 66
H214	VR_CTL_PHY	VR_CTL				REG_CPUCORE_SW_FREQ 66
H215	VR_CTL_PHY	VR_CTL				REG_CPUCORE_RAMPADJ 66
H216	VR_CTL_PHY	VR_CTL				REG_CPUCORE_EN_PWR 66
H217	VR_CTL_PHY	VR_CTL				CPUCORE_EN_PWR_R 66
H218	VR_CTL_PHY	VR_CTL				REG_CPUCORE_RSET 66
H219	VR_CTL_PHY	VR_CTL				REG_CPUAXG_COMP 66
H220	VR_CTL_PHY	VR_CTL				CPUAXG_COMP_RC 66
H221	VR_CTL_PHY	VR_CTL				REG_CPUAXG_FB 66
H222	VR_CTL_PHY	VR_CTL				CPUAXG_FB_RC 66
H223	VR_CTL_PHY	VR_CTL				CPUAXG_FB_R_1 66
H224	VR_CTL_PHY	VR_CTL				CPUAXG_FB_R_2 66
H225	VR_CTL_PHY	VR_CTL				REG_CPUAXG_HFCOMP 66
H231		SENSE				REG_CPUAXG_VSEN 66
H232		SENSE				REG_CPUAXG_RGND 66
H233	VR_CTL_PHY	VR_CTL				REG_CPUAXG_IMON 51 66
H234	VR_CTL_PHY	VR_CTL				CPUAXG_IMON_R 66
H235	VR_CTL_PHY	VR_CTL				REG_CPUAXG_TM 66
H236	VR_CTL_PHY	VR_CTL				REG_CPUAXG_TCOMP 66
H237	VR_CTL_PHY	VR_CTL				REG_CPUAXG_SW_FREQ 66
H238	VR_VID_PHY	VR_VID				CPU_VIDSCLK 13 66
H239	VR_VID_PHY	VR_VID				CPU_VIDSCLK_R 13
H240	VR_VID_PHY	VR_VID				CPU_VIDALERT_L 13 66
H241	VR_VID_PHY	VR_VID				CPU_VIDALERT_R_L 13
H242	VR_VID_PHY	VR_VID				CPU_VIDSOUT 13 66
H243	VR_VID_PHY	VR_VID				CPU_VIDSOUT_R 13
Output Bus						
H198	POWER_PHY	POWER	1.1V			PPVCORE_S0_CPU 6
H199	POWER_PHY	POWER	1.1V			PPVAXG_S0 6

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3.3V S5/5V S4

	Physical	Spacing	Voltage	DIDT	NO_TEST		
Input Bus							
H1840	POWER_PHY	POWER	12V			REG_VIN_U7600	71
H1850	POWER_PHY	POWER	5V			REG_VCC1_U7600	71
H1860	POWER_PHY	POWER	5V			REG_VCC2_U7600	71
3.3V S5							
H1840	POWER_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_P3V3S5	71
H1850	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_P3V3S5	71
H1850	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_P3V3S5_RC	71
H1840	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_P3V3S5	71
H1860	VR_CTL_PHY	VR_LGATE	12V	TRUE		REG_LGATE_P3V3S5	71
H1860	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_P3V3S5	71
H1837	VR_CTL_PHY	VR_CTL				REG_P3V3S5_ISEN	71
H1837	VR_CTL_PHY	VR_CTL				REG_P3V3S5_OCSET	71
H1838	VR_CTL_PHY	VR_CTL				REG_P3V3S5_FSET	71
H1837	VR_CTL_PHY	VR_CTL				REG_P3V3S5_VOUT	71
H1837	VR_CTL_PHY	VR_CTL				REG_P3V3S5_VOUT_R	71
H1837	VR_CTL_PHY	VR_CTL				REG_P3V3S5_FB	71
5V S3							
H1840	POWER_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_P5VS4	71
H1850	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_P5VS4	71
H1850	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_P5VS4_RC	71
H1840	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_P5VS4	71
H1860	VR_CTL_PHY	VR_LGATE	12V	TRUE		REG_LGATE_P5VS4	71
H1860	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_P5VS4	71
H1837	VR_CTL_PHY	VR_CTL				REG_P5VS4_ISEN	71
H1837	VR_CTL_PHY	VR_CTL				REG_P5VS4_OCSET	71
H1838	VR_CTL_PHY	VR_CTL				REG_P5VS4_FSET	71
H1837	VR_CTL_PHY	VR_CTL				REG_P5VS4_VOUT	71
H1837	VR_CTL_PHY	VR_CTL				REG_P5VS4_VOUT_R	71
H1837	VR_CTL_PHY	VR_CTL				REG_P5VS4_FB	71
Output Bus							
H1810	POWER_PHY	POWER	5V			PP5V_S5	6
H1810	POWER_PHY	POWER	5V			PP5V_S4	6
H1810	POWER_PHY	POWER	3.3V			PP3V3_S5	6
FET Switched							
H1820	POWER_PHY	POWER	5V			PP5V_S0	6
H1820	POWER_PHY	POWER	3.3V			PP3V3_S4	6
H1820	POWER_PHY	POWER	3.3V			PP3V3_S0	6
H1820	POWER_PHY	POWER	3.3V			PP3V3_S4_ENET	6
H1820	POWER_PHY	POWER	3.3V			PP3V3_TBTLC	6
H1840	POWER_PHY	POWER	3.3V			PP3V3_S4_AP	6
H1840	POWER_PHY	POWER	3.3V			PP3V3_S0_SSD	6

VDDQ S3 (1.5V)/VTT S0

	Physical	Spacing	Voltage	DIDT	NO_TEST		
Input Bus							
H1820	POWER_PHY	POWER	5V			REG_V5IN_U7700	72
Local Ground							
H1830	GND_PHY	GND	0V			AGND_VDDQS3	72
VDDQ S3							
H1820	POWER_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_VDDQS3	72
H1820	POWER_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_VDDQS3_L	72
H1820	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_VDDQS3	72
H1820	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_VDDQS3_RC	72
H1820	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_VDDQS3	72
H1820	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_VDDQS3_R	72
H1820	VR_CTL_PHY	VR_LGATE	12V	TRUE		REG_LGATE_VDDQS3	72
H1820	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_VDDQS3	72
H1830	POWER_PHY	POWER	1.5V			PPVDDQ_S3_SENSE	
H1820	VR_CTL_PHY	VR_CTL				REG_VDDQS3_VDDQSNS	72
H1820	VR_CTL_PHY	VR_CTL				REG_VDDQS3_VREF	72
H1820	VR_CTL_PHY	VR_CTL				REG_VDDQS3_REFIN	72
H1820	VR_CTL_PHY	VR_CTL				REG_VDDQS3_MODE	72
H1820	VR_CTL_PHY	VR_CTL				REG_VDDQS3_TRIP	72
H1820	VR_CTL_PHY	VR_CTL				LDO_DDRVTTS0_SNS	72
Output Bus							
H1810	POWER_PHY	POWER	1.5V			PPVDDQ_S3	6
H1810	POWER_DDR_PHY	POWER_DDR	0.75V			PPDDRVTT_S0	6
FET Switched							
H1820	POWER_PHY	POWER	1.5V			PP1V5_S0	6
Sensed							
H1820	POWER_PHY	POWER	1.5V			PPVDDQ_S3_DDR	6
H1840	POWER_PHY	POWER	1.5V			PP1V5_S0_CPU_MEM	6
H1840	POWER_PHY	POWER	1.5V			PPFBVDDQ_S0_GPU	6

DDR3 Vref

	Physical	Spacing	Voltage	DIDT	NO_TEST		
Memory Vref							
H1830	POWER_PHY	POWER	3.3V			PP3V3_S4_VREFMRGN_DAC	34
H1830	POWER_PHY	POWER	3.3V			PP3V3_S4_VREFMRGN_CTRL	34
H1830	POWER_DDR_PHY	POWER_DDR	0.75V			PPDDRVREF_DQ_MEM_A_S3	6
H1830	POWER_DDR_PHY	POWER_DDR	0.75V			PPDDRVREF_DQ_MEM_B_S3	6
H1441	POWER_DDR_PHY	POWER_DDR	0.75V			CPU_DIMM_VREF_DAC_A	11 34
H1441	POWER_DDR_PHY	POWER_DDR	0.75V			CPU_DIMM_VREF_DAC_B	11 34
H1830	POWER_DDR_PHY	POWER_DDR	0.75V			PPDDRVREF_CA_MEM_A_S3	6
H1830	POWER_DDR_PHY	POWER_DDR	0.75V			PPDDRVREF_CA_MEM_B_S3	6
H1830	POWER_DDR_PHY	POWER_DDR	0.75V			CPU_DDR_VREF	11
H1840	POWER_DDR_PHY	POWER_DDR	0.75V			PPDDRVTT_S3	6

1.8V S0

	Physical	Spacing	Voltage	DIDT	NO_TEST		
1.8V S0							
H1150	POWER_PHY	VR_SWITCH	5V	TRUE		REG_PHASE_P1V8S0	72
H1150	VR_CTL_PHY	VR_CTL				REG_P1V8S0_VFB	72
H1150	VR_CTL_PHY	VR_CTL				REG_P1V8S0_SYNCH	72
Output Bus							
H1810	POWER_PHY	POWER	1.8V			PP1V8_S0	6

HDD S0

	Physical	Spacing	Voltage	DIDT	NO_TEST		
HDD S0							
H1830	POWER_PHY	POWER	5V			PP5V_S0_HDD	6

12V S5

	Physical	Spacing	Voltage	DIDT	NO_TEST		
Input Bus							
H1830	POWER_PHY	POWER	12V			PP12V_ACDC	6
FET Switched							
H1830	POWER_PHY	POWER	12V			PP12V_S0	6
Sensed							
H1830	POWER_PHY	POWER	12V			PP12V_S5	6
H1830	POWER_PHY	POWER	12V			PP12V_G3H	6
H1441	POWER_PHY	POWER	12V			PP12V_G3H_P3V42	73
H1440	POWER_PHY	POWER	12V			PP12V_S0_FBVDDQ	6
H1440	POWER_PHY	POWER	12V			PP12V_S0_CPU_P1V05	6
H1440	POWER_PHY	POWER	12V			PP12V_S0_VCCSA	6
H1440	POWER_PHY	POWER	12V			PP12V_S0_P1V05	6
H1830	POWER_PHY	POWER	12V			PP12V_S0_HDD	6
H1840	POWER_PHY	POWER	12V			PP12V_S0_BLC	6

Ground/Common

	Physical	Spacing	Voltage	DIDT	NO_TEST	
Common						
H1830	GND_PHY	GND	0V			GND

3V42 S0

	Physical	Spacing	Voltage	DIDT	NO_TEST		
3V42 S0							
H1330	POWER_PHY	VR_SWITCH	5V	TRUE		P3V42G3H_SW	73
H1330	VR_CTL_PHY	VR_CTL				P3V42G3H_FB	73
H1330	VR_CTL_PHY	VR_CTL				P3V42G3H_SHDN_L	73
H1330	POWER_PHY	POWER	3.3V			PP3V3_G3	6
H1330	POWER_PHY	POWER	3.3V			PP3V42_G3H	6

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Thunderbolt

Thunderbolt-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_I2C_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
TBT_SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
TBTDP_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	0.075MM
TBT_GEN_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

Thunderbolt-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_I2C_ISO	*	=2x_DIELECTRIC	?
TBT_SPI_ISO	*	=2x_DIELECTRIC	?
TBTDP_ISO	*	=5x_DIELECTRIC	?
TBTDP_ISO	TOP,BOTTOM	=7x_DIELECTRIC	?
TBT_GEN_ISO	*	=2x_DIELECTRIC	?
BGA_TBT_AREA	*	0.075MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA_TBT	BGA_TBT_AREA
TBT_I2C	*	*	TBT_I2C_ISO
TBT_SPI	*	*	TBT_SPI_ISO
TBTDP	*	*	TBTDP_ISO
TBT_GEN	*	*	TBT_GEN_ISO

SOURCE: Bill Cornelius's T29 Routing Notes

DisplayPort

DP-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	0.08MM	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

DP-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_ISO	*	=6.7X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DISPLAYPORT	*	*	DP_ISO

MAX LENGTH OF DISPLAYPORT TRACES: 6 INCHES

DISPLAYPORT INTRA-PAIR MATCHING SHOULD BE 1 PS. INTER-PAIR MATCHING SHOULD BE WITHIN 150 PS.
DISPLAYPORT AUX CHANNEL INTRA-PAIR MATCHING SHOULD BE 5 PS.

TBT IC Net Properties

Electrical Contraint Set	Physical	Spacing		
	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_P<3..0>	NO_TEST=TRUE 36 90
	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_N<3..0>	NO_TEST=TRUE 36 90
DP_TBTSNK0_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_P<3..0>	NO_TEST=TRUE 36
DP_TBTSNK0_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_N<3..0>	NO_TEST=TRUE 36
	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_C_P	36 90
	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_C_N	36 90
DP_TBTSNK0_AUX	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_P	36
DP_TBTSNK0_AUX	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_N	36
	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_P<3..0>	NO_TEST=TRUE 36 90
	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_N<3..0>	NO_TEST=TRUE 36 90
DP_TBTSNK1_ML	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_P<3..0>	NO_TEST=TRUE 36
DP_TBTSNK1_ML	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_N<3..0>	NO_TEST=TRUE 36
	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_C_P	36 90
	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_C_N	36 90
DP_TBTSNK1_AUX	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_P	36
DP_TBTSNK1_AUX	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_N	36
DP_TNTPNL_TBT_ML_MUX	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_P<3..0>	NO_TEST=TRUE 75
DP_TNTPNL_TBT_ML_MUX	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_N<3..0>	NO_TEST=TRUE 75
DP_TNTPNL_TBT_ML_MUX	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_P<3..0>	NO_TEST=TRUE 75
DP_TNTPNL_TBT_ML_MUX	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_N<3..0>	NO_TEST=TRUE 75
DP_TNTPNL_TBT_AUX_MUX	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_P	75
DP_TNTPNL_TBT_AUX_MUX	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_N	75
	DP_85D	DISPLAYPORT	DP_TBTSRC_AUX_C_P	75
	DP_85D	DISPLAYPORT	DP_TBTSRC_AUX_C_N	75
	TBT_I2C_55S	TBT_I2C	I2C_TBTRTR_SCL	36 50
	TBT_I2C_55S	TBT_I2C	I2C_TBTRTR_SDA	36 50
TBT_SPI_CLK	TBT_I2C_55S	TBT_SPI	TBT_SPI_CLK	36
TBT_SPI_MOSI	TBT_I2C_55S	TBT_SPI	TBT_SPI_MOSI	36
TBT_SPI_MISO	TBT_I2C_55S	TBT_SPI	TBT_SPI_MISO	36
TBT_SPI_CS_L	TBT_I2C_55S	TBT_SPI	TBT_SPI_CS_L	36
	TBT_GEN_55S	TBT_GEN	TBT_A_CONFIG1_BUF	36 77
	TBT_GEN_55S	TBT_GEN	TBT_A_CONFIG2_RC	36 77
	TBT_GEN_55S	TBT_GEN	TBT_B_CONFIG1_BUF	36 79
	TBT_GEN_55S	TBT_GEN	TBT_B_CONFIG2_RC	36 79
	TBT_GEN_55S	TBT_GEN	TBT_A_LSTX	36 77
	TBT_GEN_55S	TBT_GEN	TBT_A_LSRX	36 77
	TBT_GEN_55S	TBT_GEN	TBT_B_LSTX	36 79
	TBT_GEN_55S	TBT_GEN	TBT_B_LSRX	36 79
	TBT_GEN_55S	TBT_GEN	DP_TBTSNK0_HPD	36 90
	TBT_GEN_55S	TBT_GEN	DP_TBTSNK1_HPD	36 90
	TBT_GEN_55S	TBT_GEN	DP_TBTSRC_HPD	36 75
	TBT_GEN_55S	TBT_GEN	DP_TBTSNK0_DDC_CLK	76 92
	TBT_GEN_55S	TBT_GEN	DP_TBTSNK0_DDC_DATA	76 92
	TBT_GEN_55S	TBT_GEN	DP_TBTSNK1_DDC_CLK	76 91
	TBT_GEN_55S	TBT_GEN	DP_TBTSNK1_DDC_DATA	76 91
	TBT_GEN_55S	TBT_GEN	VIDEO_ON	74 78
	TBT_GEN_55S	TBT_GEN	VIDEO_ON_L	5 78
	TBT_GEN_55S	TBT_GEN	BDV_BKL_PWM	48 75
	TBT_GEN_55S	TBT_GEN	GPU_LCD_BKLT_PWM	75 91
	TBT_GEN_55S	TBT_GEN	LCD_BL_PWM	75
	TBT_GEN_55S	TBT_GEN	LCD_BL_FILT	75
	TBT_GEN_55S	TBT_GEN	LCD_BKLT_PWM	75 80

*: Only used on hosts supporting T29 video-in

TBT/DP Net Properties

Electrical Contraint Set	Physical	Spacing		
Port A				
TBT_A_R2D	TBTDP_90D	TBTDP	TBT_A_R2D_C_P<0>	NO_TEST=TRUE 36 77
TBT_A_R2D	TBTDP_90D	TBTDP	TBT_A_R2D_C_N<0>	NO_TEST=TRUE 36 77
TBT_A_R2D_PINV	TBTDP_90D	TBTDP	TBT_A_R2D_C_N<1>	NO_TEST=TRUE 36 77
TBT_A_R2D_PINV	TBTDP_90D	TBTDP	TBT_A_R2D_C_P<1>	NO_TEST=TRUE 36 77
	TBTDP_90D	TBTDP	TBT_A_R2D_P<1..0>	NO_TEST=TRUE 77
	TBTDP_90D	TBTDP	TBT_A_R2D_N<1..0>	NO_TEST=TRUE 77
DP_TBTPA_ML1	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_P<1>	NO_TEST=TRUE 36 77
DP_TBTPA_ML1	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_N<1>	NO_TEST=TRUE 36 77
DP_TBTPA_ML3	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_P<3>	NO_TEST=TRUE 36 77
DP_TBTPA_ML3	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_N<3>	NO_TEST=TRUE 36 77
	DP_85D	DISPLAYPORT	DP_TBTPA_ML_P<1>	NO_TEST=TRUE 77
	DP_85D	DISPLAYPORT	DP_TBTPA_ML_N<1>	NO_TEST=TRUE 77
	DP_85D	DISPLAYPORT	DP_TBTPA_ML_P<3>	NO_TEST=TRUE 77
	DP_85D	DISPLAYPORT	DP_TBTPA_ML_N<3>	NO_TEST=TRUE 77
	DP_85D	DISPLAYPORT	DP_A_LSX_ML_P<1>	77
	DP_85D	DISPLAYPORT	DP_A_LSX_ML_N<1>	77
	TBTDP_90D	TBTDP	TBT_A_D2R_C_P<1..0>	NO_TEST=TRUE 77
	TBTDP_90D	TBTDP	TBT_A_D2R_C_N<1..0>	NO_TEST=TRUE 77
TBT_A_D2R1	TBTDP_90D	TBTDP	TBT_A_D2R_P<1>	NO_TEST=TRUE 36 77
TBT_A_D2R1	TBTDP_90D	TBTDP	TBT_A_D2R_N<1>	NO_TEST=TRUE 36 77
TBT_A_D2R0	TBTDP_90D	TBTDP	TBT_A_D2R_P<0>	NO_TEST=TRUE 36 77
TBT_A_D2R0	TBTDP_90D	TBTDP	TBT_A_D2R_N<0>	NO_TEST=TRUE 36 77
DP_TBT_A_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_C_P	36 77
DP_TBT_A_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_C_N	36 77
	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_P	77
	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_N	77
	DP_85D	DISPLAYPORT	DP_A_AUXCH_DDC_P	77
	DP_85D	DISPLAYPORT	DP_A_AUXCH_DDC_N	77
	TBTDP_90D	TBTDP	TBT_A_D2R1_AUXDDC_P	NO_TEST=TRUE 77
	TBTDP_90D	TBTDP	TBT_A_D2R1_AUXDDC_N	NO_TEST=TRUE 77
Port B				
TBT_B_R2D	TBTDP_90D	TBTDP	TBT_B_R2D_C_P<1..0>	NO_TEST=TRUE 36 79
TBT_B_R2D	TBTDP_90D	TBTDP	TBT_B_R2D_C_N<1..0>	NO_TEST=TRUE 36 79
	TBTDP_90D	TBTDP	TBT_B_R2D_P<1..0>	NO_TEST=TRUE 79
	TBTDP_90D	TBTDP	TBT_B_R2D_N<1..0>	NO_TEST=TRUE 79
DP_TBTPB_ML1	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<1>	NO_TEST=TRUE 36 79
DP_TBTPB_ML1	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_N<1>	NO_TEST=TRUE 36 79
DP_TBTPB_ML3	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<3>	NO_TEST=TRUE 36 79
DP_TBTPB_ML3	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_N<3>	NO_TEST=TRUE 36 79
	DP_85D	DISPLAYPORT	DP_TBTPB_ML_P<1>	NO_TEST=TRUE 79
	DP_85D	DISPLAYPORT	DP_TBTPB_ML_N<1>	NO_TEST=TRUE 79
	DP_85D	DISPLAYPORT	DP_TBTPB_ML_P<3>	NO_TEST=TRUE 79
	DP_85D	DISPLAYPORT	DP_TBTPB_ML_N<3>	NO_TEST=TRUE 79
	DP_85D	DISPLAYPORT	DP_B_LSX_ML_P<1>	NO_TEST=TRUE 79
	DP_85D	DISPLAYPORT	DP_B_LSX_ML_N<1>	NO_TEST=TRUE 79
	TBTDP_90D	TBTDP	TBT_B_D2R_C_P<1..0>	NO_TEST=TRUE 79
	TBTDP_90D	TBTDP	TBT_B_D2R_C_N<1..0>	NO_TEST=TRUE 79
TBT_B_D2R1	TBTDP_90D	TBTDP	TBT_B_D2R_P<1>	NO_TEST=TRUE 36 79
TBT_B_D2R1	TBTDP_90D	TBTDP	TBT_B_D2R_N<1>	NO_TEST=TRUE 36 79
TBT_B_D2R0	TBTDP_90D	TBTDP	TBT_B_D2R_P<0>	NO_TEST=TRUE 36 79
TBT_B_D2R0	TBTDP_90D	TBTDP	TBT_B_D2R_N<0>	NO_TEST=TRUE 36 79
DP_TBT_B_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_C_P	36 79
DP_TBT_B_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_C_N	36 79
	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_P	79
	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_N	79
	DP_85D	DISPLAYPORT	DP_B_AUXCH_DDC_P	79
	DP_85D	DISPLAYPORT	DP_B_AUXCH_DDC_N	79
	TBTDP_90D	TBTDP	TBT_B_D2R1_AUXDDC_P	NO_TEST=TRUE 79
	TBTDP_90D	TBTDP	TBT_B_D2R1_AUXDDC_N	NO_TEST=TRUE 79

DisplayPort

Electrical Contraint Set	Physical	Spacing		
Graphics Source				
DP_INTPNL_EG_ML_MUX	DP_85D	DISPLAYPORT	DP_INT_EG_ML_P<3..0>	NO_TEST=TRUE 75 90
DP_INTPNL_EG_ML_MUX	DP_85D	DISPLAYPORT	DP_INT_EG_ML_N<3..0>	NO_TEST=TRUE 75 90
DP_INTPNL_EG_AUX_MUX	DP_85D	DISPLAYPORT	DP_INT_EG_AUX_P	NO_TEST=TRUE 75 90
DP_INTPNL_EG_AUX_MUX	DP_85D	DISPLAYPORT	DP_INT_EG_AUX_N	NO_TEST=TRUE 75 90
	DP_85D	DISPLAYPORT	DP_INT_EG_AUX_C_P	75
	DP_85D	DISPLAYPORT	DP_INT_EG_AUX_C_N	75
Internal Panel				
	DP_85D	DISPLAYPORT	DP_INTPNL_ML_C_P<3..0>	NO_TEST=TRUE 75
	DP_85D	DISPLAYPORT	DP_INTPNL_ML_C_N<3..0>	NO_TEST=TRUE 75
DP_INTPNL_ML_CONN	DP_85D	DISPLAYPORT	DP_INTPNL_ML_P<3..0>	NO_TEST=TRUE 75 78
DP_INTPNL_ML_CONN	DP_85D	DISPLAYPORT	DP_INTPNL_ML_N<3..0>	NO_TEST=TRUE 75 78
DP_INTPNL_AUX_CONN	DP_85D	DISPLAYPORT	DP_INTPNL_AUX_P	75 78
DP_INTPNL_AUX_CONN	DP_85D	DISPLAYPORT	DP_INTPNL_AUX_N	75 78
Internal DP SPDIF				
		HDA	DP_INT_SPDIF_AUDIO	56 78

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GDDR5

GDDR5-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
GDDR_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	12 MM	=STANDARD	=STANDARD
GDDR_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
GDDR_MA_PHY	*	GDDR_45S
GDDR_ADBI_PHY	*	GDDR_45S
GDDR_CTRL_PHY	*	GDDR_45S
GDDR_CLK_PHY	*	GDDR_80D
GDDR_DQ_PHY	*	GDDR_45S
GDDR_EDC_PHY	*	GDDR_45S
GDDR_DBI_PHY	*	GDDR_45S
GDDR_WCK_PHY	*	GDDR_80D

Main Segment Min Spacing Rules for 4.5 Gbps or Less (AMD Doc# 49919)

	Trace-to-Trace				Isolation				
Table	Micro	Design	Strip	Design	Micro	Design	Strip	Design	Comments
5-6/5-7	2:1	2:1	2:1	2:1	5:1	5:1	5:1	5:1	Memory address (MA). Implented 4.5 Gbps or less rules for K70.
5-6/5-7	2:1	2:1	2:1	2:1	5:1	5:1	5:1	5:1	Address dynamic bus inversion (ADBI)
5-6/5-7	2:1	2:1	2:1	2:1	5:1	5:1	5:1	5:1	Control (CTRL)
5-6/5-7	5:1	5:1	5:1	5:1	5:1	5:1	5:1	5:1	Clock (CLK)
5-6/5-7	3:1	3:1	3:1	3:1	5:1	5:1	5:1	5:1	Data (DQ)
5-6/5-7	7:1	7:1	7:1	7:1	7:1	7:1	7:1	7:1	Error detection pins (EDC). Using larger isolation rules,
5-6/5-7	3:1	3:1	3:1	3:1	5:1	5:1	5:1	5:1	Data dynamic bus inversion (DBI)
5-6/5-7	5:1	5:1	5:1	5:1	5:1	5:1	5:1	5:1	Forwarded clock (WCK)

GDDR5-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR_ISO	*	=3X_DIELECTRIC	?
GDDR_ISO	TOP,BOTTOM	=5X_DIELECTRIC	?
GDDR_MA2MA	*	=2X_DIELECTRIC	?
GDDR_MA2MA	TOP,BOTTOM	=3X_DIELECTRIC	?
GDDR_ADBI2ADBI	*	=2X_DIELECTRIC	?
GDDR_ADBI2ADBI	TOP,BOTTOM	=2X_DIELECTRIC	?
GDDR_CTRL2CTRL	*	=2X_DIELECTRIC	?
GDDR_CTRL2CTRL	TOP,BOTTOM	=2X_DIELECTRIC	?
GDDR_CLK2CLK	*	=3X_DIELECTRIC	?
GDDR_CLK2CLK	TOP,BOTTOM	=5X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR_DQ2DQ	*	=3X_DIELECTRIC	?
GDDR_DQ2DQ	TOP,BOTTOM	=3X_DIELECTRIC	?
GDDR_EDC_ISO	*	=3X_DIELECTRIC	?
GDDR_EDC_ISO	TOP,BOTTOM	=5X_DIELECTRIC	?
GDDR_EDC2EDC	*	=3X_DIELECTRIC	?
GDDR_EDC2EDC	TOP,BOTTOM	=5X_DIELECTRIC	?
GDDR_DBI2DBI	*	=3X_DIELECTRIC	?
GDDR_DBI2DBI	TOP,BOTTOM	=3X_DIELECTRIC	?
GDDR_WCK2WCK	*	=3X_DIELECTRIC	?
GDDR_WCK2WCK	TOP,BOTTOM	=5X_DIELECTRIC	?

Constraints (x in {A, B}, y in {0, 1})

Memory Address: MAxy[8:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_*_*_MA	*	*	GDDR_ISO
GDDR_*_*_MA	=SAME	*	GDDR_MA2MA

Data: DQxy[31:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_*_*_DQ	*	*	GDDR_ISO
GDDR_*_*_DQ	=SAME	*	GDDR_DQ2DQ

Address Dynamic Bus Inversion: ADBIxy

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_*_*_ADBI	*	*	GDDR_ISO
GDDR_*_*_ADBI	=SAME	*	GDDR_ADBI2ADBI

Error Detection: EDCxy[3:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_*_*_EDC	*	*	GDDR_EDC_ISO
GDDR_*_*_EDC	=SAME	*	GDDR_EDC2EDC

Control: Reset, CKExy, CSxy, WExy, RASxy, CASxy

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_CTRL	*	*	GDDR_ISO
GDDR_*_*_CTRL	*	*	GDDR_ISO
GDDR_*_*_CTRL	=SAME	*	GDDR_CTRL2CTRL

Data Dynamic Bus Inversion: DDBIxy[3:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_*_*_DBI	*	*	GDDR_ISO
GDDR_*_*_DBI	=SAME	*	GDDR_DBI2DBI

Clock: CKxy

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_*_*_CLK	*	*	GDDR_ISO
GDDR_*_*_CLK	=SAME	*	GDDR_CLK2CLK

Forwarded Clock: WCKxy[1:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_*_*_WCK	*	*	GDDR_ISO
GDDR_*_*_WCK	=SAME	*	GDDR_WCK2WCK

GPU

GPU-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_GPU_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

GPU-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_GPU_ISO	*	=4:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_GPU	*	*	CLK_GPU_ISO

GDDR5 Frame Buffer A

Electrical Contraint Set	Physical	Spacing				
Memory Address						
1642 GDDR_A0_MA	GDDR_MA_PHY	GDDR_A_0_MA	FB_A0_A<8..0>	NO_TEST=TRUE	84	86
1643 GDDR_A1_MA	GDDR_MA_PHY	GDDR_A_1_MA	FB_A1_A<8..0>	NO_TEST=TRUE	84	86
Address Dynamic Bus Inv						
1644 GDDR_A0_ADBI	GDDR_ADBI_PHY	GDDR_A_0_ADBI	FB_A0_ABI_L	NO_TEST=TRUE	84	86
1645 GDDR_A1_ADBI	GDDR_ADBI_PHY	GDDR_A_1_ADBI	FB_A1_ABI_L	NO_TEST=TRUE	84	86
Control						
1647 GDDR_A0_CKE	GDDR_CTRL_PHY	GDDR_A_0_CTRL	FB_A0_CKE_L	NO_TEST=TRUE	84	86
1648 GDDR_A0_CTRL	GDDR_CTRL_PHY	GDDR_A_0_CTRL	FB_A0_CS_L	NO_TEST=TRUE	84	86
1649 GDDR_A0_CTRL	GDDR_CTRL_PHY	GDDR_A_0_CTRL	FB_A0_WE_L	NO_TEST=TRUE	84	86
1650 GDDR_A0_CTRL	GDDR_CTRL_PHY	GDDR_A_0_CTRL	FB_A0_CAS_L	NO_TEST=TRUE	84	86
1651 GDDR_A0_CTRL	GDDR_CTRL_PHY	GDDR_A_0_CTRL	FB_A0_RAS_L	NO_TEST=TRUE	84	86
1652 GDDR_A1_CKE	GDDR_CTRL_PHY	GDDR_A_1_CTRL	FB_A1_CKE_L	NO_TEST=TRUE	84	86
1653 GDDR_A1_CTRL	GDDR_CTRL_PHY	GDDR_A_1_CTRL	FB_A1_CS_L	NO_TEST=TRUE	84	86
1654 GDDR_A1_CTRL	GDDR_CTRL_PHY	GDDR_A_1_CTRL	FB_A1_WE_L	NO_TEST=TRUE	84	86
1655 GDDR_A1_CTRL	GDDR_CTRL_PHY	GDDR_A_1_CTRL	FB_A1_CAS_L	NO_TEST=TRUE	84	86
1656 GDDR_A1_CTRL	GDDR_CTRL_PHY	GDDR_A_1_CTRL	FB_A1_RAS_L	NO_TEST=TRUE	84	86
Clock						
1657 GDDR_A0_CLK	GDDR_CLK_PHY	GDDR_A_0_CLK	FB_A0_CLK_P	NO_TEST=TRUE	84	86
1658 GDDR_A0_CLK	GDDR_CLK_PHY	GDDR_A_0_CLK	FB_A0_CLK_N	NO_TEST=TRUE	84	86
1659 GDDR_A1_CLK	GDDR_CLK_PHY	GDDR_A_1_CLK	FB_A1_CLK_P	NO_TEST=TRUE	84	86
1660 GDDR_A1_CLK	GDDR_CLK_PHY	GDDR_A_1_CLK	FB_A1_CLK_N	NO_TEST=TRUE	84	86
Data						
1661 GDDR_A0_DQ_BYTE0	GDDR_DQ_PHY	GDDR_A_0_DQ	FB_A0_DQ<7..0>	NO_TEST=TRUE	84	86
1662 GDDR_A0_DQ_BYTE1	GDDR_DQ_PHY	GDDR_A_0_DQ	FB_A0_DQ<15..8>	NO_TEST=TRUE	84	86
1663 GDDR_A0_DQ_BYTE2	GDDR_DQ_PHY	GDDR_A_0_DQ	FB_A0_DQ<23..16>	NO_TEST=TRUE	84	86
1664 GDDR_A0_DQ_BYTE3	GDDR_DQ_PHY	GDDR_A_0_DQ	FB_A0_DQ<31..24>	NO_TEST=TRUE	84	86
1665 GDDR_A1_DQ_BYTE0	GDDR_DQ_PHY	GDDR_A_1_DQ	FB_A1_DQ<7..0>	NO_TEST=TRUE	84	87
1666 GDDR_A1_DQ_BYTE1	GDDR_DQ_PHY	GDDR_A_1_DQ	FB_A1_DQ<15..8>	NO_TEST=TRUE	84	87
1667 GDDR_A1_DQ_BYTE2	GDDR_DQ_PHY	GDDR_A_1_DQ	FB_A1_DQ<23..16>	NO_TEST=TRUE	84	87
1668 GDDR_A1_DQ_BYTE3	GDDR_DQ_PHY	GDDR_A_1_DQ	FB_A1_DQ<31..24>	NO_TEST=TRUE	84	87
Error Detection						
1637 GDDR_A0_EDC0	GDDR_EDC_PHY	GDDR_A_0_EDC	FB_A0_EDC<0>	NO_TEST=TRUE	84	86
1638 GDDR_A0_EDC1	GDDR_EDC_PHY	GDDR_A_0_EDC	FB_A0_EDC<1>	NO_TEST=TRUE	84	86
1639 GDDR_A0_EDC2	GDDR_EDC_PHY	GDDR_A_0_EDC	FB_A0_EDC<2>	NO_TEST=TRUE	84	86
1640 GDDR_A0_EDC3	GDDR_EDC_PHY	GDDR_A_0_EDC	FB_A0_EDC<3>	NO_TEST=TRUE	84	86
1697 GDDR_A1_EDC0	GDDR_EDC_PHY	GDDR_A_1_EDC	FB_A1_EDC<0>	NO_TEST=TRUE	84	86
1696 GDDR_A1_EDC1	GDDR_EDC_PHY	GDDR_A_1_EDC	FB_A1_EDC<1>	NO_TEST=TRUE	84	86
1695 GDDR_A1_EDC2	GDDR_EDC_PHY	GDDR_A_1_EDC	FB_A1_EDC<2>	NO_TEST=TRUE	84	86
1694 GDDR_A1_EDC3	GDDR_EDC_PHY	GDDR_A_1_EDC	FB_A1_EDC<3>	NO_TEST=TRUE	84	86
Data Dynamic Bus Inv						
1637 GDDR_A0_DBI0	GDDR_DBI_PHY	GDDR_A_0_DBI	FB_A0_DBI_L<0>	NO_TEST=TRUE	84	86
1638 GDDR_A0_DBI1	GDDR_DBI_PHY	GDDR_A_0_DBI	FB_A0_DBI_L<1>	NO_TEST=TRUE	84	86
1639 GDDR_A0_DBI2	GDDR_DBI_PHY	GDDR_A_0_DBI	FB_A0_DBI_L<2>	NO_TEST=TRUE	84	86
1640 GDDR_A0_DBI3	GDDR_DBI_PHY	GDDR_A_0_DBI	FB_A0_DBI_L<3>	NO_TEST=TRUE	84	86
1689 GDDR_A1_DBI0	GDDR_DBI_PHY	GDDR_A_1_DBI	FB_A1_DBI_L<0>	NO_TEST=TRUE	84	86
1688 GDDR_A1_DBI1	GDDR_DBI_PHY	GDDR_A_1_DBI	FB_A1_DBI_L<1>	NO_TEST=TRUE	84	86
1687 GDDR_A1_DBI2	GDDR_DBI_PHY	GDDR_A_1_DBI	FB_A1_DBI_L<2>	NO_TEST=TRUE	84	86
1686 GDDR_A1_DBI3	GDDR_DBI_PHY	GDDR_A_1_DBI	FB_A1_DBI_L<3>	NO_TEST=TRUE	84	86
Forwarded Clock						
1635 GDDR_A0_WCK0	GDDR_WCK_PHY	GDDR_A_0_WCK	FB_A0_WCLK_P<0>	NO_TEST=TRUE	84	86
1634 GDDR_A0_WCK0	GDDR_WCK_PHY	GDDR_A_0_WCK	FB_A0_WCLK_N<0>	NO_TEST=TRUE	84	86
1633 GDDR_A0_WCK1	GDDR_WCK_PHY	GDDR_A_0_WCK	FB_A0_WCLK_P<1>	NO_TEST=TRUE	84	86
1632 GDDR_A0_WCK1	GDDR_WCK_PHY	GDDR_A_0_WCK	FB_A0_WCLK_N<1>	NO_TEST=TRUE	84	86
1691 GDDR_A1_WCK0	GDDR_WCK_PHY	GDDR_A_1_WCK	FB_A1_WCLK_P<0>	NO_TEST=TRUE	84	86
1690 GDDR_A1_WCK0	GDDR_WCK_PHY	GDDR_A_1_WCK	FB_A1_WCLK_N<0>	NO_TEST=TRUE	84	86
1693 GDDR_A1_WCK1	GDDR_WCK_PHY	GDDR_A_1_WCK	FB_A1_WCLK_P<1>	NO_TEST=TRUE	84	86
1692 GDDR_A1_WCK1	GDDR_WCK_PHY	GDDR_A_1_WCK	FB_A1_WCLK_N<1>	NO_TEST=TRUE	84	86

GDDR5 Frame Buffer B

Electrical Contraint Set	Physical	Spacing				
Memory Address						
1698 GDDR_B0_MA	GDDR_MA_PHY	GDDR_B_0_MA	FB_B0_A<8..0>	NO_TEST=TRUE	84	87
1699 GDDR_B1_MA	GDDR_MA_PHY	GDDR_B_1_MA	FB_B1_A<8..0>	NO_TEST=TRUE	84	87
Address Dynamic Bus Inv						
1696 GDDR_B0_ADBI	GDDR_ADBI_PHY	GDDR_B_0_ADBI	FB_B0_ABI_L	NO_TEST=TRUE	84	87
1697 GDDR_B1_ADBI	GDDR_ADBI_PHY	GDDR_B_1_ADBI	FB_B1_ABI_L	NO_TEST=TRUE	84	87
Control						
1698 GDDR_B0_CKE	GDDR_CTRL_PHY	GDDR_B_0_CTRL	FB_B0_CKE_L	NO_TEST=TRUE	84	87
1701 GDDR_B0_CTRL	GDDR_CTRL_PHY	GDDR_B_0_CTRL	FB_B0_CS_L	NO_TEST=TRUE	84	87
1702 GDDR_B0_CTRL	GDDR_CTRL_PHY	GDDR_B_0_CTRL	FB_B0_WE_L	NO_TEST=TRUE	84	87
1703 GDDR_B0_CTRL	GDDR_CTRL_PHY	GDDR_B_0_CTRL	FB_B0_CAS_L	NO_TEST=TRUE	84	87
1704 GDDR_B0_CTRL	GDDR_CTRL_PHY	GDDR_B_0_CTRL	FB_B0_RAS_L	NO_TEST=TRUE	84	87
1705 GDDR_B1_CKE	GDDR_CTRL_PHY	GDDR_B_1_CTRL	FB_B1_CKE_L	NO_TEST=TRUE	84	87
1706 GDDR_B1_CTRL	GDDR_CTRL_PHY	GDDR_B_1_CTRL	FB_B1_CS_L	NO_TEST=TRUE	84	87
1707 GDDR_B1_CTRL	GDDR_CTRL_PHY	GDDR_B_1_CTRL	FB_B1_WE_L	NO_TEST=TRUE	84	87
1708 GDDR_B1_CTRL	GDDR_CTRL_PHY	GDDR_B_1_CTRL	FB_B1_CAS_L	NO_TEST=TRUE	84	87
1709 GDDR_B1_CTRL	GDDR_CTRL_PHY	GDDR_B_1_CTRL	FB_B1_RAS_L	NO_TEST=TRUE	84	87
Clock						
1699 GDDR_B0_CLK	GDDR_CLK_PHY	GDDR_B_0_CLK	FB_B0_CLK_P	NO_TEST=TRUE	84	87
1710 GDDR_B0_CLK	GDDR_CLK_PHY	GDDR_B_0_CLK	FB_B0_CLK_N	NO_TEST=TRUE	84	87
1700 GDDR_B1_CLK	GDDR_CLK_PHY	GDDR_B_1_CLK	FB_B1_CLK_P	NO_TEST=TRUE	84	87
1711 GDDR_B1_CLK	GDDR_CLK_PHY	GDDR_B_1_CLK	FB_B1_CLK_N	NO_TEST=TRUE	84	87
Data						
1712 GDDR_B0_DQ_BYTE0	GDDR_DQ_PHY	GDDR_B_0_DQ	FB_B0_DQ<7..0>	NO_TEST=TRUE	84	87
1713 GDDR_B0_DQ_BYTE1	GDDR_DQ_PHY	GDDR_B_0_DQ	FB_B0_DQ<15..8>	NO_TEST=TRUE	84	87
1714 GDDR_B0_DQ_BYTE2	GDDR_DQ_PHY	GDDR_B_0_DQ	FB_B0_DQ<23..16>	NO_TEST=TRUE	84	87
1715 GDDR_B0_DQ_BYTE3	GDDR_DQ_PHY	GDDR_B_0_DQ	FB_B0_DQ<31..24>	NO_TEST=TRUE	84	87
1716 GDDR_B1_DQ_BYTE0	GDDR_DQ_PHY	GDDR_B_1_DQ	FB_B1_DQ<7..0>	NO_TEST=TRUE	84	88
1717 GDDR_B1_DQ_BYTE1	GDDR_DQ_PHY	GDDR_B_1_DQ	FB_B1_DQ<15..8>	NO_TEST=TRUE	84	88
1718 GDDR_B1_DQ_BYTE2	GDDR_DQ_PHY	GDDR_B_1_DQ	FB_B1_DQ<23..16>	NO_TEST=TRUE	84	88
1719 GDDR_B1_DQ_BYTE3	GDDR_DQ_PHY	GDDR_B_1_DQ	FB_B1_DQ<31..24>	NO_TEST=TRUE	84	88
Error Detection						
1720 GDDR_B0_EDC0	GDDR_EDC_PHY	GDDR_B_0_EDC	FB_B0_EDC<0>	NO_TEST=TRUE	84	87
1721 GDDR_B0_EDC1	GDDR_EDC_PHY	GDDR_B_0_EDC	FB_B0_EDC<1>	NO_TEST=TRUE	84	87
1722 GDDR_B0_EDC2	GDDR_EDC_PHY	GDDR_B_0_EDC	FB_B0_EDC<2>	NO_TEST=TRUE	84	87
1723 GDDR_B0_EDC3	GDDR_EDC_PHY	GDDR_B_0_EDC	FB_B0_EDC<3>	NO_TEST=TRUE	84	87
1724 GDDR_B1_EDC0	GDDR_EDC_PHY	GDDR_B_1_EDC	FB_B1_EDC<0>	NO_TEST=TRUE	84	87
1725 GDDR_B1_EDC1	GDDR_EDC_PHY	GDDR_B_1_EDC	FB_B1_EDC<1>	NO_TEST=TRUE	84	87
1726 GDDR_B1_EDC2	GDDR_EDC_PHY	GDDR_B_1_EDC	FB_B1_EDC<2>	NO_TEST=TRUE	84	87
1727 GDDR_B1_EDC3	GDDR_EDC_PHY	GDDR_B_1_EDC	FB_B1_EDC<3>	NO_TEST=TRUE	84	87
Data Dynamic Bus Inv						
1720 GDDR_B0_DBI0	GDDR_DBI_PHY	GDDR_B_0_DBI	FB_B0_DBI_L<0>	NO_TEST=TRUE	84	87
1721 GDDR_B0_DBI1	GDDR_DBI_PHY	GDDR_B_0_DBI	FB_B0_DBI_L<1>	NO_TEST=TRUE	84	87
1722 GDDR_B0_DBI2	GDDR_DBI_PHY	GDDR_B_0_DBI	FB_B0_DBI_L<2>	NO_TEST=TRUE	84	87
1723 GDDR_B0_DBI3	GDDR_DBI_PHY	GDDR_B_0_DBI	FB_B0_DBI_L<3>	NO_TEST=TRUE	84	87
1724 GDDR_B1_DBI0	GDDR_DBI_PHY	GDDR_B_1_DBI	FB_B1_DBI_L<0>	NO_TEST=TRUE	84	87
1725 GDDR_B1_DBI1	GDDR_DBI_PHY	GDDR_B_1_DBI	FB_B1_DBI_L<1>	NO_TEST=TRUE	84	87
1726 GDDR_B1_DBI2	GDDR_DBI_PHY	GDDR_B_1_DBI	FB_B1_DBI_L<2>	NO_TEST=TRUE	84	87
1727 GDDR_B1_DBI3	GDDR_DBI_PHY	GDDR_B_1_DBI	FB_B1_DBI_L<3>	NO_TEST=TRUE	84	87
Forwarded Clock						
1728 GDDR_B0_WCK0	GDDR_WCK_PHY	GDDR_B_0_WCK	FB_B0_WCLK_P<0>	NO_TEST=TRUE	84	87
1729 GDDR_B0_WCK0	GDDR_WCK_PHY	GDDR_B_0_WCK	FB_B0_WCLK_N<0>	NO_TEST=TRUE	84	87
1730 GDDR_B0_WCK1	GDDR_WCK_PHY	GDDR_B_0_WCK	FB_B0_WCLK_P<1>	NO_TEST=TRUE	84	87
1731 GDDR_B0_WCK1	GDDR_WCK_PHY	GDDR_B_0_WCK	FB_B0_WCLK_N<1>	NO_TEST=TRUE	84	87
1740 GDDR_B1_WCK0	GDDR_WCK_PHY	GDDR_B_1_WCK	FB_B1_WCLK_P<0>	NO_TEST=TRUE	84	87
1741 GDDR_B1_WCK0	GDDR_WCK_PHY	GDDR_B_1_WCK	FB_B1_WCLK_N<0>	NO_TEST=TRUE	84	87
1742 GDDR_B1_WCK1	GDDR_WCK_PHY	GDDR_B_1_WCK	FB_B1_WCLK_P<1>	NO_TEST=TRUE	84	87
1743 GDDR_B1_WCK1	GDDR_WCK_PHY	GDDR_B_1_WCK	FB_B1_WCLK_N<1>	NO_TEST=TRUE	84	87

GPU

Electrical Contraint Set	Physical	Spacing				
Clocks						
1747	CLK_GPU_55S	CLK_GPU	PEX_TSTCLK_O_PL		83	
1748	CLK_GPU_55S	CLK_GPU	PEX_TSTCLK_O_NG		83	
1746	CLK_PCIE_PHY	CLK_PCIE	GPU_TESTMODE		83	
1750	CLK_PCIE_PHY	CLK_PCIE	GPU_PEX_TERMP		83	
1745	CLK_GPU_55S	CLK_GPU	FB_A0_CK_MID	NO_TEST=TRUE	86	
1744	CLK_GPU_55S	CLK_GPU	FB_A1_CK_MID	NO_TEST=TRUE	86	
1743	CLK_GPU_55S	CLK_GPU	FB_B0_CK_MID	NO_TEST=TRUE	87	
1742	CLK_GPU_55S	CLK_GPU	FB_B1_CK_MID	NO_TEST=TRUE	87	
1741	CLK_GPU_55S	CLK_GPU	FB_C0_CK_MID	NO_TEST=TRUE	88	
1740	CLK_GPU_55S	CLK_GPU	FB_C1_CK_MID	NO_TEST=TRUE	88	
1739	CLK_GPU_55S	CLK_GPU	FB_D0_CK_MID	NO_TEST=TRUE	89	
1738	CLK_GPU_55S	CLK_GPU	FB_D1_CK_MID	NO_TEST=TRUE	89	
1737	CLK_GPU_55S	CLK_GPU	GPU_JTAG_TCK		91	
1736	CLK_GPU_55S	CLK_GPU	GPU_ROM_SCLK		91	
1735	CLK_GPU_55S	CLK_GPU	GPU_ROM_SCLK_R		91	
1752	CLK_GPU_55S	CLK_GPU	GPU_OSC_27M_XTAL_P		91	
1751	CLK_GPU_55S	CLK_GPU	GPU_OSC_27M_XTAL_N		91	
SMB						
1554	SMB_PHY	SMB	GPU_SMB_CLK		91	
1553	SMB_PHY	SMB	GPU_SMB_DAT		91	
1552	SMB_PHY	SMB	GPU_SMB_CLK_R		50	91
1751	SMB_PHY	SMB	GPU_SMB_DAT_R		50	91
PCIe Compensation						
1681	PCIE_50S	COMP_PCIE	FB_CAL_PD_VDDQ		94	
1680	PCIE_50S	COMP_PCIE	FB_CAL_PU_GND		94	
1679	PCIE_50S	COMP_PCIE	FB_CAL_TERM_GND		94	

Frame Buffer Reset

Electrical Contraint Set	Physical	Spacing				
Reset						
1744 GDDR_A0_RESET	GDDR_50S	GDDR_CTRL	FB_A0_RESET_L		84	86
1745 GDDR_A1_RESET	GDDR_50S	GDDR_CTRL	FB_A1_RESET_L		84	86
1746 GDDR_B0_RESET	GDDR_50S	GDDR_CTRL	FB_B0_RESET_L		84	87
1747 GDDR_B1_RESET	GDDR_50S	GDDR_CTRL	FB_B1_RESET_L		84	87
1748 GDDR_C0_RESET	GDDR_50S	GDDR_CTRL	FB_C0_RESET_L		85	88
1749 GDDR_C1_RESET	GDDR_50S	GDDR_CTRL	FB_C1_RESET_L		85	88
1750 GDDR_D0_RESET	GDDR_50S	GDDR_CTRL	FB_D0_RESET_L		85	89
1751 GDDR_D1_RESET	GDDR_50S	GDDR_CTRL	FB_D1_RESET_L		85	89

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PAGE TITLE: GDDR5/GPU Constraints

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GDDR5 FRAME BUFFER C

Electrical Contraint Set	Physical	Spacing			
Memory Address					
1642 GDDR_C0_MA	GDDR_MA_PHY	GDDR_C_0_MA	FB_C0_A<8..0>	NO_TEST=TRUE	85 88
1643 GDDR_C1_MA	GDDR_MA_PHY	GDDR_C_1_MA	FB_C1_A<8..0>	NO_TEST=TRUE	85 88
Address Dynamic Bus Inv					
1644 GDDR_C0_ADBI	GDDR_ADBI_PHY	GDDR_C_0_ADBI	FB_C0_ABI_L	NO_TEST=TRUE	85 88
1645 GDDR_C1_ADBI	GDDR_ADBI_PHY	GDDR_C_1_ADBI	FB_C1_ABI_L	NO_TEST=TRUE	85 88
Control					
1647 GDDR_C0_CKE	GDDR_CTRL_PHY	GDDR_C_0_CTRL	FB_C0_CKE_L	NO_TEST=TRUE	85 88
1648 GDDR_C0_CTRL	GDDR_CTRL_PHY	GDDR_C_0_CTRL	FB_C0_CS_L	NO_TEST=TRUE	85 88
1649 GDDR_C0_CTRL	GDDR_CTRL_PHY	GDDR_C_0_CTRL	FB_C0_WE_L	NO_TEST=TRUE	85 88
1650 GDDR_C0_CTRL	GDDR_CTRL_PHY	GDDR_C_0_CTRL	FB_C0_CAS_L	NO_TEST=TRUE	85 88
1651 GDDR_C0_CTRL	GDDR_CTRL_PHY	GDDR_C_0_CTRL	FB_C0_RAS_L	NO_TEST=TRUE	85 88
1652 GDDR_C1_CKE	GDDR_CTRL_PHY	GDDR_C_1_CTRL	FB_C1_CKE_L	NO_TEST=TRUE	85 88
1653 GDDR_C1_CTRL	GDDR_CTRL_PHY	GDDR_C_1_CTRL	FB_C1_CS_L	NO_TEST=TRUE	85 88
1654 GDDR_C1_CTRL	GDDR_CTRL_PHY	GDDR_C_1_CTRL	FB_C1_WE_L	NO_TEST=TRUE	85 88
1655 GDDR_C1_CTRL	GDDR_CTRL_PHY	GDDR_C_1_CTRL	FB_C1_CAS_L	NO_TEST=TRUE	85 88
1656 GDDR_C1_CTRL	GDDR_CTRL_PHY	GDDR_C_1_CTRL	FB_C1_RAS_L	NO_TEST=TRUE	85 88
Clock					
1657 GDDR_C0_CLK	GDDR_CLK_PHY	GDDR_C_0_CLK	FB_C0_CLK_P	NO_TEST=TRUE	85 88
1658 GDDR_C0_CLK	GDDR_CLK_PHY	GDDR_C_0_CLK	FB_C0_CLK_N	NO_TEST=TRUE	85 88
1659 GDDR_C1_CLK	GDDR_CLK_PHY	GDDR_C_1_CLK	FB_C1_CLK_P	NO_TEST=TRUE	85 88
1660 GDDR_C1_CLK	GDDR_CLK_PHY	GDDR_C_1_CLK	FB_C1_CLK_N	NO_TEST=TRUE	85 88
Data					
1661 GDDR_C0_DQ_BYTE0	GDDR_DQ_PHY	GDDR_C_0_DQ	FB_C0_DQ<7..0>	NO_TEST=TRUE	85 88
1662 GDDR_C0_DQ_BYTE1	GDDR_DQ_PHY	GDDR_C_0_DQ	FB_C0_DQ<15..8>	NO_TEST=TRUE	85 88
1663 GDDR_C0_DQ_BYTE2	GDDR_DQ_PHY	GDDR_C_0_DQ	FB_C0_DQ<23..16>	NO_TEST=TRUE	85 88
1664 GDDR_C0_DQ_BYTE3	GDDR_DQ_PHY	GDDR_C_0_DQ	FB_C0_DQ<31..24>	NO_TEST=TRUE	85 88
1665 GDDR_C1_DQ_BYTE0	GDDR_DQ_PHY	GDDR_C_1_DQ	FB_C1_DQ<7..0>	NO_TEST=TRUE	85 88
1666 GDDR_C1_DQ_BYTE1	GDDR_DQ_PHY	GDDR_C_1_DQ	FB_C1_DQ<15..8>	NO_TEST=TRUE	85 88
1667 GDDR_C1_DQ_BYTE2	GDDR_DQ_PHY	GDDR_C_1_DQ	FB_C1_DQ<23..16>	NO_TEST=TRUE	85 88
1668 GDDR_C1_DQ_BYTE3	GDDR_DQ_PHY	GDDR_C_1_DQ	FB_C1_DQ<31..24>	NO_TEST=TRUE	85 88
Error Detection					
1669 GDDR_C0_EDC0	GDDR_EDC_PHY	GDDR_C_0_EDC	FB_C0_EDC<0>	NO_TEST=TRUE	85 88
1670 GDDR_C0_EDC1	GDDR_EDC_PHY	GDDR_C_0_EDC	FB_C0_EDC<1>	NO_TEST=TRUE	85 88
1671 GDDR_C0_EDC2	GDDR_EDC_PHY	GDDR_C_0_EDC	FB_C0_EDC<2>	NO_TEST=TRUE	85 88
1672 GDDR_C0_EDC3	GDDR_EDC_PHY	GDDR_C_0_EDC	FB_C0_EDC<3>	NO_TEST=TRUE	85 88
1673 GDDR_C1_EDC0	GDDR_EDC_PHY	GDDR_C_1_EDC	FB_C1_EDC<0>	NO_TEST=TRUE	85 88
1674 GDDR_C1_EDC1	GDDR_EDC_PHY	GDDR_C_1_EDC	FB_C1_EDC<1>	NO_TEST=TRUE	85 88
1675 GDDR_C1_EDC2	GDDR_EDC_PHY	GDDR_C_1_EDC	FB_C1_EDC<2>	NO_TEST=TRUE	85 88
1676 GDDR_C1_EDC3	GDDR_EDC_PHY	GDDR_C_1_EDC	FB_C1_EDC<3>	NO_TEST=TRUE	85 88
Data Dynamic Bus Inv					
1677 GDDR_C0_DBI0	GDDR_DBI_PHY	GDDR_C_0_DBI	FB_C0_DBI_L<0>	NO_TEST=TRUE	85 88
1678 GDDR_C0_DBI1	GDDR_DBI_PHY	GDDR_C_0_DBI	FB_C0_DBI_L<1>	NO_TEST=TRUE	85 88
1679 GDDR_C0_DBI2	GDDR_DBI_PHY	GDDR_C_0_DBI	FB_C0_DBI_L<2>	NO_TEST=TRUE	85 88
1680 GDDR_C0_DBI3	GDDR_DBI_PHY	GDDR_C_0_DBI	FB_C0_DBI_L<3>	NO_TEST=TRUE	85 88
1681 GDDR_C1_DBI0	GDDR_DBI_PHY	GDDR_C_1_DBI	FB_C1_DBI_L<0>	NO_TEST=TRUE	85 88
1682 GDDR_C1_DBI1	GDDR_DBI_PHY	GDDR_C_1_DBI	FB_C1_DBI_L<1>	NO_TEST=TRUE	85 88
1683 GDDR_C1_DBI2	GDDR_DBI_PHY	GDDR_C_1_DBI	FB_C1_DBI_L<2>	NO_TEST=TRUE	85 88
1684 GDDR_C1_DBI3	GDDR_DBI_PHY	GDDR_C_1_DBI	FB_C1_DBI_L<3>	NO_TEST=TRUE	85 88
Forwarded Clock					
1685 GDDR_C0_WCK0	GDDR_WCK_PHY	GDDR_C_0_WCK	FB_C0_WCLK_P<0>	NO_TEST=TRUE	85 88
1686 GDDR_C0_WCK0	GDDR_WCK_PHY	GDDR_C_0_WCK	FB_C0_WCLK_N<0>	NO_TEST=TRUE	85 88
1687 GDDR_C0_WCK1	GDDR_WCK_PHY	GDDR_C_0_WCK	FB_C0_WCLK_P<1>	NO_TEST=TRUE	85 88
1688 GDDR_C0_WCK1	GDDR_WCK_PHY	GDDR_C_0_WCK	FB_C0_WCLK_N<1>	NO_TEST=TRUE	85 88
1689 GDDR_C1_WCK0	GDDR_WCK_PHY	GDDR_C_1_WCK	FB_C1_WCLK_P<0>	NO_TEST=TRUE	85 88
1690 GDDR_C1_WCK0	GDDR_WCK_PHY	GDDR_C_1_WCK	FB_C1_WCLK_N<0>	NO_TEST=TRUE	85 88
1691 GDDR_C1_WCK1	GDDR_WCK_PHY	GDDR_C_1_WCK	FB_C1_WCLK_P<1>	NO_TEST=TRUE	85 88
1692 GDDR_C1_WCK1	GDDR_WCK_PHY	GDDR_C_1_WCK	FB_C1_WCLK_N<1>	NO_TEST=TRUE	85 88
Memory Address					
1745 GDDR_A0_MA	GDDR_MA_PHY	GDDR_A_0_MA	FB_A0_A<12>	NO_TEST=TRUE	84 86
1746 GDDR_A1_MA	GDDR_MA_PHY	GDDR_A_1_MA	FB_A1_A<12>	NO_TEST=TRUE	84 86
1747 GDDR_B0_MA	GDDR_MA_PHY	GDDR_B_0_MA	FB_B0_A<12>	NO_TEST=TRUE	84 87
1748 GDDR_B1_MA	GDDR_MA_PHY	GDDR_B_1_MA	FB_B1_A<12>	NO_TEST=TRUE	84 87
1749 GDDR_C0_MA	GDDR_MA_PHY	GDDR_C_0_MA	FB_C0_A<12>	NO_TEST=TRUE	85 88
1750 GDDR_C1_MA	GDDR_MA_PHY	GDDR_C_1_MA	FB_C1_A<12>	NO_TEST=TRUE	85 88
1751 GDDR_D0_MA	GDDR_MA_PHY	GDDR_D_0_MA	FB_D0_A<12>	NO_TEST=TRUE	85 89
1752 GDDR_D1_MA	GDDR_MA_PHY	GDDR_D_1_MA	FB_D1_A<12>	NO_TEST=TRUE	85 89

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Electrical Contraint Set	Physical	Spacing			
Memory Address					
1695 GDDR_D0_MA	GDDR_MA_PHY	GDDR_D_0_MA	FB_D0_A<8..0>	NO_TEST=TRUE	85 89
1696 GDDR_D1_MA	GDDR_MA_PHY	GDDR_D_1_MA	FB_D1_A<8..0>	NO_TEST=TRUE	85 89
Address Dynamic Bus Inv					
1695 GDDR_D0_ADBI	GDDR_ADBI_PHY	GDDR_D_0_ADBI	FB_D0_ABI_L	NO_TEST=TRUE	85 89
1697 GDDR_D1_ADBI	GDDR_ADBI_PHY	GDDR_D_1_ADBI	FB_D1_ABI_L	NO_TEST=TRUE	85 89
Control					
1698 GDDR_D0_CKE	GDDR_CTRL_PHY	GDDR_D_0_CTRL	FB_D0_CKE_L	NO_TEST=TRUE	85 89
1699 GDDR_D0_CTRL	GDDR_CTRL_PHY	GDDR_D_0_CTRL	FB_D0_CS_L	NO_TEST=TRUE	85 89
1700 GDDR_D0_CTRL	GDDR_CTRL_PHY	GDDR_D_0_CTRL	FB_D0_WE_L	NO_TEST=TRUE	85 89
1702 GDDR_D0_CTRL	GDDR_CTRL_PHY	GDDR_D_0_CTRL	FB_D0_CAS_L	NO_TEST=TRUE	85 89
1703 GDDR_D0_CTRL	GDDR_CTRL_PHY	GDDR_D_0_CTRL	FB_D0_RAS_L	NO_TEST=TRUE	85 89
1705 GDDR_D1_CKE	GDDR_CTRL_PHY	GDDR_D_1_CTRL	FB_D1_CKE_L	NO_TEST=TRUE	85 89
1706 GDDR_D1_CTRL	GDDR_CTRL_PHY	GDDR_D_1_CTRL	FB_D1_CS_L	NO_TEST=TRUE	85 89
1707 GDDR_D1_CTRL	GDDR_CTRL_PHY	GDDR_D_1_CTRL	FB_D1_WE_L	NO_TEST=TRUE	85 89
1708 GDDR_D1_CTRL	GDDR_CTRL_PHY	GDDR_D_1_CTRL	FB_D1_CAS_L	NO_TEST=TRUE	85 89
1709 GDDR_D1_CTRL	GDDR_CTRL_PHY	GDDR_D_1_CTRL	FB_D1_RAS_L	NO_TEST=TRUE	85 89
Clock					
1699 GDDR_D0_CLK	GDDR_CLK_PHY	GDDR_D_0_CLK	FB_D0_CLK_P	NO_TEST=TRUE	85 89
1710 GDDR_D0_CLK	GDDR_CLK_PHY	GDDR_D_0_CLK	FB_D0_CLK_N	NO_TEST=TRUE	85 89
1708 GDDR_D1_CLK	GDDR_CLK_PHY	GDDR_D_1_CLK	FB_D1_CLK_P	NO_TEST=TRUE	85 89
1711 GDDR_D1_CLK	GDDR_CLK_PHY	GDDR_D_1_CLK	FB_D1_CLK_N	NO_TEST=TRUE	85 89
Data					
1712 GDDR_D0_DQ_BYTE0	GDDR_DQ_PHY	GDDR_D_0_DQ	FB_D0_DQ<7..0>	NO_TEST=TRUE	85 89
1713 GDDR_D0_DQ_BYTE1	GDDR_DQ_PHY	GDDR_D_0_DQ	FB_D0_DQ<15..8>	NO_TEST=TRUE	85 89
1714 GDDR_D0_DQ_BYTE2	GDDR_DQ_PHY	GDDR_D_0_DQ	FB_D0_DQ<23..16>	NO_TEST=TRUE	85 89
1715 GDDR_D0_DQ_BYTE3	GDDR_DQ_PHY	GDDR_D_0_DQ	FB_D0_DQ<31..24>	NO_TEST=TRUE	85 89
1716 GDDR_D1_DQ_BYTE0	GDDR_DQ_PHY	GDDR_D_1_DQ	FB_D1_DQ<7..0>	NO_TEST=TRUE	85 89
1717 GDDR_D1_DQ_BYTE1	GDDR_DQ_PHY	GDDR_D_1_DQ	FB_D1_DQ<15..8>	NO_TEST=TRUE	85 89
1718 GDDR_D1_DQ_BYTE2	GDDR_DQ_PHY	GDDR_D_1_DQ	FB_D1_DQ<23..16>	NO_TEST=TRUE	85 89
1719 GDDR_D1_DQ_BYTE3	GDDR_DQ_PHY	GDDR_D_1_DQ	FB_D1_DQ<31..24>	NO_TEST=TRUE	85 89
Error Detection					
1720 GDDR_D0_EDC0	GDDR_EDC_PHY	GDDR_D_0_EDC	FB_D0_EDC<0>	NO_TEST=TRUE	85 89
1721 GDDR_D0_EDC1	GDDR_EDC_PHY	GDDR_D_0_EDC	FB_D0_EDC<1>	NO_TEST=TRUE	85 89
1722 GDDR_D0_EDC2	GDDR_EDC_PHY	GDDR_D_0_EDC	FB_D0_EDC<2>	NO_TEST=TRUE	85 89
1723 GDDR_D0_EDC3	GDDR_EDC_PHY	GDDR_D_0_EDC	FB_D0_EDC<3>	NO_TEST=TRUE	85 89
1724 GDDR_D1_EDC0	GDDR_EDC_PHY	GDDR_D_1_EDC	FB_D1_EDC<0>	NO_TEST=TRUE	85 89
1725 GDDR_D1_EDC1	GDDR_EDC_PHY	GDDR_D_1_EDC	FB_D1_EDC<1>	NO_TEST=TRUE	85 89
1726 GDDR_D1_EDC2	GDDR_EDC_PHY	GDDR_D_1_EDC	FB_D1_EDC<2>	NO_TEST=TRUE	85 89
1727 GDDR_D1_EDC3	GDDR_EDC_PHY	GDDR_D_1_EDC	FB_D1_EDC<3>	NO_TEST=TRUE	85 89
Data Dynamic Bus Inv					
1728 GDDR_D0_DBI0	GDDR_DBI_PHY	GDDR_D_0_DBI	FB_D0_DBI_L<0>	NO_TEST=TRUE	85 89
1729 GDDR_D0_DBI1	GDDR_DBI_PHY	GDDR_D_0_DBI	FB_D0_DBI_L<1>	NO_TEST=TRUE	85 89
1730 GDDR_D0_DBI2	GDDR_DBI_PHY	GDDR_D_0_DBI	FB_D0_DBI_L<2>	NO_TEST=TRUE	85 89
1731 GDDR_D0_DBI3	GDDR_DBI_PHY	GDDR_D_0_DBI	FB_D0_DBI_L<3>	NO_TEST=TRUE	85 89
1732 GDDR_D1_DBI0	GDDR_DBI_PHY	GDDR_D_1_DBI	FB_D1_DBI_L<0>	NO_TEST=TRUE	85 89
1733 GDDR_D1_DBI1	GDDR_DBI_PHY	GDDR_D_1_DBI	FB_D1_DBI_L<1>	NO_TEST=TRUE	85 89
1734 GDDR_D1_DBI2	GDDR_DBI_PHY	GDDR_D_1_DBI	FB_D1_DBI_L<2>	NO_TEST=TRUE	85 89
1735 GDDR_D1_DBI3	GDDR_DBI_PHY	GDDR_D_1_DBI	FB_D1_DBI_L<3>	NO_TEST=TRUE	85 89
Forwarded Clock					
1736 GDDR_D0_WCK0	GDDR_WCK_PHY	GDDR_D_0_WCK	FB_D0_WCLK_P<0>	NO_TEST=TRUE	85 89
1737 GDDR_D0_WCK0	GDDR_WCK_PHY	GDDR_D_0_WCK	FB_D0_WCLK_N<0>	NO_TEST=TRUE	85 89
1738 GDDR_D0_WCK1	GDDR_WCK_PHY	GDDR_D_0_WCK	FB_D0_WCLK_P<1>	NO_TEST=TRUE	85 89
1739 GDDR_D0_WCK1	GDDR_WCK_PHY	GDDR_D_0_WCK	FB_D0_WCLK_N<1>	NO_TEST=TRUE	85 89
1740 GDDR_D1_WCK0	GDDR_WCK_PHY	GDDR_D_1_WCK	FB_D1_WCLK_P<0>	NO_TEST=TRUE	85 89
1741 GDDR_D1_WCK0	GDDR_WCK_PHY	GDDR_D_1_WCK	FB_D1_WCLK_N<0>	NO_TEST=TRUE	85 89
1743 GDDR_D1_WCK1	GDDR_WCK_PHY	GDDR_D_1_WCK	FB_D1_WCLK_P<1>	NO_TEST=TRUE	85 89
1744 GDDR_D1_WCK1	GDDR_WCK_PHY	GDDR_D_1_WCK	FB_D1_WCLK_N<1>	NO_TEST=TRUE	85 89

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GDDR5 FB C/D CONSTRAINTS

Apple Inc.

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Backlight Controller

BLC-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
BLC_P6MM	*	Y	0.600 MM	0.100 MM	3.0 MM	=STANDARD	=STANDARD
BLC_P3MM	*	Y	0.300 MM	0.100 MM	3.0 MM	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
POWER_BLC	*	BLC_P6MM
POWER_BLC_RET	*	BLC_P3MM
BLC_CTL_PHY	*	BLC_P3MM

BLC-specific Spacing Definitions
BLC High Voltage Output

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BLC_HV_ISO	*	1.00MM	1000

Constraints
BLC High Voltage Output

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
BLC_HV	BLC_HV	*	BLC_CTL_ISO
BLC_HV	*	*	BLC_HV_ISO

BLC Baddies

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PHASE_ISO	*	=8:1_SPACING	2000
PHASE_SW2SW	*	=1:1_SPACING	?
PHASE_SW2PWR	*	=2:1_SPACING	?
PHASE_SW2GND	*	=2:1_SPACING	?

BLC Baddies

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
BLC_PHASE	*	*	PHASE_ISO
BLC_PHASE	BLC_PHASE	*	PHASE_SW2SW
BLC_PHASE	POWER	*	PHASE_SW2PWR
BLC_PHASE	GND	*	PHASE_SW2GND

BLC Control

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BLC_CTL_ISO	*	=3:1_SPACING	?

BLC Control

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
BLC_CTL	*	*	BLC_CTL_ISO

BKLT MISCELLANEOUS

Electrical Contraint Set	Physical	Spacing		
SPI				
J6B6	SMB_PHY	SMB	SMB_PCH_BLC_SCL	50 80
J6B5	SMB_PHY	SMB	SMB_PCH_BLC_SDA	50 80
J6B7	SMB_PHY	SMB	SMB_TCON_BLC_SCL	50 80
J6B1	SMB_PHY	SMB	SMB_TCON_BLC_SDA	50 80
12M REFERENCE CRYSTAL				
J6E2	CLK_XTAL	XTAL	BLC_MCU_XTAL_IN	80
J6E3	CLK_XTAL	XTAL	BLC_MCU_XTAL_OUT	80
J6E4	CLK_XTAL	XTAL	BLC_MCU_XTAL_OUT_R	80
250K REFERENCE CLOCKS				
J6B8	CLK_PCH_50S	CLK_PCH	STRCLK_R1	80 81
J6B9	CLK_PCH_50S	CLK_PCH	LED_DRVR_CLK	81

Input Bus	Physical	Spacing	Voltage	DIDT	NO_TEST		
J7A6	POWER_PHY	POWER	12V			PP12V_S0_BLC_VIN2	80 81 82
J7A7	POWER_PHY	POWER	12V			PP12V_S0_BLC_VINP	80 82
J6B6	POWER_PHY	POWER	14V			PRE_REG_OUT	80 81
J6B7	POWER_PHY	POWER	3.3V			BLC_P3V3S	80 82
J6B7	POWER_PHY	POWER	3.3V			BLC_P3V3_REF	80 82
J6B8	POWER_PHY	POWER	3.3V			BLC_P3V3	
J6E2	POWER_PHY	POWER	3.3V			PP3V3_S0_BLC_R	80
J6H1	POWER_PHY	POWER	8V			SPTX_VIN	81
J6H2	POWER_PHY	POWER	8V			PP8V_BLC	80 81
J6H7	POWER_PHY	POWER	8V			BLC_VIN2	81 82
J6J2	POWER_PHY	POWER	14V			BOOST_FET_DRAIN	80
J6J3	POWER_PHY	POWER	12V			BOOST_VDD	80
J6J5	POWER_PHY	POWER	5V			PP5V_S0_BLC_R	80 81 82
J6J6	POWER_PHY	POWER	12V			PP12V_S0_BLC_F	82
Local Ground							
J7A5	BLC_CTL_PHY	BLC_PHASE	0V			BLC_GND_1	81 82
J6B4	BLC_CTL_PHY	BLC_PHASE	0V			BLC_GND_2	81 82
J6D5	BLC_CTL_PHY	BLC_PHASE	0V			BLC_GND_3	81 82
J6J1	GND_PHY	GND	0V			AGND_BLC	81 82
Backlight							
J7D5	BLC_CTL_PHY	BLC_PHASE				LED_DRIVER_GATE1	81
J7D6	BLC_CTL_PHY	BLC_PHASE				LED_DRIVER_GATE1_R	81
J7D8	BLC_CTL_PHY	BLC_PHASE				LED_DRIVER_GATE2	81
J7D7	BLC_CTL_PHY	BLC_PHASE				LED_DRIVER_GATE2_R	81
J6B6	BLC_CTL_PHY	BLC_PHASE				LED_DRIVER_GATE3	81
J7D9	BLC_CTL_PHY	BLC_PHASE				LED_DRIVER_GATE3_R	81
J7D3	BLC_CTL_PHY	BLC_CTL				LED_DRVR_CS_RC_1	81
J7D4	BLC_CTL_PHY	BLC_CTL				LED_DRVR_CS_RC_2	81
J7D6	BLC_CTL_PHY	BLC_CTL				LED_DRVR_CS_RC_3	81
J6D1	BLC_CTL_PHY	BLC_CTL				LED_DRIVER_CS1	81
J6D2	BLC_CTL_PHY	BLC_CTL				LED_DRIVER_CS2	81
J6D3	BLC_CTL_PHY	BLC_CTL				LED_DRIVER_CS3	81
J6F8	BLC_CTL_PHY	BLC_CTL				LED_DRVR_CS_C1	81
J6F7	BLC_CTL_PHY	BLC_CTL				LED_DRVR_CS_C2	81
J6F6	BLC_CTL_PHY	BLC_CTL				LED_DRVR_CS_C3	81
J6J9	BLC_CTL_PHY	BLC_HV	80V			LED_DRIVER_FDBK_R_1	81
J6J8	BLC_CTL_PHY	BLC_HV	80V			LED_DRIVER_FDBK_R_2	81
J6H1	BLC_CTL_PHY	BLC_HV	80V			LED_DRIVER_FDBK_R_3	81
J6H8	BLC_CTL_PHY	BLC_CTL	80V			LED_DRIVER_FDBK1	81
J6J4	BLC_CTL_PHY	BLC_CTL	80V			LED_DRIVER_FDBK2	81
J6J9	BLC_CTL_PHY	BLC_CTL	80V			LED_DRIVER_FDBK3	81
J6J3	BLC_CTL_PHY	BLC_CTL				BLC_PWM_1_R	80 81
J6H3	BLC_CTL_PHY	BLC_CTL				BLC_PWM_2_R	80 81
J6H7	BLC_CTL_PHY	BLC_CTL				BLC_PWM_3_R	80 81
J6H9	BLC_CTL_PHY	BLC_CTL				BLC_PWM_1	81 82
J6H5	BLC_CTL_PHY	BLC_CTL				BLC_PWM_2	81 82
J6H6	BLC_CTL_PHY	BLC_CTL				BLC_PWM_3	81 82
J6J8	BLC_CTL_PHY	BLC_CTL				LED_DRIVER_REF1	81 82
J6H4	BLC_CTL_PHY	BLC_CTL				LED_DRIVER_REF2	81 82
J6H2	BLC_CTL_PHY	BLC_CTL				LED_DRIVER_REF3	81 82
J7A9	BLC_CTL_PHY	BLC_CTL				LED_DRIVER_COMP1	81
J6A9	BLC_CTL_PHY	BLC_CTL				LED_DRIVER_COMP2	81
J6A8	BLC_CTL_PHY	BLC_CTL				LED_DRIVER_COMP3	81
J7A1	BLC_CTL_PHY	BLC_CTL				BCOMP1	81
J6B2	BLC_CTL_PHY	BLC_CTL				BCOMP2	81
J6B3	BLC_CTL_PHY	BLC_CTL				BCOMP3	81
J6F9	BLC_CTL_PHY	BLC_CTL				LED_DRIVER_FLT1	81
J6H9	BLC_CTL_PHY	BLC_CTL				LED_DRIVER_FLT2	81
J6H8	BLC_CTL_PHY	BLC_CTL				LED_DRIVER_FLT3	81
J6H9	BLC_CTL_PHY	BLC_CTL				LED_FLT_R_1	81
J6J1	BLC_CTL_PHY	BLC_CTL				LED_FLT_R_2	81
J6H7	BLC_CTL_PHY	BLC_CTL				LED_FLT_R_3	81
J6H5	BLC_CTL_PHY	BLC_CTL				PRE_REG_OUT_R	80
J6J5	BLC_CTL_PHY	BLC_CTL				BOOST_FB	80
J6J4	BLC_CTL_PHY	BLC_CTL				BOOST_COMP	80
J6J7	BLC_CTL_PHY	BLC_CTL				BOOST_COMP_C	80
J6H6	BLC_CTL_PHY	BLC_CTL			TRUE	BOOST_GDRV	80
J6H3	BLC_CTL_PHY	BLC_CTL			TRUE	BOOST_GDRV_R	80
J6J9	BLC_CTL_PHY	BLC_CTL				BOOST_ISNS	80
J6J8	BLC_CTL_PHY	BLC_CTL				BOOST_ISNS_R	80
J7A4	BLC_CTL_PHY	BLC_HV	80V			LED_DRVR_DRAIN_1	81
J7A3	BLC_CTL_PHY	BLC_HV	80V			LED_DRVR_DRAIN_2	81
J7A2	BLC_CTL_PHY	BLC_HV	80V			LED_DRVR_DRAIN_3	81
OUTPUT BUS							
J7B9	POWER_BLC_RET	BLC_HV	80V			IS1_BLC_F	82
J7B8	POWER_BLC_RET	BLC_HV	80V			IS2_BLC_F	82
J7B6	POWER_BLC_RET	BLC_HV	80V			IS3_BLC_F	82
J7B4	POWER_BLC_RET	BLC_HV	80V			IS1_BLC	81 82
J7B3	POWER_BLC_RET	BLC_HV	80V			IS2_BLC	81 82
J7B2	POWER_BLC_RET	BLC_HV	80V			IS3_BLC	81 82
J7B5	POWER_BLC_RET	BLC_HV	80V			BLC_LED_P_1	82
J7B7	POWER_BLC_RET	BLC_HV	80V			BLC_LED_N_1	82
J7B1	POWER_BLC_RET	BLC_HV	80V			BLC_LED_P_2	82
J7B0	POWER_BLC_RET	BLC_HV	80V			BLC_LED_N_2	82
J7A0	POWER_BLC_RET	BLC_HV	80V			BLC_LED_P_3	82
J7A8	POWER_BLC_RET	BLC_HV	80V			BLC_LED_N_3	82
J6J2	POWER_BLC	BLC_HV	80V			BLC_VOUT1	81 82
J6J4	POWER_BLC	BLC_HV	80V			BLC_VOUT2	81 82
J6J6	POWER_BLC	BLC_HV	80V			BLC_VOUT3	81 82

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BLC Constraints

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GPU CORE PHASES

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST	
Input Bus						
H100	POWER_PHY	POWER	12V			PP12V_S0_GPUCORE_FLT 96 97 98
H101	POWER_PHY	POWER	5V			PP5V_S0_GPU_VCORE_VCC 96
Local Ground						
H102	GND_PHY	GND	0V			AGND_GPU 96
Phase 1						
H103	POWER_PHY	POWER	12V			REG_LVCC_UB510 97
H104	POWER_PHY	POWER	12V			REG_UVCC_UB510 97
H105	VR_CTL_PHY	VR_CTL				REG_PWM_GPUCORE_1 96 97
H106	VR_CTL_PHY	VR_CTL				VR_GPU_PWM1_R 96
H107	POWER_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_GPUCORE_1 97
H108	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_GPUCORE_1 97
H109	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_GPUCORE_1_RC 97
H110	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_GPUCORE_1 97
H111	VR_CTL_PHY	VR_LGATE	12V	TRUE		REG_LGATE_GPUCORE_1 97
H112	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_SNUBBER_GPUCORE_1 97
H113	POWER_PHY	POWER	0.9V			PPGPUCORE_S0_SENSE_1 97
H114	SNS_DIFF_PHY	SENSE				REG_ISEN_GCORE_1_P 96 97
H115	SNS_DIFF_PHY	SENSE				REG_ISEN_GCORE_1_N 96 97
H116	SNS_DIFF_PHY	SENSE				VR_GPU_ISNS1_R_P 96
H117	SNS_DIFF_PHY	SENSE				VR_GPU_ISNS1_R_N 96
H118		SENSE				VR_GPU_ISNS1_RR_2 96
Phase 2						
H119	POWER_PHY	POWER	12V			REG_LVCC_UB530 97
H120	VR_CTL_PHY	VR_CTL				REG_PWM_GPUCORE_2 96 97
H121	VR_CTL_PHY	VR_CTL				VR_GPU_PWM2_R 96
H122	POWER_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_GPUCORE_2 97
H123	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_GPUCORE_2 97
H124	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_GPUCORE_2_RC 97
H125	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_GPUCORE_2 97
H126	VR_CTL_PHY	VR_LGATE	12V	TRUE		REG_LGATE_GPUCORE_2 97
H127	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_SNUBBER_GPUCORE_2 97
H128	POWER_PHY	POWER	0.9V			PPGPUCORE_S0_SENSE_2 97
H129	SNS_DIFF_PHY	SENSE				REG_ISEN_GCORE_2_P 96 97
H130	SNS_DIFF_PHY	SENSE				REG_ISEN_GCORE_2_N 96 97
H131	SNS_DIFF_PHY	SENSE				VR_GPU_ISNS2_R_P 96
H132	SNS_DIFF_PHY	SENSE				VR_GPU_ISNS2_R_N 96
H133		SENSE				VR_GPU_ISNS2_RR_2 96
Phase 3						
H134	POWER_PHY	POWER	12V			REG_VCC_UB550 97
H135	POWER_PHY	POWER	12V			REG_UVCC_UB550 97
H136	POWER_PHY	POWER	12V			REG_LVCC_UB550 97
H137	VR_CTL_PHY	VR_CTL				REG_PWM_GPUCORE_3 96 97
H138	VR_CTL_PHY	VR_CTL				VR_GPU_PWM3_R 96
H139	POWER_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_GPUCORE_3 97
H140	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_GPUCORE_3 97
H141	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_GPUCORE_3_RC 97
H142	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_GPUCORE_3 97
H143	VR_CTL_PHY	VR_LGATE	12V	TRUE		REG_LGATE_GPUCORE_3 97
H144	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_SNUBBER_GPUCORE_3 97
H145	POWER_PHY	POWER	0.9V			PPGPUCORE_S0_SENSE_3 97
H146	SNS_DIFF_PHY	SENSE				REG_ISEN_GCORE_3_P 96 97
H147	SNS_DIFF_PHY	SENSE				REG_ISEN_GCORE_3_N 96 97
H148	SNS_DIFF_PHY	SENSE				VR_GPU_ISNS3_R_P 96
H149	SNS_DIFF_PHY	SENSE				VR_GPU_ISNS3_R_N 96
H150		SENSE				VR_GPU_ISNS3_RR_2 96
Phase 4						
H151	POWER_PHY	POWER	12V			REG_LVCC_UB650 98
H152	VR_CTL_PHY	VR_CTL				REG_PWM_GPUCORE_4 96 98
H153	VR_CTL_PHY	VR_CTL				VR_GPU_PWM4_R 96
H154	POWER_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_GPUCORE_4 98
H155	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_GPUCORE_4 98
H156	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_GPUCORE_4_RC 98
H157	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_GPUCORE_4 98
H158	VR_CTL_PHY	VR_LGATE	12V	TRUE		REG_LGATE_GPUCORE_4 98
H159	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_SNUBBER_GPUCORE_4 98
H160	POWER_PHY	POWER	0.9V			PPGPUCORE_S0_SENSE_4 98
H161	SNS_DIFF_PHY	SENSE				REG_ISEN_GCORE_4_P 96 98
H162	SNS_DIFF_PHY	SENSE				REG_ISEN_GCORE_4_N 96 98
H163	SNS_DIFF_PHY	SENSE				VR_GPU_ISNS4_R_P 96
H164	SNS_DIFF_PHY	SENSE				VR_GPU_ISNS4_R_N 96
H165		SENSE				VR_GPU_ISNS4_RR_2 96

GPU CORE CONTROLLER

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST	
ISL6334						
H424	VR_CTL_PHY	VR_CTL				VR_GPU_COMP 96
H425	VR_CTL_PHY	VR_CTL				VR_GPU_COMP_R 96
H426	VR_CTL_PHY	VR_CTL				VR_GPU_COMP_RC 96
H427	VR_CTL_PHY	VR_CTL				VR_GPU_FB 96
H428	VR_CTL_PHY	VR_CTL				VR_GPU_FB_R 96
H429	VR_CTL_PHY	VR_CTL				VR_GPU_VDIFF 96
H430	VR_CTL_PHY	VR_CTL				VR_VDF_R1 96
H431	VR_CTL_PHY	VR_CTL				VR_VDF_R2 96
H432	VR_CTL_PHY	VR_CTL				VR_GPU_TCOMP 96
H433	VR_CTL_PHY	VR_CTL				VR_GPU_OFS 96
H434	VR_CTL_PHY	VR_CTL				VR_GPU_FS 96
H435		VR_CTL				VR_GPU_EN_VTT 96
H436		VR_CTL				PM_EN_REG_GPUCORE_S0 64 96
H437		VR_CTL				PM_PGOOD_REG_GPUCORE_S0 5 64 96
H438		VR_CTL				GPU_PSI_L 91 96
H439	VR_CTL_PHY	VR_CTL				VR_GPU_IOUT
H440	VR_CTL_PHY	VR_CTL				VR_GPU_IMON 51 96 115
H441	VR_CTL_PHY	VR_CTL				VR_GPU_FAN 96 115
H442		VR_CTL				VR_GPU_VRDHOT 96
H443		VR_CTL				VR_GPU_EN_PWR
H444	VR_CTL_PHY	VR_CTL				VR_GPU_SS 96
H445	VR_CTL_PHY	VR_CTL				VR_GPU_DAC 96
H446	VR_CTL_PHY	VR_CTL				VR_GPU_REF 96
H447	VR_CTL_PHY	VR_CTL				VR_GPU_TM 96
H448	VR_CTL_PHY	VR_CTL				VR_GPU_IMON 51 96 115
H449	VR_CTL_PHY	VR_CTL				VR_GPU_FAN 96 115
H450	VR_CTL_PHY	VR_CTL				VR_GPU_VRHOT
H451		VR_CTL				GPU_PSI_R
H452		VR_CTL				GPU_PSI_L_R 91
H453	VR_CTL_PHY	VR_CTL				VR_GPU_IMON_R 96
H454	VSNS_GPU_VDD	SNS_DIFF_PHY	SENSE			VSNS_GPU_VDD 93 96
H455	VSNS_GPU_VSS	SNS_DIFF_PHY	SENSE			VSNS_GPU_VSS 93 96
H456	SNS_DIFF_PHY	SENSE				VR_GPU_VSEN 96
H457	SNS_DIFF_PHY	SENSE				VR_GPU_RGND 96
GPU VIDS						
H458		VR_VID				REG_GPUCORE_VID7 91 96
H459		VR_VID				REG_GPUCORE_VID6 91 96
H460		VR_VID				REG_GPUCORE_VID5 91 96
H461		VR_VID				REG_GPUCORE_VID4 91 96
H462		VR_VID				REG_GPUCORE_VID3 91 96
H463		VR_VID				REG_GPUCORE_VID2 91 96
H464		VR_VID				REG_GPUCORE_VID1 91 96
H465		VR_VID				REG_GPUCORE_VID0 96
H466		VR_VID				GPU_VCORE_VID6 91
H467		VR_VID				GPU_VCORE_VID5 91
H468		VR_VID				GPU_VCORE_VID4 91
H469		VR_VID				GPU_VCORE_VID3 91
H470		VR_VID				GPU_VCORE_VID2 91
H471		VR_VID				GPU_VCORE_VID1 91
H472		VR_VID				GPU_VCORE_VID0 91
Output Bus						
H473	POWER_PHY	POWER	0.9V			PPVCORE_S0_GPU 6

GPU FBVDDQ

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST	
Input Bus						
H434	POWER_PHY	POWER	5V			REG_VCC_UB750 99
H435	POWER_PHY	POWER	5V			REG_PVCC_UB750 99
Local Ground						
H436	GND_PHY	GND	0V			AGND_FBVDDQ 99
FBVDDQ						
H437	POWER_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_FBVDDQ 99
H438	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_FBVDDQ 99
H439	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_FBVDDQ_RC 99
H440	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_FBVDDQ 99
H441	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_FBVDDQ_R
H442	VR_CTL_PHY	VR_LGATE	12V	TRUE		REG_LGATE_FBVDDQ 99
H443	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_SNUBBER_FBVDDQ 99
H444		SENSE				VSNS_FBVDDQ 94
H445	SNS_DIFF_PHY	SENSE				VSNS_FBVDDQ_P 94 99
H446	SNS_DIFF_PHY	SENSE				VSNS_FBVDDQ_N 94 99
H447	SNS_DIFF_PHY	SENSE				SNS_FBVDDQ_XW_P 99
H448	SNS_DIFF_PHY	SENSE				SNS_FBVDDQ_XW_N 99
H449		SENSE				FBVDDQ_SENSE_R 94
H450	VR_CTL_PHY	VR_CTL				REG_FBVDDQ_OCSET
H451	VR_CTL_PHY	VR_CTL				REG_FBVDDQ_VO 99
H452		SENSE				REG_FBVDDQ_FB 99
H453		SENSE				REG_FBVDDQ_RTN 99
Output Bus						
H454	POWER_PHY	POWER	1.5V			PP1V5R1V35_S0_GPU_REG 6 99

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GPU VREG CONSTRAINTS

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Caesar IV (Ethernet/SD)

CIV-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
SD_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
ENET_COMP_PHY	*	ENET_50S
ENET_DIFF_PHY	*	ENET_100D
SD_PHY	*	SD_50S

CIV-specific Spacing Definitions
Ethernet

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_DIFF_ISO	*	=6:1_SPACING	?
ENET_DIFF2DIFF	*	=3:1_SPACING	?
ENET_TRANS_ISO	*	1.27 MM	?
COMP_ENET_ISO	*	=4:1_SPACING	?

SD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SD_ISO	*	=3:1_SPACING	?

Constraints
Ethernet

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET	
ENET_DIFF	*	*	ENET_DIFF_ISO	
ENET_DIFF	ENET_DIFF	*	ENET_DIFF2DIFF	
ENET_TRANS	*	*	ENET_TRANS_ISO	2 kV isolation
COMP_ENET	*	*	COMP_ENET_ISO	
ENET_TRANS	ENET_TRANS	*	ENET_DIFF2DIFF	

SD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SD	*	*	SD_ISO

VENI, VIDI, VICI!

Electrical Contraint Set	Physical	Spacing		
Ethernet				
ENET_MDI_NORM	ENET_DIFF_PHY	ENET_DIFF	ENETCONN_MDI_P<3..0>	39 40
ENET_MDI_NORM	ENET_DIFF_PHY	ENET_DIFF	ENETCONN_MDI_N<3..0>	39 40
	ENET_DIFF_PHY	ENET_TRANS	ENETCONN_MDI_T_P<3..0>	40
	ENET_DIFF_PHY	ENET_TRANS	ENETCONN_MDI_T_N<3..0>	40
		ENET_TRANS	ENETCONN_MCT3	40
		ENET_TRANS	ENETCONN_MCT2	40
		ENET_TRANS	ENETCONN_MCT1	40
		ENET_TRANS	ENETCONN_MCT0	40
	ENET_COMP_PHY	COMP_ENET	ENET_RDAC	39
SD				
SD_DATA	SD_PHY	SD	ENET_CR_DATA<7..0> NO_TEST=TRUE	39
	SD_PHY	SD	SDCONN_DATA<7..0>	39 41
	SD_PHY	SD	SDCONN_DATA_R<7..0> NO_TEST=TRUE	41
SD_CMD	SD_PHY	SD	ENET_SD_CMD NO_TEST=TRUE	39
	SD_PHY	SD	SDCONN_CMD NO_TEST=TRUE	39 41
	SD_PHY	SD	SDCONN_CMD_R NO_TEST=TRUE	41
SD_CLK	SD_PHY	SD	ENET_SD_CLK NO_TEST=TRUE	39
	SD_PHY	SD	SDCONN_CLK NO_TEST=TRUE	39 41
	SD_PHY	SD	SDCONN_CLK_R NO_TEST=TRUE	41
	SD_PHY	SD	ENET_MEDIA_SENSE	15 18 39
	SD_PHY	SD	ENET_SD_DETECT_L	39 41
	SD_PHY	SD	SDCONN_WP	39 41
CIV SPI				
	SPI_50S	SPI	ENET_SCLK	39
	SPI_50S	SPI	ENET_MISO	39
	SPI_50S	SPI	ENET_MOSI	39
	SPI_50S	SPI	ENET_CS_L	39

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AUTO-CONSTRAINTS PG 1

4V5_*

	Physical	Spacing	Netname	
I4		PM	4V5_REG_EN	56
I5	POWER_PHY	POWER	4V5_REG_IN	56

ACDC_*

	Spacing	Netname	
I6	PM	ACDC_BURST_EN	48
I7	PM	ACDC_BURST_EN_L	48

ALL_*

	Spacing	Netname	
I8	PM	ALL_SYS_PWRGD	5 47 65

AP_*

	Spacing	Netname	
I9	GENERIC_ISO	AP_CLKREQ_L	15 21
I10	GENERIC_ISO	AP_CLKREQ_L_ISO	15 35
I11	GENERIC_ISO	AP_CLKREQ_Q_L	35
I12	GENERIC_ISO	AP_EVENT_L	35 47 48
I13	GENERIC_ISO	AP_PWR_EN_ISO	15 35
I14	PM	AP_RESET_CONN_L	35
I15	PM	AP_RESET_L	26 35
I16	PM	AP_WAKE_L	35

BLC12V_*

	Spacing	Netname
I17	PM	BLC12V_FAULT
I18	PM	BLC12V_FAULT_L
I19	PM	BLC12V_UVLO
I20	PM	BLC12V_UVLO_OUT
I21	PM	BLC12V_UVLO_REF

BLC_*

	Physical	Spacing	Voltage	Netname	
I22		GENERIC_ISO		BLC_BL	80 82
I23		GENERIC_ISO		BLC_BL_GATE	82
I24		GENERIC_ISO		BLC_BST	80 82
I25		GENERIC_ISO		BLC_BST_R	80
I26		GENERIC_ISO		BLC_BYPASS_GATE	82
I27		GENERIC_ISO		BLC_DIM_MCU	80
I28		PM		BLC_EN	78 80 81
I29		GENERIC_ISO		BLC_ENA	80
I30		GENERIC_ISO		BLC_ENA1	80 82
I31		PM		BLC_EN_DELAY	78
I32		PM		BLC_EN_R	80

BLC_*

	Physical	Spacing	Voltage	Netname	
I33		PM		BLC_EXT_BOOT	48 80
I34		PM		BLC_EXT_BOOT_L	80
I35	BLC_CTL_PHY	BLC_CTL	5V	BLC_MCU_AOUT_R	82
I36		GENERIC_ISO		BLC_MCU_BV	80 82
I37		GENERIC_ISO		BLC_MCU_BV_D	82
I38		GENERIC_ISO		BLC_MCU_BV_R	82
I39	SMB_PHY	SMB		BLC_MCU_B_SDA_CONN	80
I40		GENERIC_ISO		BLC_MCU_FLAG_V	80
I41		GENERIC_ISO		BLC_MCU_PWM5	80
I42		GENERIC_ISO		BLC_MCU_PWM5_R	80
I43		PM		BLC_MCU_RESET	80
I44		PM		BLC_MCU_RESET_L	80
I45		PM		BLC_MCU_RESET_R_L	80
I46	XDP_PHY	CLK_JTAG		BLC_MCU_RTCK	80
I47		GENERIC_ISO		BLC_MCU_RXD0	80
I48	XDP_PHY	XDP		BLC_MCU_TCK	80
I49	XDP_PHY	XDP		BLC_MCU_TDI	80
I50	XDP_PHY	XDP		BLC_MCU_TDO	80
I51	XDP_PHY	XDP		BLC_MCU_TMS	80
I52	XDP_PHY	XDP		BLC_MCU_TRST	80
I53	XDP_PHY	XDP		BLC_MCU_TXD0	80
I54		GENERIC_ISO		BLC_MCU_UVLO	80
I55		GENERIC_ISO		BLC_ON	82
I56		GENERIC_ISO		BLC_ON_DRAIN	82
I57		GENERIC_ISO		BLC_ON_R	82
I58		GENERIC_ISO		BLC_P_ON	80 81 82
I59		GENERIC_ISO		BLC_P_ON_BYPASS	82
I60		GENERIC_ISO		BLC_P_ON_D	82
I61		GENERIC_ISO		BLC_P_ON_DRAIN	82
I62		GENERIC_ISO		BLC_P_ON_D_R	82
I63		GENERIC_ISO		BLC_P_ON_GATE	82
I64		GENERIC_ISO		BLC_P_ON_R	82
I65		GENERIC_ISO		BLC_SKIP	81
I66		GENERIC_ISO		BLC_SNUB_1	81
I67		GENERIC_ISO		BLC_SNUB_2	81
I68		GENERIC_ISO		BLC_SNUB_3	81
I69		GENERIC_ISO		BLC_UVLO	80 82
I70		GENERIC_ISO		BLC_VIN2_GATE	82
I71		GENERIC_ISO		BLC_VIN2_SRC	82
I72		GENERIC_ISO		BLC_VINP_GATE	82
I73		GENERIC_ISO		BLC_VIN_SNS	81
I74		GENERIC_ISO		BLC_VSYNC	78 80
I75		GENERIC_ISO		BLC_VSYNC_R	80

BOOST_*

	Spacing	Netname	
I76	GENERIC_ISO	BOOST_BP	80
I77	GENERIC_ISO	BOOST_BYPASS	80 82
I78	GENERIC_ISO	BOOST_BYPASS_GATE	80
I79	PM	BOOST_EN_GATE	80
I80	PM	BOOST_EN_L	80
I81	GENERIC_ISO	BOOST_RC	80
I82	GENERIC_ISO	BOOST_SS	80

BT_*

	Spacing	Netname	
I83	PM	BT_PWR_EN	35
I84	PM	BT_PWR_RST_L	15 20 35
I85	PM	BT_PWR_RST_L_Q	35

BURSTMODE_*

	Spacing	Netname	
I86	PM	BURSTMODE_EN	71
I87	PM	BURSTMODE_EN_L	6 48 71

CAM_*

	Spacing	Netname	
I88	PM	CAM_EXT_BOOT	42 43
I89	PM	CAM_PROC_RESET	43
I90	PM	CAM_PROC_RESET_L	42 43

CPU_*

	Physical	Spacing	Netname	
I91		PM	CPU_PWRGD_1V05_R	28
I92		PM	CPU_PWRGD_3V3	28
I93		PM	CPU_PWRGD_3V3_R	28
I94		GENERIC_ISO	CPU_SKTOCC	64
I95	CPU_PHY	CPU	CPU_THRMTRIP_3V3	47 48
I96	CPU_PHY	CPU	CPU_THRMTRIP_R_L	48

DEBUG_*

	Spacing	Netname	
I97	PM	DEBUG_RESET_L	26 49

DP_*

	Physical	Spacing	Netname	
I98		PM	DP_AUXIO_EN	15 77 79
I99		PM	DP_GPU_MUX_EN	75
I100		GENERIC_ISO	DP_INTPNL_HPD	75 78
I101		GENERIC_ISO	DP_INT_EG_HPD	75 90
I102	TBT_GEN_55S	TBT_GEN	DP_TBTPA_DDC_CLK	76 77
I103	TBT_GEN_55S	TBT_GEN	DP_TBTPA_DDC_DATA	76 77
I104		GENERIC_ISO	DP_TBTPA_HPD	36 77
I105	TBT_GEN_55S	TBT_GEN	DP_TBTPB_DDC_CLK	76 79
I106	TBT_GEN_55S	TBT_GEN	DP_TBTPB_DDC_DATA	76 79
I107		GENERIC_ISO	DP_TBTPB_HPD	36 79

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ENETCONN_*

	Spacing	Netname	
I1	GENERIC_ISO	ENETCONN_TCT	40

ENET_*

	Physical	Spacing	Netname	
I2		GENERIC_ISO	ENET_ACT	40
I3		GENERIC_ISO	ENET_ASF_GPIO	47 48
I4		GENERIC_ISO	ENET_CLKREQ_L	15 18 40
I5		PM	ENET_CLKREQ_L_Q	39 40
I6		PM	ENET_CR_1V8_EN	
I7		PM	ENET_CR_1V8_EN_R	
I8		PM	ENET_CR_3V3_EN_L	
I9		PM	ENET_CR_3V3_EN_L_R	
I10		PM	ENET_CR_PWREN	39 41
I11	XDP_PHY	XDP	ENET_LOW_PWR	26 39 41
I12		PM	ENET_PWR_EN_L	40
I13		PM	ENET_PWR_EN_L_R	40
I14		PM	ENET_RESET_L	39 41
I15		PM	ENET_SD_RESET_L	26 41
I16		GENERIC_ISO	ENET_SR_DISABLE	39
I17		GENERIC_ISO	ENET_SR_LX	39 40
I18		PM	ENET_WAKE_L	40

FAN_*

	Spacing	Netname	
I19	GENERIC_ISO	FAN_0_PWM_FET	54
I20	GENERIC_ISO	FAN_0_PWM_FILT	54
I21	GENERIC_ISO	FAN_0_TACH_FET	54
I22	GENERIC_ISO	FAN_0_TACH_FILT	54

FBVDD_*

	Spacing	Netname	
I23	GENERIC_ISO	FBVDD_ALTVO	91 99

FB_*

	Spacing	Netname	
I24	GENERIC_ISO	FB_A0_VREFC	86
I25	GENERIC_ISO	FB_A0_VREFD	86
I26	GENERIC_ISO	FB_A1_VREFC	86
I27	GENERIC_ISO	FB_A1_VREFD	86
I28	GENERIC_ISO	FB_B0_VREFC	87
I29	GENERIC_ISO	FB_B0_VREFD	87
I30	GENERIC_ISO	FB_B1_VREFC	87
I31	GENERIC_ISO	FB_B1_VREFD	87
I32	GENERIC_ISO	FB_C0_VREFC	88
I33	GENERIC_ISO	FB_C0_VREFD	88
I34	GENERIC_ISO	FB_C1_VREFC	88
I35	GENERIC_ISO	FB_C1_VREFD	88
I36	GENERIC_ISO	FB_D0_VREFC	89
I37	GENERIC_ISO	FB_D0_VREFD	89
I38	GENERIC_ISO	FB_D1_VREFC	89
I39	GENERIC_ISO	FB_D1_VREFD	89
I40	GENERIC_ISO	FB_SW_LEG_A	84 86

FB_*

	Spacing	Netname	
I41	GENERIC_ISO	FB_SW_LEG_B	84 87
I42	GENERIC_ISO	FB_SW_LEG_C	85 88
I43	GENERIC_ISO	FB_SW_LEG_D	85 89
I44	GENERIC_ISO	FB_VREF_GPU	94

FET_*

	Physical	Spacing	Voltage	Netname	
I45		GENERIC_ISO		FET_EN_P12V_S0	74
I46		GENERIC_ISO		FET_EN_P12V_S0_BLC	74
I47		GENERIC_ISO		FET_EN_P12V_S0_BLC_R	74
I48		GENERIC_ISO		FET_EN_P12V_S0_R	74
I49		GENERIC_ISO		FET_EN_P12V_S5	74
I50		GENERIC_ISO		FET_EN_P12V_S5_R	74
I51		GENERIC_ISO		FET_EN_VDDQ_S0	74
I52		GENERIC_ISO		FET_HDD_SLGSW	52
I53	POWER_PHY	POWER	12V	FET_VCC_U7950	74
I54	POWER_PHY	POWER	12V	FET_VCC_U7970	74
I55	POWER_PHY	POWER	12V	FET_VCC_U7980	74

FLAG_*

	Spacing	Netname	
I56	GENERIC_ISO	FLAG_V	80 81 82

G3_*

	Spacing	Netname	
I57	GENERIC_ISO	G3_POWERON_L	47 48

GND_*

	Spacing	Netname	
I58	SENSE	GND_SMC_AVSS	47 48 51 55

GPU_*

	Physical	Spacing	Netname	
I59		GENERIC_ISO	GPU_ALT_VREF	84 85 91
I60		GENERIC_ISO	GPU_BUFRSTN	91
I61		GENERIC_ISO	GPU_IFPAB_PLLVDD	90
I62		GENERIC_ISO	GPU_IFPA_IOVDD	90
I63		GENERIC_ISO	GPU_IFPB_IOVDD	90
I64		GENERIC_ISO	GPU_IFPC_IOVDD	90
I65		GENERIC_ISO	GPU_IFPC_PLLVDD	90
I66	XDP_PHY	XDP	GPU_JTAG_TDI	91
I67	XDP_PHY	XDP	GPU_JTAG_TDO	91
I68	XDP_PHY	XDP	GPU_JTAG_TMS	91
I69	XDP_PHY	XDP	GPU_JTAG_TRST_L	91
I70		GENERIC_ISO	GPU_MLS_STRAP0	91
I71		GENERIC_ISO	GPU_MLS_STRAP1	91

GPU_*

	Physical	Spacing	Netname	
I72		GENERIC_ISO	GPU_MLS_STRAP2	91
I73		GENERIC_ISO	GPU_MLS_STRAP3	91
I74		GENERIC_ISO	GPU_MLS_STRAP4	91
I75		GENERIC_ISO	GPU_RESET_L	26 83 91
I76	SPI_50S	SPI	GPU_ROM_CS_L	91
I77	SPI_50S	SPI	GPU_ROM_CS_L_R	91
I78		GENERIC_ISO	GPU_ROM_HOLD_L	91
I79	SPI_50S	SPI	GPU_ROM_SI	91
I80	SPI_50S	SPI	GPU_ROM_SI_R	91
I81	SPI_50S	SPI	GPU_ROM_SO	91
I82	SPI_50S	SPI	GPU_ROM_SO_R	91
I83	SPI_50S	SPI	GPU_ROM_WP_L	91

HDD_*

	Spacing	Netname	
I84	GENERIC_ISO	HDD_12V_S0_GATE	52
I85	GENERIC_ISO	HDD_OOB_1V00_REF	52
I86	PM	HDD_PWR_EN	21 52
I87	GENERIC_ISO	HDD_PWR_EN_L	52
I88	GENERIC_ISO	HDD_PWR_EN_R	52

I2C_*

	Physical	Spacing	Netname	
I89	SMB_PHY	SMB	I2C_TCON_MAS_SCL	50 78
I90	SMB_PHY	SMB	I2C_TCON_MAS_SDA	50 78

IFPD_*

	Spacing	Netname	
I91	GENERIC_ISO	IFPD_RSET	90

IFPEF_*

	Spacing	Netname	
I92	GENERIC_ISO	IFPEF_RSET	90

ISNSA_*

	Electrical	Physical	Spacing	Netname	
I93	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P12VG3H_N	51
I94	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P12VG3H_P	51
I95	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P12VS0_CPU_P1V05_N	55
I96	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P12VS0_CPU_P1V05_P	55
I97	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P12VS0_CPU_VCCSA_N	55
I98	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P12VS0_CPU_VCCSA_P	55
I99	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P12VS0_FBVDDQ_N	51
I100	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P12VS0_FBVDDQ_P	51
I101	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P12VS0_HDD_N	51
I102	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P12VS0_HDD_P	51

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ISNSA_*

	Electrical	Physical	Spacing	Netname	
I41	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P12VS0_P1V05_N	55
I42	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P12VS0_P1V05_P	55
I43	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P1V05S0_PCH_N	51
I44	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P1V05S0_PCH_P	51
I45	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P1V5S0_CPU_MEM_N	51
I46	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P1V5S0_CPU_MEM_P	51
I47	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P3V3S0_SSD_N	51
I48	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P3V3S0_SSD_P	51
I49	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P3V3S4_AP_N	55
I410	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P3V3S4_AP_P	55
I411	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P5VS0_HDD_N	51
I412	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P5VS0_HDD_P	51
I413	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_PVDDQS3_DDR_N	51
I414	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_PVDDQS3_DDR_P	51

ISNS_*

	Physical	Spacing	Netname	
I415	SNS_PHY	SENSE	ISNS_CPUAXG_FB	51
I416	SNS_PHY	SENSE	ISNS_CPUAXG_N	51
I417	SNS_PHY	SENSE	ISNS_CPUAXG_P	51
I418	SNS_PHY	SENSE	ISNS_CPUCORE_FB	51
I419	SNS_PHY	SENSE	ISNS_CPUCORE_N	51
I420	SNS_PHY	SENSE	ISNS_CPUCORE_P	51
I421	SNS_PHY	SENSE	ISNS_GPUCORE_FB	51
I422	SNS_PHY	SENSE	ISNS_GPUCORE_N	51
I423	SNS_PHY	SENSE	ISNS_GPUCORE_P	51
I424	SNS_PHY	SENSE	ISNS_P12VG3H_R	51
I425	SNS_PHY	SENSE	ISNS_P12VS0_CPU_P1V05_R	55
I426	SNS_PHY	SENSE	ISNS_P12VS0_CPU_VCCSA_R	55
I427	SNS_PHY	SENSE	ISNS_P12VS0_FBVDDQ_R	51
I428	SNS_PHY	SENSE	ISNS_P12VS0_HDD_R	51
I429	SNS_PHY	SENSE	ISNS_P12VS0_P1V05_R	55
I430	SNS_PHY	SENSE	ISNS_P1V05S0_PCH_R	51
I431	SNS_PHY	SENSE	ISNS_P1V5S0_CPU_MEM_R	51
I432	SNS_PHY	SENSE	ISNS_P3V3S0_SSD_R	51
I433	SNS_PHY	SENSE	ISNS_P3V3S4_AP_R	55
I434	SNS_PHY	SENSE	ISNS_P5VS0_HDD_R	51
I435	SNS_PHY	SENSE	ISNS_PVDDQS3_DDR_R	51

ISOLATE_*

	Spacing	Netname	
I436	PM	ISOLATE_CPU_MEM_5V	28
I437	PM	ISOLATE_CPU_MEM_5V_L	28

JTAG_*

	Physical	Spacing	Netname	
I438	XDP_PHY	XDP	JTAG_GMUX_TMS	20
I439	XDP_PHY	XDP	JTAG_TBT_TDI	15 21
I440	XDP_PHY	XDP	JTAG_TBT_TDI_ISOL	15 36
I441	XDP_PHY	XDP	JTAG_TBT_TDO	15 21
I442	XDP_PHY	XDP	JTAG_TBT_TDO_ISOL	15 36
I443	XDP_PHY	XDP	JTAG_TBT_TMS	15 18
I444	XDP_PHY	XDP	JTAG_TBT_TMS_ISOL	15 36

LED_*

	Spacing	Netname	
I445	PM	LED_DRIVER_EN	81 82
I446	PM	LED_DRIVER_EN_L	82
I447	PM	LED_DRIVER_EN_L_R	82
I448	GENERIC_ISO	LED_DRIVER_OVP1	81 82
I449	GENERIC_ISO	LED_DRIVER_OVP1P	80 81
I450	GENERIC_ISO	LED_DRIVER_OVP1_OUT	81
I451	GENERIC_ISO	LED_DRIVER_OVP2	81 82
I452	GENERIC_ISO	LED_DRIVER_OVP2P	80 81
I453	GENERIC_ISO	LED_DRIVER_OVP2_OUT	81
I454	GENERIC_ISO	LED_DRIVER_OVP3	81 82
I455	GENERIC_ISO	LED_DRIVER_OVP3P	80 81
I456	GENERIC_ISO	LED_DRIVER_OVP3_OUT	81

LPCPLUS_*

	Spacing	Netname	
I457	GENERIC_ISO	LPCPLUS_GPIO	21 49

LPC_*

	Spacing	Netname	
I458	GENERIC_ISO	LPC_PWRDWN_L	19 26 47 49
I459	GENERIC_ISO	LPC_SERIRQ	18 47 49

MEMVTT_*

	Spacing	Netname	
I460	PM	MEMVTT_EN	28 64
I461	PM	MEMVTT_EN_L	28

MEM_*

	Spacing	Netname	
I462	GENERIC_ISO	MEM_EVENT_L	29 30 31 32 47 48

MOJO_*

	Physical	Spacing	Netname	
I463	XDP_PHY	XDP	MOJO_RX_L	45 47 48
I464	XDP_PHY	XDP	MOJO_TX_L	45 47 48

OCA_*

	Spacing	Netname	
I465	GENERIC_ISO	OCA_FET_DRAIN	82

OVP_*

	Spacing	Netname	
I466	GENERIC_ISO	OVP_OREF	82
I467	GENERIC_ISO	OVP_OUT1	82
I468	GENERIC_ISO	OVP_OUT1_R	82
I469	GENERIC_ISO	OVP_OUT2	82
I470	GENERIC_ISO	OVP_OUT2_R	82
I471	GENERIC_ISO	OVP_OUT3	82
I472	GENERIC_ISO	OVP_OUT3_R	82

P1V2_*

	Spacing	Netname	
I473	PM	P1V2_S4_EN	43

P1V8_*

	Spacing	Netname	
I474	PM	P1V8_S4_EN	43

P3V3AP_*

	Spacing	Netname	
I475	GENERIC_ISO	P3V3AP_VMON	35

P3V3_*

	Spacing	Netname	
I476	GENERIC_ISO	P3V3_S0_EN_G	74
I477	GENERIC_ISO	P3V3_S3_EN_G	74

P3V42G3H_*

	Spacing	Netname	
I478	GENERIC_ISO	P3V42G3H_BOOST	73

P5V_*

	Spacing	Netname	
I479	GENERIC_ISO	P5V_S0_EN_G	74

PCA9557D_*

	Spacing	Netname	
I480	GENERIC_ISO	PCA9557D_RESET_L	26 28 34

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PCH_*

	Physical	Spacing	Netname	
A1		PM	PCH_BLC_EXT_BOOT	21 80
A2		PM	PCH_BLC_EXT_BOOT_R	15 21
A3		PM	PCH_BLC_MCU_RESET	21 80
A4		PM	PCH_BLC_MCU_RESET_R	15 21
A5		PM	PCH_CAM_RESET	15 21
A6		PM	PCH_CAM_RESET_R	21 43
A7		GENERIC_ISO	PCH_DSWVRMEN	19
A8	CPU_PHY	CPU	PCH_PECI	21
A9	CPU_PHY	CPU	PCH_PROCPWRGD	21
A10		GENERIC_ISO	PCH_RCIN_L	21
A11		GENERIC_ISO	PCH_RI_L	19
A12		GENERIC_ISO	PCH_SMBALERT_L	15 18
A13		GENERIC_ISO	PCH_SRTCRST_L	18
A14		GENERIC_ISO	PCH_STRP_TOPBLK_SWP_L	20
A15		GENERIC_ISO	PCH_SUSWARN_L	15 19

PCIE_*

	Spacing	Netname	
A16	GENERIC_ISO	PCIE_CLKREQ5_GPIO44_L	18
A17	PM	PCIE_WAKE_L	19 35 40

PEG_*

	Spacing	Netname	
A18	GENERIC_ISO	PEG_CLKREQ_L	15 18 83

PGOOD_*

	Spacing	Netname	
A19	PM	PGOOD_P1V5_S0_DLY	28

PLT_*

	Spacing	Netname	
A20	PCH	PLT_RESET_L	20 26
A21	PCH	PLT_RST_BUF_L	26

PM_*

	Spacing	Netname	
A22	PM	PM_CLKRUN_L	47 48 49
A23	PM	PM_DSW_PWRGD	47 48 65
A24	PM	PM_EN_FET_P12V_S0	64 74
A25	PM	PM_EN_FET_P12V_S0_R	74
A26	PM	PM_EN_FET_P3V3_S0	64 74
A27	PM	PM_EN_FET_P3V3_S4	64 74
A28	PM	PM_EN_FET_P5V_S0	64 74
A29	PM	PM_EN_FET_VDDQ_S0	64 74
A30	PM	PM_EN_LDO_DDRVTT_S0	64 72
A31	PM	PM_EN_REG_CPUCORE_S0	64 66

PM_*

	Spacing	Netname	
A32	PM	PM_EN_REG_CPU_P1V05_S0	64 69
A33	PM	PM_EN_REG_FBVDDQ_S0	64 99
A34	PM	PM_EN_REG_GPUCORE_S0_R	96
A35	PM	PM_EN_REG_P1V05_S0	64 99
A36	PM	PM_EN_REG_P1V8_S0	64 72
A37	PM	PM_EN_REG_P3V3_S5	64 71 74
A38	PM	PM_EN_REG_P5V_S4	64 71
A39	PM	PM_EN_REG_VCCSA_S0	64 70
A40	PM	PM_EN_REG_VDDQ_S3	64 72
A41	PM	PM_EN_S0	64
A42	PM	PM_EN_S4	64
A43	PM	PM_EN_USB_PWR	45 46 64
A44	PM	PM_LED_A_ALL_SYS_PWRGD	5
A45	PM	PM_LED_A_BLC_GOOD	5
A46	PM	PM_LED_A_CPUAXG_PGOOD	5
A47	PM	PM_LED_A_GPU_GOOD	5
A48	PM	PM_LED_A_PGOOD_CPUCORE_S0	5
A49	PM	PM_LED_A_PGOOD_CPU_P1V05_S0	5
A50	PM	PM_LED_A_PGOOD_REG_FBVDDQ_S0	5
A51	PM	PM_LED_A_PGOOD_REG_GPUCORE_S0	5
A52	PM	PM_LED_A_PGOOD_REG_P1V05	5
A53	PM	PM_LED_A_PGOOD_REG_VDDQ_S3	5
A54	PM	PM_LED_A_S4	5
A55	PM	PM_LED_A_S5	5
A56	PM	PM_LED_A_SLP_S3	5
A57	PM	PM_LED_A_VIDEO_ON	5
A58	PM	PM_LED_K_ALL_SYS_PWRGD	5
A59	PM	PM_LED_K_BLC_GOOD	5
A60	PM	PM_LED_K_CPUAXG_PGOOD	5
A61	PM	PM_LED_K_GPU_GOOD	5
A62	PM	PM_LED_K_PGOOD_CPUCORE_S0	5
A63	PM	PM_LED_K_PGOOD_CPU_P1V05_S0	5
A64	PM	PM_LED_K_PGOOD_REG_FBVDDQ_S0	5
A65	PM	PM_LED_K_PGOOD_REG_GPUCORE_S0	5
A66	PM	PM_LED_K_PGOOD_REG_P1V05	5
A67	PM	PM_LED_K_PGOOD_REG_VDDQ_S3	5
A68	PM	PM_LED_K_SLP_S3	5
A69	PM	PM_MEM_PWRGD_L	28
A70	PM	PM_PCH_APWROK	19 65
A71	PM	PM_PCH_PWROK	15 19 26 35 43 65 80
A72	PM	PM_PCH_PWROK_APWROK	65
A73	PM	PM_PCH_SYS_PWROK	19 48 65
A74	PM	PM_PGOOD_FBVDDQ_VDDQ_S0	64
A75	PM	PM_PGOOD_FET_P12V_S0	74
A76	PM	PM_PGOOD_FET_P12V_S0_BLC	74 82
A77	PM	PM_PGOOD_FET_P12V_S5	74
A78	PM	PM_PGOOD_FET_P3V3_S0	64 74
A79	PM	PM_PGOOD_FET_P5V_S0	64 74
A80	PM	PM_PGOOD_FET_VDDQ_S0	28 64 74
A81	PM	PM_PGOOD_P3V3_S4_FET	27 35 64 74
A82	PM	PM_PGOOD_REG_ALL_P1V05_S0	64 65
A83	PM	PM_PGOOD_REG_ALL_P1V05_S0_R	28 64
A84	PM	PM_PGOOD_REG_CPUCORE_S0	5 25 65 66
A85	PM	PM_PGOOD_REG_CPU_P1V05_S0	5 64 69
A86	PM	PM_PGOOD_REG_FBVDDQ_S0	5 64 99
A87	PM	PM_PGOOD_REG_P1V05_S0	5 64 99
A88	PM	PM_PGOOD_REG_P1V8_S0	64 72
A89	PM	PM_PGOOD_REG_P3V3_S5	65 71
A90	PM	PM_PGOOD_REG_P5V_S4	64 71
A91	PM	PM_PGOOD_REG_VCCSA_S0	64 65 70
A92	PM	PM_PGOOD_REG_VDDQ_S3	5 64 72
A93	PM	PM_PWRBTN_L	15 19 25 47
A94	PM	PM_RSMRST_PCH_L	19 65
A95	PM	PM_RSMRST_PCH_L_R	65
A96	PM	PM_SLP_S3_L	5 15 19 28 40 47 48 64
A97	PM	PM_SLP_S4_L	15 19 47 64
A98	PM	PM_SLP_S5_L	15 19 47 64
A99	PCH	PM_SYSRST_L	19 25 26 47
A100	PCH	PM_THRMTRIP_L	21 48
A114	PM	PGOOD_P12V_S0_R	65
A115	PM	PGOOD_P12V_S0	64 65 74

PP12V_*

	Physical	Spacing	Voltage	Netname	
A101	POWER_PHY	POWER	12V	PP12V_LCD	78
A102	POWER_PHY	POWER	12V	PP12V_LCD_EXT	78
A103	POWER_PHY	POWER	12V	PP12V_S0_FAN_0_FILT	54
A104	POWER_PHY	POWER	12V	PP12V_S0_HDD_FET	44 52

PP1V05_*

	Physical	Spacing	Voltage	Netname	
A105	POWER_PHY	POWER	1.05V	PP1V05_S0_PCH_VCCADPLLA_F	17 22
A106	POWER_PHY	POWER	1.05V	PP1V05_S0_PCH_VCCADPLLB_F	17 22

PP1V2_*

	Physical	Spacing	Voltage	Netname	
A107	POWER_PHY	POWER	1.2V	PP1V2_ENET_INTREG	40
A108	POWER_PHY	POWER	1.2V	PP1V2_G3H_SMC_VDDC	47
A109	POWER_PHY	POWER	1.2V	PP1V2_S4_ENET_PHY_AVDDL	39
A110	POWER_PHY	POWER	1.2V	PP1V2_S4_ENET_PHY_GPHYPLL	39
A111	POWER_PHY	POWER	1.2V	PP1V2_S4_ENET_PHY_PCIEPLL	39
A112	POWER_PHY	POWER	1.2V	PP1V2_USB_HUB_CRFILT	27
A113	POWER_PHY	POWER	1.2V	PP1V2_USB_HUB_PLLFILT	27

PP1V5_*

	Physical	Spacing	Voltage	Netname	
A116	POWER_PHY	POWER	1.5V	PP1V5_S0_DP_BIAS	75

PP1V8_*

	Physical	Spacing	Voltage	Netname	
A117	POWER_PHY	POWER	1.8V	PP1V8_S0_PCH_VCCVRM_F	22 24

PP3V3R1V8_*

	Physical	Spacing	Netname	
A118	POWER_PHY	POWER	PP3V3R1V8_ENET_LR_OUT_REG	39

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PP3V3RHV_*

	Physical	Spacing	Voltage	Netname	
I34	POWER_PHY	POWER	12V	PP3V3RHV_SW_TBTAPWR	77
I35	POWER_PHY	POWER	12V	PP3V3RHV_SW_TBTBPWR	79

PP3V3_*

	Physical	Spacing	Voltage	Netname	
I3	POWER_PHY	POWER	3.3V	PP3V3_DMIC_CONN	42
I4	POWER_PHY	POWER	3.3V	PP3V3_G3H_AVREF_SMC	47 48
I5	POWER_PHY	POWER	3.3V	PP3V3_G3H_BT_FET	35
I6	POWER_PHY	POWER	3.3V	PP3V3_G3H_BT_FLT	35
I7	POWER_PHY	POWER	3.3V	PP3V3_G3H_SMC_USBMUX_R	45
I8	POWER_PHY	POWER	3.3V	PP3V3_G3H_SMC_VDDA	47
I9	POWER_PHY	POWER	3.3V	PP3V3_G3_RTC	6 26
I10	POWER_PHY	POWER	3.3V	PP3V3_PVDDQS3_ISNS	51
I11	POWER_PHY	POWER	3.3V	PP3V3_S0_PCH_VCCA_DAC_F	17 22
I12	POWER_PHY	POWER	3.3V	PP3V3_S0_SSD_FLT	44
I13	POWER_PHY	POWER	3.3V	PP3V3_S0_SW_SD_PWR	41
I14	POWER_PHY	POWER	3.3V	PP3V3_S4_ALS_F	42
I15	POWER_PHY	POWER	3.3V	PP3V3_S4_AP_FET	35
I16	POWER_PHY	POWER	3.3V	PP3V3_S4_AP_FLT	35
I17	POWER_PHY	POWER	3.3V	PP3V3_S4_ENET_FET_AVDDH	39
I18	POWER_PHY	POWER	3.3V	PP3V3_S4_ENET_FET_BIASVDDH	39
I19	POWER_PHY	POWER	3.3V	PP3V3_S4_ENET_FET_SRVDD	39
I20	POWER_PHY	POWER	3.3V	PP3V3_S4_ENET_FET_XTALVDDH	39
I21	POWER_PHY	POWER	3.3V	PP3V3_S4_USB_HUB_VDD	27
I22	POWER_PHY	POWER	3.3V	PP3V3_S5_XDP_R	25

PP4V5_*

	Physical	Spacing	Voltage	Netname	
I23	POWER_PHY	POWER	4.5V	PP4V5_AUDIO_ANALOG	56 60 62

PP5V_*

	Physical	Spacing	Voltage	Netname	
I24	POWER_PHY	POWER	5V	PP5V_AUDIO_HPAMP	56 57
I25	POWER_PHY	POWER	5V	PP5V_S0_HDD_FET	44 52
I26	POWER_PHY	POWER	5V	PP5V_S0_PCH_V5REF	24
I27	POWER_PHY	POWER	5V	PP5V_S4_EXTA	45
I28	POWER_PHY	POWER	5V	PP5V_S4_EXTA_F	45
I29	POWER_PHY	POWER	5V	PP5V_S4_EXTB	45
I30	POWER_PHY	POWER	5V	PP5V_S4_EXTB_F	45
I31	POWER_PHY	POWER	5V	PP5V_S4_EXTC	46
I32	POWER_PHY	POWER	5V	PP5V_S4_EXTC_F	46
I33	POWER_PHY	POWER	5V	PP5V_S4_EXTD	46
I34	POWER_PHY	POWER	5V	PP5V_S4_EXTD_F	46
I35	POWER_PHY	POWER	5V	PP5V_S5_PCH_V5REFSUS	24

PPHV_*

	Physical	Spacing	Voltage	Netname	
I36	POWER_PHY	POWER	12V	PPHV_SW_TBTAPWR	77
I37	POWER_PHY	POWER	12V	PPHV_SW_TBTBPWR	79

PPVBATT_*

	Physical	Spacing	Voltage	Netname	
I38	POWER_PHY	POWER	3.3V	PPVBATT_G3_RTC	26
I39	POWER_PHY	POWER	3.3V	PPVBATT_G3_RTC_R	26

PU_*

	Spacing	Netname	
I40	GENERIC_ISO	PU_U6900	64

PWR_*

	Spacing	Netname	
I41	PM	PWR_BTN	6 48
I42	PM	PWR_BTN_R	6

REG_*

	Physical	Spacing	Netname	
I43		PM	REG_CPUAXG_PGOOD	5 66
I44		PM	REG_CPUCORE_PGOOD	66
I45	CPU_PHY	CPU	REG_CPUCORE_VRHOT_L	66
I46		PM	REG_CPU_P1V05S0_PGOOD	69
I47	VR_CTL_PHY	VR_CTL	REG_FBVDDQ_SET0	99
I48	VR_CTL_PHY	VR_CTL	REG_FBVDDQ_SET1	99
I49	VR_CTL_PHY	VR_CTL	REG_FBVDDQ_SET1_R	99
I50	VR_CTL_PHY	VR_CTL	REG_FBVDDQ_SREF	99
I51		PM	REG_P1V8S0_PGOOD	72
I52		PM	REG_P3V3S5_PGOOD	71
I53		PM	REG_P5VS4_PGOOD	71
I54		PM	REG_VCCSAS0_PGOOD	70
I55		PM	REG_VDDQS3_PGOOD	72

RTC_*

	Spacing	Netname	
I56	PM	RTC_RESET_L	18 26 48
I57	PM	RTC_RESET_L_R	48

S5_*

	Spacing	Netname	
I58	PM	S5_PWRGD	47 65

SATALED_*

	Spacing	Netname	
I59	GENERIC_ISO	SATALED_L	44

SDCONN_*

	Spacing	Netname	
I60	GENERIC_ISO	SDCONN_DETECT	41
I61	GENERIC_ISO	SDCONN_ILIM	41
I62	GENERIC_ISO	SDCONN_OC_L	41

SD_*

	Spacing	Netname	
I63	GENERIC_ISO	SD_DETECT_LVL	41

SLG_*

	Spacing	Netname	
I64	PM	SLG_ENET_RESET_L	41
I65	PM	SLG_ENET_RESET_R_L	41

SMBUS_*

	Physical	Spacing	Netname	
I66	SMB_PHY	SMB	SMBUS_PCH_CLK	18 50
I67	SMB_PHY	SMB	SMBUS_PCH_CLK_R	50
I68	SMB_PHY	SMB	SMBUS_PCH_DATA	18 50
I69	SMB_PHY	SMB	SMBUS_PCH_DATA_R	50
I70	SMB_PHY	SMB	SMBUS_SMC_0_S0_SCL	47 50
I71	SMB_PHY	SMB	SMBUS_SMC_0_S0_SDA	47 50
I72	SMB_PHY	SMB	SMBUS_SMC_1_S0_SCL	47 50
I73	SMB_PHY	SMB	SMBUS_SMC_1_S0_SDA	47 50
I74	SMB_PHY	SMB	SMBUS_SMC_2_S4_SCL	47 50
I75	SMB_PHY	SMB	SMBUS_SMC_2_S4_SDA	47 50
I76	SMB_PHY	SMB	SMBUS_SMC_3_SCL	47 50
I77	SMB_PHY	SMB	SMBUS_SMC_3_SDA	47 50
I78	SMB_PHY	SMB	SMBUS_SMC_4_ASF_SCL	47 48 50
I79	SMB_PHY	SMB	SMBUS_SMC_4_ASF_SDA	47 48 50
I80	SMB_PHY	SMB	SMBUS_SMC_5_G3H_SCL	47 48 50
I81	SMB_PHY	SMB	SMBUS_SMC_5_G3H_SDA	47 48 50

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SMCISNS_*

	Physical	Spacing	Netname	
I41	SNS_PHY	SENSE	SMCISNS_CPUAXG	48 51
I42	SNS_PHY	SENSE	SMCISNS_CPUCORE	48 51
I43	SNS_PHY	SENSE	SMCISNS_GPUCORE	48 51
I44	SNS_PHY	SENSE	SMCISNS_P12VG3H	48 51
I45	SNS_PHY	SENSE	SMCISNS_P12VS0_CPU_P1V05	48 55
I46	SNS_PHY	SENSE	SMCISNS_P12VS0_CPU_VCCSA	48 55
I47	SNS_PHY	SENSE	SMCISNS_P12VS0_FBVDDQ	48 51
I48	SNS_PHY	SENSE	SMCISNS_P12VS0_HDD	48 51
I49	SNS_PHY	SENSE	SMCISNS_P12VS0_P1V05	48 55
I4A	SNS_PHY	SENSE	SMCISNS_P1V05S0_PCH	48 51
I4B	SNS_PHY	SENSE	SMCISNS_P1V5S0_CPU_MEM	48 51
I4C	SNS_PHY	SENSE	SMCISNS_P3V3S0_SSD	48 51
I4D	SNS_PHY	SENSE	SMCISNS_P3V3S4_AP	48 55
I4E	SNS_PHY	SENSE	SMCISNS_P5VS0_HDD	48 51
I4F	SNS_PHY	SENSE	SMCISNS_PVDDQS3_DDR	48 51

SMCVSNS_*

	Physical	Spacing	Netname	
I50	SNS_PHY	SENSE	SMCVSNS_CPUAXG	48 51
I51	SNS_PHY	SENSE	SMCVSNS_CPUCORE	48 51
I52	SNS_PHY	SENSE	SMCVSNS_GPUCORE	48 51
I53	SNS_PHY	SENSE	SMCVSNS_P12VG3H	48 51
I54	SNS_PHY	SENSE	SMCVSNS_P1V05S0_PCH	48 51
I55	SNS_PHY	SENSE	SMCVSNS_P1V5S0_CPU_MEM	48 51
I56	SNS_PHY	SENSE	SMCVSNS_P3V3S0	48 51
I57	SNS_PHY	SENSE	SMCVSNS_P5VS0_HDD	48 51
I58	SNS_PHY	SENSE	SMCVSNS_PVDDQS3_DDR	48 51

SMC_*

	Physical	Spacing	Netname	
I59		GENERIC_ISO	SMC_ACDC_ID	6 48
I5A		GENERIC_ISO	SMC_ACDC_ID_R	6
I5B		PM	SMC_ASSERT_RTCRST	48
I5C		GENERIC_ISO	SMC_BLC_MUX_RX_L	48 80
I5D		GENERIC_ISO	SMC_BLC_MUX_TX_L	48 80
I5E		GENERIC_ISO	SMC_CPU_CATERR_L	47 48
I5F	CPU_PHY	CPU	SMC_CPU_PECI	48
I60		PM	SMC_DELAYED_PWRGD	38 47 48 65
I61		GENERIC_ISO	SMC_DP_HPD_L	47 48
I62	CLK_XTAL	XTAL	SMC_EXTAL	47 48
I63		GENERIC_ISO	SMC_FAN_0_CTL	47 54
I64		GENERIC_ISO	SMC_FAN_0_TACH	47 54
I65		GENERIC_ISO	SMC_GFX_OVERTEMP	47 48 91
I66		GENERIC_ISO	SMC_GFX_OVERTEMP_Q	91
I67		GENERIC_ISO	SMC_GFX_OVERTEMP_R_L	91
I68		PM	SMC_GFX_THROTTLE_L	47 91
I69		PM	SMC_GFX_THROTTLE_R_L	91
I6A		PM	SMC_LRESET_L	26 47
I6B		PM	SMC_MANUAL_RST_L	48
I6C		PM	SMC_ONOFF_L	47 48
I6D		SENSE	SMC_OOB1_RX_CN	44
I6E		SENSE	SMC_OOB1_RX_FILT	44 52
I6F		SENSE	SMC_OOB1_RX_L	47 52
I70		SENSE	SMC_OOB1_RX_R	52
I71		SENSE	SMC_OOB1_TX_L	47 48
I72		SENSE	SMC_OOB2_RX_L	44 48
I73		SENSE	SMC_OOB2_TX_L	44 48
I74	CPU_PHY	CPU	SMC_PECI_L	47 48
I75	CPU_PHY	CPU	SMC_PECI_L_R	48
I76		PM	SMC_PME_S4_WAKE_L	35 47 48
I77		GENERIC_ISO	SMC_PM_G2_EN	47 48 74
I78		PM	SMC_PM_PCH_SYS_PWROK	47 48
I79		CPU	SMC_PROCHOT	47 48
I7A		PM	SMC_RESET_L	47 48 49

SMC_*

	Physical	Spacing	Netname	
I7B		GENERIC_ISO	SMC_ROMBOOT	48 49
I7C		GENERIC_ISO	SMC_RUNTIME_SCI_L	15 21 47
I7D		GENERIC_ISO	SMC_RX_L	47 48 49
I7E		PM	SMC_S4_WAKESRC_EN	35 47 48
I7F		GENERIC_ISO	SMC_TCK	47 48 49
I80		GENERIC_ISO	SMC_TDI	47 48 49
I81		GENERIC_ISO	SMC_TDO	47 48 49
I82		PM	SMC_THRMTRIP	47 48
I83		GENERIC_ISO	SMC_TMS	47 48 49
I84		GENERIC_ISO	SMC_TO_BLC_RX_L	48
I85		GENERIC_ISO	SMC_TO_BLC_TX_L	48
I86		GENERIC_ISO	SMC_TX_L	47 48 49
I87		PM	SMC_WAKE_L	47
I88		GENERIC_ISO	SMC_WAKE_SCI_L	15 21 47
I89	CLK_XTAL	XTAL	SMC_XTAL	47 48
I8A	CLK_XTAL	XTAL	SMC_XTAL_R	48

SML_*

	Physical	Spacing	Netname	
I8B	SMB_PHY	SMB	SML_PCH_0_CLK	18 50
I8C	SMB_PHY	SMB	SML_PCH_0_DATA	18 50
I8D	SMB_PHY	SMB	SML_PCH_1_CLK	18 50
I8E	SMB_PHY	SMB	SML_PCH_1_DATA	18 50

SPI_*

	Spacing	Netname	
I8F	GENERIC_ISO	SPI_DESCRIPTOR_OVERRIDE_L	15 47

SSD_*

	Spacing	Netname	
I90	GENERIC_ISO	SSD_CLKREQ_L	15 18

SYS_*

	Spacing	Netname	
I91	PM	SYS_PWROK_R	65

TBT_*

	Physical	Spacing	Voltage	Netname	
I92		GENERIC_ISO	3.3V	TBT_A_BIAS	77
I93	TBT_GEN_55S	TBT_GEN		TBT_A_CONFIG1_RC	77
I94		PM		TBT_A_HV_EN	36 77
I95		GENERIC_ISO	3.3V	TBT_B_BIAS	79
I96	TBT_GEN_55S	TBT_GEN		TBT_B_CONFIG1_RC	79
I97		PM		TBT_B_HV_EN	36 79
I98		GENERIC_ISO		TBT_CLKREQ_ISOL_L	38
I99		GENERIC_ISO		TBT_CLKREQ_L	15 38
I9A		GENERIC_ISO		TBT_DDC_XBAR_EN_L	36 76
I9B		GENERIC_ISO		TBT_EN_CIO_PWR	38
I9C		PM		TBT_EN_CIO_PWR_L	36 38
I9D		GENERIC_ISO		TBT_EN_LC_ISOL	38
I9E		GENERIC_ISO		TBT_EN_LC_PWR	36 38
I9F		GENERIC_ISO		TBT_PCH_CLKREQ_L	15 21
IA0		PM		TBT_PWR_EN	15 26 36
IA1		PM		TBT_PWR_EN_PCH	18 26
IA2		PM		TBT_PWR_ON_POC_RST_L	36 38
IA3		PM		TBT_PWR_REQ_L	15 20 36
IA4		PM		TBT_S0_EN	64
IA5		PM		TBT_SW_RESET_L	21 38

TSNS_*

	Electrical	Physical	Spacing	Netname	
IA6	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_1_1_N	53
IA7	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_1_1_P	53
IA8	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_1_2_N	53
IA9	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_1_2_P	53
IAA	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_1_3_N	53
IAB	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_1_3_P	53
IAC	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_1_N	53
IAD	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_1_P	53
IAE	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_2_N	53
IAF	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_2_P	53
IB0	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_3_N	53
IB1	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_3_P	53
IB2	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_4_N	53
IB3	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_4_P	53
IB4	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_5_N	53
IB5	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_5_P	53
IB6	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_6_N	53
IB7	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_6_P	53
IB8	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_7_N	53
IB9	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_7_P	53
IBA	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_ACDC_N	6 53
IBB	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_ACDC_P	6 53
IBC	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_SKIN_N	53
IBD	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_SKIN_P	53

UVP_*

	Spacing	Netname	
IBE	PM	UVP_IN_1	82
IBF	PM	UVP_IN_1_REF	82
IC0	PM	UVP_IN_2	82
IC1	PM	UVP_IN_3	82
IC2	PM	UVP_IN_4	82
IC3	PM	UVP_REF	82

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VREFMRGN_*

Spacing	Netname
GENERIC_ISO	VREFMRGN_CA_SODIMMA_EN 34
GENERIC_ISO	VREFMRGN_CA_SODIMMB_EN 34

VTTCLAMP_*

Spacing	Netname
GENERIC_ISO	VTTCLAMP_EN 28
GENERIC_ISO	VTTCLAMP_L 28

WOL_*

Spacing	Netname
GENERIC_ISO	WOL_EN 15 21 40

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