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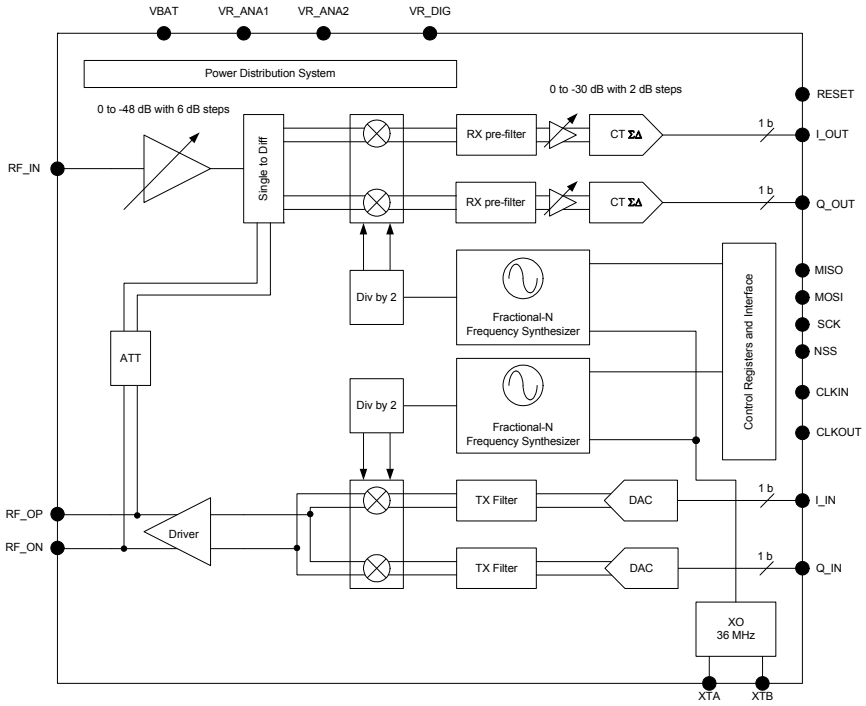
SX1257 RF Front-End Transceiver

Low Power Digital I and Q RF Multi-PHY Mode Transceiver



GENERAL DESCRIPTION

The SX1257 is a highly integrated RF front-end to digital I and Q modulator/demodulator Multi-PHY mode transceiver capable of supporting multiple constant and non-constant envelope modulation schemes. It is designed to operate over the 862 - 960 MHz European, North American and Japanese ISM (Industrial, Scientific and Medical) license-exempt frequency bands. Its highly integrated architecture allows for a minimum of external components whilst maintaining maximum design flexibility. All major RF communication parameters are programmable and most of them can be dynamically set. The SX1257 offers support for both narrow-band and wide-band communication modes without the need to modify external components. The SX1257 is optimized for low power consumption while offering the provision for high RF output power and channelized operation. TrueRF™ technology enables a low-cost external component count whilst still satisfying ETSI, FCC and ARIB regulations.

APPLICATIONS

- IEEE 802.15.4g SUN Multi-PHY Mode Smartgrid
- Cognitive / Software Defined Radio (SDR)

KEY PRODUCT FEATURES

- Fully flexible I and Q modulator and demodulator
- Half or full-duplex operation
- Bullet proof RX LNA
- Analog TX and RX pre-filtering
- Programmable tap TX FIR-DAC filter
- Linear TX amplifier for both constant and non-constant envelope modulation schemes

ORDERING INFORMATION

Part Number	Temperature Range	Qty. per Reel	Package
SX1257IWLTRT	-40;+85 C	3000	MLPQW-32

- Pb-free, Halogen Free
- RoHS / WEEE compliant product

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1. General Description

The SX1257 is a single-chip Zero-IF RF-to-digital front-end transceiver integrated circuit ideally suited for today's high performance multi-PHY mode or SDR ISM band RF applications. The SX1257 has a maximum signal bandwidth of 500 kHz in both transmission and reception and is intended as a high performance, low-cost RF-to-digital converter and provides a generic RF front-end that allows several constant and non-constant envelope modulation schemes to be handled, such as the MR-FSK, MR-OFDM and MR-O-QPSK PHYs of the IEEE 802.15.4g standard for Smart Utility Networks (SUN) and Smartgrid applications in the 862 - 960 MHz license-exempt frequency bands.

The SX1257's advanced features set greatly simplifies system design whilst the high level of integration reduces the external BOM to an optional RF power amplifier, and a handful of passive decoupling and matching components. A simple 4-wire 1-bit digital serial interface is provided for the baseband I and Q data streams to a baseband processor.

The SX1257 can operate in both half and full-duplex mode and is compliant with ETSI, FCC and ARIB regulatory requirements. It is available in a MLPQ-W 5 x 5 mm 32 lead package.

1.1. Simplified Block Diagram

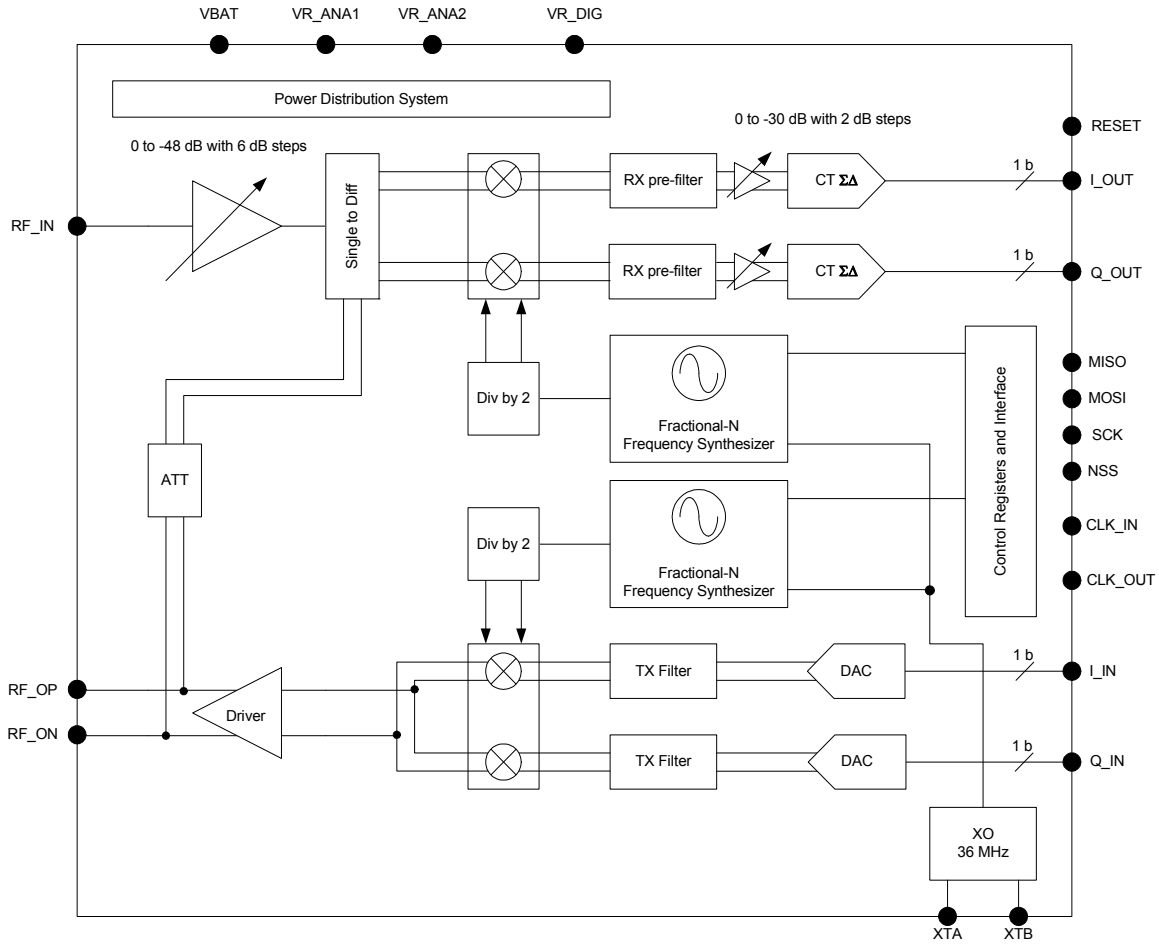


Figure 1. Block Diagram

1.2. Pin and Marking Diagram

The following diagrams illustrate the pin arrangement of the MLPQ-W package (top view) and the IC marking description.

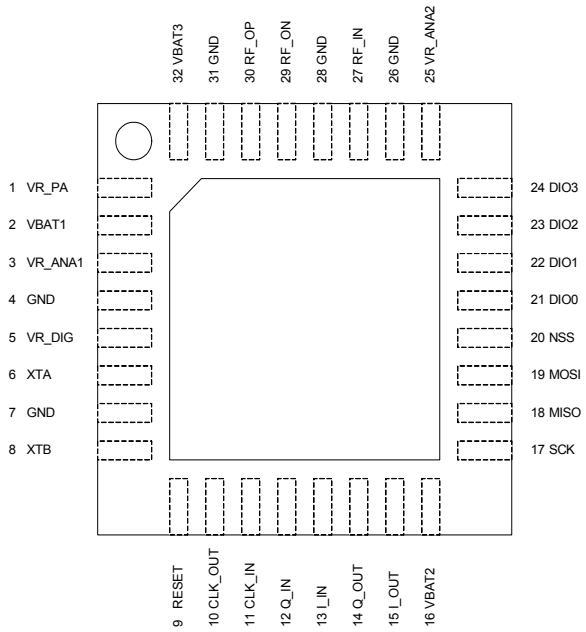


Figure 2. Pin Diagram

Figure 3. Marking Diagram

Notes yyww refers to the data code
xxxxxx refers to the lot number

1.3. Pin Description

Table 1 SX1257 Pinout

Number	Name	Type	Description
0	Ground	-	Exposed ground pad
1	VR_PA	-	Regulated supply for TX amplifier
2	VBAT1	-	VBAT Supply voltage
3	VR_ANA1	-	Regulated supply for analog TX circuit
4	GND	-	Ground
5	VR_DIG	-	Regulated supply for digital circuit
6	XTA	I/O	Crystal pad
7	GND	-	Ground
8	XTB	I/O	Crystal pad / input for external clock
9	Reset	I/O	Reset
10	CLK_OUT	O	36 MHz digital clock output
11	CLK_IN	I	36 MHz digital clock input
12	Q_IN	I	Digital baseband data input for I (inphase) channel DAC
13	I_IN	I	Digital baseband data input for Q (quadrature) channel DAC
14	Q_OUT	O	Digital baseband data output from I (inphase) channel ADC
15	I_OUT	O	Digital baseband data output from Q (quadrature) channel ADC
16	VBAT2	-	VBAT supply voltage
17	SCK	I	SPI clock
18	MISO	O	Master In Slave Output SPI output
19	MOSI	I	Master Out Slave Input SPI input
20	NSS	I	SPI chip select
21	DIO0	O	Digital I/O, software configured
22	DIO1	O	Digital I/O, software configured
23	DIO2	O	Digital I/O, software configured
24	DIO3	O	Digital I/O, software configured
25	VR_ANA2	-	Regulated supply for analog RX circuit
26	GND	-	Ground
27	RF_IN	I	RX LNA input
28	GND	-	Ground
29	RF_ON	O	Differential TX Output, negative node
30	RF_OP	O	Differential TX Output, positive node
31	GND	-	Ground
32	VBAT3	-	VBAT supply for TX amplifier

2. Electrical Characteristics

2.1. ESD Notice

The SX1257 is a high performance radio frequency device
Class 3A of the JEDEC standard JESD22-A114-C (Human Body Model) on all pins
Class B of the JEDEC standard JESD22-A115-A (Machine Model) on all pins
Class III of the JEDEC standard JESD22-C101-C (Charged Device Model) on all pins

2.2. Absolute Maximum Ratings

Stresses above the values listed below may cause permanent device failure. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Table 2 Absolute Maximum Ratings

Symbol	Description	Min	Max	Units
VDDmr	Maximum Supply Voltage	-0.5	3.9	V
Tmr	Maximum Temperature	-55	115	°C
Tj	Maximum Junction Temperature	-	125	°C
Pmr	Maximum RF Input Level	-	+6	dBm

2.3. Operating Range

Operating ranges define the limits for functional operation and parametric characteristics of the device as described in this section. Functionality outside these limits is not implied.

Table 3 Operating Ranges

Symbol	Description	Min	Max	Units
VDDop	Operational Supply Voltage	2.7	3.6	V
Top	Operational Temperature	-40	+85	°C
Clop	Load Capacitance on Digital Ports	-	25	pF
ML	RF Input Level	-	0	dBm

2.4. Electrical Specifications

The table below gives the electrical specifications of the transceiver under the following conditions:

supply Voltage = 3.3 V, temperature = 25 °C, f_{XOSC} = 36 MHz, f_{RF} = 915 MHz, OFDM with 16-QAM, 3/4 rate coded with 26 active tones (IEEE 802.15.4g MR-OFDM Option 3). Output power = -5 dBm (100 ohm differential transmission), TXBWANA = 250 kHz, RXBWANA = 250 kHz, External baseband RX filter = 150 kHz, unless otherwise specified.

2.4.1. Power Consumption

Table 4 Power Consumption Specification

Symbol	Description	Conditions	Min	Typ	Max	Units
IDDSL	Supply Current in Sleep Mode		-	0.5	1	uA
IDDST	Supply Current in Standby Mode	Crystal oscillator enabled	-	1.15	1.5	mA
IDDRX	Supply Current in Receive Mode		-	20	25	mA
IDDTX	Supply Current in Transmit Mode	RFOutput Power = -5 dBm	-	58	85	mA

2.4.2. Frequency Synthesis

Table 5 Frequency Synthesizer Specification

Symbol	Description	Conditions	Min	Typ	Max	Units
FR	Synthesizer Frequency Range	Programmable	862	-	1020	MHz
FXOSC	Crystal Oscillator Frequency	See Section 5	32	36	36	MHz
TS_OS	Crystal Oscillator Wake-up Time	From sleep mode	-	300	500	us
TS_FS	RX Frequency Synthesizer Wake-up Time	Crystal Oscillator Enabled	-	100	150	us
FSTEP	Frequency Synthesizer Step Size	FSTEP = FXOSC / 2^{19}	61	68.7	68.7	Hz
TS_HOP_RX	RX Frequency Synthesizer Hop Time (to within 10 kHz of target frequency)	200 kHz step 400 kHz step 1.2 MHz step 25 MHz step	- - - -	tbd tbd tbd tbd	- - - -	us us us us
TS_HOP_TX	RX Frequency Synthesizer Hop Time (to within 10 kHz of target frequency)	200 kHz step 400 kHz step 1.2 MHz step 25 MHz step	- - - -	tbd tbd tbd tbd	- - - -	us us us us

2.4.3. Transmitter Front-End

Table 6 TX Front-End Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
FCLK_IN	External Clock Frequency for TX Synthesizer or DAC input clock	SX1257 slave mode	32	-	36	MHz
TXPmax	TX Maximum Output Power	Saturated Power	+5	+8	-	dBm
TXP1dB	TX 1 dB Compression Point	Peak Value	+3	+6	-	dBm
TXOIP3	TX Output IP3	-5 dBm average output power	+13	+16	-	dBm
PHN	Transmitter Phase Noise	100 kHz offset from carrier	-	-98	-	dBc/Hz
PHNF	Transmitter Output Noise Floor	10 MHz offset from carrier	-131	-128	-	dBc/Hz
PHNID	Transmitter Integrated DSB Phase Noise	Integrated bandwidth from 500 Hz to 125 kHz	-	0.6	1.5	°RMS
TXGM	Transmitter IQ Gain Mismatch		-	0.5	1	dB
TXPM	Transmitter IQ Phase Mismatch		-	1	3	°
TXBWANA	Transmitter Analog Prefilter BW (SSB)	Programmable	210	-	850	kHz
TXBWANAPrc	Transmitter Analog Prefilter BW precision		-30	-	+30	%
TXBWDIFG	Transmitter FIR-DAC Taps	Programmable	24	-	64	-
TXLO	TX LO Leakage (Before DC offset Calibration)	ADC rms input: -10 dBFS	-	-8	-	dBc
TXEVM	Transmitter Error Vector Magnitude			tbd		dB
TS_TR	Transmitter Wake-up Time	Frequency synthesizer enabled	-	120	-	us

2.4.4. Receiver Front-End

Table 7 RX Front-End Specification

Symbol	Description	Conditions	Min	Typ	Max	Units
FCLK_IN	External Clock Frequency for RX ADC	SX1257 slave mode	32	-	36	MHz
CLK_INJ	External Clock Jitter Specification	External clock. White noise	-	-	0.01	%
RXNF	Receiver Noise Figure	Maximum LNA Gain	-	7	10	dB
RXGR	RX Gain Range	Adjustable in 2 dB steps	-	70	-	dB
IIP3	3rd Order Input Intercept Point Unwanted tones are 2 MHz and 3.8 MHz above the LO	Lowest LNA gain Highest LNA gain	+10 -28	- -25	- -	dBm dBm
RXGM	Receiver IQ Gain Mismatch		-	0.5	1	dB
RXPM	Receiver IQ Phase Mismatch		-	1	3	°

Table 7 RX Front-End Specification

Symbol	Description	Conditions	Min	Typ	Max	Units
RXBWANA	Receiver Analog Prefilter BW (SSB)	Programmable	250	-	750	kHz
TS_RE	Receiver Wake-up Time	Frequency synthesizer enabled	-	tbd	-	ms

2.4.5. SPI Bus Digital Specification

Table 8 SPI Digital Specification

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{IH}	Digital Input High Level		0.8	-	-	VDD
V_{IL}	Digital Input Low Level		-	-	0.2	VDD
V_{OH}	Digital Output High Level	Imax = 1 mA	0.9	-	-	VDD
V_{OL}	Digital Output Low Level	Imax = -1 mA	-	-	0.1	VDD
F_{SCK}	SCK Frequency		-	-	10	MHz
t_{ch}	SCK High Time		50	-	-	ns
t_{cl}	SCK Low Time		50	-	-	ns
t_{rise}	SCK Rise Time		-	5	-	ns
t_{fall}	SCK Fall Time		-	5	-	ns
t_{setup}	MOSI Set-up Time	From MOSI change to SCK rising edge	30	-	-	ns
t_{hold}	MOSI Hold Time	From SCK rising edge to MOSI change	60	-	-	ns
t_{nsetup}	NSS Set-up Time	From NSS falling edge to SCK rising edge	30	-	-	ns
t_{nhold}	NSS Hold Time	From SCK falling edge to NSS rising edge	100	-	-	ns
t_{nhigh}	NSS High Time Between SPI Access		20	-	-	ns
t_{data}	Data Hold and Set-up Time		250	-	-	ns

3. Chip Description

This section describes the architecture of the SX1257 Multi-PHY mode transceiver.

3.1. Power Supply Strategy

The SX1257 employs an advanced power distribution scheme (PDS), which provides stable operating characteristics over the full temperature and voltage range of operation.

The SX1257 can be powered from any low-noise voltage source via pins VBAT1, VBAT2 and VBAT3. Decoupling capacitors should be connected, as suggested in the reference design, on VR_PA, VR_DIG, VR_ANA1 and VR_ANA2 pins to ensure a correct operation of the built-in voltage regulators.

3.2. Low Battery Detector

A low battery detector is also included allowing the generation of an interrupt signal in response to passing a programmable threshold adjustable through the register RegLowBat. The interrupt signal can be mapped to the DIO0 pin, through the programmation of RegDioMapping.

3.3. Frequency Synthesizer

The SX1257 incorporates two separate state of the art fractional-N PLLs for the TX and RX circuit blocks

3.3.1. Reference Oscillator

The crystal oscillator is the main timing reference of the SX1257. It provides the reference source for the transmit and receive frequency synthesizers and as a clock for digital processing.

The XO startup time, TS_OSC, depends on the actual XTAL being connected on pins XTA and XTB. When using the built-in sequencer, the SX1257 optimizes the startup time and automatically triggers the PLL when the XO signal is stable. To manually control the startup time, the user should monitor the signal CLK_OUT which will only be made available on the output buffer when a stable XO oscillation is achieved.

An external crystal controlled source, such as a clipped-sinewave TCXO, clock can be used to replace the crystal oscillator, This external source should be provided on XTB (pin 8) and XTA (pin 6) should be left open, as illustrated in Figure 4, below.

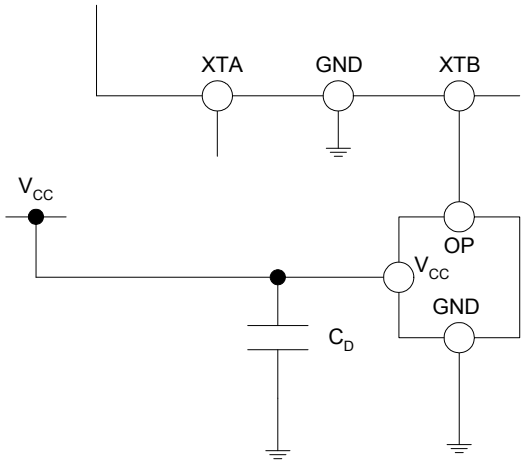


Figure 4. TCXO Connection

The peak-peak amplitude of the input signal must never exceed 1.8 V. Please consult your TCXO supplier for an appropriate value of decoupling capacitor, CD. Due to the low jitter requirements required by the receiver digital block it is recommended that only a crystal controlled external frequency source is used.

3.3.2. CLK_OUT Output

For master mode operation the SX1257 provides a system clock output made available at pin CLK_OUT.

3.3.3. PLL Architecture

The SX1257 incorporates two fourth-order type fractional-N sigma-delta PLLs. The PLLs include integrated VCO and programmable bandwidth loop filter, removing the need for any external components. The PLLs are autocalibrating and are capable of fast switching and settling times.

3.3.3.1. VCO

Both TX and RX VCOs operate at twice the RF frequency, with the oscillators centered at 1.9 GHz. This reduces any LO leakage in receive mode, to improve the quadrature precision of the receiver, and to reduce the pulling effects on the VCO during transmission.

The VCO calibration is fully automated, calibration times are fully transparent to the end-user as the processing time is included in the TS_TR and TS_RE specifications.

3.3.3.2. PLL Bandwidth

The bandwidth of the PLL loop filters are independently configurable via the configuration registers TxPllBw and RxPllBw for the modulation schemes supported, as well as fast channel switching and lock times to support FHSS and frequency agile applications, such as AFA.

3.3.3.3. Carrier Frequency and Resolution

Both the TX and RX embed a 19-bit sigma-delta modulator and the frequency resolution, constant over the entire frequency range, is calculated using the following formula:

$$F_{STEP} = \frac{F_{XOSC}}{2^{19}}$$

The RX and RX carrier frequencies are programmed through registers RegFrfRx and RegFrfTx, split across register addresses 0x01 to 0x03 and 0x04 to 0x06, respectively, and are calculated by:

$$F_{RF} = F_{STEP} \times Frfxx(23,0)$$

where: Frfxx is the integer value of the RegFrfRx or RegFrfTx as defined above.

Note: As stated above, the Frfxx settings are split across 3 bytes for both the transmitter and receiver frequency synthesizers. A change in the center frequency will only be taken into account when the least significant byte FrfxxLsb in RegFrfxxLsb is written and when exiting SLEEP mode

3.3.3.4. PLL Lock Time

RX and TX PLL lock times are a function of a number of technical factors, such as synthesized frequency, frequency step, etc. The SX1257 includes an auto-sequencer that manages the start-up sequence of the PLL.

3.3.3.5. Lock Detect Indicator

A lock indication signal for both RX and TX PLLs can be accessed via DIO pins, and is toggled high when the PLL reaches its locking range. Please refer to Table 11 to map this interrupt to the desired DIO pins.

3.4. Transmitter Analog Front-End Description

The analog front-end of the SX1257 transmitter stage comprises the TX frequency synthesizer, I and Q channel filters, the I / Q mixer and RF amplifier blocks.

3.4.1. Architectural Description

The block diagram of the transmitter front-end block is illustrated below.

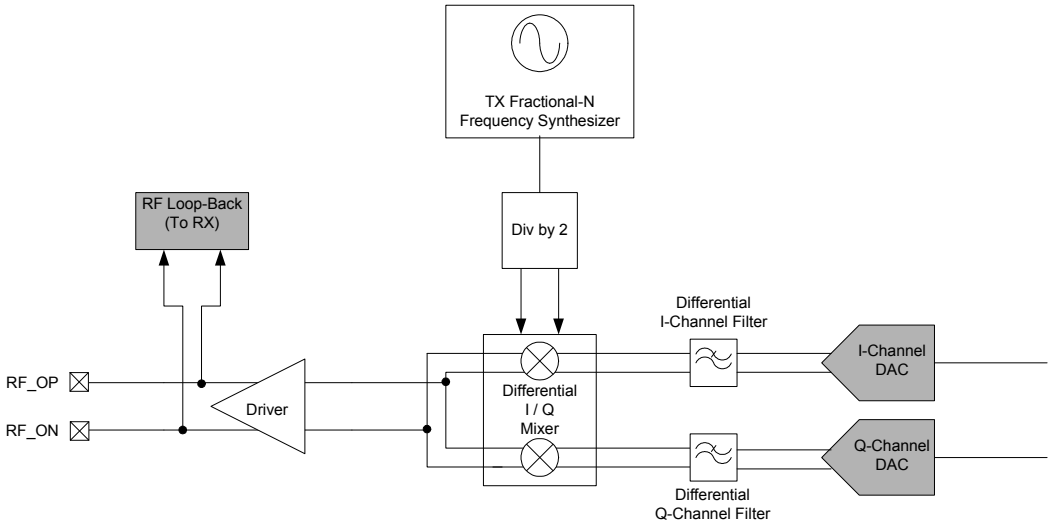


Figure 5. SX1257 Transmitter Analog Front-End Block Diagram

3.4.2. TX I / Q Channel Filters

Differential analog I and Q signals input to the TX Front-End from the TX FIR DAC are filtered by I and Q channel filters. These filters smooth the reconstructed analog waveforms and remove quantization noise generated by the I and Q channel TX FIR DACs. The filters are unity gain third-order low pass Butterworth types with programmable bandwidth configured via TxAnaBw.

The 3 dB BW of the analog TX filter BW can be calculated from:

$$BW_{3dB} = \frac{17.15}{(41 - RegTxBwAna(4,0))}$$

The analog filter bandwidth should be set to greater than the signal bandwidth so as to reduce any group delay variations.

The range of programmable TX analog filter bandwidths is tabulated below in Table 9.

Table 9 TX Analog Filter Single Sideband Bandwidth

TxAnaBw (Dec)	TxAnaBw (Bin)	SSB Filter BW (kHz)	TxAnaBw (Dec)	TxAnaBw (Bin)	SSB Filter BW (kHz)
0	00000	209	16	10000	343
1	00001	214	17	10001	357
2	00010	220	18	10010	373
3	00011	226	19	10011	390
4	00100	232	20	10100	408
5	00101	238	21	10101	429
6	00110	245	22	10110	451
7	00111	252	23	10111	476
8	01000	260	24	11000	504
9	01001	268	25	11001	536
10	01010	277	26	11010	572
11	01011	286	27	11011	613
12	01100	296	28	11100	660
13	01101	306	29	11101	715
14	01110	318	30	11110	780
15	01111	330	31	11111	858

3.4.3. TX I / Q Up-Conversion Mixers

The TX I / Q mixer block mixes the baseband analog I and Q signals with that from the PLL frequency synthesizer and up converts to the RF carrier frequency. The mixer block includes a highly linear I/ Q mixer stage with programmable gain configurable via configuration register RegTxGain. The modulated RF signal is input to the TX RF amplifier stage.

3.4.4. RF Amplifier

The TX amplifier receives the input signal from the TX mixer and provides two differential outputs. The first output provides the RF_OP and RF_ON signals in TX mode. The second output is used to provide an internal differential signal to the receiver during RX gain calibration. The amplifier provides good linear performance required to meet the peak to average power level variation of OFDM.

The peak output power is +5 dBm, which allows for an average output power of greater than -5 dBm with 10 dB back-off. The Output signal is intended to be amplified through a suitable external RF power amplifier to the maximum permissible

level allowed by relevant regulatory standards. The optimum load impedance presented RF amplifier is 100 ohms differential.

3.5. Transmitter Digital Baseband Description

The transmitter digital baseband section contains separate I and Q channel digital-to-analog convertors.

3.5.1. Digital-to-Analog Converters

The TX DAC is the first block of the SX1257 transmitter. It accepts the 1-bit I and Q noise shaped 32 Msample/second or 36 MSample/second bit-stream from the baseand processor and converts into two analog differential signals. Each TX DAC provides 8-bits of resolution in a 500 kHz bandwidth which corresponds to maximum RF transmitted double sideband bandwidth of 1 MHz.

A programmable Finite Impulse Response (FIR) filter allows the removal of the digital modulator noise from the external baseband processor. The number of taps implemented by the FIR-DAC and subsequent single-side DAC bandwidth is controlled by the parameter TxDacBw.

Table 10 TX DAC Single Sideband Bandwidth

TxDacBw (Dec)	TxDacBw (Bin)	No. DAC-FIR Taps	SSB Filter BW (kHz)
0	000	24	
1	001	32	450
2	010	40	
3	011	48	
4	100	56	
5	101	64	290

Examples of the FIR DAC normalized magnitude response are illustrated below.

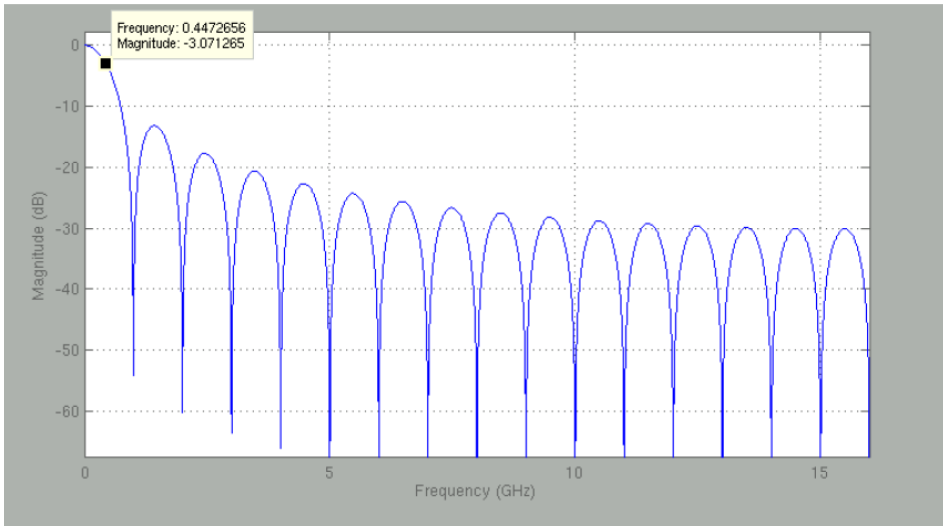


Figure 6. FIR-DAC Normalized Magnitude Response with f_S = 32 MHz and N = 32

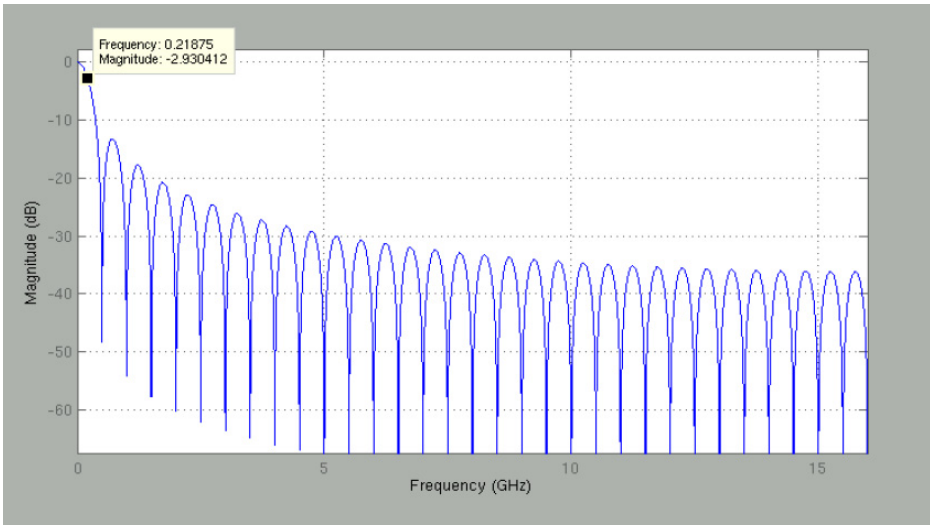


Figure 7. FIR-DAC Normalized Magnitude Response with f_S = 32 MHz and N = 64

The DAC 3dB bandwidth is proportional to the sampling frequency fs and inversely proportional to the number of taps N. In the case where f_S = 32MHz with N = 32 the 3 dB bandwidth is typically 450 kHz. Reducing the bandwidth may be useful to reduce the quantisation noise contribution when the signal bandwidth request is lower, as is illustrated in the case where N = 64, resulting in a 3 dB bandwidth of approximately 290 kHz.

3.5.2. I and Q Serial Interface

I and Q data is input to the DACs on the rising edge of the reference sampling clock and is sampled on a falling edge. The TX DAC can be used either with an external clock CLK_IN or with the internal clock, available on CLK_OUT for data synchronization (recommended mode).

The I and Q channel bit stream timing diagram is illustrated below.

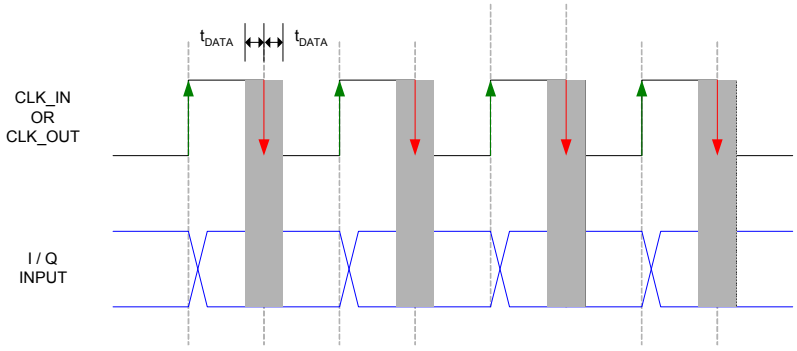


Figure 8. Transmitter I and Q Channel Bit-Stream Timing Diagram

3.6. Receiver Analog Front-End Description

The SX1257 Receiver Front-End is based upon a Zero-IF architecture, ideally suited to handle multiple complex modulation schemes. The RX chain incorporates a programmable gain LNA and single to differential buffer, I / Q mixer, separate I and Q channel analog low-pass filters and programmable baseband amplifiers. The amplified differential analog I and Q outputs are input to two 5th order continuous-time Sigma-Delta Analog to Digital Converters (ADC) for further signal processing in the digital domain.

3.6.1. Architectural Description

The block diagram of the receiver front-end block is illustrated below.

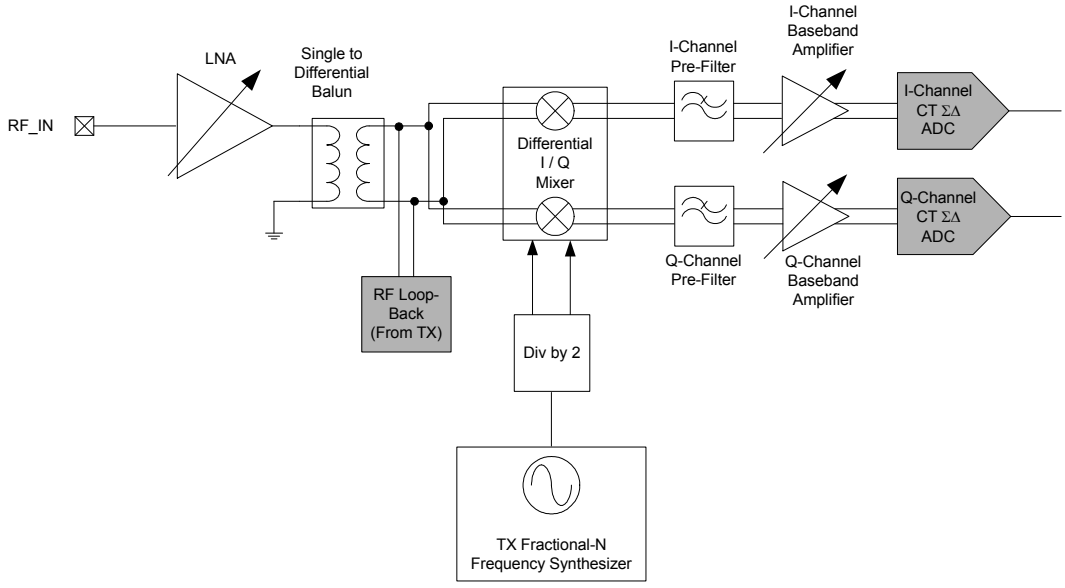


Figure 9. SX1257 Receiver Analog Front-End Block Diagram

3.6.2. LNA and Single to Differential Buffer

The LNA uses a common-gate topology, which allows for a flat characteristic over the whole frequency range. It is designed to have an input impedance of 50 Ohms or 200 Ohms (as selected with bit LnaZin in RegRxAnaGain). A single to differential buffer is implemented to improve the second order linearity of the receiver.

The LNA gain, including the single-to-differential buffer, is programmable over a 48 dB dynamic range, and gain control can be enabled via an external AGC function.

3.6.3. I /Q Downconversion Quadrature Mixer

The mixer is inserted between output of the RF buffer stage and the input of the I and Q channel analog low-pass filter stages.This block is designed to downconvert the spectrum of the input RF signal to base-band and offers both high IIP2 and IIP3 responses.

3.6.4. Baseband Analog Filters and Amplifiers

The differential I and Q baseband mixer signals are pre-filtered by a programmable 1st order low-pass pre-filter and input to programmable linear baseband amplifiers. The single sideband 3 dB bandwidth of the pre-filters can be programmed between 250 kHz and 750 kHz. This additional pre-filtering improves the selectivity of the receiver for complex modulation schemes, such as OFDM.

The amplifier stage gain offers 32 dB of programmable gain, in 2 dB steps, from -24 dB to +6 dB via configuration register RegRxAnaGain while the analog filter bandwidth is programmed via the two least significant bits of configuration register RegRxBw.

3.7. Receiver Digital Baseband

The receiver digital baseband section contains separate I and Q channel continuous time Sigma-Delta analog-to-digital converters to digitize and filter the analog bit stream.

3.7.1. Architectural Block Diagram

The block diagram of the receiver digital baseband is illustrated below.

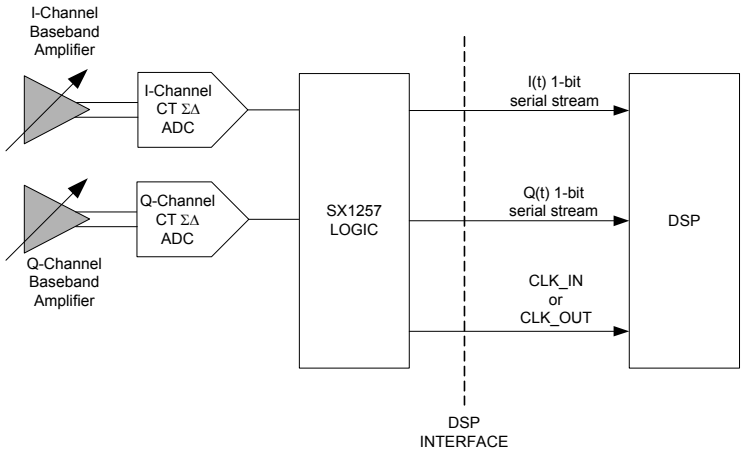


Figure 10. SX1257 Digital Receiver Baseband Block Diagram

3.7.2. Analog-to-Digital Converters

The receiver digital baseband consists of separate I and Q channel 5th order continuous-time sigma-delta modulator analog -to-digital converters which sample and digitize the analog baseband I and Q signals output at the analog baseband amplifiers.

The ADC output allows for 13-bits of resolution after decimation and filtering by the external baseband processor within a 500 kHz maxium bandwidth, corresponding to a maximum RF received double sideband bandwidth of 1 MHz.

The ADC output is one bit per channel quadrarure bit stream at 32 or 36 MSamples/s.

3.7.3. Temperature Sensor

The receiver ADC can be used to perform a temperature measurement by digitizing the sensor response. The response of the sensor is -1C / Lsb. Since a CMOS temperature sensor is not accurate by nature, the sensor should be calibrated at ambient temperature for a precise reading.

It takes less than 100 us for the SX1257 to evaluate the temperature (from setting RxAdcTemp = “1”). The AdcTemp value can be read at Q_OUT. Since there is no on-chip decimation or averaging it is recommmended that data on Q_OUT is externally processed, for example using a simple FFT.

The temperature measurement should be performed with the SX1257 in StandbyEnable Mode (RegMode = 0x01)

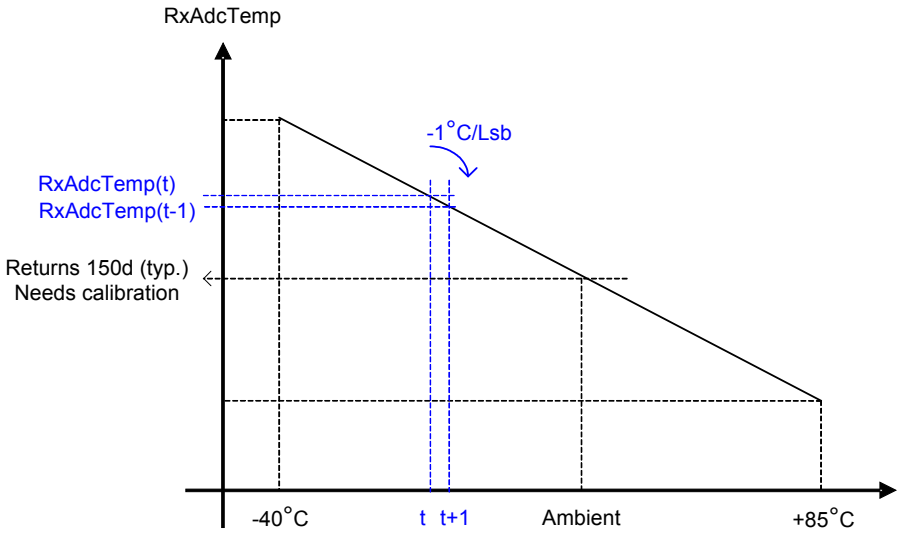


Figure 11. Temperature Sensor Response

3.7.4. I and Q Serial Interface

I and Q data is input to the ADCs on the rising edge of the reference sampling clock and is sampled on a falling edge. The RX ADC can be used either with an external clock CLK_IN or with the internal clock, available on CLK_OUT (recommended mode) for data synchronization. The I and Q channel bit stream timing diagram is illustrated below.

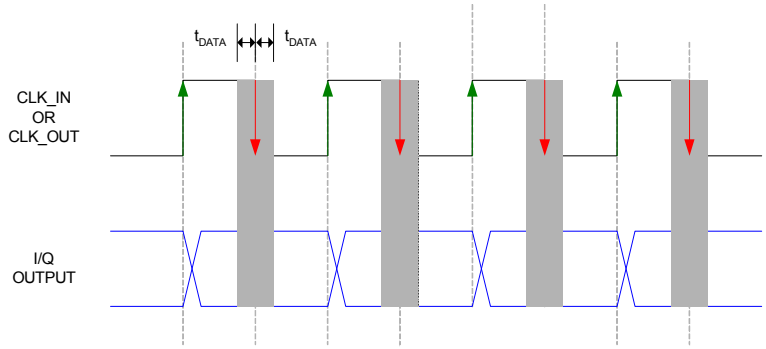


Figure 12. Receiver I and Q Channel Bit-Stream Timing Diagram

3.8. Loop-Back

The SX1257 provides mechanisms to both monitor and externally calibrate both the RF transmission path and the I and Q bit streams generated by the external baseband processor.

3.8.1. Digital Loop-Back

The digital loop-back enables the connection of the input and output I and Q baseband bit streams prior to processing by the SX1257.

This loop back path enables the validation of the transmitter and receiver baseband processing paths.

3.8.2. RF Loop Back

The RF loop-back path connects the balanced RF output signal of the transmitter driver stage to the output of the differential mixer of the receiver. This path provides a mechanism for the external baseband processor to implement a calibration for the following:

- Receiver I, Q gain mismatch
- Receiver I and Q phase imbalance
- Transmitter I, Q gain mismatch
- Transmitter I and Q phase imbalance
- Transmitter DC offset

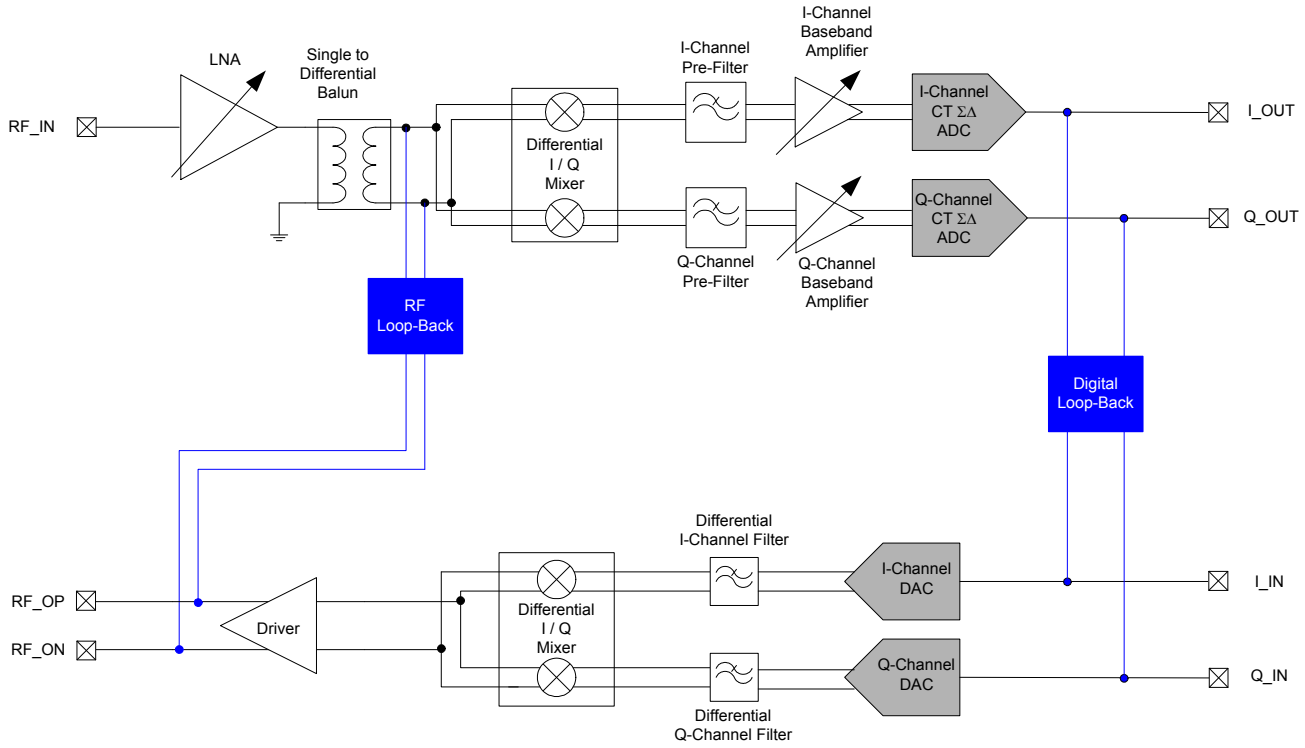


Figure 13. Digital and RF Loop-Back Paths

4. Digital Interface

The SX1257 has several operating modes, configuration parameters and internal status indicators. All these operating modes, configuration parameters and status information are stored in internal registers that may be accessed by the external micro-controller via the serial SPI interface.

4.1. SPI Bus Interface

The SPI interface gives access to the configuration register via a synchronous full-duplex protocol corresponding to CPOL = 0 and CPHA = 0 in Motorola/Freescale nomenclature. Only the slave side is implemented.

Two access modes to the registers are provided:

- SINGLE access: an address byte followed by a data byte is sent for a write access whereas an address byte is sent and a read byte is received for the read access. The NSS pin goes low at the begin of the frame and goes high after the data byte.
- BURST access: the address byte is followed by several data bytes. The address is automatically incremented internally between each data byte. This mode is available for both read and write accesses. The NSS pin goes low at the beginning of the frame and stay low between each byte. It goes high only after the last byte transfer.

An example of a typical SPI single access to a register is illustrated below.

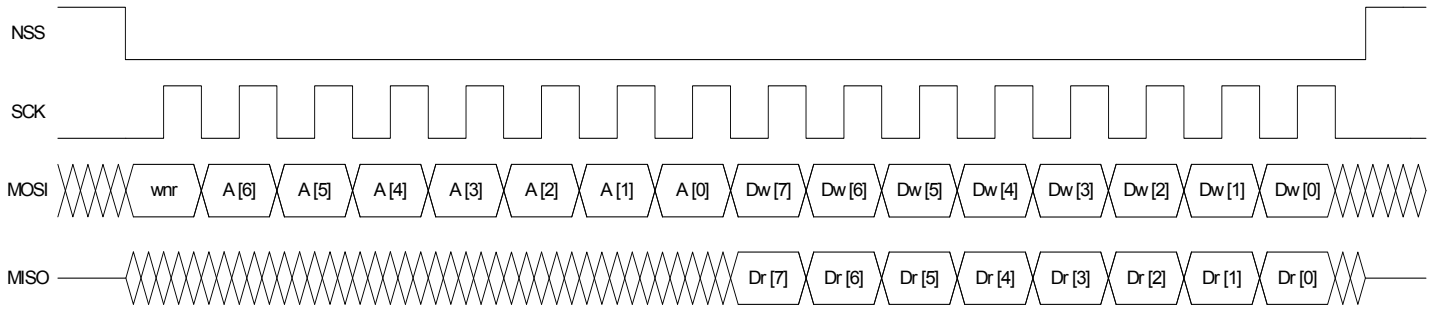


Figure 14. SPI Timing Diagram (Single Access)

MOSI is generated by the master on the falling edge of SCK and is sampled by the slave (i.e. this SPI interface) on the rising edge of SCK. MISO is generated by the slave on the falling edge of SCK.

A transfer always starts by the NSS pin going low. MISO is high impedance when NSS is high.

The first byte is the address byte. It is made of:

- wnr bit, which is 1 for write access and 0 for read access
- 7 bits of address, MSB first

The second byte is a data byte, either sent on MOSI by the master in case of a write access, or received by the master on MISO in case of read access. The data byte is transmitted MSB first.

Succeeding bytes may be sent on MOSI (for write access) or received on MISO (for read access) without rising NSS and re-sending the address. The address is then automatically incremented at each new byte received (BURST mode).

The frame ends when NSS goes high. The next frame must start with an address byte. The SINGLE access mode is actually a special case of BURST mode with only 1 data byte transferred.

During the write accesses, the byte transferred from the slave to the master on the MISO line is the value of the written register before the write operation.

4.2. Digital IO Pin Mapping

Four general purpose IO pins are available on the SX1257 and their configuration is controlled through the RegDioMapping configuration register.

Table 11 DIO Mapping

Mode	Diox Mapping	DIO3	DIO2	DIO1	DIO0
Sleep	00	-	-	-	-
	01	-	-	-	-
	10	-	-	-	-
	11	-	-	-	
Standby	00	-	xosc_ready	-	-
	01	-	-	-	-
	10	-	-	-	-
	11	-	-	-	-
RX	00	pll_lock_rx	-	-	pll_lock_rx
	01	-	-	-	pll_lock_rx
	10	-	-	-	pll_lock_rx
	11	-	-	-	Low Bat
TX	00	pll_lock_tx	-	pll_lock_tx	-
	01	-	-	-	-
	10	-	-	-	-
	11	-	-	-	-

5. Configuration and Status Registers

5.1. General Description

Table 12 Configuration Register Summary

Address	Register Name	Reset Value	Default Value	Description
0x00	RegMode	0x00		Operating modes of the SX1257
0x01	RegFrfRxMsb	0xCB		RX carrier frequency MSB
0x02	RegFrfRxMid	0x55		RX carrier frequency intermediate bits
0x03	RegFrfRxLsb	0x55		RX carrier frequency LSB
0x04	RegFrfTxMsb	0x00		RX carrier frequency MSB
0x05	RegFrfTxxMid	0xCB		RX carrier frequency intermediate bits
0x06	RegFrfTxLsb	0x55		RX carrier frequency LSB
0x07	RegVersion	0x01		Semtech ID relating to the silicon revision
0x08	RegTxGain	0x2E		TX DAC and mixer gain setting
0x0A	RegTxBw	0x30		TX FE PLL and analog filter bandwidths
0x0B	RegTxDacBw	0x02		TX DAC bandwidth
0x0C	RegRxAnaGain	0x3F		RX FE LNA and baseband amplifier gain
0x0D	RegRxBw	0xFD		RX FE ADC and analog filter bandwidths
0x0E	RegRxPLLBw	0x06		RX FE PLL bandwidth
0x0F	RegDioMapping	0x00		Mapping of DIO pins
0x10	RegClkSelect	0x02		Sampling clock congfiguration
0x11	RegMode Status	0x00		SX1257 mode status
0x1A	RegLowBatThres	0x02		Low battery threshold

Notes - Reset values are automatically refreshed at Power on Reset
- DEFAULT values are the Semtech recommended register values, optimizing the device operation
*- Registers for which the DEFAULT value differs from the RESET values are denoted by a * in the tables of this section*

5.2. Mode Configuration Registers

Table 13 Mode Configuration Registers

Name (Address)	Bits	Variable Name	Mode	Default Value	Description
RegMode (0x00)	7-4	-	r	0000	unused
	3	PADriverEnable	rw	0	Enables the TX PA driver 0 = Disabled 1 = Enabled
	2	TxEnable	rw	0	Enables the TX front-end and PLL (except the TX PA driver) 0 = Disabled 1 = Enabled
	1	RxEnable	rw	0	Enables the RX front-end and PLL 0 = Disabled 1 = Enabled
	0	StandbyEnable	rw	1	Enables the PDS and the oscillator in Standby Mode 0 = Disabled 1 = Enabled

5.3. Frequency Synthesizer Configuration Registers

Table 14 Frequency Synthesizer Configuration Registers

Name (Address)	Bits	Variable Name	Mode	Default Value	Description
RegFrfRxMsb (0x01)	7-0	FrfRx(23:16)	rw	0xCB	MSB of the RX carrier frequency
RefFrfRxMid (0x02)	7-0	FrfRx(15:8)	rw	0x55	Middle byte of the RX carrier frequency
RefFrfRxLsb (0x03)	7-0	FrfRx(7:0)	rw	0x55	LSB of the RX carrier frequency $F_{RF} = F_{STEP} \times Frfxx(23,0)$ With a 36 MHz XO default value 0xCB5555 FrfRx = 915 MHz and frequency resolution = 68.66455 Hz The RX RF frequency is updated only under the following conditions:Hz (36 MHz XO) - RefFrfRxLsb is written - When exiting SLEEP mode
RegFrfTxMsb (0x04)	7-0	FrfTx(23:16)	rw	0xCB	MSB of the TX carrier frequency

Table 14 Frequency Synthesizer Configuration Registers

Name (Address)	Bits	Variable Name	Mode	Default Value	Description
RefFrfTxMid (0x05)	7-0	FrfTx(15:8)	rw	0x55	Middle byte of the TX carrier frequency
RefFrfTxLsb (0x06)	7-0	FrfTx(7:0)	rw	0x55	LSB of the TX carrier frequency $F_{RF} = F_{STEP} \times Frfxx(23,0)$ With a 36 MHz XO default value 0xCB5555 FrfTx = 915 MHz and frequency resolution = 68.66455 Hz The TX RF frequency is updated only under the following conditions:Hz (36 MHz XO) - RefFrfTxLsb is written - When exiting SLEEP mode

5.4. Revision Configuration Register

Table 15 Revision Configuration Register

Name (Address)	Bits	Variable Name	Mode	Default Value	Description
RegRevision (0x07)	7-0	Version	r	0x21	IC version code (Current revision V2A)

5.5. Transmitter Front-End Configuration Registers

Table 16 Transmitter Front-End Configuration Registers

Name (Address)	Bits	Variable Name	Mode	Default Value	Description
RegTxGain (0x08)	7	-	r	0	Unused
	6-4	TxDacGain	rw	010	DAC gain, programmable in 3 dB steps: 000 = maximum gain - 9 dB 001 = maximum gain - 6 dB 010 = maximum gain - 3 dB 011 = maximum gain (0 dB full scale)
	3-0	TXMixerGain	rw	1110	Mixer gain, programmable in 2 dB steps: $Gain \sim -38 + 2 \times Int(TxMixerGain(3,0))dB$
RegTxBw (0x0A)	7	-	r	0	unused
	6-5	TxPllBw	rw	11	TX PLL bandwidth, programmable: 00 = 75 kHz 01 = 150 kHz 10 = 225 kHz 11 = 300 kHz
	4-0	TxAnaBw	rw	0000	TX analog filter bandwidth, programmable: $Bandwidth = \frac{17.5}{2 \times (41 - Int(TxBw(4,0)))} MHz$
RegTxDacBw (0x0B)	7-3	-	r	00000	unused
	2-0	TxDacBw	rw	010	Number of taps of TX FIR-DAC, programmable: $N = 24 + 8 \times Int(TxDacBw(2,0))$ where $N_{MAX} = 64$

5.6. Receiver Front-End Configuration Registers

Table 17 Receiver Front-End Configuration Registers

Name (Address)	Bits	Variable Name	Mode	Default Value	Description
RegRxAnaGain (0x0C)	7-5	RxLnaGain	rw	001	RX LNA gain setting: 000 = not used 001 = G1 = highest gain power - 0 dB 010 = G2 = highest gain power - 6 dB 011 = G3 = highest gain power - 12 dB 100 = G4 = highest gain power - 24 dB 101 = G5 = highest gain power - 36 dB 110 = G6 = highest gain power - 48 dB 111 = not used
	4-1	RxBasebandGain	rw	1111	RX Baseband amplifier gain, programmable: $Gain = Gain + 2 \times Int(RxBasebandGain(4,1))dB$
	1	LnaZin	rw	1	LNA input impedance 0 = 50 Ω 1 = 200 Ω
RegRxBw (0x0D)	7-5	RxAdcBw	rw	111	RX ADC BW, programmable: 010 = 100 kHz < RxAdcBw < 200 kHz 101 = 200 kHz < RxAdcBw < 400 kHz 111 = 400kHz < RxAdcBw
	4-2	RxAdcTrim	rw	111	RX ADC trim 32 MHz reference crystal: RxAdcTrim = 110 36 MHz reference crystal: RxAdcTrim = 101
	1-0	RxBasebandBw	rw	01	Bandwidth of RX analog roofing filter, programmable: 00 = 750 kHz 01 = 500 kHz 10 = 375 kHz 11 = 250 kHz
RegRxPLLBw (0x0E)	7-3	-	r	0000	unused
	2-1	RxPllBw	rw	11	RX PLL bandwidth, programmable: 00 = 75 kHz 01 = 150 kHz 10 = 225 kHz 11 = 300 kHz
	0	RxAdcTemp	rw	0	RX ADC temperature measurement mode 0 = Disabled 1 = Enabled

5.7. DIO Mapping Configuration Register

Table 18 DIO Mapping Configuration Register

Name (Address)	Bits	Variable Name	Mode	Default Value	Description
RegDioMapping (0x0F)	7-6	Dio0Mapping	rw	00	Mapping of pins DIO0 to DIO3. See Table 11for further information.
	5-4	Dio1Mapping	rw	00	
	3-2	Dio2Mapping	rw	00	
	1-0	Dio3Mapping	rw	00	

5.8. Additional Parameter Configuration Registers

Table 19 Additional Parameters Configuration Registers

Name (Address)	Bits	Variable Name	Mode	Default Value	Description
RegClkSelect (0x10)	7-4	-	r	0000	unused
	3	DigitalLoopBack	rw	0	Digital loop back enable 0 = Disabled 1 = Enabled
	2	RfLoopBack	rw	0	RF Loop back enable for RX analog gain calibration 0 = Disabled 1 = Enabled
	1	Clk_out	rw	1	CLK_OUT enable 0 = Disabled 1 = Enabled
	0	TxDacClkSelect	rw	0	Clock select for TX DAC 0 = Internal clock (XTAL) 1 = External clock (CLK_IN)
RegModeStatus (0x11)	7-3	-	r	00000	unused
	2	LowBatEnable	rw	0	LowBat detect flag 0 = VBAT > LowBat threshold 1 = VBAT < LowBat threshold (low battery)
	1	PllLockRx	r	0	Asserted when RX PLL locked
	0	PlllLockTx	r	0	Asserted when TX PLL locked

Table 19 Additional Parameters Configuration Registers

Name (Address)	Bits	Variable Name	Mode	Default Value	Description
RegLowBatThres (0x1A)	7-3	-	r	00000	unused
	2-0	LowBatThres	rw	010	LowBat Threshold 000 = 2.516 V 001 = 2.619 V 010 = 2.724 V 011 = 2.829 V 100 = 2.935 V 101 = 3.037 V 110 = 3.143 V 111 = 3.245 V

6. Application Information

6.1. Crystal Resonator Specification

The specification for the crystal resonator of the reference oscillator circuit block is tabulated below in Table 20.

Table 20 Crystal Resonator Specification

Symbol	Description	Conditions	Min	Typ	Max	Units
FXOSC	XTAL Frequency		32	-	36	MHz
RS	XTAL Series Resistance		-	30	140	Ω
C0	XTAL Shunt Capacitance		-	2.8	7	pF
CLOAD	External Foot Capacitance	On each pin XTA and XTB	8	16	22	pF

Notes - The initial frequency tolerance, temperature stability and ageing performance should be chosen in accordance with the target operating temperature range and the receiver bandwidth selected
- The loading capacitance should be applied externally, and adapted to the actual Cload specification of the XTAL

6.2. Reset of the Chip

A power-on reset of the SX1257 is automatically triggered at power up. Additionally, a manual reset can be issued by controlling the RESET pin (pin 9).

6.2.1. POR

If the application requires the disconnection of VDD from the SX1257, despite the extremely low Sleep Mode current, the user should wait for 10 ms from of the end of the POR cycle before commencing communications over the SPI bus. Pin 9 (RESET) should be left floating during the POR sequence.

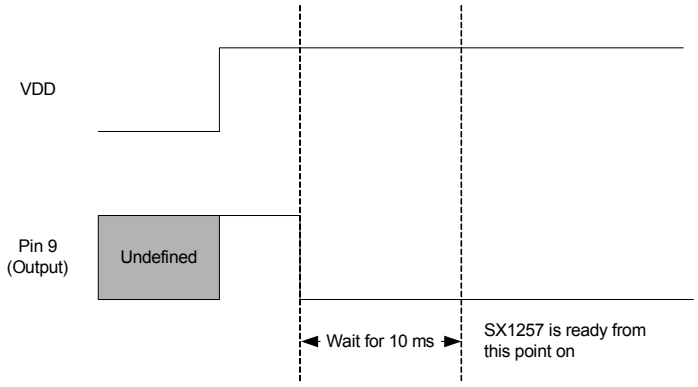


Figure 15. POR Timing Diagram

Please note that CLK_OUT activity can be used to detect that the chip is ready.

6.2.2. Manual Reset

A manual reset of the SX1257 is possible even for applications in which VDD cannot be physically disconnected. Pin 9 should be pulled high for a hundred microseconds, and then released. The user should then wait for 5 ms before using the chip.

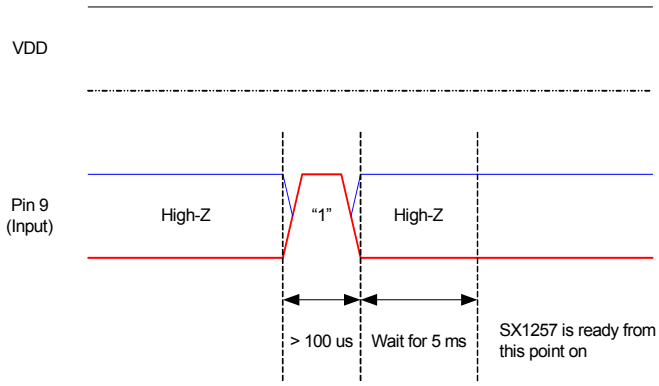


Figure 16. Manual Reset Timing Diagram

Please note that whilst pin 9 is driven high, an over current consumption of 10 mA may be observed on VDD

6.3. TX Noise Shaper

In order to generate a single TX bit-stream, th 8-bit I and Q signal should be processed by an external third order sigma-delta modulator (implemented within the baseband processor). The noise shaper should be stable for input signals lower than -3dBFS and compatible with SX1257 noise requirements. It is advised that the integrator outputs are saturated to avoid any wraparound of the 2's-complement digital word.

A representative block diagram of a single-bit feed-forward modulator is illustrated below.

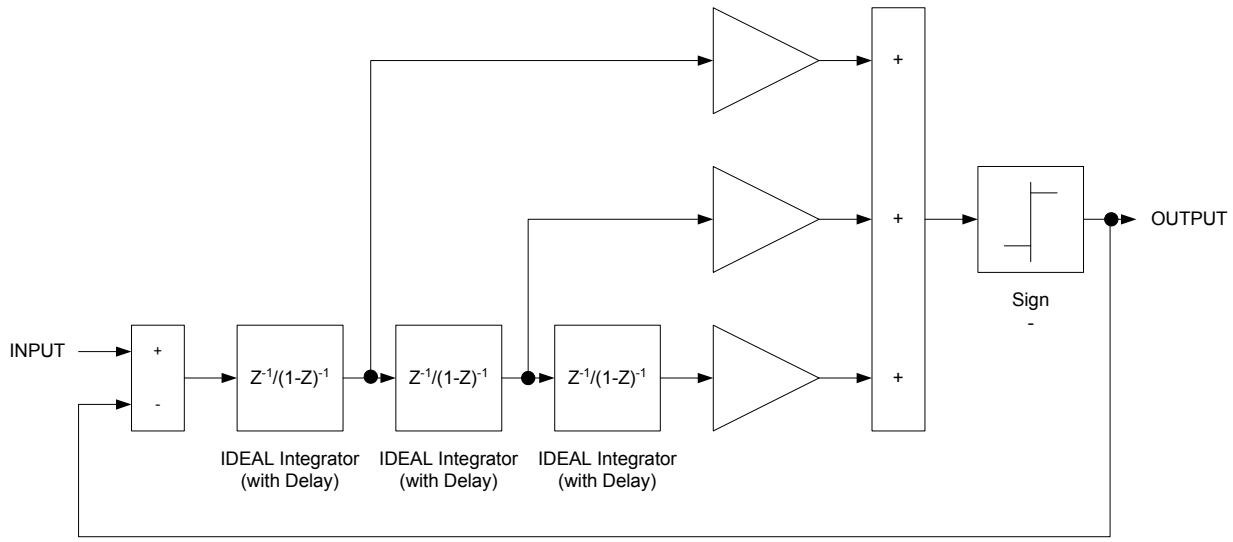


Figure 17. Example Digital Modulator Implementation

6.4. Reference Design

Please contact your Semtech representative for evaluation tools, reference designs and design assistance. Note that all schematics shown in this section are full schematics, listing ALL required components, including those required for power supply decoupling.

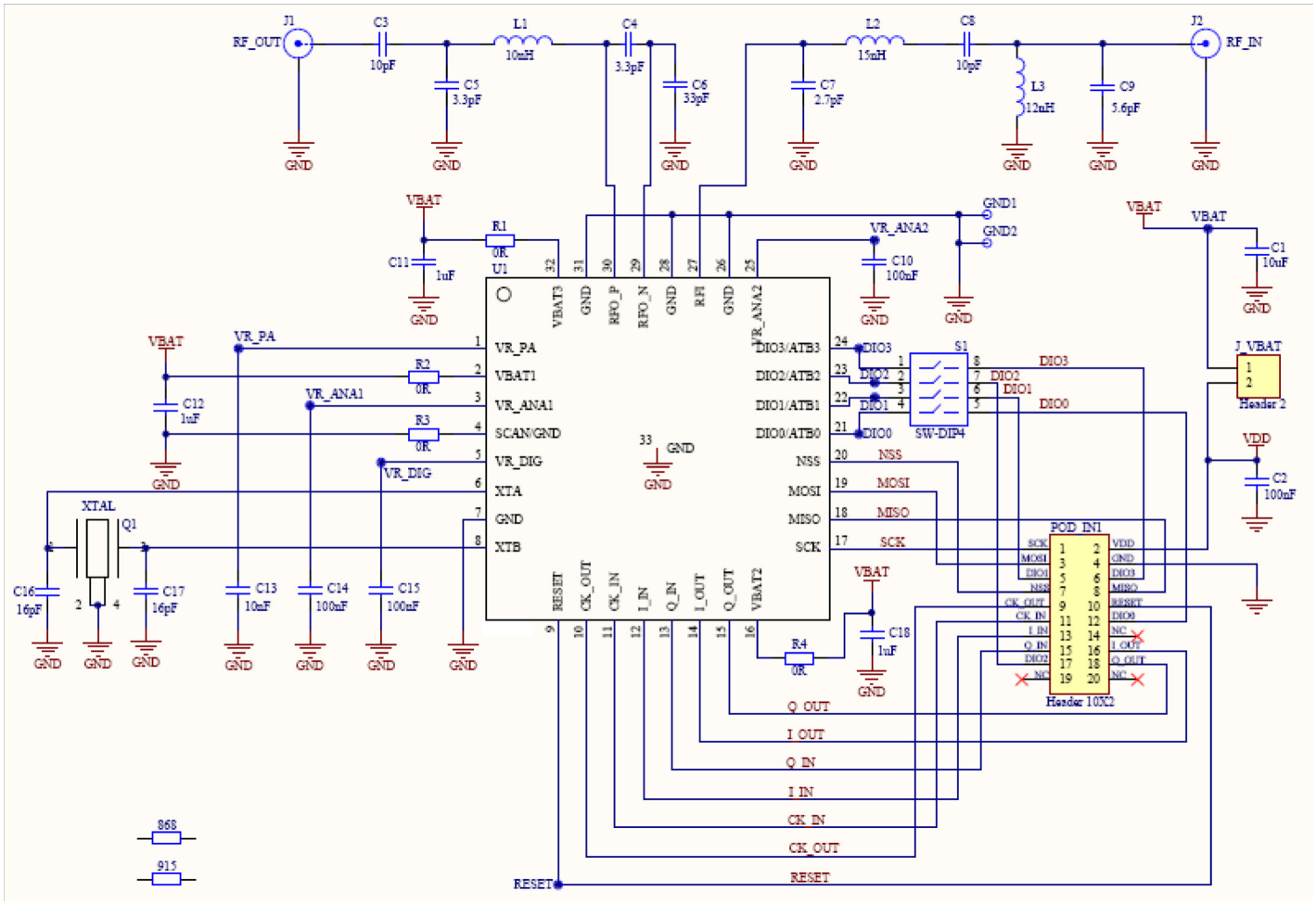
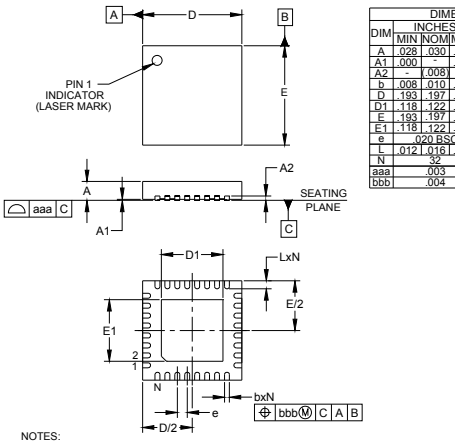


Figure 18. SX1257 Application Schematic

7. Packaging Information

7.1. Package Outline Drawing

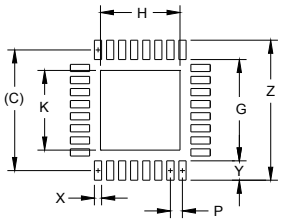


DIMENSIONS						
DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.028	.030	.031	0.70	0.75	0.80
A1	.000	-	.002	0.00	-	0.05
A2	-	(.008)	-	-	(0.20)	-
b	.008	.010	.012	0.18	0.25	0.30
D	.193	.197	.201	4.90	5.00	5.10
D1	.118	.122	.126	3.00	3.10	3.20
E	.193	.197	.201	4.90	5.00	5.10
E1	.118	.122	.126	3.00	3.10	3.20
e	.020 BSC			0.50 BSC		
L	.012	.016	.020	0.30	0.40	0.50
N	32			32		
aaa	.003			0.08		
bbb	.004			0.10		

NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

Figure 19. Package Outline Drawing

7.2. Recommended Land Pattern



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.193)	(4.90)
G	.161	4.10
H	.130	3.30
K	.130	3.30
P	.020	0.50
X	.012	0.30
Y	.031	0.80
Z	.224	5.70

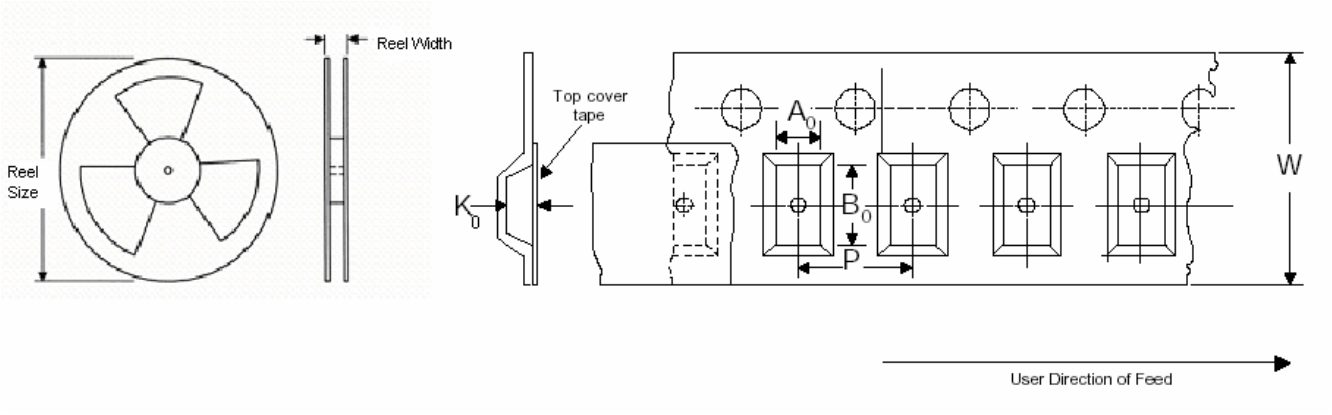
NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
3. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.
4. SQUARE PACKAGE-DIMENSIONS APPLY IN BOTH X AND Y DIRECTIONS.

Figure 20. Recommended Land Pattern

7.3. Thermal Impedance

The thermal impedance of this package is: **Theta ja = 23.8° C/W typ**., calculated from a package in still air, on a 4-layer FR4 PCB, as per the Jedec standard.

7.4. Tape and Reel Specification



Carrier Tape (mm)				Reel (mm)				
Tape Width (W)	Pocket Pitch (P)	A_O / B_O	K_O	Reel Size	Reel Width	Min. Trailer Length (mm)	Min. Leader Length (mm)	QTY per Reel
12 +/- 0.30	8 +/- 0.20	5.25 +/- 0.20	1.10 +/- 0.10	330.2	12.4	400	400	3000

Note Single sprocket holes

Figure 21. Tape and Reel Specification

8. Chip Revisions

SX1257 revision history is tabulated below in Figure 21.

Table 21 Chip Revision Identification

Chip Version	Register Value @Address 0x07	Lot Codes (See Figure 3)	Comment
V2A	0x21	-	-

9. Revision History

Table 22 Datasheet Revision History

Revision	Date	Comment
1	February 2012	First FINAL datasheet revision

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