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Digital Design Assignment-5

I] $T_c \geq T_{pcq} + T_{setup} + T_{pd}$ {Setup constraint}

$\therefore T_{cmin} = 11$

$= 100 + 200 + 900 + 300 + 500$

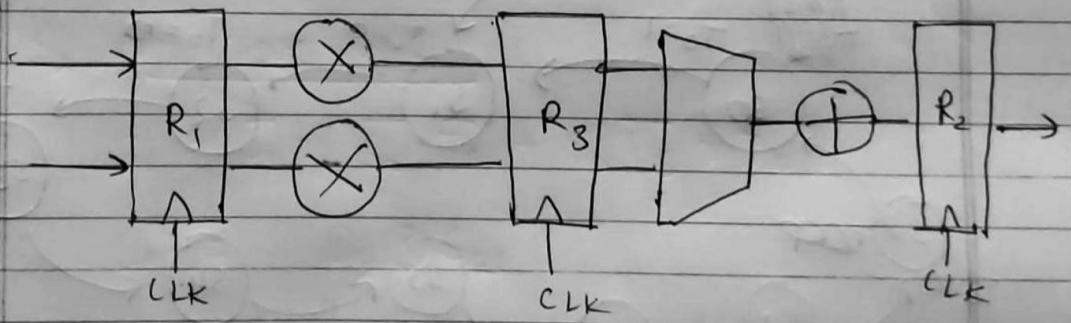
$= 2000ps$

II] $T_c + T_{skew} \geq T_{pcq} + T_{setup} + T_{pd}$ {setup constr. with Skew}

$\therefore T_{cmin} = 11 - T_{skew}$

$= 2000 - 200 = 1800ps$

III]



Here, $T_{cmin}(R_3) = T_{pcq}(R_1) + T_{pd}(Mul) + T_{setup}(R_3)$

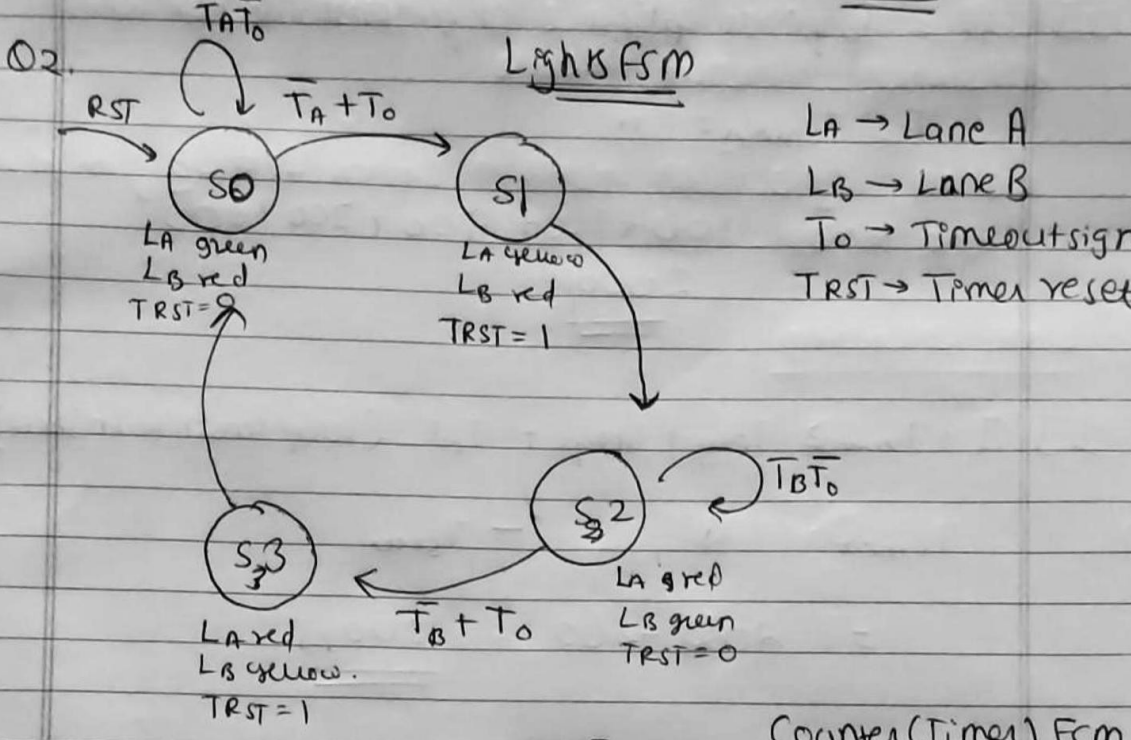
$= 1200ps$

$T_{cmin}(R_2) = T_{pd}(mux) + T_{pd}(add) + T_{pcq}(R_3) + T_{setup}(R_2)$

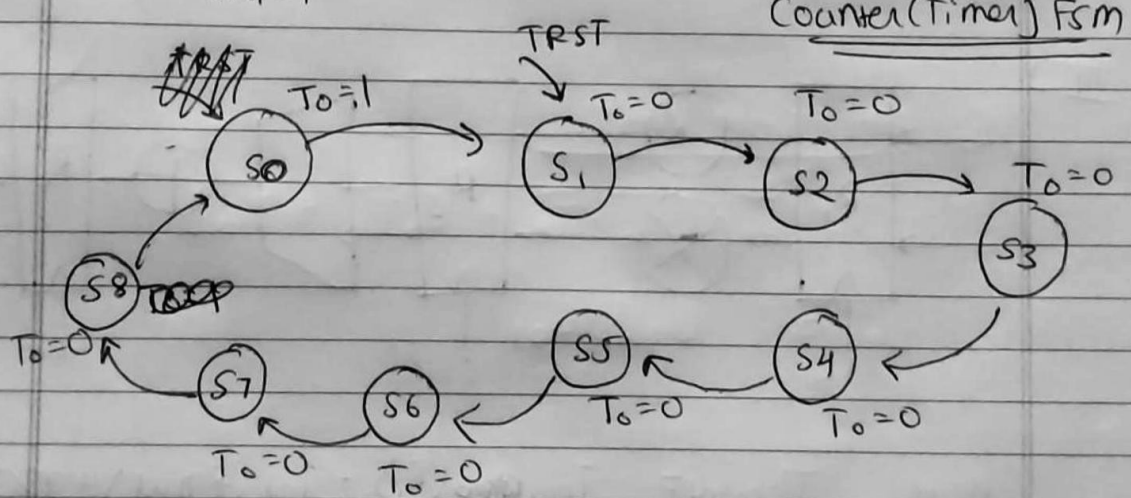
$= 1100ps$

$\therefore T_{cmin} = \max(T_{cmin R_2}, T_{cmin R_3}) = 1200ps$

Q2.



$L_A \rightarrow$ Lane A
$L_B \rightarrow$ Lane B
$T_o \rightarrow$ Timeoutsignal
$T_{RST} \rightarrow$ Timer reset.



when The traffic is present on a lane & it is green, it remains green for 8 cycles after which it now moves to the next state,

If the other lane also has traffic, then it stays green

The FSM is split into 2 factors Counter & Lights FSM, counter module outputs T_0, which tells when timeout occurs.

When lights fsm moves in states S1 or S3, it resets the timer.

State encoding

	S_0	S_1
S0	0	0
S1	0	1
S2	1	0
S3	1	1

S_1 Next state logic

$$S_1' = \overline{S_1} \cdot (\overline{S_0} \cdot \overline{T_A} + S_0 \overline{T_B} + T_0)$$

$$S_0' = S_0 \otimes S_{21}$$

State transition table

S_0	S_1	T_A	T_B	T_0	S_0'	S_1'
0	0	1	X	0	0	0
0	0	0	X	X	0	1
0	0	X	X	1	0	1
0	1	X	X	X	1	0
1	0	X	1	0	1	0
1	0	X	0	X	1	1
1	0	X	X	1	1	1
1	1	X	X	X	0	0