UNIVERSITÉ DE MONTRÉAL

DEVOIR 4

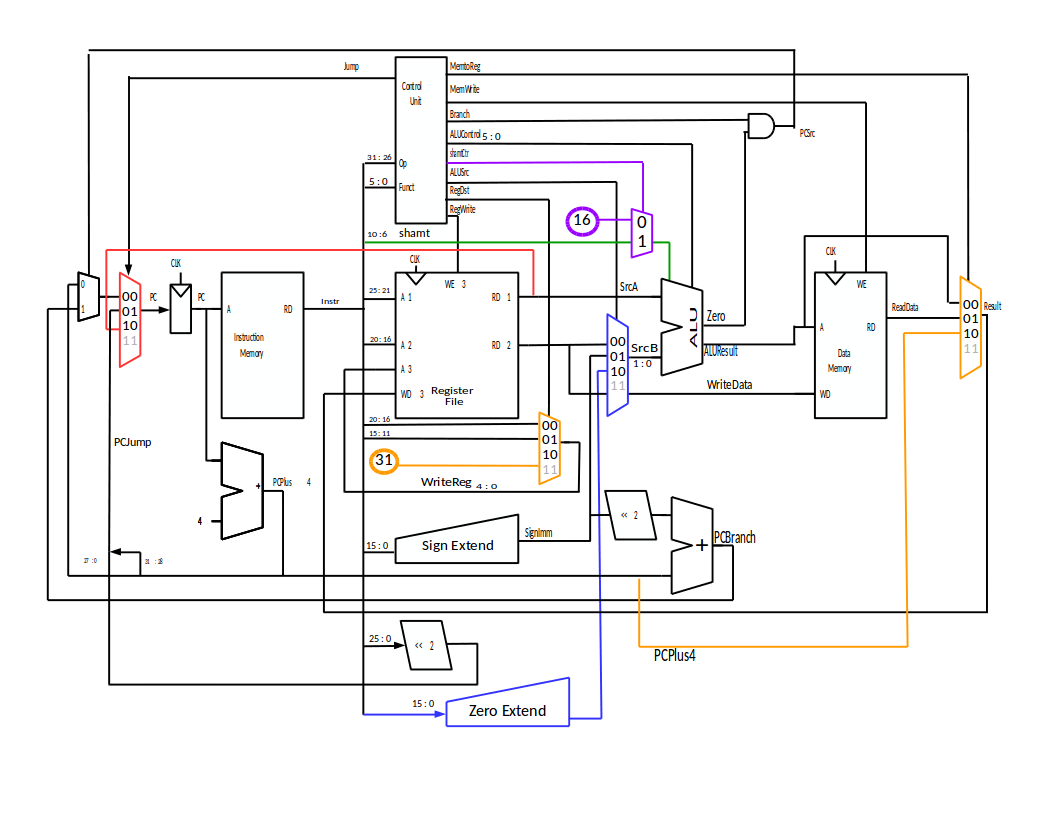
PAR:

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**Schéma du processeur MIPS**

**Table de vérité de l’unité de contrôle**



**Testbench pour ALU**

library IEEE;

use IEEE.STD\_LOGIC\_1164.all; use IEEE.STD\_LOGIC\_UNSIGNED.all;

entity testbench\_ALU is

end;

architecture test of testbench\_ALU is

component alu

port (a, b: in STD\_LOGIC\_VECTOR(31 downto 0);

f: in STD\_LOGIC\_VECTOR (5 downto 0);

shamt: in STD\_LOGIC\_VECTOR(4 downto 0);

z, o : out STD\_LOGIC;

y: out STD\_LOGIC\_VECTOR(31 downto 0));

end component;

signal a, b: STD\_LOGIC\_VECTOR(31 downto 0);

signal f: STD\_LOGIC\_VECTOR (5 downto 0);

signal shamt: STD\_LOGIC\_VECTOR(4 downto 0);

signal z, o : STD\_LOGIC;

signal y: STD\_LOGIC\_VECTOR(31 downto 0);

begin

dut: alu port map (a, b, f, shamt, z, o, y);

process begin

a <= X"80000000";

shamt <= "00001";

-- sll

b <= X"00000001";

f <= "000000";

wait for 10 ns;

assert y = X"00000010";

report "sll failed";

wait for 20 ns;

b <= X"7fffffff";

-- A + B

f <= "100000";

wait for 10 ns;

assert y = X"ffffffff";

report "add failed";

wait for 20 ns;

-- A - B

f <= "100010";

wait for 10 ns;

assert y = X"00000001";

report "sub failed";

wait for 20 ns;

-- A and B

f <= "100100";

wait for 10 ns;

assert y = X"00000000";

report "and failed";

wait for 20 ns;

-- A or B

f <= "100101";

wait for 10 ns;

assert y = X"ffffffff";

report "or failed";

wait for 20 ns;

-- A xor B

f <= "100110";

wait for 10 ns;

assert y = X"ffffffff";

report "xor failed";

wait for 20 ns;

-- A nor B

f <= "100111";

wait for 10 ns;

assert y = X"00000000";

report "nor failed";

wait for 20 ns;

-- A SLTU B

f <= "101011";

wait for 10 ns;

assert y = X"00000000";

report "sltu failed";

wait for 20 ns;

-- A SLT B

f <= "101010";

wait for 10 ns;

assert y = X"00000000";

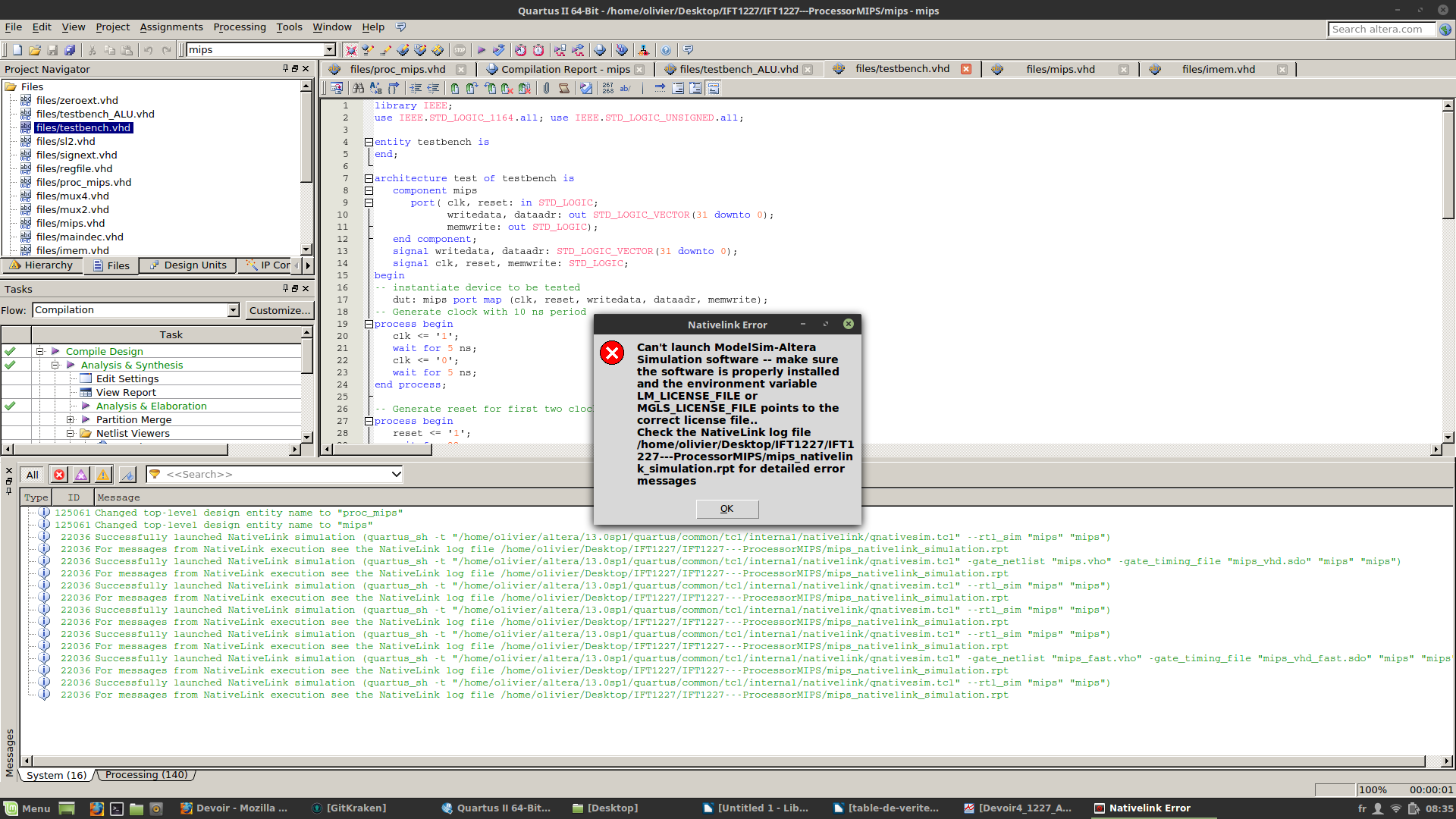
report "slt failed";

wait for 10 ns;

end process;

end;

**Note : Nous n’avons pas été en mesure de simuler les Testbenchs pour ce qui semble être une erreur de licence.**

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