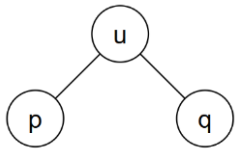
CS 516000 FPGA Architecture & CAD

Homework 4 (Due: 2024/12/09)

1. (a) Based on the Boolean function of *Conn(A)* for SAT-based detail routing in lecture note p.10 of Unit13, draw a possible structure of switch block (1, 3).
   (b) Other than exponentially increasing runtime for large instances, what is the biggest disadvantage of SAT-based detail routing?

2. Consider the FPGA architecture shown on p.13 of Unit 12. Suppose the resource requirement of modules p and q are <12, 1, 2> and <7, 0, 1>, respectively.
   (a) Give the (width, height) of each element in the irreducible realization list $L_p(0,0)$.

   (b) Compute IRL $L_u(0,0)$, where u is an internal node with vertical cut in a slicing tree.

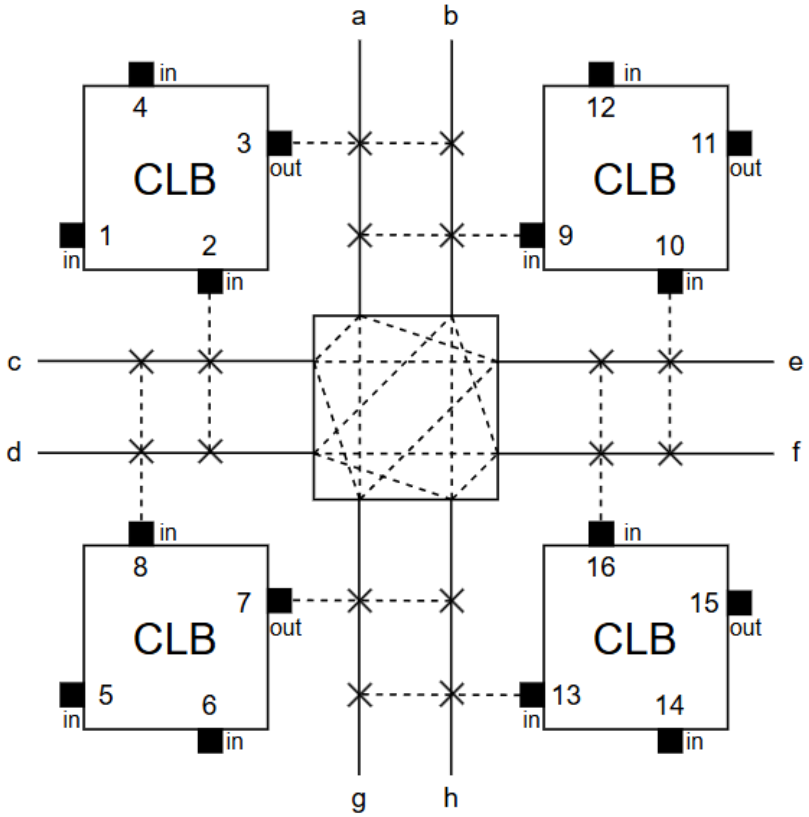


3. The following figure shows part of an FPGA.
   (a) Find a feasible routing solution for two 3-pin nets, one connecting pin set {3, 8, 9} and the other connecting pin set {7, 10, 13}.
   (b) Construct a partial routing resource graph consisting of nodes for pins 2, 3, 7, 8, 9, 10, 13, 16 and wire segments a-h.

   (c) The VPR router may generate the routing solution 3→b→h→13 for net (3, 13)

   and the routing solution 7→h→f→16 for net (7, 16) in the first iteration. Describe

   how VPR will resolve their conflicts in subsequent iterations.


a
b
in
4
3
CLB
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1
in
2
in
in
12
11
CLB
out
9
in
10
in
c
e
d
f
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8
7
CLB
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5
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6
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16
15
CLB
out
13
in
14
in
g
h