Problem B: Power and Timing Optimization Using Multibit Flip-Flop

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Q&A

Q1. Here are some questions about the ICCAD2024 contest, Problem B:

1. Could you give a formulated definition about the function TNS(), like the relation between TNS() and DisplacementDelay, QpinDelay, TimingSlack.
2. In the paper, part 4: "Inst C1 FF1 15 20" may be wrong. Not 15 but 10. If so, two lines need revision.
3. No data range, like: 0 <= the number of flip-flops <= 1e5, and I think every variable needs data range.
4. Can routing circuit overlap? (wire connections between each pair of pins)

A1.

1. In each testcase we will give out pin delay information. This would be a reference value for contestants to optimize. The new timing delay would be related to how much displacement the contestant made, and also the increase or decrease of QpinDelay.
   Taking one single-bit flip-flop FF_0 for example, let WL_0^Q be the original testcase' half-perimeter wirelength of the Q pin of FF_0, and δ_0 be QpinDelay of the FF_0. Should the contestants' submitted result displaced FF_0 to a new location, the new wirelength delay slow down by DisplacementDelay * ($WL_0^{Q\prime} - WL_0^Q$), where WL_0^Q stands for the new wirelength of the Q pin of the displaced FF_0; If FF_0 is changed to another flip-flop FF_0' in the submitted result, with δ_0' being the new QpinDelay, the increased gate delay would be δ_0' - δ_0.
   In the end, the delay would be propagated to the next stage of flip flop FF_N's D pin, where N denotes the next level. Let WL_N^D be the half-perimeter wirelength of the D pin of FF_N, and S_{FFN} be the original slack of FF_N. The new D-pin slack for FF_N, which we denote it as S_{FFN}', is calculated as follows:
   $S_{FFN}' = S_{FFN} + (\delta_0 - \delta_0') + \text{DisplacementDelay} * (WL_0^Q - WL_0^{Q\prime}) + \text{DisplacementDelay} * (WL_N^D - WL_N^{D\prime})$

Where $WL_N^{D\prime}$ stands for the new half-perimeter wirelength of the D pin of FF_N', if FF_N is displaced to a new place or swapped to FF_N'.

2. Yes, you are right. It should be 10. We will revise the statements.
3. Thanks for your suggestion. We do not intend to provide the data range from each value for now. Contestants are expected to take care of program robustness by accommodating INT_MAX for each integer and DBL_MAX for each floating number.
4. We are not asking the contestants to do routing for this problem. Contestants just need to output the netlist connectivity information and make sure the output netlist is functionally equivalent to the input network.

Q2. I am writing to request further clarification regarding the delay calculation for Problem B in the contest materials.

Upon reviewing the provided information, it seems that the "original and new pin location" and the slack calculation of each net is not clearly formulated. It would be beneficial if you could provide a specific example to illustrate the formulation.

I would greatly appreciate your assistance in providing additional explanation on these definitions to ensure clarity in my understanding of the problem.

A2. In each testcase we will give out pin delay information. This would be a reference value for contestants to optimize. The new timing delay would be related to how much displacement the contestant made, and also the increase or decrease of QpinDelay.

Taking one single-bit flip-flop FF_0 for example, let WL_0^Q be the original testcase' half-perimeter wirelength of the Q pin of FF_0, and δ_0 be QpinDelay of the FF_0. Should the contestants' submitted result displaced FF_0 to a new location, the new wirelength delay slow down by DisplacementDelay * ($WL_0^{Q\prime} - WL_0^Q$), where WL_0^Q stands for the new wirelength of the Q pin of the displaced FF_0; If FF_0 is changed to another flip-flop FF_0' in the submitted result, with δ_0' being the new QpinDelay, the increased gate delay would be δ_0' - δ_0.

In the end, the delay would be propagated to the next stage of flip flop FF_N's D pin, where N denotes the next level. Let WL_N^D be the half-perimeter wirelength of the D pin of FF_N, and S_{FFN} be the original slack of FF_N. The new D-pin slack for FF_N, which we denote it as S_{FFN}', is calculated as follows:

$S_{FFN}' = S_{FFN} + (\delta_0 - \delta_0') + \text{DisplacementDelay} * (WL_0^Q - WL_0^{Q\prime}) +$

DisplacementDelay * ($WL_N^D - WL_N^{D\prime}$)
Where $WL_N^{D\prime}$ stands for the new half-perimeter wirelength of the D pin of FF_N', if FF_N is displaced to a new place or swapped to FF_N'.

Q3. Hello, i want to ask about if there exist multi-bit flip flops in the initial cell placement or it just only have one bit flip flops?
Thanks.

A3. Input may contain both single-bit flip-flops and multi-bit flip-flops.

Q4. Hello, i have few more question about question problem B!

1. How to calculate TNS for each flip flop? Is there a formula in terms of the given **Q pin delay**, **TimingSlack D/Q** and the **DisplacementDelay**?
2. Is it means **clock to Q delay** for **Q pin delay**?
3. Will it have negative slack in the given intput?
4. In the initial given placement, does it include combinational logic cells such as AND gate, OR gate etc. Or it only contains flip flops?
5. What does the width and height mean for Placement row? Does it mean the placement grid? For instance, if the Placement row's width and height is 2 and 10, the placement grid width and height will be 2 and 10, am i right?

A4.

1. In each testcase we will give out pin delay information. This would be a reference value for contestants to optimize. The new timing delay would be related to how much displacement the contestant made, and also the increase or decrease of QpinDelay.
   Taking one single-bit flip-flop FF_0 for example, let WL_0^Q be the original testcase' half-perimeter wirelength of the Q pin of FF_0, and δ_0 be QpinDelay of the FF_0. Should the contestants' submitted result displaced FF_0 to a new location, the new wirelength delay slow down by DisplacementDelay * ($WL_0^{Q\prime} - WL_0^Q$), where WL_0^Q stands for the new wirelength of the Q pin of the displaced FF_0; If FF_0 is changed to another flip-flop FF_0' in the submitted result, with δ_0' being the new QpinDelay, the increased gate delay would be δ_0' - δ_0.
   In the end, the delay would be propagated to the next stage of flip flop FF_N's

D pin, where N denotes the next level. Let WL_N^D be the half-perimeter wirelength of the D pin of FF_N, and S_{FFN} be the original slack of FF_N. The new D-pin slack for FF_N, which we denote it as S_{FFN}', is calculated as follows:

$S_{FFN}' = S_{FFN} + (\delta_0 - \delta_0') + \text{DisplacementDelay} * (WL_0^Q - WL_0^{Q\prime}) + \text{DisplacementDelay} * (WL_N^D - WL_N^{D\prime})$

Where $WL_N^{D\prime}$ stands for the new half-perimeter wirelength of the D pin of FF_N', if FF_N is displaced to a new place or swapped to FF_N'.

2. Yes, the Q pin delay means the clock-to-Q delay.
3. Input could have negative slacks.
4. The initial given placement will include the combinational logic cells, but these combinational cells would be marked as the fixed points which means we don't want contestants to move these combinational cells, only need to focus on sequential cells.
5. Sorry for the confusion. We will update the statements to make them clearer. The width and height of PlacementRow are the cell site width and cell site height, and we will also give the site count. One placement row is composed of multiple cell sites, which means that the height of PlacementRow is the height of a cell site and the width of PlacementRow is the sum of all cell site widths.

Q5. Hello, I want some clarification regarding problem B "Power and Timing Optimization Using Multibit Flip-Flop", specifically regarding the TNS (total negative slack).

In the problem description, in regards to the flip-flop delays, we are given: 1. Displacement Delay Coefficient, 2. the Q-pin delay of each flip-flop, and 3. the timing slack of each flip-flop's pins. However, the problem statement did not explicitly mention how TNS is calculated with the given information.

I have the following questions:

1. How is TNS calculated using the given delays?
2. Is Q-pin delay referring to clock-to-Q propagation delay?
3. I believe there is a typo in the sample input example. The x-axis coordinates for FF C1 and C2 should be 10, not 15.

A5.

1. In each testcase we will give out pin delay information. This would be a reference value for contestants to optimize. The new timing delay would be related to how much displacement the contestant made, and also the increase or decrease of QpinDelay.
   Taking one single-bit flip-flop FF_0 for example, let WL_0^Q be the original testcase' half-perimeter wirelength of the Q pin of FF_0, and δ_0 be QpinDelay of the FF_0. Should the contestants' submitted result displaced FF_0 to a new location, the new wirelength delay slow down by DisplacementDelay * ($WL_0^{Q\prime} - WL_0^Q$), where WL_0^Q stands for the new wirelength of the Q pin of the displaced FF_0; If FF_0 is changed to another flip-flop FF_0' in the submitted result, with δ_0' being the new QpinDelay, the increased gate delay would be δ_0' - δ_0.
   In the end, the delay would be propagated to the next stage of flip flop FF_N's D pin, where N denotes the next level. Let WL_N^D be the half-perimeter wirelength of the D pin of FF_N, and S_{FFN} be the original slack of FF_N. The new D-pin slack for FF_N, which we denote it as S_{FFN}', is calculated as follows:
   $S_{FFN}' = S_{FFN} + (\delta_0 - \delta_0') + \text{DisplacementDelay} * (WL_0^Q - WL_0^{Q\prime}) + \text{DisplacementDelay} * (WL_N^D - WL_N^{D\prime})$
   Where $WL_N^{D\prime}$ stands for the new half-perimeter wirelength of the D pin of FF_N', if FF_N is displaced to a new place or swapped to FF_N'.
2. Yes, the Q pin delay means the clock-to-Q delay
3. Yes, you are right. It should be 10. We will revise the statements.

Q6. Hello, what I am asking about is Question B on the seventh page, concerning the calculation method of timing slack. I've attached a screenshot of the description on this page. My question is, the prompt doesn't provide the calculation method for TNS (Total Negative Slack) in the final cost metrics. It only provides parameters and descriptions related to it, but it's clearly stated for other parts. So, I'm wondering if this part has been overlooked.

Timing slack and delay information. For each instance pin in the design we will give out a timing slack information. The delay model is formulated by displacement delay and Q-pin delay. The definition of displacement is the Manhattan distance between the original pin location and the new pin location. For any cell displacement we times the coefficient with the displacement distance to get the displacement delay. For every flip-flop gate defined in the library we define a Q-pin delay for it.

Syntax

DisplacementDelay <coefficient>

QpinDelay <libCellName> <delay>

TimingSlack <instanceCellName> <PinName> <slack>

Example

DisplacementDelay 0.01

QpinDelay FF1 1

QpinDelay FF2 3

QpinDelay FF2A 2

TimingSlack C1 D 1

TimingSlack C1 Q 0

TimingSlack C2 D 1

TimingSlack C2 Q 0

A6. In each testcase we will give out pin delay information. This would be a reference value for contestants to optimize. The new timing delay would be related to how much displacement the contestant made, and also the increase or decrease of QpinDelay.

Taking one single-bit flip-flop FF_0 for example, let WL_0^Q be the original testcase' half-perimeter wirelength of the Q pin of FF_0, and δ_0 be QpinDelay of the FF_0. Should the contestants' submitted result displaced FF_0 to a new location, the new wirelength delay slow down by DisplacementDelay * ($WL_0^{Q\prime} - WL_0^Q$), where WL_0^Q stands for the new wirelength of the Q pin of the displaced FF_0; If FF_0 is changed to another flip-flop FF_0' in the submitted result, with δ_0' being the new QpinDelay, the increased gate delay would be δ_0' - δ_0.

In the end, the delay would be propagated to the next stage of flip flop FF_N's D pin, where N denotes the next level. Let WL_N^D be the half-perimeter wirelength of the D pin of FF_N, and S_{FFN} be the original slack of FF_N. The new D-pin slack for FF_N, which we denote it as S_{FFN}', is calculated as follows:

$S_{FFN}' = S_{FFN} + (\delta_0 - \delta_0') +$ DisplacementDelay * $(WL_0^Q - WL_0^{Q\prime}) +$ DisplacementDelay * $(WL_N^D - WL_N^{D\prime})$

Where $WL_N^{D\prime}$ stands for the new half-perimeter wirelength of the D pin of FF_N', if FF_N is displaced to a new place or swapped to FF_N'.

Q7. Regarding the cost metric mentioned in the document, considering that better results in the evaluation can lead to higher scores, I would like to inquire whether the cost metric can transform the results into larger values when the timing, power, and area of the placement are all minimized. In other words, does the value obtained from the cost metric increase as the placement results improve?
If so, when the D component in the cost metric increases, the penalty incurred should be larger. Why does it seem that in this scenario, higher cost metric values are achieved?

Furthermore, is it possible to release the internal computations of $TNS(i)$, $Power(i)$, and $Area(i)$? Or would you provide evaluators or references for participants to conduct self-assessment in this regard?

A7. The cost metrics are given along with each testcase. It does not change with placement results.

In each testcase we will give out pin delay information. This would be a reference value for contestants to optimize. The new timing delay would be related to how much displacement the contestant made, and also the increase or decrease of QpinDelay.
Taking one single-bit flip-flop FF_0 for example, let WL_0^Q be the original testcase' half-perimeter wirelength of the Q pin of FF_0, and δ_0 be QpinDelay of the FF_0. Should the contestants' submitted result displaced FF_0 to a new location, the new wirelength delay slow down by DisplacementDelay * ($WL_0^{Q\prime} - WL_0^Q$), where WL_0^Q stands for the new wirelength of the Q pin of the displaced FF_0; If FF_0 is changed to another flip-flop FF_0' in the submitted result, with δ_0' being the new QpinDelay, the increased gate delay would be δ_0' - δ_0.
In the end, the delay would be propagated to the next stage of flip flop FF_N's D pin, where N denotes the next level. Let WL_N^D be the half-perimeter wirelength of the D pin of FF_N, and S_{FFN} be the original slack of FF_N. The new D-pin slack for FF_N, which we denote it as S_{FFN}', is calculated as follows:
$S_{FFN}' = S_{FFN} + (\delta_0 - \delta_0') +$ DisplacementDelay * ($WL_0^Q - WL_0^{Q\prime}$) + DisplacementDelay * ($WL_N^D - WL_N^{D\prime}$)
Where $WL_N^{D\prime}$ stands for the new half-perimeter wirelength of the D pin of FF_N', if FF_N is displaced to a new place or swapped to FF_N'.

Q8. I have a question about the input "PlacementRows" mentioned at the end of p.6 of the spec. According to the description, the placement rows would cover the whole die, and all instances must be placed on the rows. However, the rowWidth is 2 in this example, which is too small for both 1-bit and 2-bt FF, given in the same example. Does that mean we can only place the FFs on the coordinates
(x, y) = (2k, 10c), for k = 0 ~ DieWidth/2- 1, c = 0 ~ DieHeight/10 - 1 in this example? Or it's just a typo; the rowWidth should be equal to the DieWidth, which is 50 in this case.

A8. Sorry for the confusion. We will update the statements to make them clearer. The width and height of PlacementRow are the cell site width and cell site height, and we will also give the site count. One placement row is composed of multiple cell sites, which means that the height of PlacementRow is the height of a cell site and the width of PlacementRow is the sum of all cell site widths.

The placement rows would cover the whole placement region but may not cover the whole die. All instances must be placed on the row, and all the instances width is guaranteed to be n * cell site height (n is integer and n >= 1).

Q9. I am writing to inquire about some questions about problem B as described below.

1. I'd like to inquire whether there is a discrepancy in the coordinates labeled in the example diagram on page 9 of the document. (The coordinates labeled in the bottom left corner do not match those described on page 10.)
2. In the example diagram on page 9, what is the significance of the dashed square grids marked? They do not correspond to the "bin" and "row" as described in the example.
3. Do flip-flops need to be placed with their edges aligned to the rows (both horizontally and vertically) when placed?

A9.

1. It is typo. The x-coordinate of C1 and C2 should be 10. We will revise the statements.
2. Dashed square grids are an illustration of cell sites. The example may have some typos; we will update the example to make it more clear.
3. Please refer to the Evaluation part. Each cell needs to be placed on site and no cell could be placed overlapping another.

Q10. Hello, I'm one of the participant from ICCAD24' and currently reading the spec for question B in ICCAD contest in 2024. But I have some questions concerning the spec.

1. Is that guaranteed that the Die'S width and height is divisible by the bin width and heights ?
2. For the TNG(i), we are aimed to minimized the total negative stack of the flip flop. But with the given information without hold time and the time budget, how do we know that if the instance is positive slack or negative slack ? Is there any formula that we can determine if that's the case or not ?
3. Will it be in the case that two or more output from flip-flop map(connect) to the one input of the flip-flop ? (I think it may be the case that 1 output connect to several input, but will it be the case vice versa ?)

A10.

1. No, we are not guaranteed that the die width and height are divisible by the bin width and height. We have defined PlacementRows within DieSize, so even though the bins at the top and the right boundary might be smaller if the die width or height are not divisible by bin width and height, it would not be a placeable area.
2. In each testcase we will give out pin delay information. This would be a reference value for contestants to optimize. The new timing delay would be related to how much displacement the contestant made, and also the increase or decrease of QpinDelay.

   Taking one single-bit flip-flop FF_0 for example, let WL_0^Q be the original testcase' half-perimeter wirelength of the Q pin of FF_0, and δ_0 be QpinDelay of the FF_0. Should the contestants' submitted result displaced FF_0 to a new location, the new wirelength delay slow down by DisplacementDelay * ($WL_0^{Q\prime} - WL_0^Q$), where WL_0^Q stands for the new wirelength of the Q pin of the displaced FF_0; If FF_0 is changed to another flip-flop FF_0' in the submitted result, with δ_0' being the new QpinDelay, the increased gate delay would be δ_0' - δ_0.

   In the end, the delay would be propagated to the next stage of flip flop FF_N's D pin, where N denotes the next level. Let WL_N^D be the half-perimeter wirelength of the D pin of FF_N, and S_{FFN} be the original slack of FF_N. The new D-pin slack for FF_N, which we denote it as S_{FFN}', is calculated as follows:

   $S_{FFN}' = S_{FFN} + (\delta_0 - \delta_0') + \text{DisplacementDelay} * (WL_0^Q - WL_0^{Q\prime}) + \text{DisplacementDelay} * (WL_N^D - WL_N^{D\prime})$

Where $WL_N^{D\prime}$ stands for the new half-perimeter wirelength of the D pin of FF_N', if FF_N is displaced to a new place or swapped to FF_N'.

3. The output of flip-flops are connected to either combinational gates of later sequential gates, so it is possible that the outputs of multiple single-bit flip-flops are connected to the same multi-bit flip-flop as its inputs. Multi-fanout nets are possible.

Q11. I have recently reviewed the documentation for Problem B of the IC/CAD Contest 2024 and have a few inquiries regarding the problem statement:

1. Regarding the Cell Library, if there are 1-bit, 2-bit, and 4-bit Flip-Flops available, is it permissible during the banking process to merge two 1-bit Flip-Flops into one 4-bit Flip-Flop, while retaining four empty pins (2 sets of D and Q)?

2.
(1) Regarding displacement delay, is it true that the delay is calculated based on the displacement of pins, meaning that any displacement of a cell results in an increase in displacement delay?

If the distance between pins of the same net decreases after relocation, does this lead to a reduction in displacement delay? Please clarify this section further.
(2) As for timing slack, it represents the current timing situation. How to calculate the new timing slack using the modified displacement delay and Q-pin delay?

3.
(1) Does "Uniform Bin" imply that all bins have the same BinMaxUtil and size?
(2) Can bins have non-square shapes?
(3) Is it possible for bins to not be fully accommodated within the layout? (For example, when the longer side of the die can only accommodate 2.5 bins)

4. Are there scenarios where multi-row-height cells occur?

5. In "PlacementRows 0 0 2 10", does the '2' signify that cells' x-coordinates can only be placed at multiples of 2?

6. In the "Format of Output Data Syntax," under CellInst, the format is stated as

"Inst <instName> <locationX> <locationY> <orientation>."

(1) Does this mean cells can only accept horizontal flipping, or are there other rotation options?

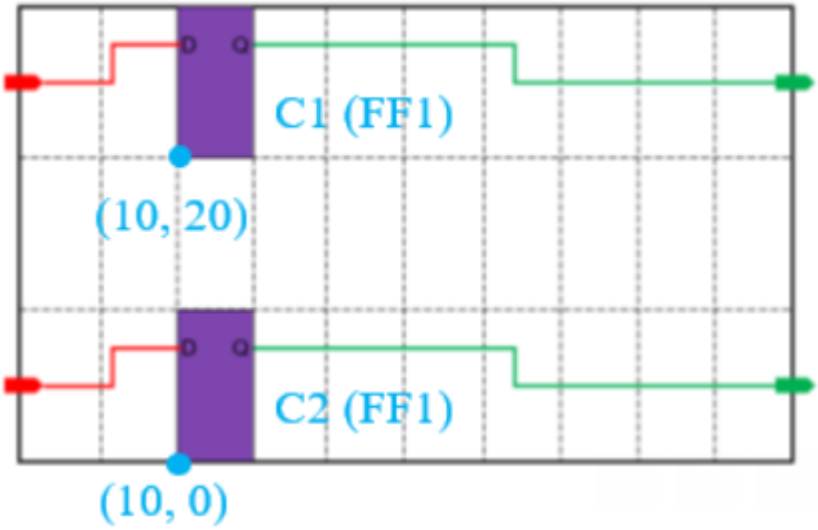
(2) How should the <orientation> be represented to indicate the rotation status?

Furthermore, there is a correction regarding the Example provided. The coordinates of the objects should be adjusted as follows:

NumInstances 2

Inst C1 FF1 15 20 -> Inst C1 FF1 10 20

Inst C2 FF1 15 0 -> Inst C1 FF1 10 0



I would greatly appreciate it if you could take the time to address these queries. Thank you for your attention to this matter.

A11.

1. As long as contestants could provide a complete mapping list of how the flip-flops are changed, we allow logically equivalent solutions.
2. In each testcase we will give out pin delay information. This would be a reference value for contestants to optimize. The new timing delay would be related to how much displacement the contestant made, and also the increase or decrease of QpinDelay.

   Taking one single-bit flip-flop FF_0 for example, let WL_0^Q be the original testcase' half-perimeter wirelength of the Q pin of FF_0, and δ_0 be QpinDelay of the FF_0. Should the contestants' submitted result displaced FF_0 to a new location, the new wirelength delay slow down by DisplacementDelay * ($WL_0^{Q\prime} - WL_0^Q$), where WL_0^Q stands for the new wirelength of the Q pin of the displaced FF_0; If FF_0 is changed to another flip-flop FF_0' in the submitted

result, with δ_0' being the new QpinDelay, the increased gate delay would be δ_0' - δ_0.

In the end, the delay would be propagated to the next stage of flip flop FF_N's D pin, where N denotes the next level. Let WL_N^D be the half-perimeter wirelength of the D pin of FF_N, and S_{FFN} be the original slack of FF_N. The new D-pin slack for FF_N, which we denote it as S_{FFN}', is calculated as follows:

$S_{FFN}' = S_{FFN} + (\delta_0 - \delta_0') + \text{DisplacementDelay} * (WL_0^Q - WL_0^{Q\prime}) + \text{DisplacementDelay} * (WL_N^D - WL_N^{D\prime})$

Where $WL_N^{D\prime}$ stands for the new half-perimeter wirelength of the D pin of FF_N', if FF_N is displaced to a new place or swapped to FF_N'.

3. (1) Yes
   (2) It depends on the dimensions of BinWidth and BinHeight.
   (3) Max placement utilization ratio defined in this contest divides the Die Area of the design into bins whose dimensions are (BinWidth, BinHeight). The first bin starts from (<lowerLeftX>, <lowerLeftY>) of DieSize, and repeats with (BinWidth, BinHeight) throughout the DieSize.
4. Yes, the cell height may be n * row height (n is an integer and n >= 1).
5. Please refer to the Evaluation part. Each cell needs to be placed on site and no cell could be placed overlapping another.
6. We have revised the problem formulation and orientation is not considered in this contest.
7. Yes, you are right. It should be 10. We will revise the statements.

Q12. We are writing to ask some questions for Problem B:

1. If a FFN has multiple predecessor FF0s (e.g. for a 2-NAND gate, two input pins connect to 2 predecessor FF0s respectively and the output pin connects to successor FFN), how to determine the delta QpinDelay (δ0 – δ0') in slack calculation?
2. Would it be better if there were explicit labels for logic gates I/O pins so we can check the relationship between FF0 and FFN?
3. It seems that ./sanity file checks the mapping information for all FFs. We are not sure that if an FF is not mapped into another form of FF, should we still put it into the output file (such as "C1/D map C1/D")?
4. In the sample case, 'clk' are lowercase in the INPUT declaration and uppercase in line 43, which is difficult to parse.
5. How to identify which net indicate a clock field? Is it by the keyword 'clk',

'CLK', or other labels?

A12.

1. We calculate the problem with the larger one.
2. Thank you for your suggestion. Each pin for logic gates has a prefix of IN* or OUT* to identify if it is an input or output pin.
3. Yes. Even if the output is using the same flip-flop type, contestant should still list the mapping.
4. The input will be consistent in the same case.
5. We will make them all aligned in the same case. Output should use the same case as input. Cell name is not limited to upper case.

Q13. I would also like to ask if other test cases would be available soon, as there is only one toy case available.
Besides, I would like to ask in the toy case, it seems that the banking of two FFs does not show any benefits compared to regular papers,
whereas using MBFFs should show power/area advantages. Will this phenomenon need to be considered?
For example, in the toy case provided, the area of banking two FFs results in 2 times in terms of area cost:

```
FlipFlop 1 SVT_FF_1 741 480 3
...
FlipFlop 2 SVT_FF_2 798 1960 5
...
```

Regarding power, the cost of using an MBFF is also approximately 2 times compared to the original cost of using 2 FFs:

```
GatePower SVT_FF_1 1.4781e+01
GatePower SVT_FF_2 5.2515e+01
```

Thanks for your clarification.

A13. Thank you for your query. New testcase has been released. Please refer to the newly released testcase.

Q14. I have noticed that the input format specification does not provide explicit information regarding the driving source of each flip-flop's D-pin. This may lead to

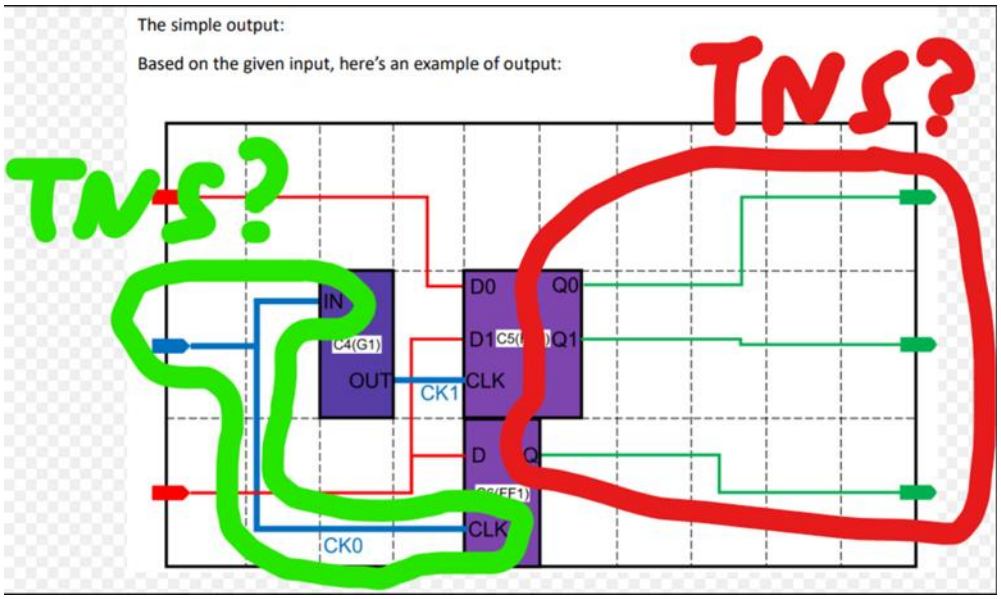
difficulties in computing the modified slack of each flip-flop (e.g. nets connecting a D-pin with multiple pins, multi-input combinational gates, determining the functionalities of each pin of a flip-flop cell)
Could you please provide more information to clarify the above issues?

A14. In this contest we are focusing on the wirelength model for timing delay. We are formulating this problem in a way that contestants could compete in this simplified sandbox environment to focus on the objective optimization.

Q15. Additionally, in the sample case provided on the website, the height of cell SVT_FF_2 is listed as 1960, which is not an integer multiple of the cell site height and appears to be extraordinarily large. Could you confirm if there was a typo in this instance?

A15. Cell heights are not necessarily an integer multiple of site height. Please refer to Figure 4 for the definition of legality.

Q16. About TNS, I read the Q&A document and I still have something to ask. Do the TNS only happen within nets between FFs, or it also happens between the input/output pins and the FFs? Furthermore, we only need to consider the D pins and Q pins, not the CLK pins, right?



A16. For our testcases, INPUT and OUTPUT nets would also have TNS.
Yes. The testcase would give out TimingSlack for each D pin and QpinDelay for each flip-flop.

Q17. Here are 4 questions about the 2024 ICCAD Problem B:

1: How should the hypernet HPWL calculation be handled when calculating displacement delay? For example, if there exists a net that connects to the output of comb1 cell, the input of comb2 cell, and the D pin of the flip-flop, how should the WL_D for the flip-flop be calculated?

2: Similar to Q1, if a comb cell has 2 inputs from different flip-flops, how should the WL be calculated for this case?

3: Could you provide the pin definition list for both the clk name reservation and the pin names(either input or output) for both the comb cells and flip-flop cells in the cell library?

4: Will multiple clock signals appear in the test case?

A17.

1. We are defining the pin-to-pin connection from the previous register or INPUT to the next register. In this case, it should be the HPWL from the output of comb1 to the D pin.
2. If a comb cell has 2 inputs from different flip-flops, they should have been two different nets. They are calculated independently.
3. Please refer to the newly released testcase for all the inputs pin names.
4. All clock nets will start with the name CLK.

Q18. I have more questions to ask:

1. In case1, that is, the sample testcase, there are two lines of <PlacementRows>, shouldn't it have only one <PlacementRows> line?
2. In the Q&A section, you mentioned that the size of the bins might not be the same. Can I place FFs in the smaller bins?

A18.

1. There can be multiple lines of PlacementRows
2. PlacementRows might be different. The constraint for legality is to align the bottom left corner. Please refer to Figure 4.

Q19. Can you provide a larger case, the current one has some limitations?

A19. Thank you for your interest. We have release testcase1.

Q20. We noticed the response to Q11.4 in the Q&A for Problem B, which states, "Yes, the cell height may be n * row height (n is an integer and n >=1)."
However, we found that in case 1 given in Problem B, the "PlacementRows 480 3600 57 240 395" indicates that the row height should be 240.
And "FlipFlop 2 SVT_FF_2 798 1960 5" shows that the height of this Flip-Flop is 1960, which is not a multiple of 240.
Could you please clarify if we have a misunderstanding?

A20. Cell heights are not necessarily an integer multiple of site height. Please refer to Figure 4 for the definition of legality.

Q21. Do we need to consider positive slack for calculating the sum of TNS in the cost metrics ?

A21. No. The cost only considers negative slack.

Q22. Are all the D and Q pins on SBFFs named "D" and "Q"? Are all the D and Q pins on MBFFs named "Di" and "Qi"? Furthermore, are all the clk pins named "CLK"?

A22. Yes. Please follow the format of each testcase and align these prefixes.

Q23. I would like to further ask what does the pin location X and Y mean in the gate and FF library, is it the relative position to the corner, or the center or the absolute position? Because it seems that the position is out of the bound given the width and height of the gate / FF instance in the recently released case:

FlipFlop 4 FF47 867 84 9
Pin Q0 7230 1260
Pin Q1 7230 3360

Pin Q2 7230 5460
Pin Q3 7230 7560
Pin D0 90 1540
Pin D1 90 3080
Pin D2 90 5740
Pin D3 90 7280
Pin CLK 1875 2520
Gate G1 459 42 5
Pin OUT1 90 1260
Pin OUT2 90 3640
Pin IN1 3215 1040
Pin IN2 3895 760
Pin IN3 90 3080

A23. Thanks for your input. We are revising the testcase and will update soon.

Q24. The naming convention for the pins of multi-bit flip-flops is a bit unclear to us. For the D pins, is the naming sequence simply D0, D1, D2, and so on? Is it similar to the Q pins as well? Does Di correspond to Qi? Is the clock pin conventionally named CLK? Additionally, is there a way to tell from the pin names of a combinational gate whether they are input or output? For example, in the documentation, the examples are named IN and OUT.
Regarding the slack example, when there is only one path, how should we calculate slack if multiple Q pins are connected to one D pin? Should we take the sum or the maximum? If we take the maximum, how can we determine which is the critical path?

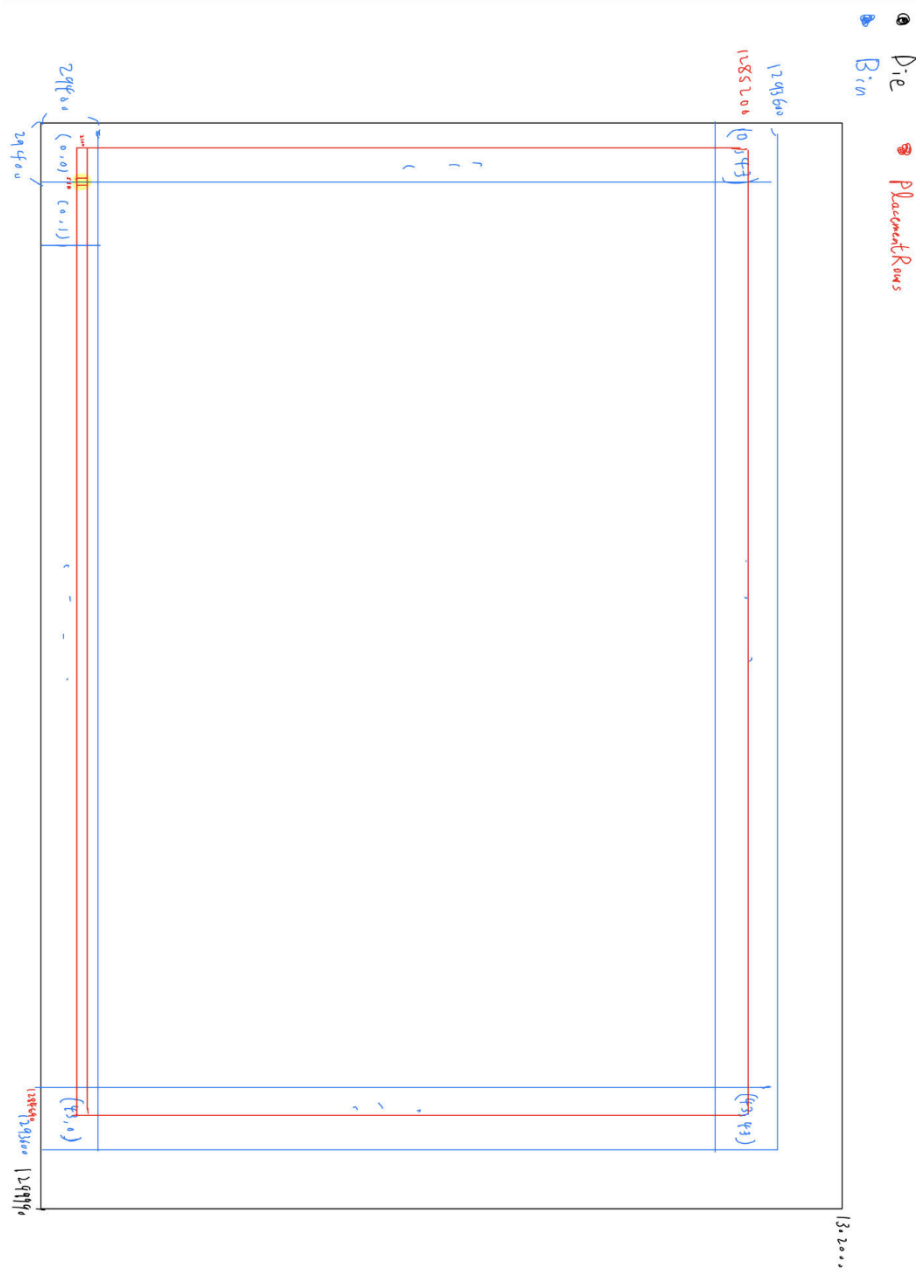
A24. FlipFlop has Q0, Q1, Q2, …, D0, D1, D2, … etc. Di is corresponding to Qi. Clock pin is conventionally named CLK or clk. You can tell a combinational gate's pin name by its prefix. It would be IN* or OUT*, in either upper or lower case.

Q25. When a D pin is arrived by multiple Q paths, do we take the min or max arrival time of them?

A25. Sorry, we are not sure what you meant by "D pin is arrived by multiple Q paths". Q pin is the output pin and D pin is the input pin. If a D pin is directly wired to multiple Q pins, the output signal may conflict. If there are multiple timing arcs

arriving to the D pin, take the max arrival time.

Q26. For the new released case(testcase1),
I noticed that there are sites crossing the boundary of bin(0,0) and bin(0,1).
(The bottom-left corner of the attached image shows a rough sketch of this case)



My question is:
In this case, if the site is fully occupied by a cell, does bin(0,1) have to take a portion of the site area into consideration while calculating its bin utility?

A26. As long as the cell overlaps the bin, the overlapping area is considered.

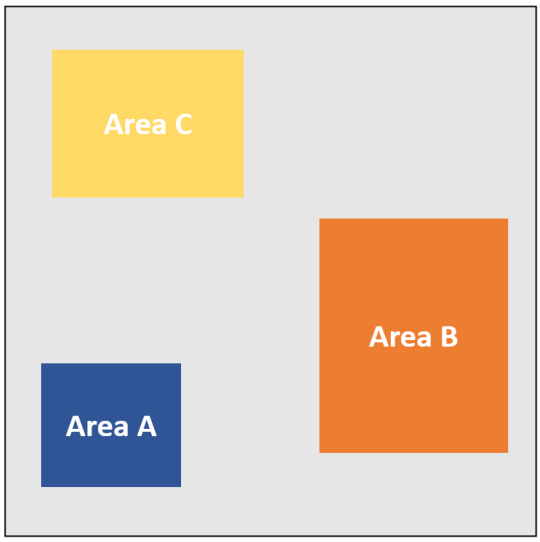
Q27.

1. Is the number of each FF type necessarily the power of 2?
2. Since the initial placement could contain negative slack, I wonder if it is guaranteed to be a good enough solution for the timing condition, and we better preserve its overall structure in the final solution, or is it just an arbitary legal placement?
3. Can two cells share one edge or one corner? Or should every cell be completely disjoint from each other and any shared point between two cells is not allowed?

A27.

1. Not necessary. For example, there might be FF with 6 bits.
2. It is not necessary a good enough solution.
3. Yes. Two cells can share one edge or one corner.

Q28. Hello, I have some question about placement. Is there going to be multiple placement area throughout the die? For example:



If the answer if yes, then how will the input format be for placement rows, will the placement rows sorted by the area or somehow? Also, will the "site hight" be all the same inside one placement area?

A28. Placeable area is defined by the union of all PlacementRows. In another words. As long as the area is within a defined PlacementRows, it is a placeable area. Placement area could also be rectilinear.

Q29. I want to ask that why in testcase1, there are locations larger than FFs' width and height? (like the following situation: 3080>42, 980>42)

```
FlipFlop 1 FF4 663 42 3
Pin Q 90 3080
Pin D 90 980
Pin CLK 2895 700
```

A29. Thanks for your input. We are revising the testcase and will update soon.

Q30. I have another question: The FF info gives us D0, Q0, .. as its pin name, but the net give us IN0, OUT0, ...
Does the D0 means IN0? and Q0 means OUT0? (See following two figs)

```
731   FlipFlop 4 FF42 867 84 9
732   Pin Q0 6975 1260
733   Pin Q1 7740 3080
734   Pin Q2 7740 5460
735   Pin Q3 6975 7560
736   Pin D0 90 1540
737   Pin D1 90 3080
738   Pin D2 90 5460
739   Pin D3 90 7280
740   Pin CLK 1875 3360
```

```
Net net15501 4
Pin C30379/OUT1
Pin C3223/IN3
Pin C3225/IN1
Pin C24534/IN2
```

A30. IN0 and OUT0 are combinational gates' pin names. D0 and Q0 are sequential cell' pin names.

Q31. We are writing to ask some questions related to Problem B:
1. Will you provide a final score evaluator?
2. We see in Q12.1 that if a FFN has multiple predecessor FF0s, we take the larger QpinDelay of FF0. Do we also calculate the DisplacementDelay in this way when there are multiple predecessors?

A31.
1: We are not planning to provide the score evaluator at this stage.
2: Yes.

Q32. I am writing this letter to verify my understanding on the topic previously brought up by other contestants(see the attached picture). In the QA, the answer is to take the maximum delta QpinDelay.
(1)Consider the same scenario described in the picture, suppose FF1 and FF2 are the two distinct predecessor of FF0, and delta QpinDelay(FF1) > delta QpinDelay(FF2) but delta WL0Q(FF1) < delta WL0Q(FF2), which value should I substitute into the SFFN' calculation? Should I substitude max(delta QpinDelay) and max(delta WL0Q), or should I use max(delta QpinDelay + DisplacementDelay*(delta WL0Q)) instead?
(2)I wonder if each D pin in all the FFs are connected to only one input pin, which I figure should be true since otherwise the logic value of D pin will be ambiguous.

Q12. We are writing to ask some questions for Problem B:

1. If a FFN has multiple predecessor FF0s (e.g. for a 2-NAND gate, two input pins connect to 2 predecessor FF0s respectively and the output pin connects to successor FFN), how to determine the delta QpinDelay (δ0 – δ0') in slack calculation?

A32:
1.Consider each as path ("FF1 to FF0" and "FF2 to FF0") as individual timing arc. Calculate each timing arc and take the large one (worst condition).
2: Yes.

Q33. I am writing to confirm the following pin naming formats:
(1) Are the indices for D and Q in all FF all start from 0?
(2) Are the indices for input and output in all gates named INi and OUTi, where i starts from 1?

A33.
(1) Yes.
(2) Yes.

Q34. I have a question about ICCAD 2024 problem B: Multibit Flip-Flop, and I want to check whether my thought is right or wrong.

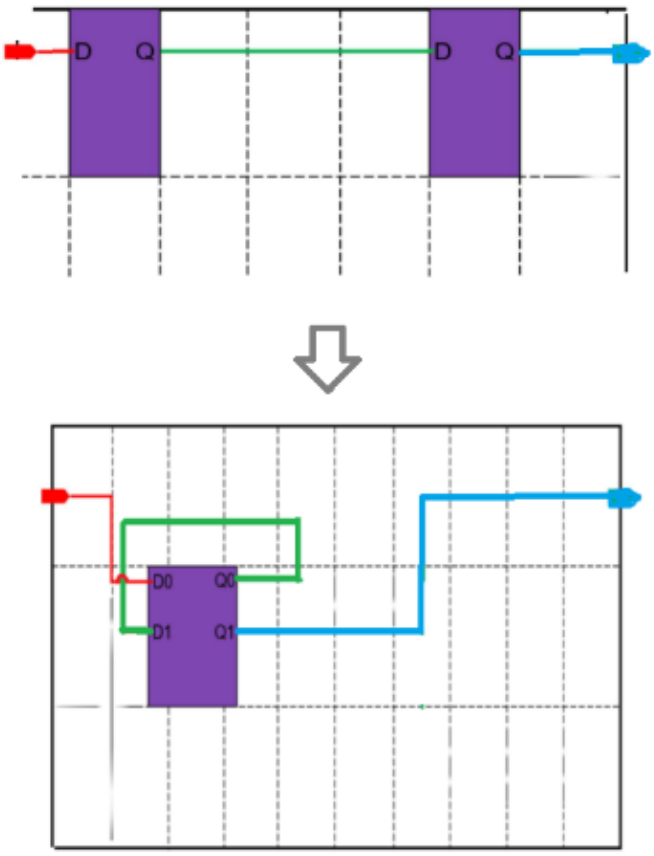
In the PDF pages 12, (5) Evaluation C. mentioned:
" Nets connected to the flip-flops must remain **functionally equivalent** to the data input." Can I suppose that if there is a path that passes through 3 flip-flops, the final

result should also pass through 3 flip-flops whether flip-flops are banking or debunking, that is removing flip-flops is violated in this problem right? We can only banking or debanking flip-flops.

A34. By functionally equivalent we meant that the output circuits from the contestants should be logically equivalent to the input circuits. Contestants are allowed to change, bank, debank, or move sequential flip-flops. Removing flip-flops which resulted in unconnected dangling signal is violating the problem.

Q35.

1. What is the meaning of TimingSlack?
   Is TimeSlack the maximum delay represented by the product of Manhattan distance and coefficient, allowing the lines in front of the D pin to change?
2. Can multiple series-connected triggers be merged into one through banking?
   For example,is the following operation legal?



A35.

1. The meaning of TimingSlack is to represent the margin between data required time and data arrival time. TimingSlack is not the same as delay.
2. It’s legal

Q36. In the cell library syntax
FlipFlop <bits> <flipFlopLibCellName> <libCellWidth> <libCellHeight> <pinCount>
Pin <pinName> <pinLocationX> <pinLocationY>
Can I assume <pinLocationX> and <pinLocationY> are both integers and not floating points?

A36. Yes, x,y are integers.

Q37.

1. Is it a fair assumption to make that the values for alpha,beta,gamma,delta will be fairly uniform across the public testcases as well as the hidden testcases? Or can it be expected that one of these parameters might dominate over the others? If so, is there anything we should know about which factor(timing/power/area) we should be more biased towards?
2. On page 4 of the problem document, the following line has been mentioned "Contestants cannot extend the cell size (or region) to solve the density violation or Flip-Flop overlap issues. The goal is to optimize the multiple objectives: timing and power; without increasing the cell's region or area (die size)."

   What does this exactly imply? Does it mean that upsizing(i.e, changing the drive strength) is not allowed?

3. Will there be macros present in the initial layout? If yes, will they be movable?
4. Are the pin locations relative to the bottom left corner of an instantiated cell?

A37.
1. Timing, power, and area are key metrics for modern chip designs, and trade-offs between each metrics is one of the key point of this competition. We do not encourage contestants to bias their objectives leaning towards any direction that forfeit other objectives.
2. Yes
3. There is fixed gate as explained in the question.
4. Yes

Q38. How to calculate the WLq if the Q pin connects to more than one pin?

A38. Consider an output pin Q and it's loads I1,I2,I3
For calculating Q->Ii, HPWL is determined by Manhattan distance between Q and Ii.

Q39. In page 14, one of the lines mentions "TNS stands for total negative slack. We'll calculate the slack values of each output of flip-flop and accumulate all negative slack values to formulate TNS cost."

However, the equation given allows us to calculate the slack value of the D-pin, i.e the input of the flip-flop, not the output. Am I looking at this correctly? How can the formulation provided be extended to the output pin as well? Also, will slacks of all the input and outpin pins be considered during TNS calculation or will it just be the output pin slack?

A39. Thank you for your inquiry. It should be fixed as Dpin slack. The problem formulation should be updated.

Q40. In problem B, will there be any PlacementRow or cell that is multi-height, e.g., the top-most green cell in Figure 4? Or, for each test case, there will be just "one unified height" for "all PlacementRows and cells"?

A40. It's possible to have placementRows with different heights. Multi-height cell is allowable.

Q41. I have two more questions about B:

1. There is no logic gate present in the case given so far, is it that this design itself does not have logic gates or the provided file will not contain information about the location of the logic gate part.

2. Will the area of the logic gate section be calculated into the BinMaxUtil limit? If so, how will the area of the gate section be given?

A41.

1. The calculation should include the cell's area proportion as described in the problem.
2. Given the length and width of the gate, the area should be computable.

Q42. According to the new definition of timing slack, I have some questions about the timing path.

1. According to the spec, it is possible that more than one Q pin connects to one D pin via a combinational gate. And this may result in multi-timing paths for some D pins, while it has only one slack value. Can we know the slack is from which Q pin? or the pair-wise critical timing path would be given in this case?

2. Would the gate delay of a standard cell be given?

A42.

1. Contestants must calculate the arrival time for multi-timing paths and determine the critical path by themselves. The slack is calculated as the difference between the latest data arrival time and data required time.
2. We assume all combinational gate delays are equal or 0. contestants don't need to consider the combinational gate delay when calculating arrival time.

Q43. I have a question about timing slack. Do we need to consider the change in wire length of the clock (clk) when calculating the slack? For example, in Figures 5 and 6 of your document, clk1 has become shorter. Should we adjust the slack of register FF2 by subtracting a term: displacement_delay * (WL_clk1* - WL_clk1)?

A43. Timing slack calculation in this problem doesn't involve delay of clock pin.

Q44. Do we have to figure out the critical path of Timeslack by ourselves, or will there always be only one path from Flipflop's Qpin -> combinational circuit -> Flipflop's Dpin? Having multiple flipflops' fanouts connected to a sequence of gates

and then connected to a flipflip's fanin is common for every circuit. This problem will severely affect our calculations on Timeslack. Can you give an example of finding the critical path of timeslack?

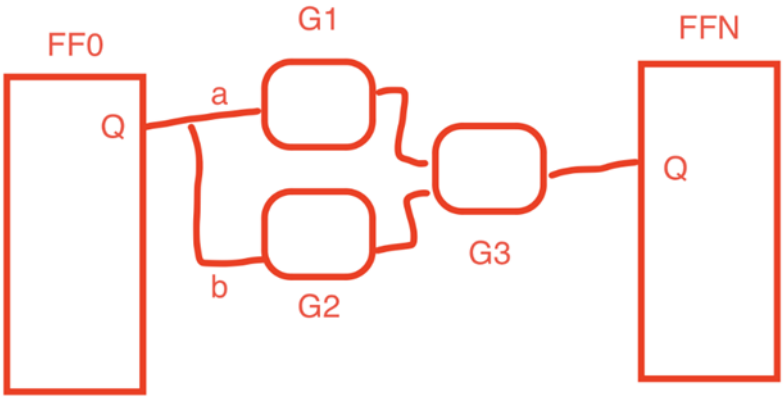
A44. There could be multiple paths. If a gate has multiple inputs, the delay is dominated by the latest arrival time of each signal. Please refer to Q16.

Q45. I am requesting further clarification regarding the delay calculation for Problem B in the contest materials.

With the image I provided below, in this case, there exist two paths from FF0 to FFN, (FF0->G1->G3->FFN) and (FF0->G2->G3->FFN).

1. How can I get the slack of FFN given FF0's qpin delay? Path1 or Path2? (assume that wire a is longer than wire b)

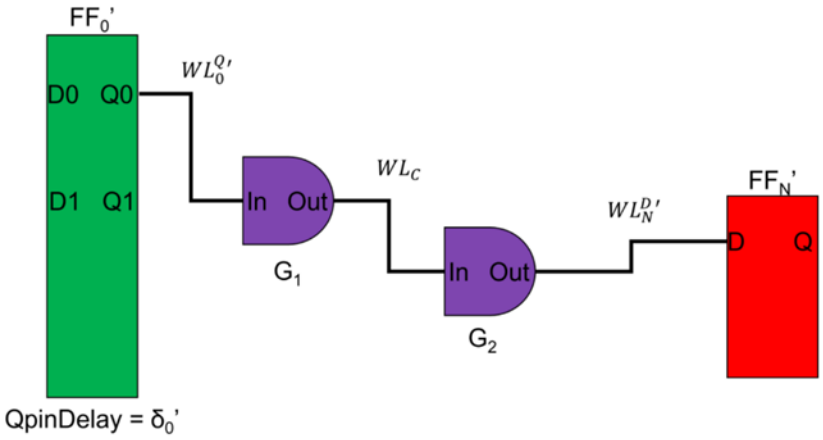
2. Assuming that FF0 has been replaced or merged, should I take the longest or shortest path to get the new slack of FFN?



3. In the latest material, the slack is calculated as follows. Assuming that the slack of FF0 is large, the slack of FFN is large(100, for example), too, but the distance between FF0 and FFN is small. According to the formula, the new slack of FFN' is calculated without considering the slack of FF0' but the position of FFN', so even if the slack of FF0' is negative, it is independent of the slack of FFN', and the slack of FFN' can still be close to 100. Do I understand correctly?

$S_{FFN}' = S_{FFN} + (\delta_0 - \delta_0') + \text{DisplacementDelay} * (WL_0^Q - WL_0^{Q\prime}) + \text{DisplacementDelay} * (WL_N^D - WL_N^{D\prime})$

$S_{FFN} = S_{FF0} + \delta_0 + \text{DisplacementDelay} * (WL_0^Q + WL_C + WL_N^D)$



A45.

1. The delay would be dominated by the latest arrival time of each signal. In this instance, G3's delay is dominated by either a or b, depending on which path has the latest arrival time. Please refer to Q16.

2. Take the latest arrival time as the delay to calculate the slack.

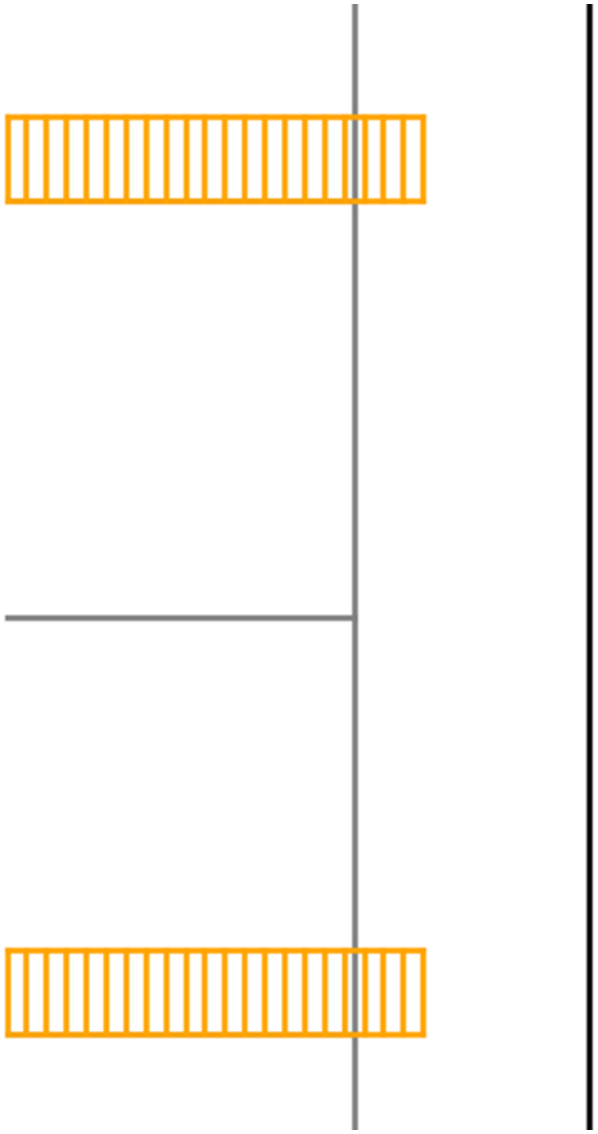
3. Please refer to Q16 as an example. The slack of FFN' would still be affected by the differences from FF0 to FF0'.

Q46. Could you please tell us where TimingSlack is used in the problem? Could you provide an example?

A46. The final score calculation involves the negative Dpin slack. For example, if one Dpin has an initial timing slack 5. After your banking/debanking operations, the arrival time of that Dpin is increased by 6, thus Dpin slack changes to –1, then it will contribute the penalty when scoring. On the other hand, it's possible to fix a violating Dpin by decreasing the arrival time.

Q47.

1. The image is based on the results of case1. In the image, the borders are defined with black lines for the Die, gray lines for the Bin, and orange lines for the PlacementRows. I would like to know if the PlacementRows can extend beyond the boundaries of the Bin as illustrated in the image, or if the Width and Height of the Bin necessarily need to match the values provided in the input file exactly. If another Bin were to be drawn to the right, it would exceed the boundaries of the DieSize.
2. Regarding the example in Figure 5, "Input CK0 0 15", is there a typographical error? I believe it should be CLK0, as the Net does not define which Net the pin CK0 belongs to.



A47.

1. All instances must be placed within the die region. All instances must be without overlap and placed on-site of PlacementRows. So it dosen't matter whether placementRow is over the boundary or not, you can't put cell outside of the die region.
2. It is a typo.

Q48.

1. Does any clock slack or clock skew issue need to be considered?
2. For each FlipFlop, given one of its input pins named "D0", must it have an output pin named as "Q0"? Similarly, "D1" for "Q1", ..., "D7" for "Q7"? If not, how should the contestants determine which output pin is corresponded to which input pin?
3. Given a gate with 2 or more input pins, does it need to wait for the latest coming input signal? Will gates have their own delays?
4. On p.11 of the problem description document, why the NumNets is 4, but not 7 (N1, N2, N3, N4, N5, CK0 and CK1)?

A48.

1. Clock delay is not considered in this problem.
2. Yes, if Di exists, then there must be a Qi. i>=0.
3. The delay is dominated by the latest arrival signal. We do not consider combinational gate delay in this contest.
4. Thank you for your feedback. The problem description should be updated along with this update.

Q49.

1. Does each pin in these libraries have a fixed naming convention, including capitalization? If not, how can we determine which pins are D pins and which are Q pins? This information becomes necessary when banking flip flops to create larger ones, as we need to know the D and Q of the flip flop first before we can map them onto the new flip flop. For example, as per the example above, we believe the format is: for a 1-bit flip flop, D is "D", Q is "Q", and clock is "CLK". For flip flops with 2 bits or more, D is "D{starting from 0}", Q is "Q{starting from 0}", and clock is "CLK". The gate information is a bit sparse, and we are not very clear on it.

2. Could you provide more cases for us to test? We hope these cases include many flip flops and gates.

3. Could you provide the initial score for each case, as well as the TNS, power, area, and D values?

4. "Nets connected to the flip-flops must remain functionally equivalent to the data input. The result should not leave any open or short net." This is a statement mentioned in the question. Could you explain and provide examples of what are "open net" and "short net"?

A49.

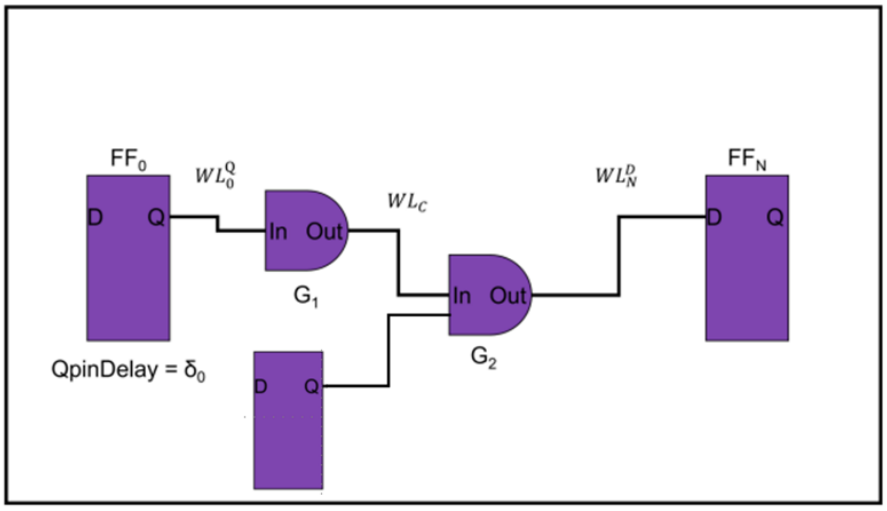
1. Please refer to our previous answer from ICCAD'24 CAD Contest Problem B Q&A Q22. All Dpins must be named as Di, so are Qpins; where D is capital and Q is capital. For gate pins, if pinName[0:2 or 3] is in/out or IN/OUT, then it's an input/output pin. CLK pin is annotated as CLK. The submitted result from contestants must align with each testcase's naming convention.

2. Testcases1 has a moderate amount of flip-flops and gates. We are preparing more testcases but some of them will be hidden testcases.

3. We do not plan to have release the initial score at this moment.

4. See Q1

Q50. How do we determine the slack when a FF has multiple ancestor FFs? As depicted in the figure.



A50. The final slack of FFN/D is decided by two timing paths:

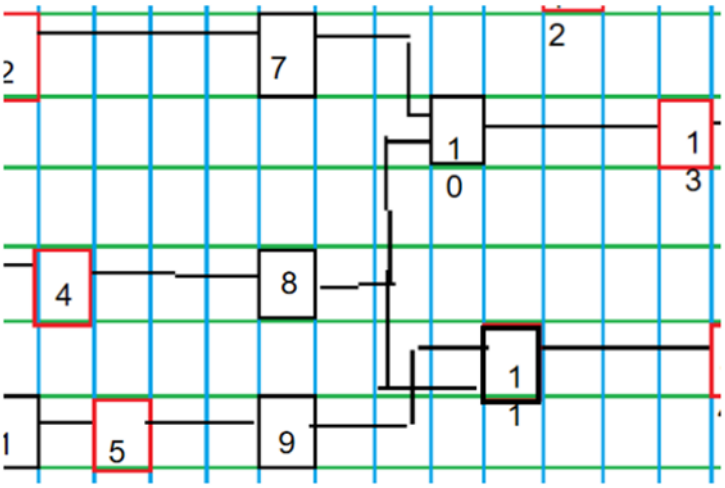
1. FF0/Q -> G1/IN->G1/OUT->G2/IN1->G2->OUT->FFN/D
2. FFbottom/Q -> G2/IN2->G2->OUT->FFN/D

The arrival time of G2/OUT = max(Arrival(G2/IN1), Arrival(G2/In2))

Arrival(G2/IN2) = QpinDelay of FFbottom/Q + HPWL(FFbottom/Q, G2/IN2) * displacementDelay.

Refer to Q12 to understand more about how to use initial slack and arrival time to determine final slack.

Q51. I'd like to ask how to know the pin direction of combination logical cells.Like the example in the followed picture,to caculate the FF13' timingslack,the FF13's D need a Q,but from the Nets and combination logical cells' pins,we may find the FF5's Q,it is not right obviously.So I suggest that the the pins' name of combination logical cells to be defined like input1,input2,output1 and so on,then we can distinguish the pin in and pin out.



A51. Please refer to our previous answer from ICCAD'24 CAD Contest Problem B Q&A Q22. All Dpins must be named as Di, so are Qpins; where D is capital and Q is capital. For gate pins, if pinName[0:2 or 3] is in/out or IN/OUT, then it's an input/output pin. CLK pin is annotated as CLK. The submitted result from contestants must align with each testcase's naming convention.

Q52. I am writting to confirm the following pin naming formats:

1. Are the indices for D and Q in all FF all start from 0?
2. Are the indicies for input and output in all gates named INi and OUTi, where i starts from 1?

A52.

1. Yes.
2. Yes.

Q53. In QA16., you mentioned that the slack through the OUTPUT wire should be also considered. However, there isn't any information about the initial slack of output pins in the test case or the way to calculate it in the problem. How do I evaluate it, or could we just ignore the wirelength from the q pin of the last stage to the output port?

A53. In our latest revision we are focusing on d-pin slacks. If the testcase does not give out the slack of the last stage of the output port, contestants are not required to calculate the slack of that stage.

Q54. Is signal "CLK" in mapping of filp-flop necessary? If I want to debank 1 (CLK named C0/CLK) ff into 2 (C1, C2), what mapping should I use?

A54. Every Flip-Flop pin that connects to a signal that has defined in the net needs mapping. C0/CLK map C1/CLK C0/CLK map C2/CLK

Q55. In the new testcase released yesterday, I have seen that there is a cyclic dependency between registers connected by the same clock net. Are they mergeable or would that cause logic inconsistency? Also, are registers belonging to different clock nets mergeable?

A55. Registers are mergeable if the resultant circuit is still functionally equivalent to the circuit before the merge. Registers belonging to different clock nets are not mergeable.

Q56. CLK pin mapping can be one-to-many or many-to-one. During our test, we saw sanity find the following output as a possible solution. We would like to have a more detailed format or rule for CLK pin mapping.

```
CellInst 4
Inst reg1 SVT_FF_1 5952 3600
Inst reg2 SVT_FF_1 1278 3600
Inst reg3 SVT_FF_1 1278 6000
Inst reg4 SVT_FF_1 3615 3600
reg1/D map reg1/D
reg1/CLK map reg2/CLK
reg1/Q map reg1/Q
reg2/D map reg2/D
reg2/CLK map reg2/CLK
reg2/Q map reg2/Q
reg3/D map reg3/D
reg3/CLK map reg2/CLK
reg3/Q map reg3/Q
reg4/D map reg4/D
reg4/CLK map reg2/CLK
reg4/Q map reg4/Q
~
```

A56. CLK pin mapping can be one-to-many or many-to-one. We want contestants to note that the format of pin-to-pin mapping is based on cell mapping.

Q57. If two ff connect to different CLK nets, can i bank them into one MBFF?

A57. No.

Q58. We want to submit the file for problem B, however we couldn't find any naming rule for the binary file that we put in the tgz file. Is there any naming rule for the binary file?

A58. Your program should be able execute like following:

./cadb_0000_alpha <input.txt> <output.txt>

Please follow the naming convention by prefixing your binary as cadb_0000*, where 0000 is the placeholder of contestants serial number. Please replace 0000 with your registered team number.

The *_alpha stands for the alpha testing stage. For each stage please specify with different postfixes (*_beta, *_final).

Please note that contestants should follow the naming description otherwise the score will be annulled.

Q59.

1. Take test_case1_0614 for example. In the cost metrics,

$$\sum_{v \in FF} \left(\alpha \cdot TNS(i) + \beta \cdot Power(i) + \gamma \cdot Area(i)\right) + \lambda \cdot D$$

if is an instance of FF1, then should be 0.019300 and should be 5610*4200=23562000. However, both and are 5, making the power term negligible in the formula. This seems to make no sense. So, do and refer to the direct numerical values provided in the testcase? Or they are normalized values? Or and are just inappropriate in this case? If they are normalized values, how should they be calculated?

2. In the formula,

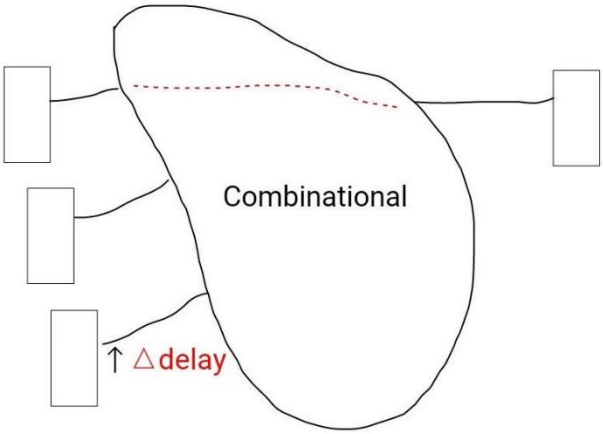
$$S_{FFN} = S_{FF0} + \delta_0 + \text{DisplacementDelay} * (WL_0^Q + WL_C + WL_N^D)$$

   1) when the circuit is like FF1---G1---G2---FF2, is the HPWL of the combinational circuit between G1 and G2 as described in the document. Is the HPWL here the Manhattan distance between G1/O and G2/I (suppose all cells here have only one bit)? Does it mean that other gates between G1 and G2 (if any) can be ignored when calculating the path from FF1 to FF2?
   2) it seems that the calculation of delay is done in a propagated way according to previous QAs. Suppose a path in the circuit is INPUT---FF1---G1---FF2---G2---FF3---OUTPUT and all cells here have only one bit. Now the ONLY operation is to move FF1. Obviously, the slack of FF2/D will change because changes. Now, will the slack of FF3/D change due to the change of the slack of FF2/D?

A59.

1. I think there are some missing symbols in the problem description. We might need to clarify the question first lest giving out confusing answers in rush.
2. (1) HPWL of the net between G1 and G2 is not affecting the contest result as G1 and G2 are immobile.
2. (2) Yes.

Q60. 1. As discussed in Q12.(1) and Q32.(1), we need to calculate each timing arc separately.
However, the combinational components are black boxes so we do not know which timing arc is the worst path.
As shown in the example below, we have 3 FFs on the left side and they will propagate the signal through a combinational component to the output FF on the right side.
As answered in Q12.(1), the negative slack will increase by the larger delta delay.
However, the timing path with a larger delta delay (the bottom one) might not be the worst path. If another path (the top one) has the worst timing, then the slack on FFN will remain the same.
How do we calculate the output slack in this case?



A60. Contestants could track the propagation of the delay from the previous stage to the next stage. The combinational gate delays could be treated as constants.

Q61. I wonder whether the height of a flip-flop could be larger than that of the placement row which contains the flip-flop or not.
If not, the information of the height of the placecment row seems unnecessary.

A61. Contestants program is expected to handle any row height flip-flops.

Q62. Hello, I would like to ask a question about the testcase of problem B. A Net must have one output pin(INPUT/OUT/Q), right? I found that all pins of "net103570" in testcase1 only contain pins of type 'CLK' and 'IN'. How can I parse such a net? There is no way to know the upper level of a certain IN of this net.

```
237467  Net net103522 703
237468  Pin C41845/OUT1
237469  Pin C82726/CLK
237470  Pin C87096/CLK
237471  Pin C98346/CLK
237472  Pin C98414/CLK
237473  Pin C98345/CLK
237474  Pin C88340/CLK
237475  Pin C97658/CLK
```

```
202973  Net net103570 360
202974  Pin C102052/CLK
202975  Pin C102053/CLK
202976  Pin C102280/CLK
202977  Pin C102279/CLK
202978  Pin C101586/CLK
202979  Pin C101587/CLK
202980  Pin C101211/CLK
```

A62. We formulate the testcase by extracting and simplifying only partial information of the whole circuit to contestants. net103570 is apparently a clock net and only necessary information is leave out for net103570.

Q63.

1.in document page 16 say that (screenshot)

> *D* stands for the number of bins that violates the utilization rate threshold. We'll calculate the total area cost of the flip-flops taking up in each bin and sum up all violating bins to formulate *D* cost.
>
> If the program and the output data violate any of these above bullets, you will get 0 score for the corresponding test case.

This means that even if we have some bin utilization violations or timing negative slack (TNS), we can still earn points in this contest as long as we meet the evaluation constraints. However, in practical applications, negative slack often indicates that the data might be incorrect.

2. in samplecase line6~8 is input cell library

```
6   NumInput 2
7   Input in 8344 22840
8   Input clk 0 1970
```

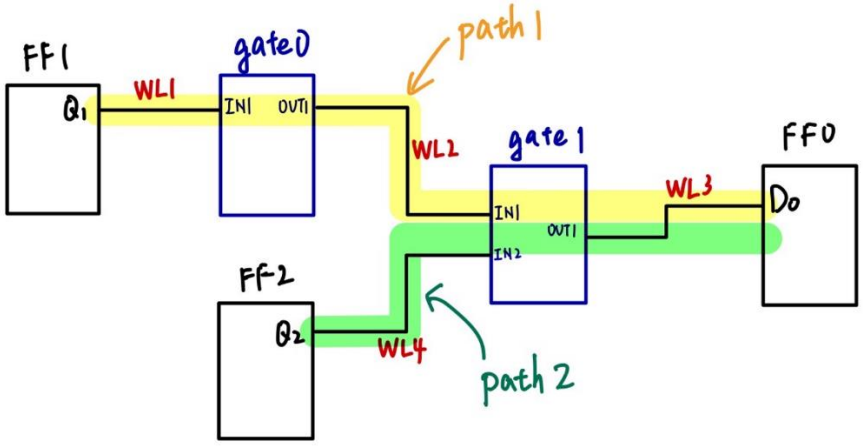
```
42  Net clk 5
43  Pin CLK
44  Pin reg4/CLK
45  Pin reg3/CLK
46  Pin reg2/CLK
47  Pin reg1/CLK
```

so in line 43 should be change to "Pin clk" ?

A63. Yes. That's a typo to simplecase. Thanks for pointing out.

Q64.

1. In Q32, we have already determined that we need to calculate the different paths ("FF1 to FF0" and "FF2 to FF0") and take the maximum. However, in the following example, FF1 also passes through gate0 first. If we cannot determine the delay of gate0, how do we calculate the "FF1 to FF0" path? Should we set the delay of all gates to 0? That is, only use this function to calculate new slack: max(delta Qpindelay of FF1 + DisplacementDelay*delta(WL1+WL2+WL3) + original_slack of path1, Qpindelay of FF2 + DisplacementDelay*delta(WL4+WL3) + original_slack of path2). Is that correct?



2. In addition, in this example, how do we calculate the original slack of path1 & path2? Because the initial critical path of FF0 might be path1 or path2, without knowing the delays of gate0 and gate1 and other constants, how can we determine whether it's path1 or path2? Even if we know, we can't determine the original slack of the other path. Please list the detailed formulas clearly.

3. As in A28: "Placeable area is defined by the union of all PlacementRows." So, will the Placeable area be a continuous region and form a rectangle?

4. Furthermore, besides being placed on-site as their bottom-left corners align with the site grids of the PlacementRows, should there be an additional condition that the entire cell must be completely within the Placeable area?

A64.

1. Combinational gates are considered constants in this contest, therefore, contestants only need to consider combinational gate delay as constants and propagate delay of each maneuver. Your calculation generally looks correct.

2. Contestants are expected to deduct the delay based on the given information. Each D pin would be given an initial delay, and QpinDelay as well as DisplacementDelay is provided.
3. That’s not in the definition. A union a two area could be disjoint.
4. That’s not in the definition.

Q65. May you generate a sample output including debanking operation?
Plus, I wonder if debanking a flip-flop which is generated by the operation of banking is legal, and how do i handle with the mapping of clock pins in the output file if the operation of debanking or "debanking after banking" exists?

A65. (1)Thank you for the suggestion. We’ll see if that’s feasible.
(2)It is legal. But please note that contestants should only list the final product of their circuit. No intermittent product should be listed. Redundant intermittent flip-flops listed in the output file would be considered violation.
(3)Map each clock pins (one-to-many or many-to-one)

Q66. In the Submission Announcement, it is mentioned that the files required for the alpha test need to be submitted according to the requirements of each task. However, in "4.2 Program Requirements," it is stated that the rule for the binary executable file name will be given on the contest website, but currently, there are no naming rules provided on the website. Therefore, I would like to inquire about the naming rules for the alpha test submission.

Additionally, in the sample case provided for case1, there are the following two lines in the PlacementRows section:
PlacementRows 480 3600 57 240 395
PlacementRows 480 6000 57 240 395
in the sample output, the instances "Inst reg5 SVT_FF_2 5952 3600" and "Inst reg6 SVT_FF_2 1278 3600" are placed on-site, but the FF exceeds the placement row's range. Is this acceptable?

A66. (1) Thank you for your reminder. We updated Program Requirement parts.
(2) That’s not in the definition

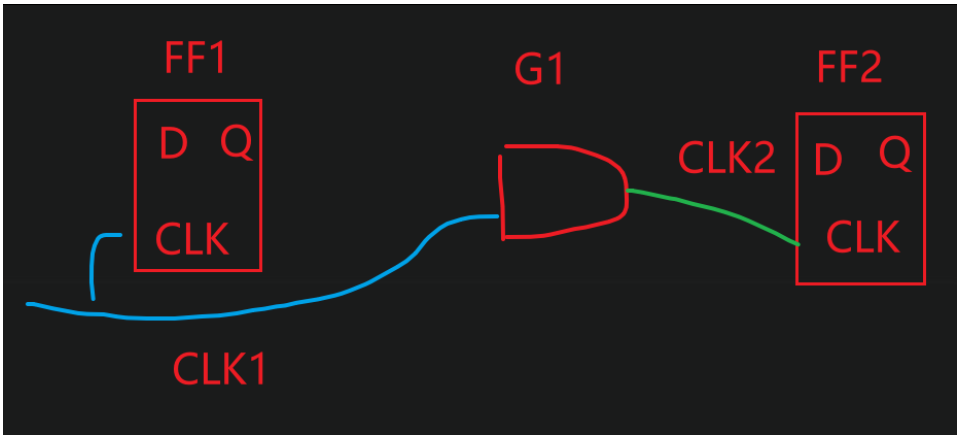
Q67. I am writing to inquire the submit binary naming rule in problem B.

A67. Thank you for your reminder. We updated Program Requirement parts.

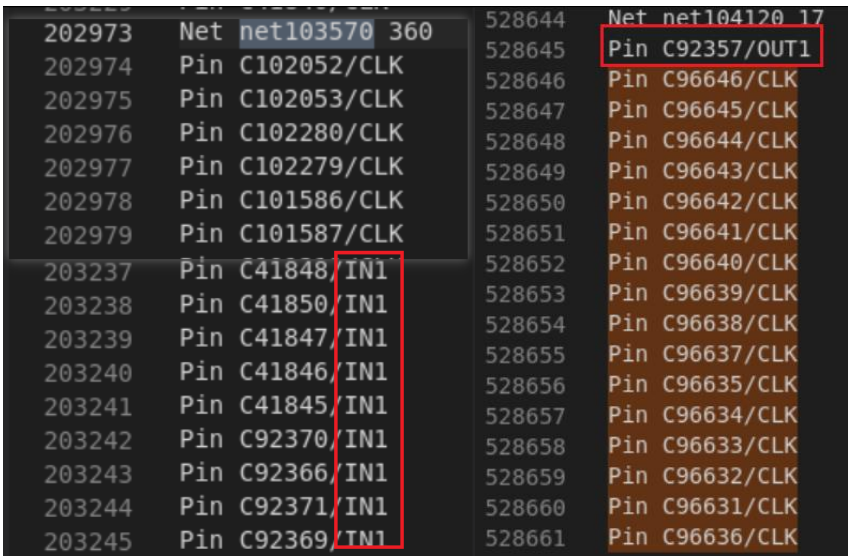
Q68. I wanted to ask whether it is possible to merge flip-flops whose CLK pins belong to separate CLK nets, and if it is possible, would it be possible to give a small example? I tried searching for the answer in the Q/A pdf released but I was unable to find an answer for it, so I wanted to clarify it directly once again.

A68. No. Merging flip-flops whose CLK pins belong to separate CLK nets should result in short circuit.

Q69. 1. It is said in A17.4 that All clock nets will start with the name CLK. However, in test case 1, all nets start with 'net'. It is troublesome to distinguish clk nets, as we have to check whether there is any pin named 'CLK in parsing all pins in the net concerned.
2. We are not sure about whether clk nets can relate to each other. As seen in the figure, if clk1 connects to the input of combinational gate G1, and clk 2 connects to the output of G1, is it possible that G1 acts as a buffer, and clk1 and clk2 (in other words, flip flop FF1 and FF2) lie in the same clk domain?



3. Is CLK pin an input, output or inout pin? We have observed in testcase1 that for nets connected to CLK pins, they can also connect to IN and OUT pins of combinational gates.



A69. 1. Thank you for your feedback. We'll seek the possibility to improve the testcase.

2. It is feasible in practical usage, but in this contest we have simplified the issue to contestants and we are not distinguishing the functionality of any combinational gate, so CLK1 and CLK2 are considered as two different CLK.

Q70. In **case1/sampleCase**, i notice that the two placement rows are not connect continuously in vertical direction, which makes me confusing. Since the FF height size is larger than site height, even the FF is placed "on site" , part of the FF will still definitely be placed outside of the placement row. I think there must be something wrong for site hight in this testcase! I know that the cell can be placed across the placement rows, but shouldn't all the cell be enclosed inside the placement rows?

By the way, will all the comb cells and ff cells be placed "on site" in the given input?

A70. We do not require all cells to be enclosed within PlacementRows. We do not guarantee all cells to be placed on site in the given input.

Q71. I am writting to inquire about the following:
(1). Are all the clock nets in the netlist are named CKi, where i is
a integer starting from 0?
(2). If (1) is true. Are all the "CK" in uppercase? Or it might also
be lower case?

A71.
(1) Not necessary. (2) Net names could be upper or lower case.

Q72. We cannot verify that this equation is correct from testcase1:

\[S_{FFN} = S_{FF0} + \delta_0 + \text{DisplacementDelay} \times (WL_0^Q + WL_C + WL_N^D) \]

Here's our verification process.

Find two flip-flops, C42059 and C42075, which are connected by net28176 (a 2-pin net):
Net net28176 2
Pin C42059/Q
Pin C42075/D

Their positions are:
Inst C42059 FF1 396780 562800
Inst C42075 FF1 382500 562800

From the cell library, we know that:
FlipFlop 1 FF1 5610 4200 3
Pin Q 1110 3640
Pin D 1345 400

So far, we can calculate the positions of Pin C42059/Q and Pin C42075/D as (397890, 566440) and (383845, 563200), respectively. Therefore, the HPWL is \((397890 - 383845) + (566440 - 563200) = 17285 \).

Both are FF1 types:
QpinDelay FF1 18.052032

Then, their timing slacks are:
TimingSlack C42059 D 89.247696
TimingSlack C42075 D 175.082764

Finally, the displacement delay:

DisplacementDelay 0.01

From the equation, we can calculate the value:
\[S_{FF0} + \delta_0 + \text{DisplacementDelay} \times
(WL_0^Q + WL_C + WL_N^D) \]
= 89.247696 + 18.052032 + 0.01 * 17285
= 280.149728

The result is different from our expectation, which should be C42075's timing slack: 175.082764.

Have we misunderstood the problem and equation? If so, how should we apply this equation correctly in this case? Or is the testcase incorrect?

Thank you for your explanation.

A72. The equation is
$S_{FFN} = S_{FF0} + \delta_0 + \text{DisplacementDelay} * (WL_0^Q + WL_C + WL_N^D)$
Only when S FF0 is the starting level of FF.
In your case, C42059 is not a starting level FF. Therefore, you should first find the starting point and then use the following equation to update and calculate the slack of both C42059 and C42075.
$S_{FFN}' = S_{FFN} + (\delta_0 - \delta_0') + \text{DisplacementDelay} * (WL_0^Q - WL_0^{Q\prime}) + \text{DisplacementDelay} * (WL_N^D - WL_N^{D\prime})$

The following help you backtrace to a point where you can find another FF prior to C42059, proving that C42059 is not the starting point.

Net net28176 2
Pin C42059/Q
Pin C42075/D
(backtrace @ C42059)

Net net28175 3
Pin C41907/OUT1
Pin C42059/D

Pin C42057/IN2
(backtrace @ C41907)

Net net28177 4
Pin C3541/OUT1
Pin C41907/IN2
Pin C16476/IN2
Pin C33689/IN3
(backtrace @ C3541)

Net net28179 10
Pin C108290/OUT1
Pin C3541/IN1
Pin C16100/IN2
Pin C7307/IN2
Pin C22739/IN5
Pin C22304/IN3
Pin C107906/IN1
Pin C107535/IN1
Pin C73364/IN3
Pin C73275/IN1
(backtrace @ C108290)

Net net28187 7
Pin C37761/OUT1
Pin C108290/IN1
Pin C4771/IN1
Pin C27922/IN1
Pin C2850/IN3
Pin C73390/IN5
Pin C73342/IN6
(backtrace @ C37761)

Net net28192 6
Pin C73771/Q
Pin C37761/IN1
Pin C37774/IN1
Pin C4190/IN2

Pin C37453/IN1
Pin C37479/IN1
(backtrace @ C73771)
Here, C73771 is a FF prior to C42059, hence C42059 is not the starting point.

Q73. As the slack calculation goes as: SFFN' = SFFN + (δ0 – δ0') + DisplacementDelay * **(WL0Q– WL0Q′)** +DisplacementDelay * **(WLND – WLND′)**, what if FFN and FF0 connect directly to each other? Should we calculate the wirelength between the two FF (that is both WL0Q and WLND) once or twice?

A73. You should calculate the slack until it converges.

Q74. Can all circuits in the testcase be represented as DAG?

A74. No, it is not guaranteed to be a DAG.

Q75. I wanted to know how question 35 part 2 is legal in the Q/A pdf. Isn't there a logic dependency between the flip-flops connected in series? Is it implied that on merging series connected flip-flops, the new flip-flop has an internal mechanism for handling one cycle delay for logic dependency between the D0 and D1 pin(as shown in the diagram for Q35 part2)?
If that's the case, then if there are multiple such flip-flops connected in series(lets say 3, FF1,FF2,FF3 connected in that order), is it possible to merge FF1 and FF3 together(skipping over the FF2 in the middle)?

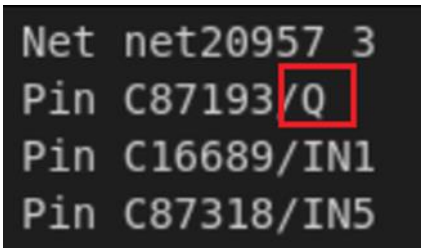
A75.
(1) Yes , it is implied that on merging series connected flip-flops, the new flip-flop is able to handle one cycle delay for logic dependency between the D0 and D1.
(2) Yes, it is possible as long as they are connected to the same clock net.

Q76. We have some further questions,
1) As the response and QA42.(2) indicated, I think we cannot track the propagation in the combinational components if we don't know the constant delay value of the combinational gates.

Suppose the arrival time at FFN is "n * constant combinational delay + Displacement delay + QpinDelay of FF0". Since the QpinDelay and Displacement delay of a path are absolute values, we can track the arrival time of different timing paths when the constant combinational delay is known.
2) If the constant combinational delay is given, or is 0. Are we supposed to write a timing propagation ourselves to get which one of the input FF0s finally propagates the latest signal to FFN?

A76.
(1) You can assume that all combinational gate delays are 0 and focus on the optimization of register banking and debanking. (2) As stated in section 3.2 Format of Output Data, we expect a Iist of bottom-left coordinates of cell instances in the design, and the changed cells and their corresponding pin mappings. The preceding does NOT require contestant to provide the timing propagation information. In your case, if you wish to determine which one of the input FF0s finally propagates the latest signal to FFN, then yes, you can write a timing propagation yourself to get that information.

Q77. We have some questions for problem B:
1. In Q52, it is said that the indices for D and Q in all FF all start from 0. However, in test case 1, the names of pins in single-bit FFs are "D" and "Q" but not "D0" and "Q0". Currently, we use hard code to address the indices naming issue (we check whether the ff is multi-bit of single bit, and decide whether to write "D0" or "D"). Will this be modified in the future? If so, will it be a modified version of testcases before the beta test, so we can address the new naming format in time?



2. We are confused about whether the slack calculation is cascaded. Take the case in Q59.2(2) for example, where the timing arc goes as FF1->FF2->FF3. Suppose we ONLY modify FF1, and leave FF2 untouched.

$$S_{FFN} = S_{FF0} + \delta_0 + \text{DisplacementDelay} * (WL_0^Q + WL_C + WL_N^D)$$

A59 2(2) follows the above equation that there will be a butterfly effect in the slack calculation, which means the Dpin slack of FF3 will be affected by FF1's modification.

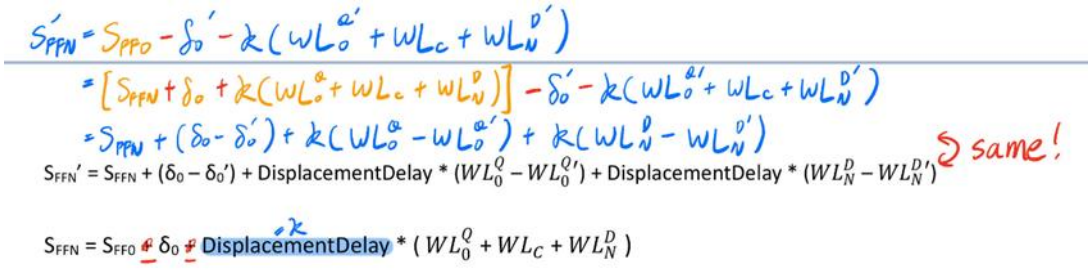
$S_{FFN}' = S_{FFN} + (\delta_0 - \delta_0') + \text{DisplacementDelay} * (WL_0^Q - WL_0^{Q\prime}) + \text{DisplacementDelay} * (WL_N^D - WL_N^{D\prime})$

However, SFF0 is gone in the final formulation of slack calculation. The function of Q64.1 is derived from this equation. Under the function of Q64.1, if we want to calculate the slack of FF3 cin the FF1->FF2->FF3 case, apart from the HPWL displacement of FF2 and FF3, we only need to concern the delta Qpindelay of FF2, which is only related to the FF type of FF2 and have nothing to do with FF1. Q64.1 is also acknowledged and yet conflicts with Q59.2(2).
We favor the uncascaded model because slacks should not cross the FF accumulation and are associated with different positions/negedges.

A77.

(1) In Q52, it is stated that the indices of D and Q in all FF all start from 0, if there are indices. With single-bit FFs, we may or may not provide indices as they are not necessary. Therefore, this will NOT be modified in the future. (2) Q64.1 does NOT conflict with Q59.2(2). In Q64.1, FF1 and FF2 are assumed to be the starting level FF of the design. This assumption is NOT equivalent to the assumption that the slack calculation can neglect the timing delay of multi-level FF. The timing delay model in our criteria remains the SAME.

Q78. Is the formula of the S_FFN given incorrectly? Here's our derivation.
Changing the formula in the last line in the image (S_FFN = ...) can derivate the second formula you gave (S_FFN' = ...).
While we can't do that with the original formula.

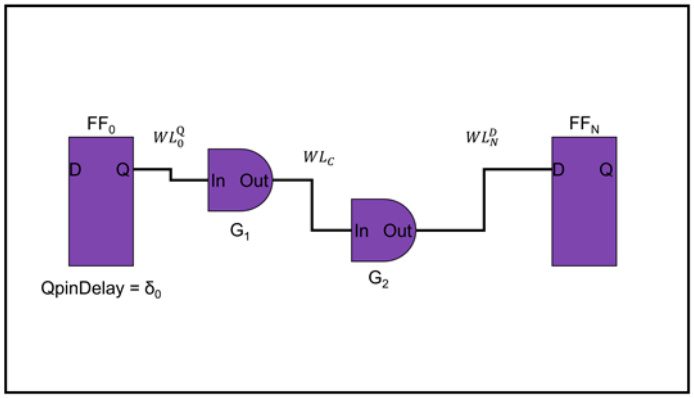


A78.

$S_{FFN}' = S_{FFN} + (\delta_0 - \delta_0') + \text{DisplacementDelay} * (WL_0^Q - WL_0^{Q\prime}) + \text{DisplacementDelay} * (WL_N^D - WL_N^{D\prime})$ - (1)

$S_{FFN} = S_{FF0} + \delta_0 + DisplacementDelay * (WL_0^Q + WL_C + WL_N^D) - (2)$

In equation (2) the S_{FFN} is not the same to the S_{FFN} in equation (1), it actually denotes the slack of the following figure. Therefore, both equations are definitions, not a derivation of each other.



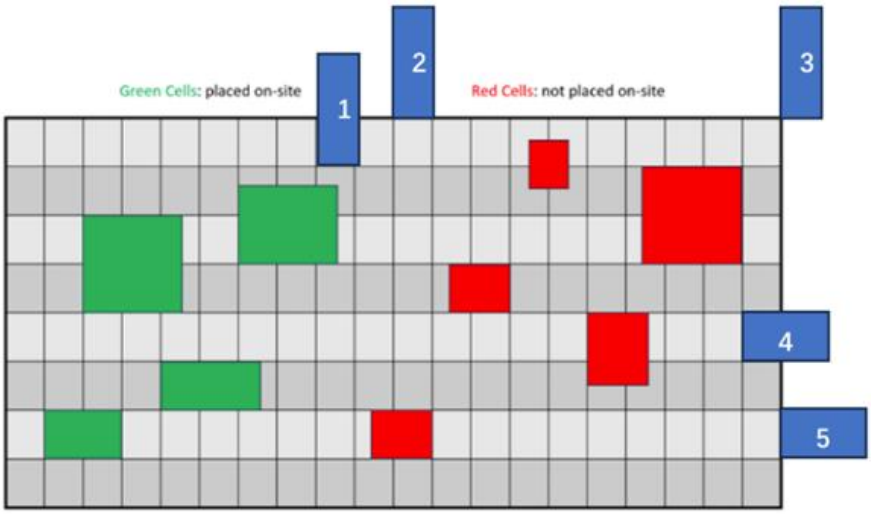
Q79.

1. (Sorry for missing symbols due to some incompatibility issues.) Take test_case1_0614 for example. In the cost metrics,

$$\sum_{\forall i \in FF} \left(\alpha \cdot TNS(i) + \beta \cdot Power(i) + \gamma \cdot Area(i)\right) + \lambda \cdot D$$

if i is an instance of FF1, then $Power(i)$ should be 0.019300 and $Area(i)$ should be 5610*4200=23562000. However, both β and γ are 5, making the power term negligible in the formula. This seems to make no sense. So, do $Power(i)$ and $Area(i)$ refer to the direct numerical values provided in the testcase? Or they are normalized values? Or β and γ are just inappropriate in this case? If they are normalized values, how should they be calculated?

2. In QA64.4 and QA70, you mentioned that there is no need for cells to be enclosed within PlecementRows. To ensure my understanding is correct, I have made some supplements based on the examples in the document, as shown in the following figure. May I ask which of the 5 blue cells are legal? (Assume that all of them are within die region)

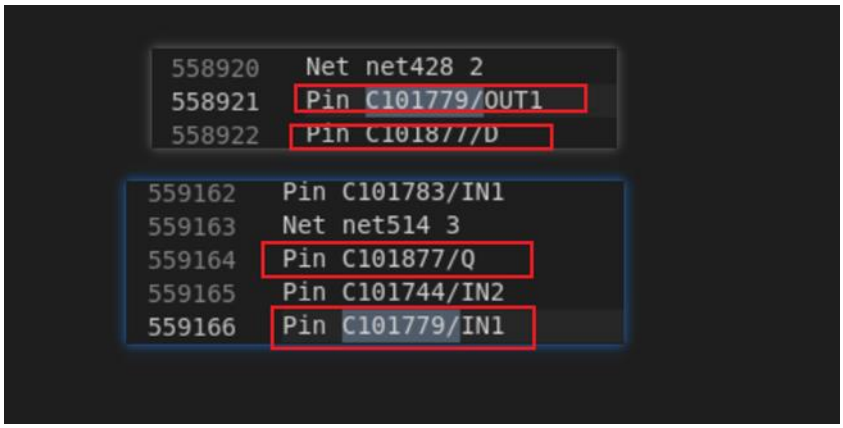


A79.

(1) You should expect different combinations of weight. This cost function is designed so that we choose our objective (e.g. area dominant, timing dominant, power dominant…). In your question statement, the power term is indeed nearly negligible given the combinations of weight. The combinations of weight we provided is just one of the scenarios but not inappropriate.

(2) The area of any cells should not exceed the die area. Therefore, considering that the white space in your figure is outside of the die area. All 5 blue cells are illegal. That being said, if all 5 blue cells of yours are in the die area (i.e. if the white space in your figure is in the die area), Cell 1, 4 and 5 are legal as they are not required to be enclosed within PlacementRows and their bottom-left corners all align with the site grids. The bottom-left corners of Cell 2 and 3 are not aligned with the site grids but above the site.

Q80. We found a loop in the netlist of testcase1. Does it support the non-cascaded model of Slack calculation?



A80. No.

Q81. 對於 problemB 的 output 規定有些問題

現在我有一個 2-bit FF 作為輸入
輸出是兩個 single bit FF
該如何表示

ex:將 reg3 (2-bit FF) map 成 C1 C2 (皆為 single-bit FF)
若 output 這樣表示:
reg3/D0 map C1/D
reg3/Q0 map C1/Q
reg3/CLK map C1/CLK
reg3/D1 map C2/D
reg3/Q1 map C2/Q
reg3/CLK map C2/CLK

sanity 將會回傳"can't map duplicately reg3/CLK"
若要過 sanity 則須第三行或第六行刪除
但這不符合現實
如同 Q54 所提及的
我們也認同不論 C1 或 C2 的 CLK 都應該同時與 reg3/CLK mapping

想請問哪裡可能有誤
附件為測試用 input 及我們認為正確的 output(但此 output 過不了 sanity)

($./sanity sampleCase2 output.txt)

```
CellInst 4
Inst C1 SVT_FF_1 1221 6000
Inst C2 SVT_FF_1 1278 6000
Inst C3 SVT_FF_1 1278 3600
Inst C4 SVT_FF_1 5952 3600
reg1/D map C4/D
reg1/Q map C4/Q
reg1/CLK map C4/CLK
reg2/D map C3/D
reg2/Q map C3/Q
reg2/CLK map C3/CLK
reg3/D0 map C1/D
reg3/Q0 map C1/Q
reg3/CLK map C1/CLK
reg3/D1 map C2/D
reg3/Q1 map C2/Q
reg3/CLK map C2/CLK
```

Alpha 10
Beta 10
Gamma 0.0000002
Lambda 10
DieSize 0 0 23475 23280
NumInput 2
Input in 8344 22840
Input clk 0 1970
NumOutput 1
Output out 23075 11410
FlipFlop 1 SVT_FF_1 741 480 3
Pin D 152 30
Pin CLK 494 30
Pin Q 38 270
FlipFlop 2 SVT_FF_2 798 1960 5
Pin D0 494 350
Pin CLK 95 30
Pin Q0 665 30
Pin D1 494 510
Pin Q1 665 750

NumInstances 3
Inst reg1 SVT_FF_1 5952 3600
Inst reg2 SVT_FF_1 1278 3600
Inst reg3 SVT_FF_2 1278 6000
NumNets 6
Net p0 2
Pin reg1/Q
Pin reg2/D
Net p1 2
Pin reg2/Q
Pin reg3/D0
Net p2 2
Pin reg3/Q0
Pin reg3/D1
Net out 2
Pin reg3/Q1
Pin out
Net in 2
Pin in
Pin reg1/D
Net clk 4
Pin CLK
Pin reg3/CLK
Pin reg2/CLK
Pin reg1/CLK
BinWidth 1200
BinHeight 1200
BinMaxUtil 25
PlacementRows 480 3600 57 240 395
PlacementRows 480 6000 57 240 395
DisplacementDelay 0.01
QpinDelay SVT_FF_1 0.02
QpinDelay SVT_FF_2 0.06
TimingSlack reg1 D -0.183134
TimingSlack reg2 D 0.149378
TimingSlack reg3 D -0.152106
GatePower SVT_FF_1 1.4781e+01
GatePower SVT_FF_2 5.2515e+01

A81. Thank you for your information, you are correct. We will update the sanity checker.

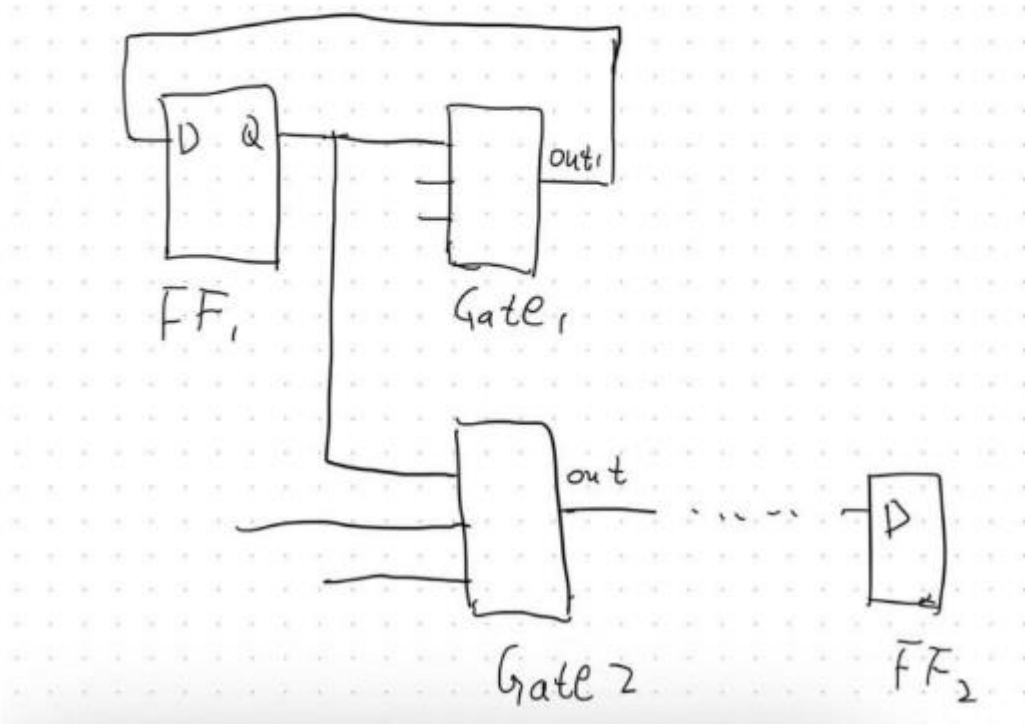
Q82. I want to ask about providing a place-on-site checker and the evaluator to this problem. The checker will help ensure all cell instances are correctly placed on-site within the defined placement rows, as required by the contest guidelines. These would greatly assist us in verifying and improving our program.

A82. We will only provide the sanity checker for now.

Q83.

```
Net net4043 3
Pin C102682/Q
Pin C10947/IN1
Pin C10152/IN4
```

```
Net net1030 2
Pin C10152/OUT1
Pin C102682/D
```



In testcase1_0614, there are many subcircuits, as shown in the figure, where one FF's Q pin (C102682/Q) connects to a gate's input (C10152/IN4) and the gate's output (C10152/OUT1) connects to the same FF's D pin (C102682/D). This means that there are rings in the netlist. Therefore, if the slack is calculated in a propagation way, the

slack of D pins which are on a certain ring will be negative infinity. Calculating D pin slack through propagation seems to make no sense, since it should only be determined by clock period (skews...), delay of wire/combinational logic between two FFs, setup time of D and CLK to Q time of Q.

A83. The “ring” is not negative infinity. A timing arc is calculated from clock trigger to endpoint. We are formulating this problem as a simplified simulation to real design circuit. These formulations are intended to lower the barrier so that contestants can focus on and sequential optimization.

Q84. May I know if the final score values will be scaled? Since the current metric will be extremely biased by the area cost. Thanks.

A84. The metric is a combination of power, area, and timing. Each testcase would have different weight values for these costs and contestants are expected to adjust their program to optimize for the best scores with each given metrics.

Q85.

1. In the documentation of Problem B. The formula of slack is shown below.

$$S_{FFN} = S_{FF0} + \delta_0 + \text{DisplacementDelay} * (WL_0^Q + WL_C + WL_N^D)$$

We tried to verify the formula in the initial case, but we found that the result was different. For example, in testcase1_0614, the Q pin of flip flop C100700 is connected directly to the D pin of flip flop C100701. Hence, we calculated the slack of C100701 based on the given formula. However, the calculated slack was different from the given slack of C100701. There are many other cases with the same issue. Is that correct?

2. In testcase1_0614, the area cost dominates the overall cost, as shown in the attached table. This suggests that optimization for timing and power has significantly less impact in this case. Is this a normal condition?

	Timing	Power	Area	Violated Bins
Weight	1	5	5	10
Initial value	657.883	457.185	4.62506e+11	1

3. If the input case includes multi-bit flip-flops that are debanked in the output result, the clk pin will exhibit a one-to-many mapping. When we test this condition with our own test case, the one-to-many mapping fails the sanity check. Could you verify the functionality of the sanity checker to ensure it handles this condition correctly?

A85.
1. Contestants are expected to take the input slack value and use the above formula to calculate the differences after their moves.
2. Each testcase would have different cost metrics.
3. Our sanity checker has been updated. Please refer to the latest checker. Thank you.

Q85. Could you please explain how the final overall ranking is calculated based on each case? Is it done by standardizing each case and then taking the overall average, or is there another method used?

A85. We will rescale the score of each cases. Then, the final score will be the weighted sum of the score of each cases. The weight will be decided according to the size of the testcases.

Q86. The latest update of testcase1 and testcase2 was 8/12, does that mean that in the final test, the 8/12 version will be used instead of their older version?

A86. Yes, testcase1_0812 and testcase2_0812 will be used in the final test, and all the older version should be considered deprecated.

Q87. Since time factor is considered in evaluation, we wonder whether the open cases (testcase1_0812, testcase2_0812) will be included in final evaluation. If they are

included, is it okay to directly output the result file computed in advance for timing benefits? Or is there extended explanation or regulations about this trick?

A87. Measures will be taken to prevent contestants from computing the result in advance for timing benefits. Please do not try to do so.

Q88. Testcase1_0812 including nets with only one pin is what we expected. However, The circuit in testcase2 also has nets with only one pin (e.g. C52049/OUT1, the Instance exists, but unlike testcase1, the pin's net is not specified in testcase2, which is after beta submission). This is what we didn't expect, since the case was released after beta submission . We understand the test case is difficult to generate, but we still want to ask if it is possible to modify testcase2 /hidden case so it has the same rule as testcase1. Or it is guaranteed that the format of the hidden case must follow either one of the public cases, Thank you.

A88. The situation you mentioned in testcase2_0812 does not affect the outcome and will remain unchanged. As you can see from the beta test result, contestants are still able to generate legal result and have final scores.

Q89. We have noticed some discrepancies between our calculations and your TNS-related calculations. Therefore, we would like to clarify the correct methodology using the following four cases. We would appreciate it if you could provide a detailed calculation process (specific numerical calculations, which formula was used, and the reason) for calculate the updated slack for each flip-flop (FF) for each of these four cases.

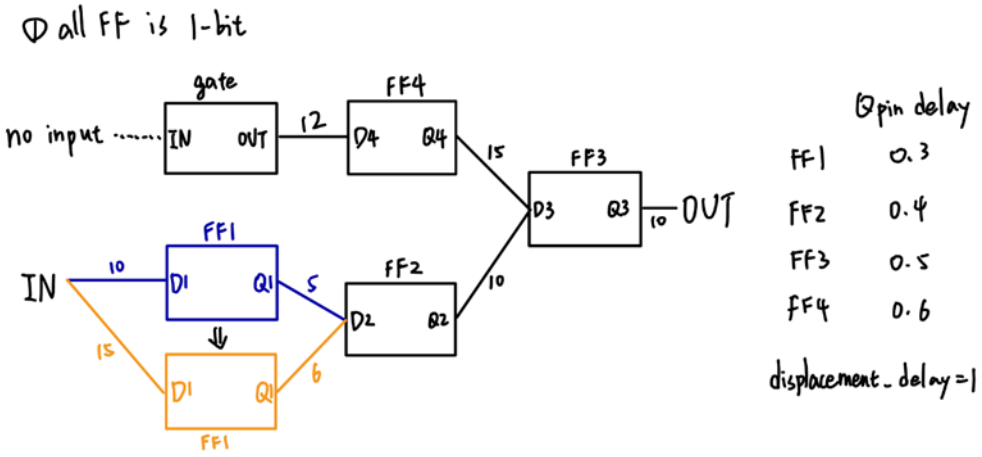
formula 1:

$$S_{FFN} = S_{FF0} + \delta_0 + \text{DisplacementDelay} * (WL_0^Q + WL_C + WL_N^D)$$

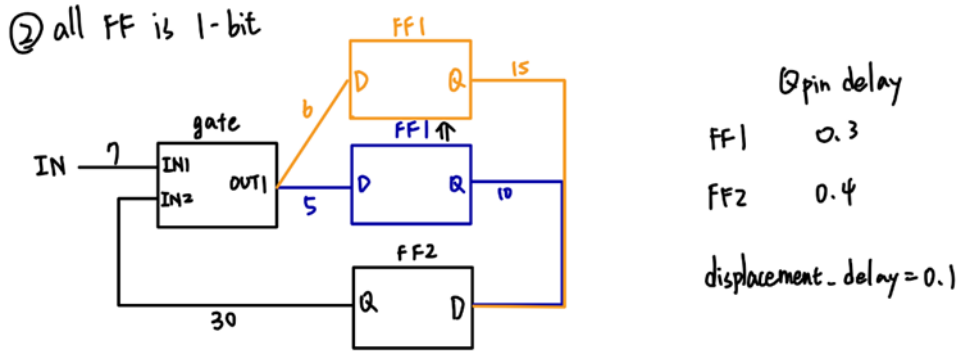
formula 2:

$$S_{FFN}' = S_{FFN} + (\delta_0 - \delta_0') + \text{DisplacementDelay} * (WL_0^Q - WL_0^{Q\prime}) + \text{DisplacementDelay} * (WL_N^D - WL_N^{D\prime})$$

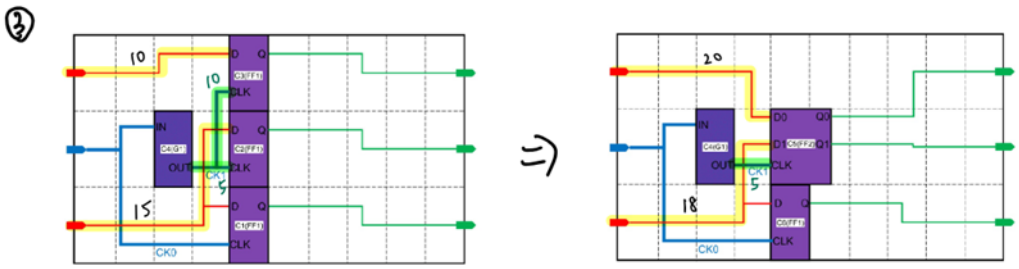
(1) The first case involves a gate with no inputs and what constitutes a starting level flip-flop (FF). All the numbers on the diagram represent wirelength. The initial slack for all FFs is -5. If we move the original blue FF to the position of the orange FF, how will the slack change?



(2) The second case concerns FFs with loops. All the numbers on the diagram represent wirelength. The initial slack for all FFs is -5. If we move the original blue FF to the position of the orange FF, how will the slack change?

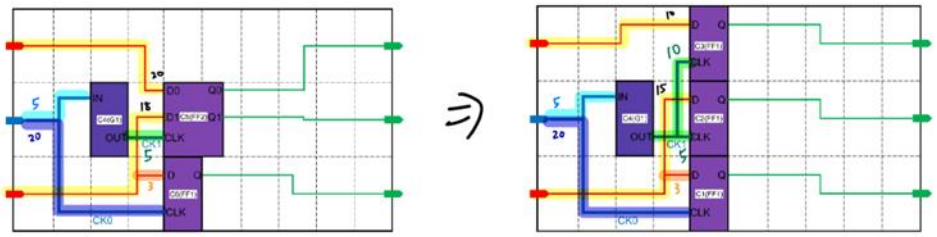


(3) The third case is related to Banking. All the numbers on the diagram represent wirelength. The initial slack for all FFs is -5.



(4) The fourth case is related to Debanking. All the numbers on the diagram represent wirelength. The initial slack for all FFs is -5.

④



Ⓑpin delay

FF1 0.3 displacement_delay=1

FF2 0.4

2. Additionally, we would like to ask about the method used to score the test cases. A85 mentioned that each test case would be rescaled. Could you please provide the exact scoring method? Is it like Problem A below?

4. Evaluation Criteria

- Correctness is necessary. If the generated netlist is not functionally equivalent to the given netlist, the contestants will get zero points for the case.
- ***cost*** for each case: The cost reported by the cost function estimator on the finally outputted netlist.
- ***point*** for each case:

$$\boldsymbol{point} = \frac{\min\left(\boldsymbol{cost}\ of\ the\ case\ from\ all\ teams\right)}{\boldsymbol{cost}\ of\ the\ case} \times 100\%$$

- ***final_score*** is the sum of ***point*** of all cases.
- The team having the largest ***final_score*** wins.

3. I would like to ask if the coordinates of the sites are always integers. If not, how should they be represented in the OUTPUT file?

4. In A79, you mentioned that Cell 1, 4, and 5 are legal, but we found that Cell 5 fails in your provided evaluator. Could you please confirm the evaluator?

A89.

1. (1) Please use formula 2 to calculate the timing change with displacement. Take FF1's initial slack as SFFN. WLDN is 10, WLDN' is 15. The new slack for FF1 is -5-5=-10. Please calculate the rest using formula 2.

(2) Please use formula 2 to calculate the timing change with displacement. Take FF1's initial slack as SFFN. WLDN is 5, WLDN' is 6. The new slack for FF1 is -5-1=-16. Please calculate the rest using formula 2.

(3),(4) Please use formula 2 to calculate the timing change with displacement and take the difference between the Manhattan distance from the driver to the load.

2. The scoring metric is similar to Problem A. The scaling would be related to the scale of the testcase and each contestants' performance.
3. Yes.
4. Thank you for your input. The final evaluator is robust to handle this scenario.

Q90.
1. Is the directory I uploaded my final submission's binary executable correct?

2. If the initial placement isn't legal because a flip-flop isn't on site, we need to move or merge the flip-flop somewhere on site, correct? Furthermore, if the flip-flop isn't connected to anything, can we directly remove or ignore the flip-flop from in final placement?

A90.
1. "cadb_xxxx_final <input.txt> <output.txt>" is the correct format.
2. We expect contestants to handle data input robustly.

Q91. Another question, you only care about the binary executable, right? Can I have other files in the directory besides the executable? Thanks.

A91. Please make sure the binary name is in accordance to the requested format, and make sure binary is executable.

Q92. The position of C43456 in testcase_3 is not located at the bottom-left corner of the PlacementRows. Could you please clarify if this is an error in the case or if we are expected to move it to a valid position? We believe it to be an error, as this issue does not appear in other cases.

```
Inst C43454 FF1 457980 772800
Inst C43455 FF45 447780 798000
Inst C43456 FF1 0 0
Inst C43457 FF1 443700 777000
Inst C43458 FF1 419220 793800
```

A92. We expect contestants to handle data input robustly.

Q93. We have 3 questions about problem B.
1. In testcase_3, the position of instance C43456(FF1) is (0,0), which is out of all Placement Rows.
2. We noticed that DisplacementDelay is reduced in recent cases (0.01->0.001, 0.001->0.0001). Will the final cases' DisplacementDelays also be small?
3. In previous version of testcase1 and testcase2, TNS accounts for ~30% and ~5% proportion of total cost respectively since the weights of TNS are larger, making it hard to bank Flipflops. Will there be similar weight combinations in the final case ?

A93.
1. Yes.
2. We expect contestants to handle data input robustly.
3. We expect contestants to handle various weights and optimize based on the objective metrics.

Q94. I have some questions regarding the scoring method:
1. My understanding is that the score is composed of TNS, Power, Area and D. We expect the score to be as low as possible, symbolizing the optimization of PPA. My first question is about TNS: TNS is calculated by summing the slack values of all FlipFlops that are negative, so the TNS value should be negative. However, this seems to encourage a lower TNS value, as it would reduce the overall score. Does TNS signify that the signal did not arrive within the required time, thus needing a penalty? If so, $\alpha \times$TNS should ensure a positive result.

2. My second question concerns still the sample case. In this example, the area and power consumption of a 2-bit flip-flop are significantly greater than those of a 1-bit flip-flop, so choosing a 1-bit flip-flop is a no-brainer. In the sample case, $\alpha=10$, $\beta=10$, $\gamma=0.0000002$, $\lambda=10$. Without violating any utilization rate thresholds, the score is composed of TNS, Power, and Area, with TNS and Power accounting for the majority. There are a total of 4 instances, all using the 1-bit flip-flop from the library. The power of a 1-bit FF in the sample is 14.781, so $14.781 \times 4 \times \beta = 591.24$. The result should not be lower than this minimum, but in the alpha test result, the best result is 584.6. I don't understand how this score is calculated. Could you demonstrate how to calculate the initial score without altering any content of the sample case?

3. My third question also relates to the sample case. The connection relationships of the instances are reg1->reg2->reg3->reg4, and the initial slack values are set as follows:

TimingSlack reg1 D: -0.183134
TimingSlack reg2 D: 0.149378
TimingSlack reg3 D: -0.152106
TimingSlack reg4 D: 0.150923

I would like to know how these initial values are calculated. If I make no changes, is the

$$\text{TNS} = -0.183134 - 0.152106?$$

4. My fourth question is, if I move reg1 to a new position (from (5952, 3600) to (6000, 4000)), according to Q72, we need to find the starting point, which is reg1. Will the slack value of reg2 be:

$$\text{Slack}_{\text{reg2}} = S_{\text{reg1}} + 0 + \text{DisplacementDelay} \times (|\text{reg2}_x - 6000| + |\text{reg2}_y - 4000|) - (|\text{reg2}_x - 5952| + |\text{reg2}_y - 3600|)$$

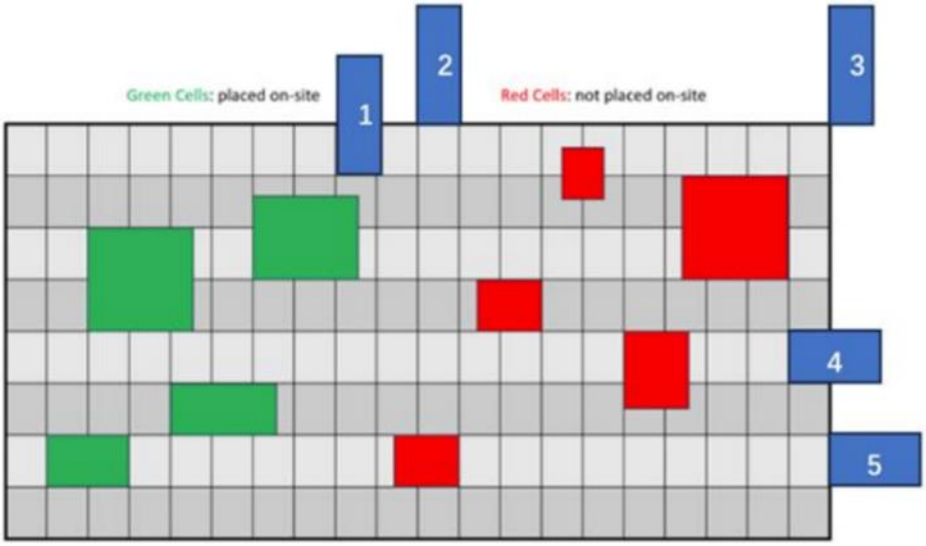
How should the slack value of reg3 be updated based on the change in reg2's slack value? Could you illustrate this using symbols or actual values? When does the information "TimingSlack reg2 D 0.149378" and "TimingSlack reg3 D -0.152106" come into play? Lastly, in what situation is the following formula used?

$$S_{FFN} = S_{FF0} + \delta_0 + \text{DisplacementDelay} * (WL_0^Q + WL_C + WL_N^D)$$

A94.

1. TNS stands for total negative slacks. The lower the better.
2. Please kindly refer to 4.1 Runtime factor on $\log_2$ computation.
3. It is generated by timing analysis tool.
4. Changing the position of reg1 does not change the slack of reg3.

Q95. Hi, I would like to ask about a problem in ICCAD Problem B, as discussed in Q79. If blocks 1, 2, and 3 are all on-site and do not exceed the die boundary, they should be considered a valid solution. However, the released evaluator causes a segmentation fault in this case.



Can you please check if the evaluator can calculate the bin density for blocks 1, 2, and 3 if they do not exceed the boundary of the die?

Can you kindly check if the numBinViolation function, when called within the score function in the evaluator, will not crash in the case mentioned above?

A95. Thank you for your input. The final evaluator can handle this scenario robustly.

Q96. I was testing my program with the provided `preliminary-evaluator`.
I noticed that if there's a multi-output gate, then the negative slack of any flip-flop following a non-first output of the gate would be ignored.

Is this a feature or a bug?
I mean, there might be contestants utilizing this "feature" to get a better score.

A96. Thank you for your feedback. This is a preliminary evaluation method. Please expect final evaluator would consider all output pin slacks.

Q97. When I used the preliminary-evaluator to test my program, I found that if the output of a gate is not the first one (OUT2, OUT3, ...), the slack of their connecting flip-flop won't be take into account. Namely, no penalty for these flipflops.

Please refer to the attached file, the expected final score is 111300, while the preliminary-evaluator gave 1300.

A97. Thank you for your input. The final evaluator can handle this scenario robustly.

Q98. We wanted to bring to your attention an issue we've encountered with testcase3. Specifically, we noticed that instance C73122 is initially a single-bit flip-flop (FF27).

```
76348   Inst C73122 FF27 497250 149100
```

```
635   FlipFlop 1 FF27 11220 2100 3
636   Pin Q 9525 420
637   Pin D 90 980
638   Pin CLK 1620 1540
```

However, there are two separate nets connected to its Q pin.

```
370179   Net net46924 2
370180   Pin C73122/Q
370181   Pin C30010/IN1
```

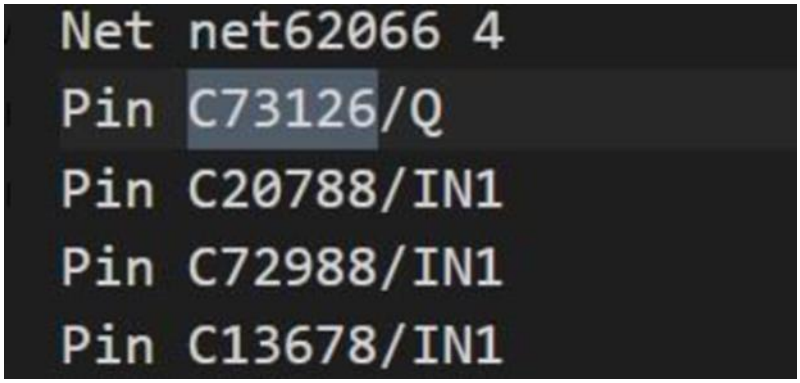
```
433301   Net net62062 3
433302   Pin C73122/Q
433303   Pin C20703/IN2
433304   Pin C22367/IN1
```

This issue is not isolated to C73122.
We have observed similar discrepancies with C73120 and other instances as well.
We would like to report this issue and kindly request an updated version of testcase3 at your earliest convenience.

A98. The Net syntax in this contest describes a part of the net connectivity to the Pins.

Q99. We have encountered an issue while working on Testcase 3. Specifically, we noticed that the same pin appears in two different nets.
Could you please clarify if this is the intended behavior? Should we consider these as separate nets, or should they be treated as a single net?

```
Net net21374 2
Pin C73126/Q
Pin C31400/IN1
```



A99. The Net syntax in this contest describes a part of the net connectivity to the Pins.

Q100. I would like to ask a question about the preliminary checker. The checker said that our output format are correct, but when it calculate the score it results in the segmentation fault(core dumped)

A100. Please note that passing sanity checker does not guarantee success in case submission.

Q101. I am writing to inquire about an issue we encountered while using the preliminary evaluator provided for the competition. We successfully used the evaluator to calculate the final score for testcase2_0812 and testcase3. However, when testing with testcase1_0812, the evaluator passed the test but encountered a segmentation fault while calculating the final score.
We attempted to debug the issue and found that the problem might be related to the "numBinViolation" function within the preliminary evaluator.
Could you please confirm if there might be an issue with the preliminary evaluator itself? Alternatively, is it possible that the scenario we encountered with testcase1_0812 is something that the evaluator did not anticipate, leading to the failure in calculating the final score?

A101. Thank you for your input. The final evaluator can handle this scenario robustly.

Q102. We have observed that a particular pin (INPUT88) is connected to multiple nets, which is generally unusual in circuit. Could you please advise on how we should

handle this situation? Specifically, should we consider these nets as a single net for banking purposes?

A102. The Net syntax in this contest describes a part of the net connectivity to the Pins. Please consider each timing calculated from driver to load.

Q103. Could you please confirm if my binary executable file name, the directory I submitted my file to, and the execution format are all correct? Just to clarify, we execute the .txt files using their names directly, without the inclusion of '<' and '>', correct?

A103. Without the inclusion of '<' and '>' is correct.

Q104. We found that in case3, some pins are defined in multiple nets:

```
Net net65 18
Pin INPUT1
Pin C96058/D0
Pin C96058/D1
Pin C96054/D0
Pin C96054/D1
Pin C96040/D0
```

```
Net net1 2
Pin INPUT1
Pin C61613/D2
```

I'm wondering whether this will be fixed in the final test.

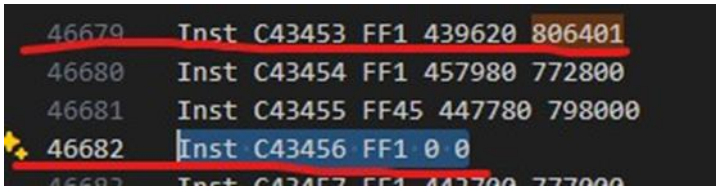
A104. The Net syntax in this contest describes a part of the net connectivity to the Pins.

Q105. When we execute preliminary-evaluator for grading our output of testcase3, everything goes well but the scoring phase.

We pass ALL the checking including, connection, banking, and so on.
But preliminary-evaluator occurs **segmentation fault** when scoring testcase3 which also passes all the checking likewise.
One of our classmates in another group also meets the same problem(preliminary-evaluator segmentation fault)

A105. Thanks for your input. The final evaluator can handle this scenario robustly.

Q106. In addition to the previous issue, we have also encountered another concern regarding the illegal initial placement of instances in testcase3.



Specifically, instances C43453 and C43456 are not positioned on valid sites. Could you please confirm if such placement issues will be addressed in the final testcases?

A106. We expect contestants to handle data input robustly.