CT Verilog Series

My Very First Verilog Coding (Update about Waveform Format)

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聲明

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Update on Generating Waveform

- For IC design flow, not for FPGA design flow
  - Popular Verilog simulators
    - Cadence NCVerilog (or Xcelium)
    - Synopsys VCS
    - Siemens EDA's ModelSim
      - Formerly Mentor Graphics
  - Waveform viewer
    - nWave (one of the components in Synopsys Verdi)

- Synopsys did not support FSDB-format waveform from third-party EDA tools since June 2022

Simulation with Waveform Dumping

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- For Verdi FSDB format, add the following code segment

```
initial begin
  $fsdbDumpfile("majority.fsdb");
  $fsdbDumpvars;
end
```

or `$fsdbDumpvars(0, test);`

Mandatory option! Do not forget it!!

```
$ irun majority_t5.v majority_func.v +access+r
```

Simulation with Waveform Dumping

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- For standard VCD (Value Change Dump) format:

```
initial begin
  $dumpfile("counter.vcd");
  $dumpvars(0, stimulus);
end
```

- For compressed Debussy/Verdi FSDB format:

```
initial begin
  $fsdbDumpfile("counter.fsdb");
  $fsdbDumpvars;
end
```

Invoke the Waveform Viewer

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- Using nWave on Linux workstations
  - One of the components in Verdi

```
$ nWave
```

- You should learn the basic concepts of Linux UI

Two Options to Generate Waveforms

- Using Synopsys VCS
  - Generate FSDB-format waveform (native support)
- Using Cadence NCVerilog (Xcelium)
  - Generate VCD-format waveform
  - Note: VCD format does not support packed-array debugging
    - E.g., `reg [1:0] buffer [0:7]` can not be traced as a packed array in VCD format

Synopsys VCS

- Dump FSDB-format waveform in the testbench

```
initial begin
  $fsdbDumpfile("design_waveform.fsdb");
  $fsdbDumpvars("+all");
end
```

- Simulation command

```
$ vcs testbench.v design.v \
      -full64 -R -debug_access+all +v2k
```

- Launch nWave to open the FSDB waveform file

```
$ nWave design_waveform.fsdb &
```

Cadence NCVerilog (Xcelium)

- Dump VCD-format waveform in the testbench

```
initial begin
  $dumpfile("design_waveform.vcd");
  $dumpvars("+all");
end
```

- Simulation command

```
$ ncverilog testbench.v design.v +access+r
```

- Launch nWave to open the VCD waveform file

```
$ nWave design_waveform.vcd &
```

  - Note that nWave will convert the waveform into FSDB format and save it