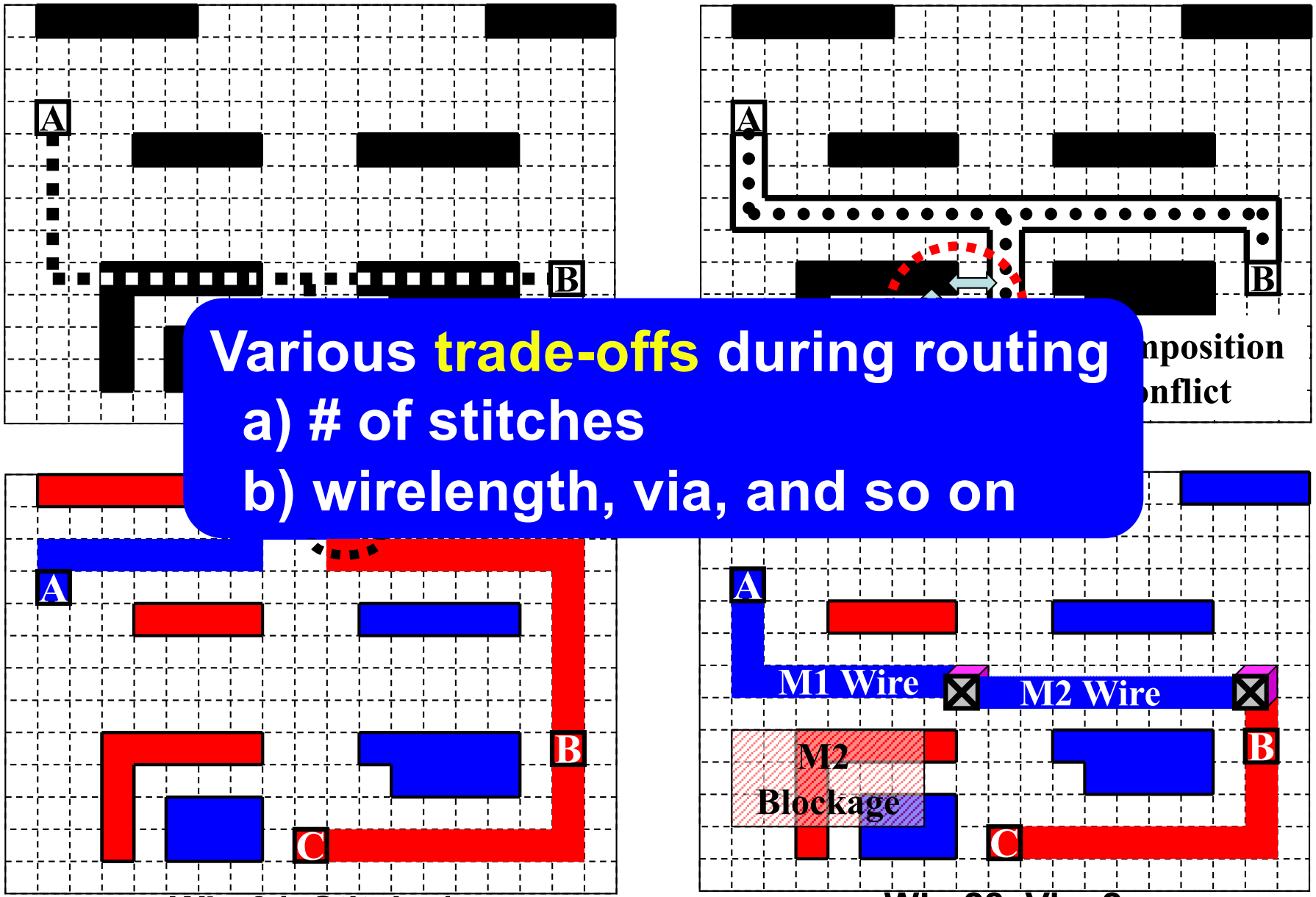
Double/Triple Patterning Aware Detailed Routing

Motivational Example



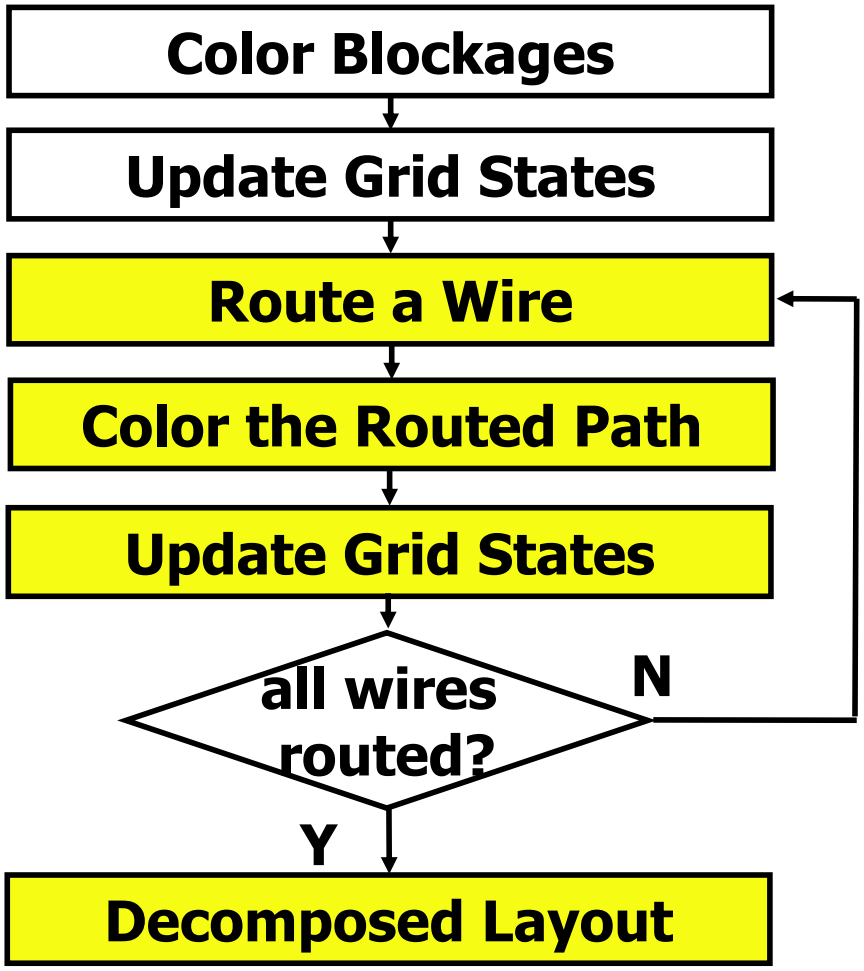
DPL-Aware Routing

- Given
  - Netlist
  - Routing grid
  - Minimum spacing requirement
  - Two masks (colors)
- Objective
  - Route the nets with simultaneous color assignment
  - Minimize the total wirelength, the number of stitches, vias and coloring conflicts

Double Patterning Technology Friendly Detailed Routing

Minsik Cho, Yongchan Ban, David Z. Pan

Overall Flow



- **Simultaneous routing and decomposition**
- No additional step for layout decomposition

Grid State for DPT

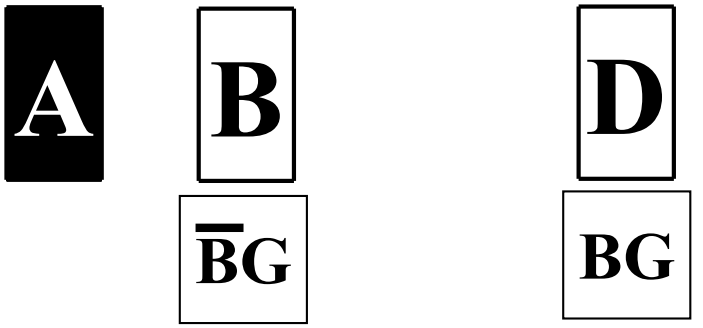
- Four possible states for each routing grid using a 2-bit variable – small overhead

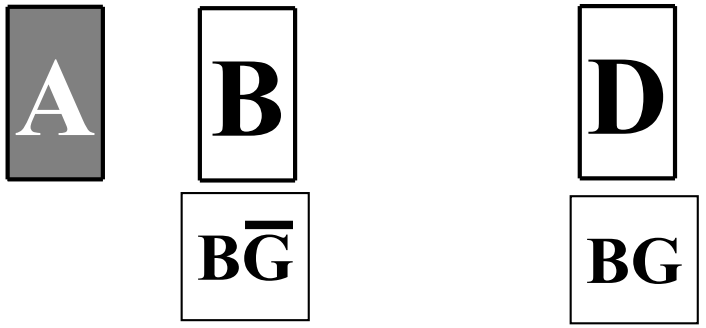
Black-colorable
Existence of grey-colored objects in the proximity

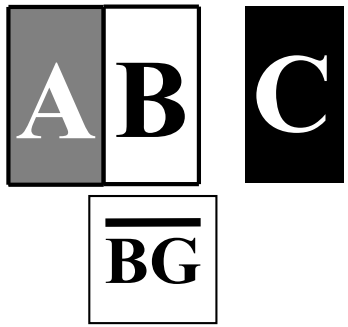
Grey-colorable
Existence of black-colored objects in the proximity

Uncolorable
Existence of grey and black-colored objects in the proximity

Bicolorable
Non-existence of any colored objects in the proximity

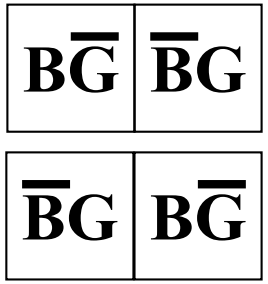






Penalty for DPT-Unfriendly Path

- While finding a path during routing, the following cases along the path are penalized



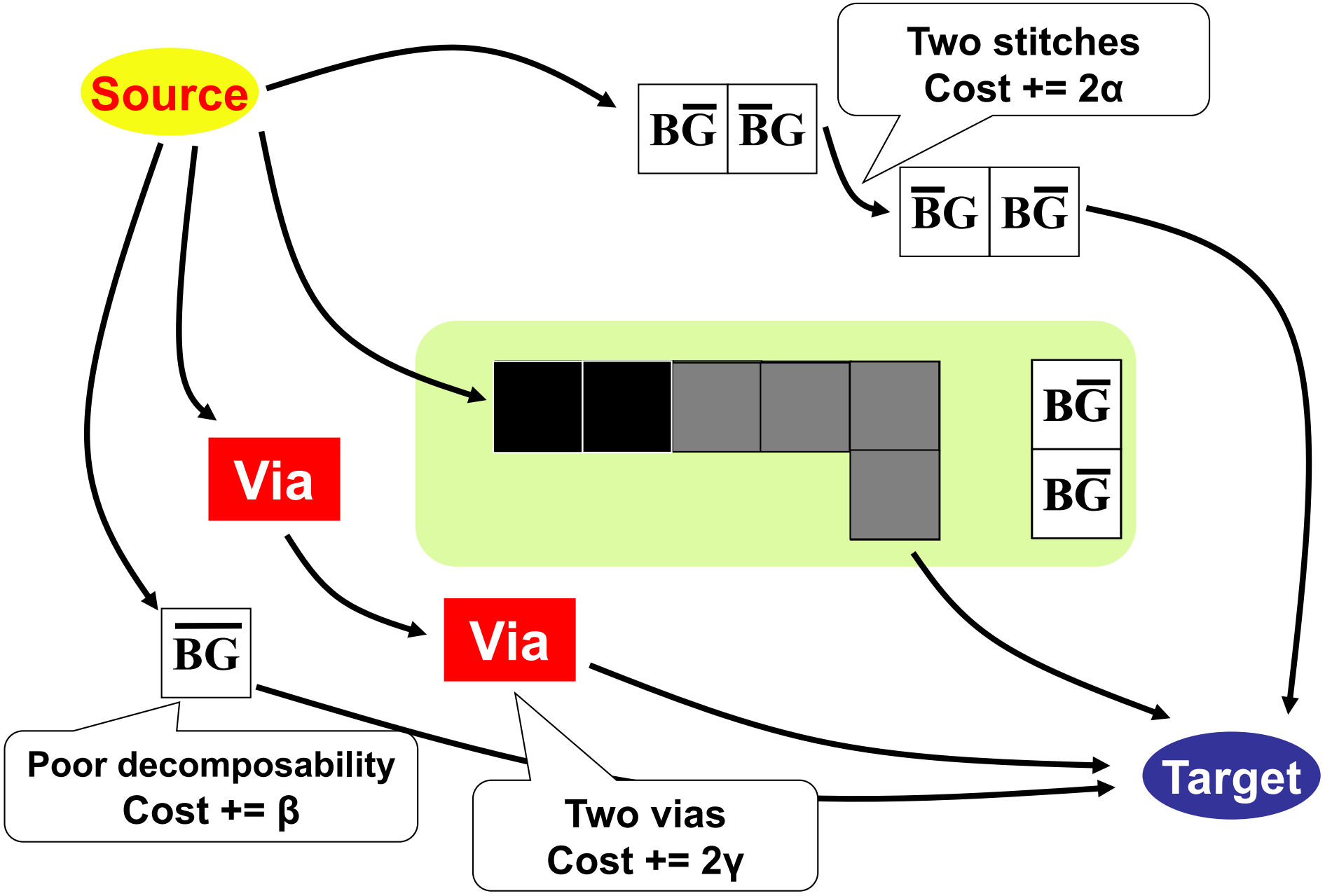
Both cases will introduce a stitch, while coloring the path — **Stitch cost: α**

This case will lead to a uncolorable layout — **Failure: β**

Some colorable path may have many vias to avoid uncolorable grids — **Via cost: γ**

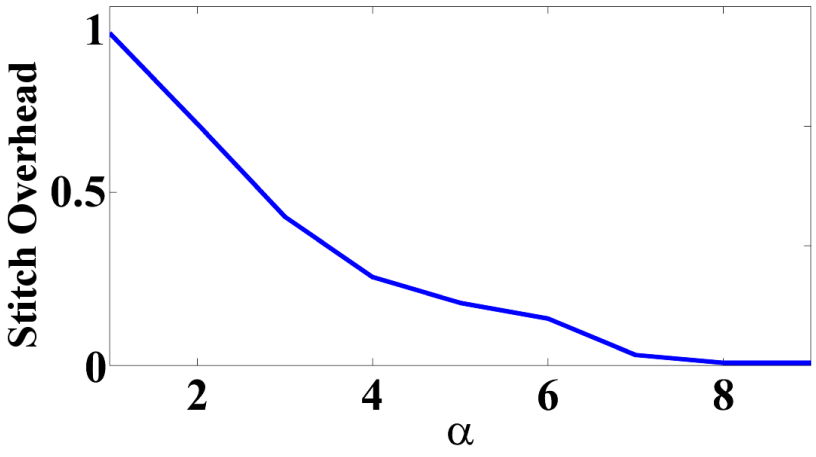
- Perform a detailed routing using the A* search
- Additional cost modification to find a path

Penalty for DPT-Unfriendly Path

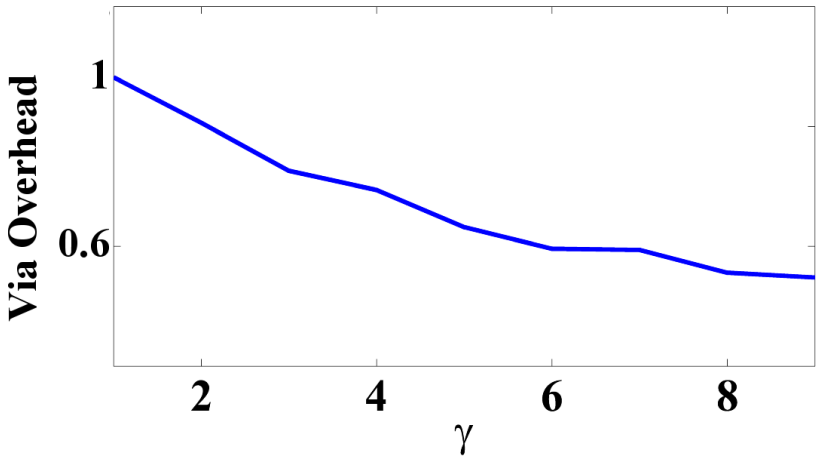


Penalty overhead of the DPFR

- Stitch reduction by α cost



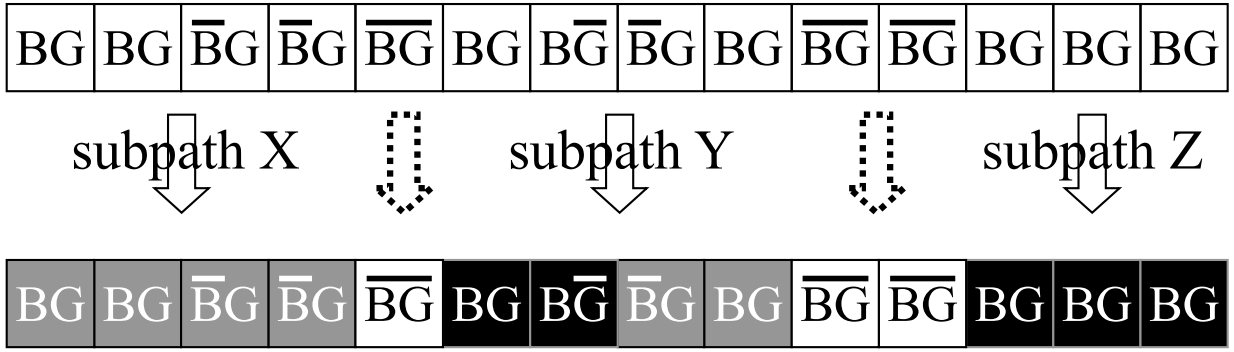
- Via reduction by γ cost



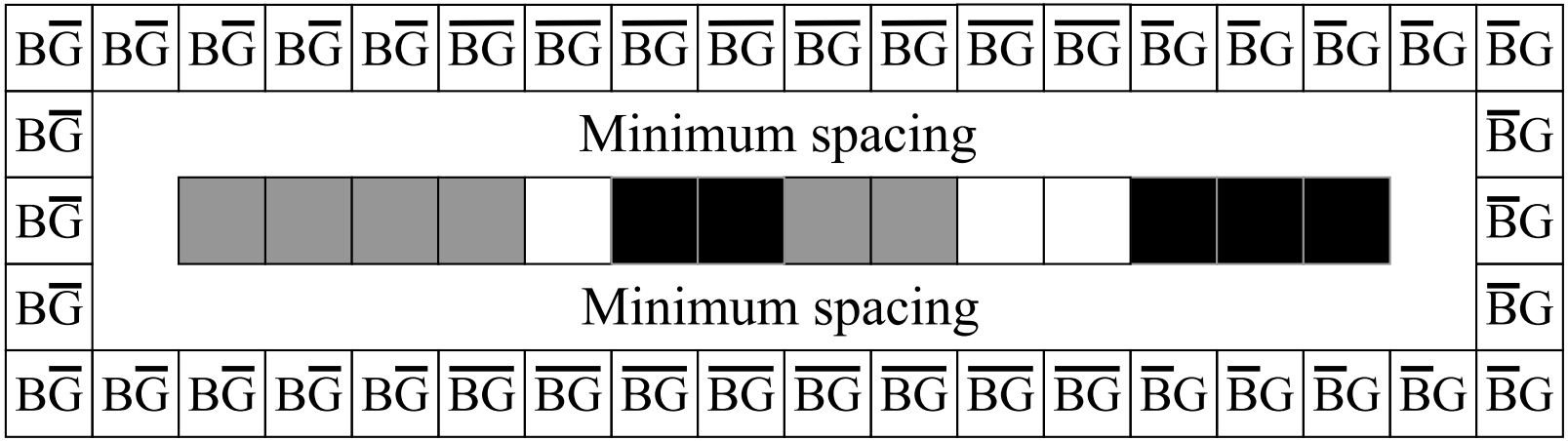
- More α penalty to the routing cost to discourage stitches.
- More γ penalty to decrease the # of vias.
- β » α to minimize the number of uncolored grids.
- **Adjust the penalty costs with the degree of manufacturing difficulty.**

Coloring Path & Shadow

- Routing Path Coloring



- Color Shadow

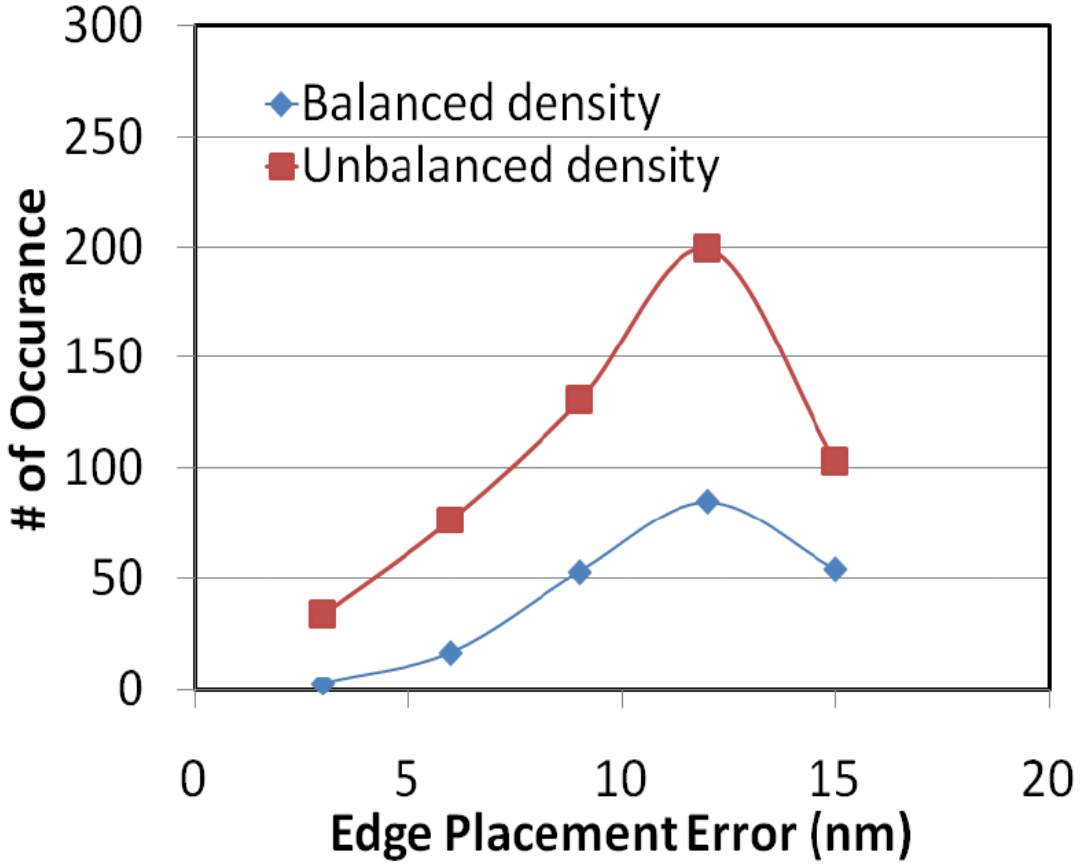


Double Patterning-Aware Detailed Routing with Mask Usage Balancing

Seong-I Lei, Chris Chu and Wai-Kei Mak

Introduction

- Balanced mask usage can enhance layout printability



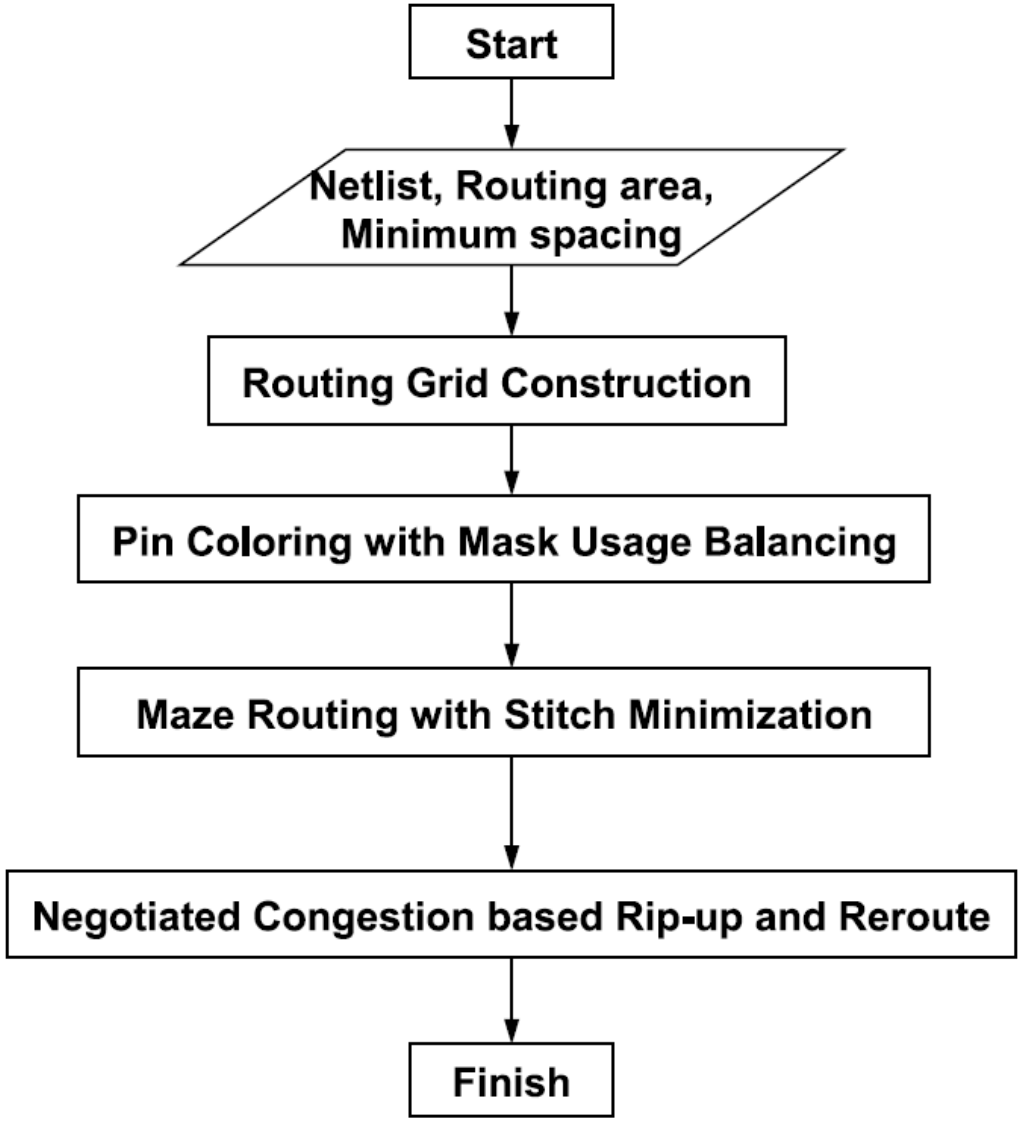
Unbalanced:

RED 27% BLUE 73%

Balanced:

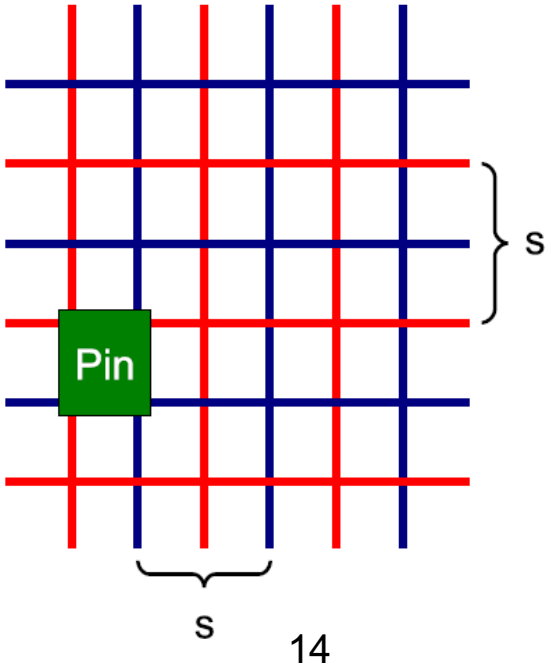
RED 50% BLUE 50%

Overall Flow



Routing Grid Construction

- A uniform grid and the color of each track is defined before routing
- Each track is assigned either RED or BLUE and adjacent tracks in horizontal or vertical direction must be assigned different colors



ILP-Based Pin Coloring with Mask Usage Balancing

- Determine the coloring assignment of a pin for later routing stage.
- Balance the mask usage of the two colors.
- Parameters and variables used in the ILP formulation.

Parameters	
N	the total number of nets
α	the lower bound of the coloring ratio
Variables	
p_a	0-1 integer variable that $p_a = 1$ if pin a is assigned to a RED track and $p_a = 0$ otherwise
s_j	0-1 integer variable that $s_j = 1$ means net j will have at least one stitch and $s_j = 0$ otherwise

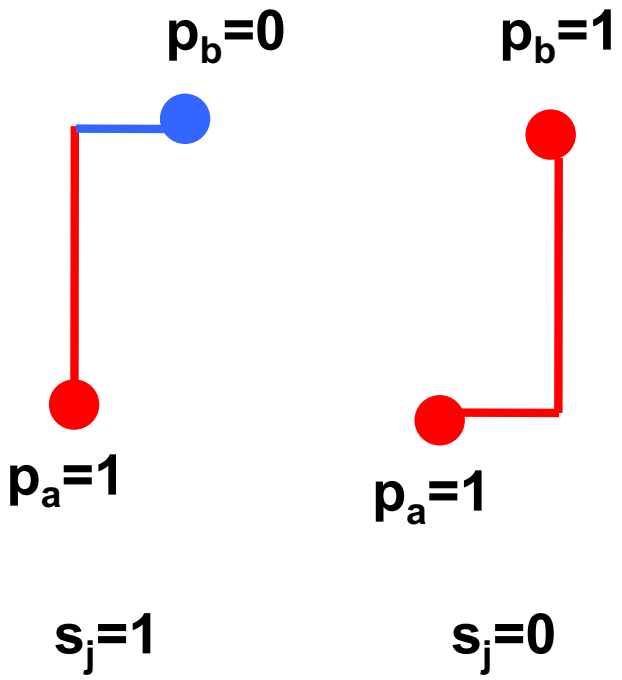
ILP-Based Pin Coloring with Mask Usage Balancing

- The number of stitches is minimized in the objective.

$$min \sum_{j=1}^{N} s_j$$

$$s.t. \quad p_a - p_b \leq s_j \quad \forall \text{net } j(a,b) \qquad (1)$$

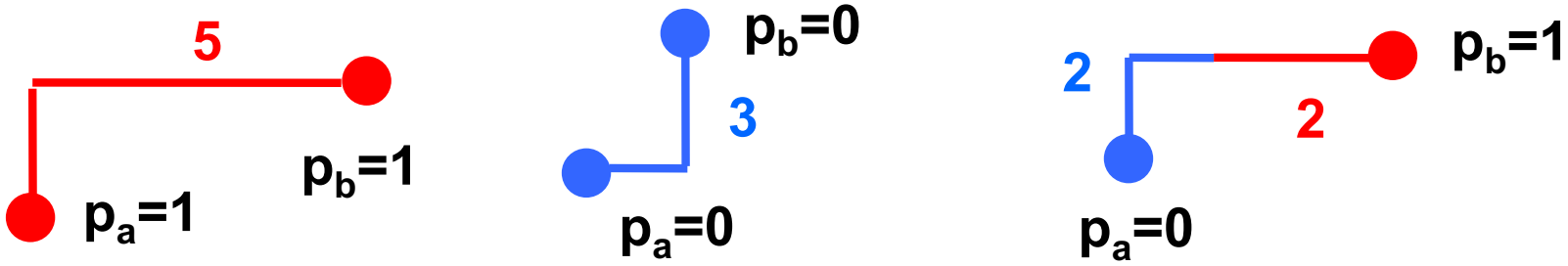
$$p_a - p_b \geq -s_j \quad \forall \text{net } j(a,b) \qquad (2)$$



ILP-Based Pin Coloring with Mask Usage Balancing

- Constraint (3) for mask usage balancing.

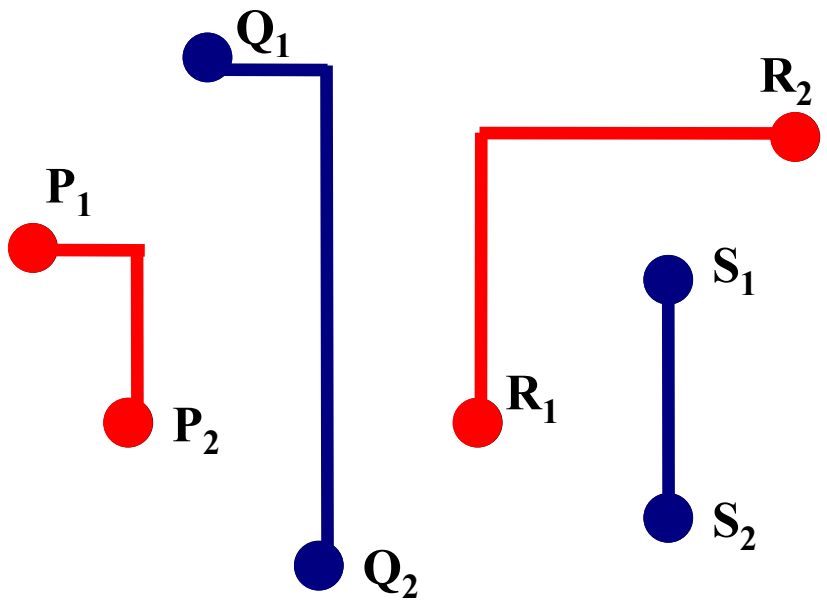
$$\alpha \leq \sum_{j=1}^{N} \frac{0.5HPWL_j}{totalHPWL}(p_a + p_b) \leq 1 - \alpha \qquad (3)$$



RED coloring ratio = (5+0+2)/(5+3+4) = 0.58

ILP-Based Pin Coloring with Mask Usage Balancing

- Pin coloring stage can help to reduce the number of stitches and balance the mask usage.



Maze Routing with Stitch Minimization

- We use A* search algorithm to perform maze routing.
- Minimize WL, the number of stitches and vias.
- If the solution propagates to a different color track, a stitch cost is added to the cost function.
- If the solution propagates to another layer, a via cost is added to the cost function.

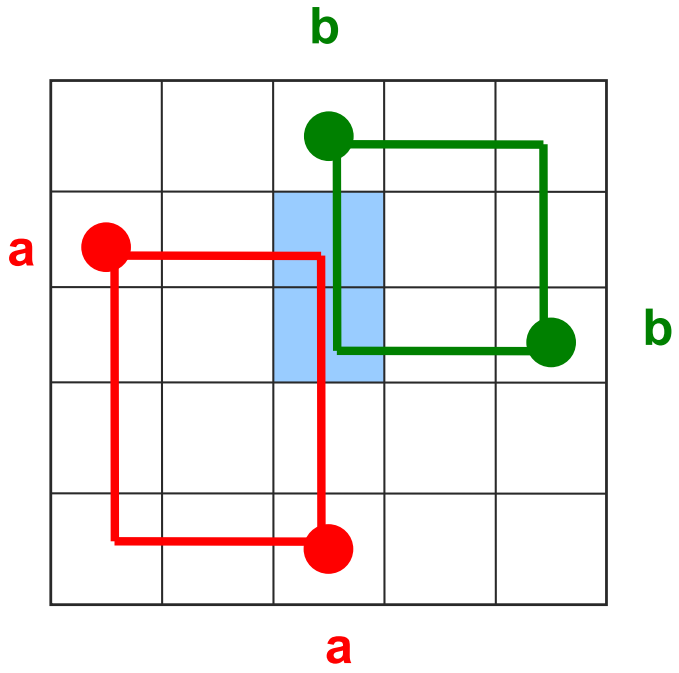
Maze Routing with Stitch Minimization

- After solving the ILP, if the two pins of a net are assigned to the same color, we will perform the maze routing using only the tracks of that color.

- Otherwise, we perform the maze routing using all the tracks.

Negotiated Congestion based Rip-up and Reroute

- We adopt a negotiated congestion based routing scheme in rip-up and reroute.

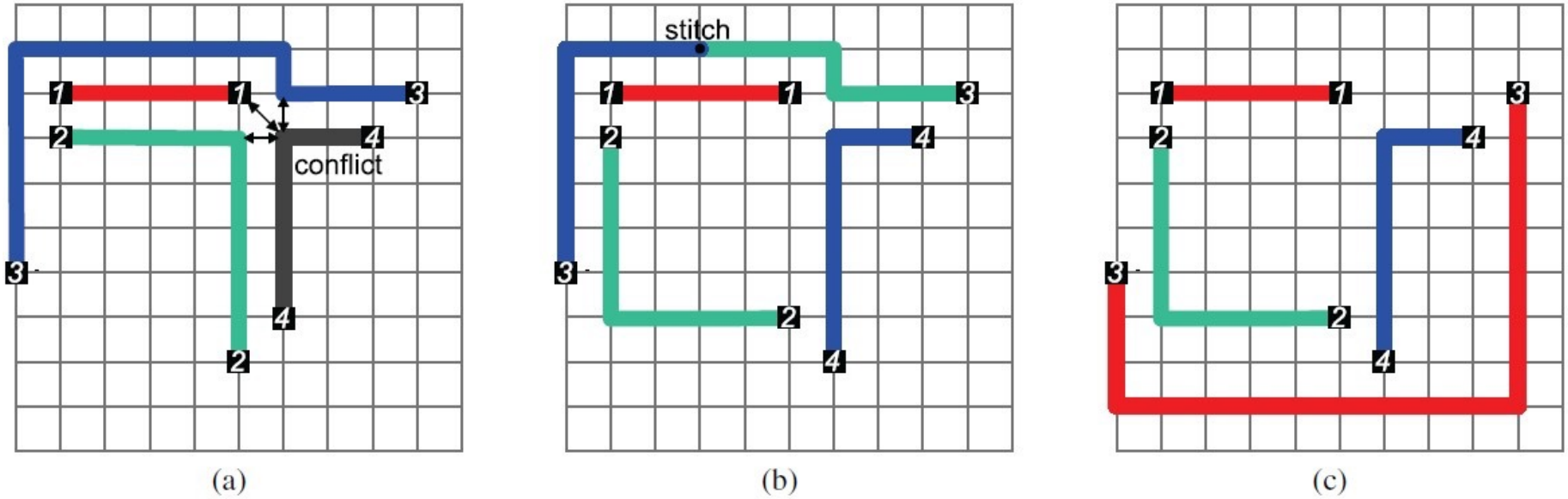


TPL Aware Routing and Its Comparison with Double Patterning Aware Routing in 14nm Technology

Q. Ma, H. Zhang, M.D.F. Wong

TPL Aware Routing

- Most hard-to-decompose features are generated during the routing stage
- Considering TPL during routing can improve the layout decomposability

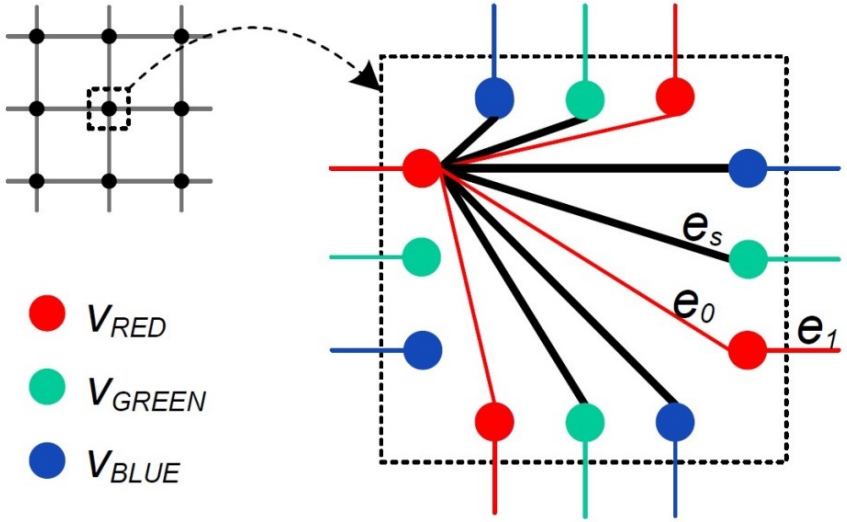


TPL Aware Routing

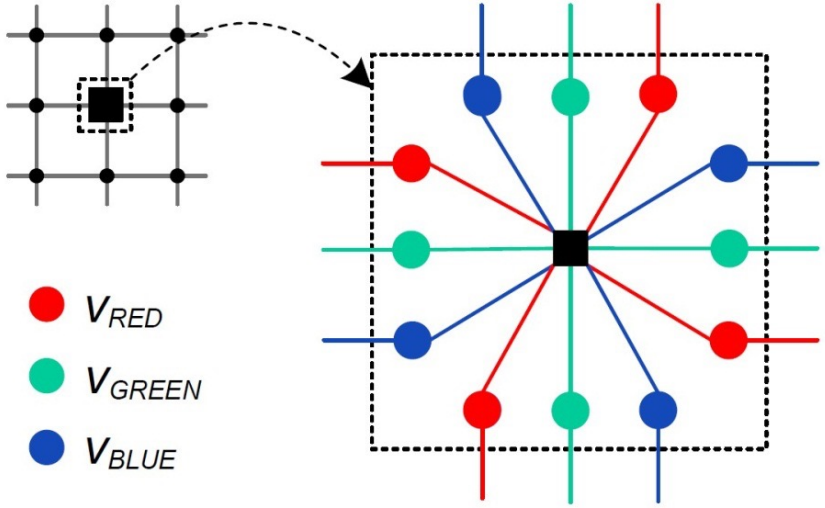
- Given
  - Netlist
  - Routing grid
  - Minimum spacing requirement
  - Three masks (colors)
- Objective
  - Route the nets with simultaneous color assignment
  - Minimize total color-conflicting wire length
  - Minimize number of stitches

TPL Aware Maze Routing

- Route a single net
  - In presence of previously routed nets with color assignment
  - Minimize weighted sum of wire-length, color-conflicting wire-length and number of stitches
- Graph splitting approach



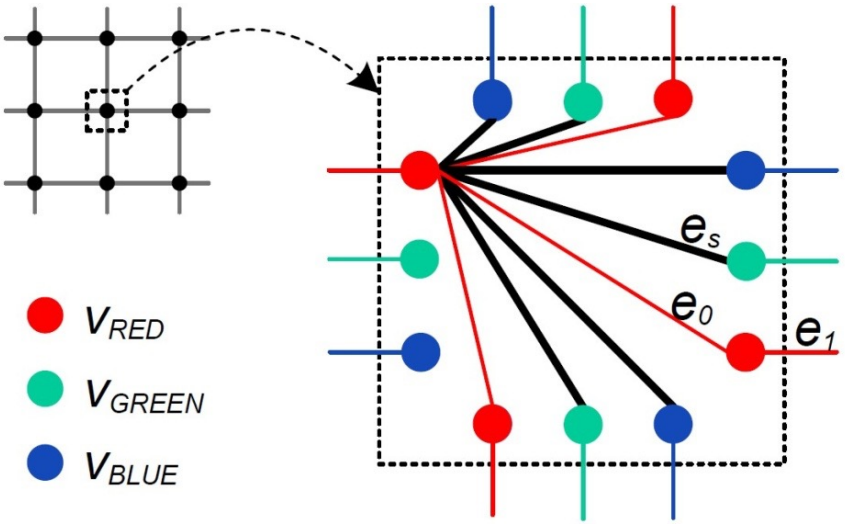
Graph model for a non-terminal vertex



Graph model for a terminal vertex

TPL Aware Maze Routing (Cont')

- Graph splitting approach
  - Each intersection is modeled by a set of 12 nodes with associated edges
  - At each intersection, type e_s edge implies the use of a stitch while type e_0 edge implies no stitch used there
  - Type e_1 edge between two same colored nodes from adjacent intersections

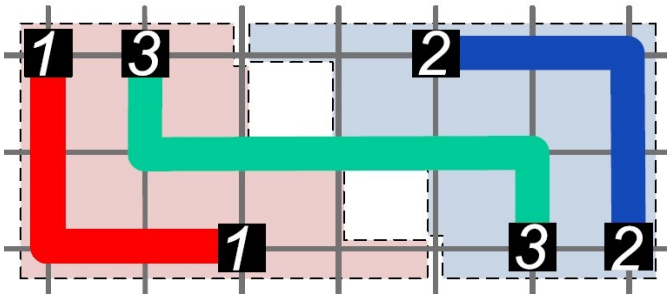


cost of type e_0 edge = 0
cost of type e_s edge = penalty of a stitch

cost of type e_1 edge
= 1 if no conflict with any previously routed and colored nets;
or 1 + penalty of a unit of color-conflicting wire length, otherwise

TPL Aware Maze Routing (Cont')

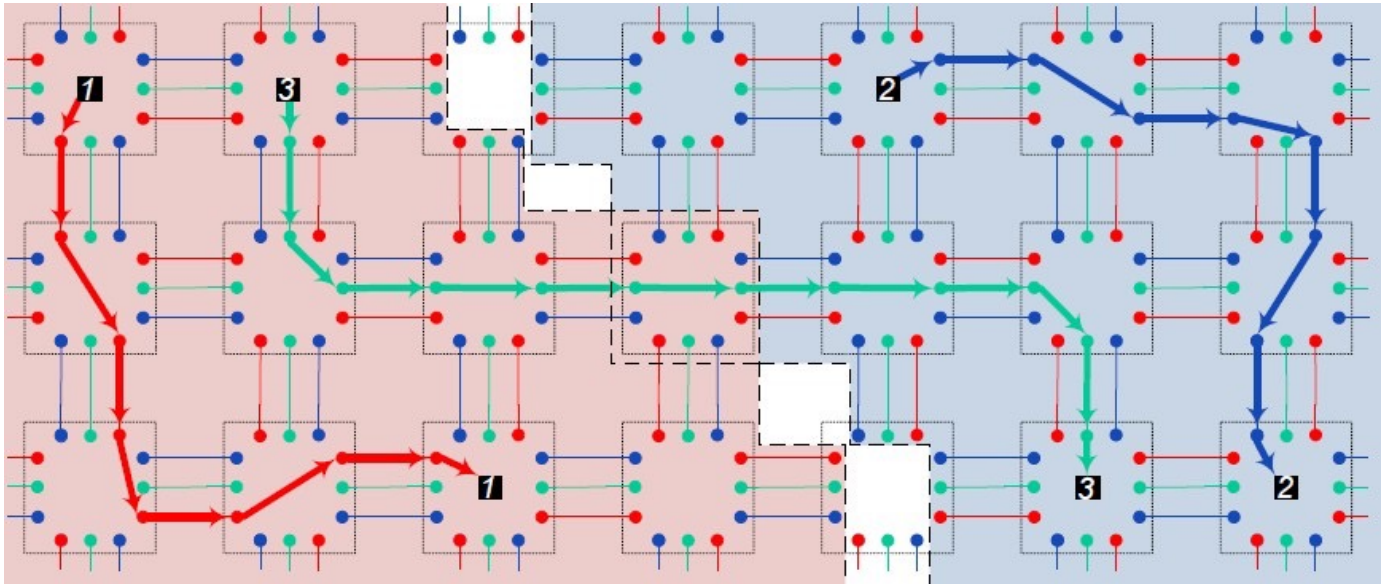
- Example



Routes on the original grid

Assume net routing order is: 1, 2, 3

blue conflict region after routing & coloring net 2

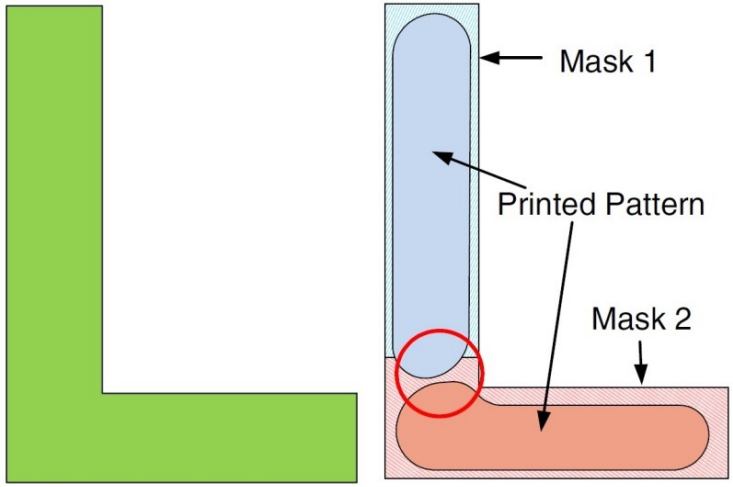


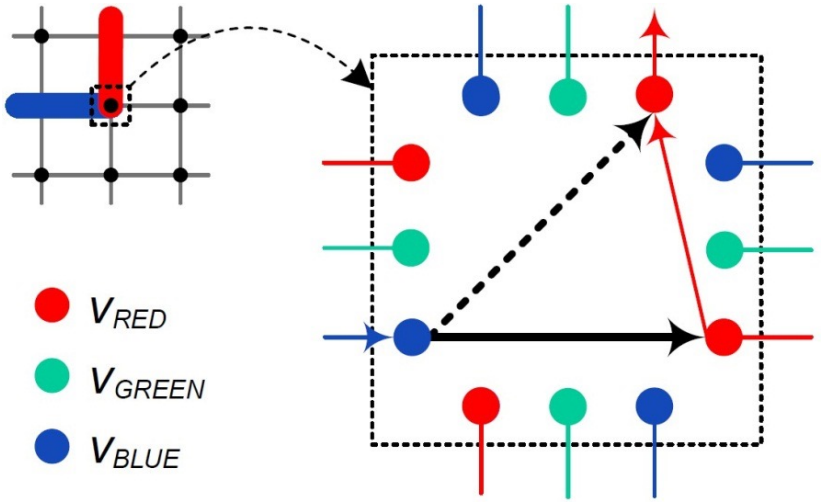
Routes on the expanded graph

red conflict region after routing & coloring net 1

Forbidding Stitch at Corner

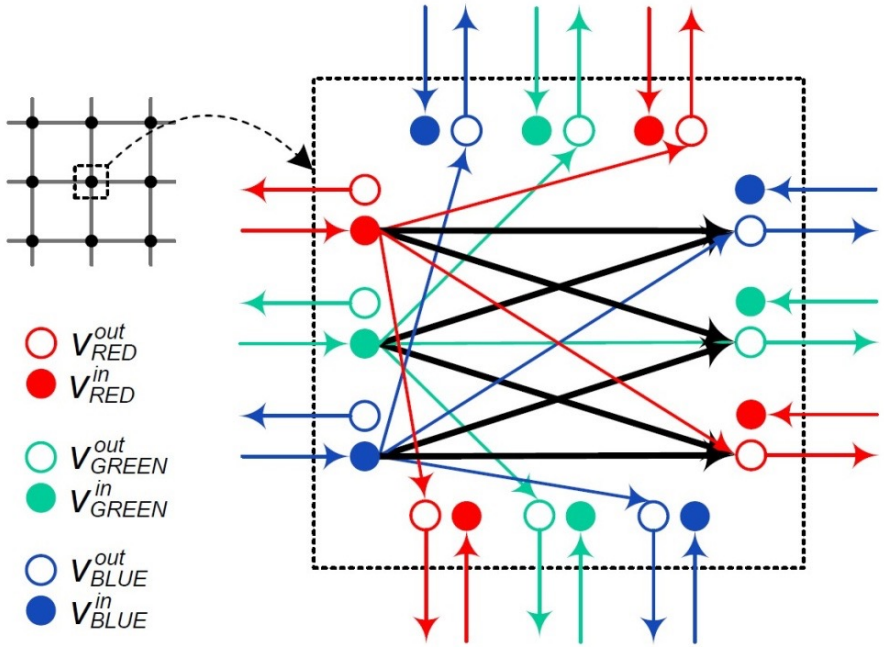
- Corner stitch is undesirable
  - Overlay error
  - Line-end effect
- Adapt our graph model to forbid stitch at corner
  - Remove the edges corresponding to corner stitches
  - Not done yet!



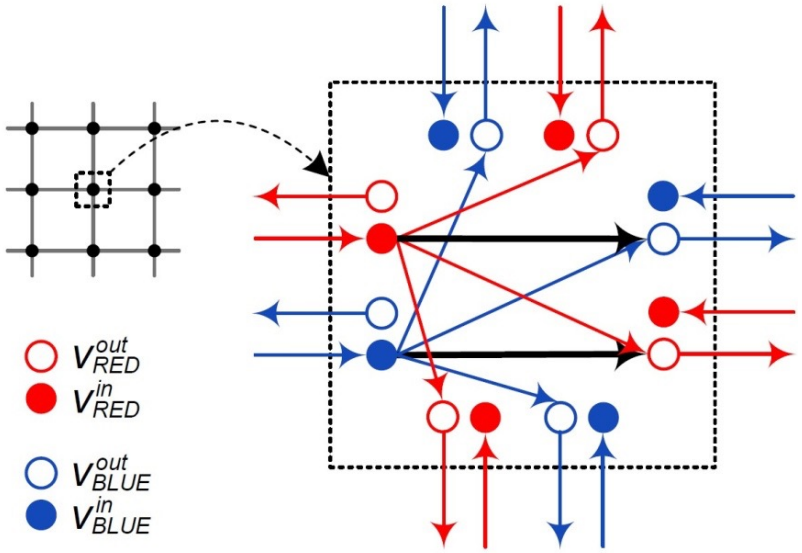


Forbidding Stitch at Corner (Cont')

- Further split the graph
  - Each vertex *v* is split into v^{in} *and* v^{out}
  - Each edge within the original graph model is directed from a v^{in} to a v^{out}



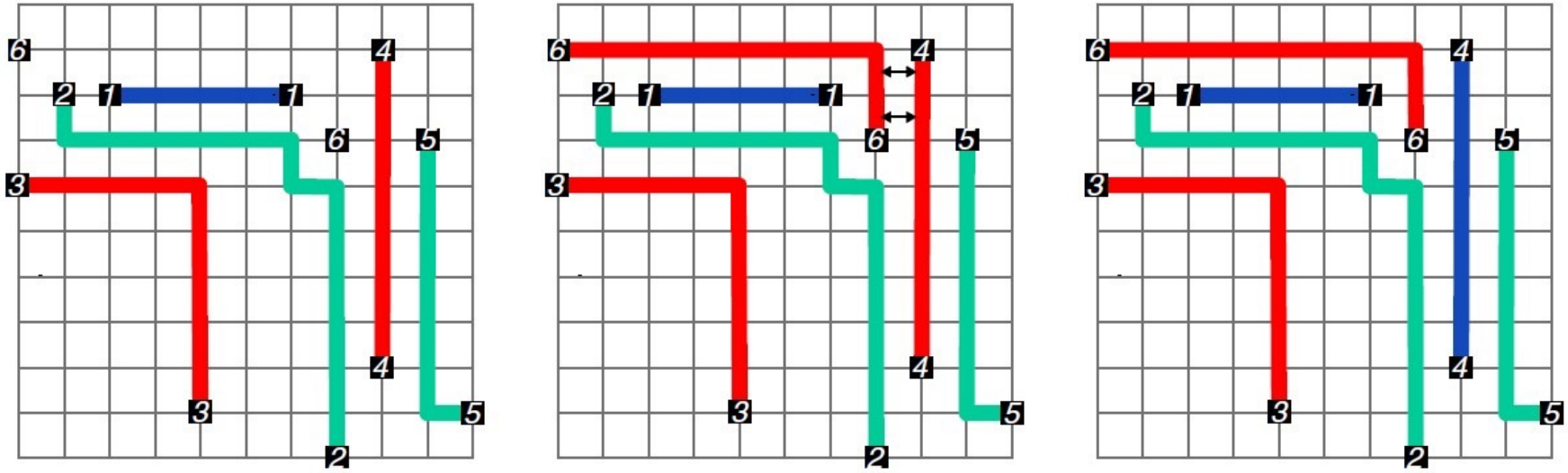
Graph model for TPL



Graph model for DPL

Overall Routing Scheme

- Route all nets one by one without resource sharing
- Edges where color-conflicts occurred become more costly
- Nets with color-conflicts are iteratively rerouted



Overall Routing Scheme (Cont')

- Balancing features on three masks
  - Ensures that each mask is fully utilized
  - Helps the printability enhancement
- We effectively control the balancing on the fly
  - Keep track of the total wire length in each color l_{Red} ,l_{Green} ,l_{Blue}
  - Set edge cost proportional to total wire length in each color
    - $c_{Red} / l_{Red} = c_{Green} / l_{Green} = c_{Blue} / l_{Blue}$
    - The more edges in this color are used, the more expensive the edges in this color will be

References

- [Cho+ ICCAD08] Double Patterning Technology Friendly Detailed Routing
- [Lei+ ISQED2014] Double Patterning-Aware Detailed Routing with Mask Usage Balancing
- [Ma+ DAC2012] TPL Aware Routing and Its Comparison with Double Patterning Aware Routing in 14nm Technology