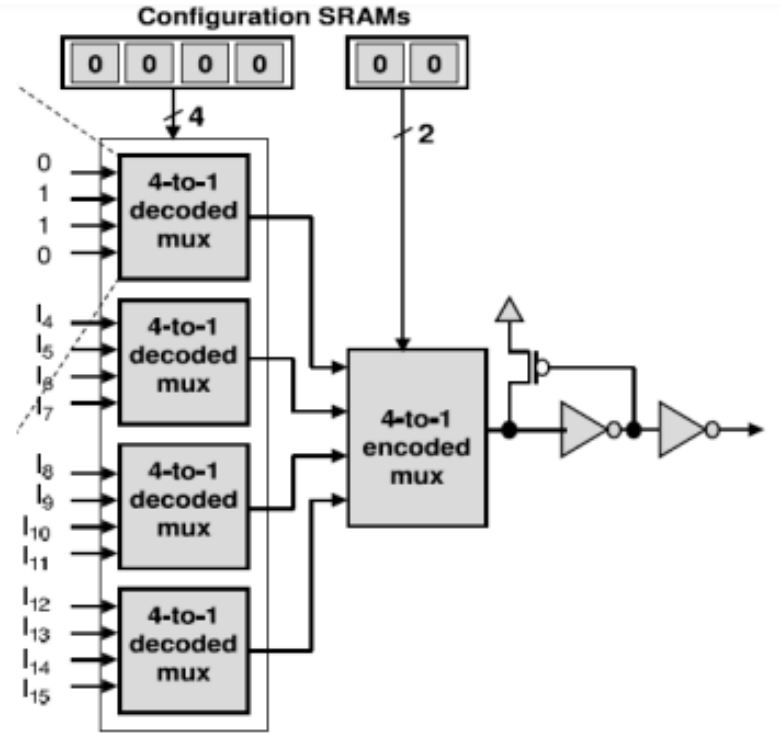
CS 516000 FPGA Architecture & CAD

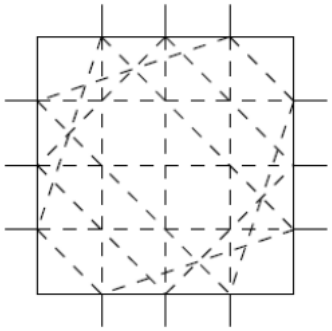
Homework 2 (Due: 2024/10/17)

1. Prove or disapprove that any 4-variable function can be implemented by no more than three 3-input LUTs?

2. What is the advantage of constructing a 16-to-1 multiplexers as below rather than using five 4-to-1 encoded MUXes as building blocks?

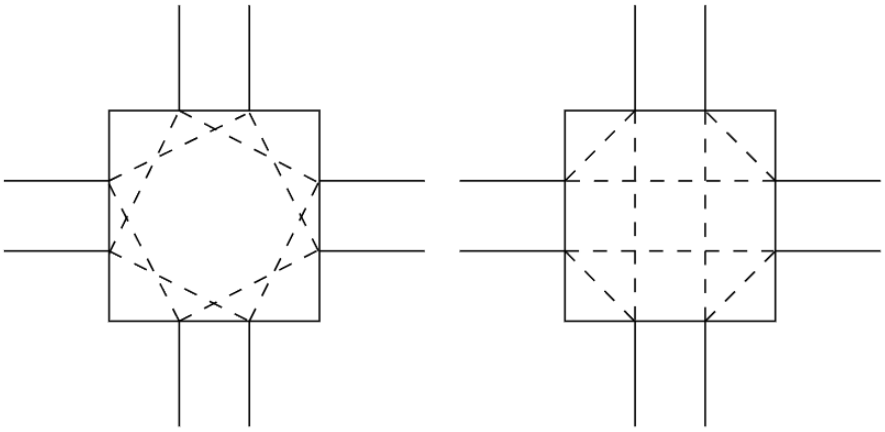


3. (a) What is the switch block flexibility value F_s of the switch block structure shown below?



(b) Is RRV (2, 1, 0, 1, 0, 1) routable on the switch block structure above? If it is routable, draw the connections of the switch block.

(c) Consider two switch blocks below with the same $F_s = 2$. Do they have the same number of routable RRVs? Explain your answer.



Switch Block A Switch Block B

4. (a) What are the advantages and disadvantages of pass transistor switches and tri-state buffer switches in FPGAs?

   (b) Since the chip capacity is growing much faster than package pinout, the number of interconnect lines between FPGAs is often much smaller than the required number of signals. What is the commonly used technique to solve this problem? Briefly explain the technique.

5. Refer to the Adaptive Logic Module (ALM) shown on the lecture note Unit 8 page 20, give a mapping using a minimum number of ALMs.