CS5120 VLSI System Design, Spring 2024

Design for Testability (DFT) with Scan Technique

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Outline

- Why IC testing?
- Fault Modeling
- Scan Test
- Other DFT Techniques
- Verilog Coding Style vs. DFT

Why IC Testing?

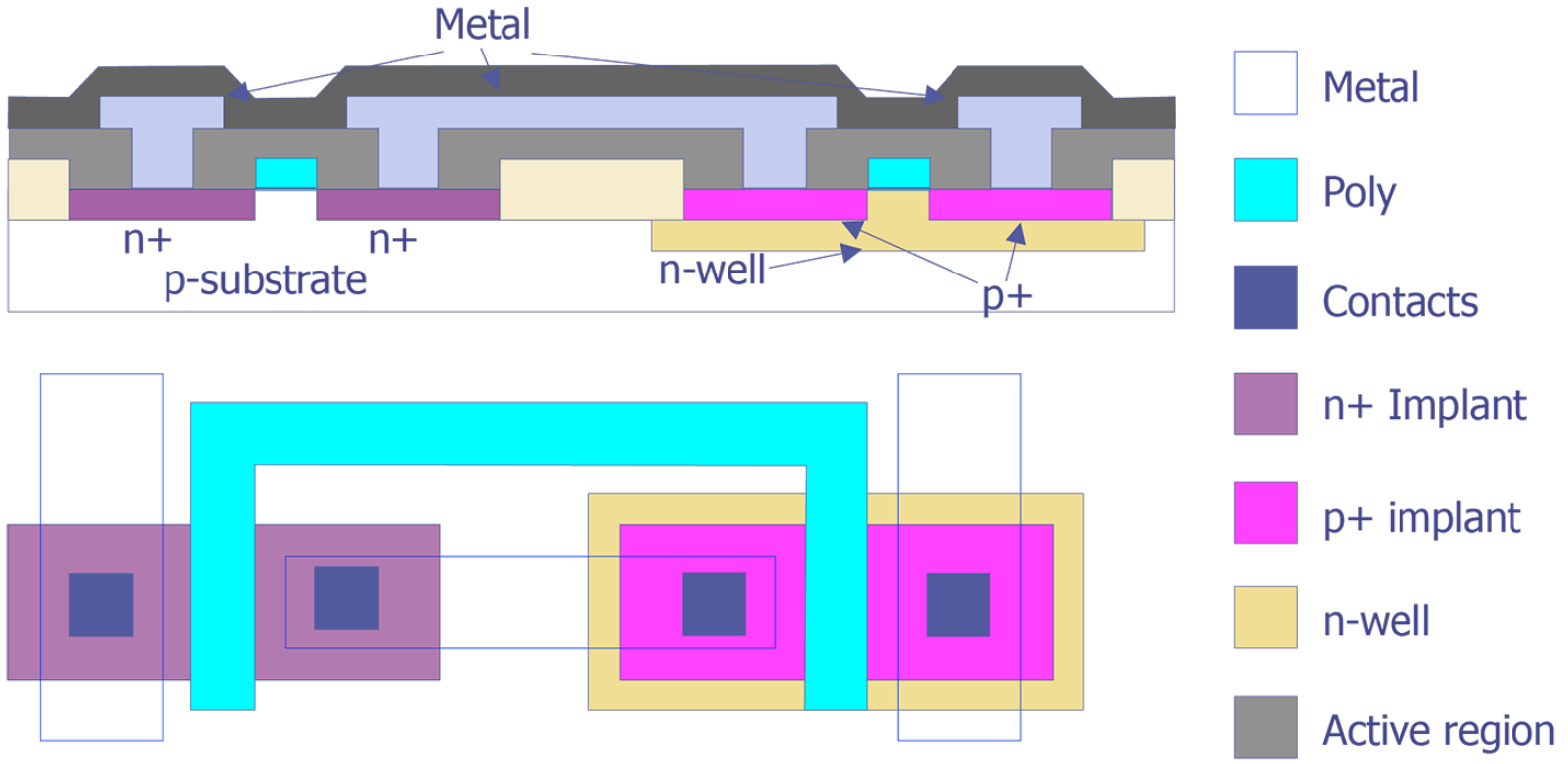
- Semiconductor testing

IC Production

- IC Design (with only simulation) is not the final goal
  - Without production, your design is not real
- IC manufacturing
  - Design
    - Debugging/verification
  - Test chip – shuttle bus
    - Post-silicon validation
  - IC production, assembly and test
    - Pilot run
    - Yield ramp-up
    - Mass production

IC Fabrication Process

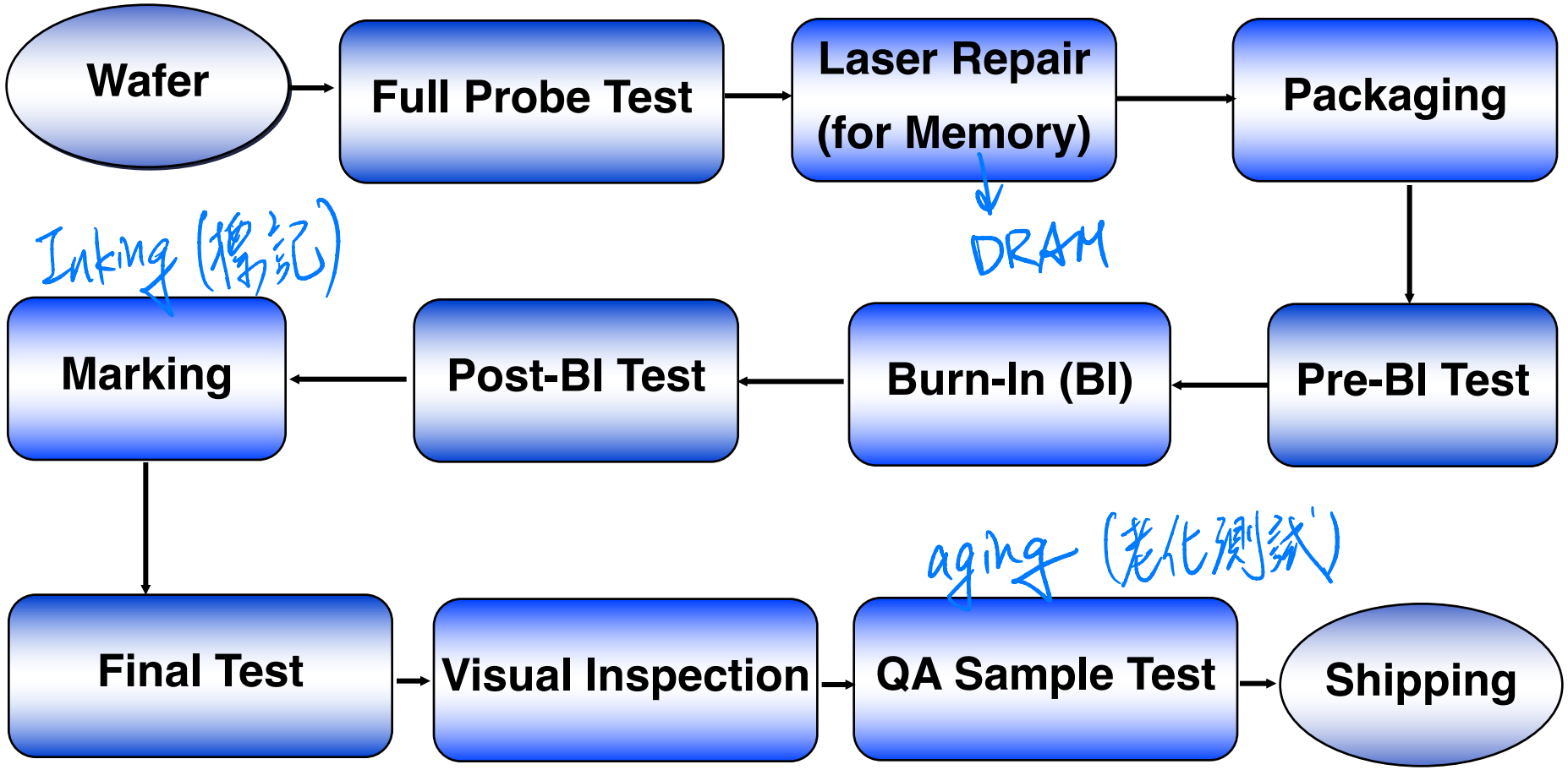
- Lithography
- Etching
- Deposition
- Chemical mechanical polishing (CMP)
- Oxidation
- Ion implantation
- Diffusion



Layout Example

https://www.semitracks.com/reference-material/design/device-recognition.php

Typical IC Production Flow (After Fabrication)



Why Testing?

- Purpose of product test: to guarantee quality, reliability, performance, etc.

Defect detected during IC test

Defect detected during system test

Defect detected during field test

Fault Modeling

- Yield (Y) is the ratio of # good dies per wafer to # dies per wafer, or the fraction of dies that are produced free of defects
  - $Y = \frac{\text{\# good dies}}{\text{\# total dies}} = \frac{50}{100} = 50\%$
- Defect level (DL) is the fraction of bad parts among the parts that pass all tests and are shipped
  - $DL = 1 - Y^{(1-FC)}$
- Fault coverage (FC) refers to the real defect coverage (probability that T (test) detects any possible fault – in F or not)
- DL is measured in terms of DPM (defects per million)

PPM (parts per million)

Design for Testability

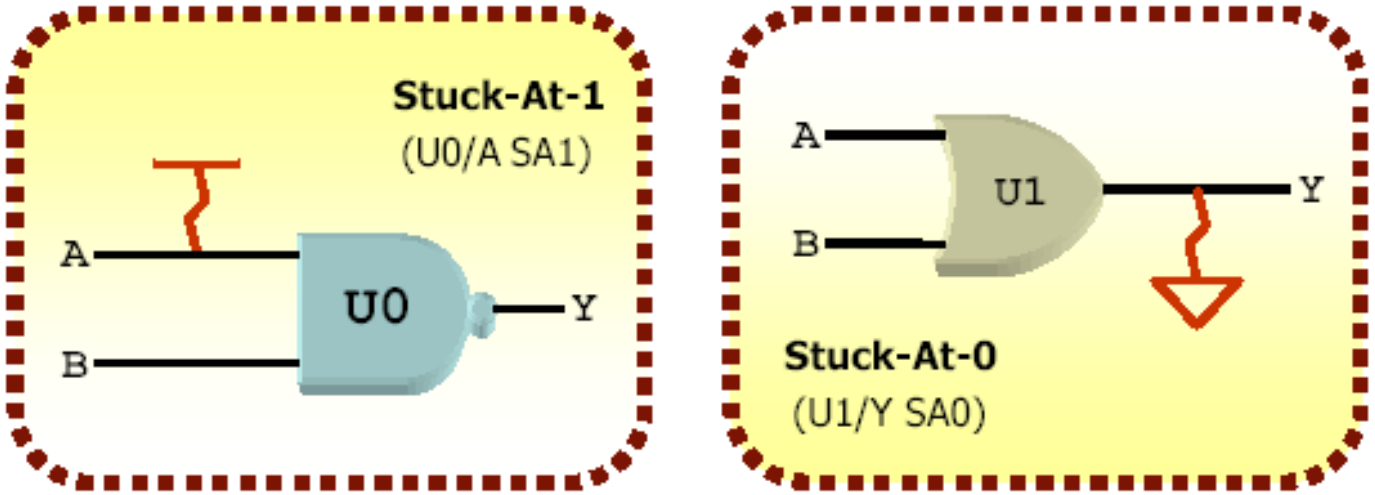
- Or Design for Test, DFT
  - IC design techniques that add testability features to a hardware design
  - Facilitate the manufacturing tests to the designed hardware
- Fault modeling
- Scan test
- Software-based test
- Built-In Self Test (BIST)
- Boundary scan

Fault Modeling

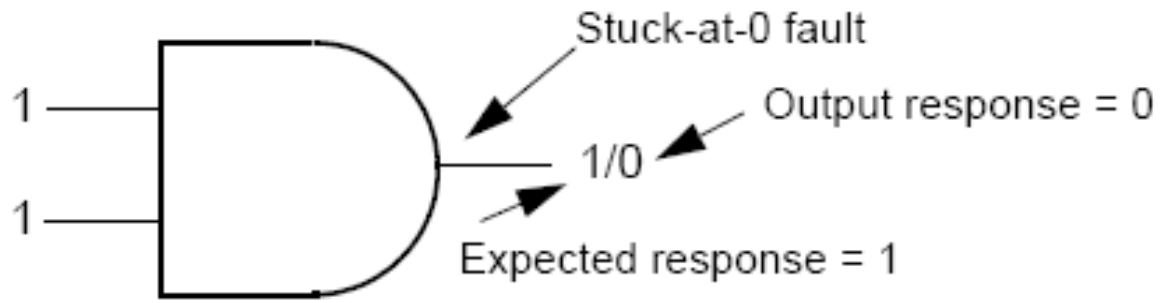
Logical Fault Model

- # physical defects is countless!!
- Simple *logical* model: independent of technology details
  - Stuck-at faults (s-a-1 and s-a-0) (short faults)
  - Stuck-open faults (open faults)
  - Bridging faults (short faults)
  - Timing faults (delay faults)
- Reducing the complexity of fault detection algorithm
- Applicable to any physical defect manifesting as a signal that is stuck at a fixed logic level
- One stuck-at fault can model one or more kinds of defects
  - Generally we apply single stuck-at fault model to evaluate test patterns for real cases with multiple faults

Stuck-At Faults

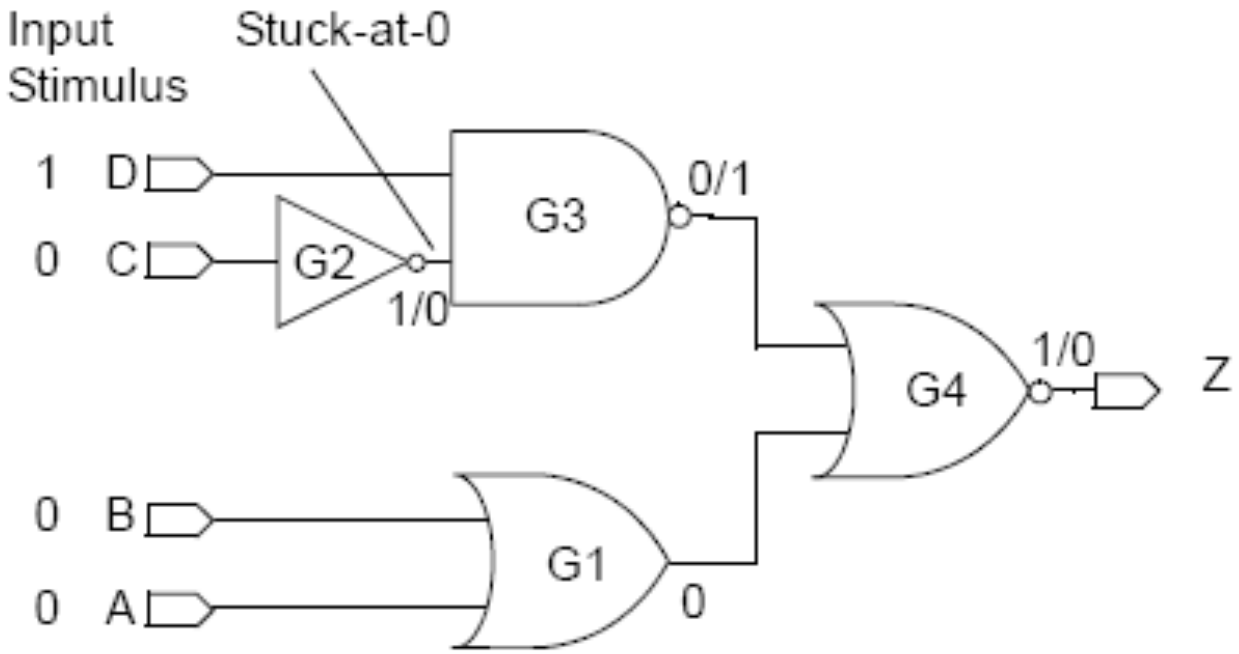


Two-Input AND Gate With Stuck-At-0 Fault on Output Pin

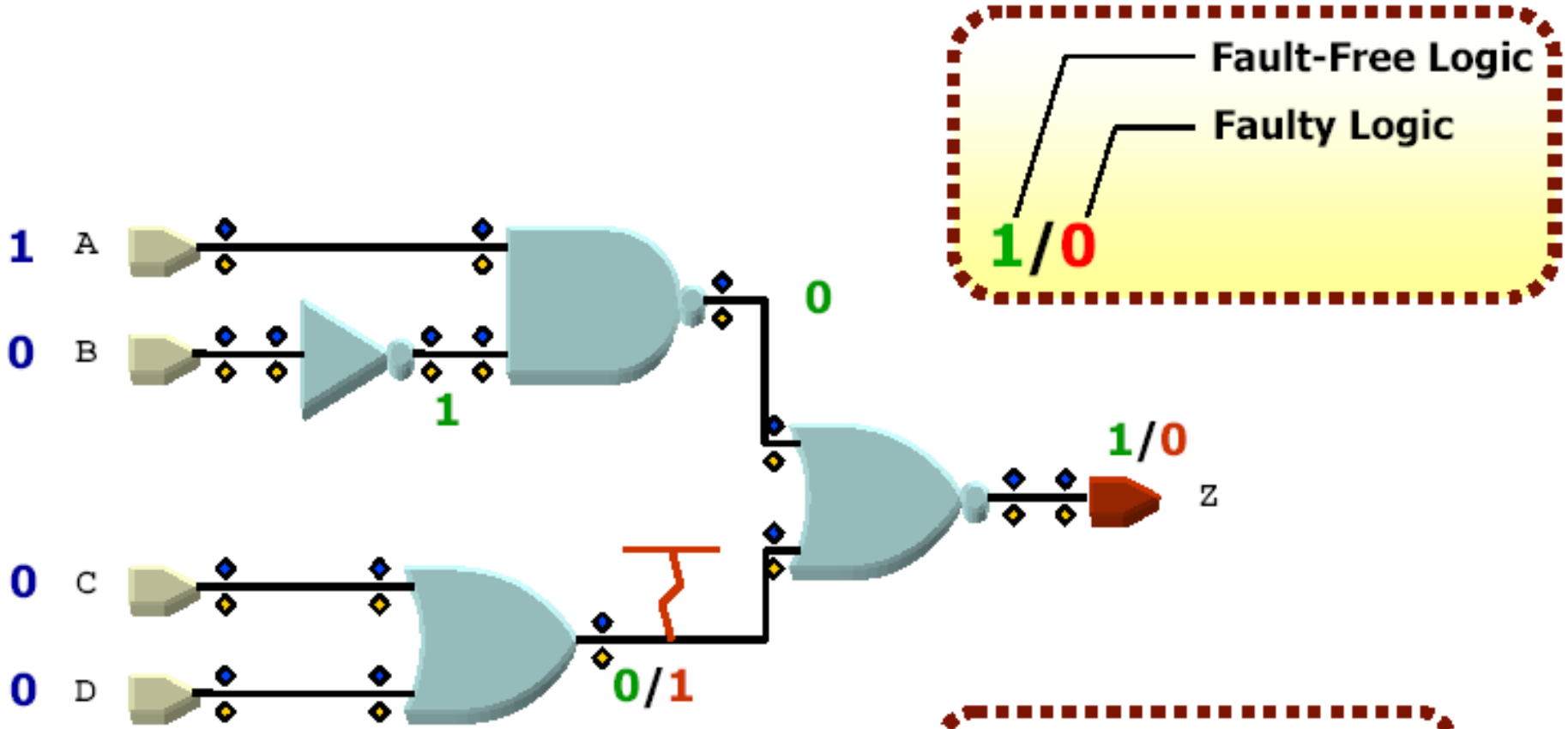


Fault Detection

- Controllability
- Observability
- Single stuck-at fault model
  - Single-fault vs. multiple-fault model
  - Greatly reduces the complexity
  - Acceptable defect coverage from industrial experience



Fault List



Total Faults

$$N_f = 2(N_{pins} + N_{ports}) = 2(11 + 5) = 32$$

Fault Coverage

- $FC = \dfrac{\#\text{ detected faults}}{(\#\text{ total faults} - \#\text{ of undetectable faults})}$
- Fault simulation
  - Determines all faults detected by a test vector
  - Logic simulation
    - Fault-free circuit
  - Fault injection
    - Faulty circuit

Scan Test

ATPG (Automatic Test Pattern Generation)

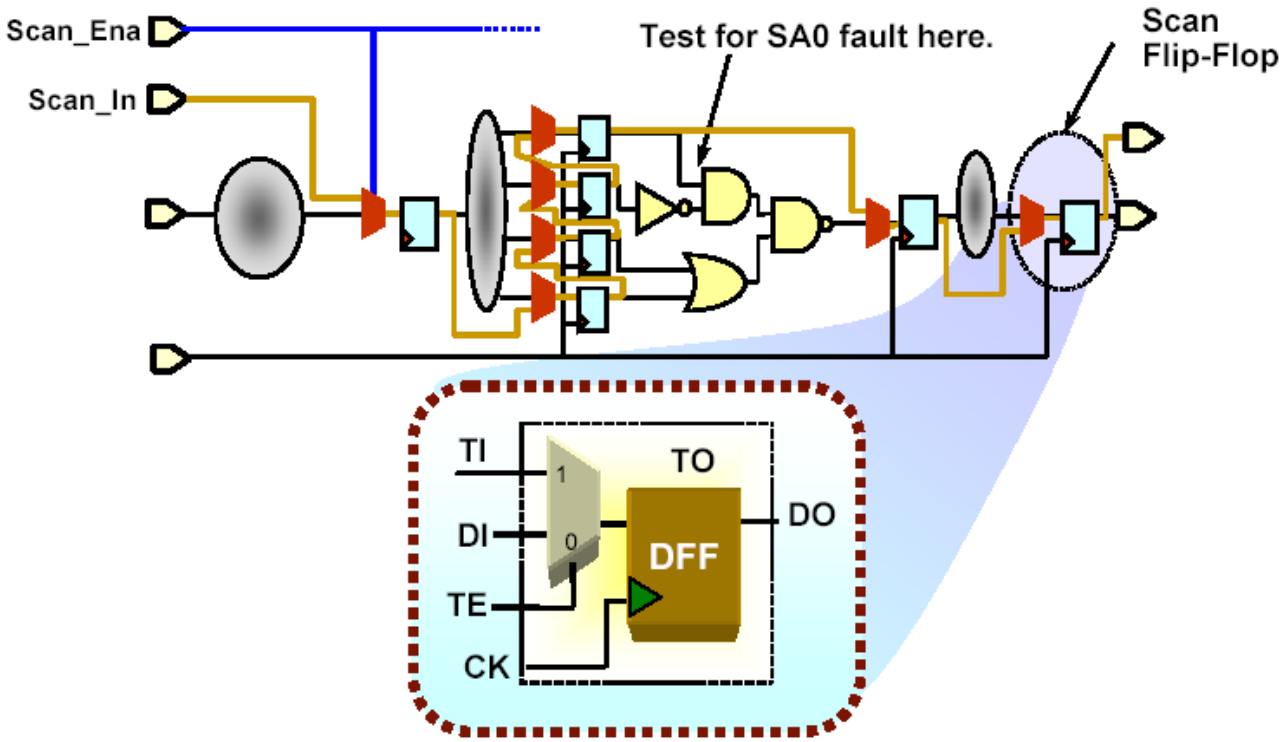
- ATPG generates test patterns with fault coverage statistics
  - Random pattern generation technique
  - Deterministic pattern generation technique
- Well understood for combinational circuits
- Not efficient for sequential circuits
  - Coverage is not high enough
- Structure DFT techniques
  - Internal scan

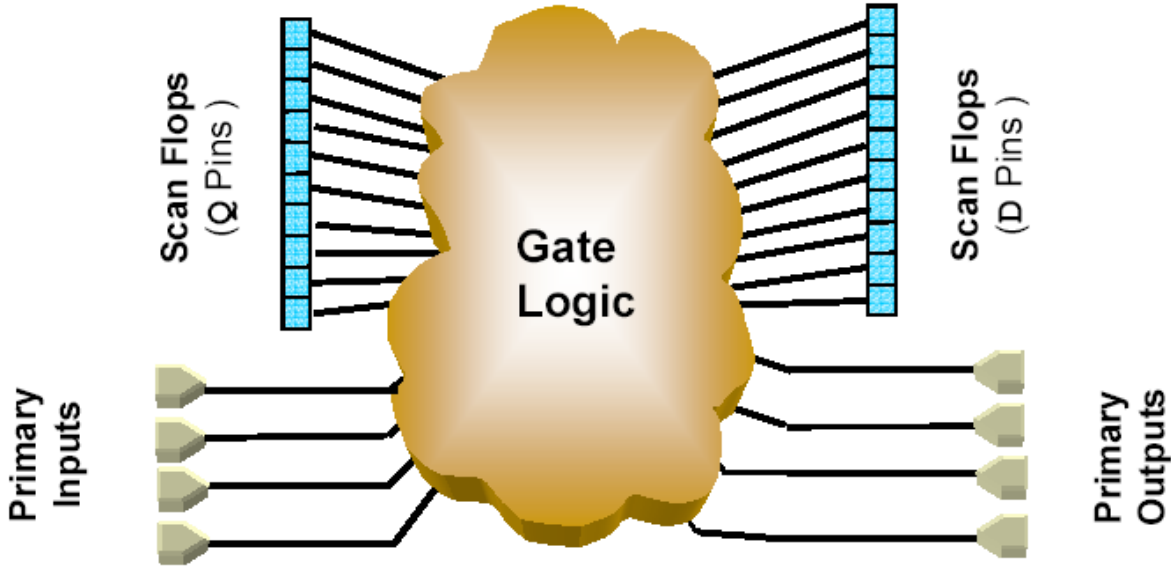
Scan Technique

- Controllability of sequential cells
  - Ability to assign the state vector from the primary inputs
- Observability of sequential cells
  - Ability to observe the next state from the primary outputs

Concept of Full Scan

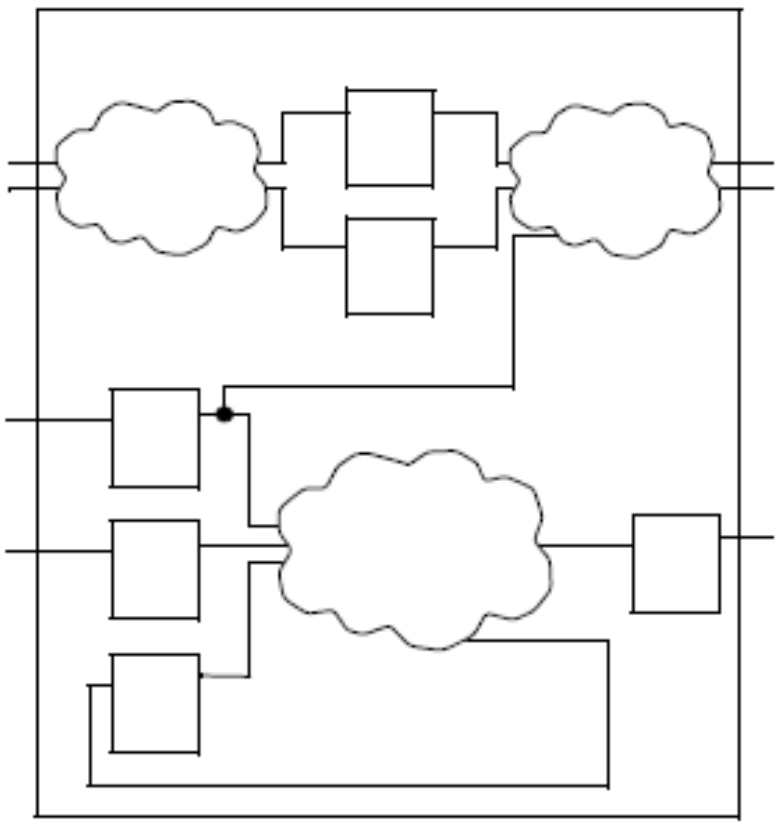
- All sequential cells are replaced by CAD tools with their scannable equivalents during scan insertion
- Providing virtual Inputs and Outputs



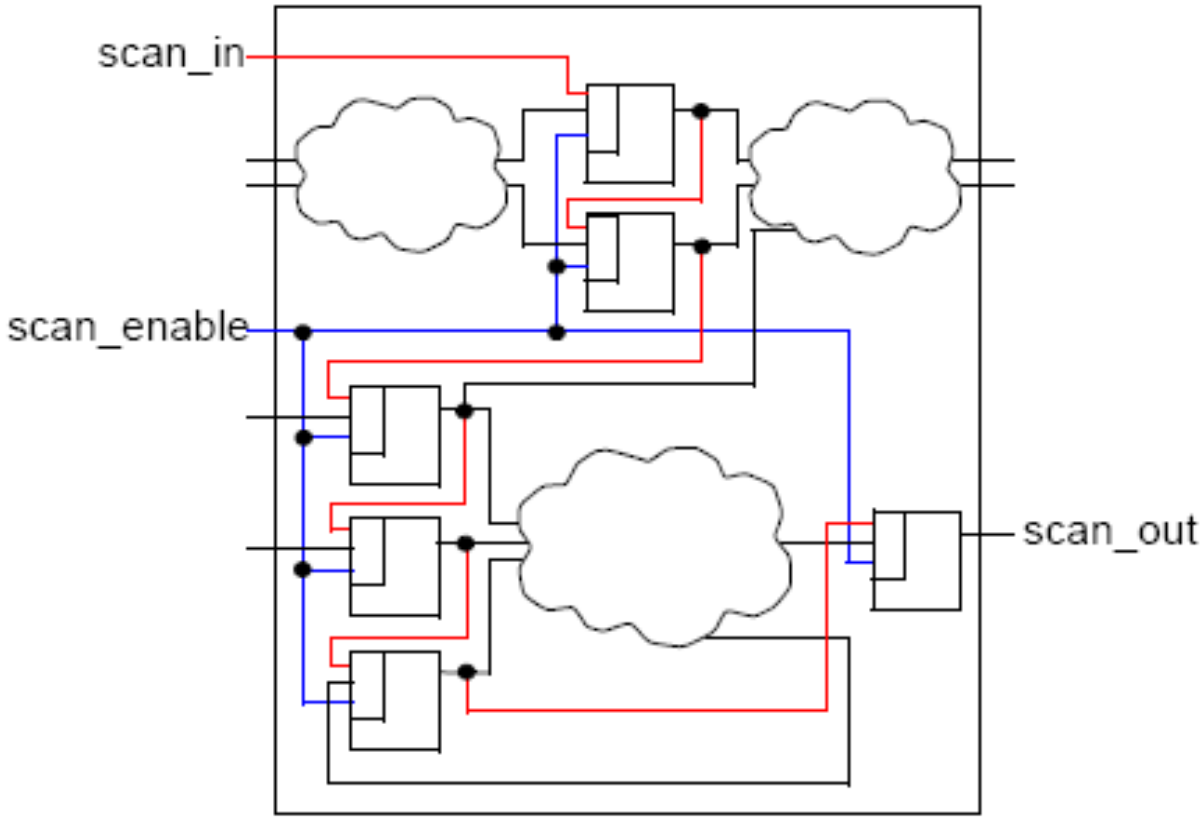


Flip-flops that can be **scanned**
→ **controllable** and **observable.**

Another Example of Full-Scan

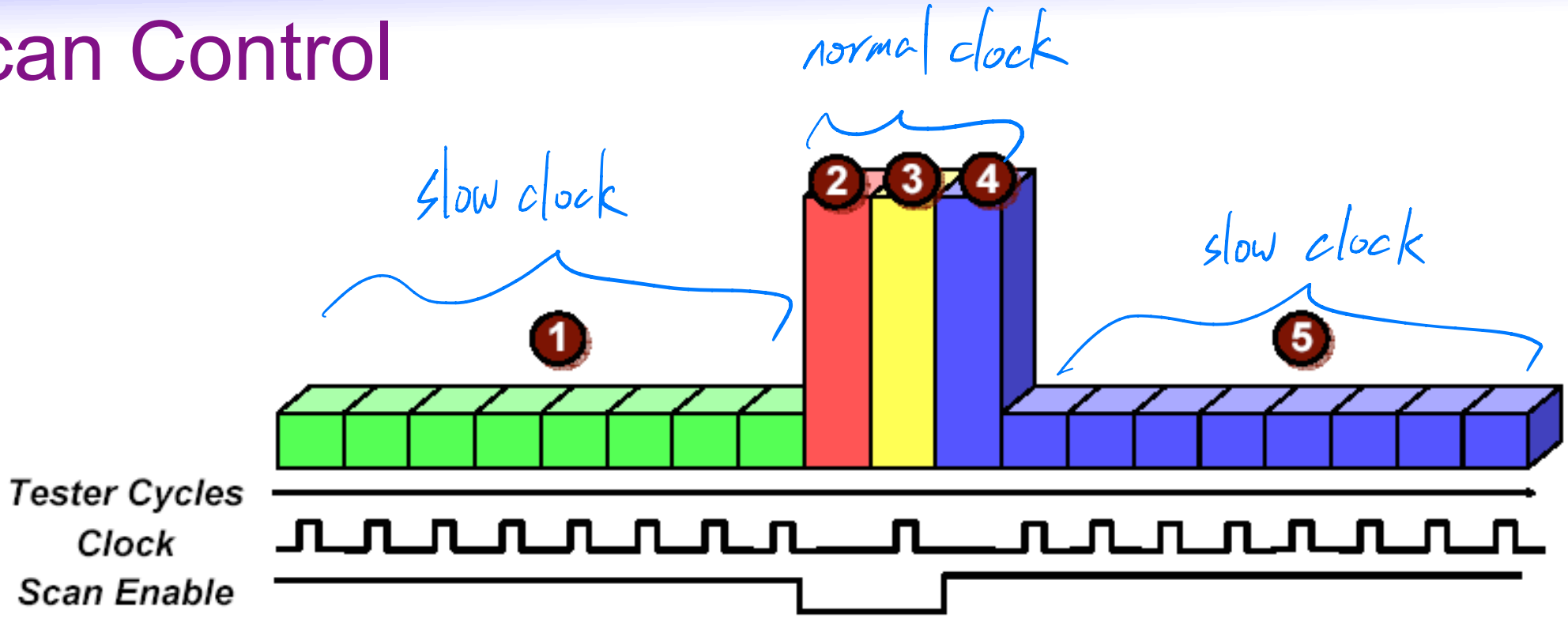


Without Scan



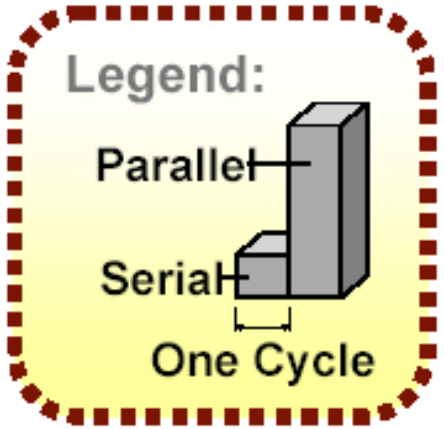
With Full Scan

Scan Control



Five Phases

① Scan-In
② Parallel Measure
③ Parallel Capture
④ First Scan-Out
⑤ Scan-Out



Scan Control (cont)

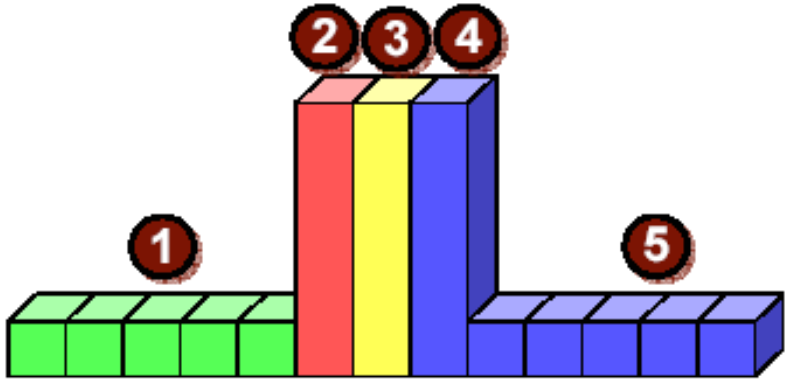
1. **Scan-In Phase:**
In each cycle, the next scan bit is applied serially to **SI**. On the clock edge, it is shifted in to the scan chain. Meanwhile, parallel outputs are masked.

2. **Parallel Measure:**
PIs are applied early in the cycle. The clock remains inactive. The CUT is now in a known state. POs are measured late in the cycle.

3. **Parallel Capture:**
The clock is pulsed once. This captures virtual PO data in the scan chain. The CUT is left in a don't-care state. Captured bits are ready for scan out.

4. **First Scan-Out:**
With no clock, the **SO** port is strobed, measuring the first scanned-out bit.

5. **Scan-Out Phase:**
In each cycle, the next captured bit is scanned out and measured at **SO**.



Full Scan

- All scan flops initialize nodes within the design (controllability)
  - Vs. partial scan technique
- Scan flops capture results from within the design (observability)
- Inserting a scan path involves replacing all flip-flops with their scannable equivalent flip-flops
  - Larger area than non-scan registers; larger setup time requirement
  - Area and performance overhead
  - Extra primary input/output pins
- The modified sequential cells are chained together to form one or more large shifting paths
  - Single scan chain
  - Multiple scan chains → 切成多個 scan chain，信有多個 scan in, scan out I/O

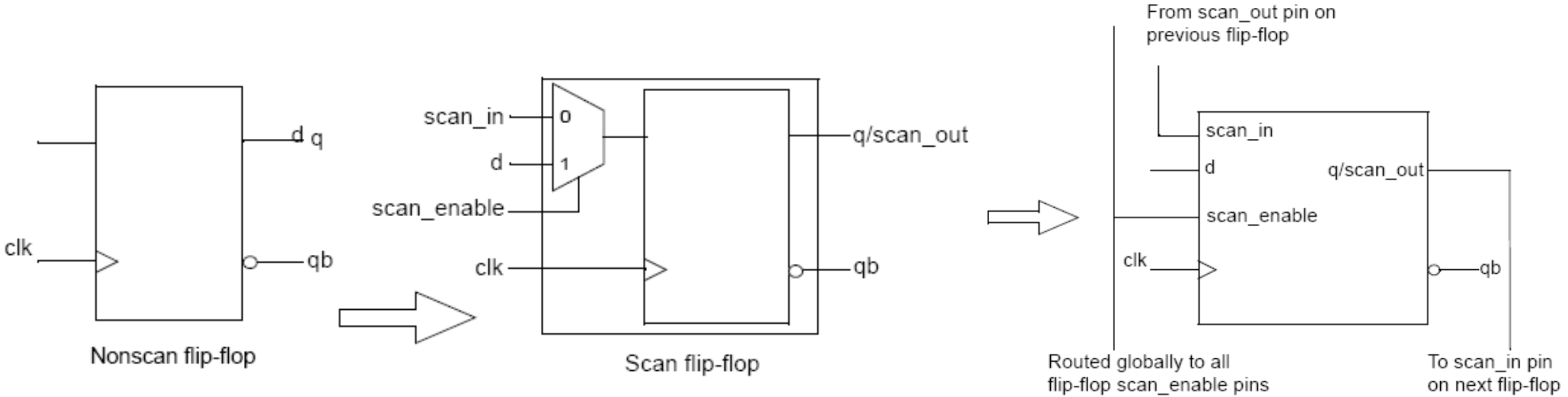
Full Scan (cont)

- An automatic methodology
  - Scan insertion + ATPG
- High fault coverage than partial scan
- Better diagnostic capability compared with partial scan
- Extended features
  - Debugging
  - Profiling
- Scannable equivalents
  - Multiplexed flip-flop (MUX scan)
  - Clocked scan
  - Level-sensitive scan design (LSSD)
  - Auxiliary-clock LSSD

Mux Scan Technique

- Flip-Flop with an additional MUX
- Test pins
  - Scan input
  - Scan enable
  - Scan output (can be shared with a functional output pin)
- Most commonly supported
- Mux scan cells
  - D, JK, master-slave flip-flops
  - D latches
    - Level sensitive in functional mode, edge triggered during scan shift

Mux Scan Cell



DFT Tools for Scan

- Insert scan
  - Synopsys DFT Compiler (integrated in Design Compiler)
- ATPG
  - Synopsys TetraMAX
  - User guide `/usr/cad/synopsys/doc/TetraMAX/TetraMAX_User_Guide.pdf`

Other DFT Techniques

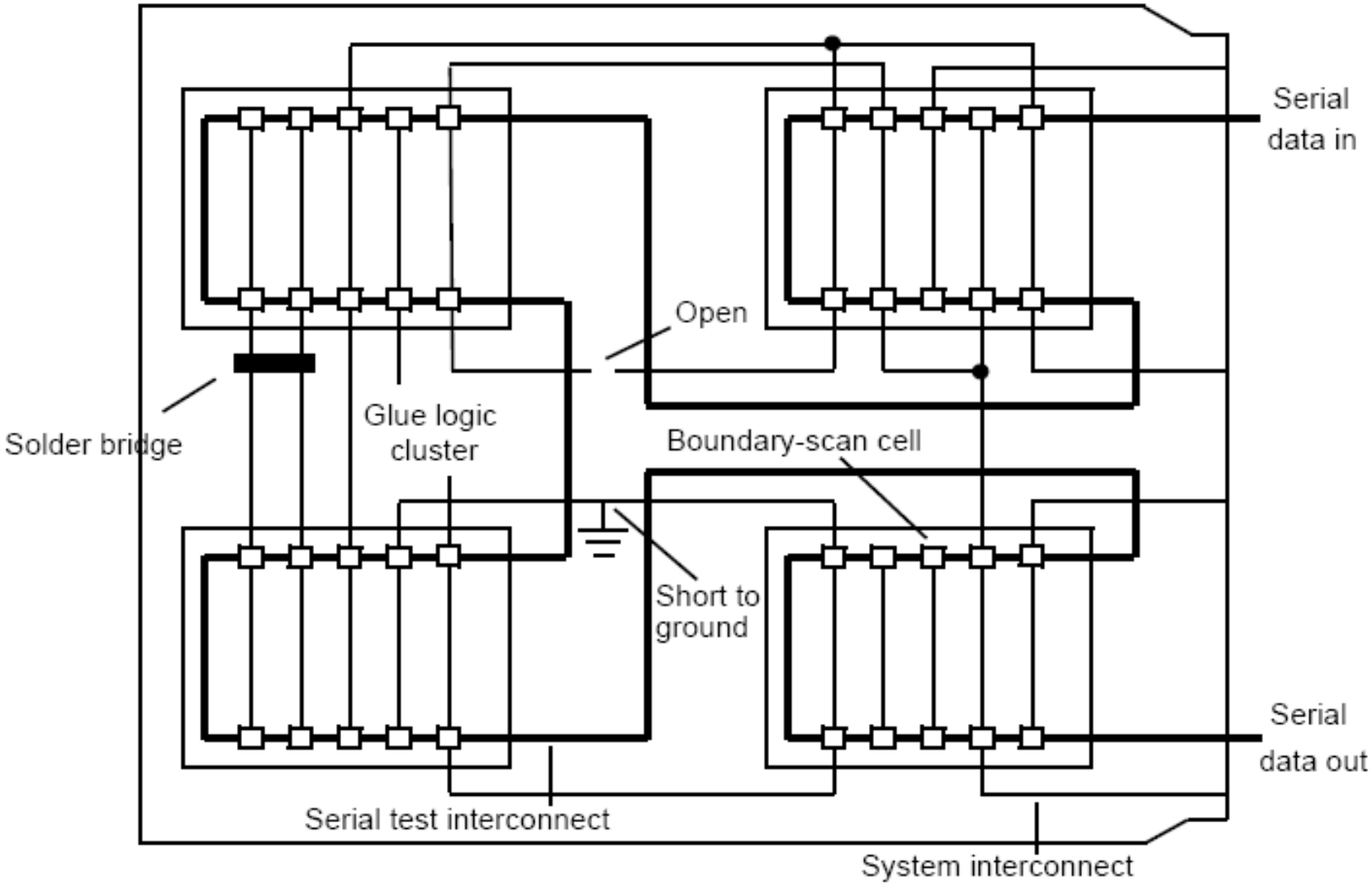
Other DFT Techniques

- Software-based test

structure test → fault coverage ↑

- Built-In Self Test (BIST)
  - Logic BIST
    - Pseudo random pattern generator
      - Utilizing LFSR (linear feedback shift register)
  - Memory BIST
    - March-based test algorithms
- Boundary scan design (for board/system level)
  - IEEE Std 1149.1
  - Board-level DFT
    - Primary for testing the interconnections between chips on the board

Board Testing with Boundary Scan

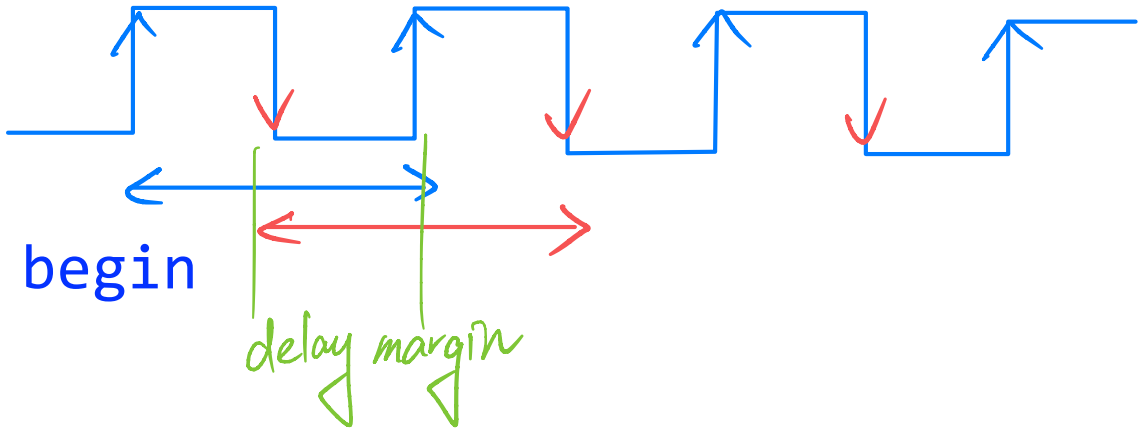


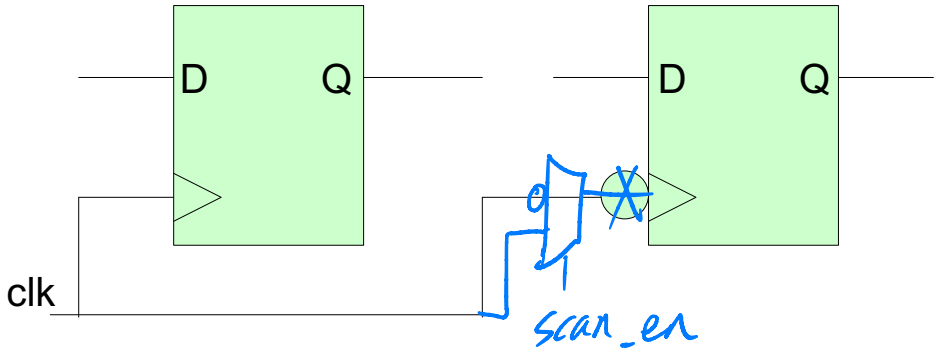
Verilog Coding Style vs. DFT

DFT Rule Violation: Mixed-Edge Clock Control

- Mixed positive and negative edge triggered clocks in one design module
  - Reduce effective clock period
  - Complicated scan testing

```
module …
   always @(posedge clock) begin
   …
   end
   always @(negedge clock) begin
   …
   end
endmodule
```

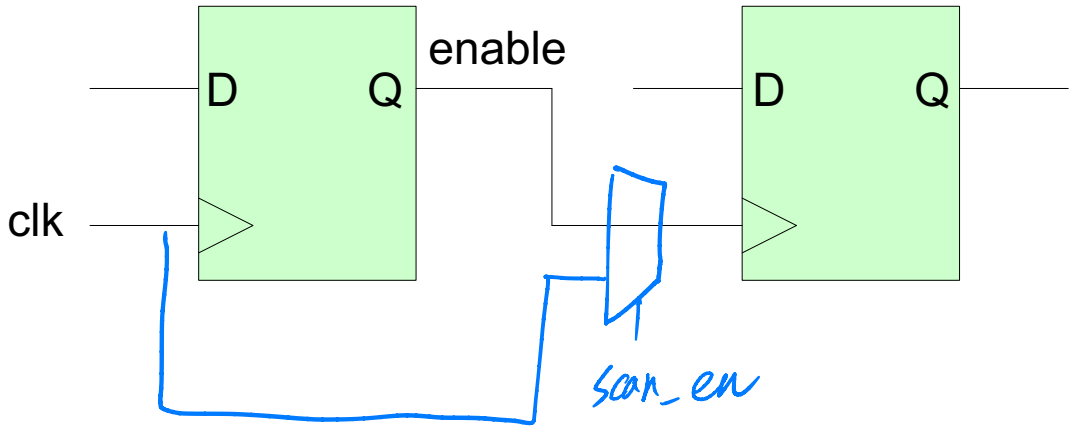




DFT Rule Violation: Asynchronous Clocking

- Asynchronous logic
  - Non-clock signal appears in the sensitivity list
  - Complicated scan testing

```
always @(posedge clk) begin
  …
end
always @(posedge enable) begin
  …
end
```



Summary

- Definition
  - Yield
  - Defect level
  - Fault model
- DFT techniques are mandatory to ensure the quality, reliability, and performance of IC product
  - Controllability
  - Observability
  - Yield vs. cost
  - Structure test vs. functional test