CS5120 VLSI System Design, Spring 2024

Design for Manufacturability (DFM)

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Lecture 19

聲明

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Design for Manufacturability (DFM)

- Consider the following issues to increase manufacturing yield
  - Crosstalk/Signal Integrity (SI)
  - Gate oxide integrity
    - Antenna fixing
  - Via resistance and reliability
    - Extra contacts
  - Metal erosion
    - Metal slotting
  - Metal liftoff
    - Metal slotting
  - Metal over-etching
    - Metal fill

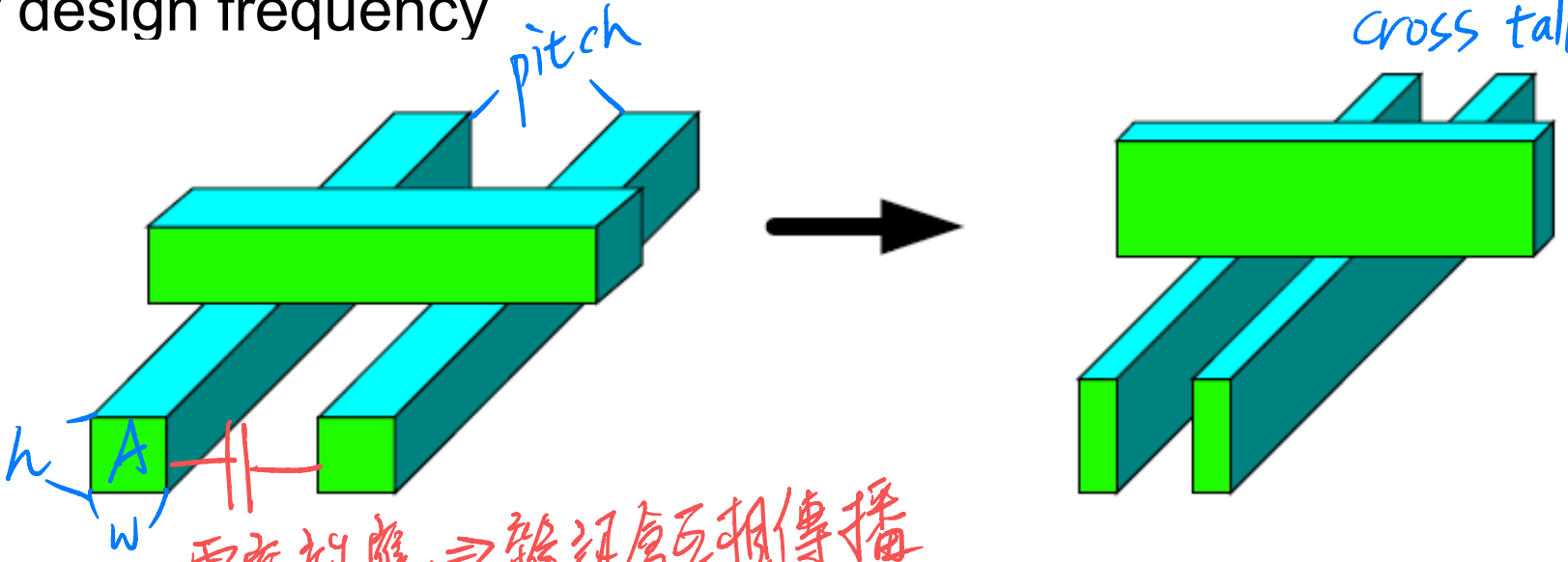
SI/Crosstalk Problem

- SI: signal integrity
- Crosstalk problem are getting more serious in 0.25um and below for:
  - Smaller pitches
  - Greater height/width ratio
  - Higher design frequency

$R \propto \frac{\rho L}{A} \Rightarrow \frac{\rho \times 0.7L}{0.7h \times 0.7W} = 1.4R$

製程微縮後

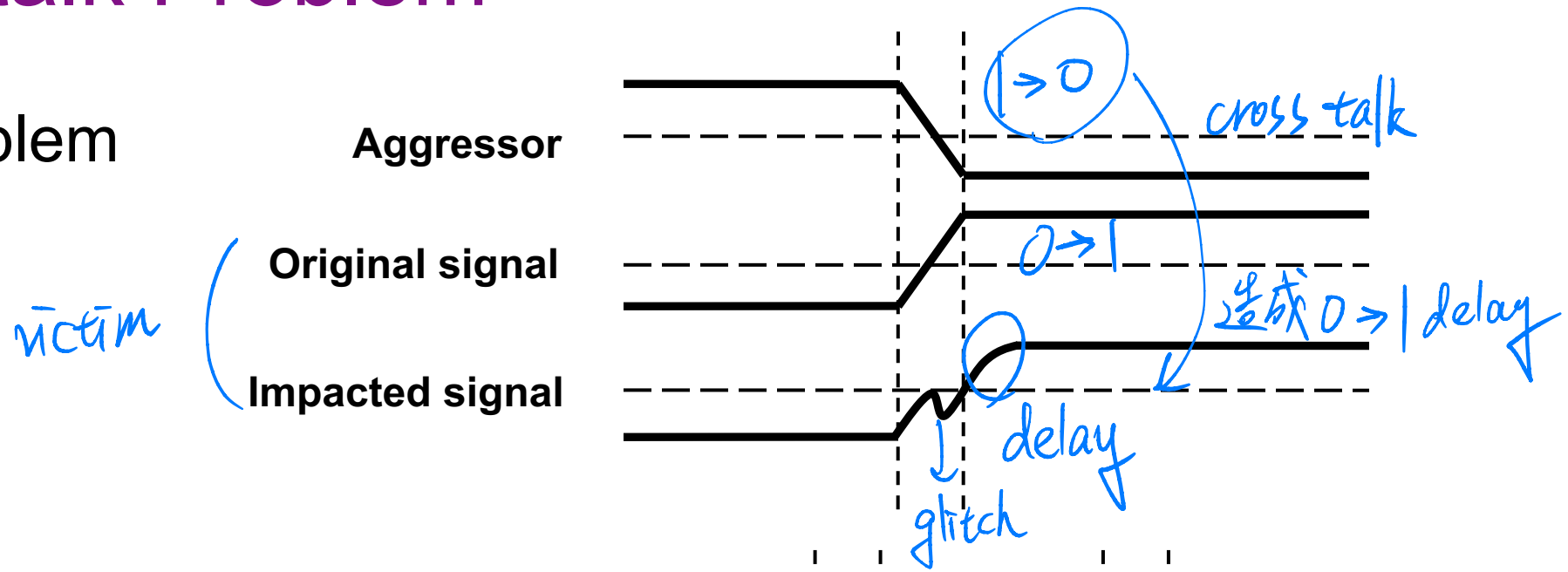
cross talk ↑



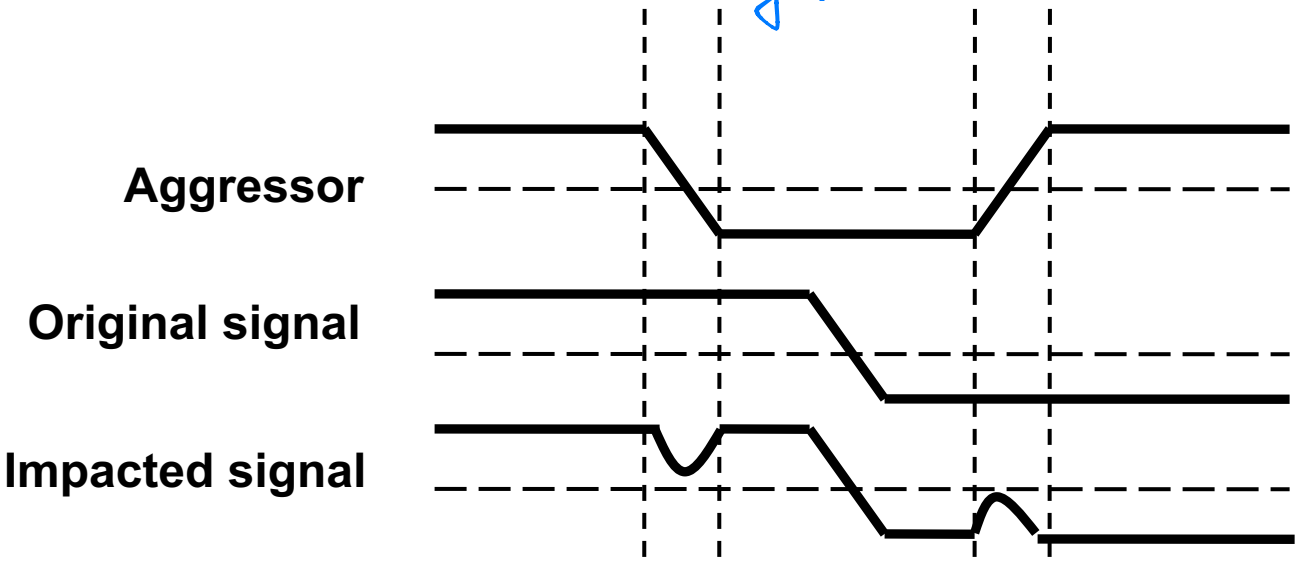
電容效應 ⇒ 雜訊會互相傳播

SI/Crosstalk Problem

- Delay problem

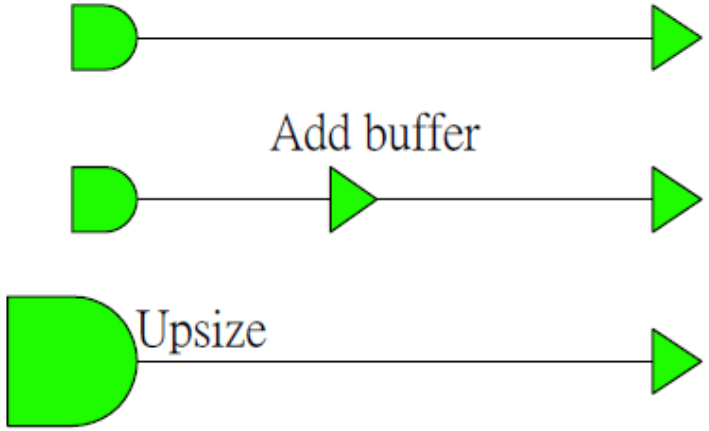


- Noise problem

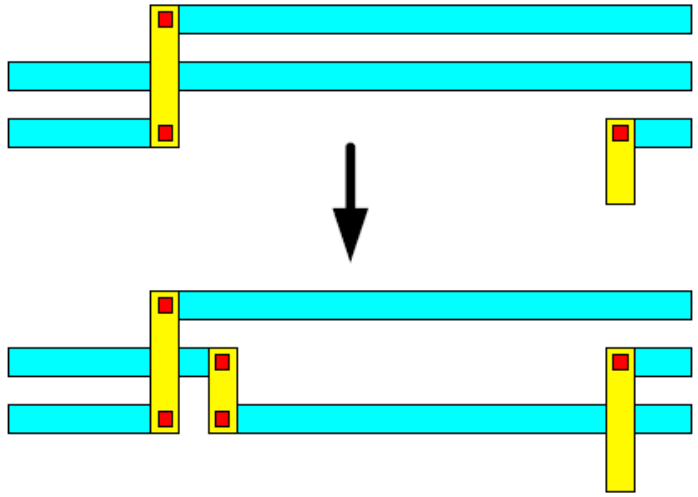


SI/Crosstalk Prevention

- Placement solution
  - Insert buffer in lines
  - Upsize driver
  - Congestion optimization



- Routing solution
  - Limit length of parallel nets
  - Wider routing grid
  - Shield special nets

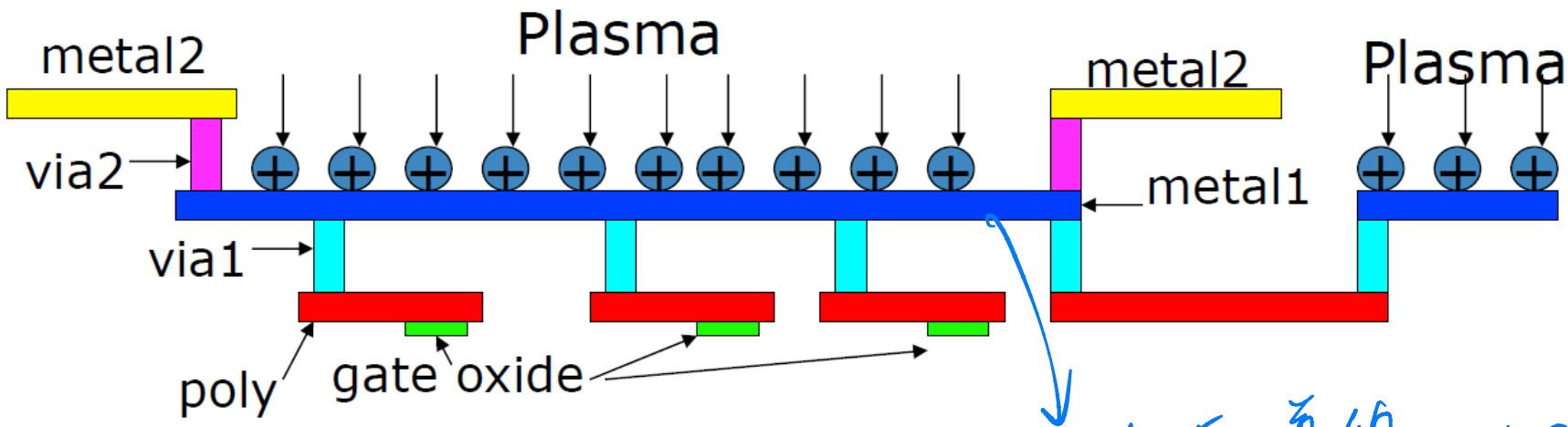


Antenna Effect

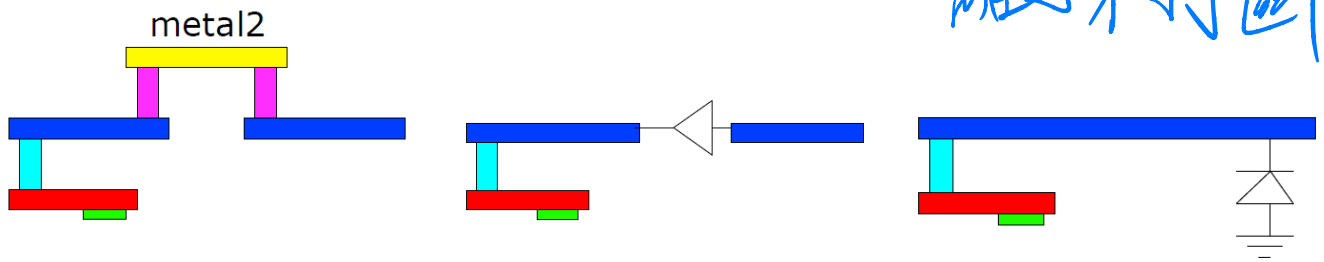
- In a chip manufacturing process, metal is initially deposited so it covers the entire chip.
- Then, the unneeded portions of the metal are removed by etching, typically in plasma (charged particles).
- The exposed metal collect charge from plasma and form voltage potential.
- If the voltage potential across the gate oxide becomes large enough, the current can damage the gate oxide.

Process Antenna Problem

- Process antenna problem may destroy the circuit after a period of time

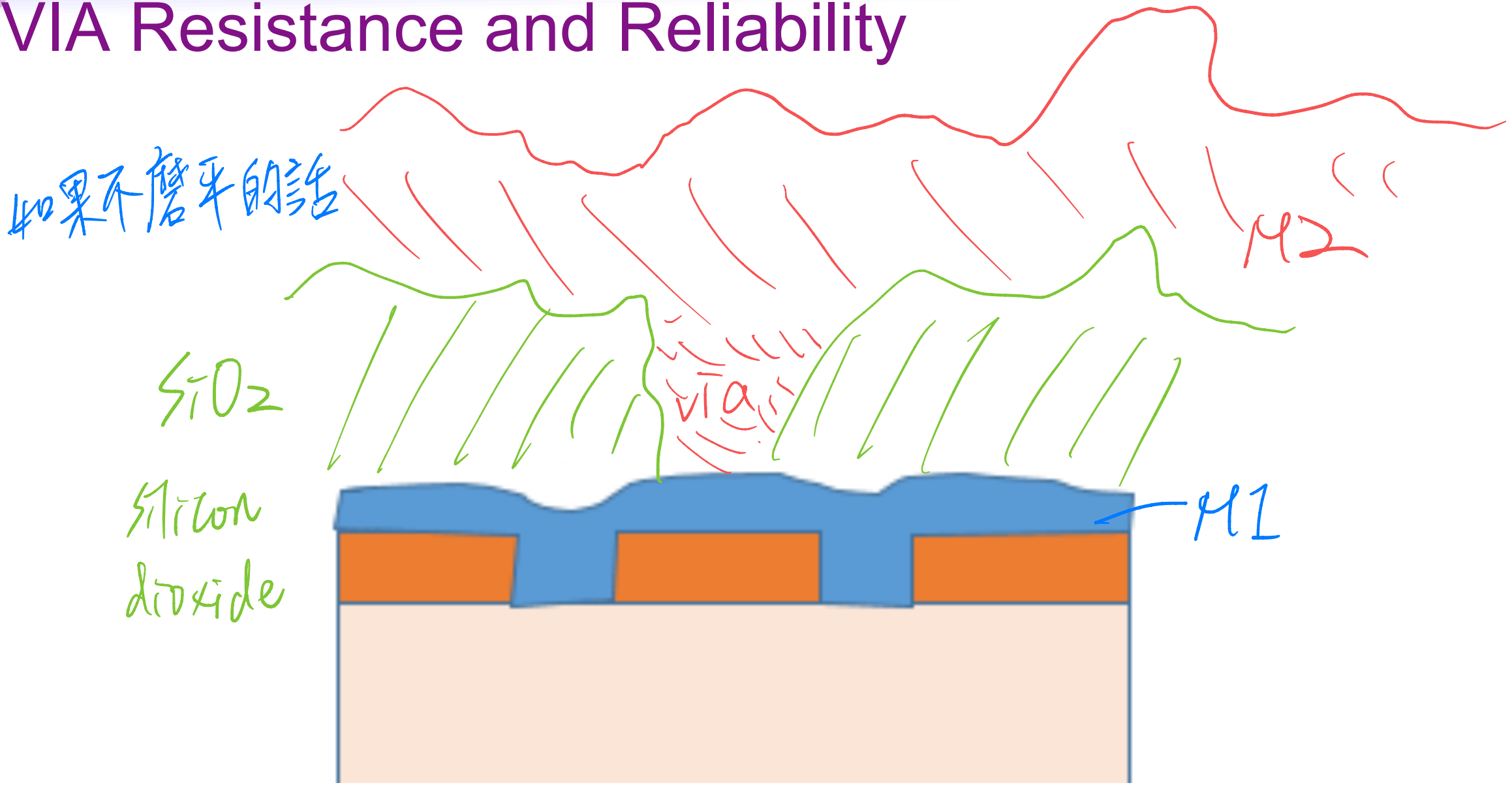


- Solution
  - Add jumper, antenna cell (diode), buffer



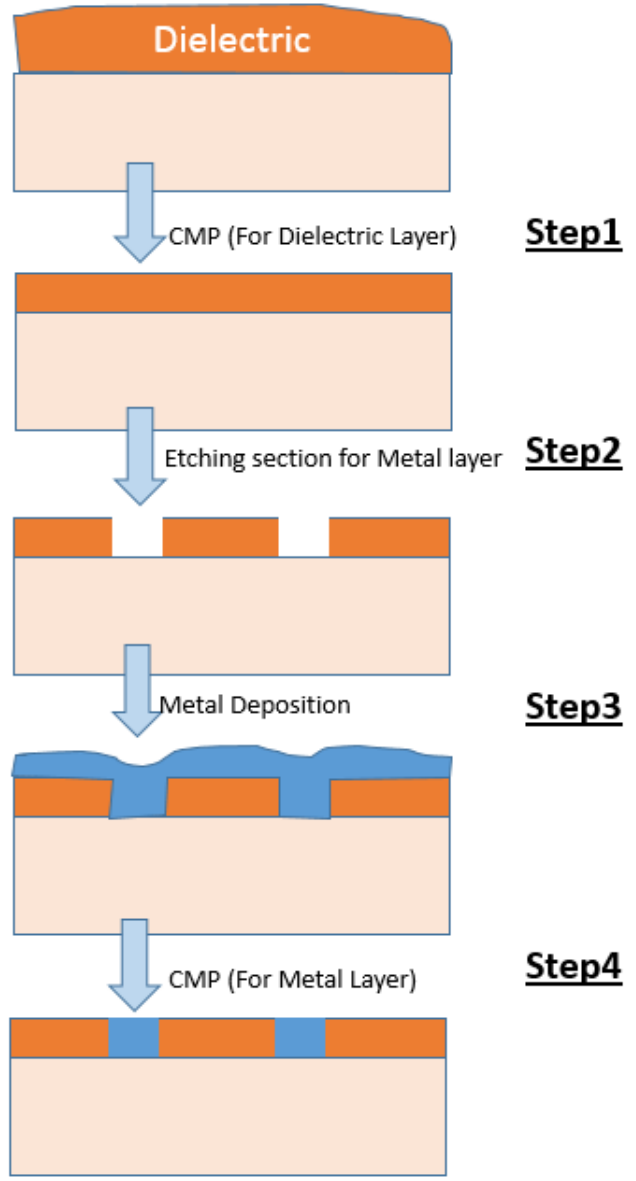
避免長導線，有可能被離子束打斷

VIA Resistance and Reliability



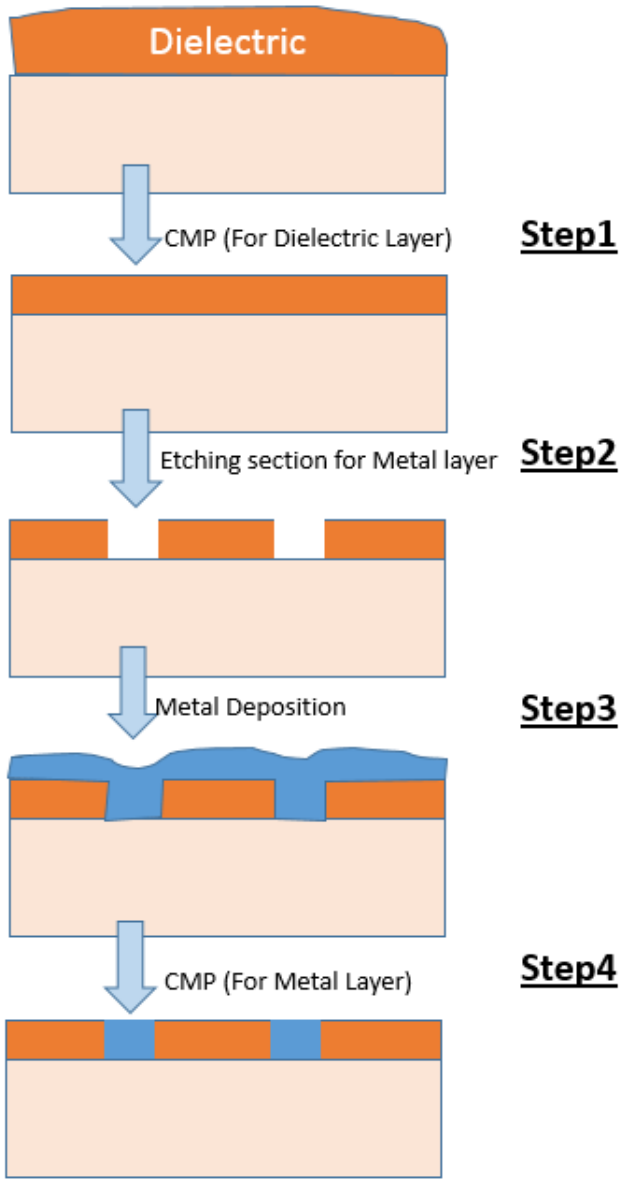
CMP Process

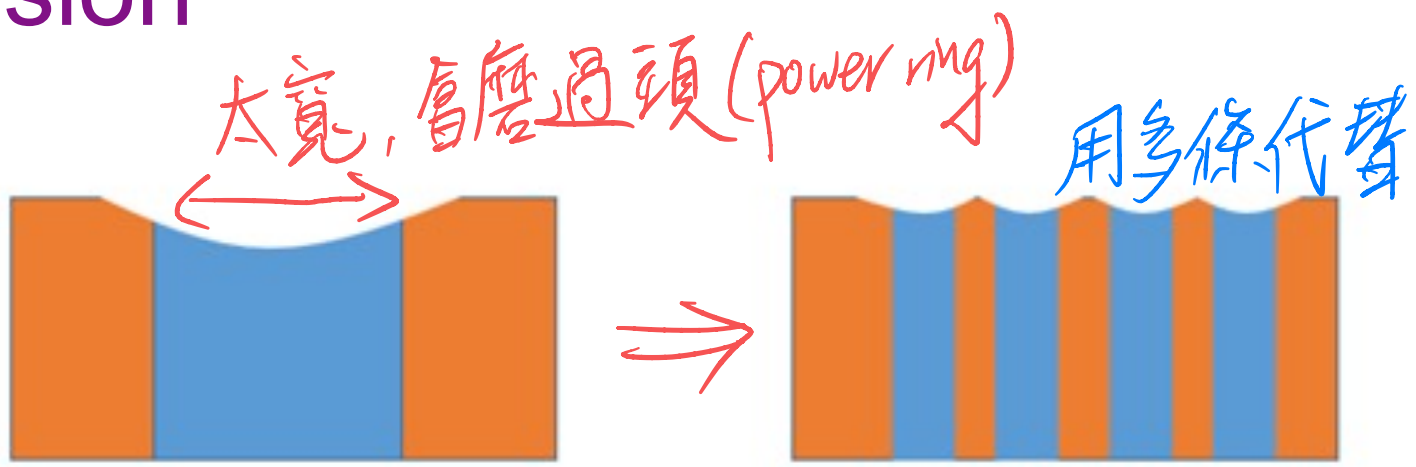
- Chemical Mechanical Polishing (CMP) process
- Metal erosion
  - Metal is mechanically softer than dielectric
    - Dishing
    - Erosion
  - Maximum metal density per layer
    - Rule to minimize erosion

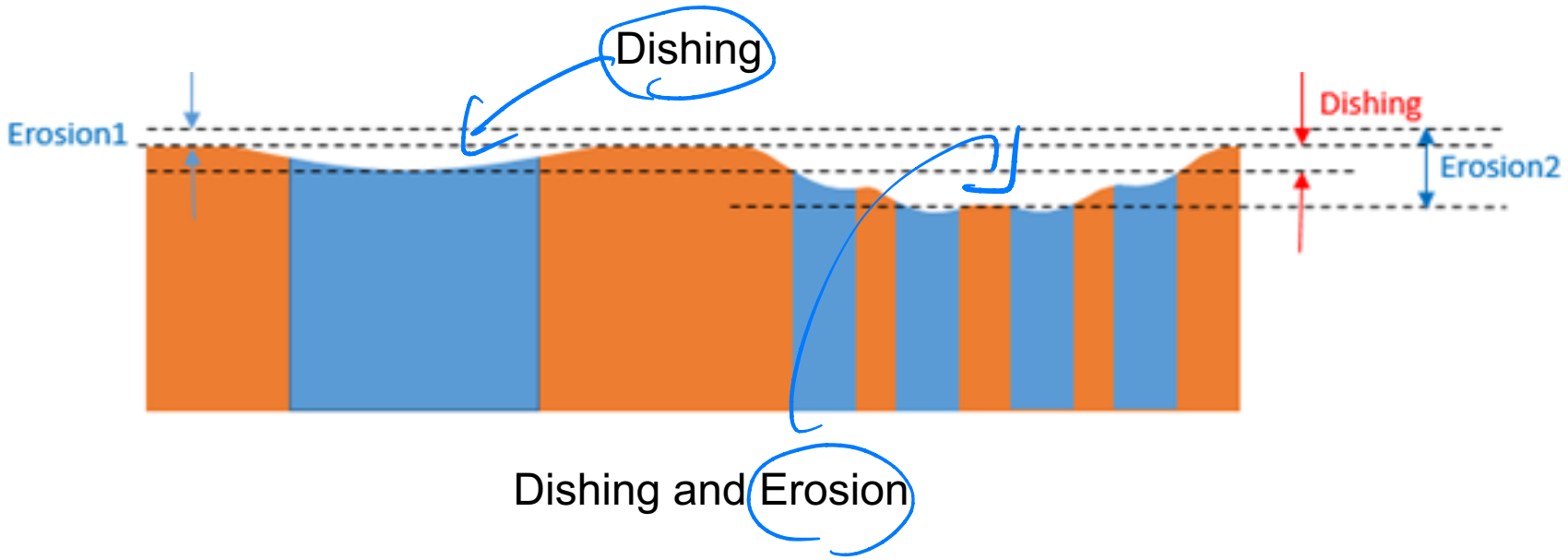


http://www.vlsi-expert.com/2015/08/dishing-and-erosion-cmp.html

Dishing and Erosion





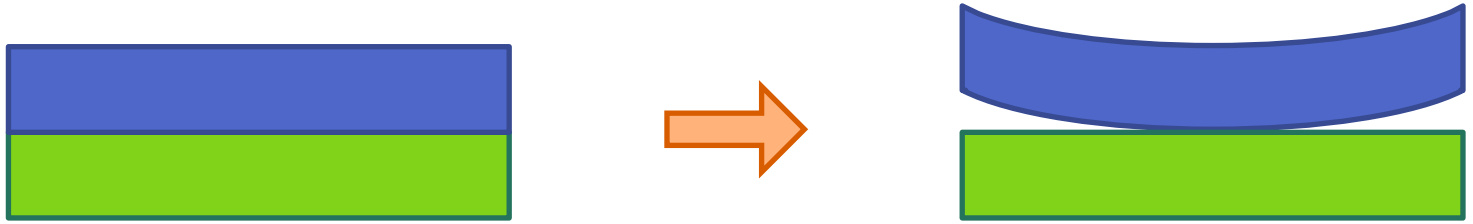


Dishing and Erosion

http://www.vlsi-expert.com/2015/08/dishing-and-erosion-cmp.html

Metal Liftoff

- Conductor and dielectric with different coefficients of thermal expansion
  - Metal can lift off with time
  - Wider metal are more vulnerable

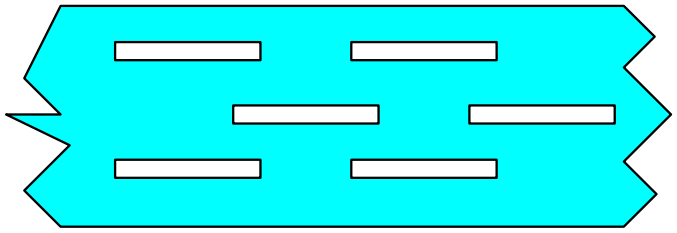


降低單層 metal 的使用

- Maximum metal density per layer
  - Rule to minimize metal liftoff

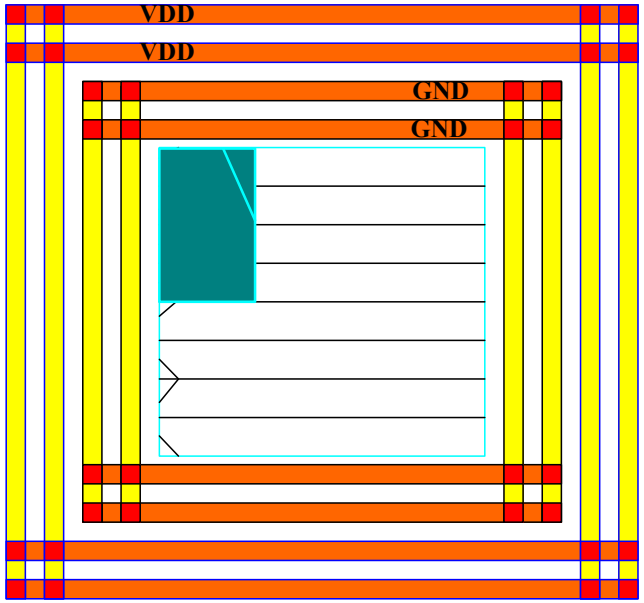
Metal Slotting or Wire Grouping for Wide Metal Wires

- Reduce the metal density
- Primarily used for power and ground traces
  - Any others if wide enough
- Different slotting parameters layer by layer

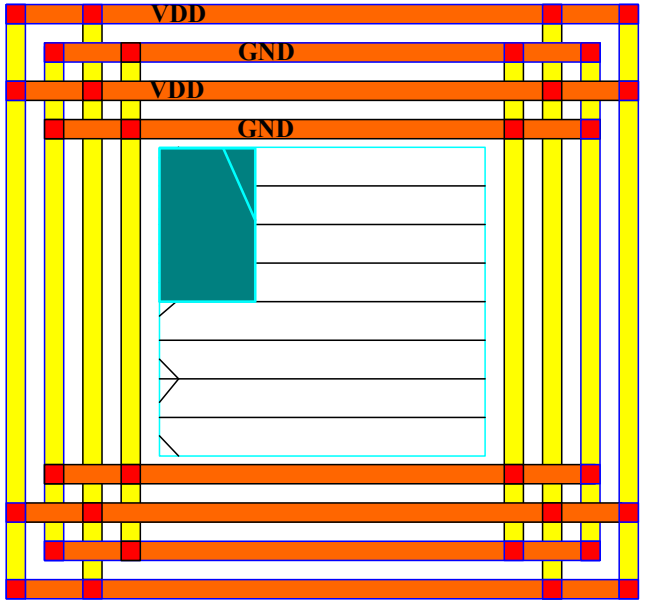


Metal Slot

Wire Groups (No Interleaving)

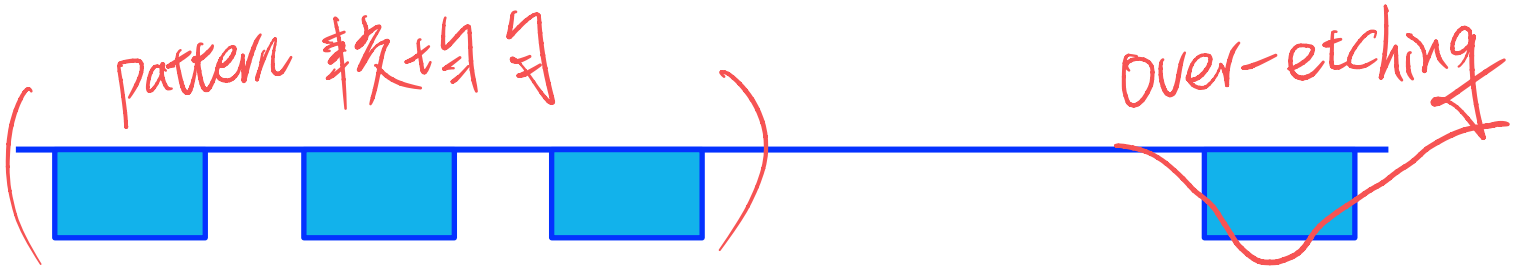


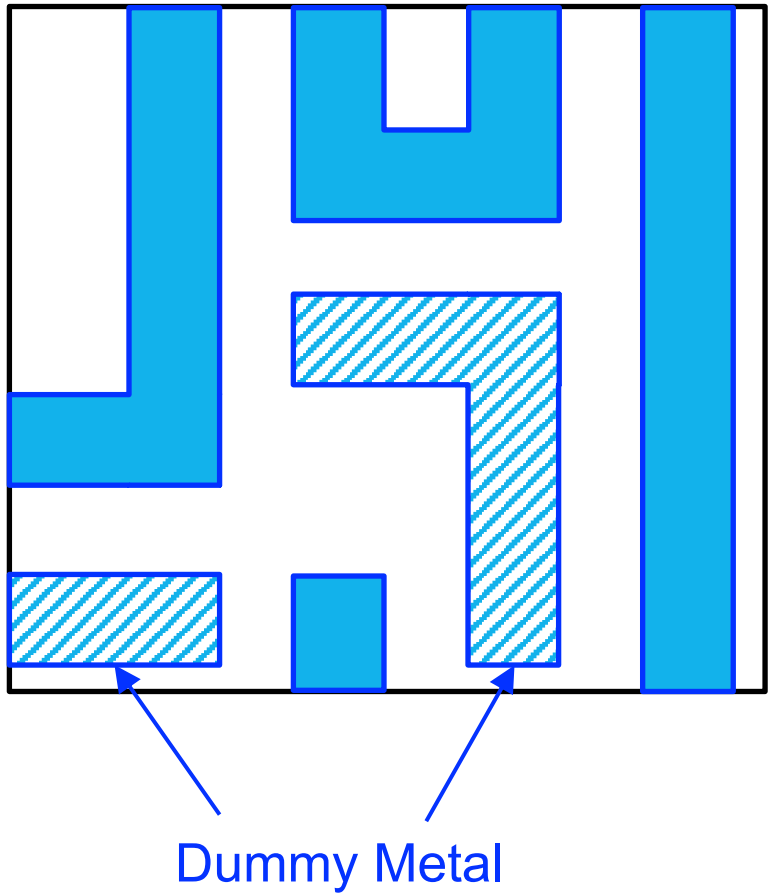
(Interleaving)



Metal Over-Etching

- A narrow metal wire separated from other metal
  - More vulnerable for over-etching



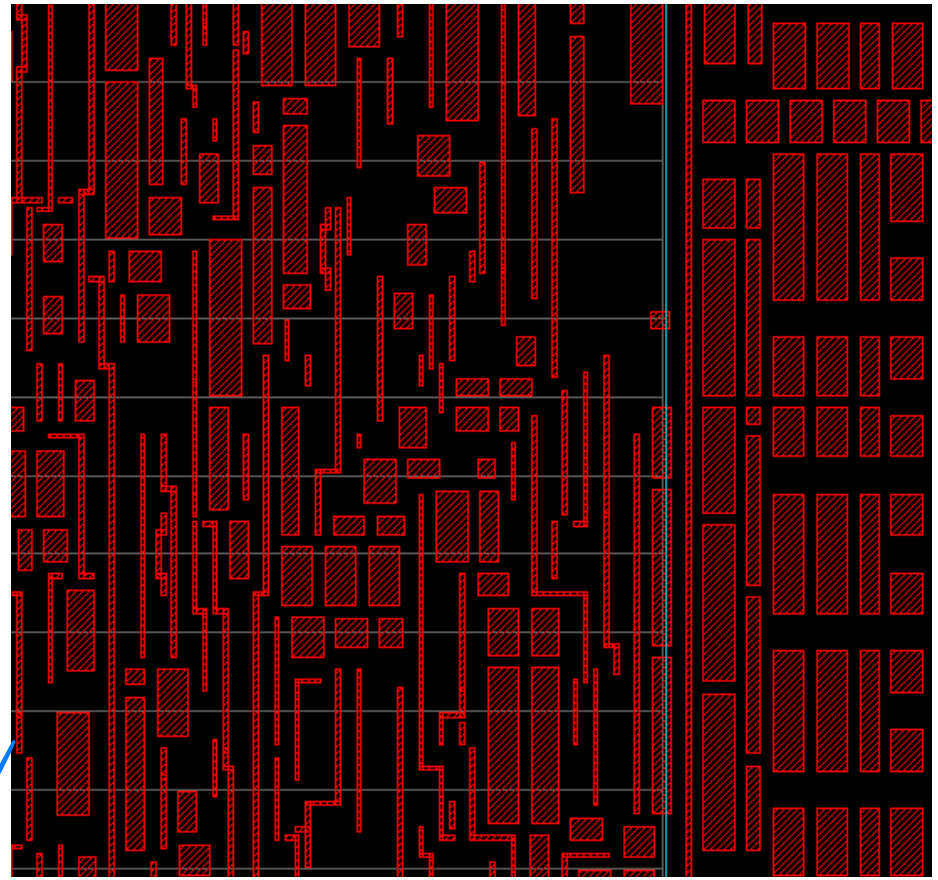


- Minimum metal density rule to prevent this
- Solution: metal fill
  - Limit the antenna fixing

Dummy Metal

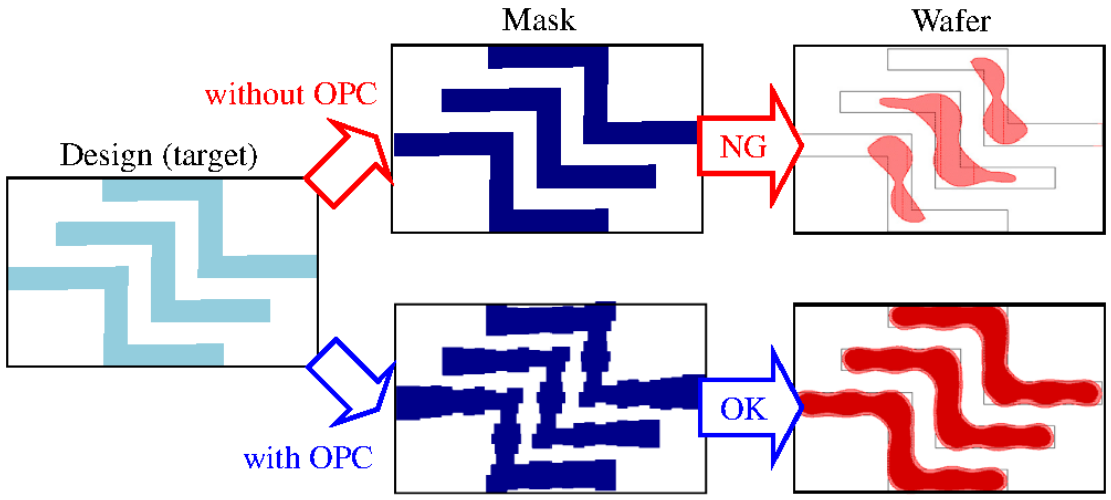
metal fill

- Why add dummy
  - Meet minimize metal density rule
  - Prevent over etching
  - Prevent sagging in local area
  - Improve yield
  - Reduce on chip variation
- Better connect dummy metal to VSS
- Side effect 可能增加 antenna effect
  - Introduce parasitic to signal line

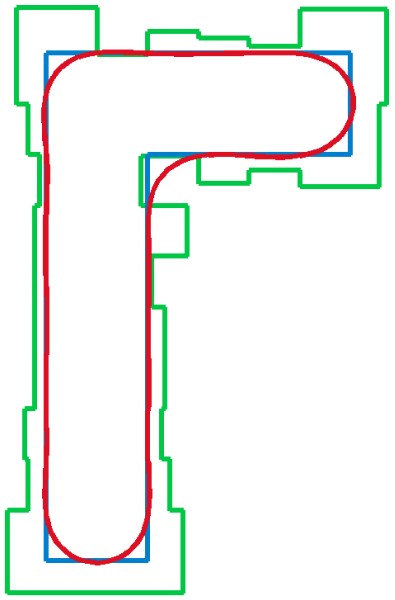


DFM – Post-Layout Correction

- Optical-proximity-correction (OPC)
- Reticle-enhancement technology (RET)



https://www.spiedigitallibrary.org/journals/journal-of-micro-nanopatterning-materials-and-metrology/volume-15/issue-02/021009/Optical-proximity-correction-with-hierarchical-Bayes-model/10.1117/1.JMM.15.2.021009.full?SSO=1



https://en.wikipedia.org/wiki/Optical_proximity_correction

Summary

- Design is not only for its functionality
- Design for test
- Design for manufacturability
- Design for reliability
- Design for quality
- …