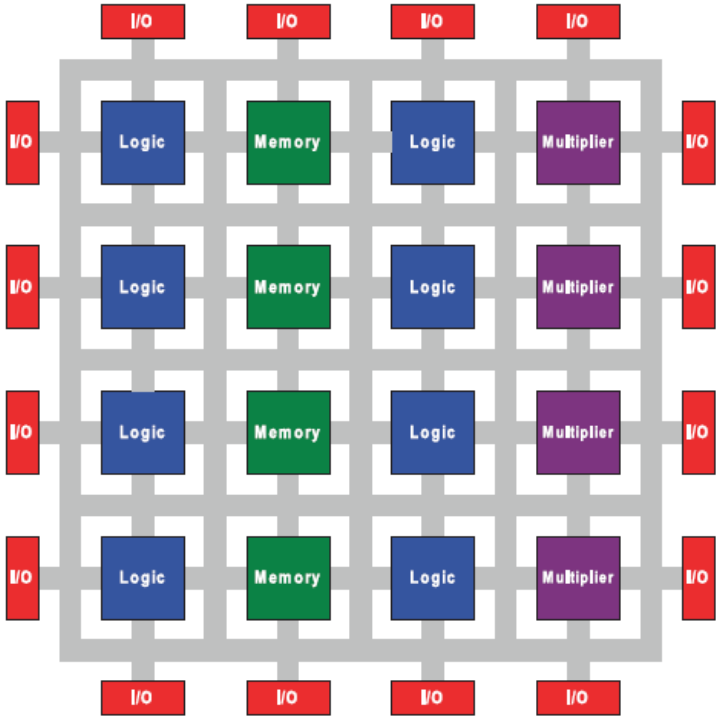
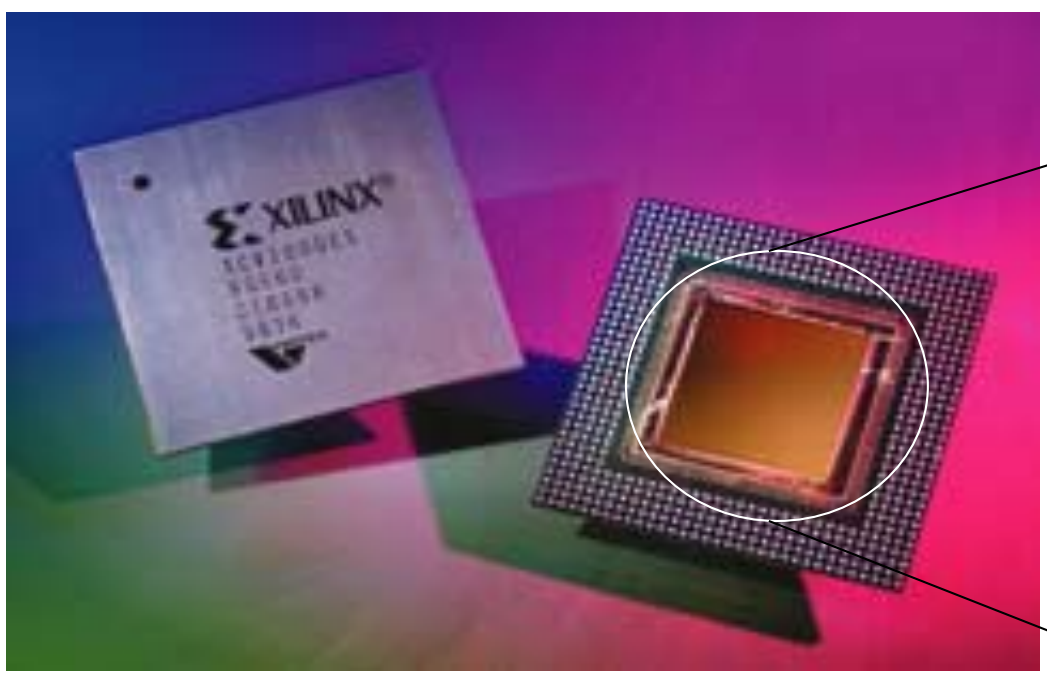
Classification and Evolution of Field Programmable Logic Devices

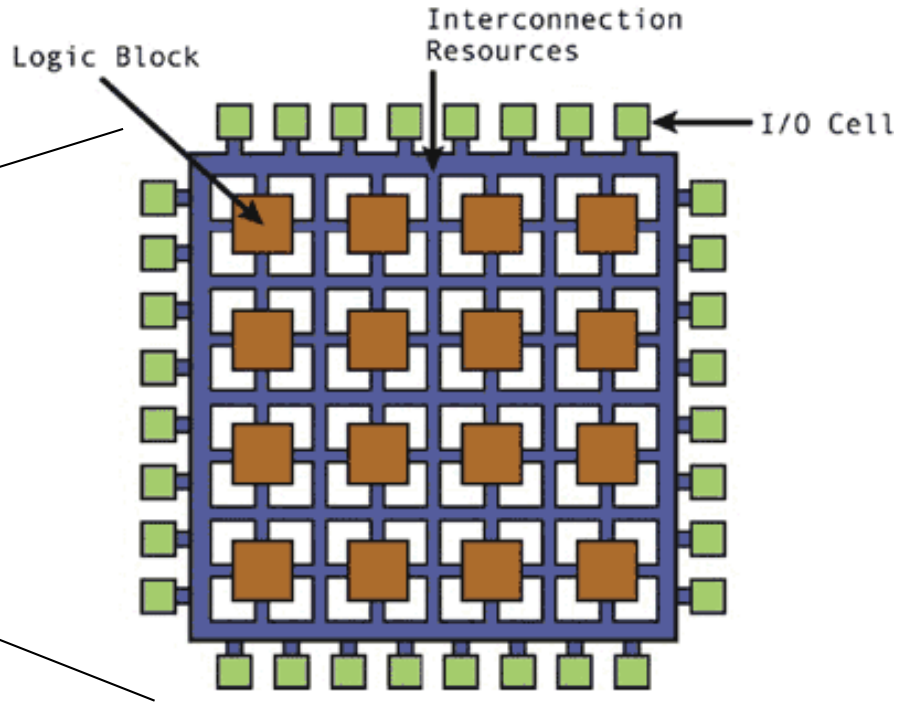
Topics

- Distinction from ASIC
- Classification & evolution of FPLDs
- FPLD markets



Field-Programmable Gate Array (FPGA)





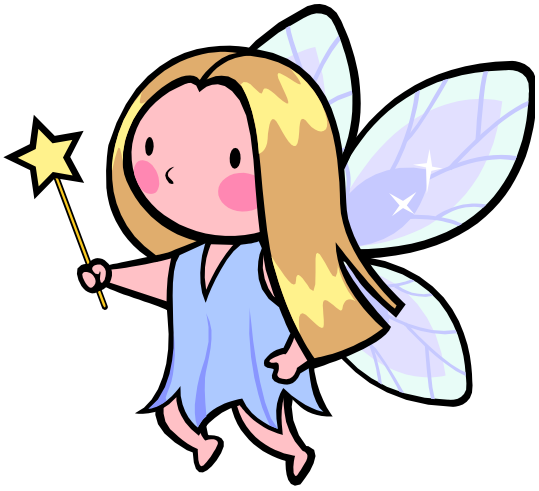
Field-Programmable Devices

- *User-configurable* ICs.
- They are standard parts, not designed for any particular application.
- Unlike traditional ASIC, logic function is specified by the user *after* the device is manufactured.

- They are programmed/configured by the users to implement their designs *at their own sites*.
- *Instant configuration* (in minutes) at users' site.

Advantages of Field-Programmable Logic Devices

- Short turnaround time for new designs
- Low startup cost
- Low inventory cost
- Low risk
- Allow easy design changes



How to make a chip that can realize different circuits and configurable?

What are the essential elements that make up any circuit?

What do you expect within a FPLD?

1. Substantial amounts of uncommitted combinational logic.
2. Contain flip-flops/latches.
3. Programmable interconnections between the combinational logic, flip-flops, and chip input/outputs.

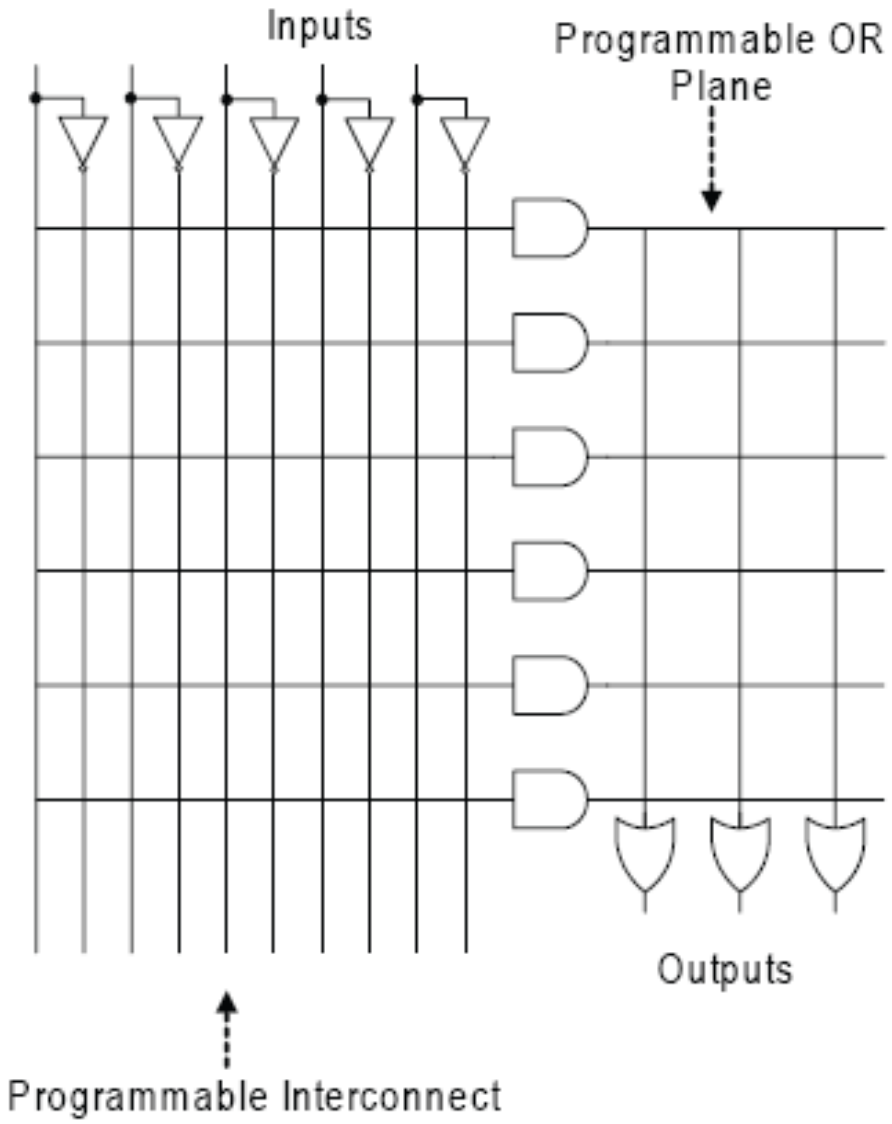
Types of Field-Programmable Devices

- *Simple Programmable Logic Devices* (SPLDs)
- *Complex Programmable Logic Devices* (CPLDs)
- *Field-Programmable Gate Arrays* (FPGAs)

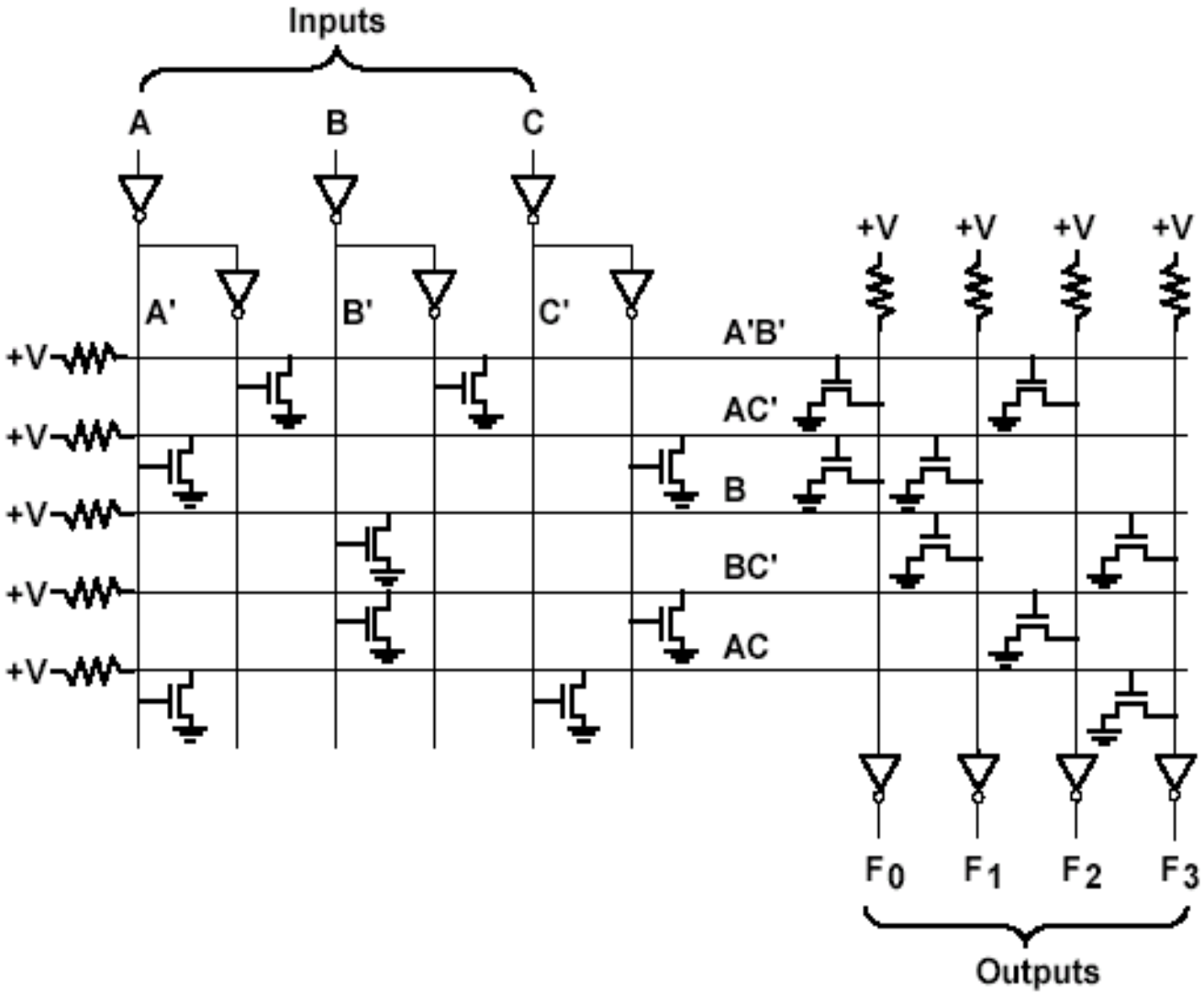
Programmable Logic Array (PLA)

- A simple programmable logic device (SPLD).
- The first programmable logic device introduced in the early 1970s by Philips.
- Use a *2-level logic* structure to implement programmed logic.
- Based on idea that logic functions can be realized in *sum-of-products* form.
- A programmable array of AND gates feeding a programmable array of OR gates.

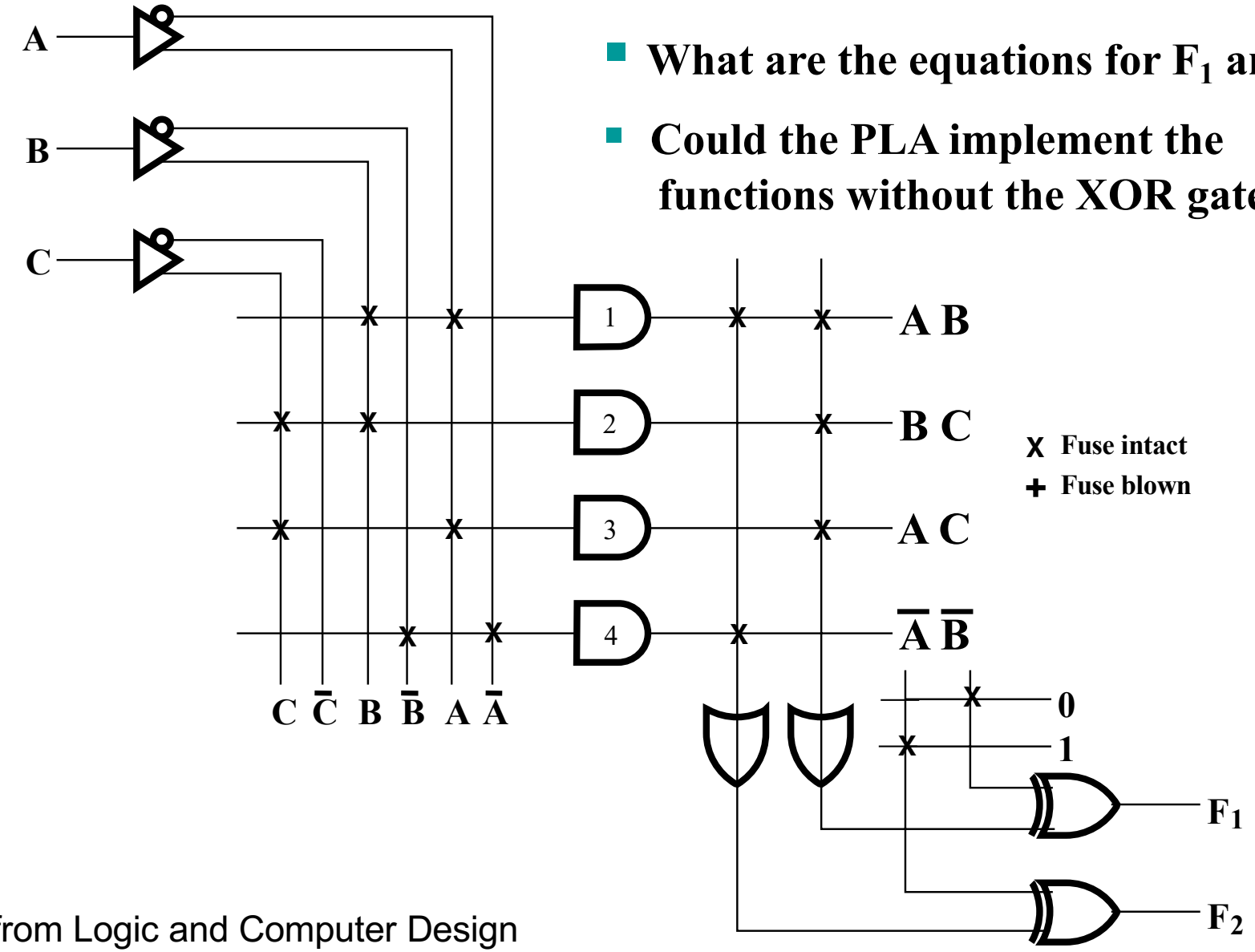
PLA Structure (Conceptual)



PLA Realization



Function Implementation by PLA

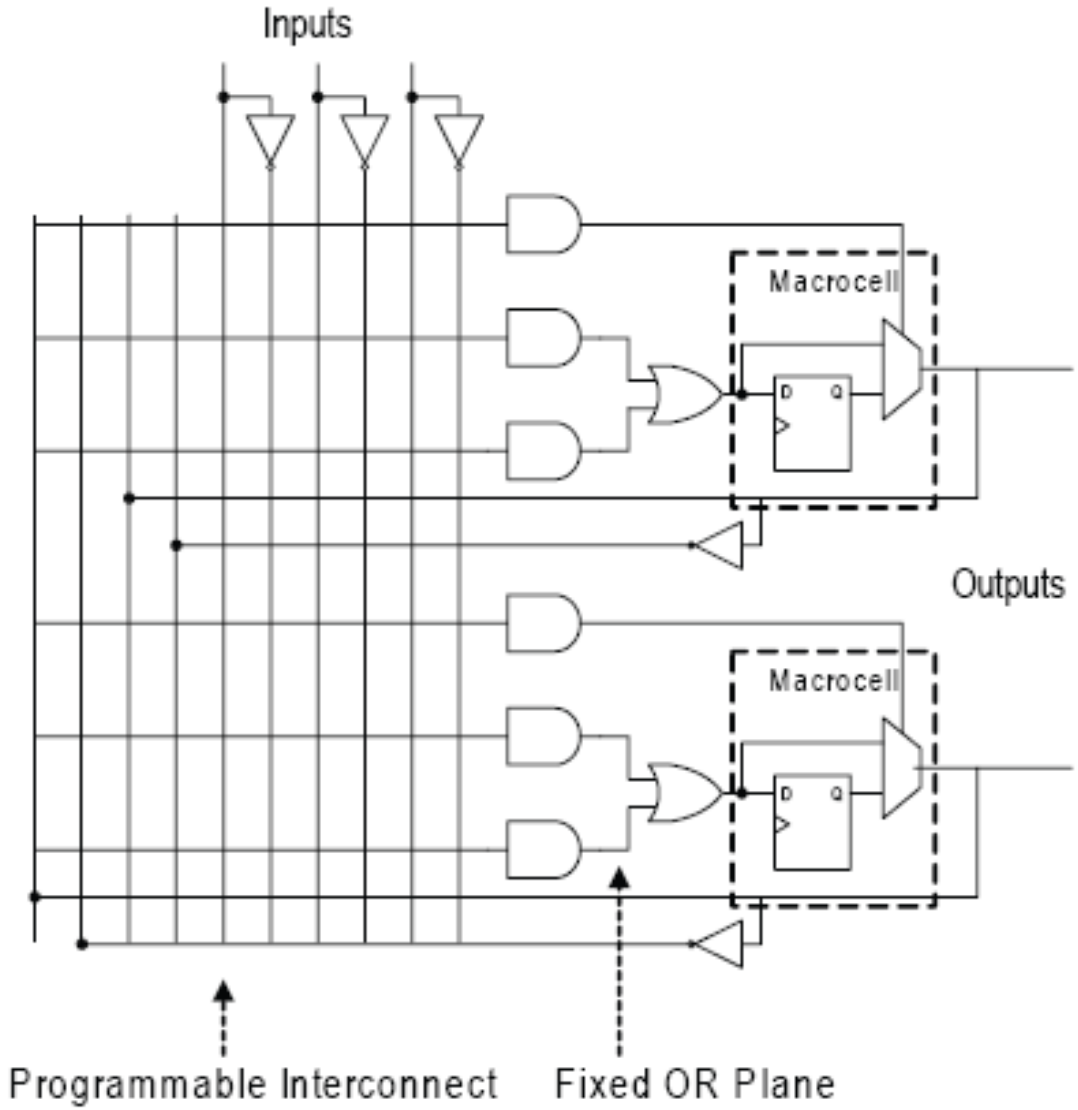


- What are the equations for F_1 and F_2?
- Could the PLA implement the functions without the XOR gates?

Programmable Array Logic (PAL)

- Introduced to overcome the weaknesses of PLAs (programmable switches were hard to fabricate correctly and introduced significant propagation delays).
- A programmable array of AND gates feeding a fixed array of OR gates.
- PAL usually contains flip-flops connected to the OR gate outputs to implement sequential circuits. (*Macrocell:* an OR gate combined with a flip-flop and extra circuitry in a PAL.)
- PLAs and PALs are useful for implementing small digital circuits, typically ≤ 32 combined inputs and

PAL Structure



Function Implementation by PAL

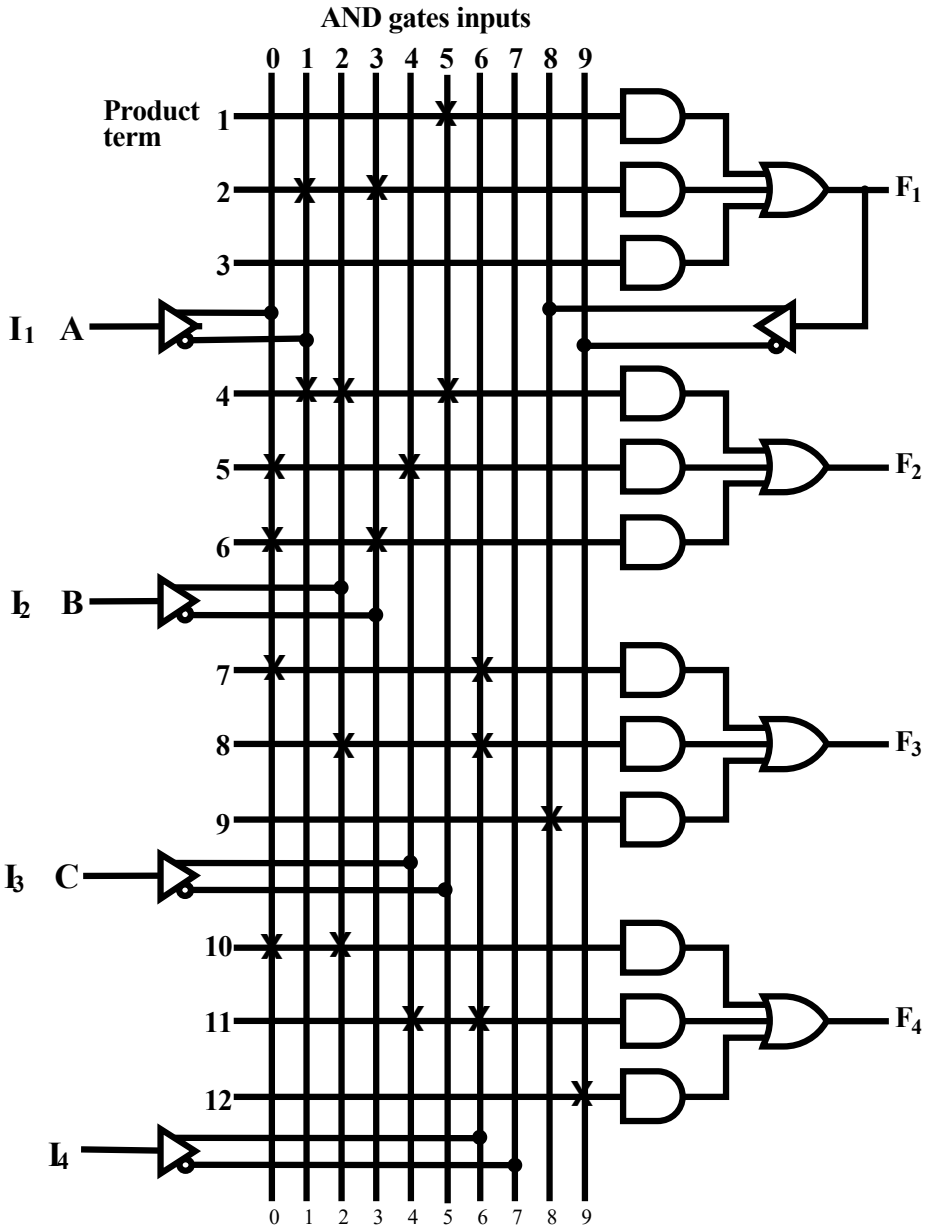
- 4-input, 4-output PAL with fixed, 3-input OR terms
- What are the equations for F1 through F4?

  F1 = $\overline{A}\ \overline{B} + \overline{C}$

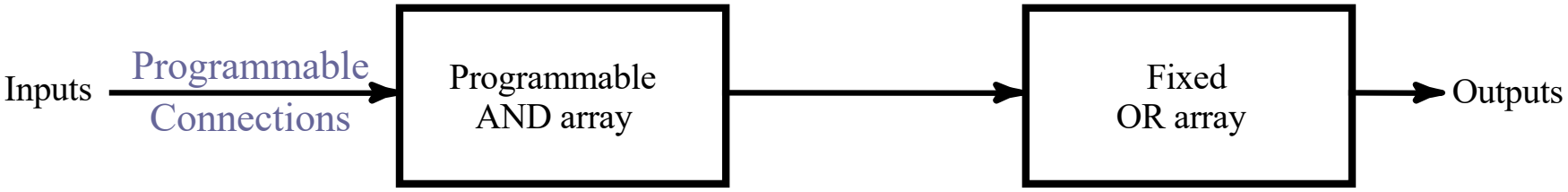
  F2 = $\overline{A}B\overline{C} + AC + AB$

  F3 =

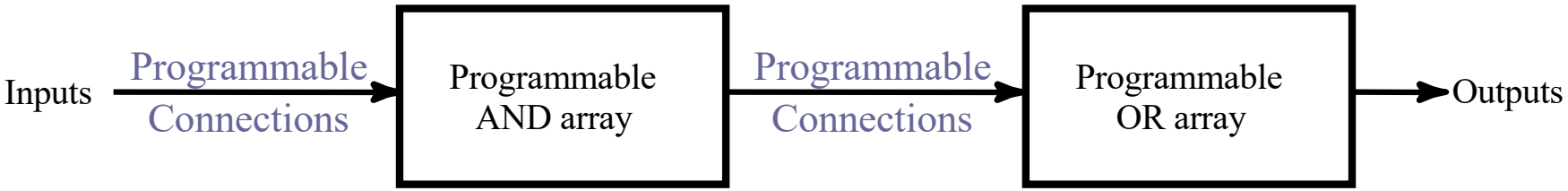
  F4 =



PAL and PLA Comparison



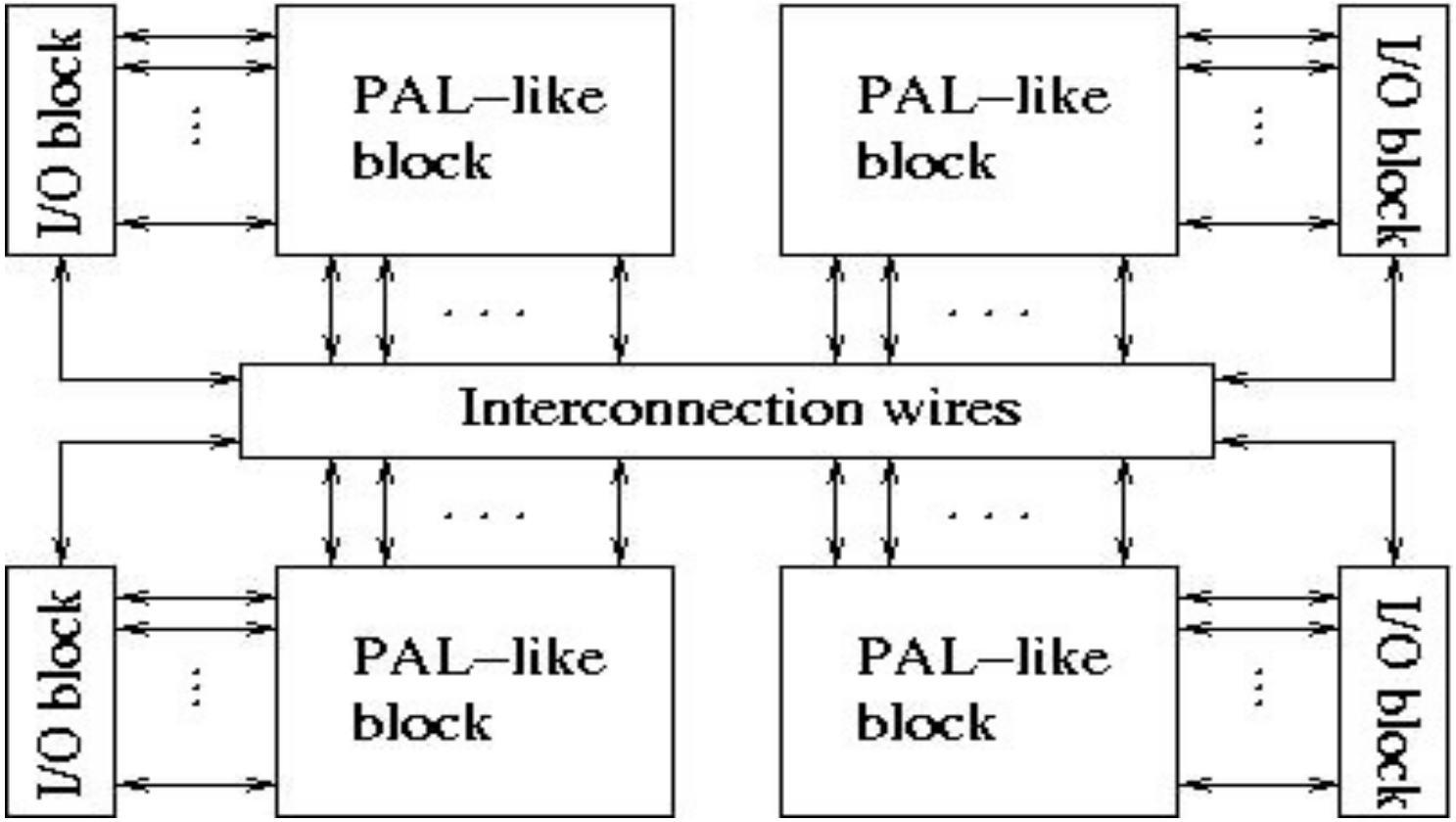
(a) Programmable array logic (PAL) device



(b) Programmable logic array (PLA) device

How to get larger capacity?

Complex Programmable Logic Device (CPLD)

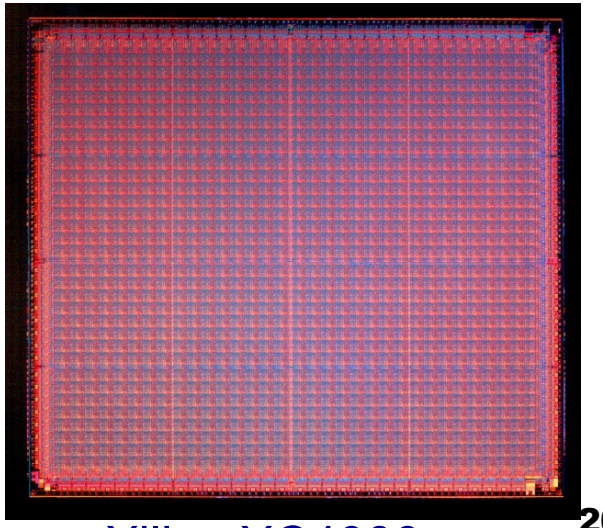


Complex Programmable Logic Device

- Combines multiple PAL-like blocks with programmable interconnect network.
- Provides much larger capacity than SPLDs.

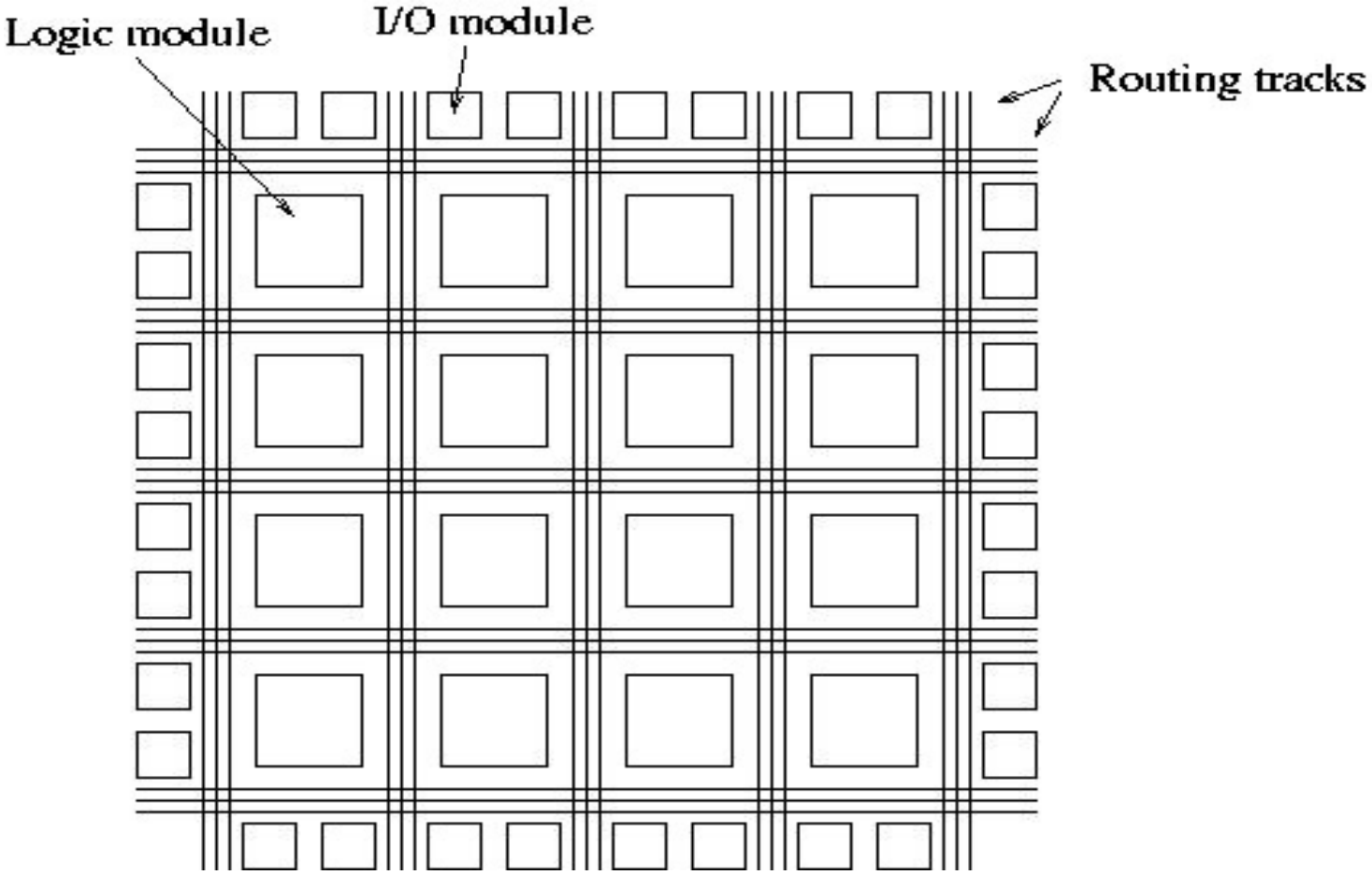
Field-Programmable Gate Array (FPGA)

- A high-capacity programmable logic device providing multi-level logic.
- Introduced in 1985 by Xilinx.
- Classic FPGA consists of an *array of programmable logic blocks* surrounded by programmable interconnect.

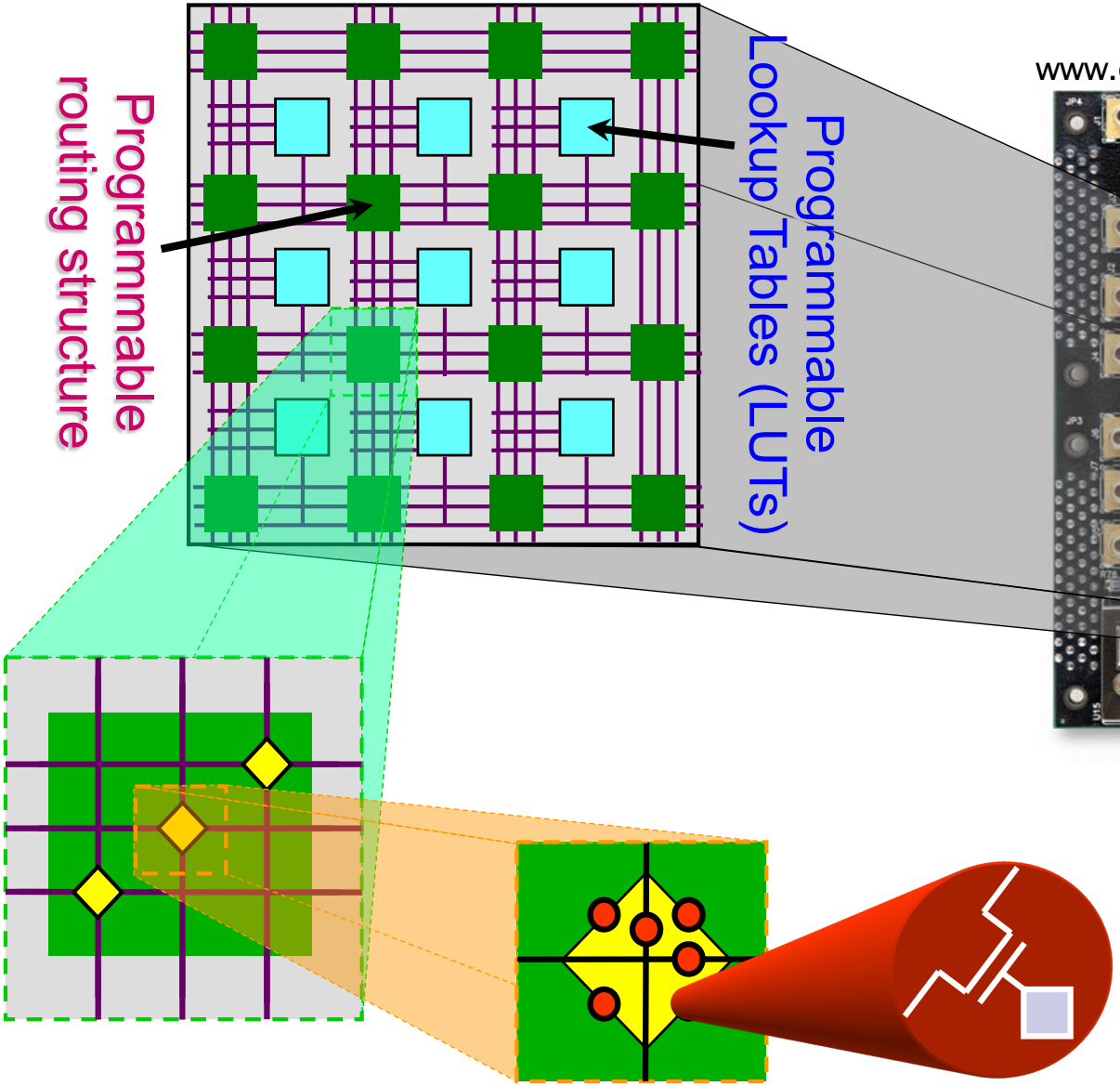


Xilinx XC4000ex

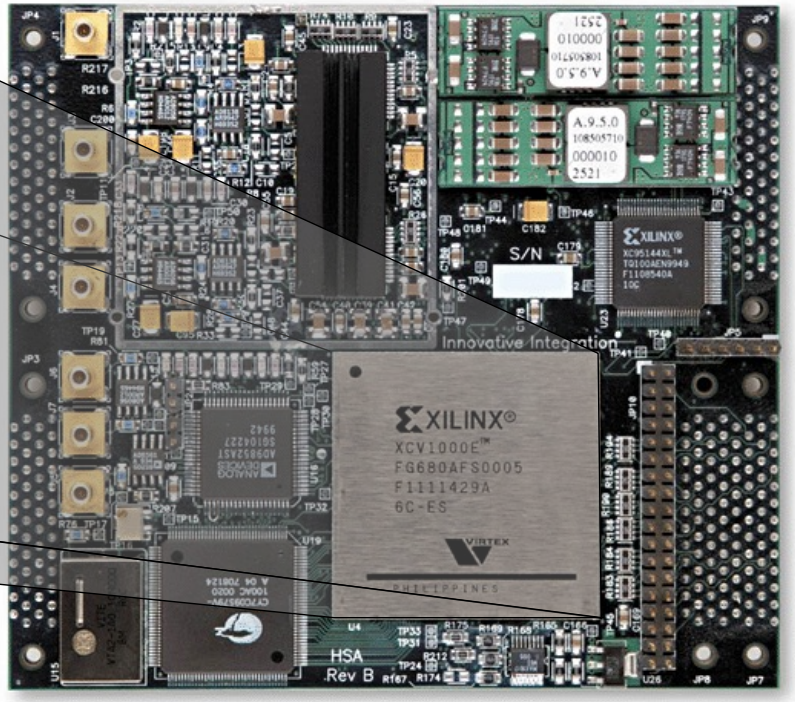
Field-Programmable Gate Array



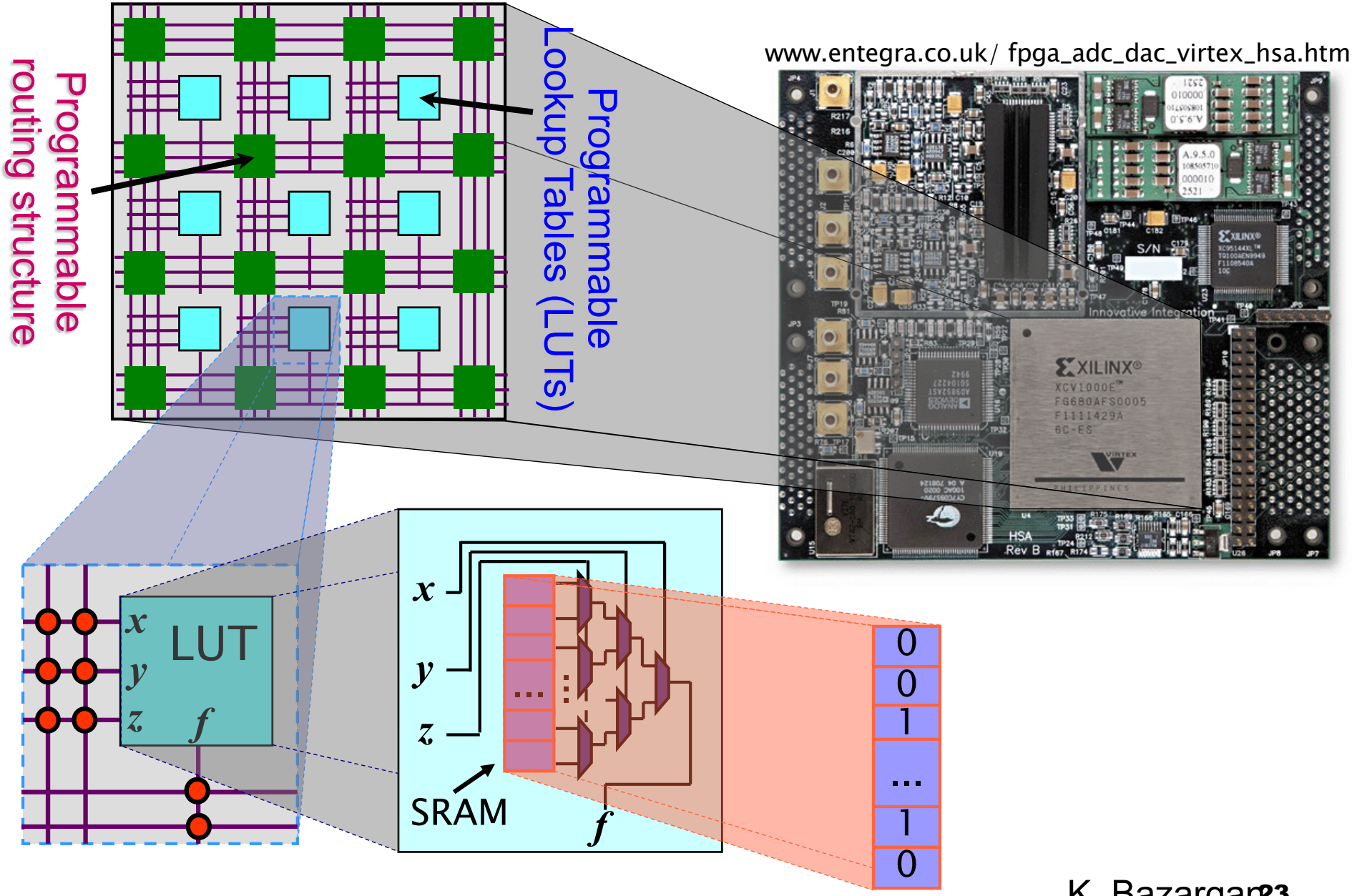
SRAM-Based FPGA



www.entegra.co.uk/ fpga_adc_dac_virtex_hsa.htm



SRAM-Based FPGA



Microprocessor vs Custom Chip vs FPGA

- Microprocessor
  - Rely on software to implement functions
  - Slowest, most power-hungry
  - Re-programmable (load different software)
- Custom Chip
  - Designed for a particular purpose
  - Fastest, most power-efficient
  - Not re-programmable
- FPGA
  - Not designed for any particular function
  - In between microprocessor and custom chip in speed and power
  - Re-programmable (most)

Rapidly Increasing Logic Capacity

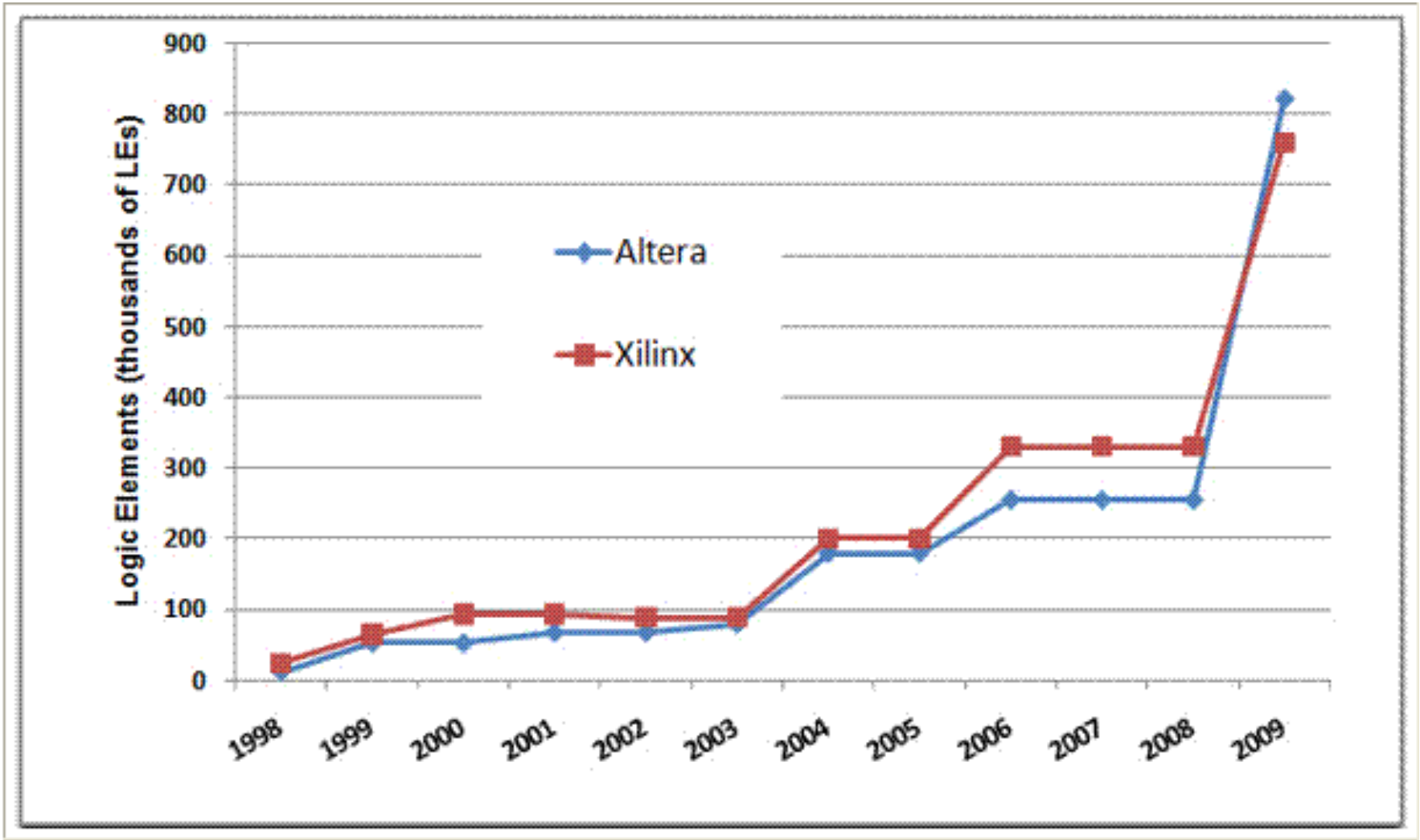
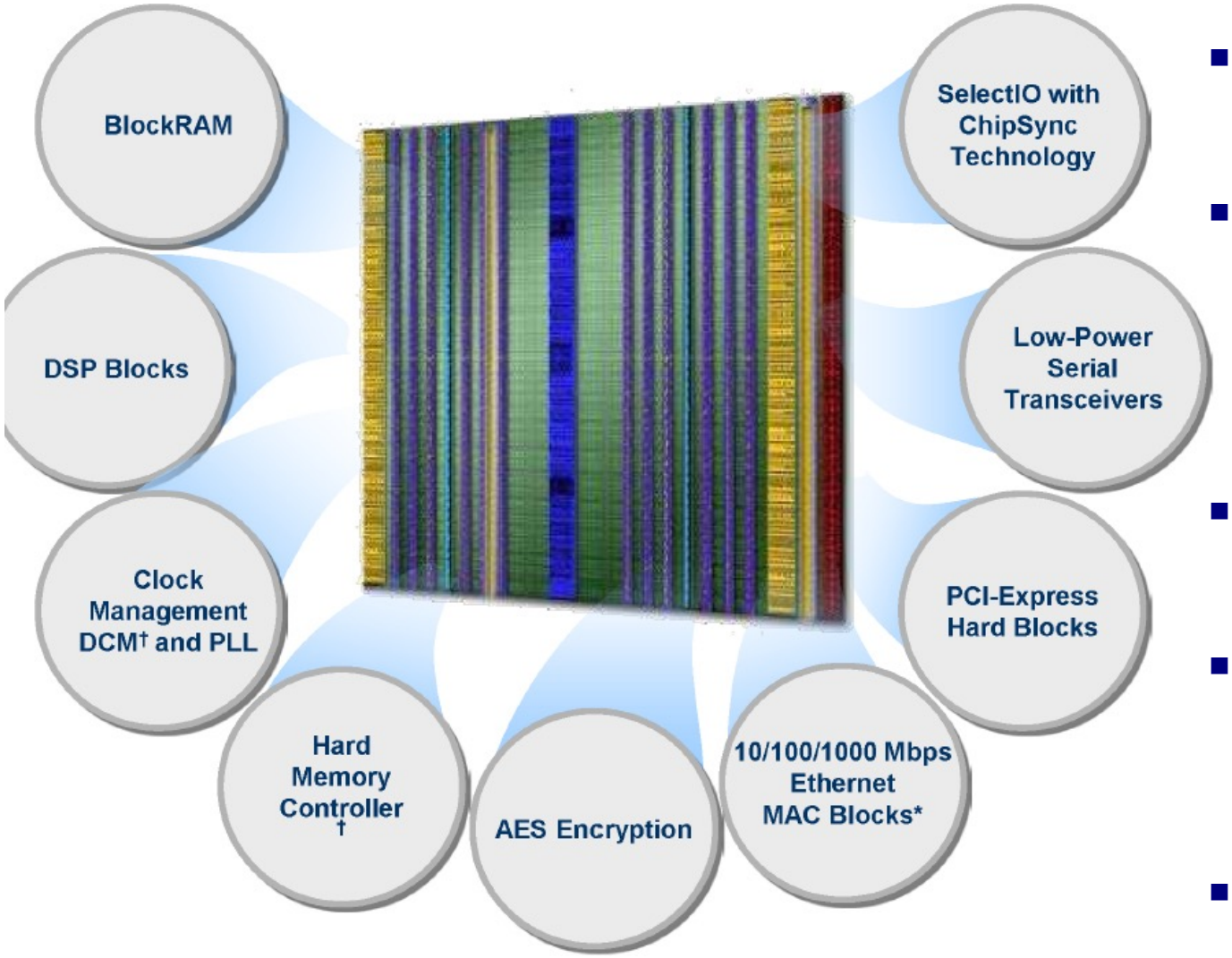


Figure 1. Largest FPGA announced (by equivalent 4-input Logic Elements - LEs).

Today's FPGAs

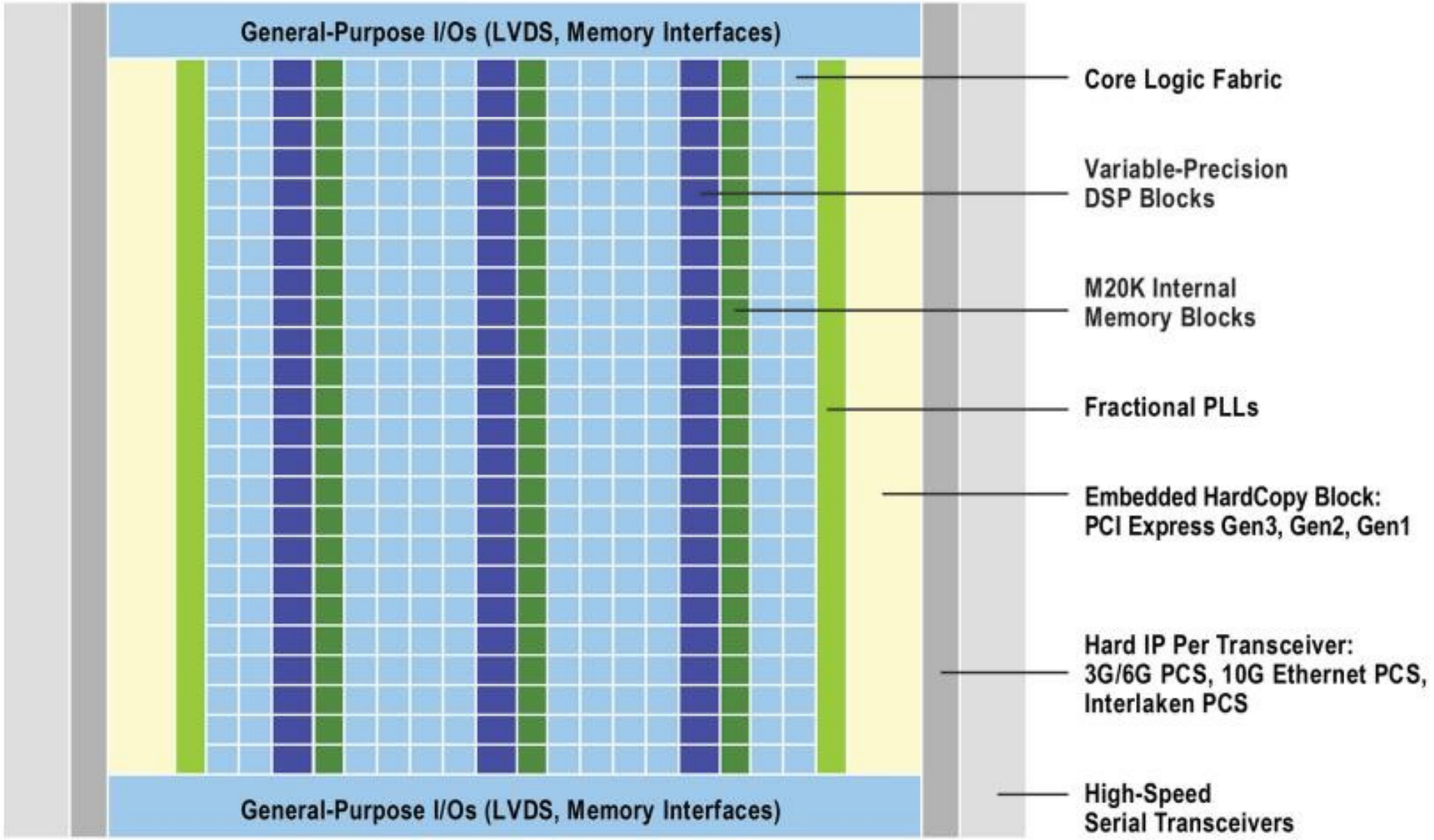
- Much more than just an array of programmable logic blocks
- Common additional resources: embedded memory blocks, fast carry logic chains, DSP blocks, etc.
- Versatile programmable I/Os
- May contain ≥ 1 microprocessors
- Applications: audio, video, wireless, industrial equipments, network components, medical, automotive, etc.
- Vendors offer a variety of FPGAs with specialized advanced features catering for different markets

Advanced Features of Today's FPGAs



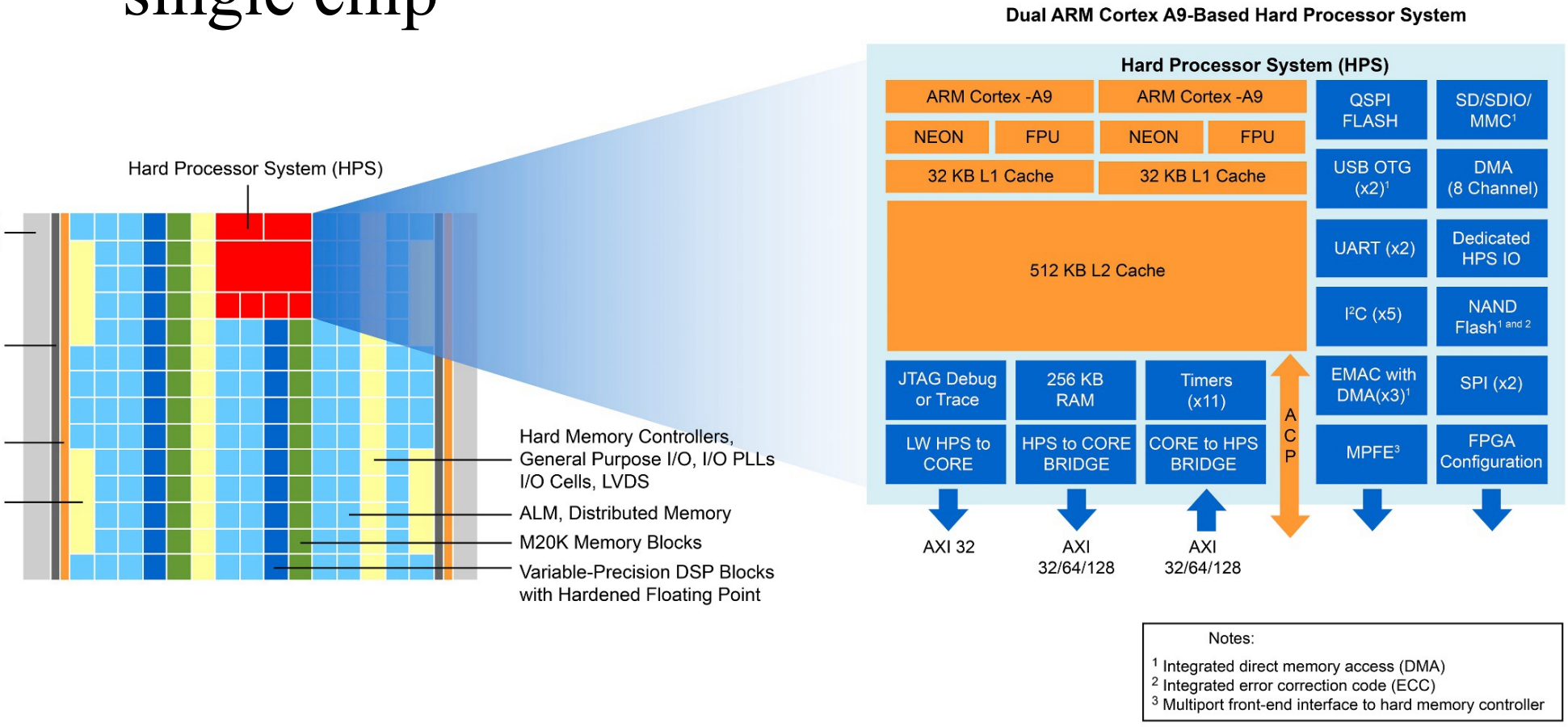
- Other resources include: Memory, DSP Slices, clock management components, and IP cores.
- Multi-Gigabit Transceiver (transmitter-receiver) does serialization and de-serialization to transmit parallel data as stream of serial bits, and convert the serial bits it receives to parallel data.
- PCI-Express is a bus interface standard for connecting components on a motherboard.
- Ethernet is the dominant wired connectivity standard. Ethernet media access controller (Ethernet MAC) block provides dedicated Ethernet functionality.
- AES encryption prevents unauthorized modification or copying.

Typical Layout of Today's FPGA



SoC FPGA

- Integrate software programmability of processor with hardware programmability of FPGA in a single chip



AI-optimized FPGAs

- Divergent DSP block requirements for different application domains
  - high-precision floating point in HPC
  - medium-precision fixed-point in communications
  - low-precision fixed-point in DL
- Embedded tensor blocks are introduced to replace conventional DSP blocks in AI-optimized FPGAs (e.g. Stratix 10 NX)

References

- S. M. Trimberger. 2015. “Three ages of FPGAs: A retrospective on the first thirty years of FPGA technology”. Proc. of IEEE, 318-331