Getting Started with Verilog Simulation

CT Verilog Series 02 Supplement 2

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登入工作站

- 首先登入工作站 (例如："ssh -X ic21". macOS 可用 "ssh -Y ic21". 請參考 How to Access **NTHUCAD Workstations** 文件。
- 登入後先建立資料夾 " `mkdir directory_name` " (例如 " `mkdir hw1` ")

```
ic21 [cthuang 10:24am] ~$mkdir hw1
```

- 進入這個資料夾 (例如：" `cd hw1` ")

```
ic21 [cthuang 10:24am] ~$cd hw1
```

Verilog Coding

- 編譯你的 Verilog code (推薦使用 Vim: " `vim filename.v` "; 利用 ftp; 或是使用 MobaXterm 上傳檔案的功能將事先準備好的檔案上傳)

```
ic21 [cthuang 9:24am] ~/hw1$vim majority.v
```

- 開啟 Vim 後按 " `i` " 進入編輯模式

```
module majority (
  a, b, c, out
);
  input a, b, c;
  output out;
  assign out = (a & b) | (a & c) | (b & c);
endmodule
```

- 編輯完後按 Esc 離開編輯模式，接著輸入 " `:wq` " (寫入及離開)
- Vim 的使用請參考**鳥哥私房菜**： https://linux.vbird.org/linux_basic/centos7/0310vi.php
- 編輯完 Verilog design 後，接著編輯 testbench.

```
ic21 [cthuang 9:24am] ~/hw1$vim majority_t.v
```

- 依照範例輸入，切記請勿直接用滑鼠剪貼 PDF 講義的文字內容，有可能複製貼上非 ASCII 字元或特殊控制字元，造成語法錯誤，不易除錯。

```
`timescale 1ns / 100ps
module test;
  reg [2:0] count;
  wire out;

  majority m(count[0], count[1], count[2], out);

  initial begin
    count = 3'b000;
    repeat (8) begin
      #100
      $display("in = %b, out = %b", count, out);
      count = count + 3'b001;
    end
  end
endmodule
```

- 觀察此目錄內目前產生的檔案，輸入 " `ls` " 可以發現有兩個檔案。

```
ic21 [cthuang 9:23am] ~/hw1$ls
majority.v  majority_t.v
```

Verilog Simulation

- 執行 Verilog Simulator (以 NCVerilog 為例)。
- 輸入"`ncverilog testbench.v filename.v `"
  在此為 `ncverilog majority_t.v majority.v`

```
ic21 [cthuang 9:30am] ~/hw1$ncverilog majority_t.v majority.v
```

- 文字模式的模擬結果如下。

```
ic21 [cthuang 9:31am] ~/hw1$ncverilog majority_t.v majority.v
ncverilog: 15.20-s039: (c) Copyright 1995-2017 Cadence Design Systems, Inc.
file: majority_t.v
        module worklib.test:v
                errors: 0, warnings: 0
file: majority.v
        module worklib.majority:v
                errors: 0, warnings: 0
                Caching library 'worklib' ....... Done
        Elaborating the design hierarchy:
        Building instance overlay tables: .................... Done
        Generating native compiled code:
                worklib.majority:v <0x2345e4c3>
                        streams:   0, words:     0
                worklib.test:v <0x795b1373>
                        streams:   4, words:  1736
        Building instance specific data structures.
        Loading native compiled code:     .................... Done
        Design hierarchy summary:
                                  Instances  Unique
                Modules:                  2       2
                Registers:                1       1
                Scalar wires:             4       -
                Initial blocks:           1       1
                Cont. assignments:        0       1
                Pseudo assignments:       3       3
                Simulation timescale:  100ps
        Writing initial simulation snapshot: worklib.test:v
Loading snapshot worklib.test:v ..................... Done
ncsim> source /usr/cad/cadence/INCISIV/cur/tools/inca/files/ncsimrc
ncsim> run
in = 000, out = 0
in = 001, out = 0
in = 010, out = 0
in = 011, out = 1
in = 100, out = 0
in = 101, out = 1
in = 110, out = 1
in = 111, out = 1
ncsim: *W,RNQUIE: Simulation is complete.
ncsim> exit
ic21 [cthuang 9:31am] ~/hw1$
```

- 如果要產生波型檔 (`filename.vcd`) 必須要在 `testbench.v` 內設定並宣告檔名。

在 Verilog Testbench 中插入額外的 initial block:

```
initial begin
  $dumpfile("majority.vcd");
  $dumpvars;
end
```

```
`timescale 1ns / 100ps
module test;
  reg [2:0] count;
  wire out;

  majority m(count[0], count[1], count[2], out);

  initial begin
    $dumpfile("majority.vcd");
    $dumpvars;
  end

  initial begin
    count = 3'b000;
    repeat (8) begin
      #100
      $display("in = %b, out = %b", count, out);
      count = count + 3'b001;
    end
  end
endmodule
```

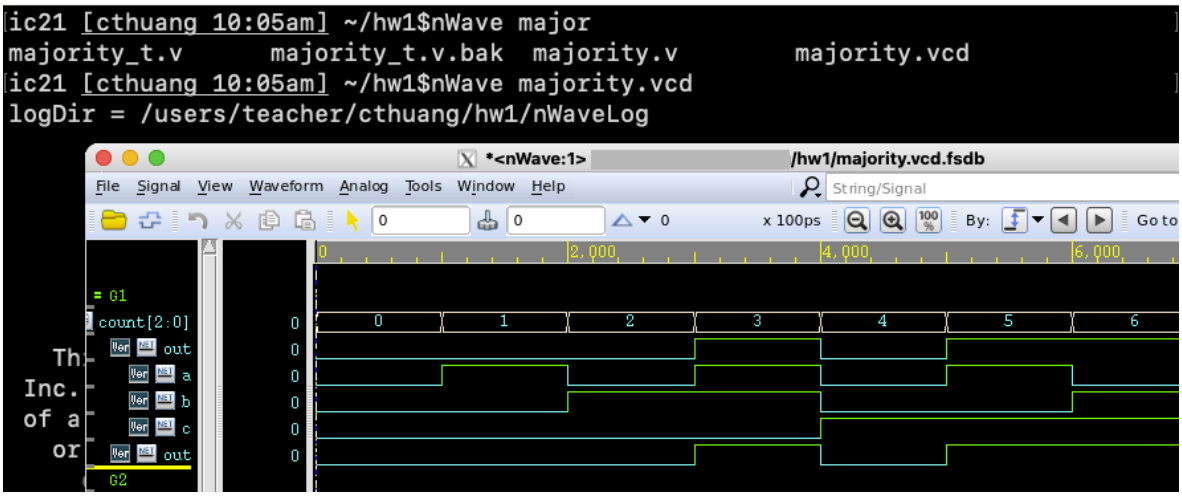
然後再執行" ncverilog testbench.v filename.v +access+r "
在此為 ncverilog majority_t.v majority.v +access+r
切記若為了紀錄波形，參數中 +access+r 不可忽略。

- 觀察此目錄內目前產生的檔案，執行 " ls "

```
ic21 [cthuang 9:37am] ~/hw1$ls
INCA_libs/  majority.vcd  ncverilog.history
majority.v  majority_t.v  ncverilog.log
```

- 可以看到出現 " filename.vcd " (在此為 majority.vcd)
- 執行 nWave (請參考 How to Access NTHUCAD Lab 中有關 DISPLAY 環境變數的設定，務必正確設定，才能遠端開啟工作站的圖形界面)。

1. 亦可下 " nWave majority.vcd " 直接打開波形檔。
2. 如果用 " nWave& " 可以將 nWave 丟到背景執行。若發現會有螢幕閃爍的情形，可以先打 nWave ⏎ 之後，按下 CTRL-z, 再打 bg ⏎ 轉到背景執行試試看，這也是一般前景轉背景執行的方式)
3. nWave 會自動把 majority.vcd 轉存成 majority.vcd.fsdb.



- 請參考講義，學會在 nWave 中加入信號以觀察模擬結果。