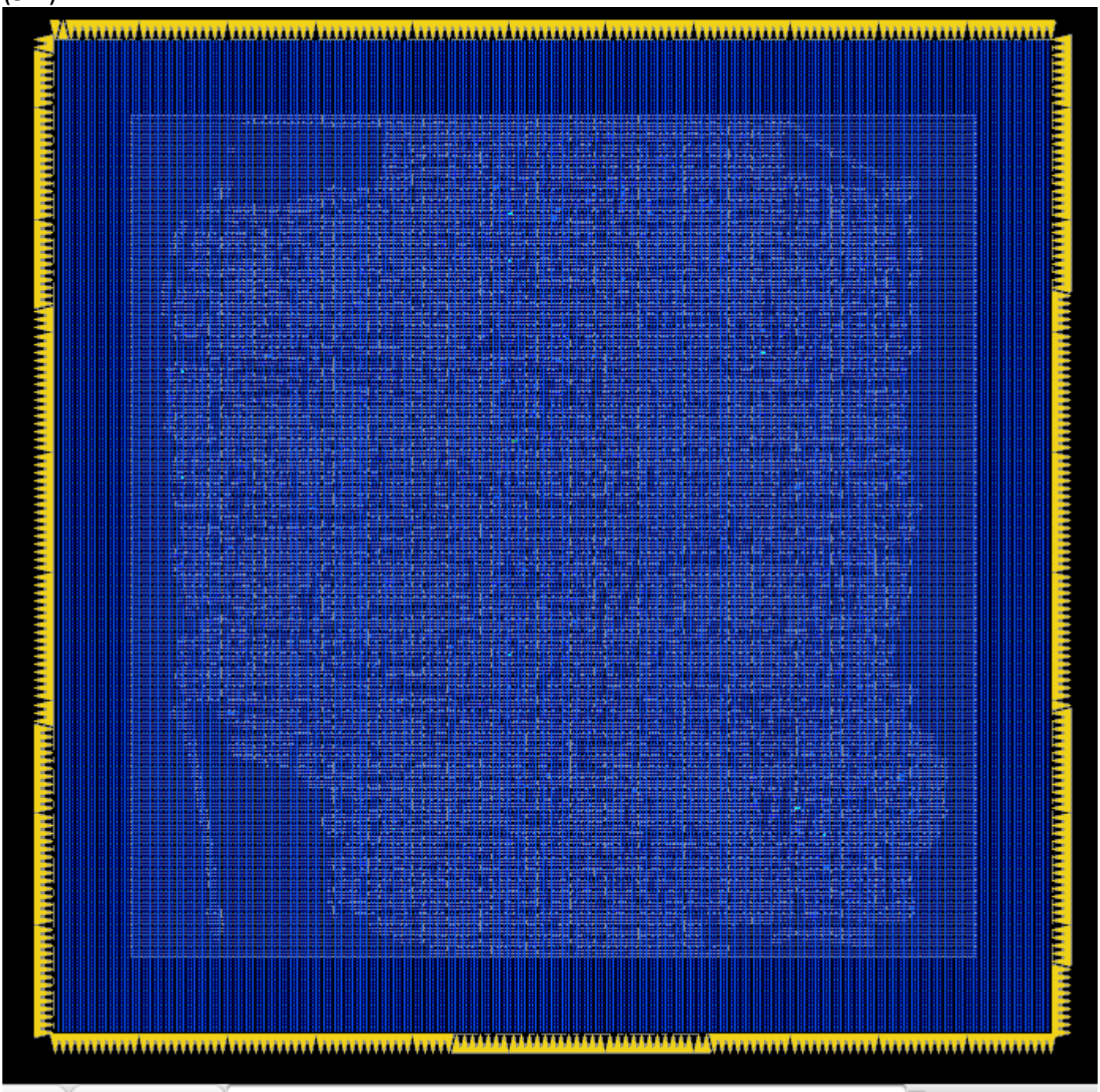
Homework 6 Report

Student ID: 112062542 Name: 賴琮翰

1. Questions (Brief and concise explanation of one to two pages would be enough. You may use Chinese. Don't copy the problem statement, just write the answer.)
Please write down the sub-question number even if you don't know how to

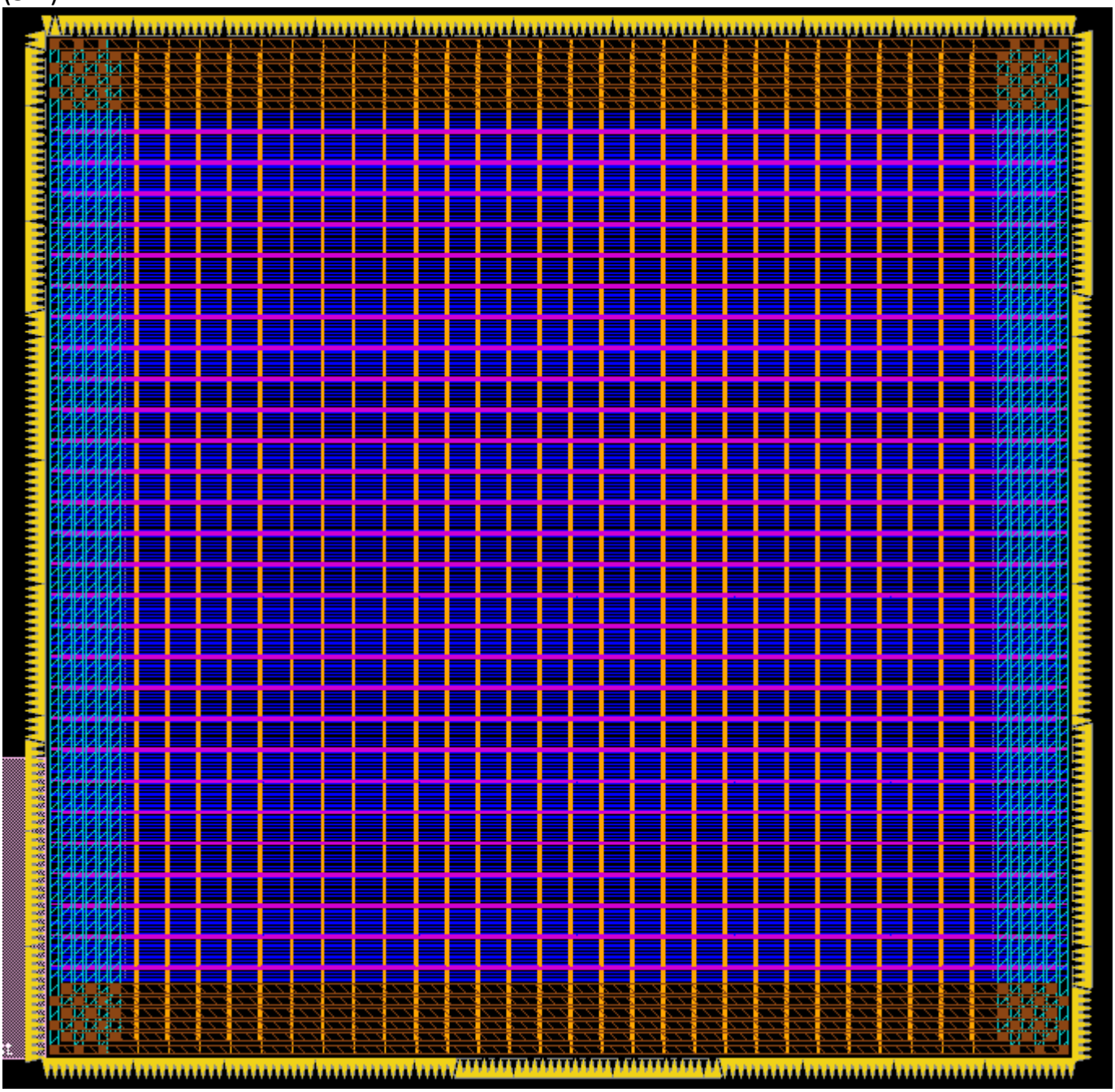
(1.a) 設定跑 Apr 的參數如: 使用製程檔，並讀取重要檔案，如: synthesis 後的 Verilog file，以及包含 design rule 的 LEF file 等。
(1.b) 設定 placement 的區域，包含晶片長寬比、chip 擺放比例等
(1.c) 設定 VDD、VSS 的 Metal 寬度與擺放位置
(1.d) 決定 standard cell 在晶片上的位置
(1.e) 決定 clock signal 連接元件的方式
(1.f) 決定 standard cell 連接的方式
(1.g) 把 track 上的空隙補滿，以利後續晶圓生產
(2.a) 電路的 gate-level netlist，經過 technology mapping 後使用 library 內的 cell，之後的後端流程即採這些 cell
(2.b) 包含電路 timing 以及 design constraint，讓 tool 可以知道 design 的 timing 需求
(2.c) 包含電路中 delay 有關的訊息，以便用在 post-sim simulation
(2.d) 當電路跑完 apr 後，.gds 用來描述產生出來的 layout
(2.e) 包含上述四個檔案的壓縮檔
(3) 因為 RTL simulation 主要目標為確認電路功能正確性，因此不需要 timing 相關資訊，且 RTL 時還沒有包含具體的 cell 以及 layout，因此也沒有實際上的物理延遲。
(4) Pre-layout power analysis 主要是為了早期設計的 power 估算，並沒有考慮實際的寄生電容以及繞線的 delay，因此結果較初略。Post-layout power analysis 包含了電路實際 layout 後產生的電阻電容，power 估算結果較準，而使用 post-sim waveform 又比使用 pre-sim waveform 結果準，原因是 post-sim waveform 有考慮電路實際的 timing。

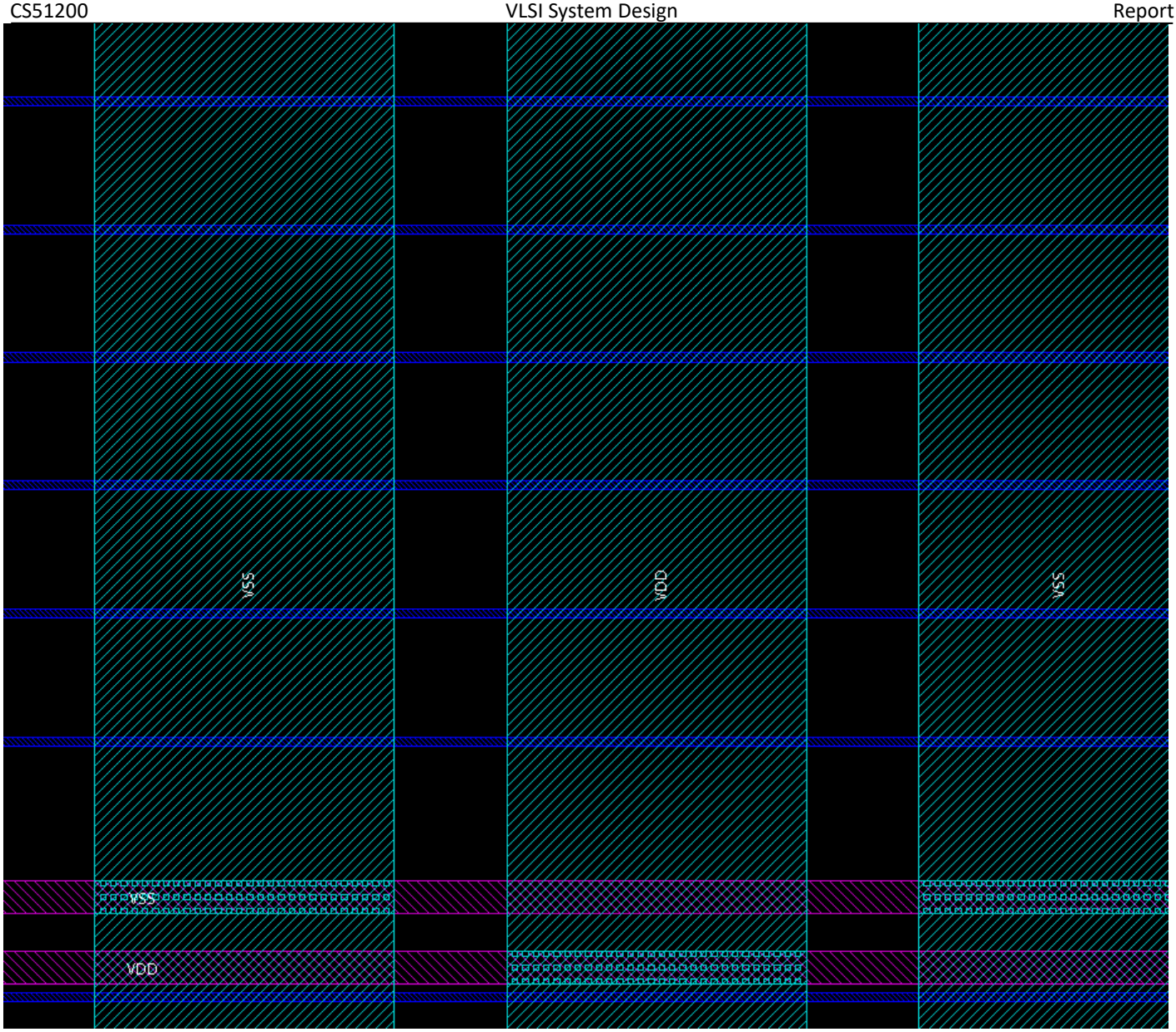
(5.1)

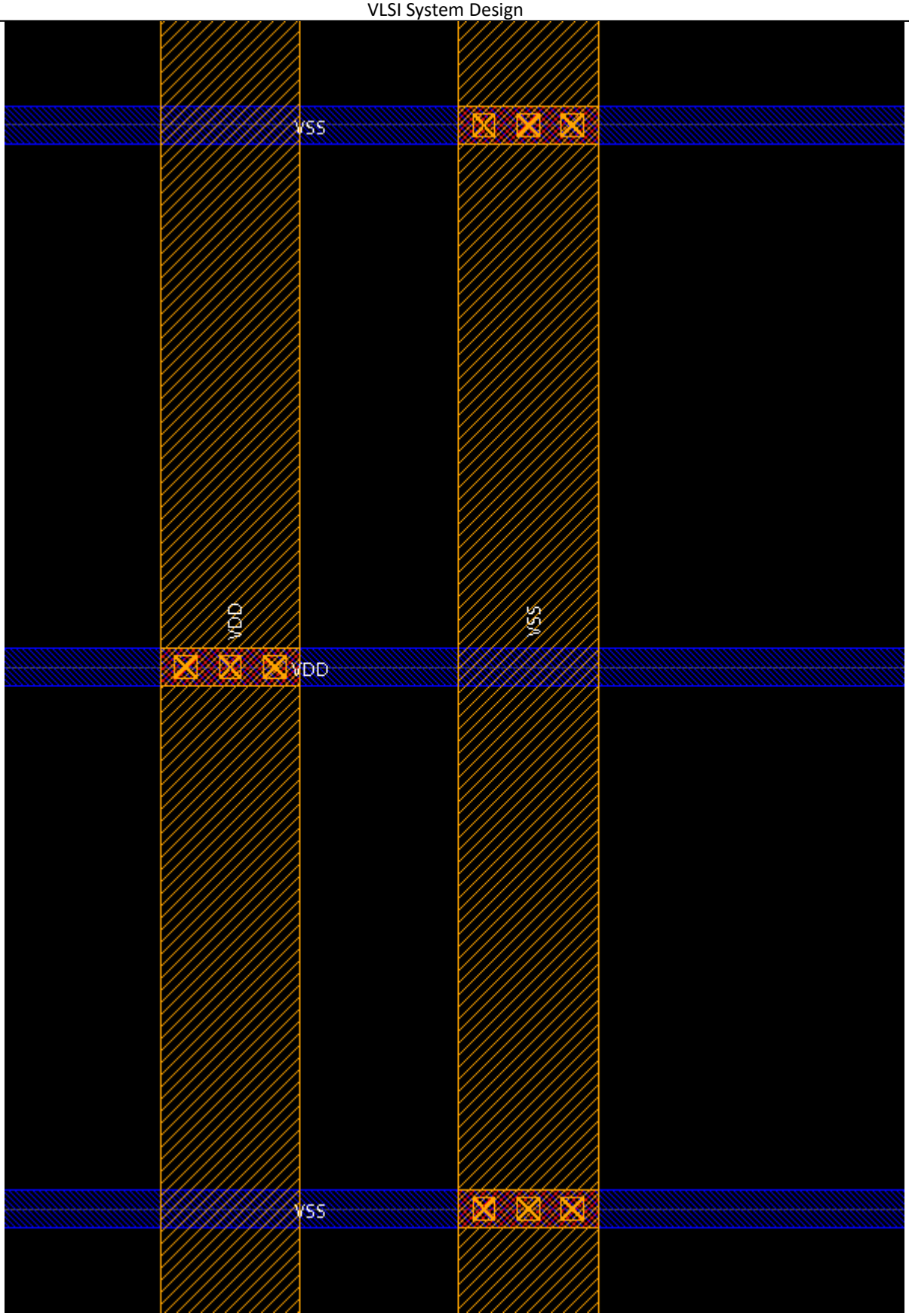


Congestion Map 可以發現 avaliable routing tracks 的數量並沒有多過於 nets 的數量(即 Overflow 多為代表 negative value 的藍色)。

(5.2)




VSS
VDD
VSS
VSS
VDD



Q. Where are the Tap cells placed?

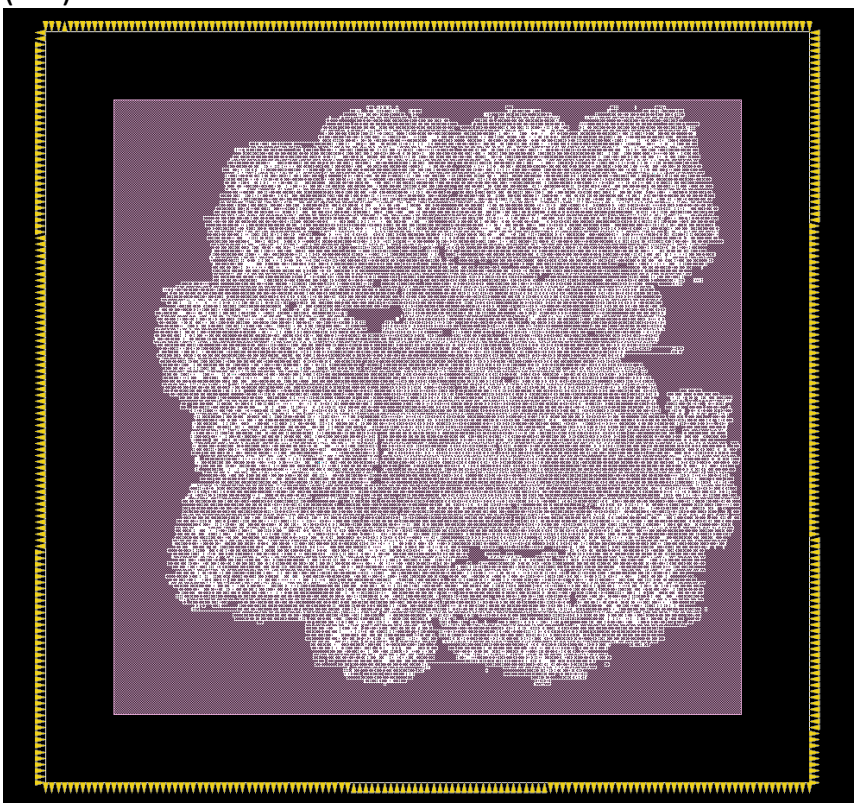
A: 有規律的放在兩個 track 中間

(5.3)

Q: How do standard cells connect with power/ground pins?

A: 用頂端或尾端連接，且相鄰兩個 track 的 standard cells 方向顛倒

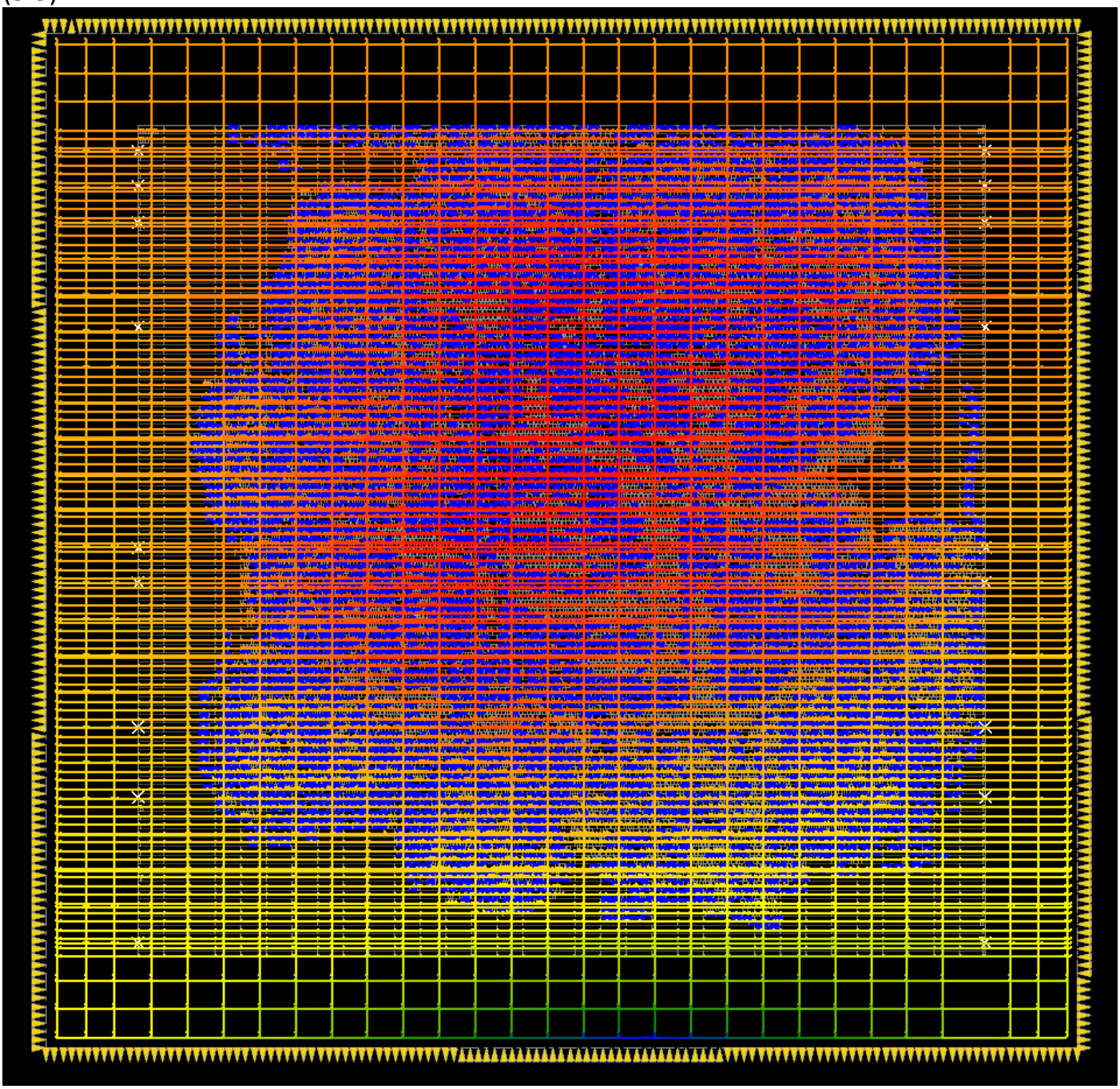
(5.4)



Q: How does the layout partitioned?

A: 根據不同 **module** 功能切割，舉例來說，最外層切成 **fc** 和 **conv_1**

(5.5)



Q. What is the worst IR drop? (Optional: Is it acceptable?)

A. 2.8402 · I think it is acceptable

(5.6)

```
Reporting Utilizations.....

Core utilization  = 55.218653
Effective Utilizations
Average module density = 0.533.
Density for the design = 0.533.
       = stdcell_area 158661 sites (54262 um^2) / alloc_area 297755 sites (101832 um^2).
Pin Density = 0.2337.
            = total # of pins 72586 / total area 310607.
*** Message Summary: 0 warning(s), 0 error(s)
```

(5.7)

```
*Verdi* : Create FSDB file 'lenet_post.fsdb'
*Verdi* : Begin traversing the scopes, layer (0).
*Verdi* : End of traversing.
Reset System
Compute start
Compute finished, start validating result...
====================
Image             [PASS]
Conv 1 activation [PASS]
Conv 2 activation [PASS]
Conv 3 activation [PASS]
FC   1 activation [PASS]
FC   2 activation [PASS]
>>> Congratulation! All result are correct
  [Post-layout gate-level simulation]
Clock Period:          10 ns,Total cycle count:       29508 cycles
====================
Simulation finish
Simulation complete via $finish(1) at time 296115392 PS + 0
./lenet_tb.v:202         $finish;
xcelium> exit
TOOL:   xmverilog      22.03-s003: Exiting on May 31, 2024 at 03:39:26 CST  (total: 00:01:13)
```

(5.8)

```
// Mapping key points ...
============================================================================
Mapped points: SYSTEM class
----------------------------------------------------------------------------
Mapped points     PI     PO     DFF       Total
----------------------------------------------------------------------------
Golden            291    209    947       1447
----------------------------------------------------------------------------
Revised           291    209    947       1447
============================================================================
CPU time     : 2.86    seconds
Elapse time  : 3       seconds
Memory usage : 135.10  M bytes
// Command: map key point
// Mapping key points ...
============================================================================
Mapped points: SYSTEM class
----------------------------------------------------------------------------
Mapped points     PI     PO     DFF       Total
----------------------------------------------------------------------------
Golden            291    209    947       1447
----------------------------------------------------------------------------
Revised           291    209    947       1447
============================================================================
// Command: analyze multiplier -cdp_info
CPU time     : 3.24    seconds
Elapse time  : 3       seconds
Memory usage : 135.35  M bytes
// Command: analyze datapath -merge -share -effort medium -verbose
CPU time     : 3.64    seconds
Elapse time  : 4       seconds
Memory usage : 137.61  M bytes
// Command: add compare point -all
// 1156 compared points added to compare list
// Command: compare
============================================================================
Compared points      PO     DFF       Total
----------------------------------------------------------------------------
Equivalent           209    947       1156
============================================================================
CPU time     : 3.96    seconds
Elapse time  : 4       seconds
Memory usage : 144.02  M bytes
// Command: analyze abort -compare
There is no abort/specified point to be analyzed.
// Command: report unmap point -notmapped
There is no unmapped point
// Command: usage
CPU time     : 3.96    seconds
Memory usage : 144.09  M bytes
// Command: report compare data -nonequivalent
0 Non-equivalent point(s) reported
0 compared point(s) reported
============================================================================
Compared points      PO     DFF       Total
----------------------------------------------------------------------------
Equivalent           209    947       1156
============================================================================
// Command: exit -force
```

(5.9)

```
  Attributes
  ----------
    i  -  Including register clock pin internal power
    u  -  User defined power group

                          Internal  Switching  Leakage    Total
Power Group               Power     Power      Power      Power   (     %)  Attrs
--------------------------------------------------------------------------------
clock_network           3.953e-04    0.0000    0.0000 3.953e-04 (49.16%)  i
register                1.345e-05 8.083e-06 2.034e-07 2.174e-05 ( 2.70%)
combinational           2.573e-04 1.282e-04 1.663e-06 3.871e-04 (48.14%)
sequential                 0.0000    0.0000    0.0000    0.0000 ( 0.00%)
memory                     0.0000    0.0000    0.0000    0.0000 ( 0.00%)
io_pad                     0.0000    0.0000    0.0000    0.0000 ( 0.00%)
black_box                  0.0000    0.0000    0.0000    0.0000 ( 0.00%)

  Net Switching Power  = 1.363e-04   (16.94%)
  Cell Internal Power  = 6.660e-04   (82.82%)
  Cell Leakage Power   = 1.867e-06   ( 0.23%)
                         ---------
Total Power            = 8.042e-04  (100.00%)

X Transition Power     = 1.738e-05
Glitching Power        =    0.0000

Peak Power             =    0.9484
Peak Time              = 38055.000
```

(5.10)

```
  Attributes
  ----------
    i  -  Including register clock pin internal power
    u  -  User defined power group

                          Internal  Switching  Leakage    Total
Power Group               Power     Power      Power      Power   (     %)  Attrs
--------------------------------------------------------------------------------
clock_network           4.065e-04 7.340e-05 9.194e-09 4.800e-04 (27.38%)  i
register                3.719e-05 1.463e-05 2.033e-07 5.202e-05 ( 2.97%)
combinational           6.349e-04 5.843e-04 1.728e-06 1.221e-03 (69.65%)
sequential                 0.0000    0.0000    0.0000    0.0000 ( 0.00%)
memory                     0.0000    0.0000    0.0000    0.0000 ( 0.00%)
io_pad                     0.0000    0.0000    0.0000    0.0000 ( 0.00%)
black_box                  0.0000    0.0000    0.0000    0.0000 ( 0.00%)

  Net Switching Power  = 6.723e-04   (38.36%)
  Cell Internal Power  = 1.079e-03   (61.53%)
  Cell Leakage Power   = 1.940e-06   ( 0.11%)
                         ---------
Total Power            = 1.753e-03  (100.00%)

X Transition Power     = 2.264e-05
Glitching Power        = 2.664e-06

Peak Power             =    0.0487
Peak Time              = 25675.100
```

(5.11)

```
  Attributes
  ----------
      i  -  Including register clock pin internal power
      u  -  User defined power group

                                 Internal  Switching  Leakage    Total
Power Group                      Power     Power      Power      Power   (     %)  Attrs
--------------------------------------------------------------------------------------
clock_network                  4.065e-04 7.340e-05 9.194e-09 4.800e-04 (42.25%)  i
register                       1.291e-05 1.470e-05 2.033e-07 2.781e-05 ( 2.45%)
combinational                  3.193e-04 3.074e-04 1.726e-06 6.283e-04 (55.31%)
sequential                        0.0000    0.0000    0.0000    0.0000 ( 0.00%)
memory                            0.0000    0.0000    0.0000    0.0000 ( 0.00%)
io_pad                            0.0000    0.0000    0.0000    0.0000 ( 0.00%)
black_box                         0.0000    0.0000    0.0000    0.0000 ( 0.00%)

  Net Switching Power          = 3.954e-04   (34.81%)
  Cell Internal Power          = 7.387e-04   (65.02%)
  Cell Leakage Power           = 1.939e-06   ( 0.17%)
                                 ---------
Total Power                    = 1.136e-03  (100.00%)

X Transition Power             = 2.118e-05
CAPP Estimated Glitching Power = 1.018e-04

Peak Power                     = 2.482e-03
Peak Time                      =  47400.00
```

2. Others (optional)
   - Suggestions or comments about this class to teacher or TA.