CS 5122-00
VLSI Design for Manufacturability

麥偉基

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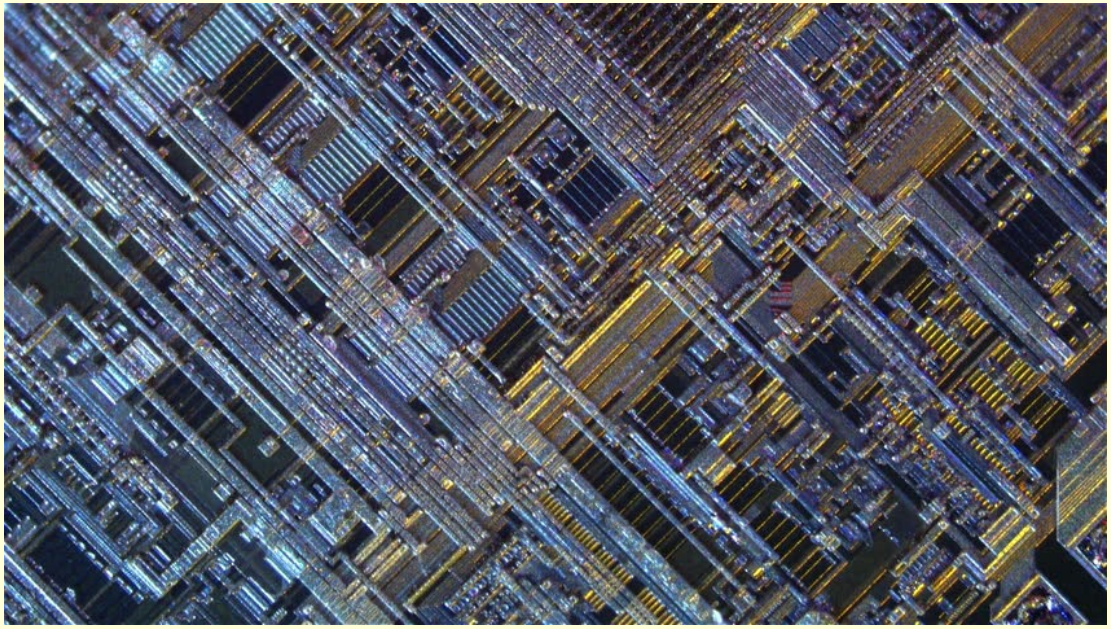
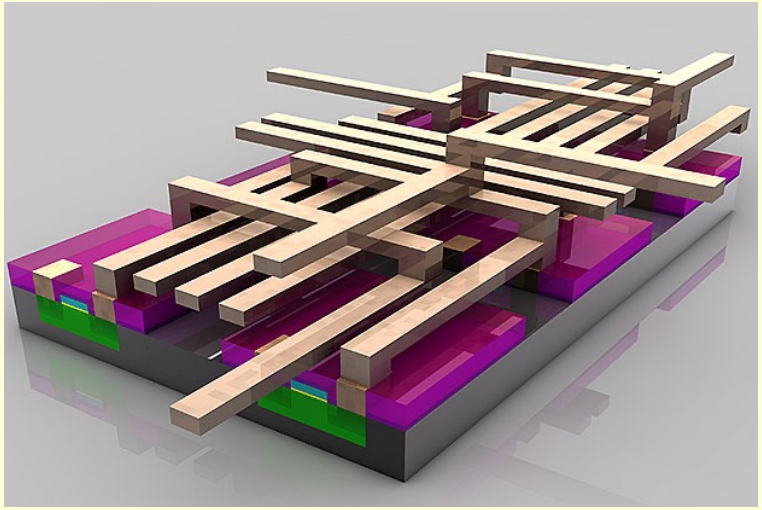
What is VLSI DFM?

Inside of a Silicon Chip

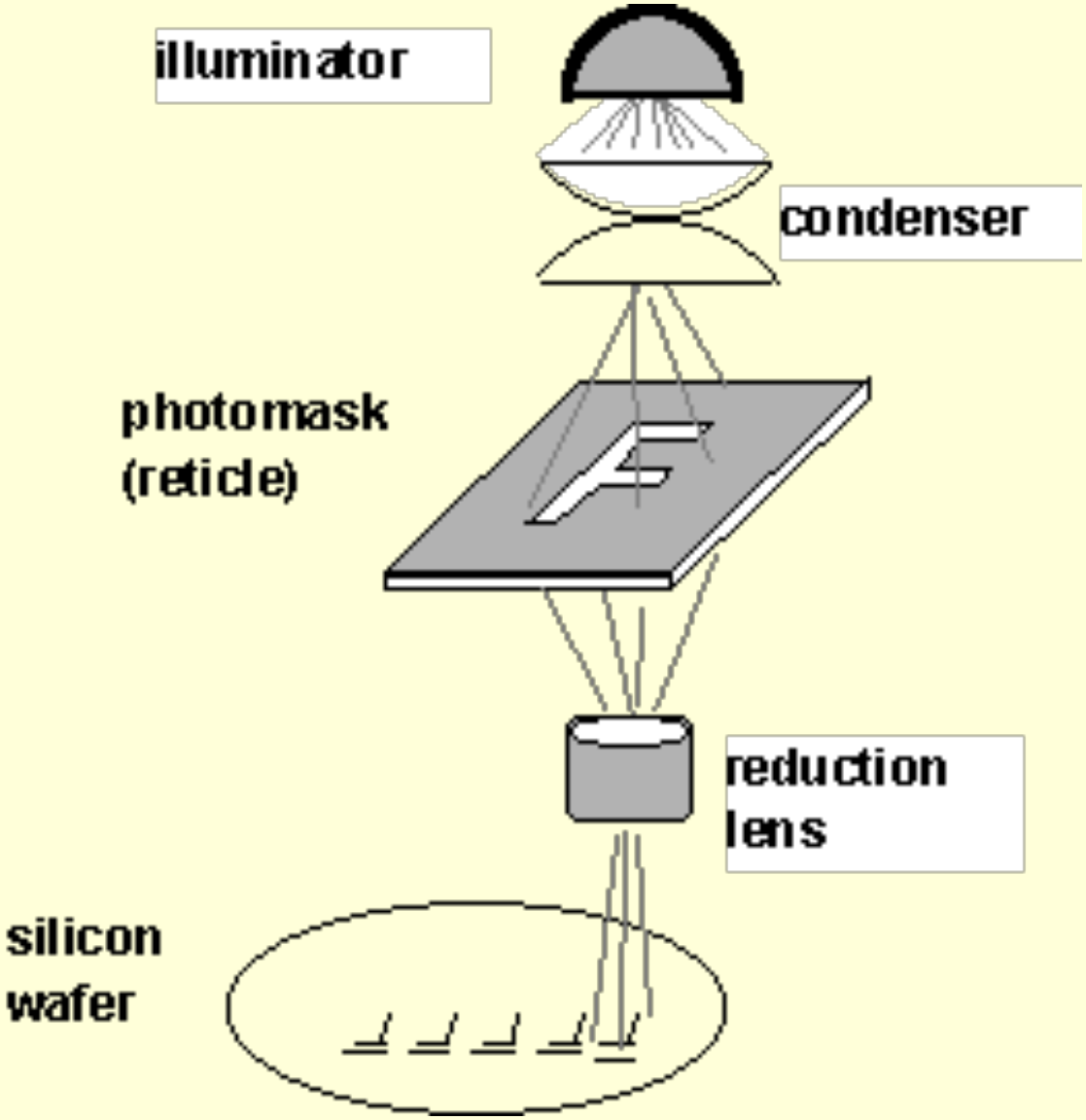


Complicated 3D structures inside a chip



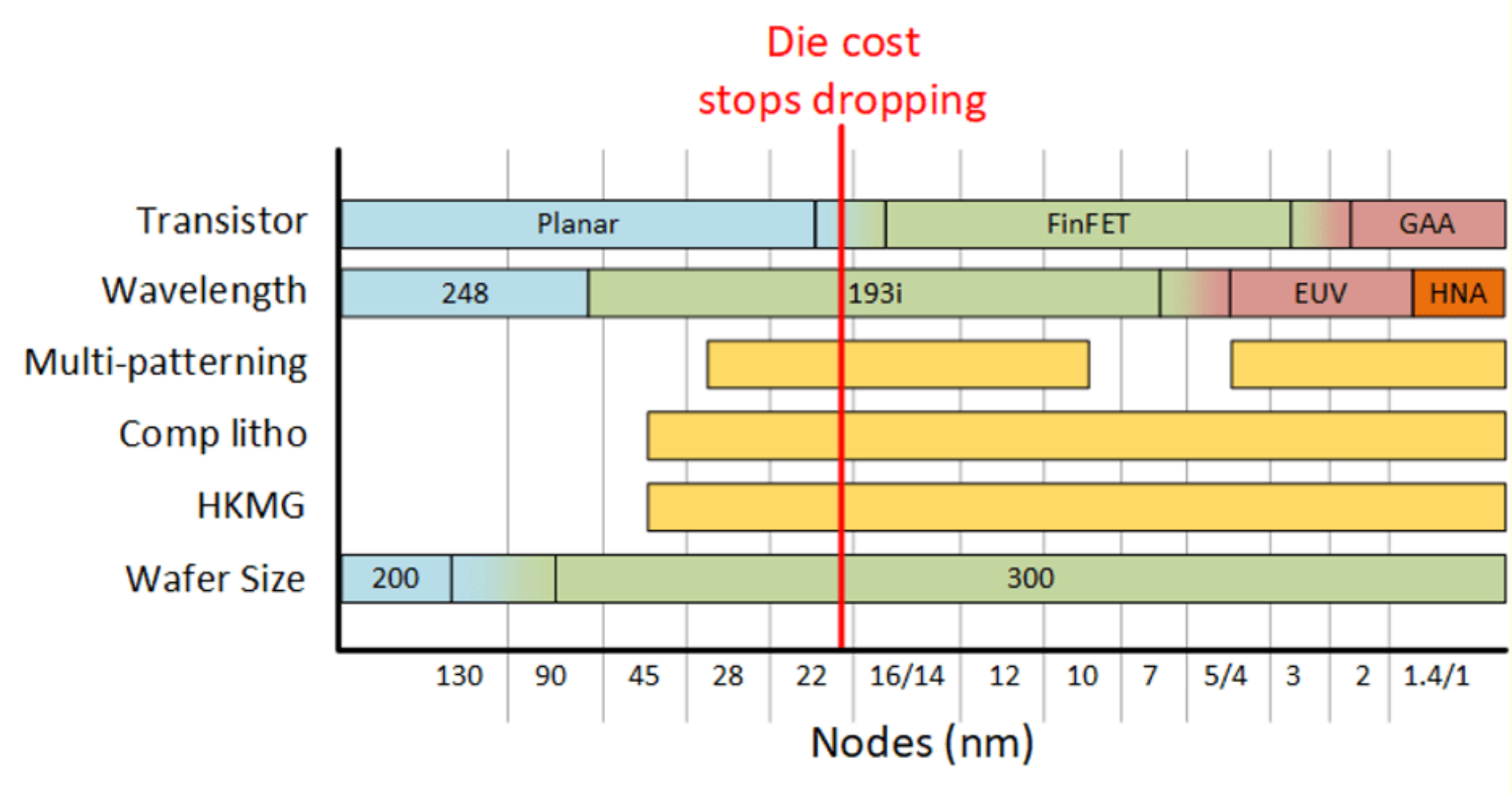
Magnified view: layers of geometric shapes forming complex circuitry

Simplified View of Lithography



But can any arbitrary layout be realized (i.e., lithography-friendly)?

Lithography Development in Last Two Decades



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- IC fabrication process is imperfect and has various limitations
- Related topics
  - Routing under Nanometer Design Rules
  - Redundant Via Insertion
  - Dummy Fill Insertion
  - Detailed Placement Refinement for Complex Manufacturing Constraints
  - Lithography Hotspot Detection
  - Mask Optimization

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- Leading edge lithography to keep scaling
  - Different kinds of multiple patterning
  - Introduction of EUV
- Related topics
  - Double/Triple Patterning Layout Decomposition
  - Double/Triple Patterning-Aware Routing
  - Double/Triple Patterning-Aware Detailed Placement
  - Self-Aligned Double Patterning Layout Decomposition
  - Self-Aligned Double Patterning-Aware Routing
  - CAD for EUV Lithography

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- Other topics
  - E-beam Direct Write/Mask Writing
  - Optimization with Hybrid Lithography (multiple patterning/DSA/e-beam)

About Instructor

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Learning Resources

- Course webpage
  - NTHU eeclass http://eeclass.nthu.edu.tw/
  - Lecture notes, assignments will be posted there

Assessment

- Written assignments 40%
- Coding Project 30%
- Exam 30%