VLSI Physical Design Automation

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National Yang Ming Chiao Tung University

Course Contents

- Introduction to VLSI/SoC design flow
- Traditional physical design processes
  - Partitioning
  - Floorplanning
  - Placement & pin assignment
  - Routing (global, detailed, clock, and power/ground routing)
  - Post-layout optimization
- Current physical design concerns and new methodologies
  - Signal/power integrity: noise modeling & optimization, IR drop
  - Design methodology: interconnect-centric design flow, buffer/wiring planning, low power methodology
  - Design for manufacturability: process variation, antenna effects, metal-fill

Objectives of This Course

- To learn essential concepts of EDA and physical design
- To get familiar with VLSI/SoC design flow and methodologies
- To learn the core/basic data structures and algorithms used in commercial EDA back-end tools
- To learn more about current deep submicron (DSM) effects and design challenges
- To learn the best of both worlds all at once: hardware and software design
- This course is suitable for graduate/senior students, IC design engineers, and CAD tool department engineers

Administrative Matters

- **Prerequisites:** data structures (or algorithms) & logic/VLSI design
- **Recommended Texts:**
  - Sait and Youssef, *VLSI Physical Design Automation: Theory and Practice,* World Scientific Publishing Co., 1999.
  - Sherwani, *Algorithms for VLSI Physical Design Automation*, 3rd Ed, Kluwer Academic Pub., 1999.
  - Kahng, Lienig, Markov, *VLSI Physical Design: From Graph Partitioning to Timing Closure,* Springer, 2011
  - Lim, *Practical Problems in VLSI Physical Design Automation*, Springer, 2008
  - Wang, Chang, and Cheng (Eds.), *Electronic Design Automation*, MK, 2009
  - Alpert, Mehta, and Sapatnekar (Eds.), *Handbook of Algorithms for Physical Design Automation*, CRC, 2009
- **References:**
  - Selected reading materials from recent publications

Administrative Matters (cont)

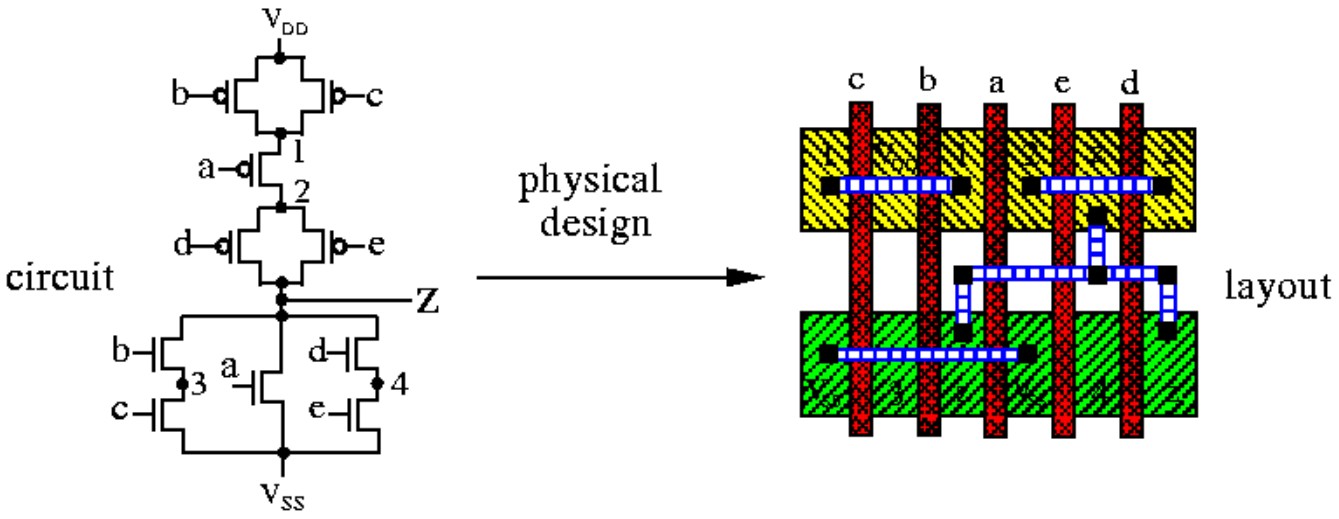
- **Grading:**
  - Individual Projects/Labs/Practices (70%)
    - 4 Labs: corner-stitching, floorplanning, 3D placement and A*search global routing
    - Modified from contest problems
  - Exams (30%): Final (open book)

- **Webpage:**
  - E3
  - Contains lecture notes, homeworks, projects, class supplemental materials and related links

- Office hours
  - Instructor: ED 407 Monday 3:30-4:30pm (by appointment)
  - TA: 張皓儒 black1120rock@gmail.com

Introduction

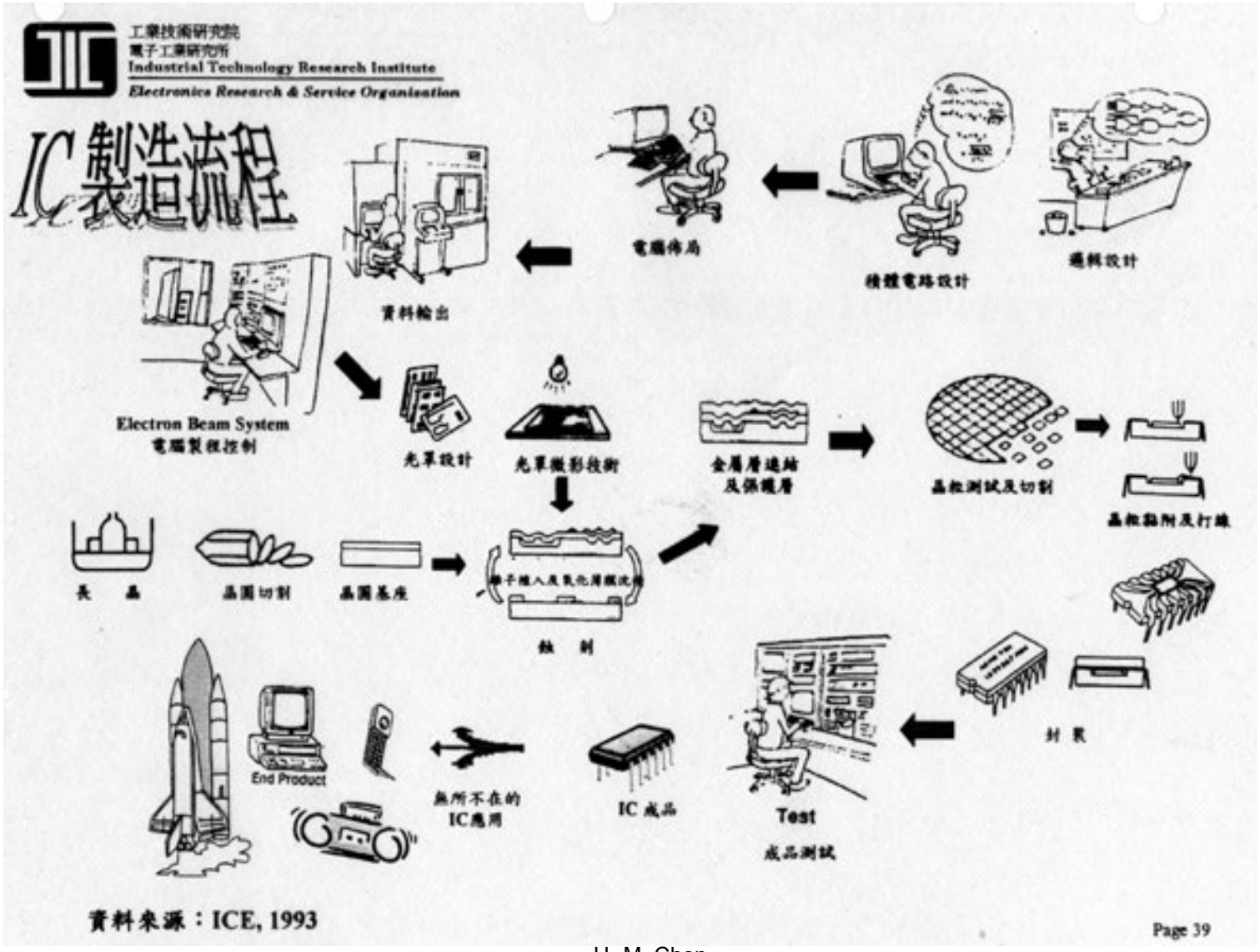
- Course contents:
  - Introduction to VLSI/SoC design flow
  - Introduction to physical design automation
  - Design trends and styles



Outline

- IC design introduction
- Technology roadmap for semiconductors and challenges
- VLSI/SoC design flows
- Introduction to electronic design automation
- Introduction to physical design
- VLSI/SoC design styles

IC Design & Manufacturing Process



From Wafer to Chip

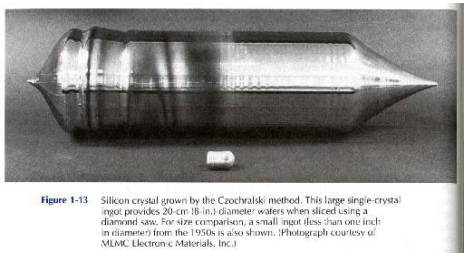
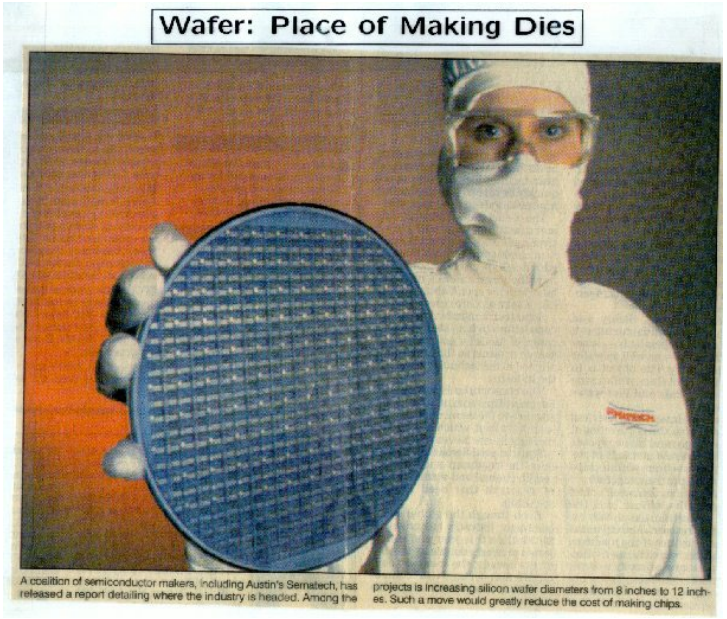


Figure 1-13 Silicon crystal grown by the Czochralski method. This large single-crystal ingot provides 20-cm (8-in.) diameter wafers when sliced using a diamond saw. For size comparison, a small ingot (less than one inch in diameter) from the 1950s is also shown. (Photograph courtesy of MEMC Electronic Materials, Inc.)



A coalition of semiconductor makers, including Austin's Sematech, has released a report detailing where the industry is headed. Among the projects is increasing silicon wafer diameters from 8 inches to 12 inches. Such a move would greatly reduce the cost of making chips.

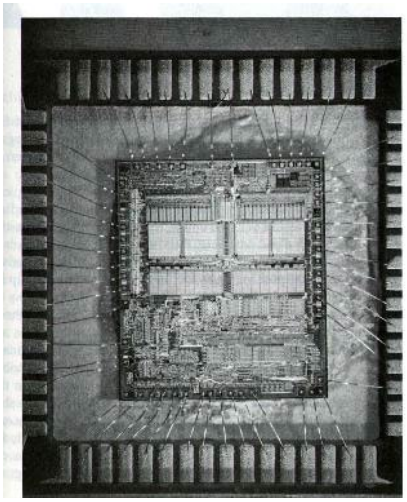
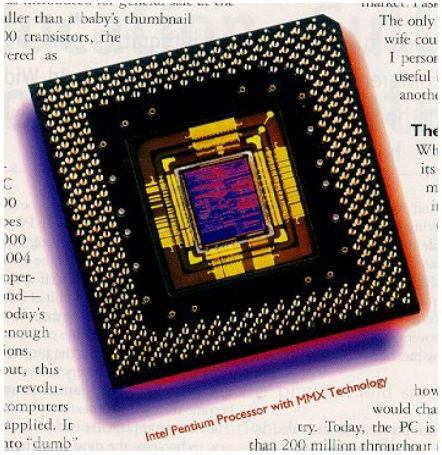


Figure 9-34 Attachment of leads from the Al pads on the periphery of the chip to posts on the package. (Photograph courtesy of Motorola, Inc.)



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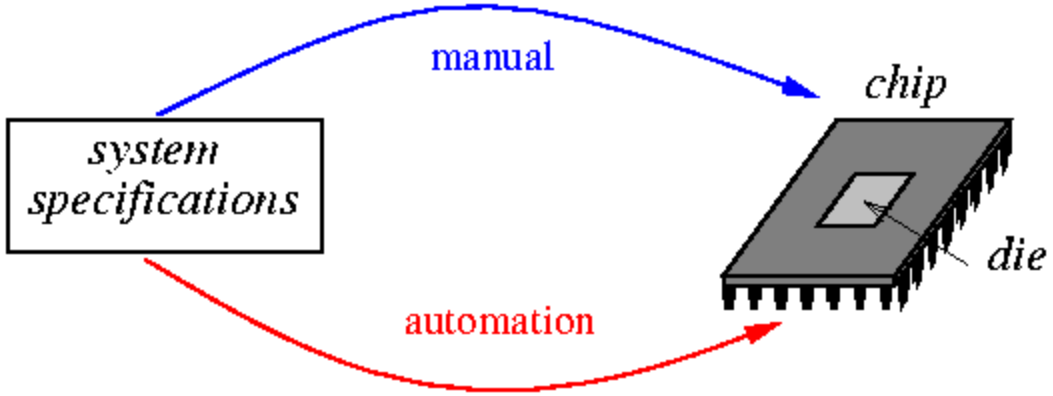
IC Design History

- In 1970's
  - The layout was the design
  - IC design was an ART
  - No simulation, no verification
- In 1980's
  - Technology CMOS 2.0~1.0
  - Design complexity 30K~400K transistors
  - Daisy, DEC (2MB RAM, .5GB HD, 1MIPS)
  - Logic simulation, Verification, CAD layout
  - ASICs
- In 1990's
  - Technology CMOS 1.0~0.18
  - Design complexity 400K~10M gates
  - SUN Sparc, Pentium4 (4GB-16GB, 1 Terabyte HD)
  - Synthesis, P&R
  - ASICs, Processors, Embedded software, FPGA
- In 2000's

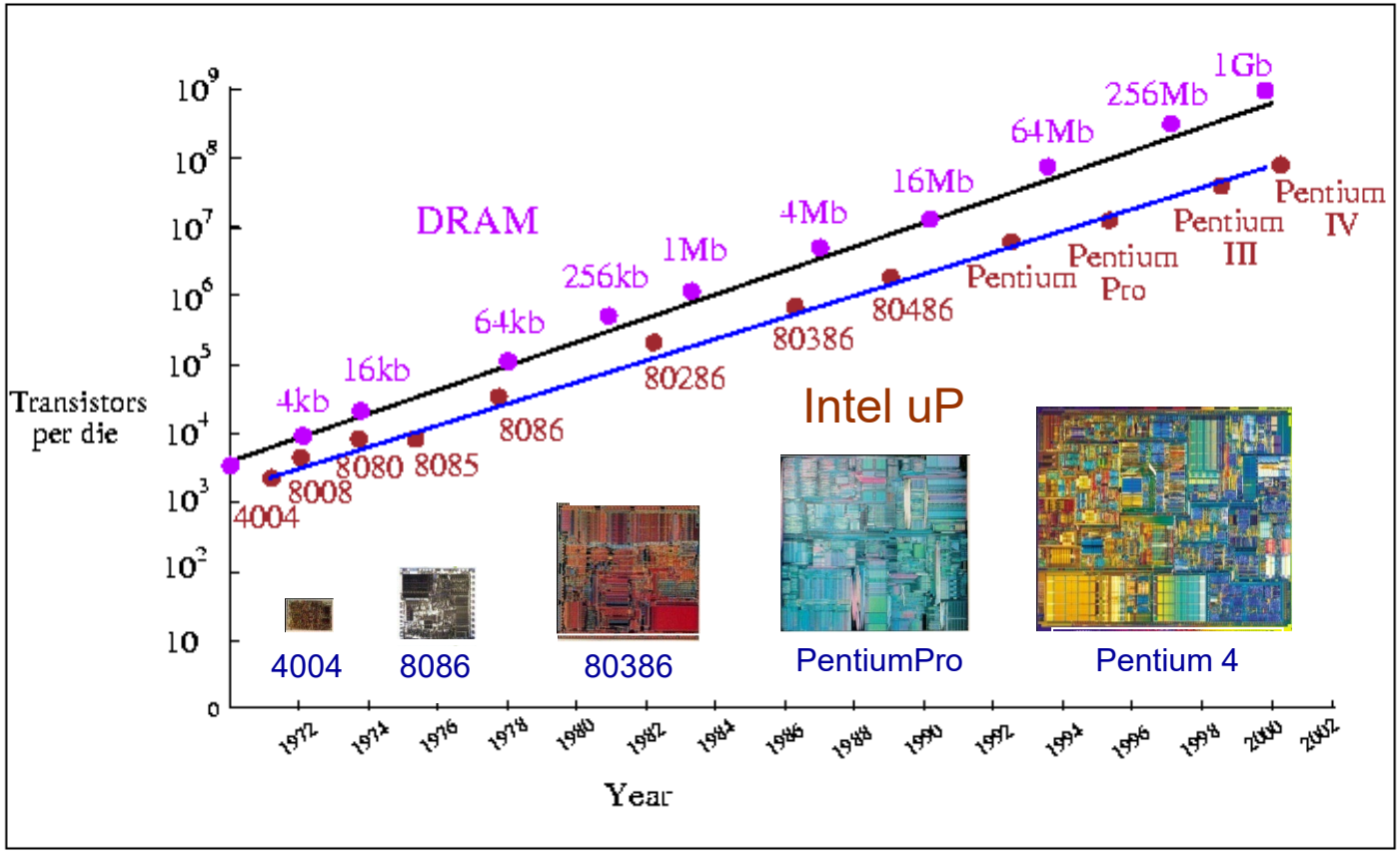
IC Design Considerations



- Several conflicting considerations:
  - **Design Complexity:** large number of devices/transistors
  - **Performance:** optimization requirements for high performance
  - **Time-to-market:** about a 15% gain for early birds
  - **Cost:** die **area**, packaging, testing, etc.
  - Others: power, signal integrity (noise, etc), testability, reliability, manufacturability, etc

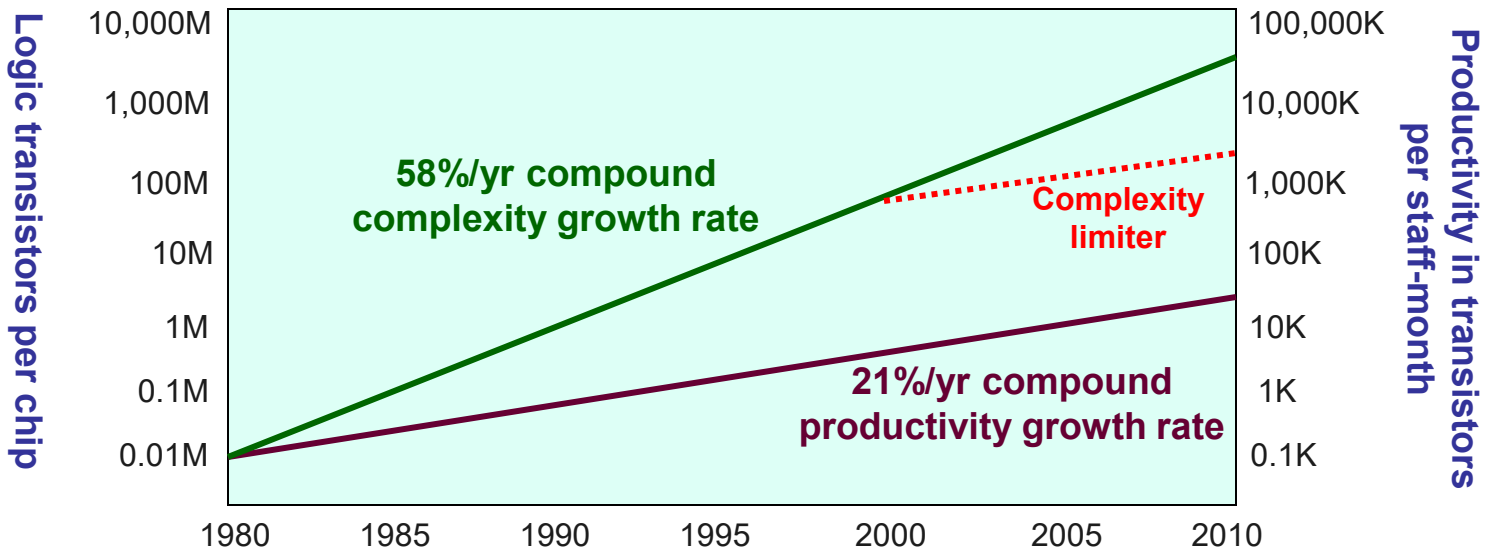
"Moore's" Law: Driving Technology Advances

- Logic capacity doubles per IC at a regular interval.
- Moore: Logic capacity doubles per IC every two years (1975).
- D. House: Computer performance doubles every 18 months (1975)



Most Slides Courtesy of Prof. T. W. Chang and Prof. Y.-L. Li

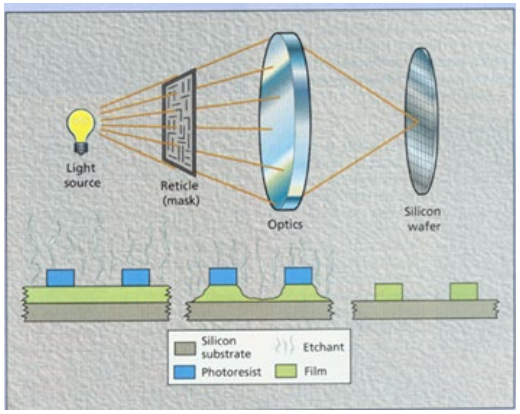
Design Productivity Crisis

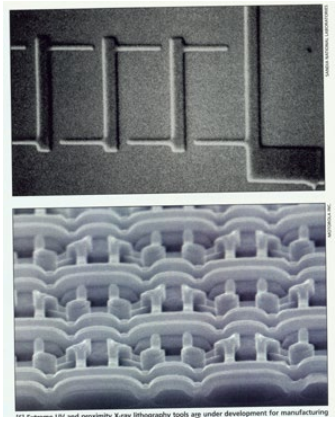


- Human factors may limit design more than technology.
- Keys to solve the productivity crisis: CAD/EDA (tool & methodology), hierarchical design, abstraction, IP reuse, etc.

Nanometer Design Challenges

- In 2005, feature size ≈ 0.1 μm, μP frequency ≈ 3.5 GHz, die size ≈ 520 mm^2, μP transistor count per chip ≈ 200M, wiring level ≈ 8 layers, supply voltage ≈ 1 V, power consumption ≈ 160 W.
  - **Feature size ☐ : sub-wavelength lithography (impacts of process variation)? noise? wire coupling? reliability?**
  - **Frequency ☐, dimension ☐ : interconnect delay? electromagnetic field effects? timing closure?**
  - **Chip complexity ☐ : large-scale system design methodology?**
  - **Supply voltage ☐ : signal integrity (noise, IR drop, etc)?**
  - **Wiring level ☐ : manufacturability? 3D layout?**
  - **Power consumption ☐ : power & thermal issues?**





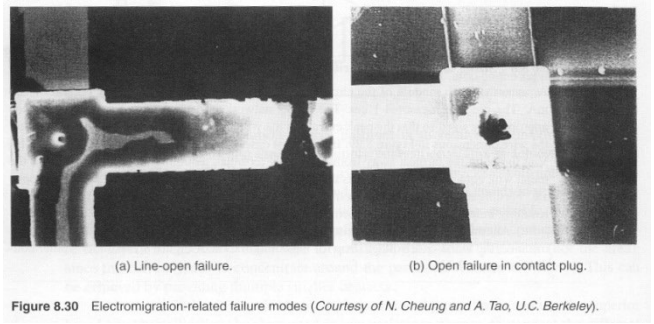
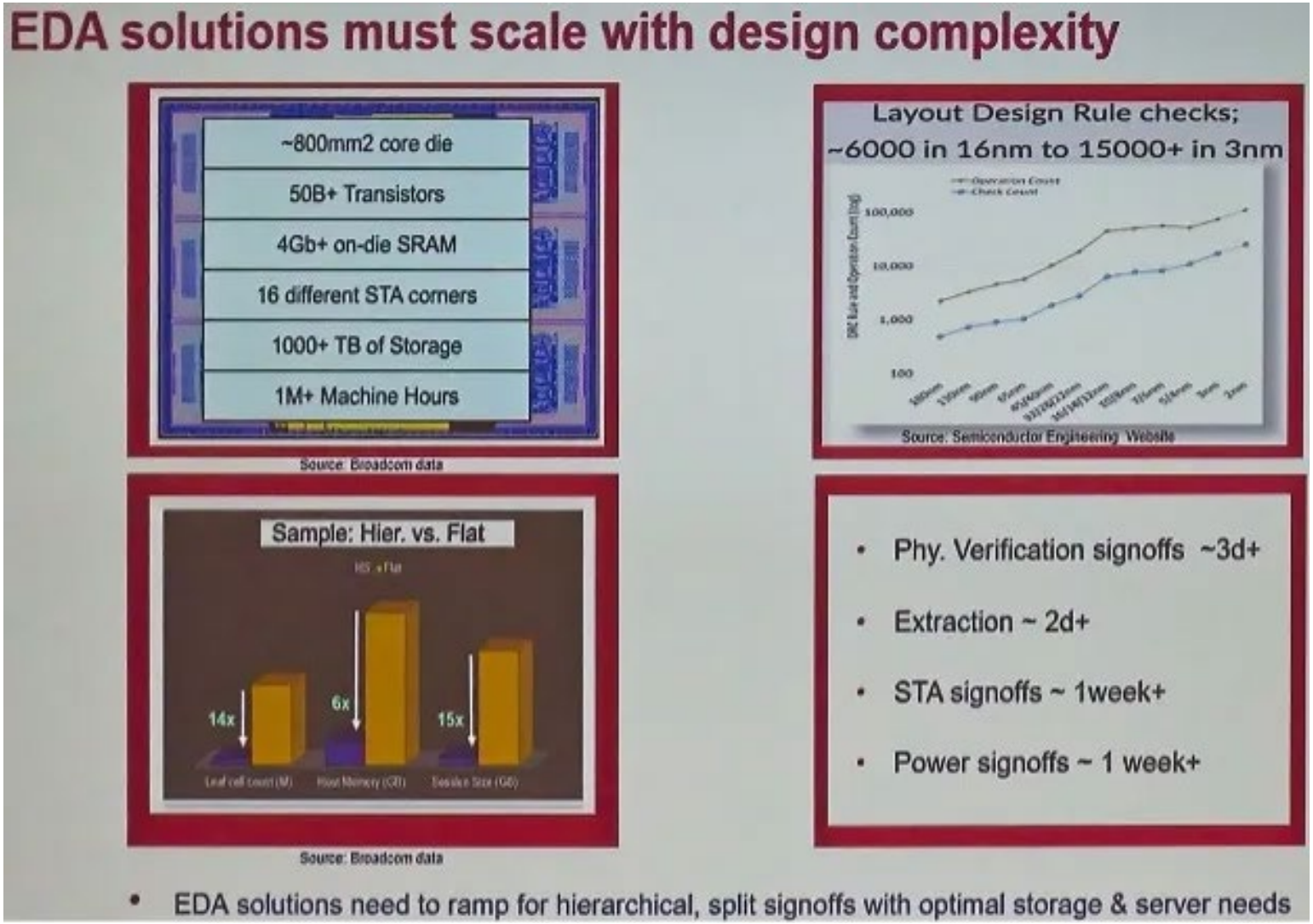


Figure 8.30 Electromigration-related failure modes (*Courtesy of N. Cheung and A. Tao, U.C. Berkeley*).

Most Slides Courtesy of Prof. Y.-W. Chang and Prof. Y.-L. Li

Design Complexity and EDA



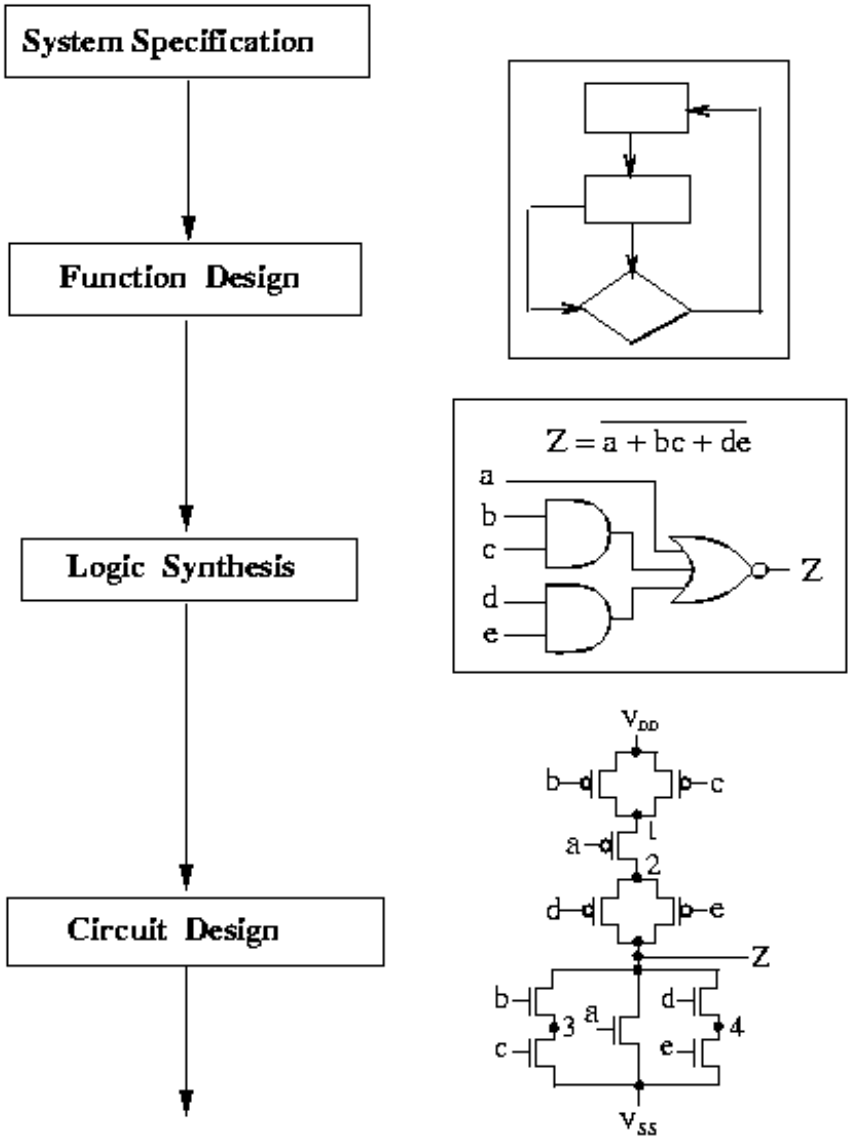
Source: Broadcom and Internet

Traditional VLSI Design Cycles

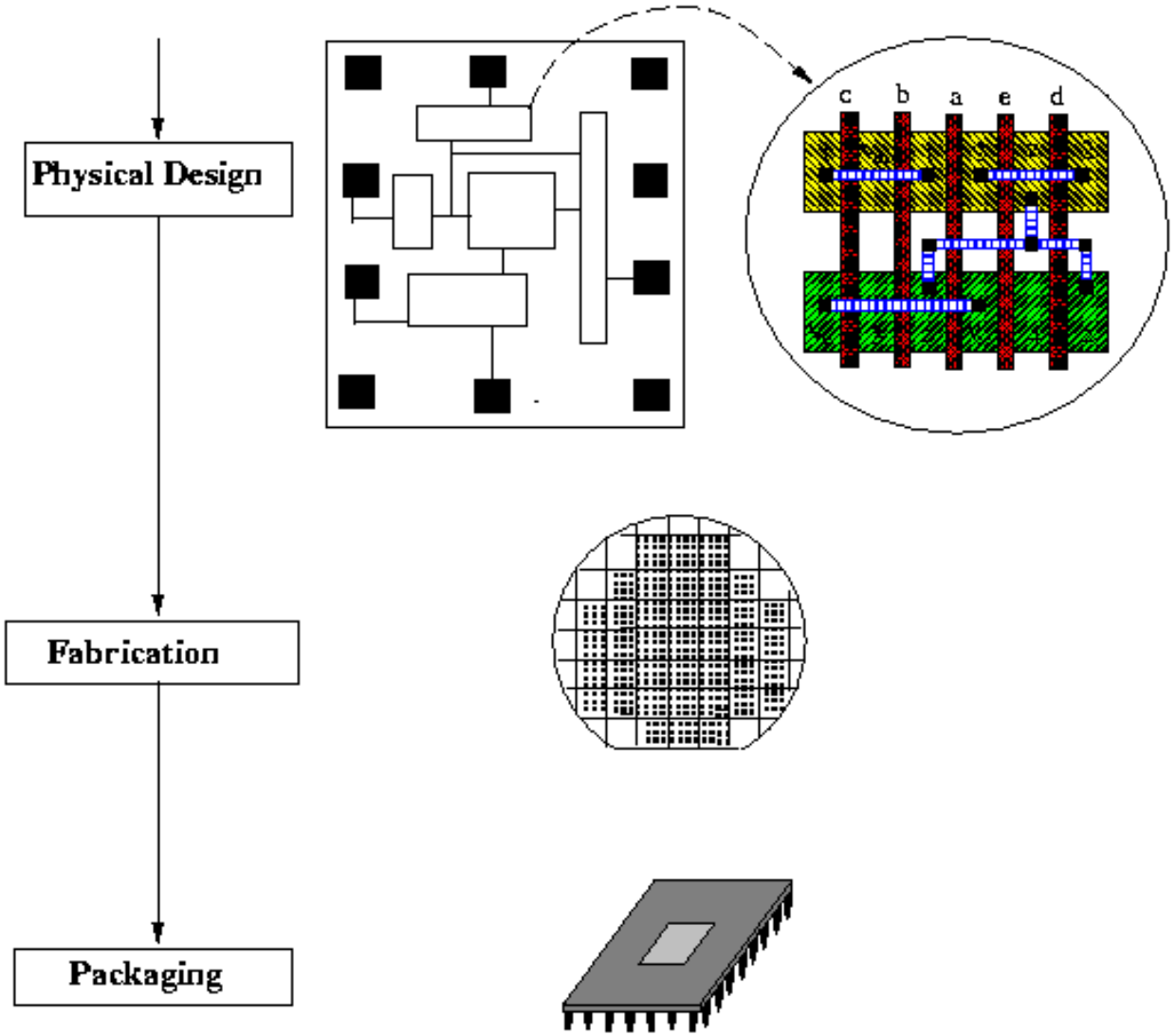
1. System specification
2. Functional design
3. Logic synthesis
4. Circuit design
5. **Physical design and verification**
6. Fabrication
7. Packaging

- Other tasks involved: testing, simulation, etc.
- Design metrics: area, speed, power dissipation, noise, design time, testability, etc.
- Design revolution: interconnect (not gate) delay dominates circuit performance in deep submicron era.
  - Interconnects are determined in physical design.
  - Shall consider interconnections in early design stages.

Traditional VLSI Design Flow

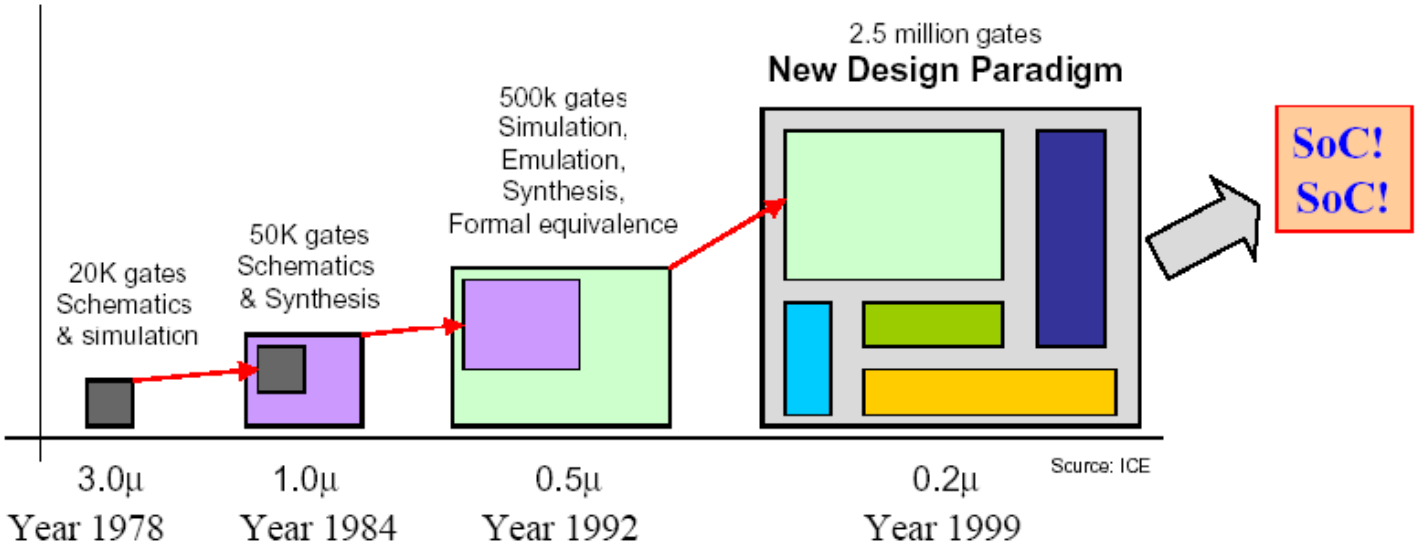


Traditional VLSI Design Flow (Cont'd)

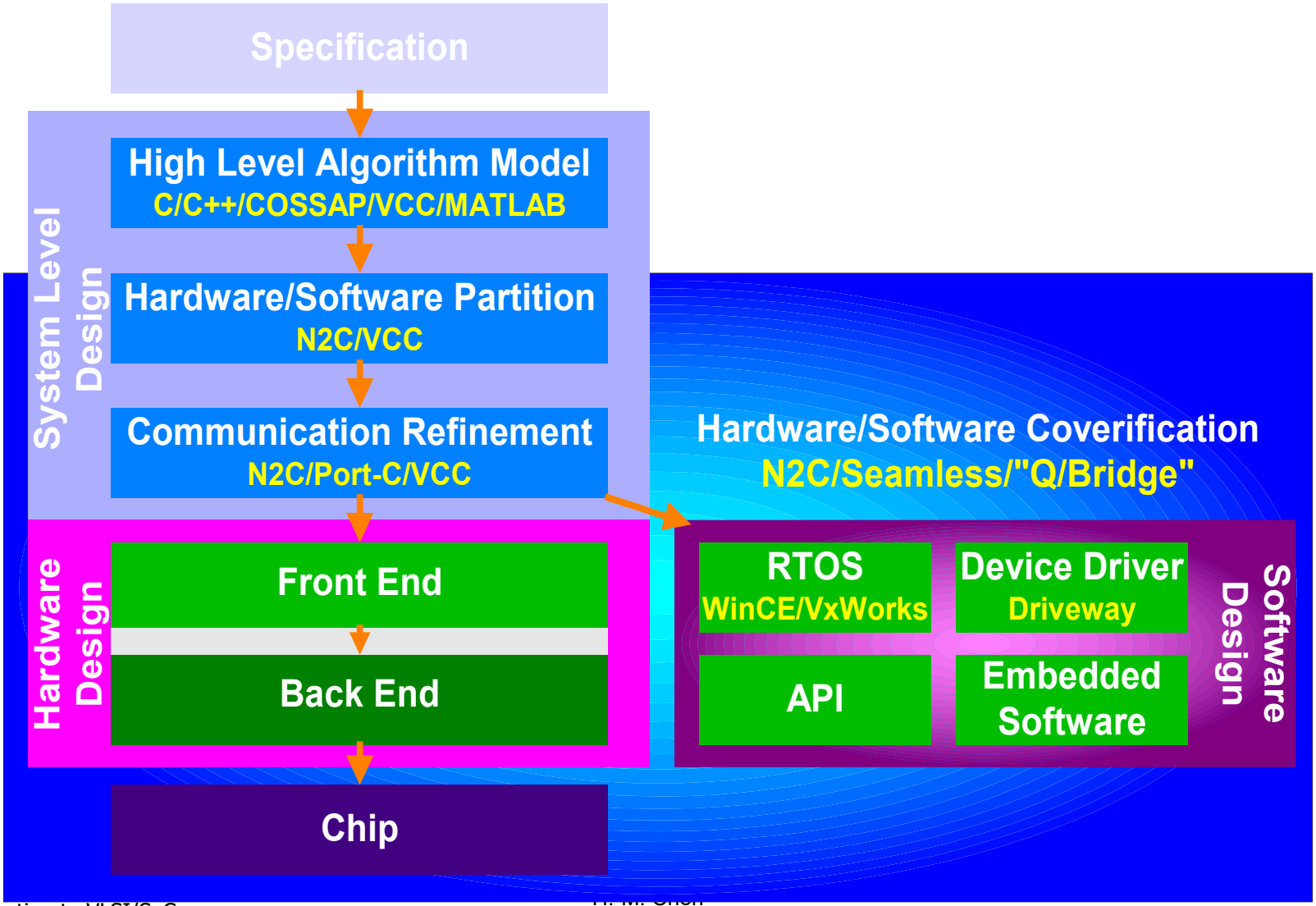


Evolution of Microelectronics

- Today's Silicon process technology
  - 0.13μm CMOS
  - ~100 M of devices, 3GHz internal clock
- Yesterday's chips are today's function blocks



System-on-a-Chip Design Flow



Electronic Design Automation (EDA)

- Due to high complexity of chip design and verification
- Objectives of VLSI CAD/EDA are to minimize/reduce:
  - The time of iteration
  - Total number of iterations
  - Time to market
- EDA provides three primary services — productivity, optimization, and assurance
- Includes ESL, front-end, back-end, and testing

Major Classes of EDA Tools

- Electronic system level (ESL) design
  - Specify and capture design tools
  - Verify, model, simulate tools
- IC front-end (FE) design
  - Design capture, verification, and synthesis tools
- IC back-end (BE) design
  - General layout of the chip (floorplanning)
  - Detailed placement, routing tools
  - Check electrical and physical design rules
  - Output of back-end design flow: **tapeout**

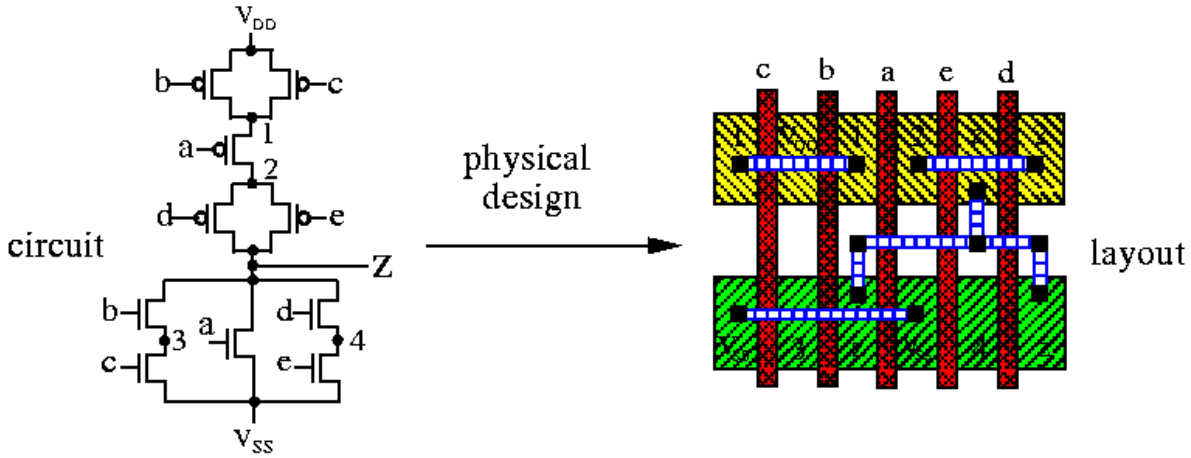
Existing EDA Tools Chronicles (1/2)

Year	Design Tools	Company
1950 ~ 1960	Manual design	
1965 ~ 1975	Layout editors Automatic routers (for PCB) Efficient partitioning algorithm	
1975 ~ 1985	Automatic placement tools Well defined phase of design of circuits Significant theoretical development in all phases	Applicon Calma Computervision
1985 ~ 1990	Performance driven placement and routing tools Parallel algorithms for physical design Significant development in underlying graph theory Combinatorial optimization problems for layouts	Daisy Mentor Valid

Existing EDA Tools Chronicles (2/2)

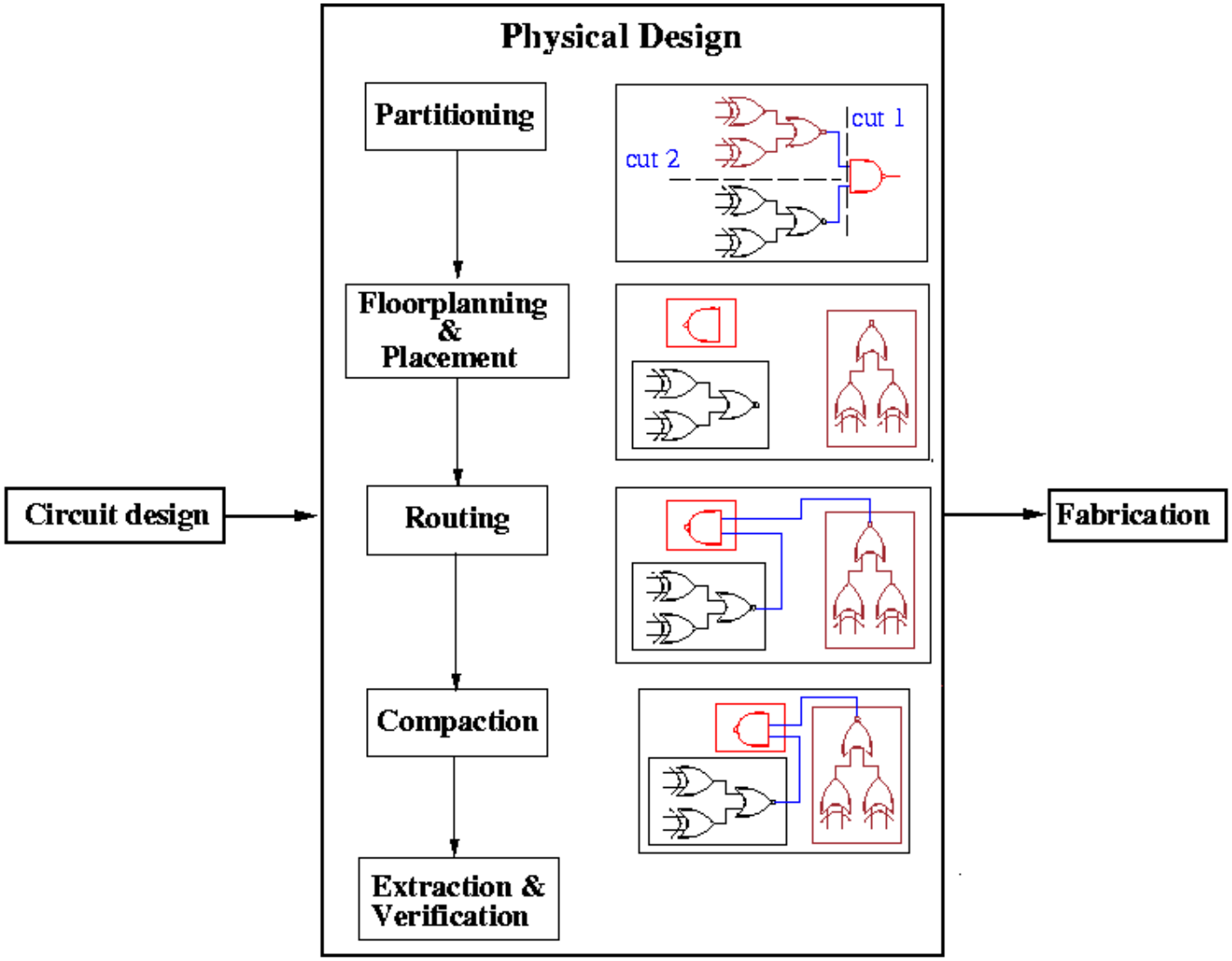
Year	Design Tools	Company
1990 ~ 1995	Over-the-Cell Routing tools Three dimensional interconnect based physical design Synthesis tools mature and gain widespread acceptance	Avanti(Synopsys) Cadence Synopsys
1995 ~ Present	Interconnect design and Modeling dominates physical design Process related tools (reliability, electro-migration)	Magma (Synopsys) Monterey Verplex (Cadence) SPC(Cadence) Numerical (Synopsys) Springsoft (Synopsys) EverCAD (Mentor)

Physical Design

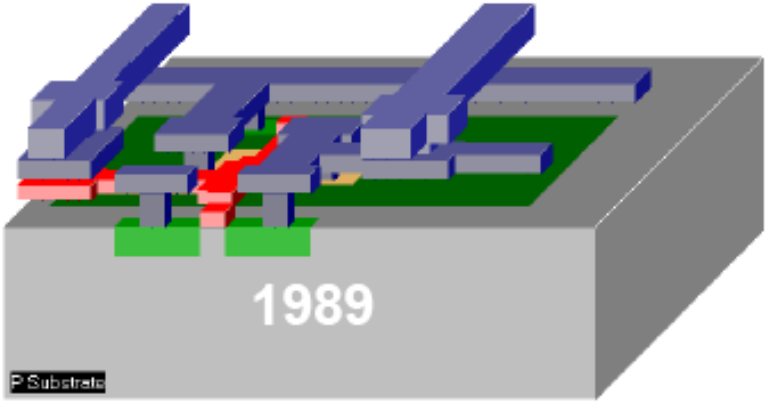


- Physical design converts a circuit description into a geometric description.
- The description is used to manufacture a chip.
- Physical design cycle:
  1. Logic partitioning
  2. Floorplanning and placement
  3. Routing
  4. Post-layout optimization
- Others: circuit extraction, timing verification and design rule checking

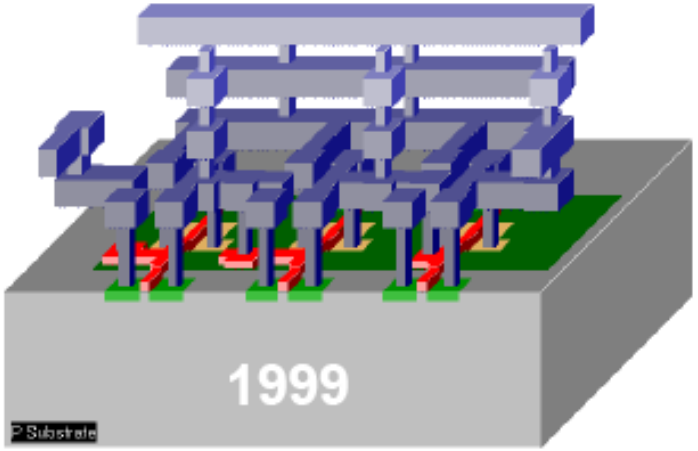
Physical Design Flow



Changes in Real IC



0.8µm CMOS



0.18µm CMOS

Technology:	0.8µm	0.18µm	0.07µm
# of Metal layers:	2~3	6	8-9
G.W. Aspect ratio (t/w):	~0.8	~1.8	~2.7
Wire length(m/chip):	~130	~1,480	~10,000

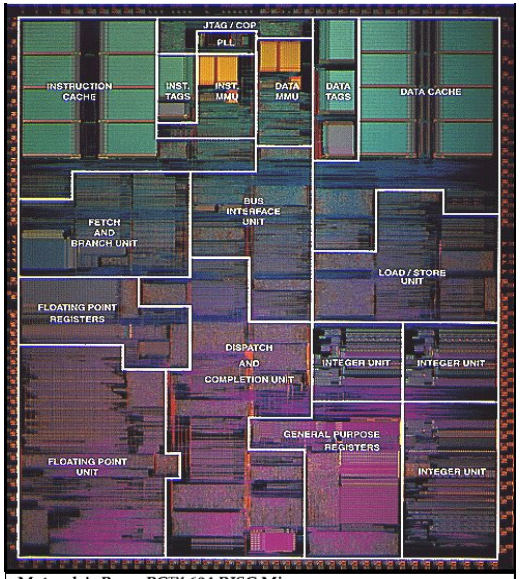
Interconnects Start to Dominates Cost and Performance

Interconnect starts to be main design constraints

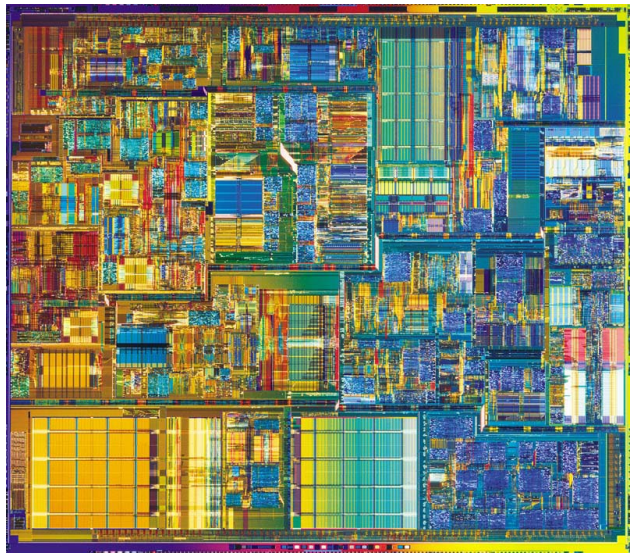
Source: L.-R. Zheng, KTH

Floorplan Examples

PowerPC 604

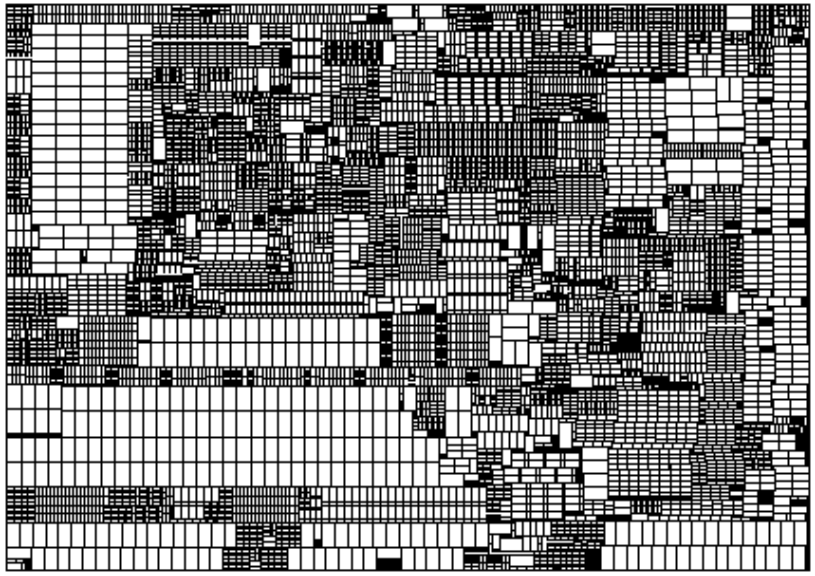


Motorola's PowerPC™ 604 RISC Microprocessor



Pentium 4

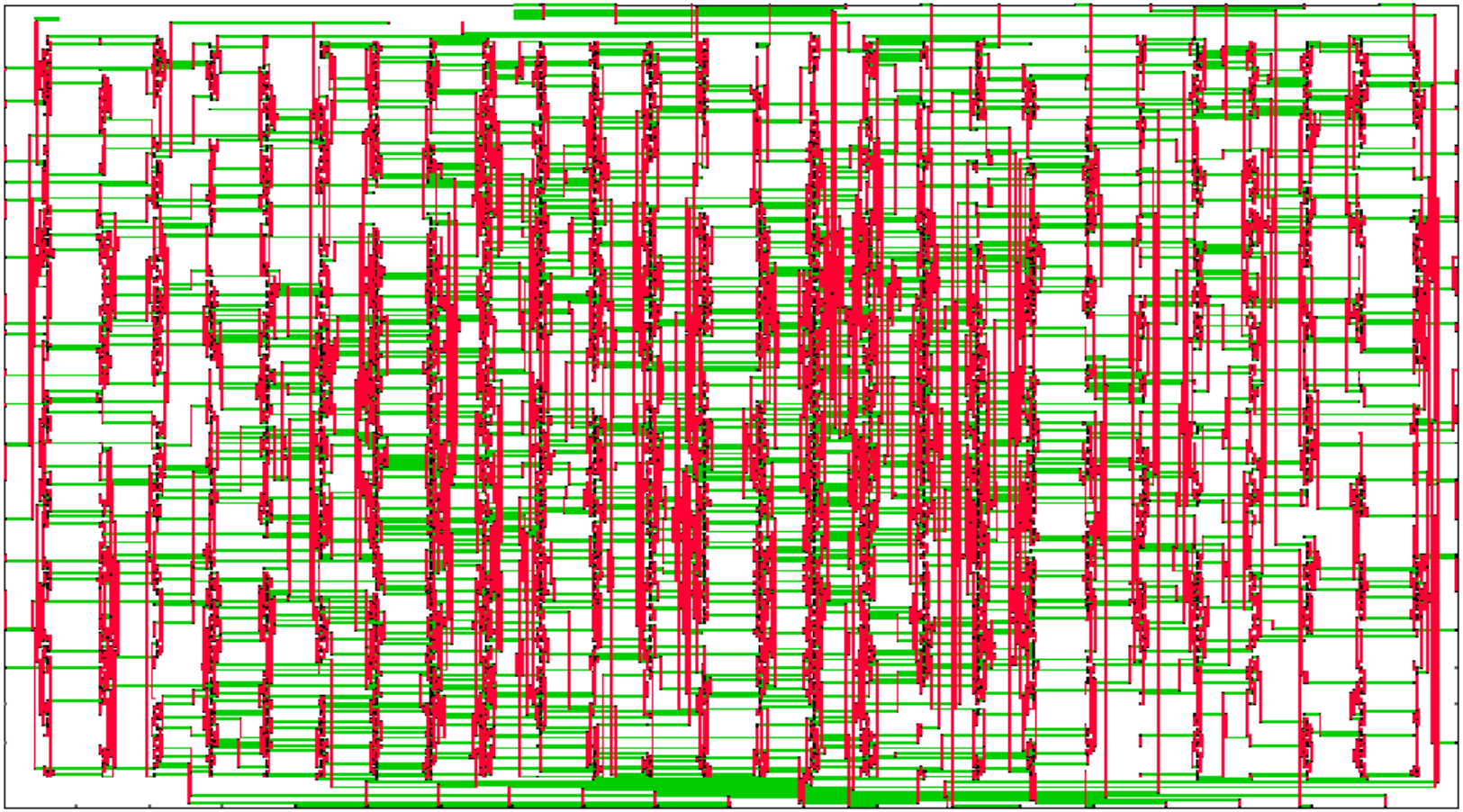
A floorplan with 9800 blocks



Most Slides Courtesy of Prof. Y.-W. Chang and Prof. Y.-L. Li

Routing Example

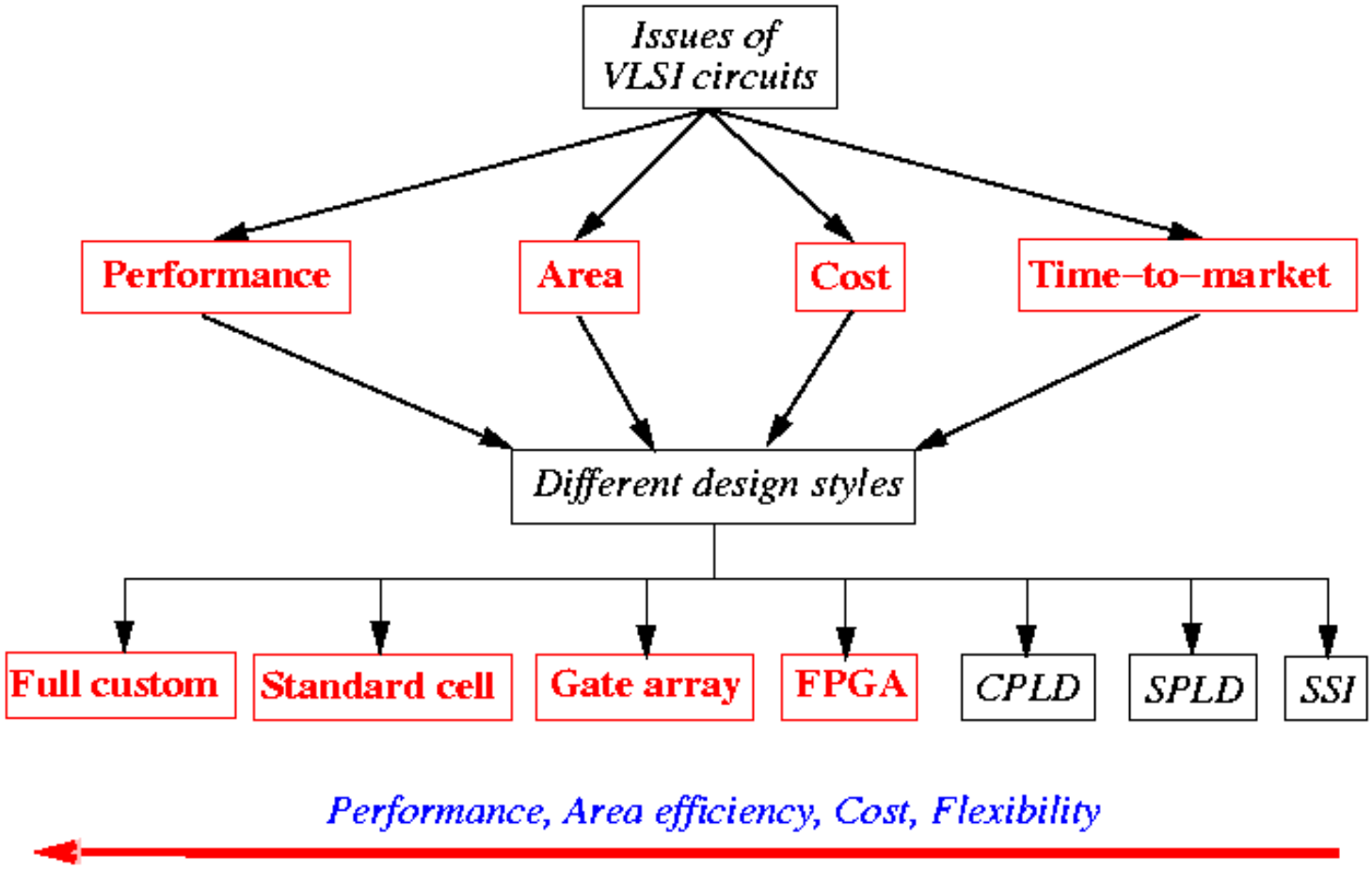
- 0.18um technology, pitch = 1 um, 2774 nets.



Why Learning Physical Design?

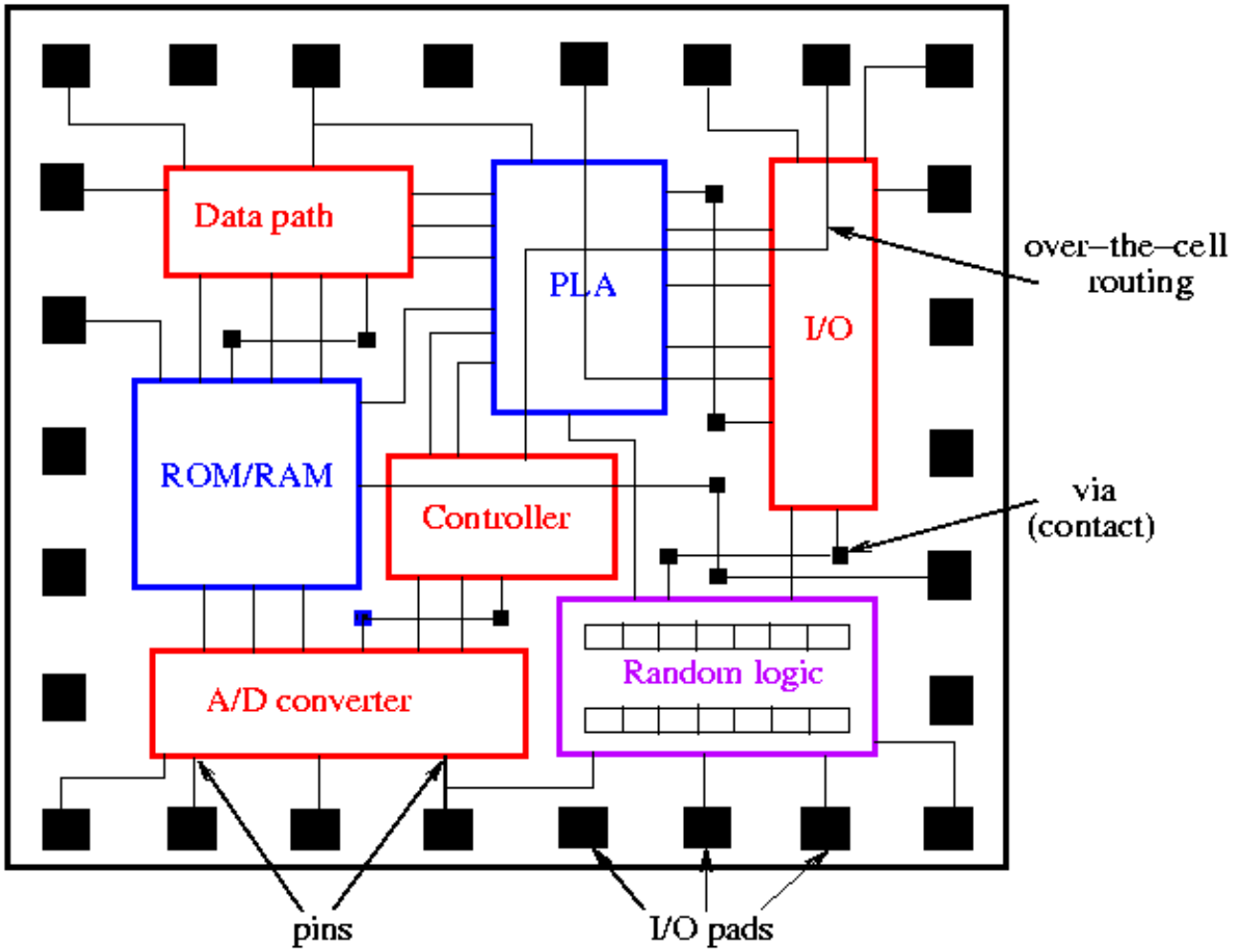
- DSM effects make physical design very hard to come around
- CAD problems are seldom touched in Taiwan, people always want to do IC design
- Learning CAD actually will enhance your design capability
- Front end tools are getting mature, back end tools are not, due to technology advancement
- Knowing more algorithmic concepts, not just using them
- Many more…

Design Styles



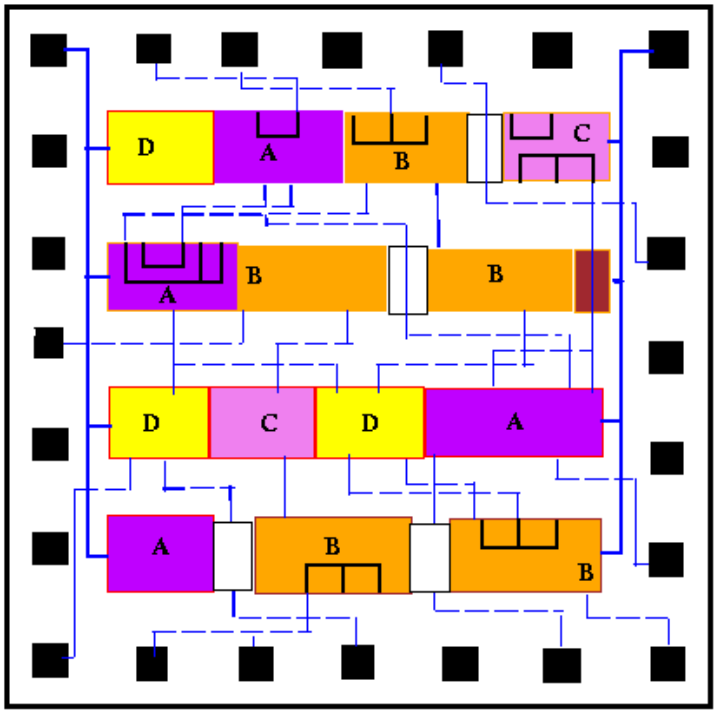
Full Custom Design Style

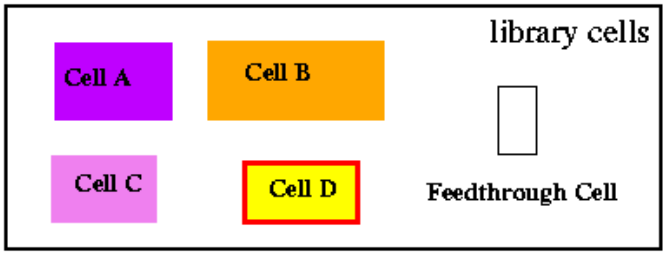
- Design every component from scratch



Standard Cell Design Style

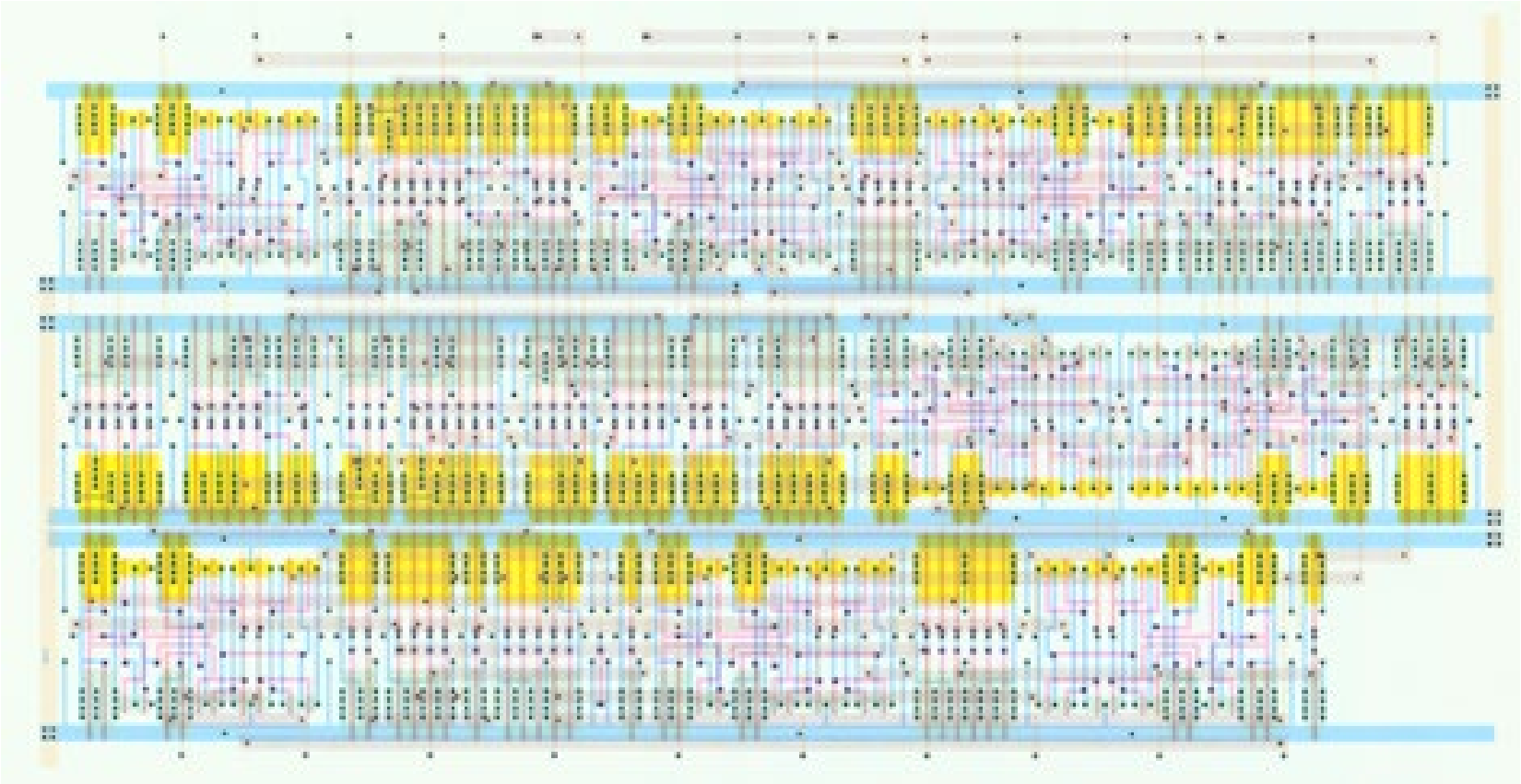
- Selects pre-designed cells (of same height) to implement logic





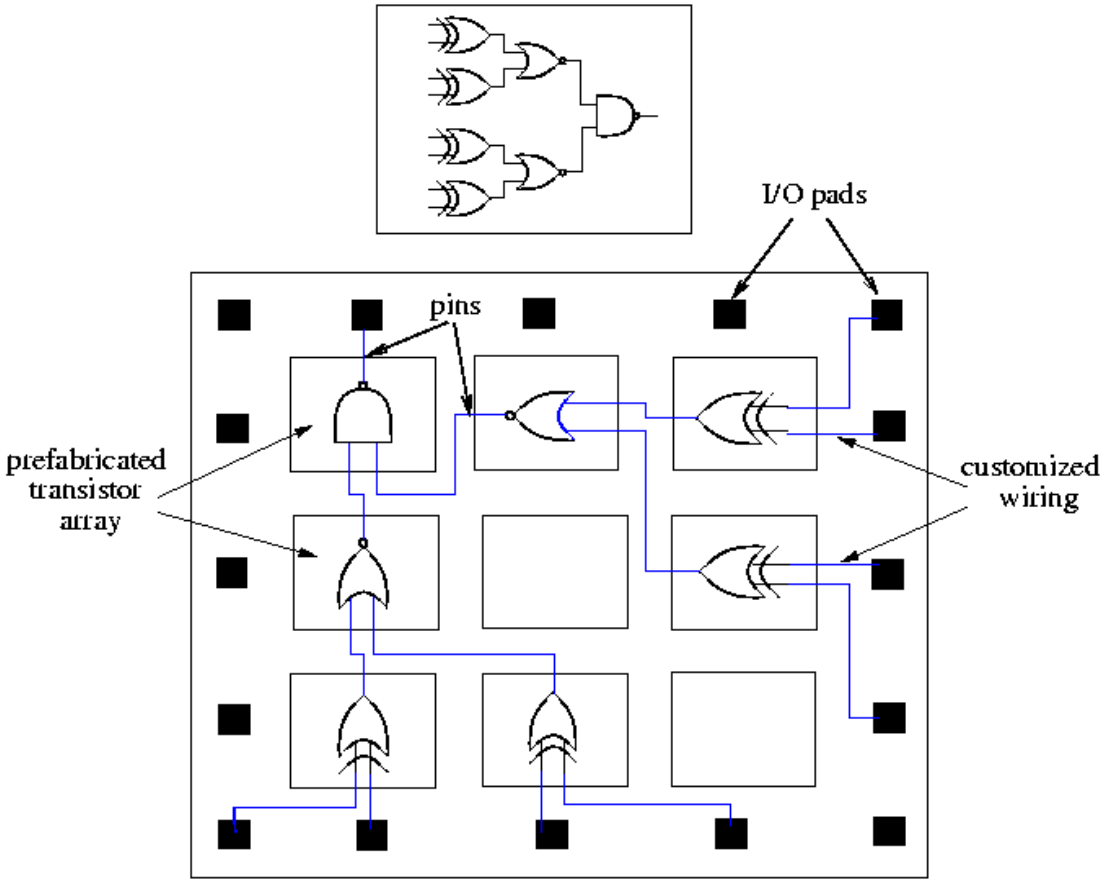
Most Slides Courtesy of Prof. Y.-W. Chang and Prof. Y.-L. Li

Standard Cell Example



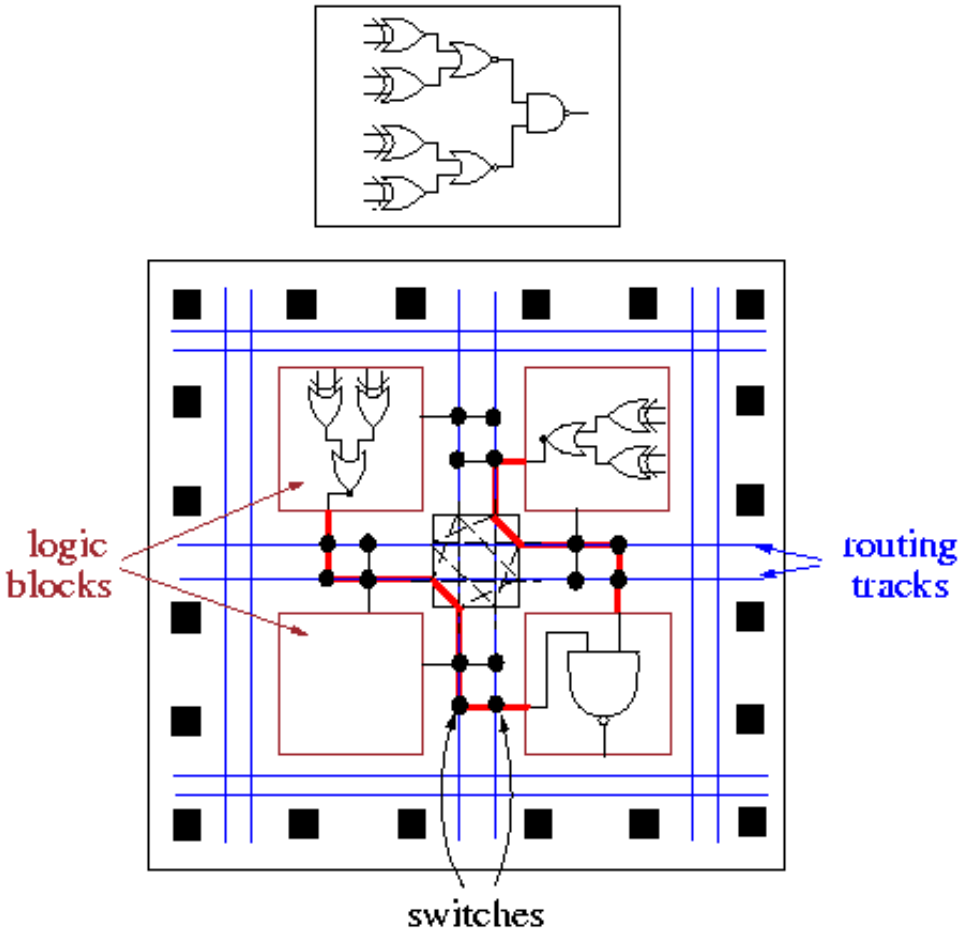
Gate Array Design Style

- Prefabricates a transistor array
- Needs wiring customization to implement logic



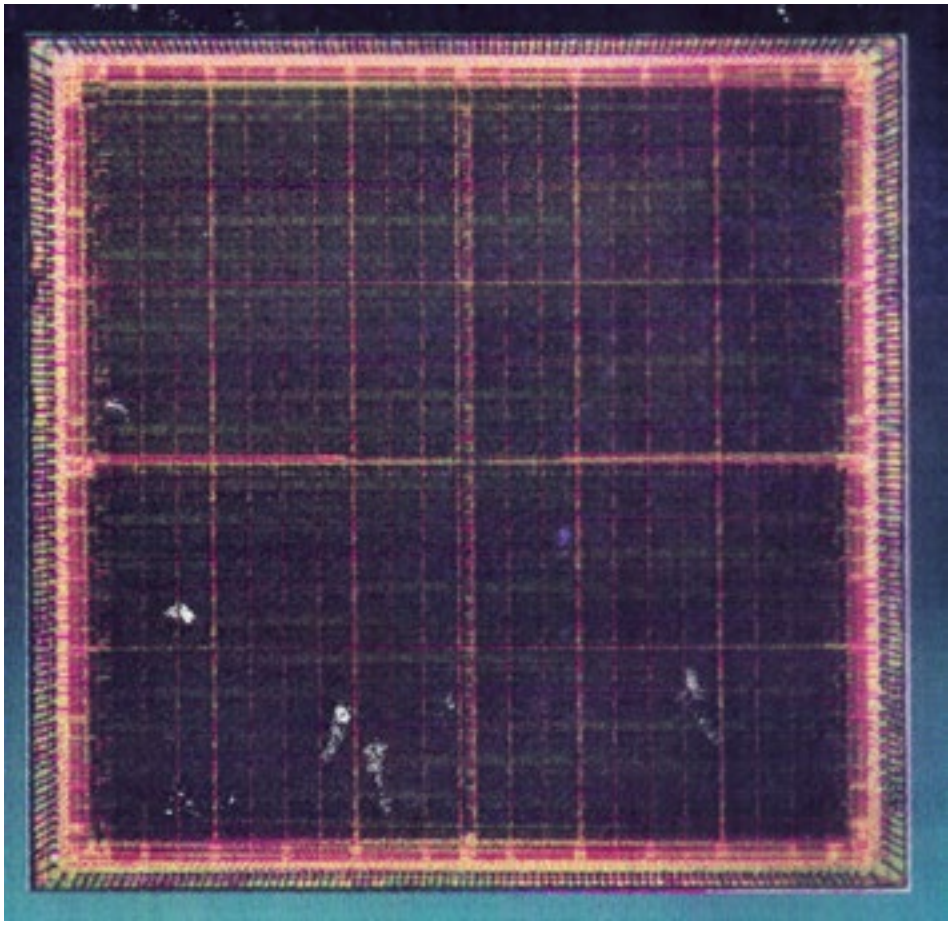
FPGA Design Style

- Logic and interconnects are both prefabricated.
- Illustrated by a symmetric array-based FPGA



Array-Based FPGA Example

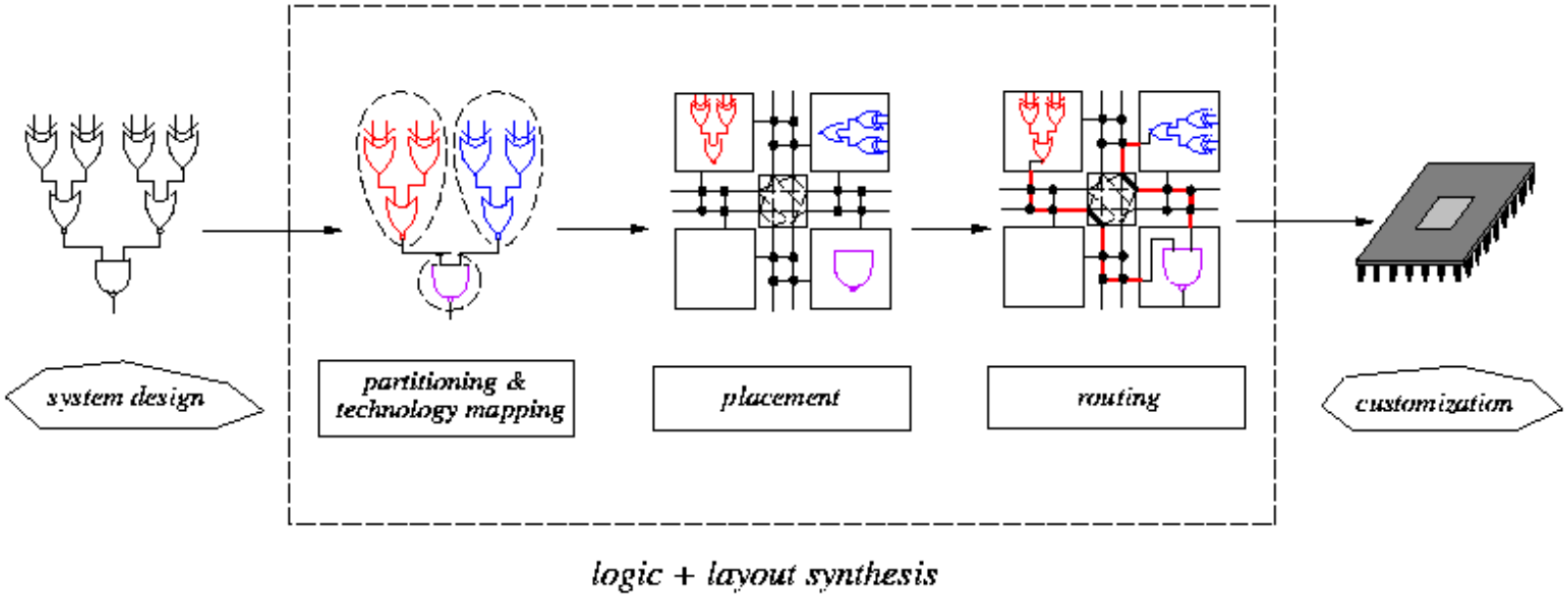
- Lucent Technologies 15K ORCA FPGA



- 0.5 um 3LM CMOS
- 2.45 M Transistors
- 1600 Flip-flops
- 25K bit user RAM
- 320 I/Os

FPGA Design Process

- Illustrated by a symmetric array-based FPGA
- No fabrication is needed



Design Styles

	Style			
	Full-custom	Standard cell	Gate array	FPGA
Cell size	Variable	Fixed height	Fixed	Fixed
Cell type	Variable	Variable	Fixed	Programmable
Cell placement	Variable	In row	Fixed	Fixed
Interconnections	Variable	Variable	Variable	Programmable
Design cost	High	Medium	Medium	Low

Design Styles (cont)

	Style			
	Full-custom	Standard cell	Gate array	FPGA
Area	Compact	Compact to moderate	Moderate	Large
Performance	High	High to moderate	Moderate	Low
Fabricate	All layers	All layers	Routing layers only	No layers