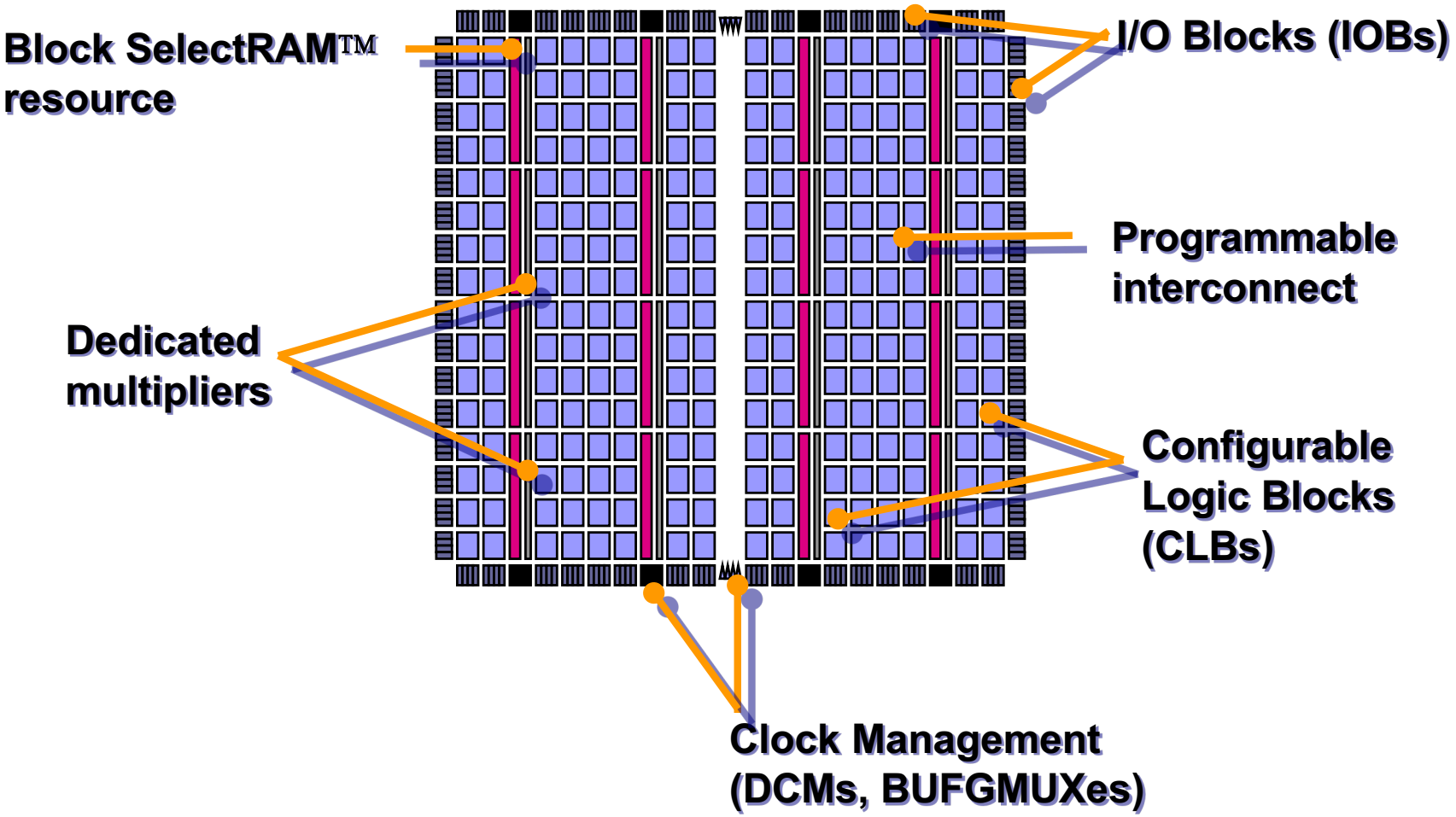
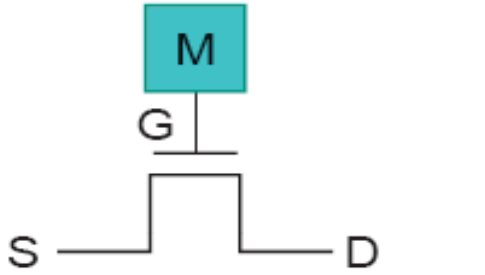
Commercial Examples (Part 1): Xilinx SRAM-based FPGAs

Xilinx FPGA

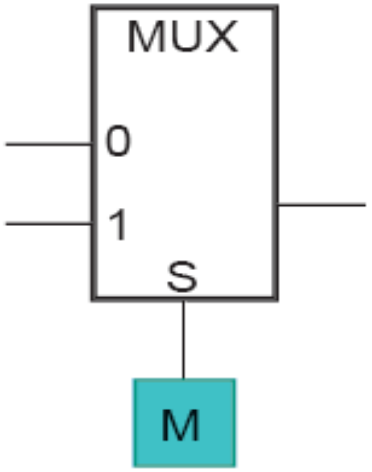
- A basic SRAM-based FPGA (Spartan-3)



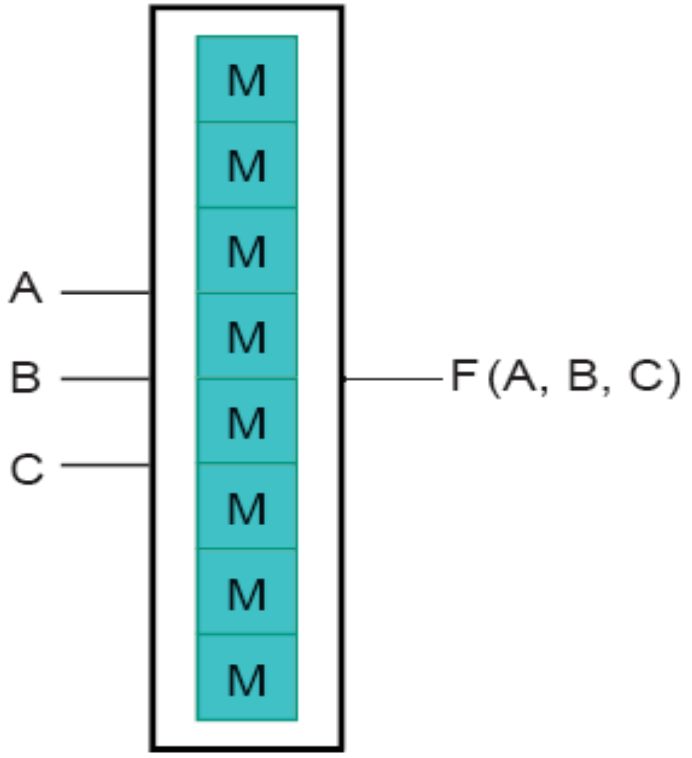
SRAM Usage



(a) Pass transistor control



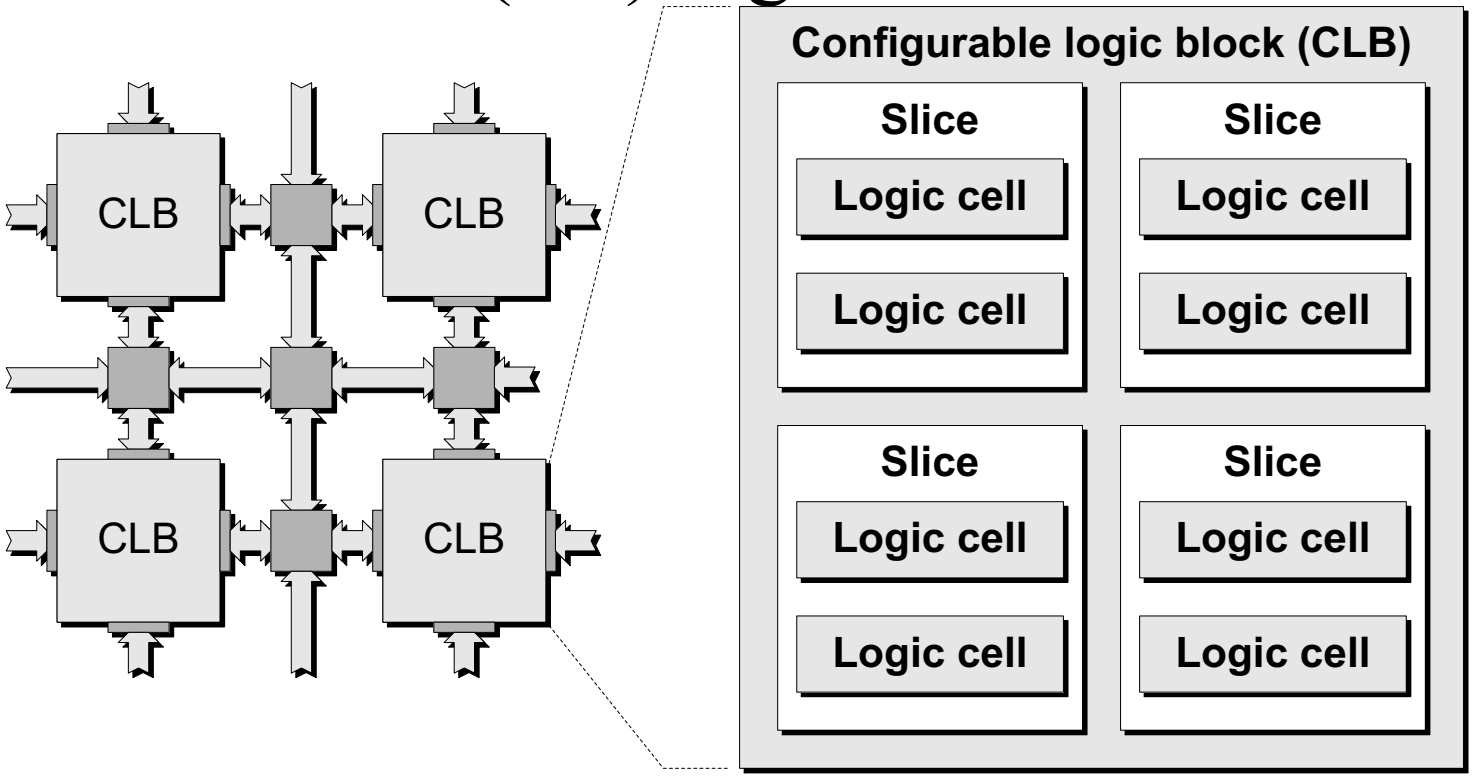
(b) Multiplexer control



(c) Look up table implementation

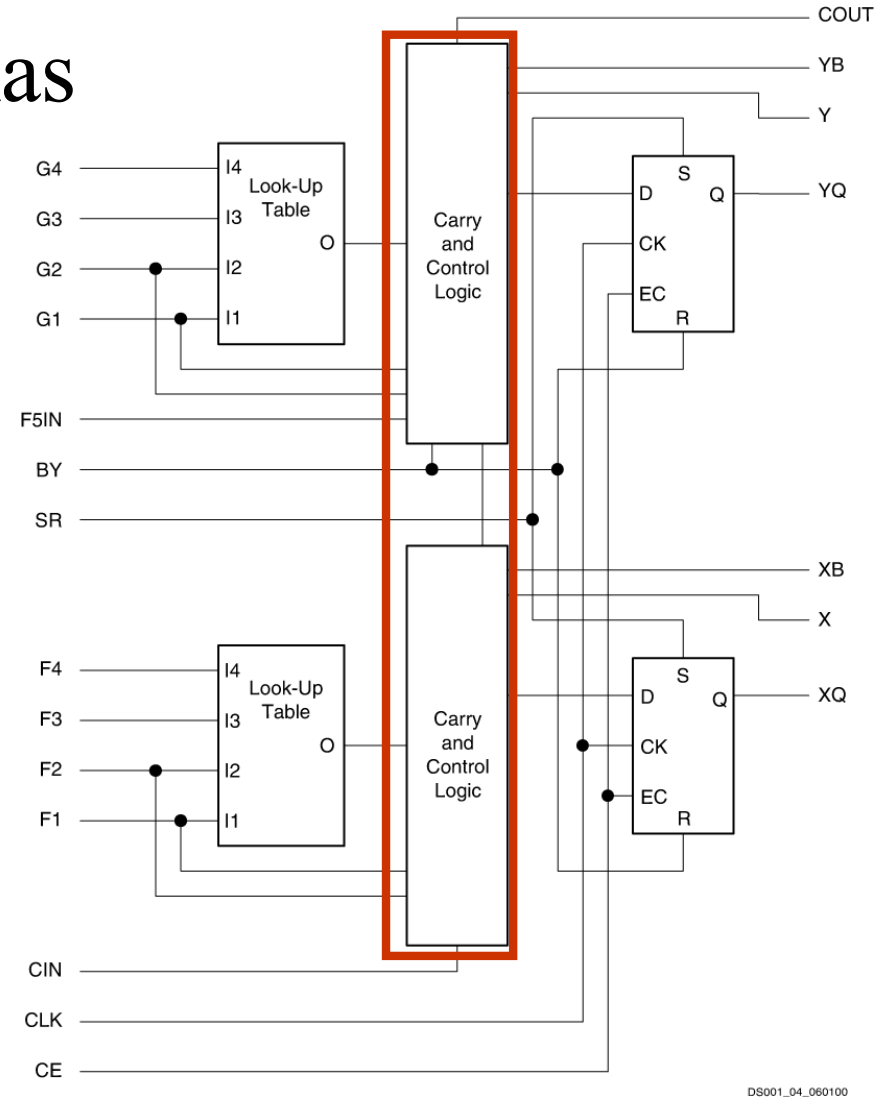
Xilinx's CLBs

- A configurable logic block (CLB) contains a few (2/4) slices.
- Each slice has a few (2/4) logic cells.



Slice Structure (Simplified View)

- E.g. A slice in Spartan-3 has
  - two 4-input LUTs
  - two carry and control logic blocks
  - two storage elements
- Carry logic runs up vertically

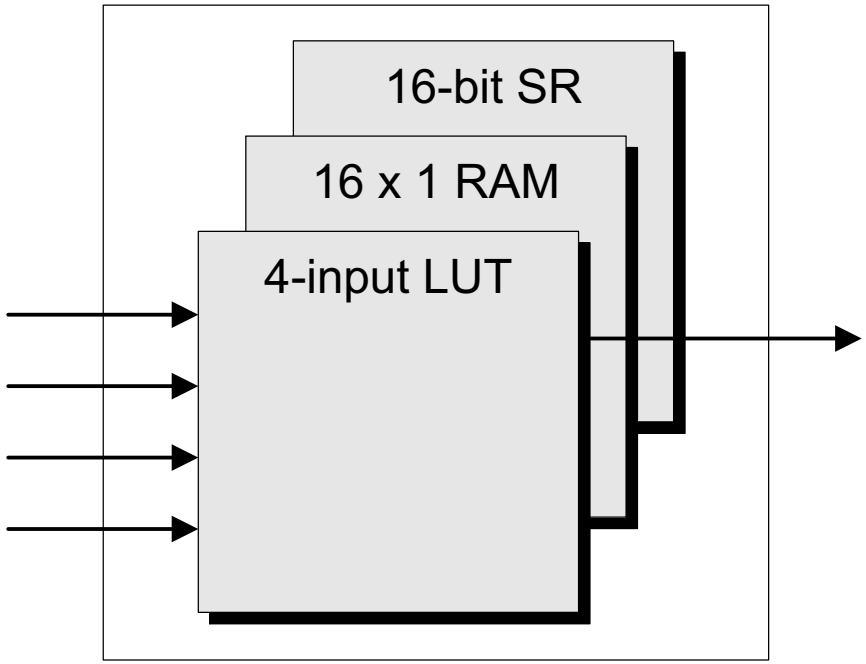


CLB Details

- Multiple roles of LUT
  - function generator/synchronous RAM/shift register
- Dedicated carry logic
  - perform fast arithmetic functions
- MUXes
  - can combine results of 2 function generators
- Storage elements
  - can be configured as DFF or latch
- CLB outputs
  - three-state drivers (BUFTs) are provided before routing

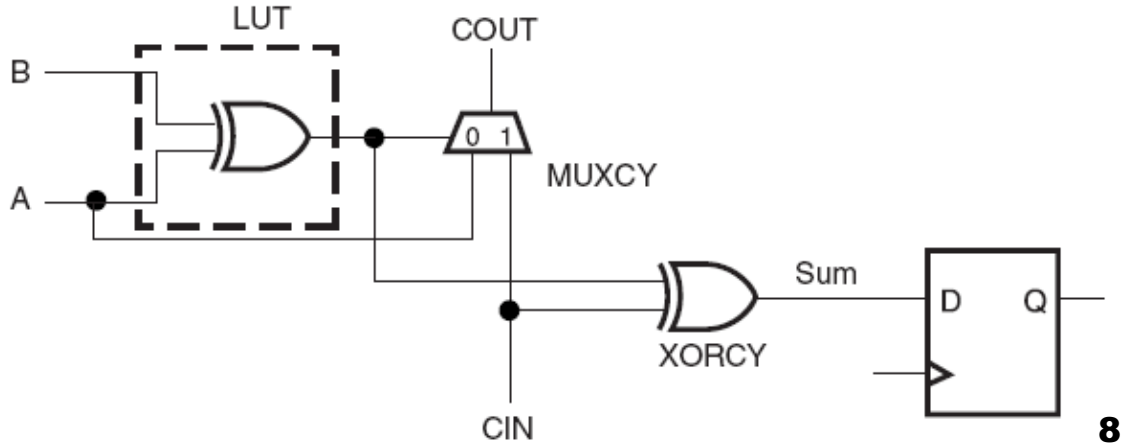
Multipurpose LUT

- E.g. A 4-LUT can be used as
  - a function generator
  - 16-bit synchronous RAM
  - 16-bit shift register



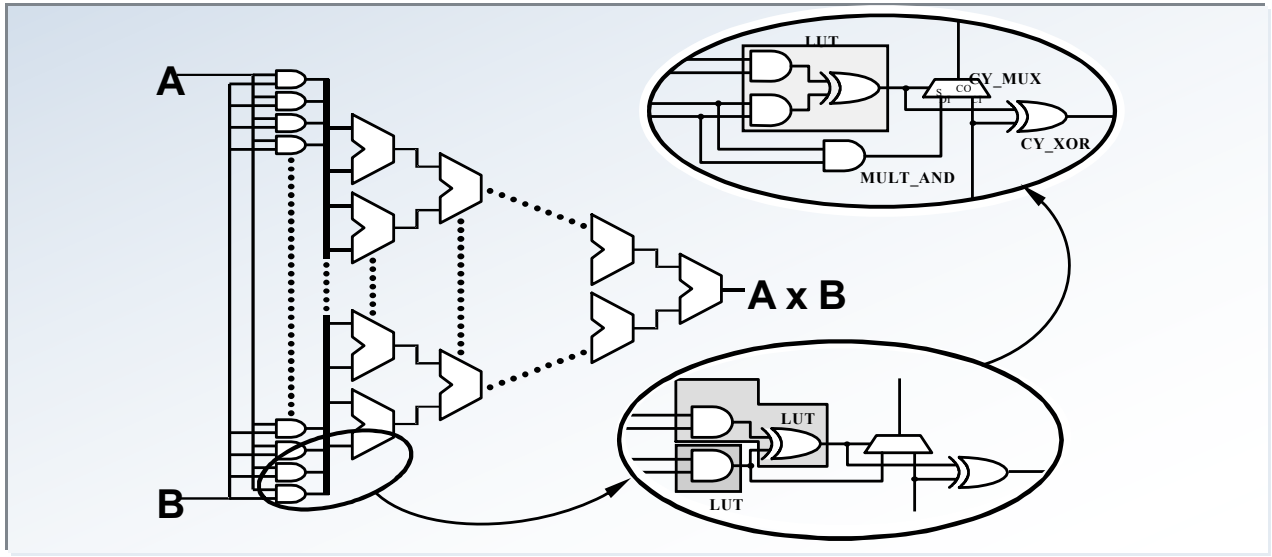
Carry and Arithmetic Logic

- Automatically used for most arithmetic functions in a design
- Include dedicated XOR gates and AND gates to implement efficient arithmetic functions together with the LUTs
- E.g. Addition



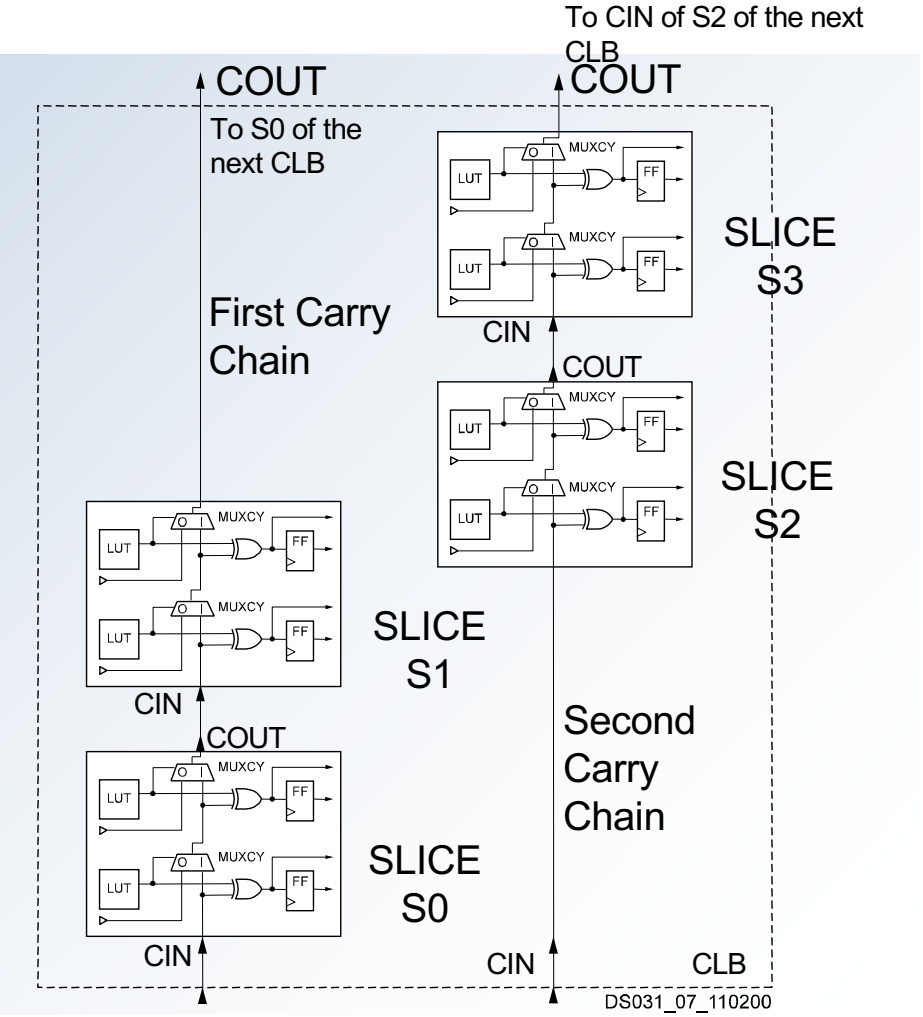
Carry and Arithmetic Logic

- Efficient multiply and add implementation
  - Earlier FPGA architectures require two LUTs per bit to perform the multiplication and addition
  - The MULT_AND gate enables an area reduction by performing the *multiply* and the *add* in one LUT per bit



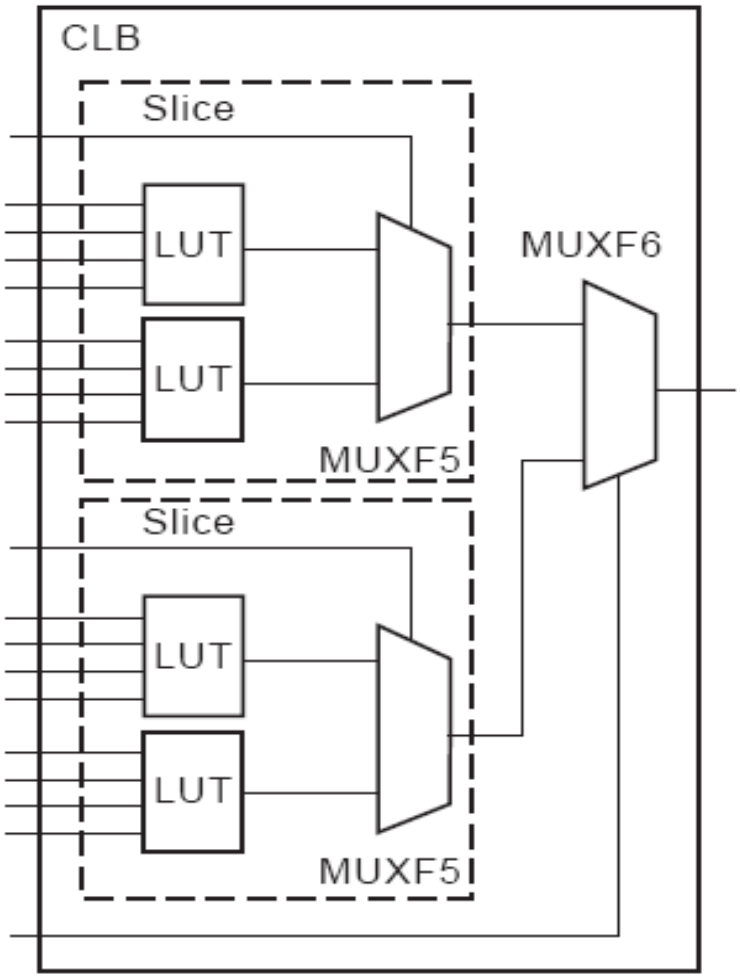
Fast Carry Logic

- Fast and complete arithmetic logic
  - Dedicated XOR gate for single-level sum completion
  - Uses dedicated routing resources
  - All synthesis tools can infer carry logic
  - Increases efficiency of arithmetic computation



MUXes in CLB connecting LUTs

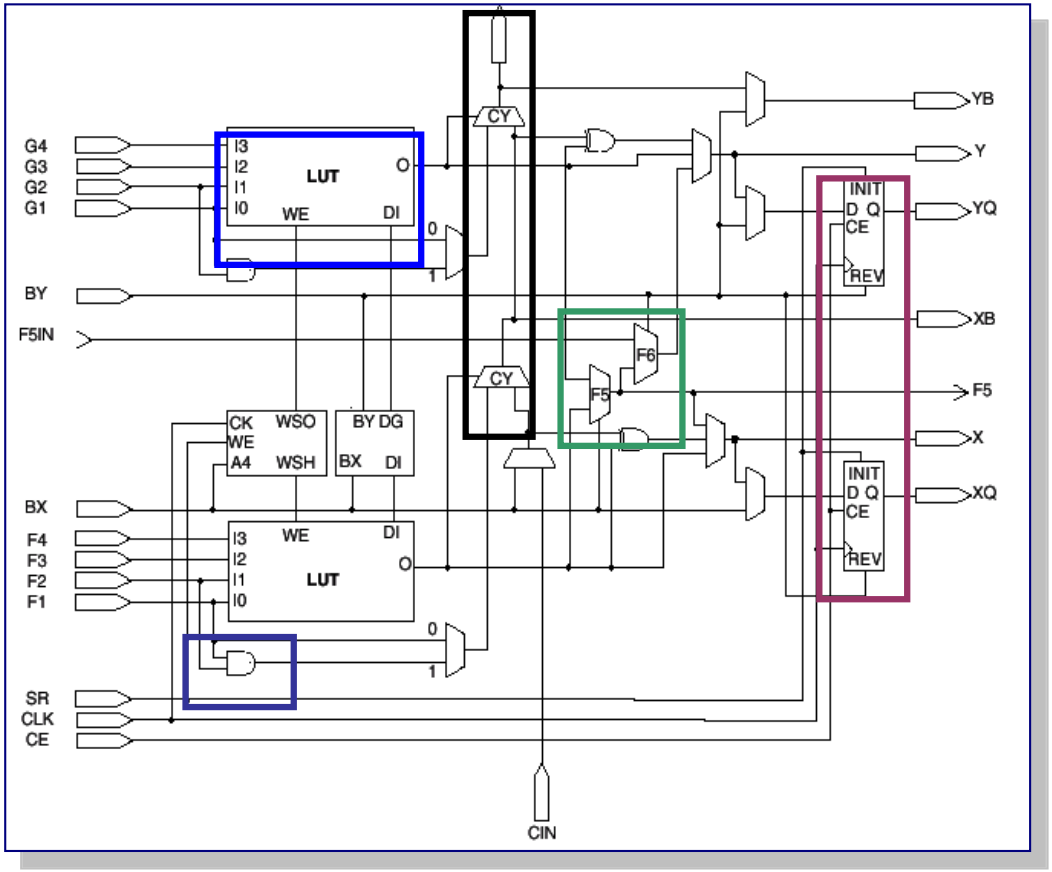
E.g.



- The MUXes increase the flexibility of a CLB
  - Output of MUX F5 can be any function of ≤5 variables or a restricted class of functions of up to 9 variables.
  - Output of MUX F6 can be any function of ≤6 variables or a restricted class of functions of up to 19 variables.

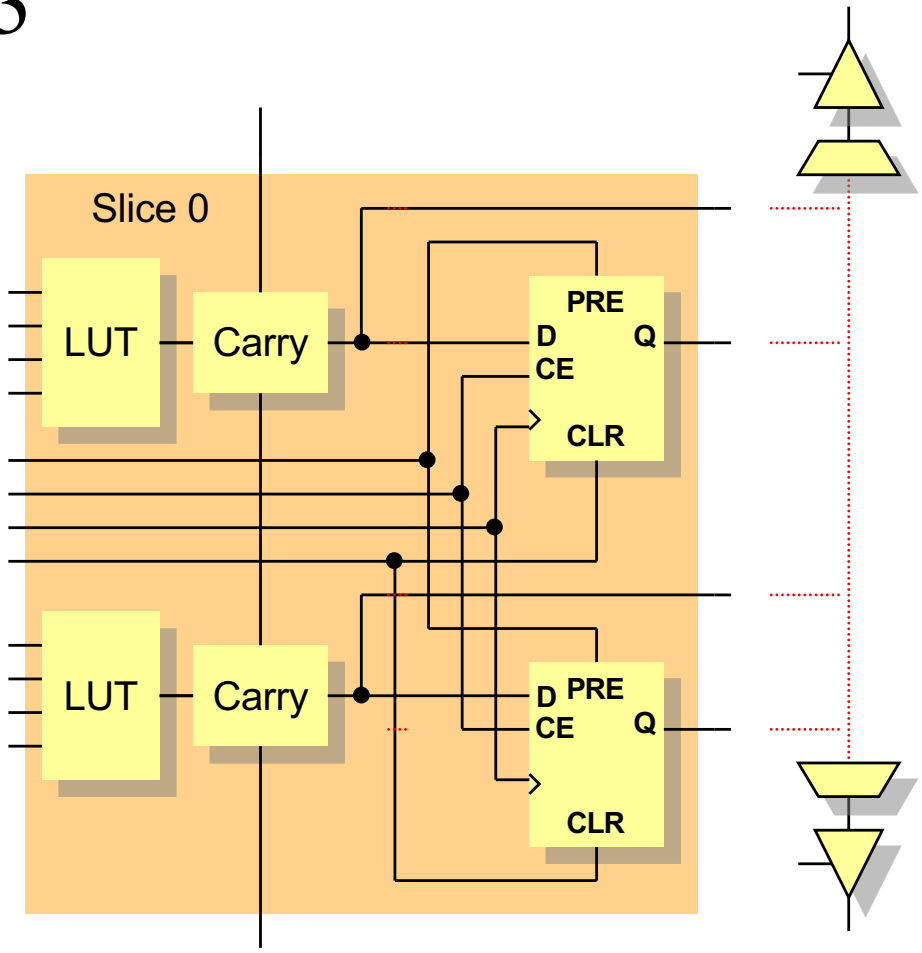
Detailed Slice Structure

- LUTs
- MUXF5, MUXF6, MUXF7, MUXF8 (only the F5 and F6 MUX are shown in this diagram)
- Carry Logic
- MULT_ANDs
- Flip-flops



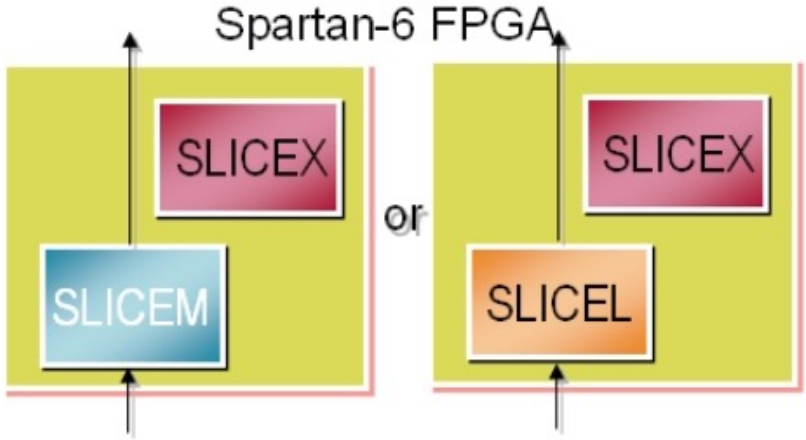
CLB Outputs

- E.g. A slice in Spartan-3
  - 4 outputs per slice
    - 2 registered, 2 non-registered
  - 2 BUFTs associated with each CLB
    - accessible by all 16 CLB outputs

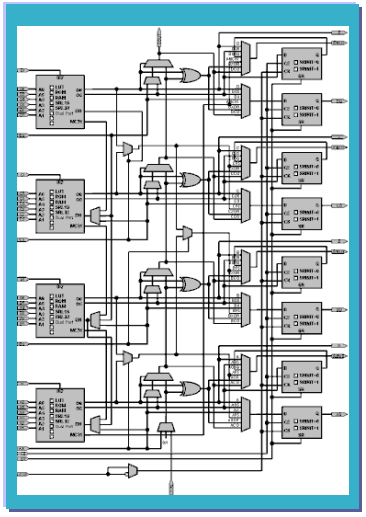


New Slice Structure in Spartan-6

- 3 Types of slices
  - Balance cost, power, performance

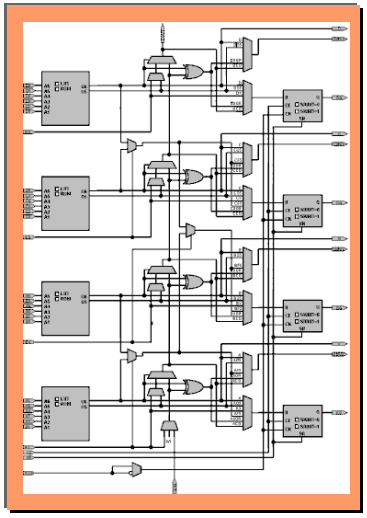


SliceM (25%)



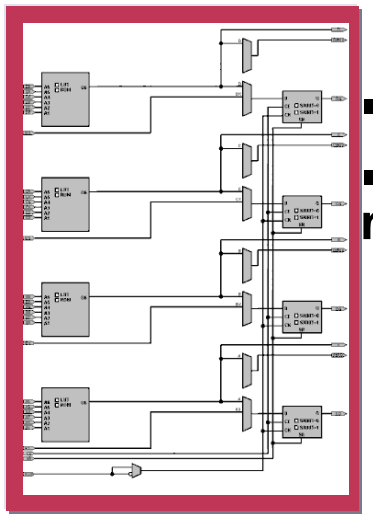
- 4 6-LUTs
- 8 registers
- w/ carry logic
- w/ wide muxes
- usable as RAM/shift register

SliceL (25%)



- 4 6-LUTs
- 8 registers
- w/ carry logic
- w/ wide muxes

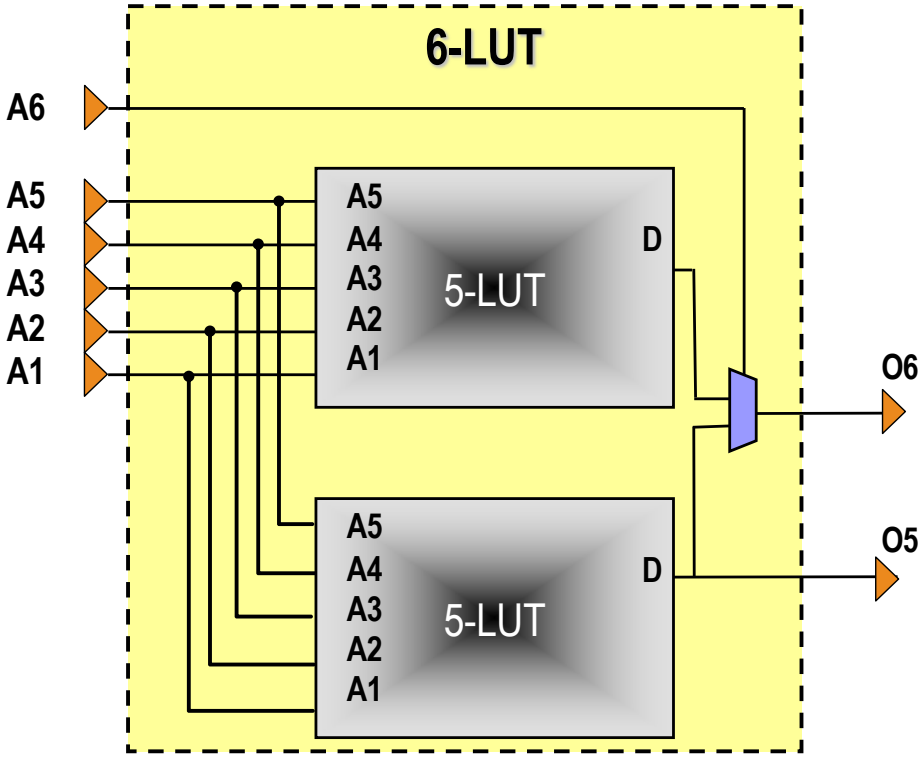
SliceX (50%)



- 4 6-LUTs
- 8 registers

New LUT Structure in Spartan-6

- 6-input LUT may serve as two 5-input LUTs with common inputs
  - Minimal speed impact to a 6-input LUT
  - One or two outputs
  - Any function of 6 variables or two functions of 5 identical variables



Interconnect

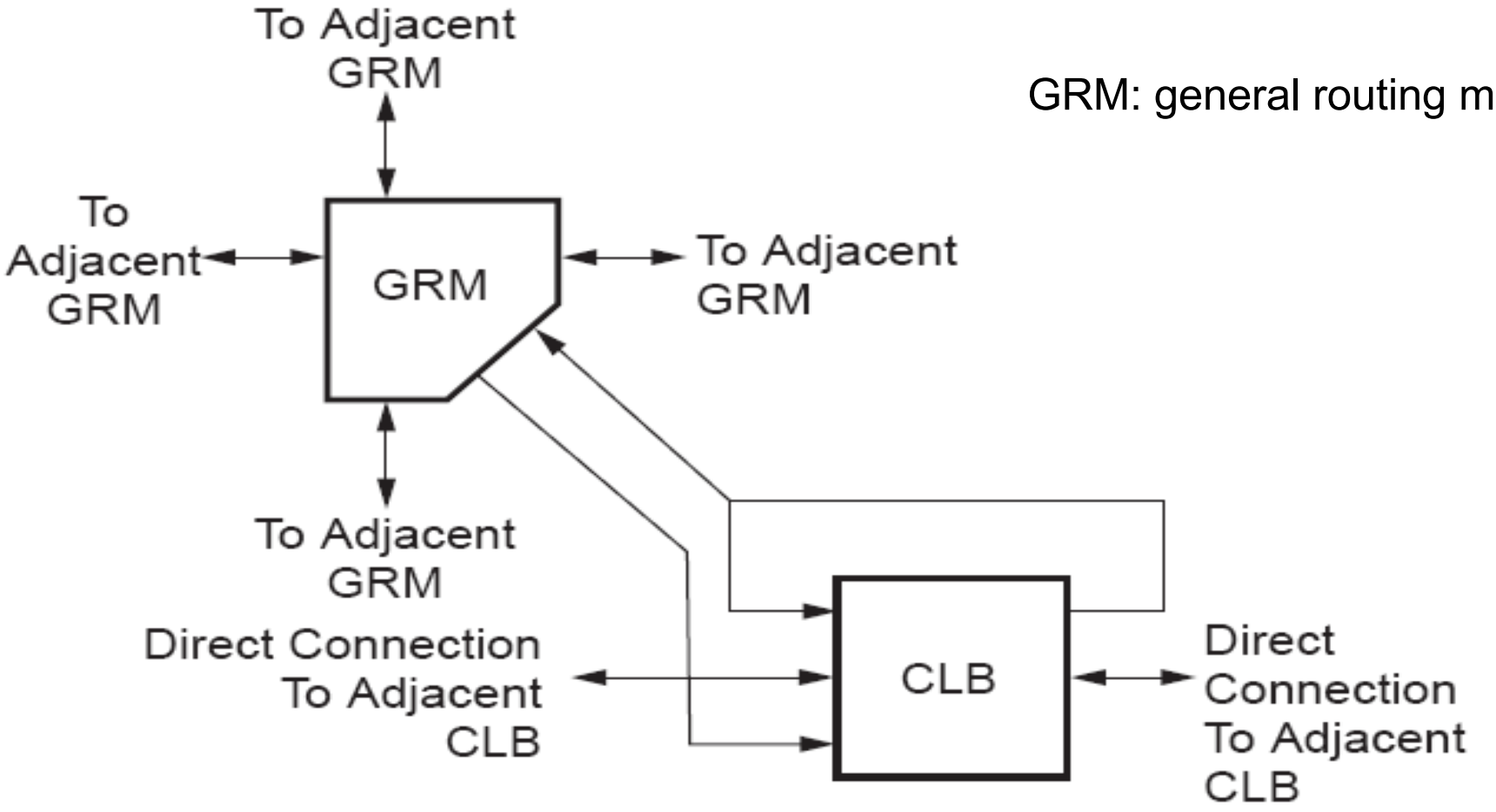
- Types of interconnect:
  - local (between slices in the same CLB or adjacent CLBs)
  - general-purpose (through general routing resources)
  - dedicated (e.g. for carry)
  - global routing network (for clock and other very high fanout signals)

General-Purpose Interconnect

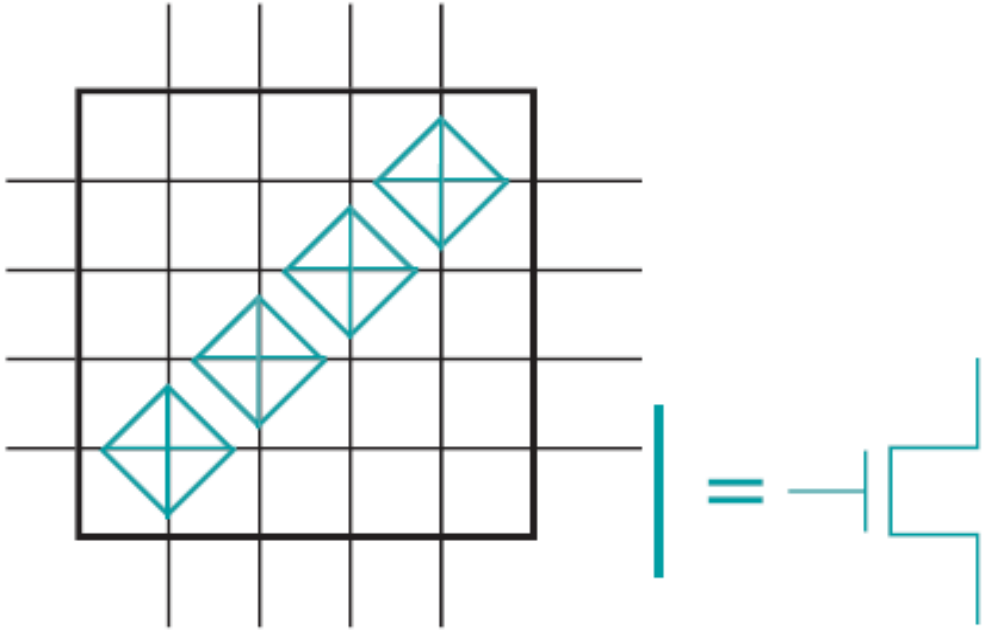
- General routing matrix (GRM) connects horizontal/vertical channels and CLBs.
- Single-length lines connect adjacent GRMs.
- Hex lines connect GRM to GRMs six blocks away.
- Buffered longlines span the chip.

General-Purpose Interconnect

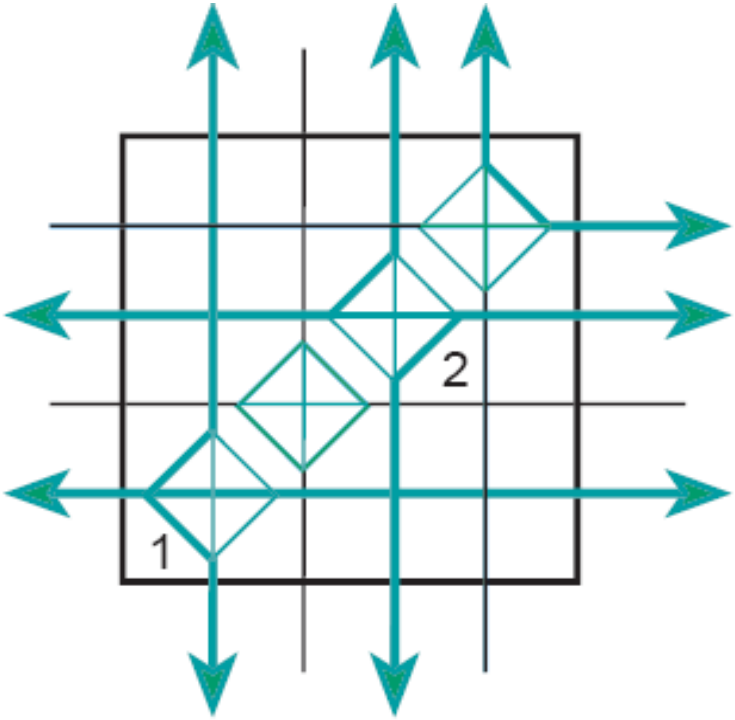
GRM: general routing matrix



General Routing Matrix



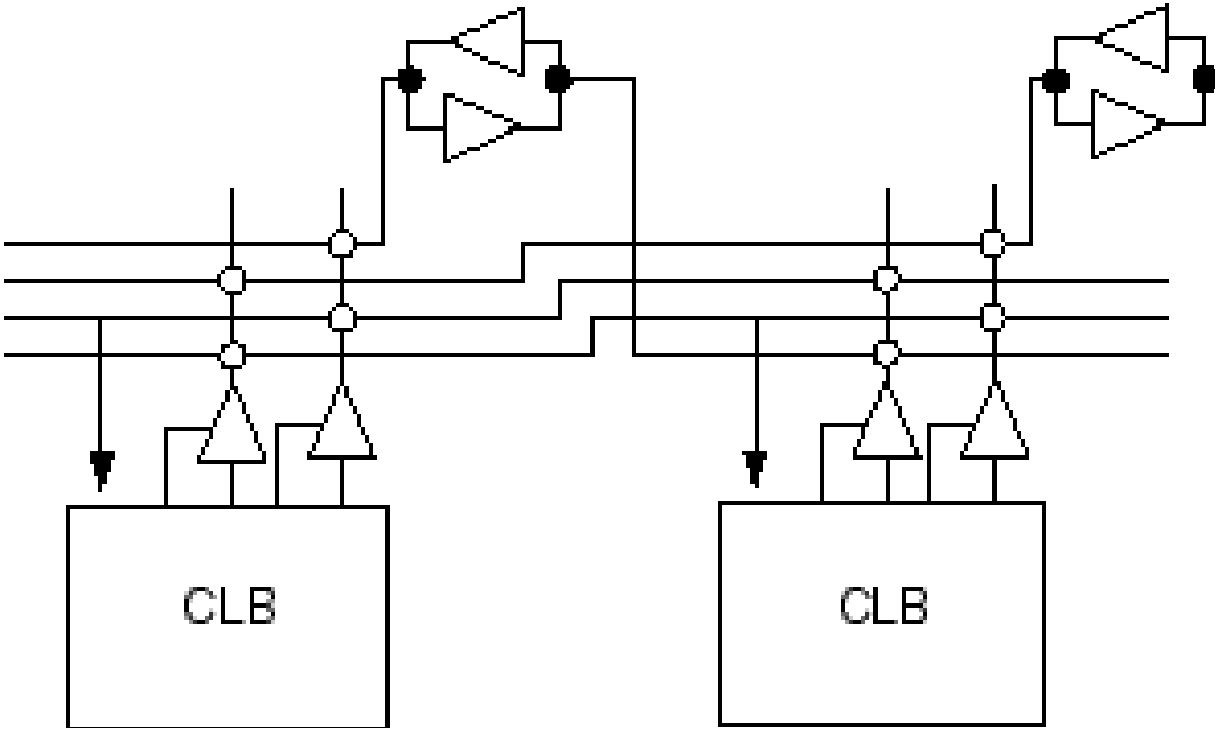
Switch box transistors



Connection example

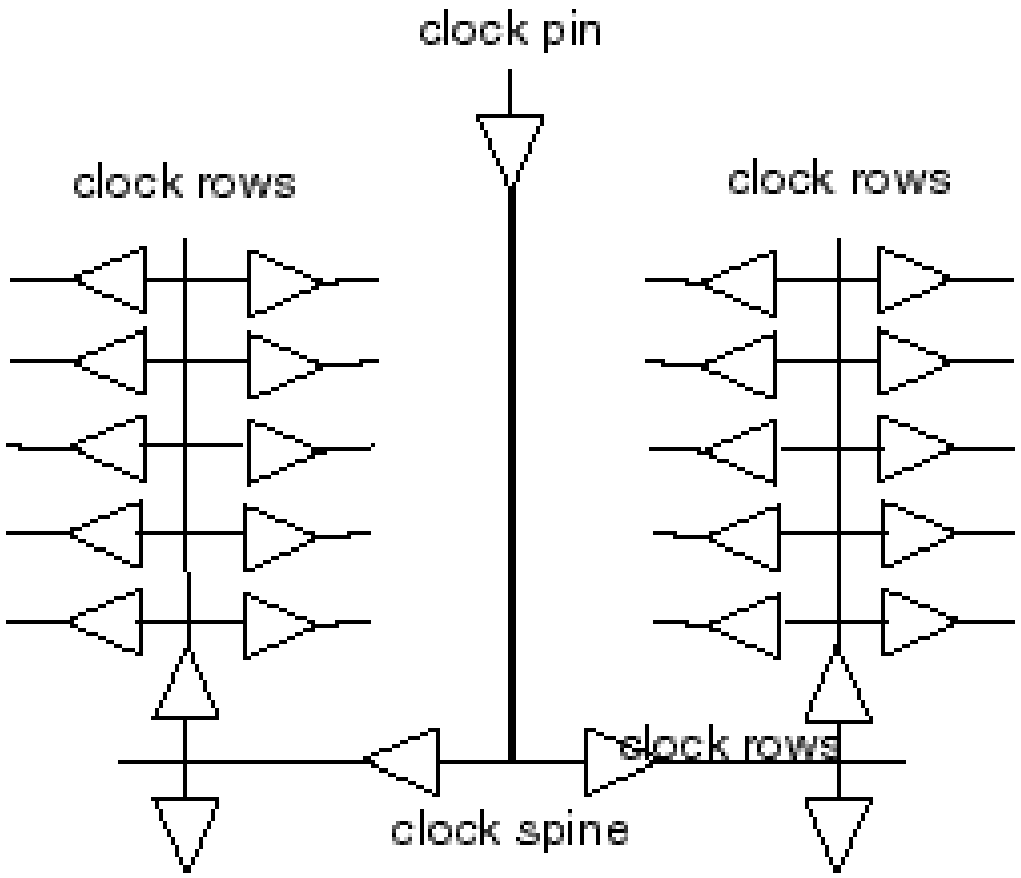
Three-State Bus

- Dedicated resources for horizontal on-chip busses:



Clock distribution

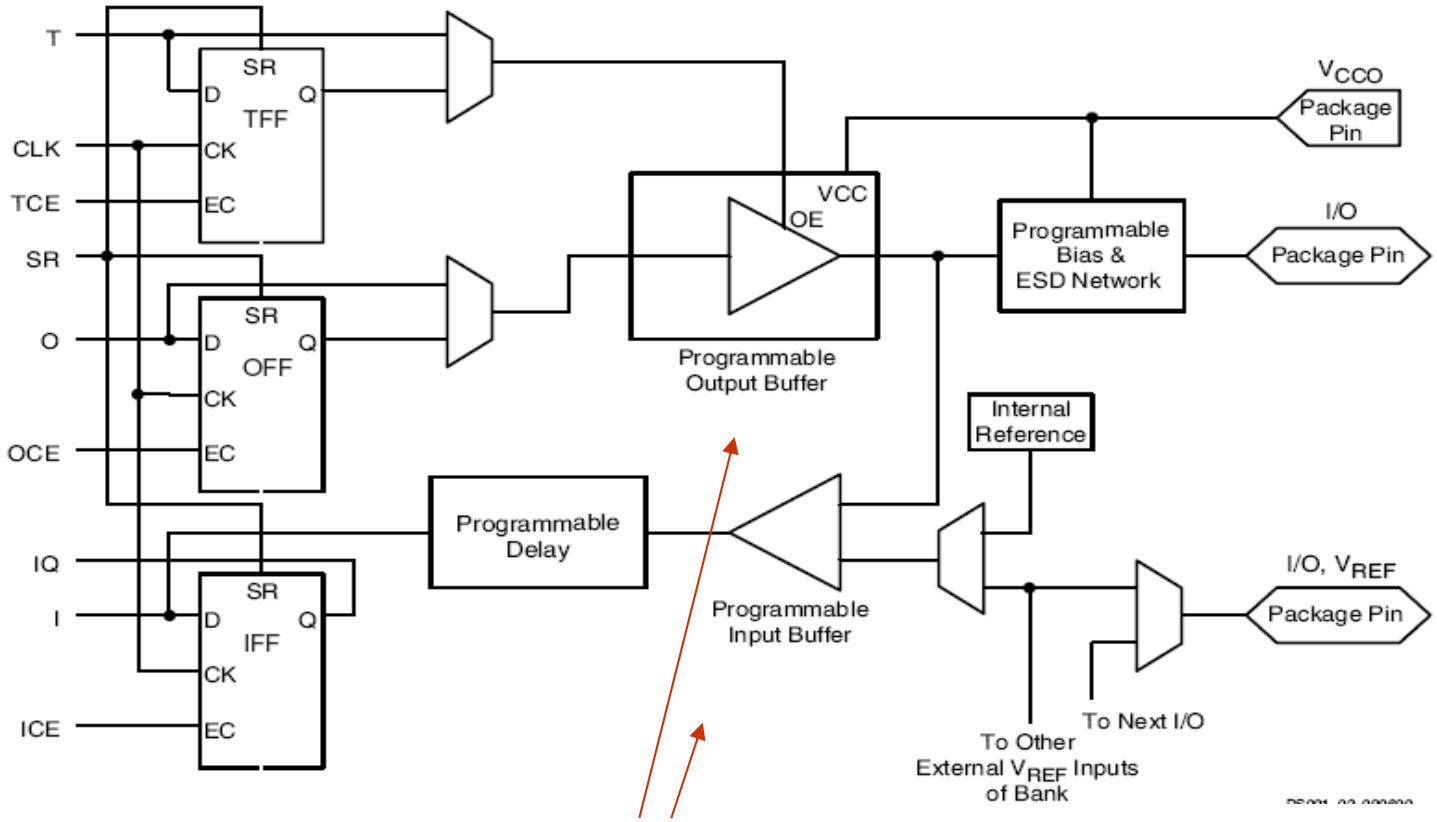
- Use global routing resources



I/O Block

- IOB provides interface between the package pins and CLBs
- Support a variety of IO standards
- Each IOB can work as uni- or bi-directional I/O
- Outputs can be forced into High Impedance
- Inputs and outputs can be registered
  - advised for high-performance I/O
- Inputs can be delayed

I/O Block Diagram

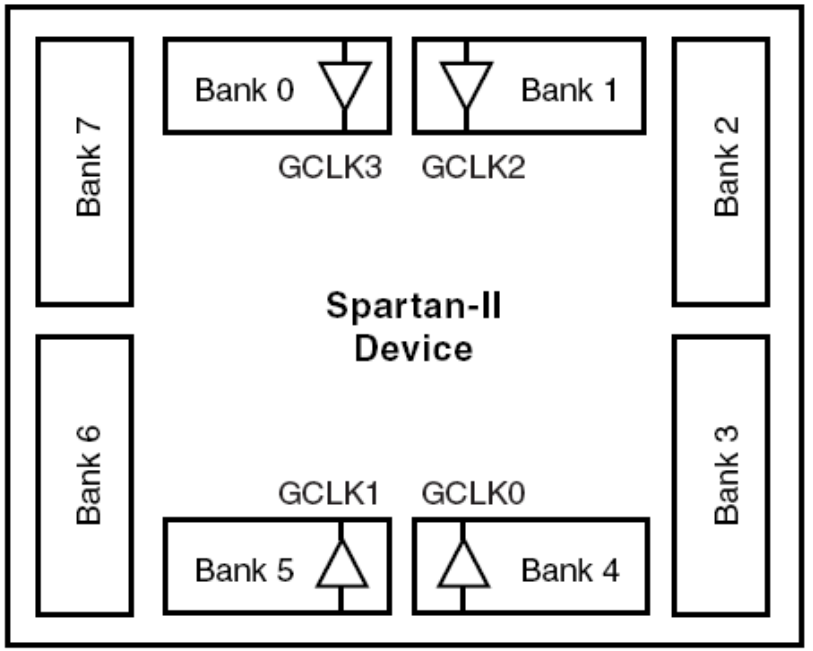


Can be configured to support different signaling standards

I/O Standards and I/O Banks

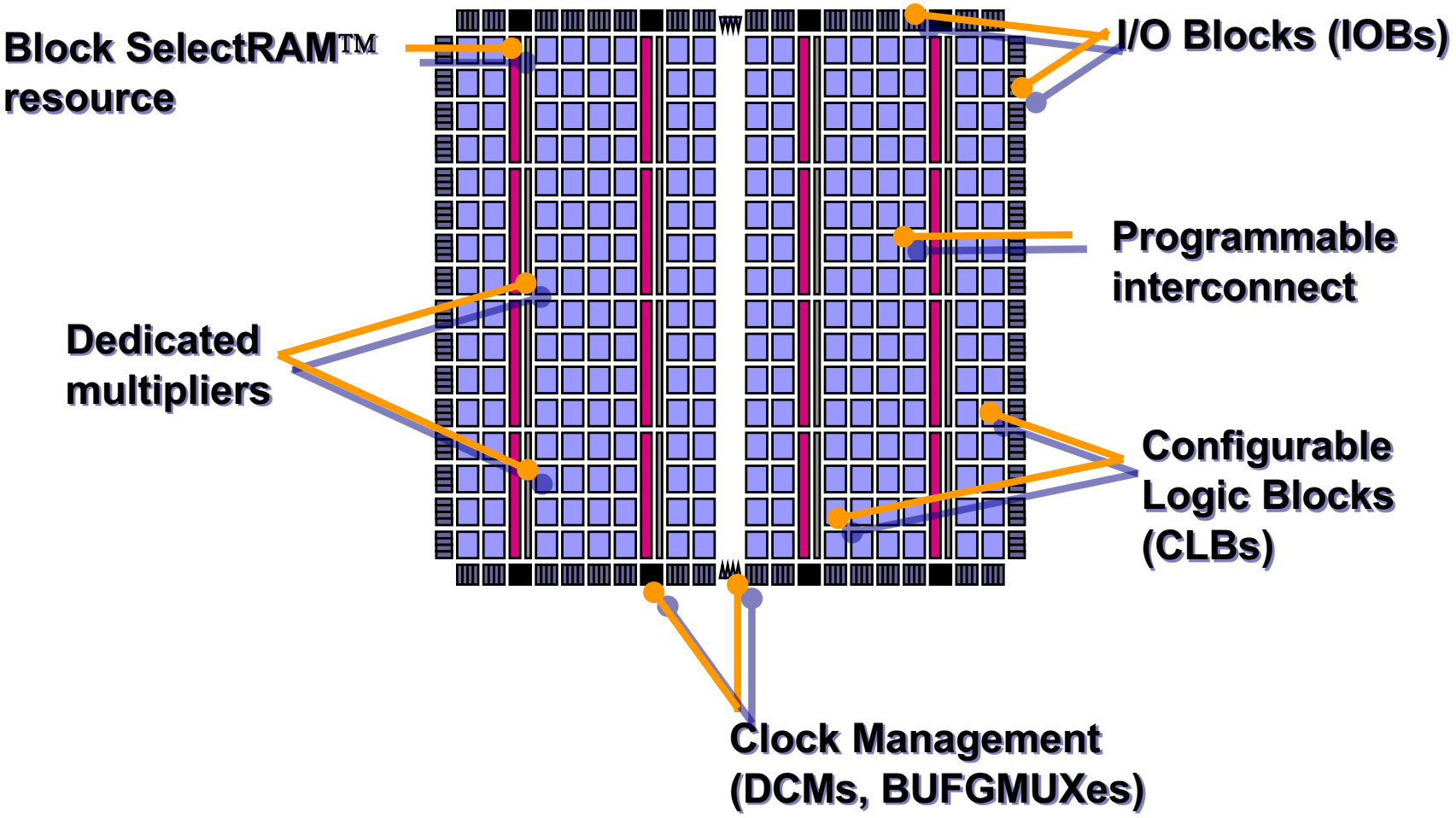
I/O Standard	Input Reference Voltage (V_{REF})	Output Source Voltage (V_{CCO})	Board Termination Voltage (V_{TT})
LVTTL (2-24 mA)	N/A	3.3	N/A
LVCMOS2	N/A	2.5	N/A
PCI (3V/5V, 33 MHz/66 MHz)	N/A	3.3	N/A
GTL	0.8	N/A	1.2
GTL+	1.0	N/A	1.5
HSTL Class I	0.75	1.5	0.75
HSTL Class III	0.9	1.5	1.5
HSTL Class IV	0.9	1.5	1.5
SSTL3 Class I and II	1.5	3.3	1.5
SSTL2 Class I and II	1.25	2.5	1.25
CTT	1.5	3.3	1.5
AGP-2X	1.32	3.3	N/A

I/O standards supported by Spartan-II



I/O bank organization.

Spartan-3 Architecture



Other Standard Features

- Block RAMs
  - Dedicated blocks of memory (18-kb blocks)
  - Use multiple blocks for larger memories
- Dedicated 18 x 18 multipliers next to block RAMs
- Clock management resources
  - Dedicated global clock multiplexers
  - Digital Clock Managers (DCMs)
    - multiple clock domains