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| **Homework 4 Report** | |
| Student ID: 123456789 | Name: 王大明 |

1. Design concept:

* Explanation of the overall hardware architecture, and block diagram of each component.
* State diagram and its detailed description (if any).
* Explanation of the dataflow.
* You may write the report in Chinese.

1. Result

|  |  |  |
| --- | --- | --- |
| Item | Description | Unit |
| RTL simulation | PASS | --- |
| Gate-level simulation | FAIL | --- |
| Gate-level simulation clock period | 10 | ns |
| Gate-level simulation latency | 10000 | cycles |
| Total cell area | 80000 |  |

1. Others (optional)

* Suggestions or comments about this class to teacher or TA.