Input may contain both single-bit flip-flops and multi-bit flip-flops.

Input could have negative slacks.

we are not guaranteed that the die width and height are divisible by the bin width and height.

it is possible that the outputs of multiple single-bit flip-flops are connected to the same multi-bit flip-flop as its inputs. Multi-fanout nets are possible.

is it permissible during the banking process to merge two 1-bit Flip-

Flops into one 4-bit Flip-Flop, while retaining four empty pins (2 sets of D and

Q)?

Cell heights can be multi-row height and are not necessarily an integer multiple of site height.

orientation is not considered in this contest.

Even if the output is using the same flip-flop type, contestant should still list the mapping. (such as "C1/D map C1/D")

If a FFN has multiple predecessor FF0s (e.g. for a 2-NAND gate, two input pins connect to 2 predecessor FF0s respectively and the output pin connects to successor FFN), how to determine the delta QpinDelay (δ0 – δ0’) in slack calculation?

We calculate the problem with the larger one (both QpinDelay and DisplacementDelay ).

Contestants must calculate the arrival time for multi-timing paths and determine the critical path by themselves.

We do not need to consider the clock delay and clock skew.

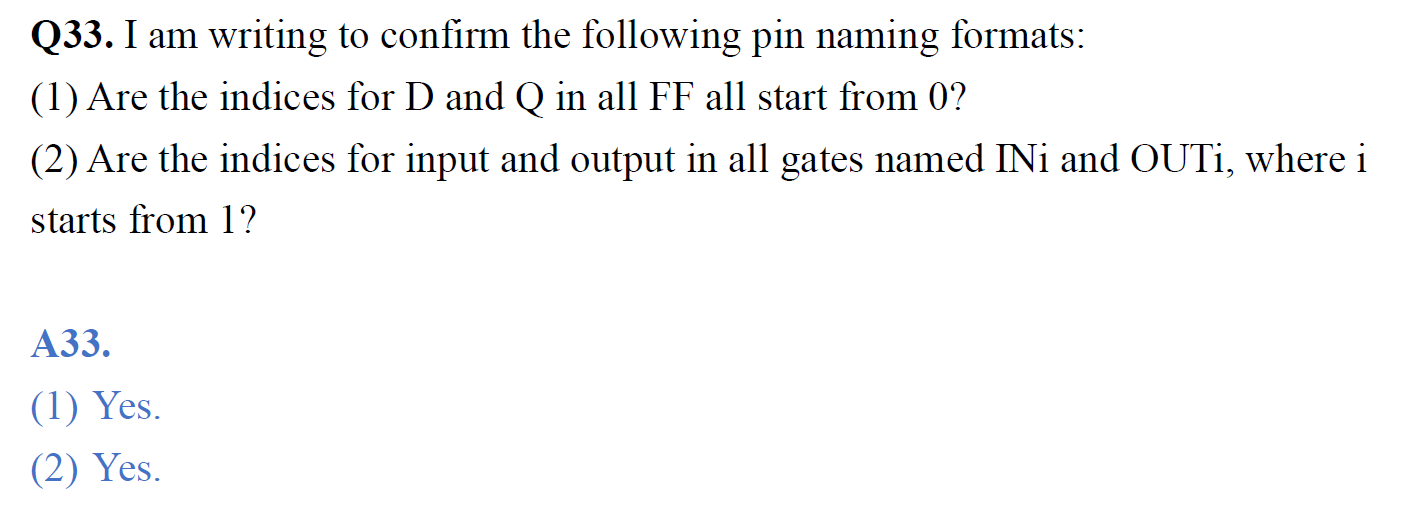
The cost only considers negative slack.

As long as the cell overlaps the bin, the overlapping area is considered in the bin utility.

Is the number of each FF type necessarily the power of 2?

Not necessary. For example, there might be FF with 6 bits.

Placement area could also be rectilinear



Pin <pinName> <pinLocationX> <pinLocationY>.

x,y are integers.

pin locations are relative to the bottom left corner of an instantiated cell.

We assume all combinational gate delays are equal or 0. contestants don’t need to consider the combinational gate delay when calculating arrival time.

we are focusing on d-pin slacks