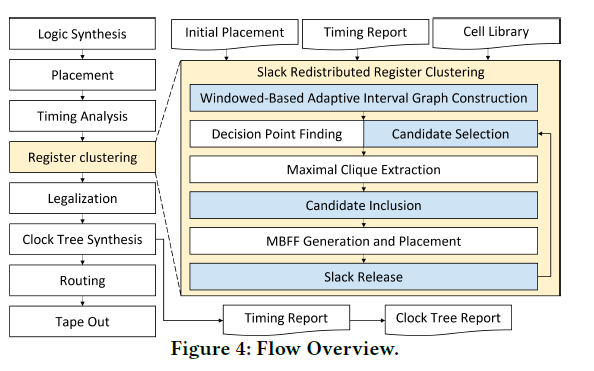
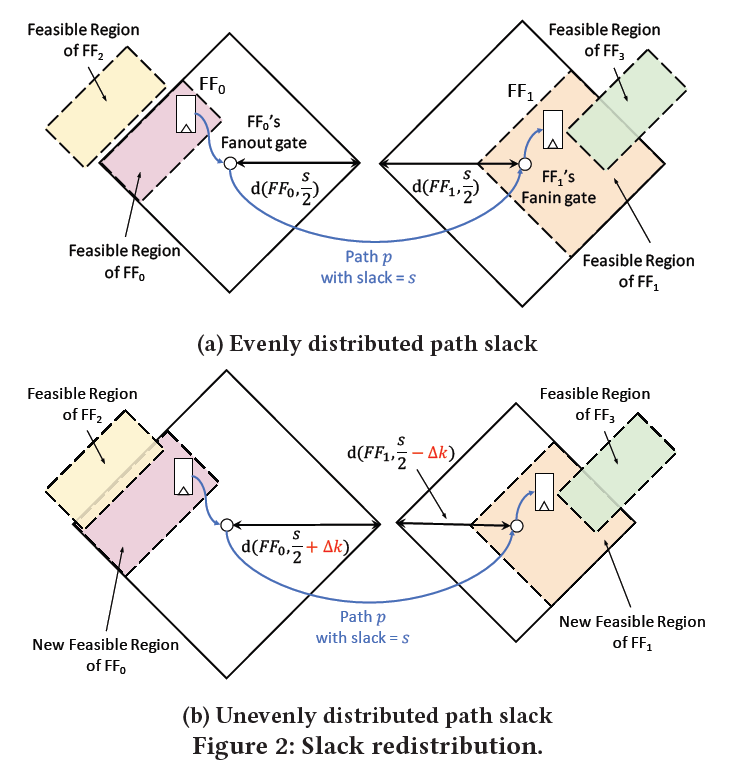
1. **Slack Redistributed Register Clustering with Mixed-Driving Strength Multi-bit Flip-Flops**





Objective: minimize Power WNS TNS

**clique partitioning approach**

**Post-placement power optimization with multi-bit flip-flops**

window-based clique extraction in the intersection graph

**INTEGRA: Fast multibit flip-flop clustering for clock power saving**

fast algorithm based on coordinate transformation and interval graph data structure

**Timing-Driven and Placement-Aware Multibit Register Composition**

ILP to minimize the total number of MBFFs and further improve performance by using incomplete MBFFs and MBFF sizing

**clustering-based approach**

**Flip-flop clustering by weighted K-means algorithm**

weighted K-means algorithm where additional weights were introduced in its cost function along with a post-processing mechanism to balance cluster sizes.

**Improved flop tray-based design implementation for power reduction**

proposed a capacitated K-means method and used ILP to globally optimize the clustering results

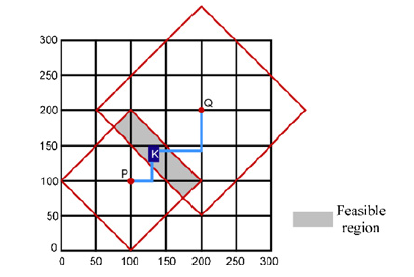
**Graceful register clustering by effective mean shift algorithm for power and timing balancing**

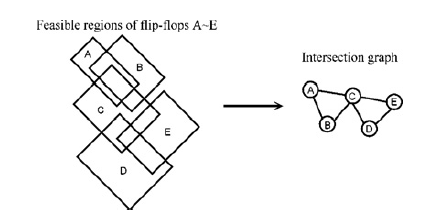
effective mean shift algorithm with timing slack consideration to minimize timing degradation and parallelizable computation to enhance scalability

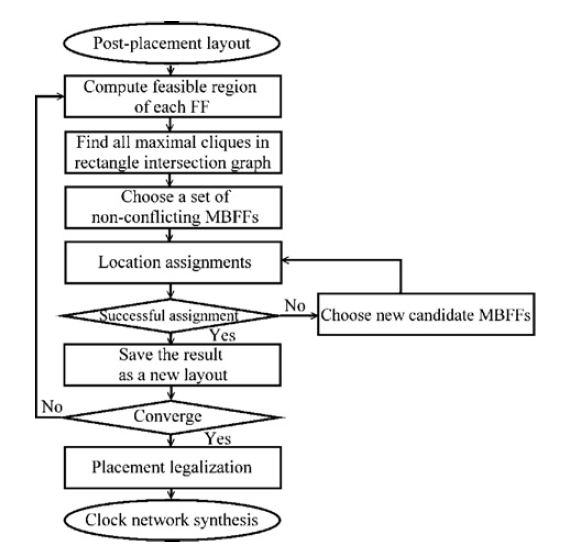
**Latch clustering for timing-power co-optimization**

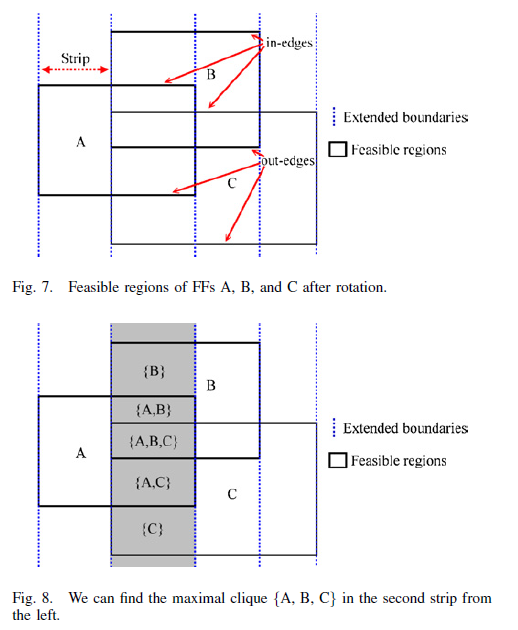
formulating the problem as a facility-location allocation problem and using ILP to satisfy timing and power requirements

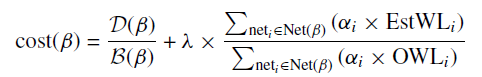
1. **Power-Driven Flip-Flop Merging and Relocation**

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To avoid creating a MBFF whose fanins and fanouts are too far away to reduce the total wirelength of signal nets

