CS577: C-Based VLSI Design

Read the Instructions and copy it to your notebook before starting the examination.

Figures for Paper 2:

Instructions and Figure 4:
Consider the Sequence Graph shown in the figure 4 below. Each MUL operation takes two-unit times, and ADD takes one unit of time. Given **3 MUL and 1 ADD and resource constraints**, schedule the graph using **minimize latency under resource-constrained (MLRC) LIST-schedule** and answer the following questions in Paper 2 marked with Figure 4. Consider **the length of the path from a node to the sink node as the priority function. In case of two nodes with same priority, the node with smaller label will be selected.**

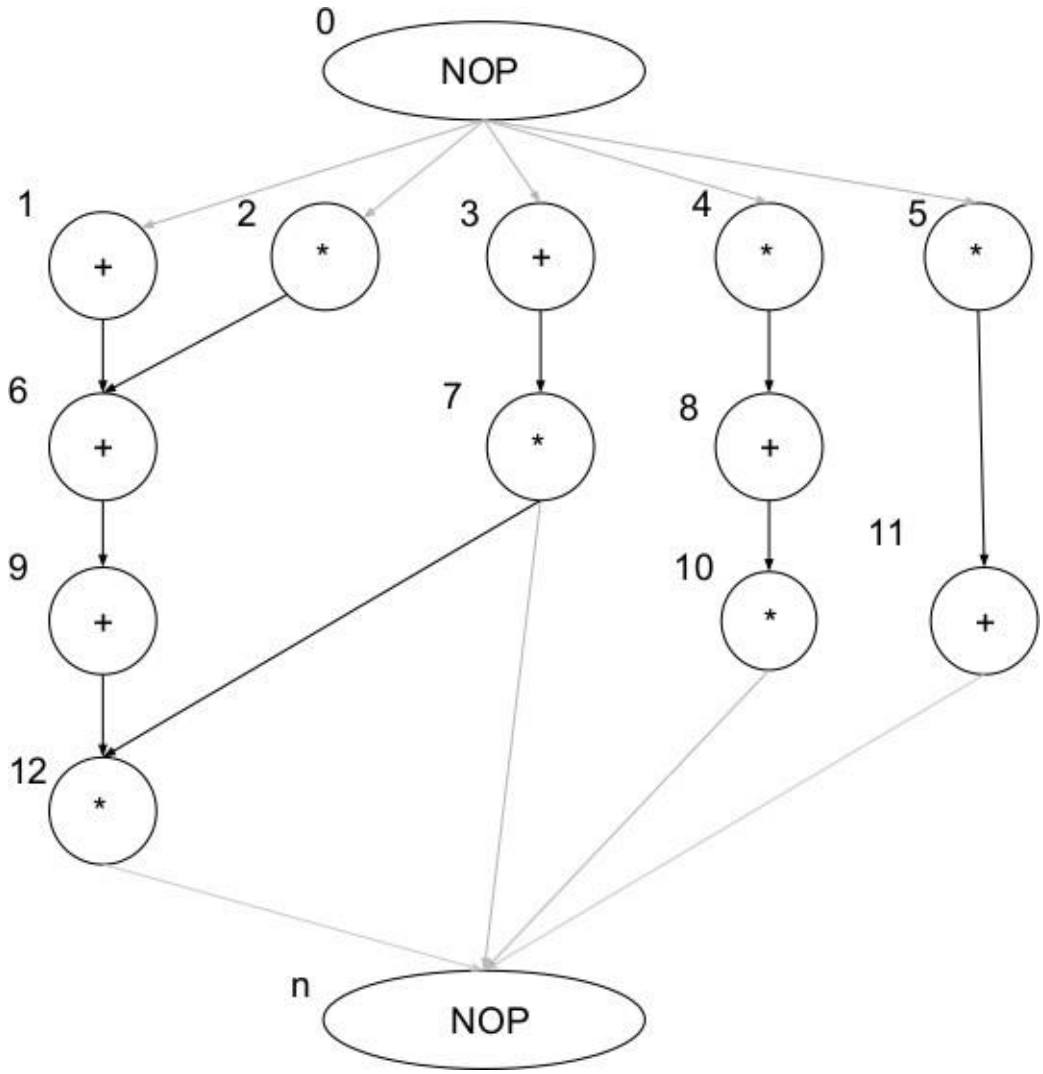

Figure 4: Sequence Graph for Questions marked with [Figure 4] in Paper 2