AN-9005

Driving and Layout Design for Fast Switching Super-Junction MOSFETs

Abstract

Power MOSFET technology has been developed towards higher cell density for lower on-resistance. There are, however, silicon limits for significant reduction in the on-resistance with the conventional planar MOSFET technology because of its exponential increase in on-resistance according to the increase of blocking capability. One of efforts to overcome the silicon limit is super-junction technology in high-voltage power MOSFETs. The super-junction technology can dramatically reduce both on-resistance and parasitic capacitances, which usually are in trade-off. With smaller parasitic capacitances, the super-junction MOSFETs have extremely fast switching characteristics and reduced switching losses. Naturally, this switching behavior occurs with greater dv/dt and di/dt that affect switching performance via parasitic components in devices and printed circuit board. It is also related to EMI performance of the system. Therefore, an optimized design is very important to operate high-speed MOSFETs. The purpose of this application note is to discuss driving methods and layout requirements in relation to switching performance of fast switching MOSFETs.

Introduction

The power losses of the switching device can be broken into four parts: conduction losses, switching losses, turn-off state losses due to leakage current, and driving losses. In most switching power applications utilizing high-voltage switching devices, the last two parts can be neglected. The conduction losses can be reduced through realizing lowest possible on-resistance. The switching losses are determined by the duration of switching transient, a period where current and voltage present simultaneously across the channel of the device. Faster switching transients reduces switching power losses. The switching device should have very low parasitic capacitances to be switched quickly. Therefore, considerable work has focused on improving on-resistance and capacitances. Successive generations of super-junction MOSFET technology have shown dramatic decrease of the transistor specific on-resistance ($R_{ON,sp}$)[1]-[2]. Smaller die size and faster switching performance can be achieved by lowering $R_{DS(ON)}$ and gate charge (Q_G). However, sharp transitions in voltage and current result in high-frequency noises and radiated EMI. To achieve low noise radiation, high values of parasitic capacitances are required. There is direct conflict in parasitic capacitance requirements. Based on recent system trends, improving efficiency is a critical goal and going with slow switching device just for EMI is not an optimized solution. This note tackles how to achieve balance between these considerations when designing with fast-switching power devices.

Super-Junction MOSFET Technologies

The $R_{DS(ON)} \times Q_G$, Figure Of Merit (FOM) is generally considered the single most important indicator of MOSFET performance in Switching Mode Power Supplies (SMPS). Therefore, several new technologies have been developed to improve the $R_{DS(ON)} \times Q_G$ FOM. The super-junction device utilizing charge balance theory was introduced to the semiconductor industry ten years back and it set a new benchmark in the high-voltage power MOSFET market[3]. Figure 1 shows the vertical structure and electric field profile of a planar MOSFET and super-junction MOSFET. Breakdown voltage of a planar MOSFET is determined by drift doping and its thickness. The slope of electric field distribution is proportional to drift doping. Therefore, thick and lightly-doped EPI is needed to support higher breakdown voltage. The major contribution to on-resistance of high-voltage MOSFET comes from the drift region. Therefore, the on-resistance exponentially increases with the light doping and thick drift layer for higher breakdown voltage, as shown in Figure 2.

Super-junction technology has deep P-type pillar-like structure in the body in contrast to the well-like structure of conventional planar technology. The effect of the pillars is to confine the electric field in the lightly doped EPI region. Thanks to this P-type pillar, the resistance of N-type EPI can be reduced dramatically compared to the conventional planar technology, while maintaining same level of breakdown voltage. Therefore, this new technology broke silicon limit in terms of on-resistance and achieved only one-third the specific on-resistance per unit area compared to planar processes[4]. It is well known that this technology also achieved unique non-linear parasitic capacitance characteristics and enabled reduced switching power losses.

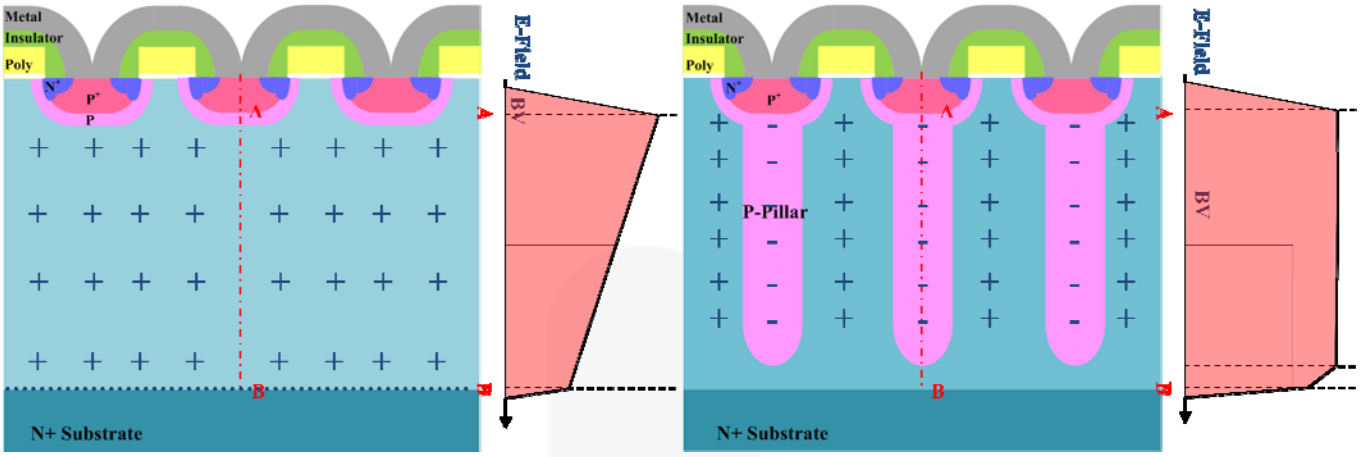

Figure 1. Planar MOSFET (Left) and Super-Junction MOSFET (Right)

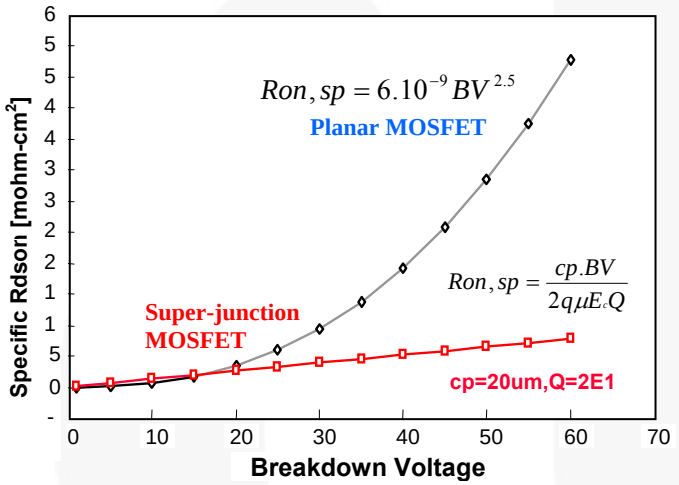

Figure 2. Specific $R_{DS(ON)}$ of Planar MOSFET and Super-Junction MOSFET as a Function of Breakdown Voltage

Power Losses in MOSFET

The super-junction devices utilizing charge-balance theory achieved great reduction in on-resistance of high-voltage MOSFETs. Since conduction losses are directly proportional to on-resistance, super-junction devices like SupreMOS® provide great advantage for conduction losses. Faster switching transient can reduce switching losses. Since a MOSFET is a uni-polar device, parasitic capacitances are the only limiting factors in switching transient. Lower parasitic capacitance is required for smaller switching losses.[5] The charge-balance principle lowers on-resistance per specific area and enables shrink of the chip size for the same $R_{DS(on)}$, compared to standard MOSFET technology. As shown in Figure 3, the latest super-junction MOSFET input capacitance and Miller capacitance are greatly reduced from the previous generation. However, output capacitance curves look similar. The latest super junction MOSFET only shows more non-linear behavior. One possible way to find out how the output capacitance corresponds to switching losses is evaluating an effective value of output capacitance. The stored energy in the output capacitance of a MOSFET can be calculated by integrating the product of output capacitance and drain-source voltage with respect to drain-source voltage from zero to drain-source voltage just before the turn-on transient. This stored energy is dissipated through the channel of the MOSFET on every turn-on of a switching cycle. The SuperFET® II MOSFET has approximately 27% reduced stored energy in output capacitance than similar on-resistance devices of previous generation SuperFET® I MOSFET for typical switching power supply bulk capacitor voltage. The benchmark of stored energy in output capacitance is shown in figure 4.

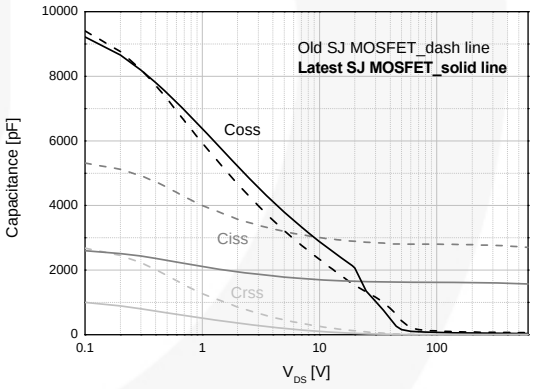

Figure 3. Capacitances of SuperFET® I MOSFET vs. SuperFET® II MOSFET

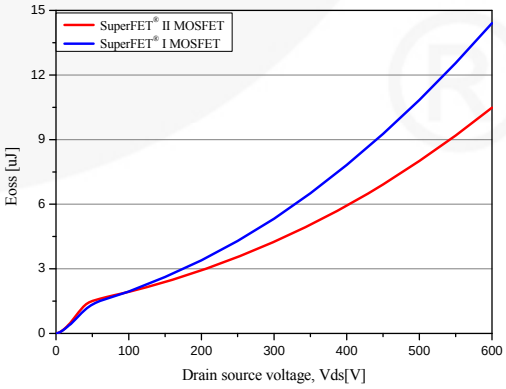

Figure 4. Stored Energy in Output Capacitance

Figure 5 shows capacitances of super-junction MOSFET and planar MOSFET. C_{ISS} of the super-junction MOSFET stays largely unchanged, but both C_{RSS} and C_{OSS} of the super-junction MOSFET become strongly non-linear. C_{RSS} decreases very rapidly around 10 V drain-source voltage. These effects allow an extremely fast dv/dt and di/dt. This high-switching speed reduces switching losses, but has negative effects, such as increased EMI, gate oscillation, and high peak drain-source voltage. Therefore, control of the maximum switching speed is very important to obtain extreme performance of super-junction MOSFETs without negative effects.

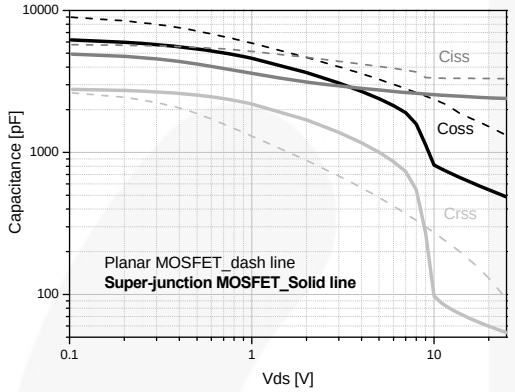

Figure 5. Comparison of Capacitances between Planar MOSFET and Super-Junction MOSFET

Influence of Circuit Parameters On Switching Characteristics

The faster switching of the power MOSFETs enables higher power conversion efficiency. However, parasitic components in the devices and boards are involving switching characteristics more as the switching speed is getting faster. This creates unwanted side effects, like high voltage or current spikes or poor EMI performance. To achieve balance, it is important to have optimized gate drive circuitry because the power MOSFET is a gate-controlled device. Minimizing of parasitic inductance and capacitance on the printed circuit board (PCB) is also important.

Effect of Gate Resistance

One of the critical control parameters in gate-drive design is the external series gate resistor (R_g). This dampens down peak drain-source voltage and prevents gate ringing caused by lead inductance and parasitic capacitances of the power MOSFET. It also slows down the rate of rise of voltage (dv/dt) and current (di/dt) during turn-on and turn-off. However, R_g affects the switching losses in MOSFETs. Controlling the losses is important as devices need to achieve the highest efficiency on the target application. Therefore, from an application standpoint, selecting the optimized R_g is very important. Too small R_g results in excessive dv/dt across drain and source of the MOSFET during switching off; therefore, low limit is a value that keeps switching dv/dt within the specification in the datasheets. Too large R_g causes more losses and poor efficiency; therefore, the upper limit is chosen to have the same switching losses as the previous version of super-junction MOSFET or competitors.

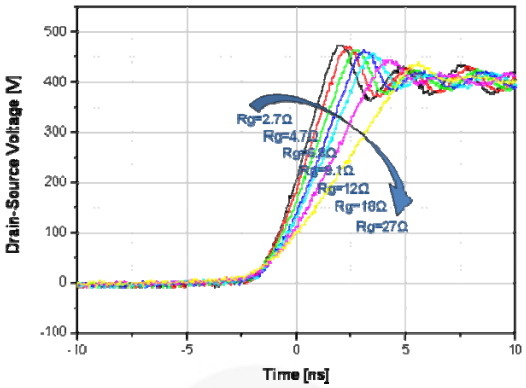

Figure 6. Drain-Source Waveforms of MOSFET According to Gate Resistors

Figure 6 shows turn-off response of a MOSFET according to various gate resistors. When the planar MOSFET or other previous-generation power MOSFET is directly replaced with the super-junction MOSFET, switching losses are reduced, but the dv/dt may become higher. To control of the super-junction MOSFET, increased R_g is required. In this case, there should be a limit line for increasing the R_g or switching losses with super-junction MOSFET can be larger. Figure 7 shows switching losses with a previous generation super-junction MOSFET and Figure 8 shows a new super-junction MOSFET. Based on the pictures, an R_g for both similar or less switching losses and controlled dv/dt can be selected.

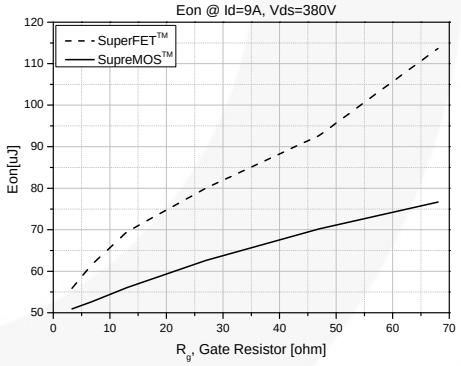

Figure 7. Turn-on Energy Loss (E_{ON}) vs. Gate Resistors

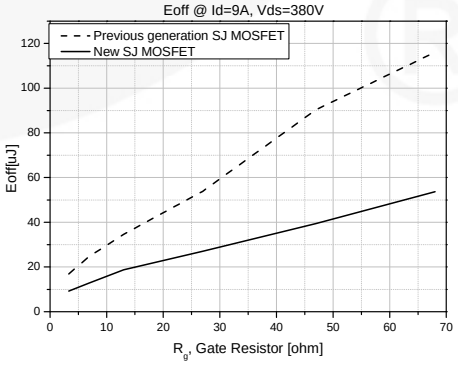

Figure 8. Turn-Off Energy Loss (E_{OFF}) vs. Gate Resistors

Effect of Clamp Diodes

The turn-on behavior of the MOSFET is strongly dominated by the reverse-recovery characteristics of free-wheeling diodes on clamped inductive switching. When an Si diode is suddenly reverse-biased, a large amount of stored charge, which has not recombined yet in depletion layers, can flow in the reverse direction before blocking the reverse voltage. SiC Schottky diodes have no reverse-recovery current during switching transition because there are no excessive minority carriers. However, there is displacement current, which is negligible, from parasitic junction capacitances. Therefore, SiC Schottky diode and Si diodes are used for clamped diodes since this drastic difference of reverse-recovery characteristics in transient behavior allows the significantly different MOSFET switching losses and dv/dt. Figure 9 shows the turn-on switching losses according to external gate resistors and with different clamping diodes. The dv/dt with a SiC Schottky diode is lower than dv/dt with Si diode due to the bigger junction capacitance of SiC, as shown Figure 10. A gap of the dv/dt values is getting larger at lower drain current level and smaller R_g. This is because, at lower current, the dv/dt is relatively low and the effect of output capacitance of the MOSFET and diode junction capacitance on the dv/dt becomes more significant.

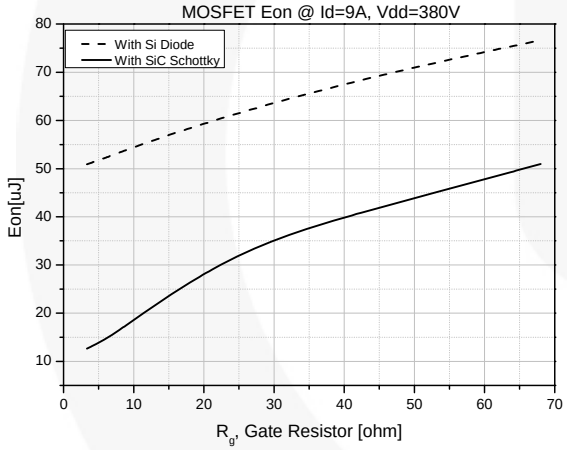

Figure 9. Turn-On Energy Loss (E_{ON}) of Super-Junction MOSFET According to Clamp Diodes

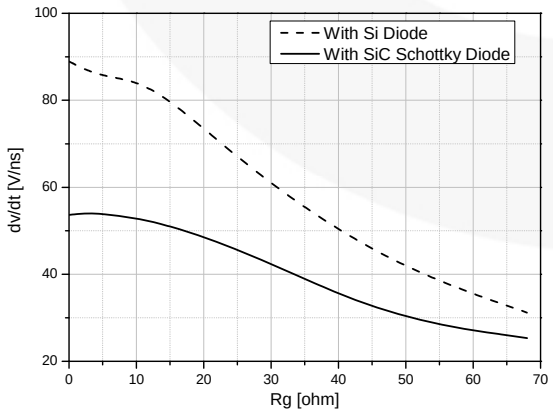

Figure 10. Turn-off dv/dt of Super-Junction MOSFET According to Clamp Diodes

Effect of Ferrite Bead Core

A major noise source has been traced to the oscillation from the MOSFET at switching on-off transient. Typically, parasitic oscillation frequencies are in the range of several tens to hundreds of megahertz. The parasitic oscillation can cause gate-source breakdown, bad EMI, large switching losses, losing gate control, and can even lead to MOSFET failures. A ferrite bead is often used on MOSFET gate leads to provide stable operation by suppressing parasitic oscillation, while minimizing switching losses. In fact, adding a ferrite bead is more effective than using gate resistance alone because the impedance of the ferrite bead varies by frequency. Figure 11 shows an equivalent circuit of ferrite bead and Figure 12 shows impedance characteristics as a function of frequency. R_{bead} and L_{bead} are the DC resistance and effective inductance of the ferrite bead. C_{para} and R_{para} are the paralleled capacitance and resistance associated with the ferrite bead. Simply, the ferrite bead is a frequency-dependent resistor. At low frequencies, C_{para} is an open circuit and L_{bead} is a short circuit, leaving only R_{bead} as the DC resistance of the ferrite bead. As frequency increases, the impedance of L_{bead} starts to increase linearly with frequency ($j\omega L_{bead}$), while the impedance of C_{para} decreases inversely proportionally to frequency ($1/j\omega C_{para}$), as shown by Equation (1):

$$Z = R + jX \quad (1)$$

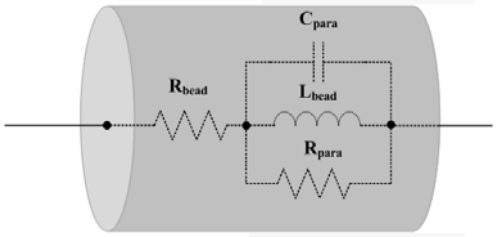

Figure 11. Equivalent Circuit of Ferrite Bead

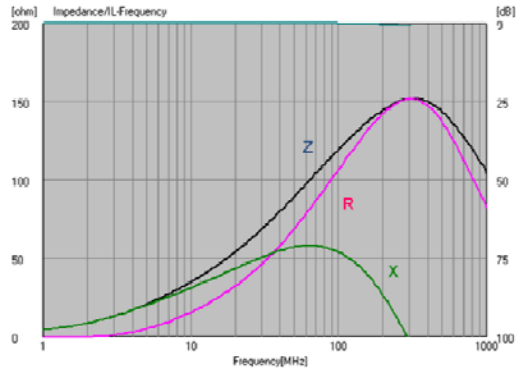

Figure 12. Impedance Characteristics vs. Frequency

The rising linear slope of the ferrite bead's impedance-versus-frequency plot is determined mainly by the inductance of L_{bead}. At a certain high-frequency point, the impedance of C_{para} begins to dominate and the ferrite bead's impedance starts to decrease, countering its inductance. In this case, the falling slope of the impedance-versus-

frequency plot is determined mainly by the parasitic capacitance, C_{para}, of the bead. At low frequency, inductive impedance is low. Therefore, the ferrite bead inductance works like resistors instead of inductors at high frequency. Normally, the parasitic oscillation frequency is much higher than switching frequency. Its high impedance at high frequency is extremely effective at blocking drain-to-gate noise. Given enough inductance in the ferrite bead combined with resistance, its high-frequency parasitic oscillation can be significantly suppressed. Figure 13 and Figure 14 present comparisons of gate oscillation according to ferrite bead. Oscillation is dramatically suppressed by using ferrite bead on gate lead of MOSFET. It is a very simple and cost-effective way to solve oscillation issues in some applications. With ferrite bead inductors, the impedance varies depending upon the material and internal structure. When selecting a ferrite bead, it is necessary to consider the impedance in the noise band, rated current, and the impedance gradient.

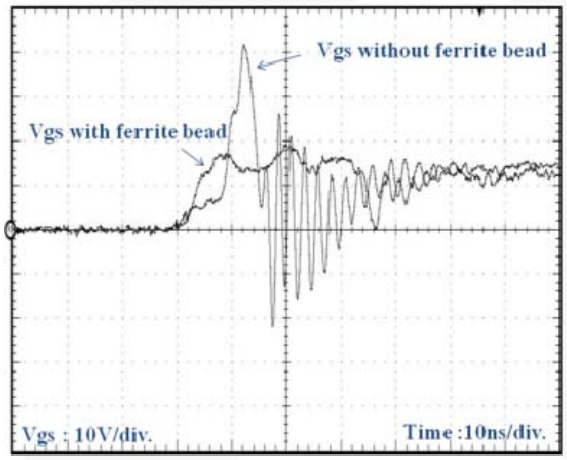

Figure 13. Gate Ringing of Super-Junction MOSFET; V_{GS} at Turn-On Transient

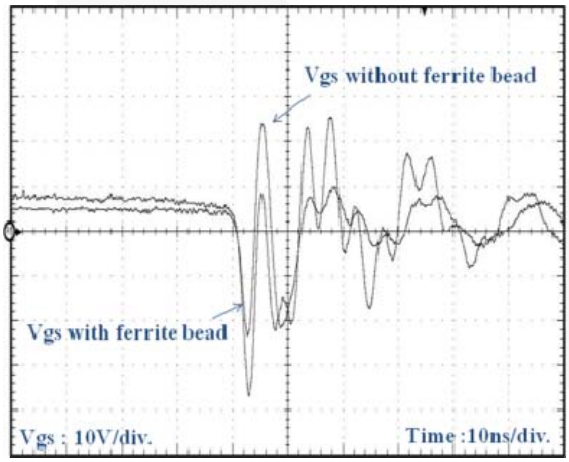

Figure 14. Gate Ringing of Super-Junction MOSFET; V_{GS} at Turn-Off Transient

Effect of Current Capability of Driver IC

The driver is the interface between the control circuit and the power MOSFET. The drive circuit amplifies the control signals to required levels to drive the power MOSFET and provides electrical isolation, when required, between the power MOSFET and the logic level control circuit, such as high-side switches on bridge topologies. The primary function of a driver is to switch a MOSFET from off state to on state and vice versa. High peak currents are needed in high-power applications so the parasitic capacitances can be charged or discharged as quickly as possible to switch MOSFETs efficiently. The switching behavior and power dissipation are dependent on current capability of the output driver, while the MOSFET gate-source voltage is between the threshold level and Miller plateau voltage. Table 1 shows the comparisons of peak sink and source current capability of drive ICs.

Table 1. Comparisons of Critical Specifications of Gate Drivers

Device	Condition	I_{PK_SINK}	I_{PK_SOURCE}
FAN3122T	C_{LOAD}=1.0 µF, f=1 kHz, V_{DD}=12 V	11.4 A	-10.6 A
FAN3224T	C_{LOAD}=1.0 µF, f=1 kHz, V_{DD}=12 V	5.0 A	-5.0 A
FAN3111C	C_{LOAD}=1.0 µF, f=1 kHz, V_{DD}=12 V	1.4 A	-1.4 A

Figure 15 - Figure 18Figure 25 show how much switching losses can be reduced with a high-current driver. The gaps in switching losses are not significant with a big gate resistor because it limits gate current.

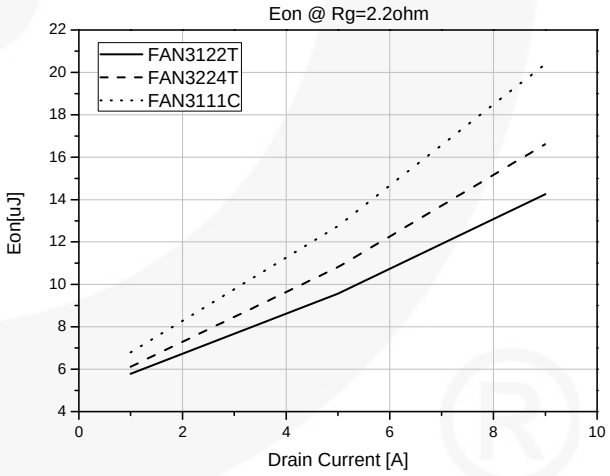

Figure 15. Turn-On Energy Loss (E_{ON}) vs. Gate Drivers with R_g=2.2 Ω

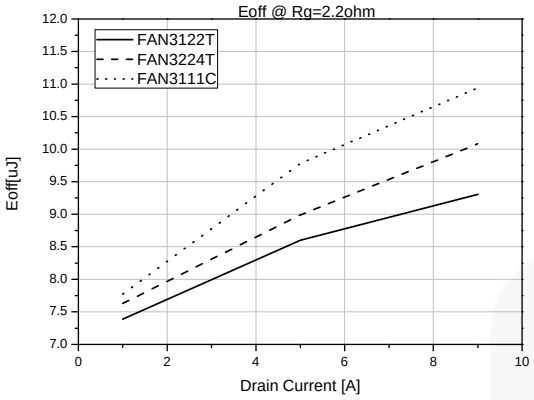

Figure 16. Turn-Off Energy Loss (E_{OFF}) vs. Gate Drivers with R_g=2.2 Ω

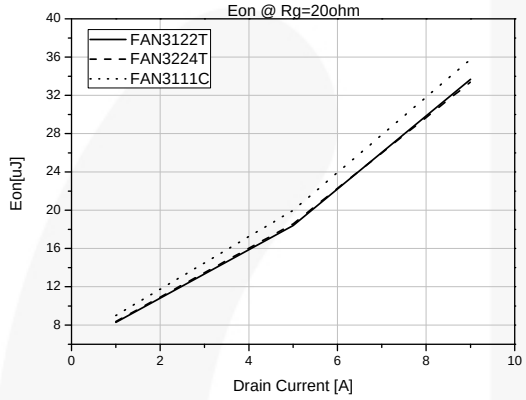

Figure 17. Turn-On Energy Loss (E_{ON}) vs. Gate Drivers with R_g=20 Ω

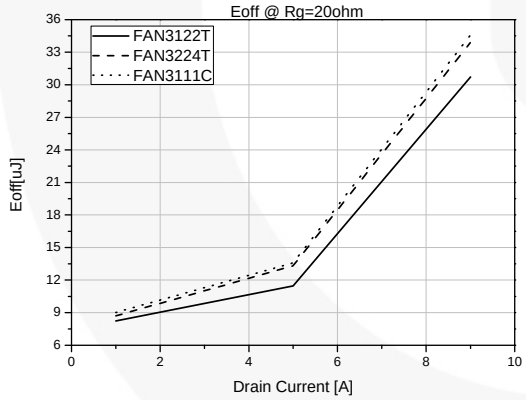

Figure 18. Turn-Off Energy Loss (E_{OFF}) vs. Gate Drivers with R_g=20 Ω

Effect of Source Inductance

Two different cases of common-source inductance are considered in an interleaved CRM PFC circuit because switching behaviors must be balanced with the common source inductance. Figure 19 presents a single phase of a two-phase interleaved CRM PFC circuit considering common source inductance. A circuit with a low value for L_s has lower turn-off switching loss and lower gate oscillation in spite of a little higher gate-source negative voltage and higher overshoot of drain-source voltage due to fast slew rate. On the contrary, another circuit with high L_s value shows much higher turn-off switching loss, higher gate oscillation, and lower overshoot of drain-source voltage due to slow slew rate, as shown in Figure 20 - Figure 25. The extremely fast switching speed of super-junction MOSFETs can lead to severe voltage and current ringing during switching due to the parasitic components of the interconnects. In applications, these interconnects generally consist of printed circuit board, component leads, cables and wires, etc. The problems that the interconnects cause are often dominated by stray inductance rather than by stray capacitance, especially in low- and medium-voltage power supplies. The best way to reduce switching noise is to minimize the common source inductance.

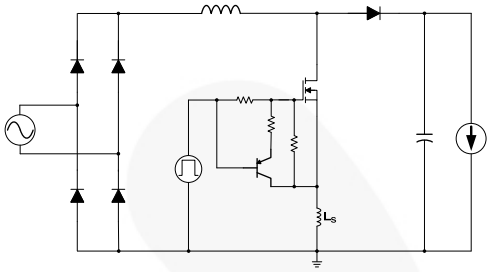

Figure 19. Single-Phase of Interleaved CRM PFC Considering Common Source Inductance

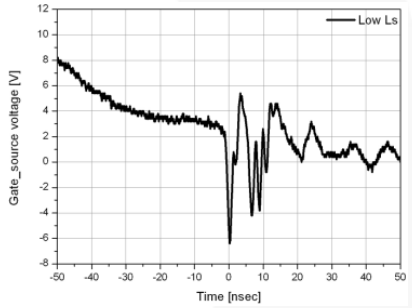

Figure 20. V_{gs} Waveform for Low L_S

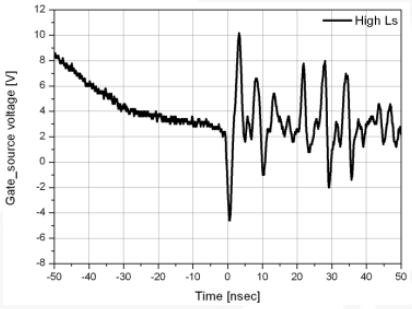

Figure 21. V_{gs} Waveform for High L_S

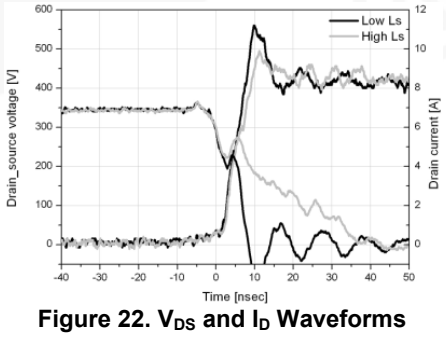

Figure 22. V_{DS} and I_D Waveforms

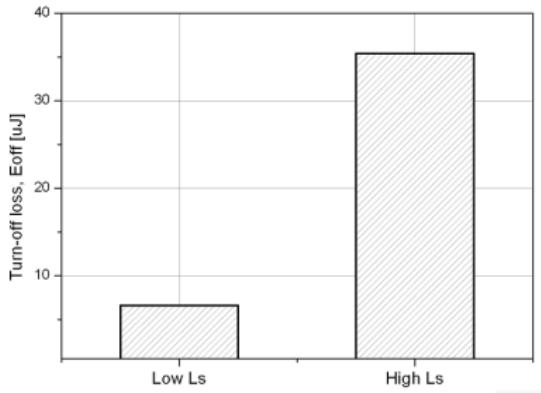

Figure 23. Turn-Off Loss

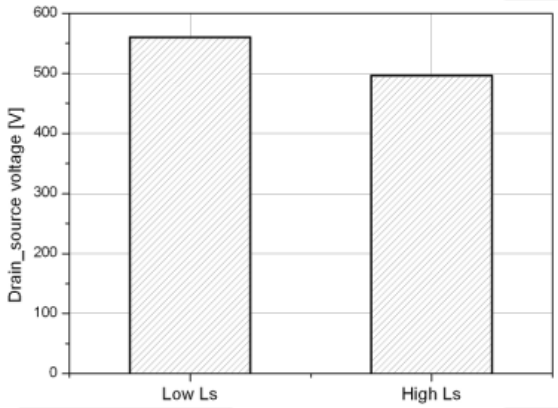

Figure 24. Peak Drain Source Voltage

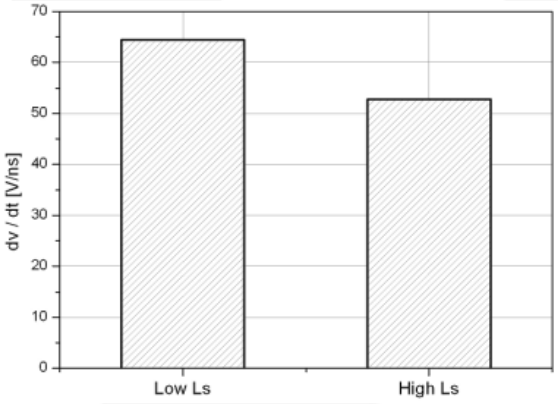

Figure 25. Slew Rate dv/dt

Effect of Gate Drive Circuit

The most important means of avoiding oscillation is minimizing the inductances, which are the long traces between gate driver and the gate.

A configuration of gate drive circuitry is also important to switching characteristics. In Figure 26, four types of gate drivers are considered. One is a PNP transistor turn-off circuit (Circuit A) that is most popular for minimizing loop and fast turn-off. As shown in the following figures, it shows lower gate oscillation and lower turn-off loss, but a little higher overshoot of drain-source voltage. A diode turn-off speed up circuit (Circuit B) has lower gate oscillation than Circuit A, but the discharge current of the MOSFET flows through off-resistor of totem-pole in gate driver IC so it has slower switching speed, higher turn-off loss, and lower overshoot of drain-source voltage. Circuit D is a compensated circuit that has reduced series resistance, R_{OFF}=5.6 Ω to achieve the same total series resistance as Circuit A. It has higher gate oscillation and higher turn-off loss. Circuit C is a driving circuit considering longer turn-on and off path than circuit A. It has higher gate oscillation. L_{P1} and L_{P2} are each parasitic inductance for turn-on and off path. To achieve the best performance for gate oscillation, it is important to connect the driver-stage ground directly to the source pin of the MOSFET as closely as possible. In this way, it is possible to reduce gate oscillation caused by parasitic components at turn-off transient. Considering all the above results, the PNP transistor turn-off circuit (Circuit A) is the best configuration for reduced gate oscillation and switching loss.

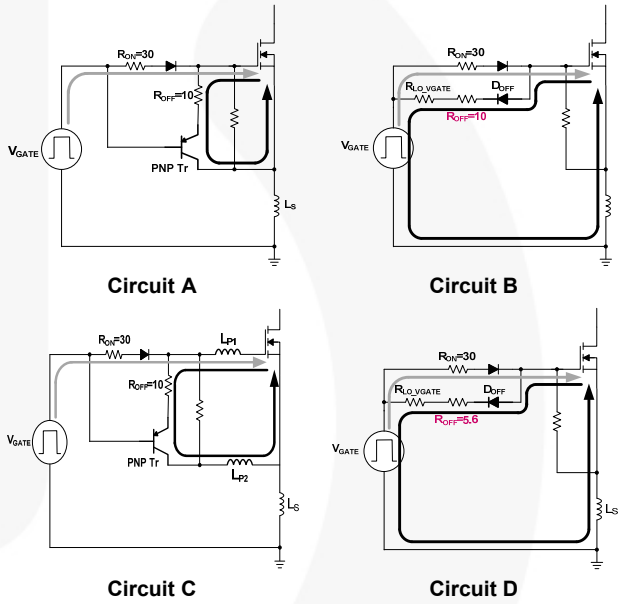

Figure 26. Gate Driving Circuits

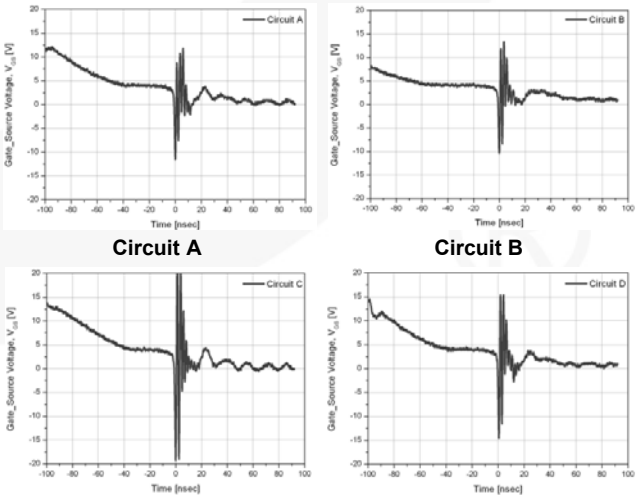

Figure 27. Turn-Off Gate-Source Voltage

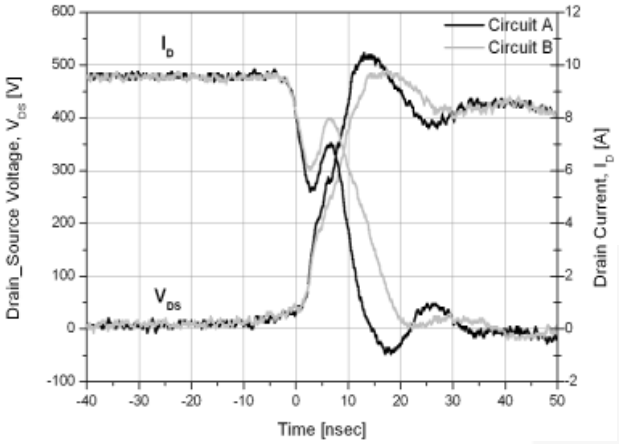

Figure 28. Circuit A & B Turn-Off Drain Current and Drain-Source Voltage

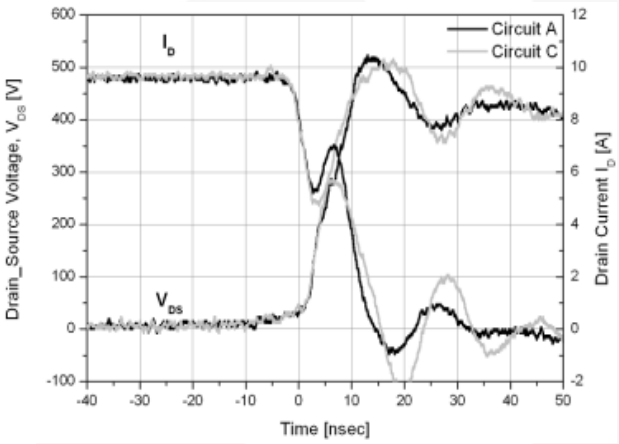

Figure 29. Circuit A & C Turn-Off Drain Current and Drain-Source Voltage

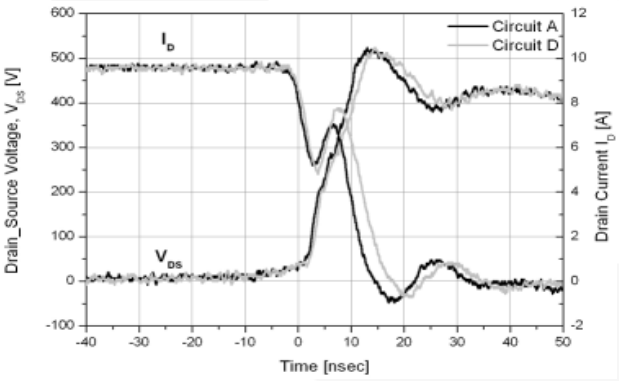

Figure 30. Circuit A & D Turn-Off Drain Current and Drain-Source Voltage

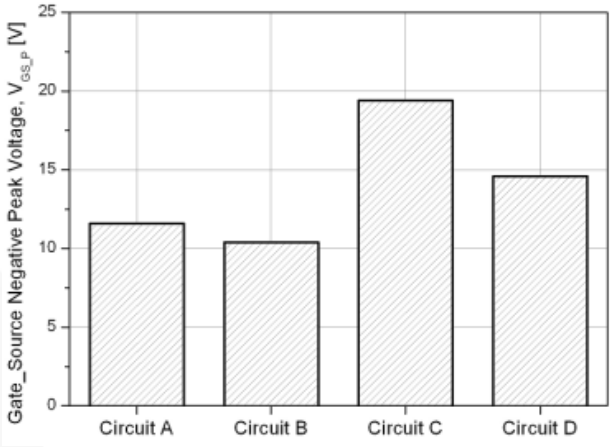

Figure 31. Gate-Source Negative Voltage

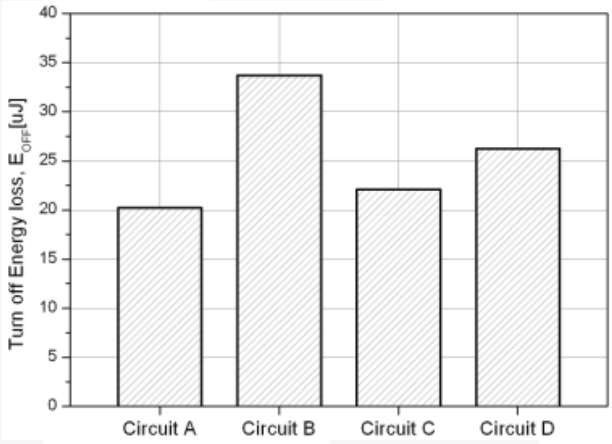

Figure 32. Turn-Off Loss

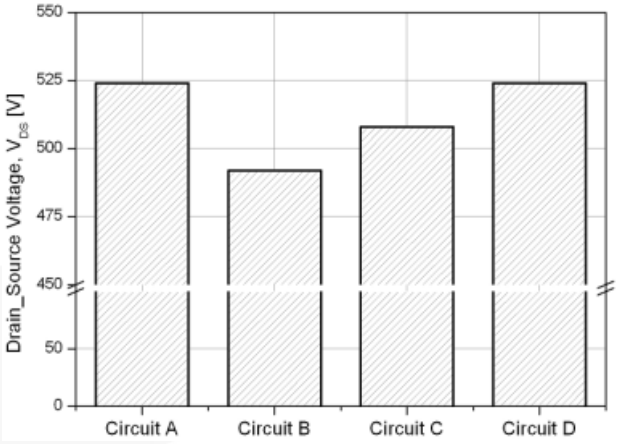

Figure 33. Drain-Source Voltage

Practical Layout Requirements

Measurement Technique

If an oscilloscope is used to measure noise, there are several precautions that must be taken. First, it's important to realize that a probe, even just a simple piece of wire, is potentially a very complex circuit. For DC signals, a probe appears as a simple conductor pair with some series resistance and a terminating resistance. However, for AC signals, the picture changes dramatically as signal frequencies increase, as shown Figure 34. Since the ground lead is a wire, it has some amount of distributed inductance, as shown Figure 35. A ground lead approximately 10 cm long clips to the ground of the circuit and a spring-loaded barrel on the probe hooks on the test point. This inductance interacts with the probe capacitance to cause ringing at frequency determined by the L and C values. This ringing is unavoidable and may be seen as a sinusoid of decaying amplitude that is impressed on pulses. The effects of ringing can be reduced by designing probe grounding so that the ringing frequency occurs beyond the bandwidth limit of the probe or oscilloscope system. To avoid grounding problems, it is important to always use the shortest ground lead. Substituting other means of grounding can cause ringing to appear on measured pulses. It is best to use the oscilloscope on its maximum bandwidth for these measurements to ensure seeing all waveforms of devices. Taking full advantage of the oscilloscope's measurement capabilities requires a probe that matches the oscilloscope's design considerations.

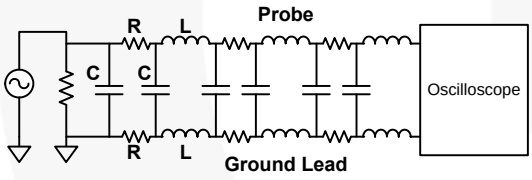

Figure 34. Equivalent Circuit of Probe for AC Signal

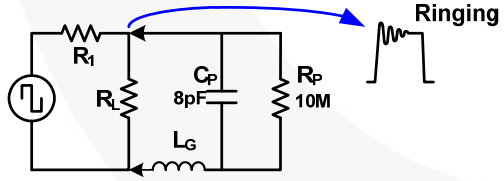

Figure 35. Effect of Ground Lead of the Probe

Figure 36 shows the standard oscilloscope probe test leads. A ground lead approximately 10 cm long clips to the ground of the circuit and a spring-loaded barrel on the probe hooks on the test point. Figure 38 shows comparison waveforms of gate according to probe setup. There is 26 V peak-to peak gate-source voltage. Figure 37 shows the same oscilloscope probe with a proper setup for low gate oscillation measurements. Both the probe barrel and the ground lead have been removed from the probe. There is 11.2 V peak-to-peak gate-source voltage. It is best to use the oscilloscope on its maximum bandwidth for these measurements. Ground lead of probe must be directly connected to the source of switching device, not the ground of bulk capacitance.

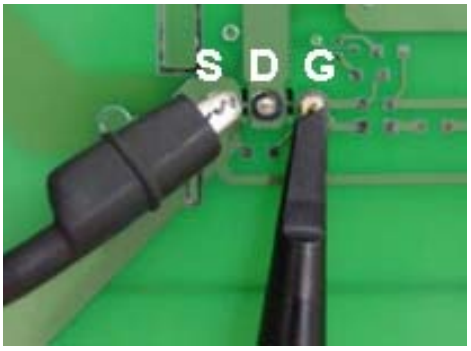

Figure 36. Measurement with Standard Setup

Figure 37. Measurement with Probe Tip and Ground Lead Removed

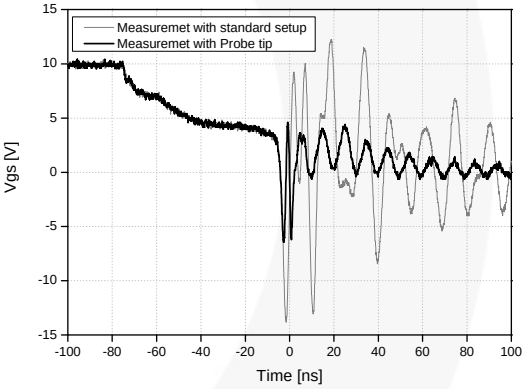

Figure 38. Comparison Measured Oscillation According to Probing Methods

Package & Layout Parasitics

To drive fast-switching super-junction MOSFETs in different applications, it is also necessary to understand the influence of the package on switching performance for the MOSFET. This is well documented in the low-voltage MOSFET arena.

Low $R_{DS(on)}$ and low inductive packages are a must for low-voltage packages to achieve best switching performance and reduced conduction losses for highest efficiency. The super-junction MOSFETs are mainly used in the voltage range of 500-600 V. In these voltage ratings, clearance and creepage distance requirements must be considered. For this reason, the most popular packages are industry standard TO-220, TO-247, TO-3P, and TO-263.

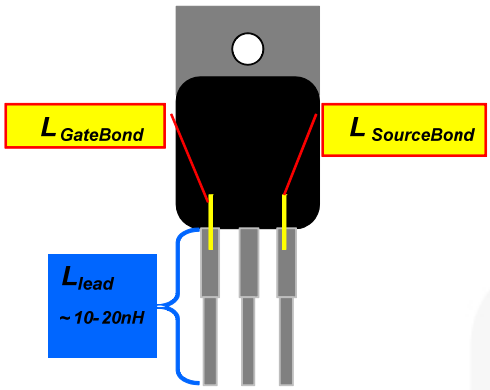

Figure 39. Several Parasitics in TO-220 Package

The impact of the package on performance is limited due to the fact that the internal gate and source bonding wire length are fixed. Only the length of the lead can be changed to reduce the source inductance of the package. Typical lead inductance of 10 nH, as shown in Figure 40, doesn't look like much, but a turn-off a current with di/dt=500 A / µs is easily possible with these MOSFETs. The voltage across this inductance is V_{IND} = 5 V and, with a turn-off di/dt of 1000 A / µs, the induced voltage is V_{IND} = 10 V. This short calculation shows that the complete source inductance, not only the lead inductance of the package, must be reduced to acceptable value. Low-inductance shunt resistors are mandatory.

Another source of noise is layout parasitic. Two types are visible: parasitic inductance and parasitic capacitance. Both parasitics influence the performance of the layout. As mentioned before, 1 cm of trace pitch has an inductance of 6-10 nH, which can be reduced by adding one layer on the topside of the PCB and a GND plane on the bottom side of the PCB. The other type is the parasitic capacitances. Figure 40 shows the principles of capacitive layout parasitics. The capacitance between one trace is immediately over the other trace or GND plane on the other side of the PCB. The second one is the capacitance built up between the device and the GND plane. Two parallel traces on both sides of PCB increase capacitance, but also reduce the inductance of the loop, resulting in less magnetic noise radiation.

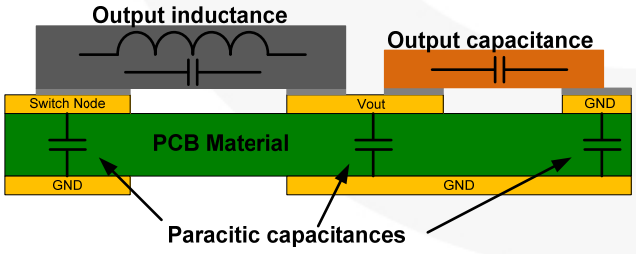

Figure 40. Capacitive Layout Parasitics

Oscillation Circuits

Figure 41 shows observed oscillation waveforms in a PFC circuit during turn-off transient of a super-junction MOSFET. In such a case, increasing gate resistance dampens down the peak drain-source voltage and prevents gate oscillation caused by lead inductance and parasitic capacitances of the super-junction MOSFET.

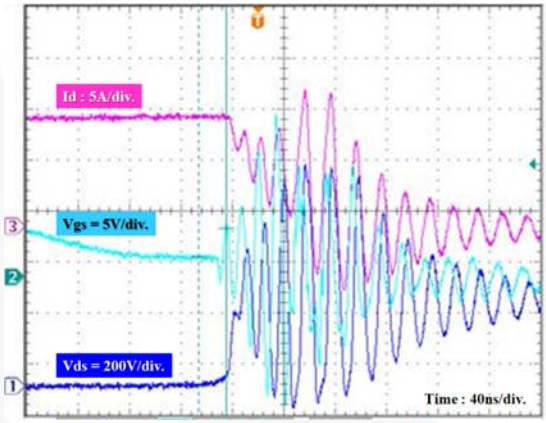

Figure 41. Capacitive Layout Parasitics

From a general perspective, there are several oscillation circuits that affect the switching behavior of the MOSFET, including internal and external oscillation circuits. Figure 42 shows a simplified schematic of a PFC circuit with both internal parasitics of a power MOSFET and an external oscillation circuits given by the external couple capacitance $C_{gd\_ext.}$ of the board layout. Parasitic components in the devices and boards involve switching characteristics more as the switching speed is increased. In Figure 42; L, C_o, and D_{boost} are the inductor, output capacitor, and boost diode. C_{gs}, C_{gd_int}, and C_{ds} are parasitic capacitances of the power MOSFET. L_{d1}, L_{s1}, L_{g1} are the drain, source, and gate wire bonding and lead inductances of the power MOSFET. R_{g_int} and R_{g_ext} are the internal gate resistors and the external gate driving resistors. $C_{gd\_ext.}$ is the parasitic gate-drain capacitance. L_D, L_S, and L_G are the drain, source, and gate copper trace stray inductances of the printed circuit board. Gate parasitic oscillation occurs in a resonant circuit by gate-drain capacitance, C_{gd}, and gate lead inductance, L_{g1}, when the MOSFET is turned on and off. When the resonance condition ($\omega L = 1/\omega C$) occurs, an oscillation voltage much larger than drive voltage $V_{gs(in)}$ is generated in V_{gs} between the gate and source because the voltage oscillation due to resonance changes in proportion to the selectivity $Q(=\omega L/R = 1/\omega CR)$ of the resonant circuit in Figure 43. The voltages across the capacitor and inductor, V_C and V_L, are given by Equations (2) and (3):

$$V_c = \frac{1}{2\pi fC} = \frac{1}{\omega CR} = Q \cdot V \tag{2}$$

$$V_L = 1 \cdot 2\pi fL = \frac{V \cdot \omega CL}{R} = Q \cdot V \tag{3}$$

where $Q = \frac{\omega L}{R} = \frac{1}{\omega CR}$

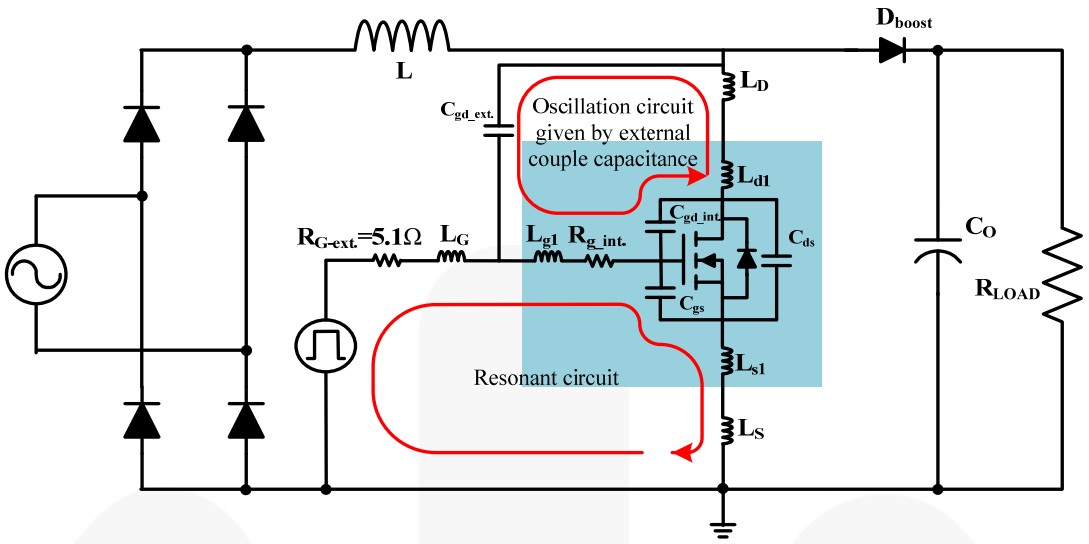

Figure 42. Simplified Schematic of PFC Circuit with Internal and External Parasitics of Power MOSFET

Oscillation voltage in drain-source of the MOSFET passes through gate-drain capacitance, C_{gd}, due to load wiring inductance L_D when MOSFET switching speed increases. When it is turned off, a resonant circuit with gate lead inductance L_{g1} is formed. As the gate resistor is extremely small, oscillation circuit Q becomes large and, when the resonance condition occurs, a large oscillation voltage is generated between that point and C_{gd} or L_{g1} and parasitic oscillation is caused. Furthermore, the voltage drop across L_S and L_{s1}, which can be represented by Equation (4), is caused by negative drain current in turn-off transient. This voltage drop across stray source inductances generates oscillation in gate-source voltage. The parasitic oscillation can cause gate-source breakdown, bad EMI, large switching losses, losing gate control, and even MOSFET failures.

$$\Delta V_{GS} = (L_S + L_{s1}) \cdot \frac{di_d(t)}{dt} \quad (4)$$

From a general perspective, there are several oscillation circuits that affect the switching behavior of the MOSFET, including internal[6][7] and external oscillation circuits. Figure 42 shows a simplified schematic for a power MOSFET with internal parasitic capacitances and external oscillation circuits given by the external couple capacitance C_{GDEXT} of the board layout. This external couple capacitance affects the V_{GS} slope during turn-off of the power MOSFET. To see how this external C_{GD} affects the switching behavior, compare it in different layouts. Both layouts are single-layer designs. For the measurements, both boost stages are running with single transistor.

The measurements were taken in a PFC boost stage at the same input voltage of V_{IN}=180 V_{AC} and output power level of P_{OUT}=300 W. The difference in oscillations is shown in Figure 44 and Figure 45. V_{GS} (green line) and V_{DS} (magenta line) are during turn off. The experimental waveforms show the effect of the high and low external C_{gd} in a given layout.

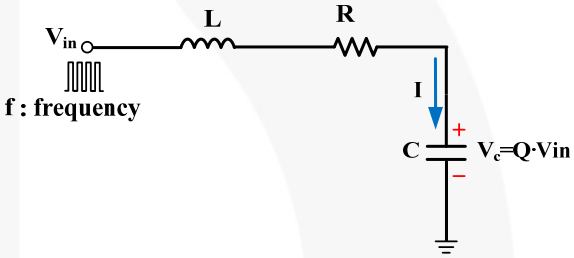

Figure 43. Resonant Circuit of R, L, and C

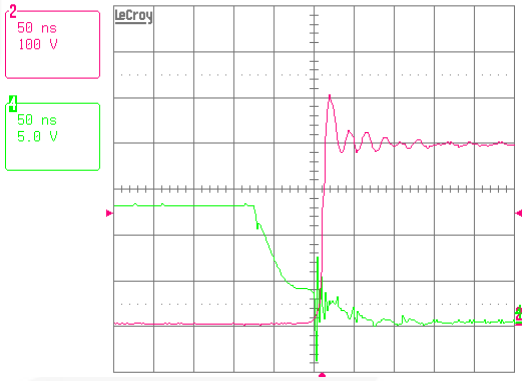

Figure 44. Turn-Off with High C_{GD_EXT}

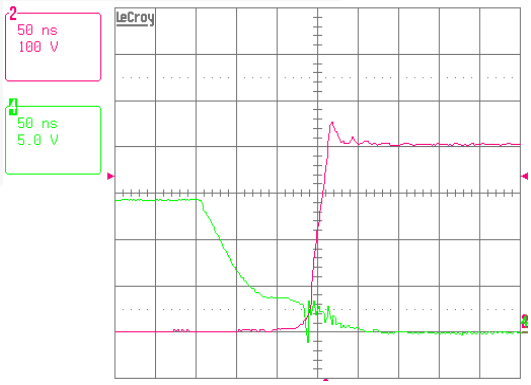

Figure 45. Turn-Off with Low C_{GD_EXT}

The oscillation effect can be forced by increasing the output power level or decreasing the input voltage at the same output power. This can also occur after an AC line drop out: when line voltage is back, the boost stage charge up the bulk capacitor to nominal voltage. During this time, when the MOSFET turns off, the drain current is quite high. The drain current commutates to the output capacitance, C_{oss}, of the MOSFET and charges it up to DC bus voltage. The voltage slope is proportional to the load current and inversely proportional to the value of the output capacitance. The value of C_{OSS} is high at low V_{DS} and low at high V_{DS}. As a result, dv/dt values of drain-source voltage change during turn-off. The high dv/dt values lead to capacitive displacement currents due to all the parasitic capacitances. Together with all the layout and parasitic inductance and capacitances, an LC oscillation circuit is only damped by the internal R_g. Under certain conditions, e.g. transient at input voltage or short-circuit conditions, high di/dt and dv/dt occur and this leads to unusual switching behavior or damaged devices. Nevertheless, with optimized layout and mechanical structure of the whole application, fast switching super-junction MOSFETs help to improve efficiency and power density.

Layout Requirements

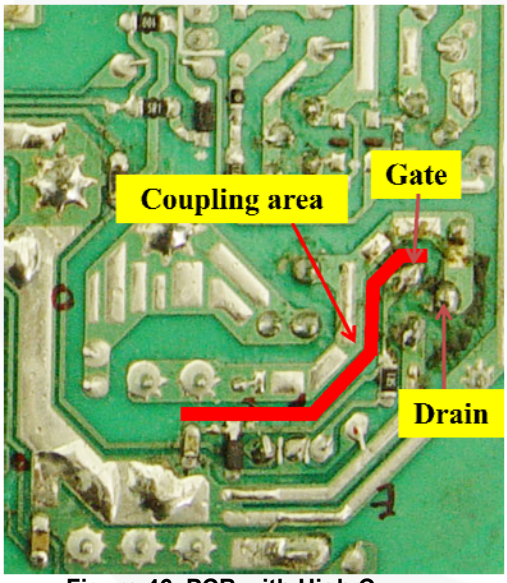

Figure 46. PCB with High C_{GD_EXT}

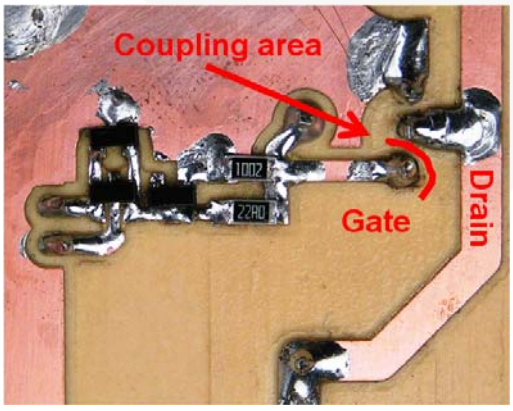

Figure 47. PCB with Low C_{GD_EXT}

External C_{gd} is one of the root causes for ringing affected by the device and PCB layout. External C_{gd} must be reduced as much as possible to reduce gate oscillation. Experimental waveforms according to PCB layout are shown in Figure 46 and Figure 47. Figure 48 - Figure 51 show layouts with high external C_{gd} and low external C_{gd}.

The capacity between traces can be calculated with:

$$C = \frac{\varepsilon_o \cdot \varepsilon_r \cdot A}{d} \quad (5)$$

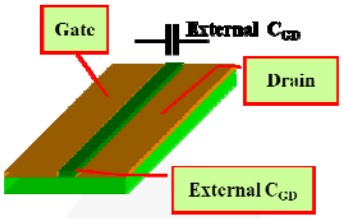

Figure 48. Single Layer Layout Example with Increased External C_{gd}

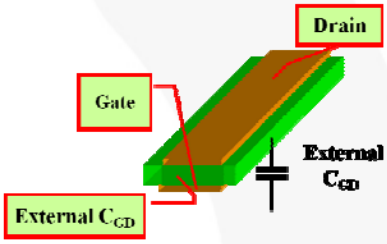

Figure 49. Double Layer Layout Example with Increased External C_{gd}

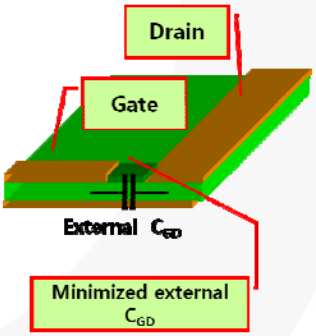

Figure 50. Single Layer Layout Example with Reduced External C_{GD}

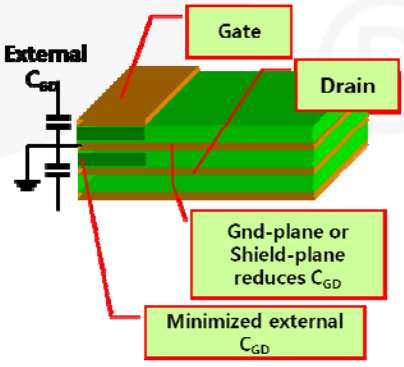

Figure 51. Double Layer Layout Example with Reduced External C_{GD}

Compare to Figure 50 and Figure 51, which show layout solutions with reduced external C_{gd}. Inductances and current loops have an influence on performance in a given application. Currents are only running in a loop and these currents create a magnetic field. If a change in the current occurs, the magnetic field changes and creates an inductive voltage, V_{IND}. With Faraday's law, the value of V_{IND} can be calculated as:

$$V_{ind} = -\frac{d\phi}{dt} = -L\frac{di}{dt} \; with \; \phi = \int_A B \cdot dA = L \cdot I \qquad (6)$$

Therefore, L depends also on the geometry of the loop. The bigger the area of the current loop, the larger inductance L. If the change in the current (di/dt) is stable, but higher inductance comes from the current loop, V_{IND} increases. Enclosed current loops with high di/dt values should be minimized. The source inductance and shunt resistor inductance must be minimized to avoid worse EMI and switching behaviors. For example, a 1 cm track on a PCB is almost same with 6-10 nH inductive impedance.

Layout Guidelines for Fast SJ MOSFETs

- To achieve the best performance of Super-Junction MOSFETs, optimized layout is required.
- Gate driver and R_g must be placed as close as possible to the MOSFET gate pin.
- Separate POWER GND and GATE driver GND.
- Minimize parasitic C_{gd} capacitance and source inductance on PCB
- For paralleling super-junction MOSFETs, symmetrical layout is mandatory.
- Slow down dv/dt, di/dt by increasing R_g or using a ferrite bead

Conclusion

As power conversion efficiency becomes more and more critical, technology of discrete devices advances every day. Extremely fast-switching super-junction MOSFETs are an essential choice for higher efficiency, but more challenging to control than previous generations. Optimized gate driver and board layout are the most important design parameters when working with fast switching MOSFETs. Practical design tips allow designers to take advantage of the features of super-junction MOSFETs.

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