AN-5233
Consideration of Power MOSFETs in Fast Charger Design

Abstract

The demand for battery capacitance up to 10,000 mAh in mobile devices is steadily increasing as devices consume more power and offering more functionality. Large battery capacity provides longer battery run-time, but needs more time to charge. This application note describes how to decrease charge time and the impact of power MOSFET selection, including a practical design example. The one serial and three parallel (1S3P) 9,700 mAh Li-Ion battery is used and 1C and 0.5C rates are set to measure charging and discharging time, respectively. Products that require large battery capacitance and fast charging time include tablet / notebook docking stations, portable music players, and commercial electronic Point-of-Sale (POS) systems.

Introduction

Capacity Rate(C-Rate)

In describing batteries, charge or discharge current is often expressed as a C-rate. The C-rate means a discharge rate relative to the capacity of a battery in an hour. A rate of 1C means an entire 3000 mAh battery is discharged in one hour at a discharge current of 3 A. A 0.5C rate indicates a discharge current of 1.5 A. The battery charging time of common Constant Current / Constant Voltage (CC/CV) mode depends on C-rate of CC Mode.

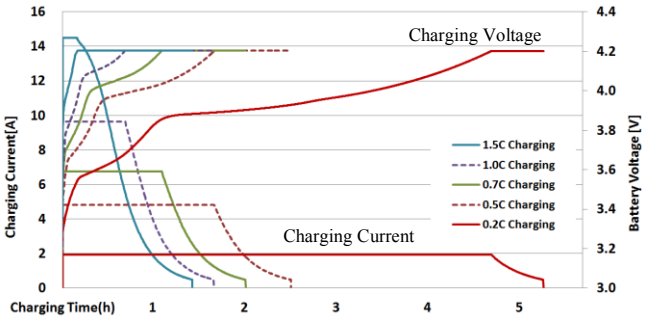


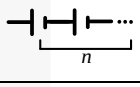
Figure 1. Battery Charging Time Comparison by C-Rate (9,700 mAh, 1S and 0.05C Cut-off Charging)

For the example Li-ion battery charging shown in Figure 1, the 1C-rate charging for 9,700 mAh shortens charging time by four (4) hours compared to the 0.2 C-rate case. For designing a fast charger, a high C-rate charging is essential.

Cell Connection: Serial vs. Parallel

Battery cells can be connected in series or parallel to achieve high capacity. Connection of cells determines battery pack voltage, C-rate, and charging time by constant current (CC). Table 1 shows several advantages of serial and parallel connection. The trend of mobile applications is forward 1S and parallel connection because 1S achieves lower system voltage, resulting in high DC-DC conversion efficiency, and parallel increases battery capacity.

Table 1. Advantages of Serial and Parallel Connection

Connection	Advantages
Serial 	High-voltage output for high-power system Short charging time Low charging current
Parallel 	Low-voltage output for low-power system High charging current Low voltage rated components

A typical charger design consists of bi-directional MOSFETs to prevent inrush current and reverse current blocking at the front-end, high-side, and low-side MOSFETs (Q_{HS}, Q_{LS}) for step down and battery switch (Q_{BATT}) to provide the charge and discharge path for the battery pack, as illustrated in Figure 2.

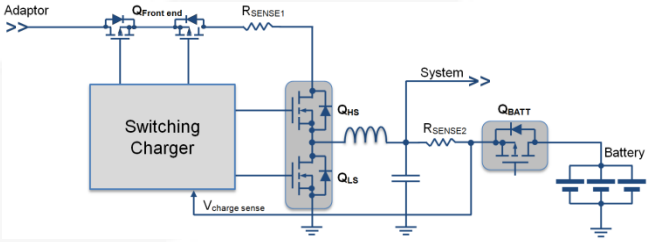


Figure 2. Charger Design Example for 1S3P Battery

The DC-DC buck converter for 1S battery charging is chosen to cover a wide input range, up to 12 V_{IN} and 4.2 V battery voltage with CC/CV Mode. It offers small form factor with optimal passive elements at a high frequency. The next section considers selecting power MOSFETs for high efficiency and power density for fast charger design.

Design of Fast Charger

Synchronous Buck Regulator MOSFETs

Selection of the high-side MOSFET is critical to achieve maximum efficiency because of the narrow duty cycle of 12 V_{IN} to 4.2 V_{OUT}. As a general rule, the high-side MOSFET can be selected at the sweet spot of key parameters where conduction loss is almost equal to switching loss. Figure 3 shows the simulated power loss distribution of five MOSFETs with different $R_{DS(ON)}$ and Q_G values under the condition of 12 V_{IN}, 4.2 V_{OUT}, 380 kHz, 12 A I_{OUT}. Device B shows the lowest power loss, but has higher Q_G than Device C and D and higher $R_{DS(ON)}$ than Device A. Device C shows balanced power losses between conduction and switching[1], but the total loss is larger than Device B.

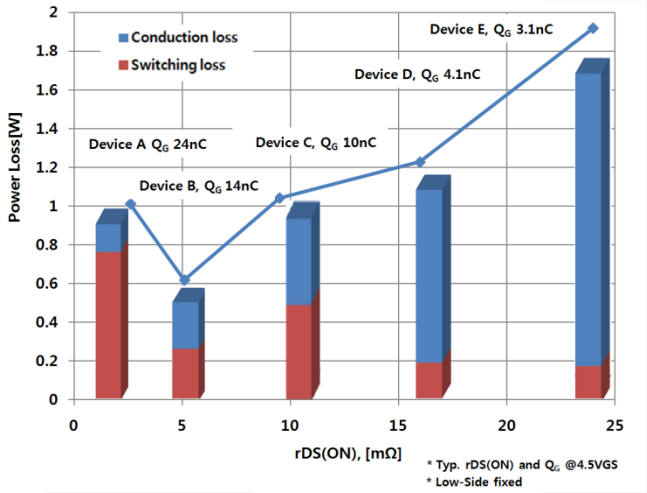


Figure 3. Power Losses of High-Side MOSFET by $R_{DS(ON)}$ and Q_G

Power losses of the high-side MOSFET can be estimated by Equations (1) and (2). Charger designers should consider MOSFET AC parameters, such as $Q_{G(SW)}$ and $V_{Plateau}$ since the most switching losses occur at the MOSFET gate-to-drain charge (Q_{GD}) and discharge state. Compared to the high-side MOSFET, the low-side MOSFET turns on and off at Zero Voltage Switching (ZVS) mode and results in very small loss. For this reason, the choice of low-side MOSFET is mainly determined by conduction loss, $R_{DS(ON)}$. A good starting point for low-side $R_{DS(ON)}$ is to select half of the high-side MOSFET's value, considering the light and heavy load current range.

$$P_{COND} = {I_{OUT}}^2 \times rDS_{(on)} \times \frac{V_{OUT}}{V_{IN}} \quad (1)$$

$$P_{SW} = \frac{V_{IN} \times I_{OUT}}{2} \times Fsw \times (t_{S(L-H)} + t_{S(H-L)}) \quad (2)$$

where, $t_{S(L-H)} = \frac{Q_{G(sw)} \times (R_{DRV(pull-up)} + R_{GATE})}{V_{DRV} - V_{plateau}}$;

$t_{S(H-L)} = \frac{Q_{G(sw)} \times (R_{DRV(pull-dn)} + R_{GATE})}{V_{plateau}}$;

$Q_{G(SW)}$: $Q_{GD} + Q_{GS2}$
(Q_{GS2}: Gate charge from V_{th} to Q_{GD} start point);

R_{GATE}: Gate resistance;

$V_{plateau}$: Plateau voltage at C_{GD} recharge period;

V_{DRV}: Gate driving voltage;

$R_{DRV(pull-up)}$: Gate driver pull-up resistance; and

$R_{DRV(pull-dn)}$: Gate driver pull-down resistance.

Battery Power Path MOSFET

On the charger output side, a P-channel MOSFET, called the "battery switch" is used for linear mode operation to regulate low charging voltage during "trickle" charge mode for a deeply discharged battery. Some of charger designs do not consider the battery switch voltage drop caused by a high charging current that affects the battery charging voltage (*see Figure 2*). Since most charger ICs read the battery voltage at the point in front of the battery switch, P-MOSFET, a high voltage drop can increase charging time.

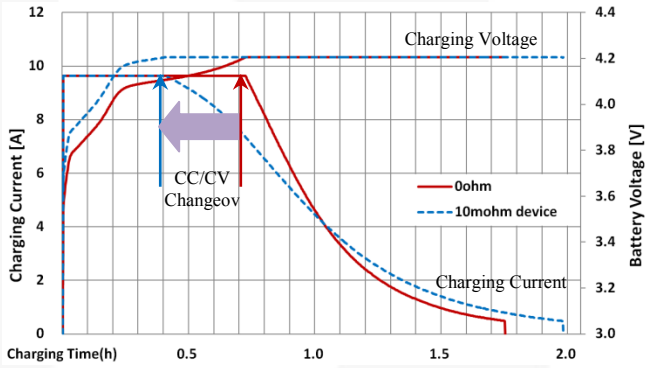


Figure 4. Charging Time Effect by Battery Switch $R_{DS(ON)}$ Variation (9700 mAh, 1C Charging)

Figure 4 shows charging time variations by the battery switch $R_{DS(ON)}$ at high charging current, 9.7 A. For example, a 10 mΩ battery switch increases charging time by 15 minutes (14%) longer to fully charge the single 9,700 mAh, Li-ion battery cell because the MOSFET voltage drop moves the CC / CV changeover point earlier and increases the charging time.

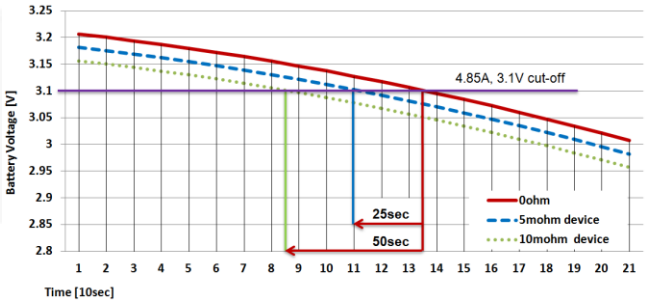


Figure 5. Discharging Cut-Off Time Comparison by Battery Switch $R_{DS(ON)}$ Variation (9700 mAh, 0.5C Discharging)

The battery switch affects battery run-time. The discharging voltage drop of battery switch moves the discharging cut off time earlier. From Figure 5, at the condition of 4.85 A linear discharging current and 3.1 V cut off, the 5 mΩ and 10 mΩ P-channel MOSFET reduce the battery run-time by 25 s and 50 s, respectively, compared to the ideal zero $R_{DS(ON)}$ switch. The battery switch $R_{DS(ON)}$ must be as lower as possible to reduce charging time and lengthen battery run-time.

Package

Package size and thermal performance tend to be a trade off when selecting power MOSFETs. Three different packages: MLP3.3x3.3, Power33 (asymmetrical N-dual), and MLP2x2 are shown in Figure 6. The package needs to be chosen by carefully considering a given charging and discharging current *(refer to the 0)*.

MLP3.3x3.3 (21.78mm²) **Power33 (9mm²)** **MLP2x2 (8mm²)**

Figure 6. MOSFET Size Comparison

Evaluation Board

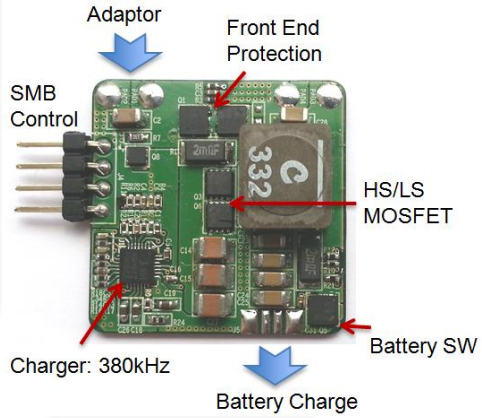


Figure 7. Board Example(30x30 mm, 1T, 6-Layer)

Figure 7 shows the 10 A rating single-cell battery pack charger design using typical synchronous buck topology shown in Figure 2. For the practical charger design; small size inductor, MLCC capacitor of input and output capacitors, and 380 kHz switching frequency are selected. Table 2 is the charger design specification for fast charging.

Table 2. Evaluation Board Specification

Item	Specification
Adaptor Voltage	12 V
Charging Voltage	4.192 V (1S)
Charging Current	~12 A
Front-End MOSFET	FDMC6679AZ
HS&LS MOSFET	FDMC7678 x 2 ea
Battery Switch MOSFET	FDMC510P
Inductor	3.3 µH (I_{SAT}=26 A, DCR Max.=7.92 mΩ, 10x11x6 mm)
Current-Sense Resistor	2 mΩ x 2 ea
Input Capacitor	33 µF MLCC x 3 ea
Output Capacitor	47 µF MLCC x 6 ea
Charger IC	380 kHz NVDC Charger
PCB	30x30 mm, 1T, 6 layers, 2 oz
Test Condition	25°C, Natural Convention

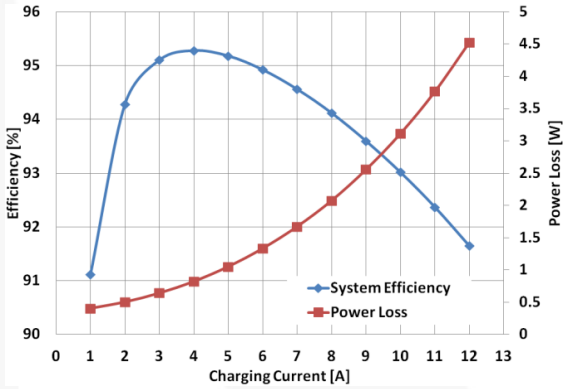


Figure 8. Efficiency vs. Constant Charging Current

Figure 8 shows the efficiency and power loss. This charger design performed 93% board efficiency at 10 A charging current and 95.3% maximum at 4 A.

Figure 9 and Figure 10 are MOSFET thermal performance of high-side and low-side MOSFETs and battery switch. The high-side and low-side MOSFETs showed 94.3°C and the battery switch showed 87.1°C at 10 A charging current.

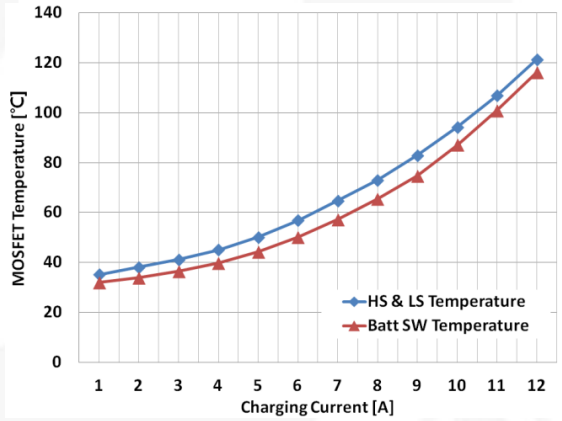


Figure 9. MOSFET Temperature of HS/LS & Battery Switch (1 A Step, 2 Min. Soak)

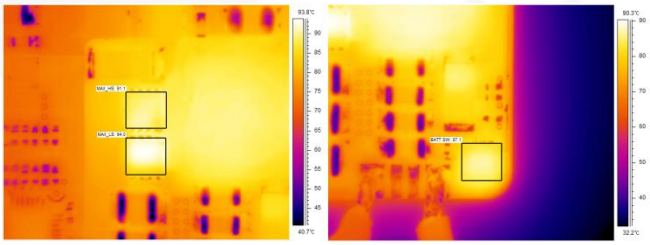


Figure 10. Thermal Snap Shots of HS/LS MOSFET & Battery Switch at 10 A Charging

Conclusion

A high-current charger system design for a parallel-connected, large-capacity Li-ion battery has been demonstrated. It must consider high-side power loss distribution between conduction and switching loss to achieve maximum efficiency. Using equations, charger designers can estimate the MOSFET loss distribution based on conduction and switching losses ratio, rather than only considering $R_{DS(ON)}$ or selecting power MOSFETs. In terms of the battery switch, voltage drop at high current moves a CC / CV changeover point earlier and the charging time increases. On the other hand, it reduced discharging time in discharging mode. In fast charger design, it is important that low power loss MOSFET selection of DC-DC buck for high-current charging and the low-$R_{DS(ON)}$ battery switch to charge to maintain long constant current period.

Table 3. Power MOSFETs for Fast Charger Design

Location	Ratings	~ 5 A	~7 A	~10 A
Front-End P-Channel	**FSID**	FDMA530PZ		FDMC6679AZ
	Package	MLP 2x2		MLP 3.3x3.3
	V_{DS}/V_{GS}	30/25 V		30/25 V
	$R_{DS(ON)}$ Max. at V_{GS}=10 V	35 mΩ		10 mΩ
High-Side & Low-Side N-Channel	**FSID**	FDMA8878	FDMC8200S	FDMC7678
	Package	MLP 2x2	MLP3x3 Dual N	MLP 3.3x3.3
	V_{DS}/V_{GS}	30/20 V	30/20 V	30/20 V
	$R_{DS(ON)}$ Max. at V_{GS}=10 V	16 mΩ	20/10 mΩ	5.3mΩ
	Q_g Typ. at V_{GS}=10 V	8.5 nC	7.3/15.7 nC	28 nC
Battery Switch P-Channel	**FSID**	FDMA908PZ	FDMC510P	FDMC610P
	Package	MLP 2x2	MLP 3.3x3.3	MLP 3.3x3.3
	V_{DS}/V_{GS}	12/8 V	20/8 V	20/8 V
	$R_{DS(ON)}$ Max. at V_{GS}=4.5 V	12.5 mΩ	8 mΩ	3.7 mΩ

References

[1] *AN-6005- Synchronous buck MOSFET loss calculations with Excel model*

Related Datasheets

FDMA530PZ — -30V Single P-Channel PowerTrench® MOSFET
FDMC6679AZ — -30V P-Channel Power Trench® MOSFET
FDMA8878 — 30V Single N-Channel Power Trench® MOSFET
FDMC8200S — 30V Single N-Channel Power Trench® MOSFET
FDMC7678 — 30V N-Channel PowerTrench® MOSFET
FDMA908PZ — -12V Single P-Channel PowerTrench® MOSFET
FDMC510P — -20V P-Channel PowerTrench® MOSFET