

HW 4

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1.

(a) sd, ld, beg
(since they need immediate)

(b) add, beg

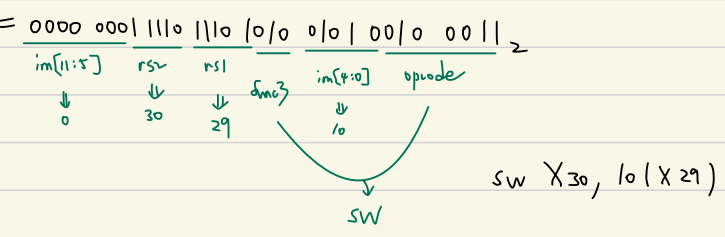
(c) Branch
MemRead
RegWrite

0 when run sd X13, 0(X12)

If Branch = 1, $PC + 4 \rightarrow PC + imm$, and $\because imm = 0$, $PC = PC + 0$ leads to infinite loop. If MemRead = 1, then MemRead, MemWrite are 1, then memory will read/write, based on $X12 + 0$ address output ReadData. And $\because RegWrite = 1$, ReadData will be written into Register File, but $\because imm[1:0] = 0$, and $X0$ is not writable, so it will not have any effect.

2.

01EEA523₁₆



(a) Branch: 0
MemRead: 0
MemtoReg: X
ALUOp: 00
MemWrite: 1
ALUSrc: 1
RegWrite: 0

(b) Reg[29], 10₁₀ (= 0000 0000 0000 000A_{hex})

3.

(a) "add" is the least time consuming one, it need 600 ps.

add: 25 + 235 + 130 + 15 + 170 + 15 + 10
PC Read I-Mem Register File Mux ALU Writing Mux Register Setup
= 600 ps

ld: 25 + 235 + 130 + 170 + 235 + 15 + 10
PC Read I-Mem Register File ALU D-Mem Mux Register Setup
= 820 ps

sd: 25 + 235 + 130 + 170 + 235 = 795 ps
PC Read I-Mem Register File ALU D-Mem

beg: 25 + 235 + 130 + 170 + 15 + 15 + 5 + 10
PC Read I-Mem Register File ALU Mux Mux Single Gate Register Setup
= 605 ps

(b) 820 ps

Since minimum clock period should be able to execute every instruction, and the longest instruction which is "ld" takes 820 ps, so the clock period should be 820 ps.

4.

Original time

$$\frac{1200 \times 4}{4 \times 10^9} \text{ (sec)}$$

$$= 12 \times 10^{-9} \text{ (sec)}$$

improved time

$$\# \text{ of clocks} = 1200 + 4$$

$$= 1204$$

$$\frac{1204}{2 \times 10^9} = 602 \times 10^{-9}$$

$$\text{speedup} = \frac{12 \times 10^{-9}}{602 \times 10^{-9}}$$

$$\approx 0.0199 \times 10^2$$

$$= 1.99 \#$$

5.

(a) RAW

① add X29, X6, X7
sub X30, X28, X29

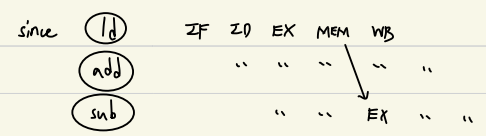
RAW

② sub X30, X28, X29
sd X30, 0(X11)

load-use

③ ld X28, 4(X5)
....
sub X30, X28, X29

(b) No since load-use hazard will not occur.



so no hazard that will require the pipeline to stall.

(c)

ld x28, 4(x5)	IF	ID	EX	MEM	WB	
add x29, x6, x11	IF	ID	EX	MEM	WB	
stall			X	X	X	X
stall				X	X	X
sub x30, x28, x29				IF	ID	EX
stall					X	X
stall						X
sd x30, 0(x11)					IF	ID

4 NOPs #

7.

(1+4)
(a) 11 clock cycles, No #

beg x11, x12, Label
sd x15, 0(x23)
ld x15, 0(x24)
add x11, x6, x12
NOP
NOP
sub x11, x13, x12

若新增 NOP 指令, 因 NOP 位於記憶體內, 故在 fetch NOP 時, 也會有 structural hazard。

∴ NO #

(b) beg x11, x12, Label
add x11, x6, x12
sub x11, x13, x12
sd x15, 0(x23)
ld x15, 0(x24)

9 cycles (5+4) #

(c) $\frac{(4+4+4)}{(2+4+4)} = 1.2 \#$

if determined in ID, should add 1 NOP between beg, sd
if " " MEM, " " 3 NOPs " beg, sd

(d) The original result takes $5+5-1=9$ cycles.
The new result with only 4 stages takes
 $5+4-1=8$ cycles. speedup = $\frac{9}{8} = 1.125 \#$

(e) The clock period of original pipelined process is 220.
The new pipelined process has a clock period of
 $\max(220, 180) + 25 = 245$. The speedup is $\frac{220 \times 9}{245 \times 8}$
 $\approx 1.0102 \#$

6.

(a)

always - not - taken
 $accuracy = \frac{5}{8} = 0.625 = 62.5 \%$

always - taken
 $accuracy = \frac{3}{8} = 0.375 = 37.5 \%$

(b) starts at T

Ground truth	NT	T	T	NT	NT	NT	NT	T
State	T	NT	T	T	NT	NT	NT	NT
Decision	T	NT	T	T	NT	NT	NT	NT
Correctness	X	X	✓	X	✓	✓	✓	X

$accuracy = \frac{4}{8} = 50 \%$

(c)

Ground truth	NT	T	T	NT	NT	NT	NT	T
State	ST	WT	ST	ST	WT	WN	SN	SN
Decision	T	T	T	T	T	NT	NT	NT
Correctness	X	✓	✓	X	X	✓	✓	X

ST : Strongly predict taken
WT : Weakly predict taken
WN : Weakly predict not taken
SN : Strongly predict not taken

$accuracy = \frac{4}{8} = 50 \%$

8.

	IF	ID	EX	MEM	WB
Cycle 1	add X12, X6, X5	-	-	-	-
Cycle 2	sub X10, X11, X12	add X12, X6, X5	-	-	-
Cycle 3	beg X11, X12, label	sub X10, X11, X12	add X12, X6, X5	-	-
Cycle 4	sd X11, 0(X12)	beg X11, X12, label	sub X10, X11, X12	add X12, X6, X5	-
Cycle 5	first instruction of the exception handler	NOP	NOP	sub X10, X11, X12	add X12, X6, X5