CS3120

Introduction of Integrated Circuit Design

Homework 2: Layout Design Q&A

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Outline

- Virtuoso
- Pre-sim
- DRC
- LVS
- PEX
- Post-sim
- Coding Style and Naming Rules
- Notice

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- **Virtuoso**
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Virtuoso

- Q1: The prompt window shows, “The cellView could not be opened for edit.”
- A1: The file is “locked” due to not properly closing icfb. To unlock the file, you need to close all icfb windows. Assuming your cell name is “inv” and the library you are using is “myLib”, you can look for a file named .cdslck in the path myLib/inv/ and delete it. After that, you should be able to open your file successfully.

Virtuoso

- Q2: Unit of the ruler?
- A2: microns.

Virtuoso

- Q3: WARNING: Failed to get a mfgGridResolution value from the tech file.
- A3: You can ignore the warning message, as it won’t affect in HW2.

Virtuoso

- Q4: How to flatten the subcircuit in layout?
- A4: You can find in menu bar -> edit -> hierarchy -> make cell…/flatten… to flatten the subcircuit in layout.

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Pre-sim

- Q1: Waveform didn’t turn out as expected and is not a logic error.
- A1: It is usually a syntax error.

Pre-sim

- Q2: What is the .cir file in the tutorial?
- A2: The .cir file is a circuit file you can include in your .sp file.
- In HW2, we provide 2 ways to complete your circuit
  - 1. yourcircuit.cir + pre_XOR.sp
  - 2. pre_XOR.sp
  - If using the first method, make sure to upload the .cir file.

Pre-sim

- Q3: Cannot create the .tr0 file after running pre-sim.
- A3: If it's not an issue with the option post settings, based on my experience, running it a few more times usually would create the .tr0 file. It could be a problem with HSPICE itself.

Pre-sim

- Q4: Can I construct the 3-bit XOR gate with several different subcircuits (subckts)?
- A4: Yes.

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DRC

- Q1: Cannot run DRC successfully.
- A1: Check out the settings in the tutorial. You don’t need to modify other settings. Make sure all paths and files are correctly set.

DRC

- Q2: Having missing port error.
- A2: Check if labels for VDD and GND are placed at the correct layers on the layout, and ensure that the corresponding metal layer's text layer is used. If the wrong layer is used, errors may occur.

DRC

- Q3: WARNING: Stamping conflict in SCONNECT – Multiple source nets stamp one target net. Use LVS REPORT OPTION or LVS SOFTCHK statement to obtain detailed information.
- A3: The warning refers to an incorrect connection caused by multiple labels on the same net in the circuit or an improper connection of the bulk, leading to a wrong connection (soft connect). You can check if the bulk is correctly connected.

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LVS

- Remember to select the right top cell.
- When running LVS, leave only the circuit information (.subckt) in .sp/.cir, and remove the simulation part (.lib, .option, .temp, .etc), so that LVS can only compare the circuit information part.

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PEX

- Q1: The port orders generated after PEX is different from pre-sim?
- A1: It is normal for the port order generated after PEX.

PEX

- Q2: .pex.netlist or .pex.cir?
- A2: Depends on the circuit defined in pre-sim.
  - 1. yourcircuit.cir + pre_XOR.sp in pre-sim:
    - hw2_XOR.pex.cir
    - hw2_XOR.pex.cir.HW2_XOR.pxi
    - hw2_XOR.pex.cir.pex
  - 2. pre_XOR.sp in pre-sim:
    - hw2_XOR.pex.netlist
    - hw2_XOR.pex.netlist.HW2_XOR.pxi
    - hw2_XOR.pex.netlist.pex

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Post-sim

- Q1: How to correctly run post-sim?
- A1: When running post-sim with the .sp file, remember to include the .cir or .netlist file after PEX. You should remove the original subcircuit definitions and calls from the circuit's original .sp file. Instead, include and call the subciruit defined in the .cir or .netlist file. Be mindful of the port order, as it needs to match the order defined in the .cir or .netlist.

Post-sim

- Q1: How to correctly run post-sim?
- A1: For example, with a .pex.cir file, you should include the corresponding .per.cir in the post-sim .sp file and call the subcircuits defined within the .pex.cir. Similarly, with a .pex.netlist, include the corresponding .pex.netlist in the post-sim .sp file and call the subcircuits defined within the .pex.netlist.

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Coding Style and Naming Rules

- You can define your own subcircuits. Make sure the final subcircuit is the same as the one shown in the coding style of the document.
- The port order of the post-sim can be different from the coding style in the document, since the netlist file created after PEX may not be the same as the one in pre-sim.

Coding Style and Naming Rules

- You need to design the circuit in HW2 based on the image in the document. Otherwise, the circuit won't be graded.
- Difference between HW2 and bonus:
  - HW2: based on the image in the document
  - Bonus: circuit different from HW2, using pass transistor, and has lower power

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Notice

- Remember to check the announcement in eeclass.
- Remember to check the updated document in eeclass. Make sure to hand out correct files.