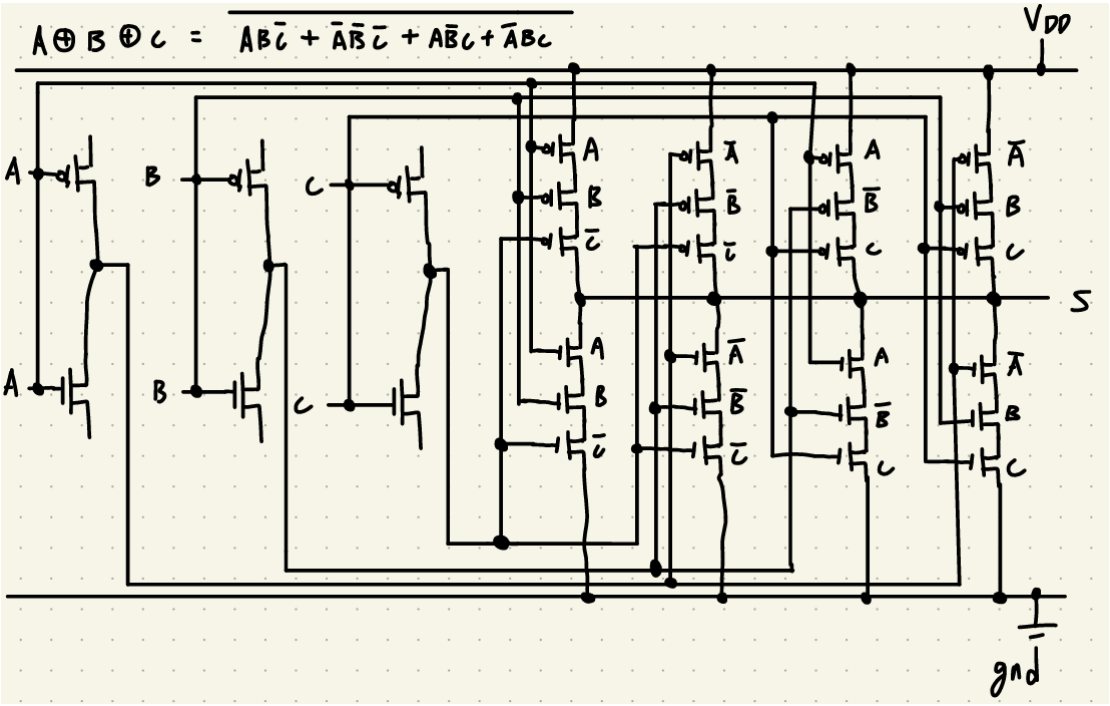
HW2_report

ID：111062107

Name：鄧弘利

目錄

1. The circuit diagram of your design and explaining your design



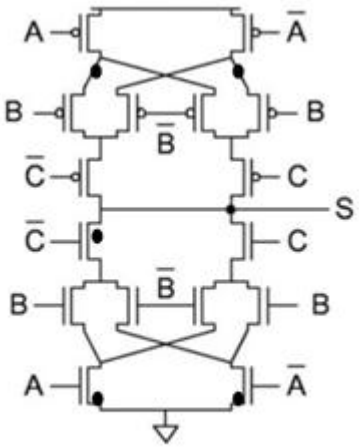
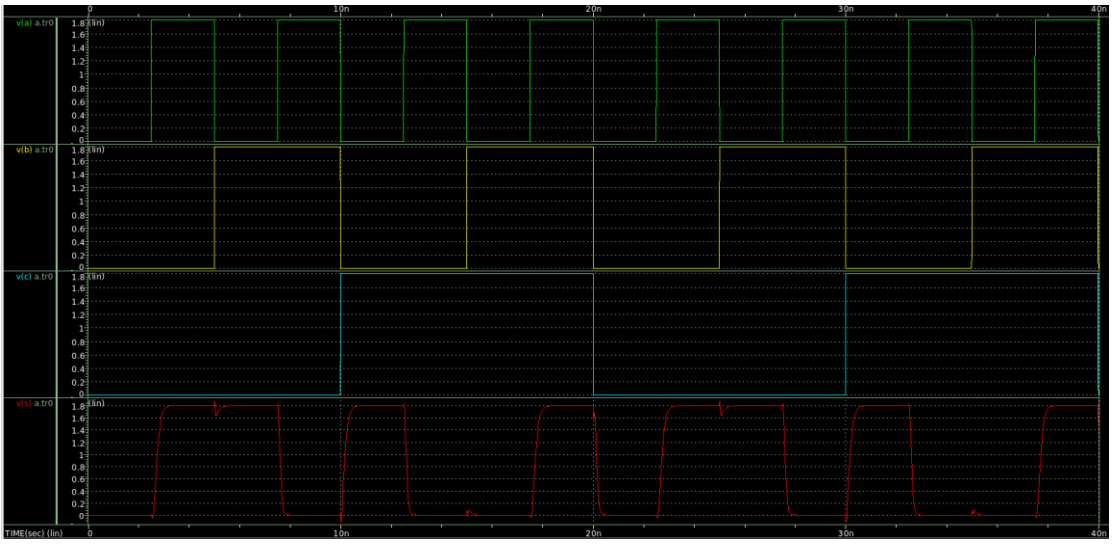


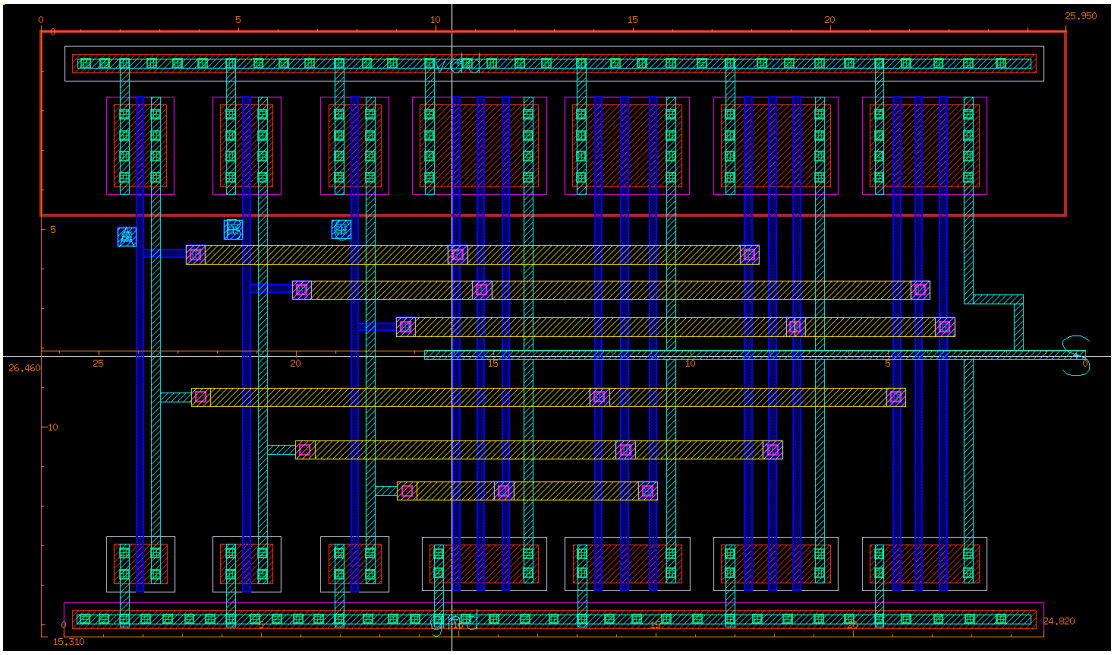
Fig. 1 3-input XOR gate

根據作業檔案界介紹裡面給的圖，我們可以知道在 n 跟 p 端，串接並聯的模式是一樣的，都是$AB\bar{C} + \bar{A}\bar{B}\bar{C} + A\bar{B}C + \bar{A}BC$，所以就可以做出這樣的 circuit diagram。

2. Pre-sim waveform

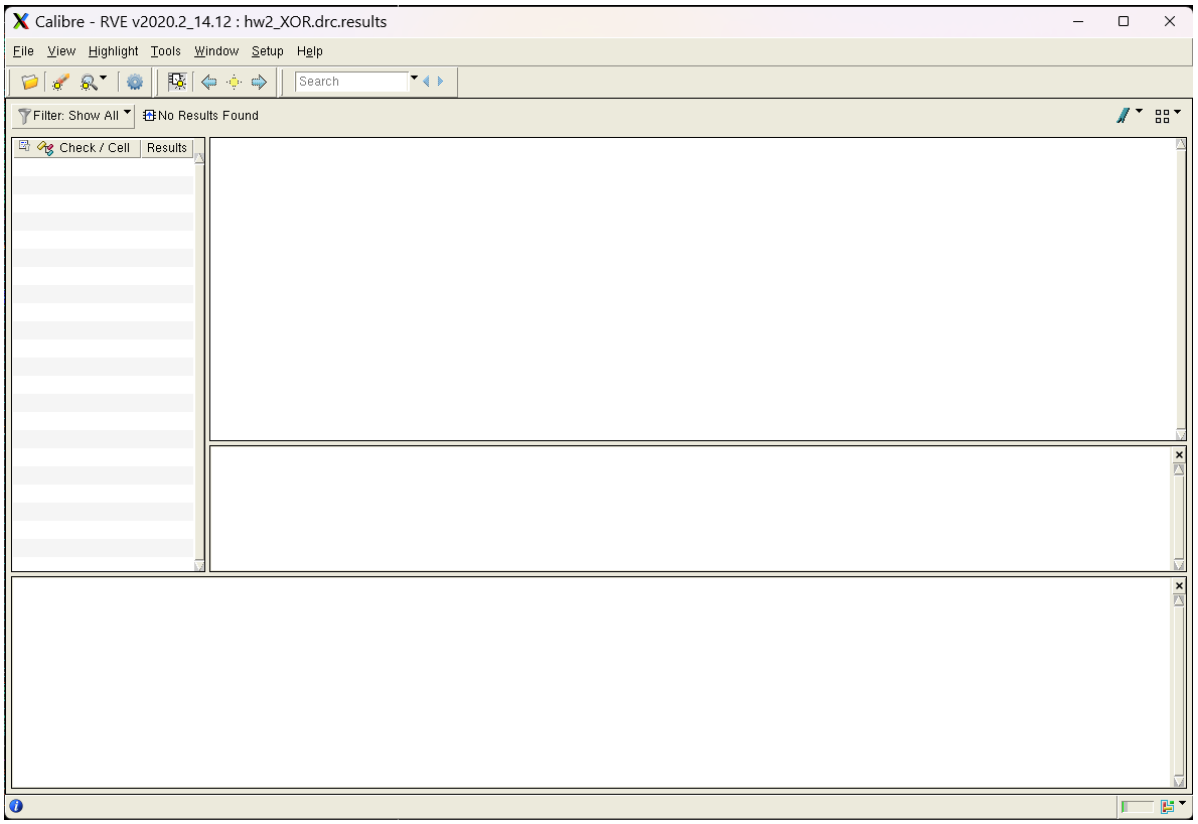


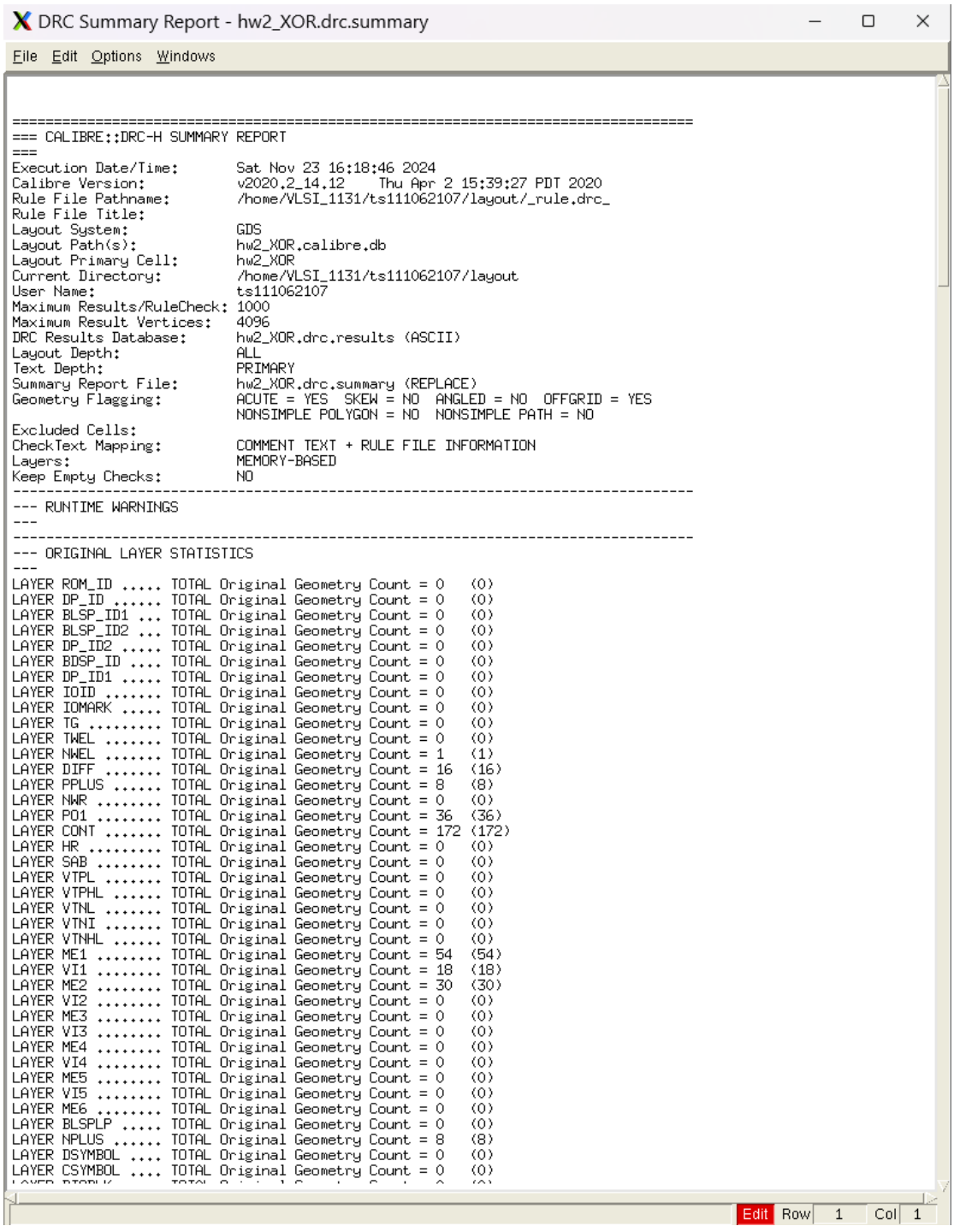
3. Screenshot of your layout (with total area measurement)



26.460 * 15.310

4. Screenshot of DRC summary report

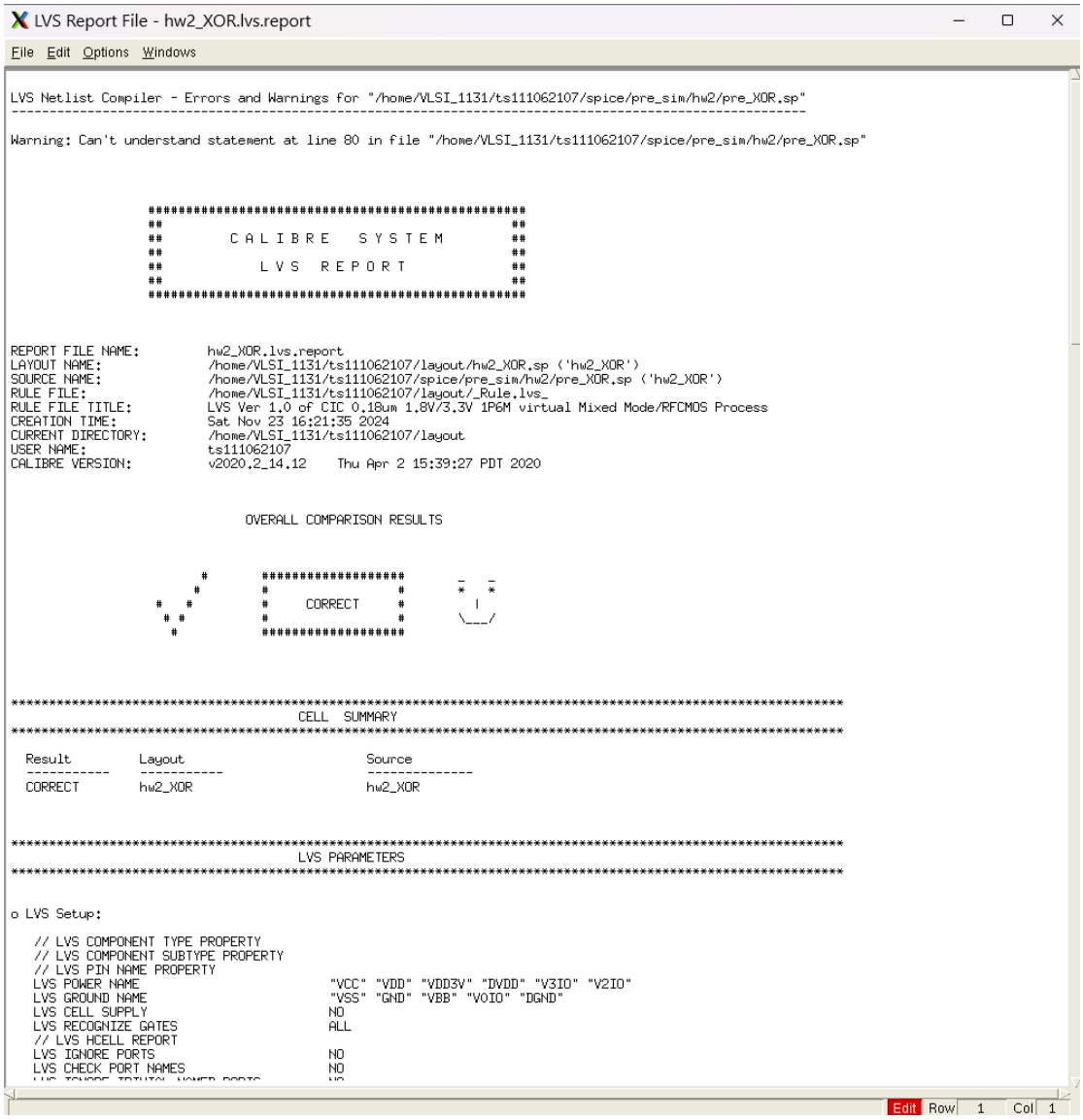





```
================================================================================
=== CALIBRE::DRC-H SUMMARY REPORT
===
Execution Date/Time:       Sat Nov 23 16:18:46 2024
Calibre Version:           v2020.2_14.12    Thu Apr 2 15:39:27 PDT 2020
Rule File Pathname:        /home/VLSI_1131/ts111062107/layout/_rule.drc_
Rule File Title:
Layout System:             GDS
Layout Path(s):            hw2_XOR.calibre.db
Layout Primary Cell:       hw2_XOR
Current Directory:         /home/VLSI_1131/ts111062107/layout
User Name:                 ts111062107
Maximum Results/RuleCheck: 1000
Maximum Result Vertices:   4096
DRC Results Database:      hw2_XOR.drc.results (ASCII)
Layout Depth:              ALL
Text Depth:                PRIMARY
Summary Report File:       hw2_XOR.drc.summary (REPLACE)
Geometry Flagging:         ACUTE = YES  SKEW = NO  ANGLED = NO  OFFGRID = YES
                           NONSIMPLE POLYGON = NO  NONSIMPLE PATH = NO
Excluded Cells:
CheckText Mapping:         COMMENT TEXT + RULE FILE INFORMATION
Layers:                    MEMORY-BASED
Keep Empty Checks:         NO
--------------------------------------------------------------------------------
--- RUNTIME WARNINGS
---
--------------------------------------------------------------------------------
--- ORIGINAL LAYER STATISTICS
---
LAYER ROM_ID ..... TOTAL Original Geometry Count = 0   (0)
LAYER DP_ID ...... TOTAL Original Geometry Count = 0   (0)
LAYER BLSP_ID1 ... TOTAL Original Geometry Count = 0   (0)
LAYER BLSP_ID2 ... TOTAL Original Geometry Count = 0   (0)
LAYER DP_ID2 ..... TOTAL Original Geometry Count = 0   (0)
LAYER BDSP_ID .... TOTAL Original Geometry Count = 0   (0)
LAYER DP_ID1 ..... TOTAL Original Geometry Count = 0   (0)
LAYER IOID ....... TOTAL Original Geometry Count = 0   (0)
LAYER IOMARK ..... TOTAL Original Geometry Count = 0   (0)
LAYER TG ......... TOTAL Original Geometry Count = 0   (0)
LAYER TWEL ....... TOTAL Original Geometry Count = 0   (0)
LAYER NWEL ....... TOTAL Original Geometry Count = 1   (1)
LAYER DIFF ....... TOTAL Original Geometry Count = 16  (16)
LAYER PPLUS ...... TOTAL Original Geometry Count = 8   (8)
LAYER NWR ........ TOTAL Original Geometry Count = 0   (0)
LAYER PO1 ........ TOTAL Original Geometry Count = 36  (36)
LAYER CONT ....... TOTAL Original Geometry Count = 172 (172)
LAYER HR ......... TOTAL Original Geometry Count = 0   (0)
LAYER SAB ........ TOTAL Original Geometry Count = 0   (0)
LAYER VTPL ....... TOTAL Original Geometry Count = 0   (0)
LAYER VTPHL ...... TOTAL Original Geometry Count = 0   (0)
LAYER VTNL ....... TOTAL Original Geometry Count = 0   (0)
LAYER VTNI ....... TOTAL Original Geometry Count = 0   (0)
LAYER VTNHL ...... TOTAL Original Geometry Count = 0   (0)
LAYER ME1 ........ TOTAL Original Geometry Count = 54  (54)
LAYER VI1 ........ TOTAL Original Geometry Count = 18  (18)
LAYER ME2 ........ TOTAL Original Geometry Count = 30  (30)
LAYER VI2 ........ TOTAL Original Geometry Count = 0   (0)
LAYER ME3 ........ TOTAL Original Geometry Count = 0   (0)
LAYER VI3 ........ TOTAL Original Geometry Count = 0   (0)
LAYER ME4 ........ TOTAL Original Geometry Count = 0   (0)
LAYER VI4 ........ TOTAL Original Geometry Count = 0   (0)
LAYER ME5 ........ TOTAL Original Geometry Count = 0   (0)
LAYER VI5 ........ TOTAL Original Geometry Count = 0   (0)
LAYER ME6 ........ TOTAL Original Geometry Count = 0   (0)
LAYER BLSPLP ..... TOTAL Original Geometry Count = 0   (0)
LAYER NPLUS ...... TOTAL Original Geometry Count = 8   (8)
LAYER DSYMBOL .... TOTAL Original Geometry Count = 0   (0)
LAYER CSYMBOL .... TOTAL Original Geometry Count = 0   (0)
```

```
--------------------------------------------------------------------------------
--- RULECHECK RESULTS STATISTICS (BY CELL)
---
--------------------------------------------------------------------------------
--- SUMMARY
---
TOTAL CPU Time:                  0
TOTAL REAL Time:                 0
TOTAL Original Layer Geometries: 343 (343)
TOTAL DRC RuleChecks Executed:   234
TOTAL DRC Results Generated:     0 (0)
```

5. Screenshot of LVS report include the message of passing LVS

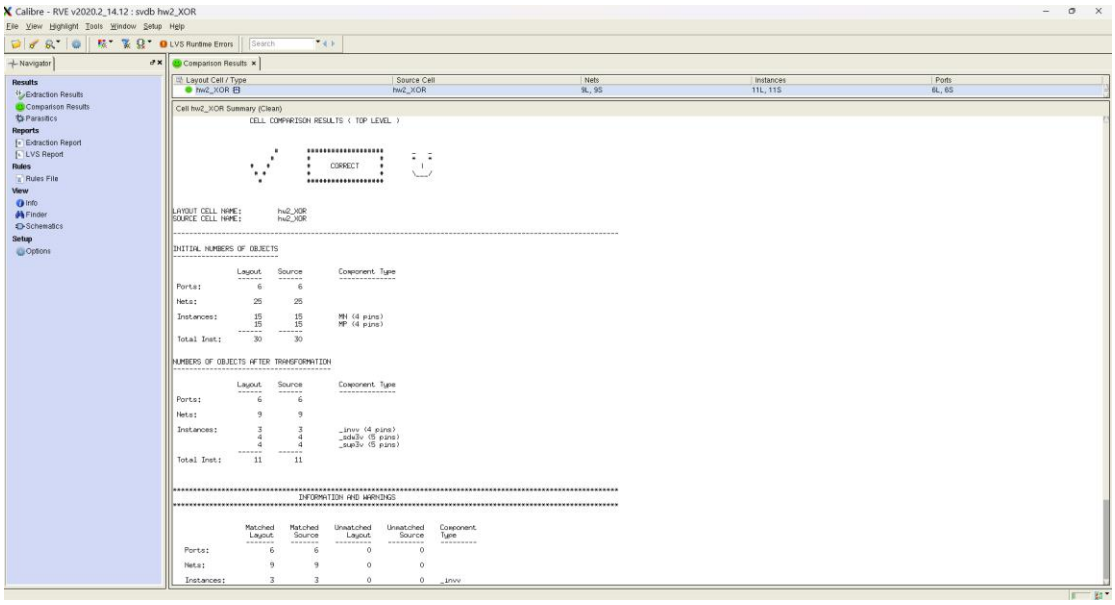


LVS Report File - hw2_XOR.lvs.report

File Edit Options Windows

```
LVS Netlist Compiler - Errors and Warnings for "/home/VLSI_1131/ts111062107/spice/pre_sim/hw2/pre_XOR.sp"
--------------------------------------------------------------------------------

Warning: Can't understand statement at line 80 in file "/home/VLSI_1131/ts111062107/spice/pre_sim/hw2/pre_XOR.sp"



                ################################################
                ##                                            ##
                ##        C A L I B R E   S Y S T E M         ##
                ##                                            ##
                ##            L V S   R E P O R T             ##
                ##                                            ##
                ################################################


REPORT FILE NAME:         hw2_XOR.lvs.report
LAYOUT NAME:              /home/VLSI_1131/ts111062107/layout/hw2_XOR.sp ('hw2_XOR')
SOURCE NAME:              /home/VLSI_1131/ts111062107/spice/pre_sim/hw2/pre_XOR.sp ('hw2_XOR')
RULE FILE:                /home/VLSI_1131/ts111062107/layout/_Rule.lvs_
RULE FILE TITLE:          LVS Ver 1.0 of CIC 0.18um 1.8V/3.3V 1P6M virtual Mixed Mode/RFCMOS Process
CREATION TIME:            Sat Nov 23 16:21:35 2024
CURRENT DIRECTORY:        /home/VLSI_1131/ts111062107/layout
USER NAME:                ts111062107
CALIBRE VERSION:          v2020.2_14.12    Thu Apr 2 15:39:27 PDT 2020


                        OVERALL COMPARISON RESULTS


                     #       ###################       _   _
                   #         #                 #       *   *
                 #   #       #     CORRECT     #         |
                  # #        #                 #       \___/
                   #         ###################


********************************************************************************************************************
                                        CELL  SUMMARY
********************************************************************************************************************

  Result         Layout                    Source
  -----------    ----------                --------------
  CORRECT        hw2_XOR                   hw2_XOR


********************************************************************************************************************
                                        LVS PARAMETERS
********************************************************************************************************************


o LVS Setup:

   // LVS COMPONENT TYPE PROPERTY
   // LVS COMPONENT SUBTYPE PROPERTY
   // LVS PIN NAME PROPERTY
   LVS POWER NAME                          "VCC" "VDD" "VDD3V" "DVDD" "V3IO" "V2IO"
   LVS GROUND NAME                         "VSS" "GND" "VBB" "VOIO" "DGND"
   LVS CELL SUPPLY                         NO
   LVS RECOGNIZE GATES                     ALL
   // LVS HCELL REPORT
   LVS IGNORE PORTS                        NO
   LVS CHECK PORT NAMES                    NO
```

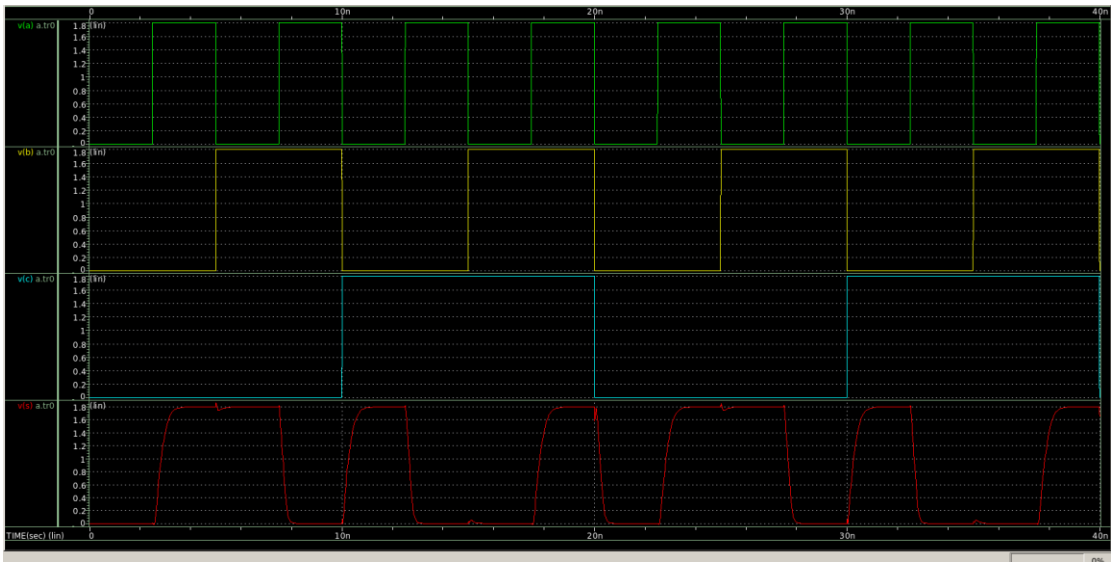
Edit Row 1 Col 1



Calibre - RVE v2020.2_14.12 : svdb hw2_XOR

```
*****************************************************************************************************
                                INFORMATION AND WARNINGS
*****************************************************************************************************

                  Matched     Matched     Unmatched    Unmatched    Component
                   Layout      Source       Layout       Source       Type
                  -------     -------     ---------    ---------    ---------
   Ports:               6           6            0            0
   Nets:                9           9            0            0
   Instances:           3           3            0            0    _invv
                        4           4            0            0    _sdw3v
                        4           4            0            0    _sup3v
                  -------     -------     ---------    ---------
   Total Inst:         11          11            0            0

o Initial Correspondence Points:
   Ports:        VDD GND A B C S
```

6. Post-sim waveform



7. Screenshot of the post-simulation result

```
******
**111062107_hw2_xor**

****** transient analysis tnom=  25.000 temp=  30.000 ******
power=  57.4925u  from=   0.              to=  40.0000n
delay1_xor= 242.4443p  targ=  20.2374n   trig=  19.9950n
delay2_xor= 312.2270p  targ=   2.8072n   trig=   2.4950n

           ***** job concluded
******
**111062107_hw2_xor**
```

8. Write down your delay and the difference in delay between rising and falling delay in the 3-input XOR gate

   Delay1XOR= 242.4443 ps
   Delay2XOR= 312.2270 ps
   |Delay1XOR − Delay2XOR| = 69.7827 ps

9. The hardness of this assignment and how you overcome it

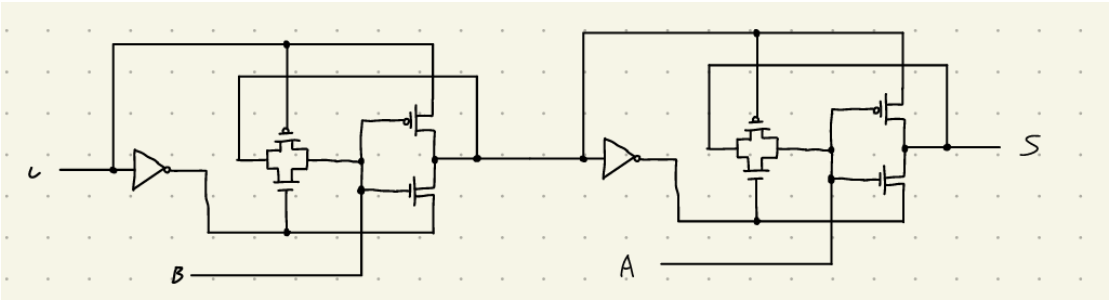
   我覺得最難的地方在於一開始 Design rule check 的地方，想要縮面積，但是又要考慮那些 rule 的話，是件很難的事情，尤其是我是新手，還沒有很熟悉介面的時候，需要花些時間才可以比較熟悉那些操作。後來我是聽我朋友的建議，就每畫一些，就開 DRC 檢查，這樣就比較可以避免最後跳出一堆錯誤的情況。

10. Any suggestions about this programming assignment

    我覺得可以再多介紹一些畫 layout 的小技巧。

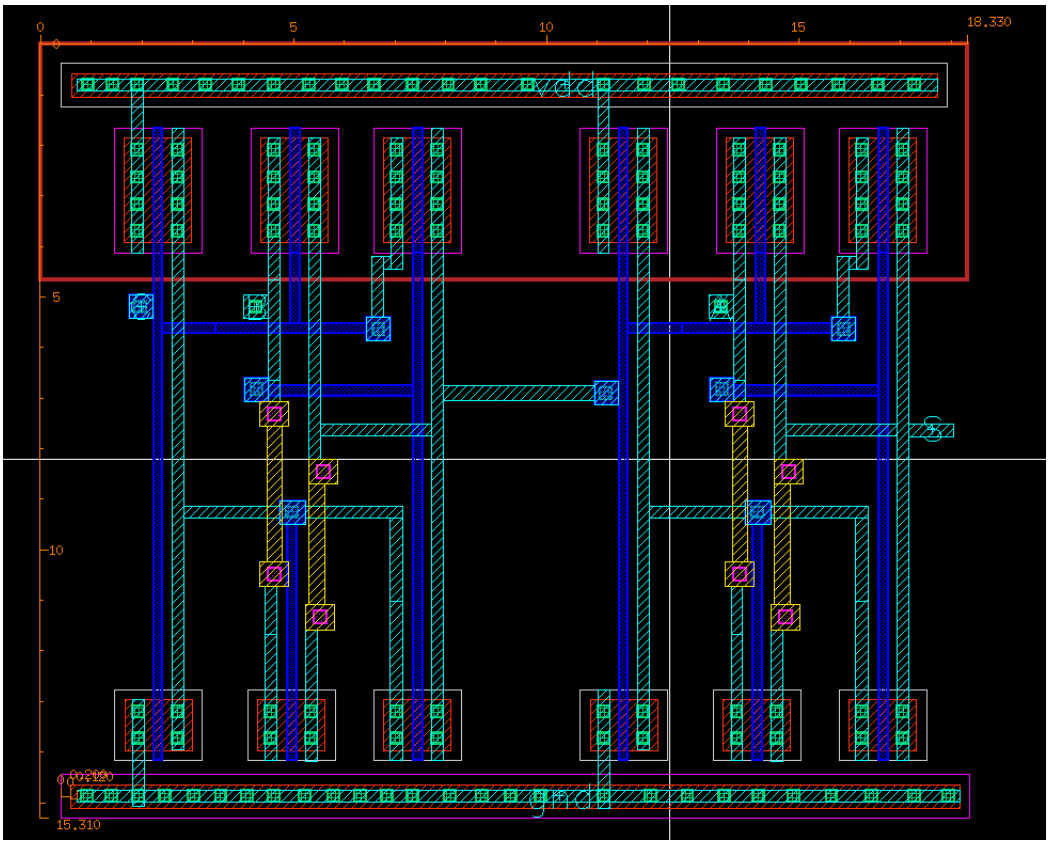
11. Bonus part

i. circuit diagram



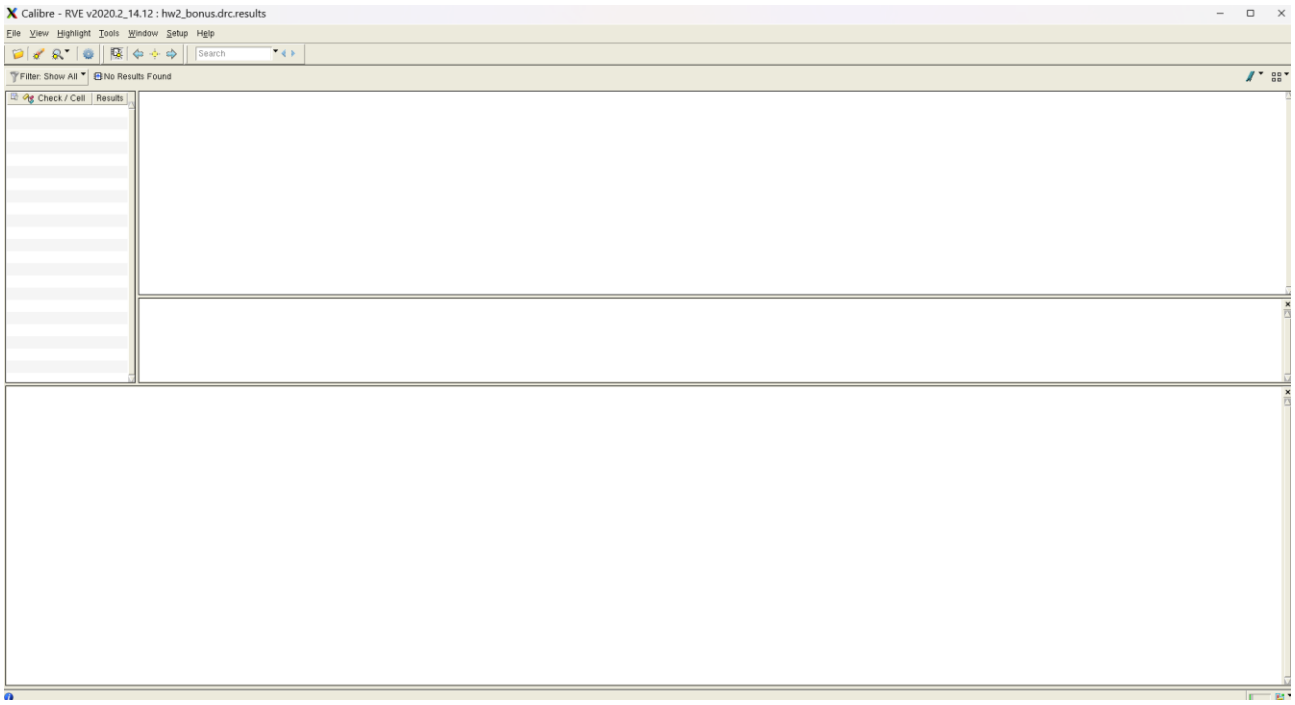
ii. Pre-sim waveform

iii. Screenshot of your layout

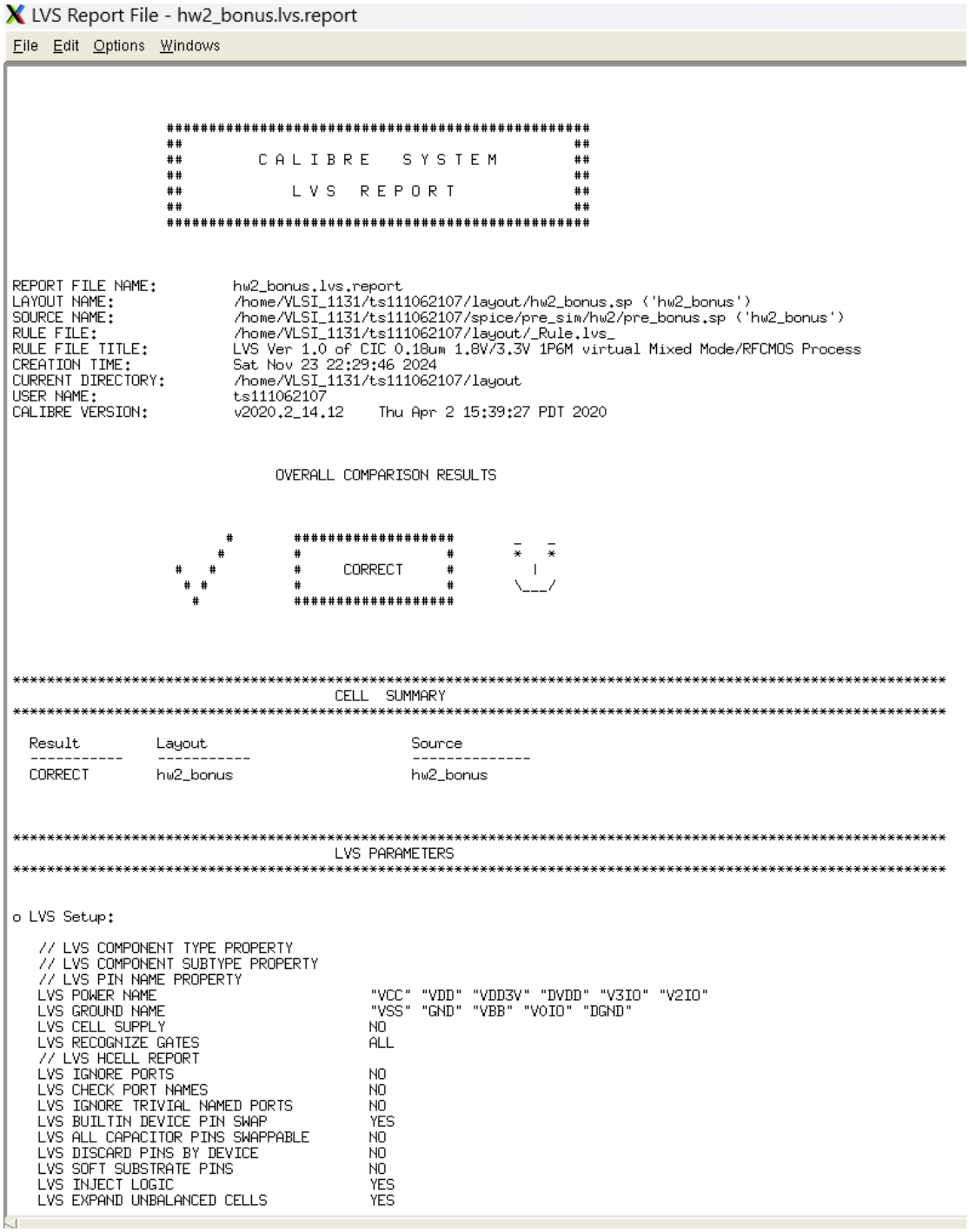


18.330 * 15.310

iv. Screenshot of DRC summary report



v. Screenshot of LVS report includes the message of passing LVS

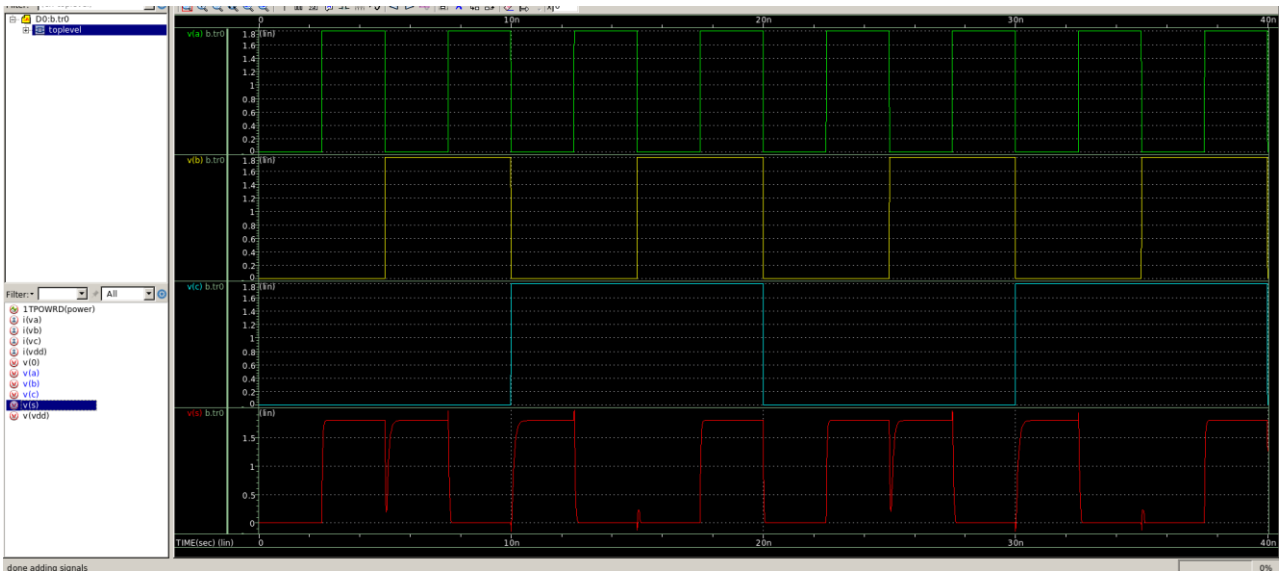


LVS Report File - hw2_bonus.lvs.report

File Edit Options Windows

```
                ################################################
                ##                                            ##
                ##        C A L I B R E   S Y S T E M         ##
                ##                                            ##
                ##            L V S   R E P O R T             ##
                ##                                            ##
                ################################################


REPORT FILE NAME:         hw2_bonus.lvs.report
LAYOUT NAME:              /home/VLSI_1131/ts111062107/layout/hw2_bonus.sp ('hw2_bonus')
SOURCE NAME:              /home/VLSI_1131/ts111062107/spice/pre_sim/hw2/pre_bonus.sp ('hw2_bonus')
RULE FILE:                /home/VLSI_1131/ts111062107/layout/_Rule.lvs_
RULE FILE TITLE:          LVS Ver 1.0 of CIC 0.18um 1.8V/3.3V 1P6M virtual Mixed Mode/RFCMOS Process
CREATION TIME:            Sat Nov 23 22:29:46 2024
CURRENT DIRECTORY:        /home/VLSI_1131/ts111062107/layout
USER NAME:                ts111062107
CALIBRE VERSION:          v2020.2_14.12    Thu Apr 2 15:39:27 PDT 2020


                          OVERALL COMPARISON RESULTS


                      #       ###################       _   _
                     #        #                 #       *   *
                  #   #       #     CORRECT     #         |
                   # #        #                 #       \___/
                    #         ###################


********************************************************************************************************************
                                    CELL  SUMMARY
********************************************************************************************************************

  Result         Layout                      Source
  -----------    -----------                 --------------
  CORRECT        hw2_bonus                   hw2_bonus


********************************************************************************************************************
                                    LVS PARAMETERS
********************************************************************************************************************


o LVS Setup:

   // LVS COMPONENT TYPE PROPERTY
   // LVS COMPONENT SUBTYPE PROPERTY
   // LVS PIN NAME PROPERTY
   LVS POWER NAME                          "VCC" "VDD" "VDD3V" "DVDD" "V3IO" "V2IO"
   LVS GROUND NAME                         "VSS" "GND" "VBB" "VOIO" "DGND"
   LVS CELL SUPPLY                         NO
   LVS RECOGNIZE GATES                     ALL
   // LVS HCELL REPORT
   LVS IGNORE PORTS                        NO
   LVS CHECK PORT NAMES                    NO
   LVS IGNORE TRIVIAL NAMED PORTS          NO
   LVS BUILTIN DEVICE PIN SWAP             YES
   LVS ALL CAPACITOR PINS SWAPPABLE        NO
   LVS DISCARD PINS BY DEVICE              NO
   LVS SOFT SUBSTRATE PINS                 NO
   LVS INJECT LOGIC                        YES
   LVS EXPAND UNBALANCED CELLS             YES
```

vi. Post-sim waveform



vii. Screenshot of the post-simulation result

```
******
**111062107_hw2_bonus**

****** transient analysis tnom=  25.000 temp=  30.000 ******
power=  20.8871u  from=   0.              to=  40.0000n
delay1_xor=  -7.4527n  targ=  12.5423n   trig=  19.9950n
delay2_xor=  13.8008p  targ=   2.5088n   trig=   2.4950n

        ***** job concluded
******
**111062107_hw2_bonus**
```

viii. Write down your delay and the difference in delay between rising and falling delay in the 3-input XOR gate.

Delay1XOR= -7.4527 ps

Delay2XOR= 13.8008 ps

|Delay1XOR − Delay2XOR| = 21.2535 ps

12. Command to open virtuoso

```
[ts111062107@linuxcad30 ~]$ source /usr/cad/synopsys/CIC/hspice.cshrc
set hspice version: 2020.12 (default)
[ts111062107@linuxcad30 ~]$ source /usr/cad/synopsys/CIC/customexplorer.cshrc
set customexplorer version: 2020.12 (default)
[ts111062107@linuxcad30 ~]$ source /usr/cad/cadence/CIC/ic.cshrc
set IC version: IC51.41.151 (default)
[ts111062107@linuxcad30 ~]$ source /usr/cad/mentor/CIC/calibre.cshrc
set calibre version : aoi_cal_2020.2_14.12/
```

source /usr/cad/synopsys/CIC/hspice.cshrc

source /usr/cad/synopsys/CIC/customexplorer.cshrc

source /usr/cad/cadence/CIC/ic.cshrc

source /usr/cad/mentor/CIC/calibre.cshrc

```
[ts111062107@linuxcad30 ~]$ cd layout
[ts111062107@linuxcad30 ~/layout]$ icfb &
[1] 18938
```

cd layout

icfb &