Yanuo Deng (James)
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eInfochips , Irvine, CA
Dear Hiring Manager

I am applying for the position of "RTL Design Engineer" in your esteemed eInfochips company.

I believe I am the right candidate for the position as I have a MSc in Microelectronics & Solid State Electronics. My 15+ years of experience, among others, includes designing a dual-MIPS SOC with a Security Engine inside. I wrote all the IP cores consisting of AES, DES, 3DES, MD5, SHA1, CRC used to speed up the DICE + RIoT security cryptography. Each IP core was about 3000 to 5000 lines in Verilog HDL, activities included designing and testing the RTLs & Netlist, and timing check rules for simulation and place & route.

I am committed to achieving results and working long hours to achieve them is not a problem as evidenced by delivering at the rate of one IP core per month, with the SOC passing at first tapeout with a US patent US7356671B1 awarded.

I am also experienced at using Linux / VxWorks, analogy simulatinon tool Hspice, and prototyping using Xilinx/Altera FPGA boards.

I have experiences at Linux kernel trimming, bootloader coding, embedded Linux systems porting at ARM/MIPS, and FreeRTOS porting at STM32.

I used NC as simulator and Verdi as wave debug.

I hope my background meets your needs and I look forward to elaborating on how my specific skills and abilities will benefit your eInfochips company.

I can be contacted at deng.ya.nuo@gmail.com or (408)444-5520 to arrange for a convenient time to meet.

Sincerely,
Yanuo Deng (James)