Yanuo Deng (James)
1565 Cress Way, Olivehurst,CA,95961 * (408)444-5520 * deng.ya.nuo@gmail.com

eInfochips , Irvine, CA
Dear Hiring Manager

I am applying for the position of "RTL Design Engineer" in your esteemed eInfochips company.

I believe I am the right candidate for the position as I have a MSc in Semiconductor. My 15+ years of experience, among others, includes designing a dual-MIPS SOC with a Security Engine inside. I wrote all the IP cores consisting of AES, DES, 3DES, MD5, SHA1, CRC used to speed up the DICE + RIoT security cryptography. Each IP core was about 3000 to 5000 lines in Verilog HDL, activities included designing and testing the RTLs & Netlist, and timing check rules for simulation and place & route.

I am committed to achieving results and working long hours to achieve them is not a problem as evidenced by delivering at the rate of one IP core per month, with the SOC passing at first tapeout with a US patent US7356671B1 awarded.

I am also experienced at using Linux / VxWorks, analogy simulatinon tool Hspice, and prototyping using Xilinx/Altera FPGA boards.

I have experiences at Linux kernel trimming, bootloader coding, embedded Linux systems porting at ARM/MIPS, and FreeRTOS porting at STM32.

I used NC as simulator and Verdi as wave debug.

I hope my background meets your needs and I look forward to elaborating on how my specific skills and abilities will benefit your eInfochips company.

I can be contacted at deng.ya.nuo@gmail.com or (408)444-5520 to arrange for a convenient time to meet.

Sincerely,
Yanuo Deng (James)

Resume of Yanuo Deng (James)

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CAREER OBJECTIVE

Focused professional with 15+ years of experience and a proven knowledge of embedded system(linux/RTOS), and digital & analogy circuit design. Aiming to leverage my skills to be a successfully Integrated Circuit Engineer, Software Engineer, or Network Security Engineer.

EXPERIENCE

C-MATRIXTECH CO.LTD., Zhuhai, China, 3 people R&D/6

Integrated Circuit Designer, Dec 2017 - Feb 2019

* Verilog coding, FPGA simulation and debug for self-powered SOC chip.
* MCU debug; Port C-language from Assembly for the MCU; Mixed (Analog) circuit design
* Achieved self-powered MCU SOC used on iPhone data cables; Mass production 10k/M

VIOMI CO.LTD., Foshan, China, 3 people R&D/200

Software (Firmware) Engineer, May 2017 - Oct 2017

* Linux driver for the Wi-Fi chip; Speech Recognition App for Linux
* Achieved smart wireless Speech Recognition module ; Mass production 3k/M

BLUEWAY CO.LTD., Huizhou, China, 5 people R&D/2500

Software (Firmware) Engineer, May 2016 - Apr 2017

* FreeRTOS system migration to STM32 for the embedded board, target for electric mowers

ADON CO.LTD., Foshan, China, 3 people R&D/350

Software (Firmware) Engineer, Oct 2013 - Dec 2015

* Linux driver & app for the Homepod (Wi-Fi speaker/charger for iPhone); Mass production, 3k/M

SKYIT SOFTWARE CO.LTD., Shunde, China, 5 people R&D/500

Software Engineer, Dec 2011 - Jul 2013

* Windows Client App by C#; Data API by C for the first order a meal Android App in China

VBRIDGE MICROSYSTEM INC, San Jose, CA, 5 people R&D/12

Digital Integrated Circuit Engineer, Apr 2005 - May 2008

* IP cores of security engineer : AES, DES, 3DES, MD5, SHA1, CRC ; 5-bits MCU core.
* All IP cores tapout in a dual-MIPS SOC Chip.
* Linux + VxWorks board support package(BSP) was built for the dual-MIPS.

EDUCATION

XI'AN university of technology, Xi'an city, Shannxi, China
Master of Science (M.S.) Microelectronics & Solid State Electronics (Apr 2005)

ADDITIONAL SKILLS

* C, Verilog, Vim, Bash, Perl, Go-language, Gnumake, git
* Linux / FreeRTOS driver

Certifications

Electronics Engineer Certification, Foshan , China , Aug 2008

Personal Characteristics

I work well within teams, and I am assertive and creative in finding the best solutions for the team. I am known to be stable and firm when coding. I am committed to achieving goals set for me. I speak and write Cantonese/Mandarin.

Referrals

Dan Teuthorn, Teledyne microwave solutions, VP engineer, 408-421-7303, Den.Teuthorn@teledyne.com
Tang Shanqiang, Cadence, Principal Application Engineer, +65-90546301, ansent@cadence.com
Stephen Fung, Atheros/Qualcomm , semicondutor engineer, 408-338-5175, stephen@thepoint.church

USA Employment Authorization Document(EAD) valided from 2021 to 2023. No work sponsor is needed.