A primer on USB Type-C and Power Delivery applications and requirements

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This introduction to USB Type-C™ and Power Delivery dives deep into various applications and their data and power requirements.

Modern technology has been pushing the boundaries of the universal serial bus (USB) standard. There is a trend towards smaller, thinner, and lighter form-factor designs where legacy USB interfaces cannot keep up. As a result, the USB Type-C™ connector ecosystem was born to address the evolving needs of modern platforms and devices. Additionally, USB Power Delivery (PD) has been modified for the Type-C connector to address the growing needs of power-hungry applications.

Introduction

You may have heard about Type-C's reversible cable and its ability to be pluggable in either the right-side up or upside down direction. However, when you think about the requirements for a particular system, you may be totally lost on what is needed versus what is a "nice to have" feature.

In this paper, we will introduce you to a few key concepts early on, but will quickly dive into the various applications, introducing Type-C concepts and requirements along the way. We will start with the most basic Type-C applications and work our way up to full-featured Type-C and PD applications.

First, let us review the evolution of USB data, starting with USB 1.0 through USB 3.1 Gen 2. **Table 1** shows the maximum transfer rate for each of the USB data transfer related specifications. This standard starts with USB 1.x supporting 1.5 Mbps (low speed) and 12 Mbps (full speed), but has evolved to support as high as 10 Gbps (SuperSpeed+) with USB 3.1 Gen 2.

Now, let us review the evolution of USB power, starting with USB 2.0 through USB PD 3.0. **Table 2** shows that the overall trend has been to increase the maximum power over the years to address the growing needs of platforms and devices. In this paper, we will focus on USB Type-C and USB PD 3.0. Without PD you can support up to 5 V at 3 A (15 W) with just Type-C alone. However, with PD, you can support up to 20 V at 5 A (100 W) over the Type-C ecosystem

Data and power roles

Before diving into applications, we want to introduce you to a few terms in regards to the application's role in both data and power transfer. When it

Specification	Data Rate Name	Maximum Transfer Rate
USB 1.0 and USB 1.1	Low Speed	1.5 Mbps
	Full Speed	12 Mbps
USB 2.0	High Speed	480 Mbps
USB 3.0	SuperSpeed	5 Gbps
USB 3.1	SuperSpeed+	10 Gbps

Table 1. USB specification and maximum voltage, current and power.

Specification	Maximum Voltage	Maximum Current	Maximum Power
USB 2.0	5 V	500 mA	2.5 W
USB 3.0 and USB 3.1	5 V	900 mA	4.5 W
USB BC 1.2	5 V	1.5 A	7.5 W
USB Type-C 1.2	5 V	3 A	15 W
USB PD 3.0	20 V	5 A	100 W

***Table 2**. USB specification and maximum voltage, current and power.*

comes to data flow in a USB connection, we have downstream facing port (DFP), upstream facing port (UFP), and dual-role-data (DRD). A DFP sends data downstream and is typically the ports on a host or the ports on a hub to which devices are connected. They source V_{BUS} power (power path between host and device) and can also source V_{CONN} power (to power electronically marked cables). An example of an application that may include a DFP is a docking station.

A port that receives data is known as a UFP. A UFP is a port on a device or a hub that connects to a host or the DFP of a hub. These ports usually sink V_{BUS}. An example of an application that may include a UFP is a monitor/display.

Lastly, the DRD port can operate as either a DFP (host) or a UFP (device). Note that the role the port initially takes on is determined by the port's power role at attach. A source port takes on the data role of a DFP and a sink port takes on the data role of a UFP. However, the port's data role may be dynamically changed using USB PD data role swap. Applications that may include DRD ports are laptops, tablets, and smartphones, to name just a few.

When it comes to power flow in a USB connection, terms include sink, source, and dual-role-power (DRP). A sink is a port that when attached consumes power from V_{BUS} and most often is a device. These could include USB peripherals such as a USB-powered light or fan. A source is a port that when

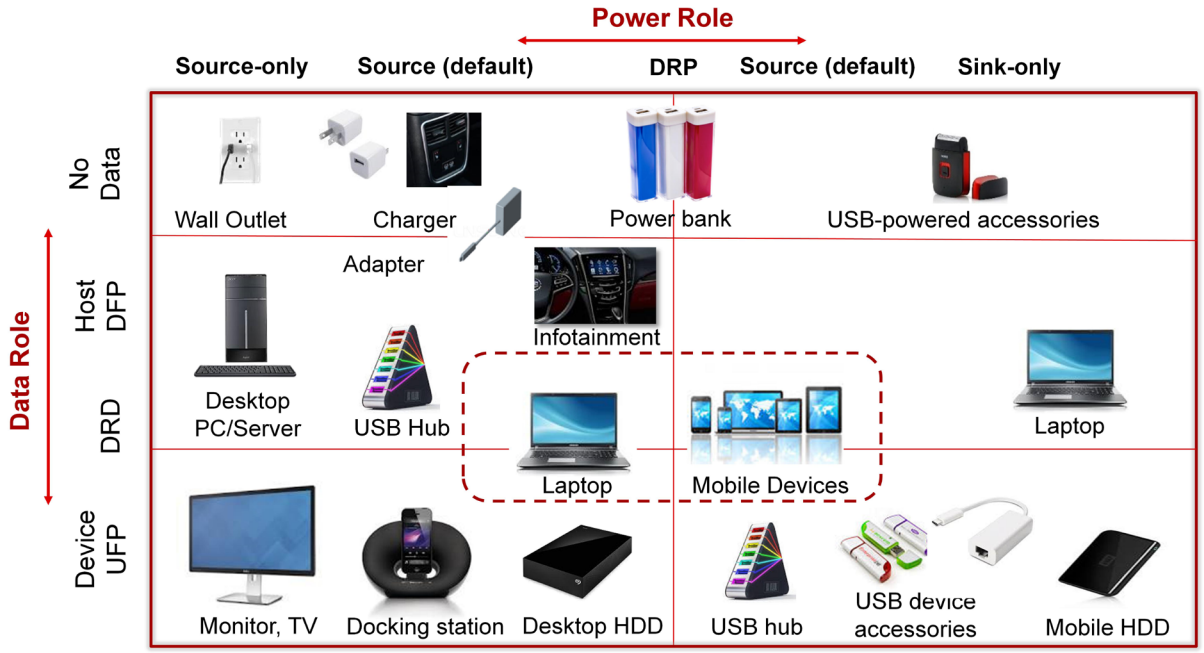

***Figure 1**. USB Type-C version 1.2 example applications.*

attached provides power over V_{BUS}. Common sources are a host or hub DFP. An example of a source application is a Type-C wall charger.

A DRP port is a port that can operate as either a sink or source, or it may alternate between these two states. When a DRP initially operates as a source, the port takes the data role of a DFP. Alternatively, when a DRP initially operates as a sink, the port takes the data role of a UFP. However, the DRP's power role may be changed dynamically by using USB PD power role swap. For example, a laptop may include a DRP port that can receive power to charge the laptop's battery, but can also deliver power to charge external accessories.

Additionally, there are two special subclasses of a DRP: sourcing device and sinking host. A sourcing device is capable of supply power, but not capable of acting as a DFP. One example of this subclass is a Type-C and PD-compatible monitor that receives data from a laptop's DFP, but also charges the laptop. A sinking host is capable of consuming power, but not capable of acting as a UFP. An example could be a hub's DFP that sends data to an accessory while being powered by that accessory. These subclasses are not covered in this paper.

Type-C UFP USB 2.0 without PD

The most simple and probably the most common application is a UFP USB 2.0 without PD (≤ 15W). Common applications include anything that is USB-powered today and does not require SuperSpeed data, such as a mouse, keyboard, wearables, and various other small electronics.

Figure 2 highlights the necessary functional blocks for a Type-C UFP USB 2.0 system.

At this point we are going to assume that you understand the USB Type-C connector pinout and how reversibility works. If necessary, however, you can find more information on this topic in the Appendix. Note that the USB 2.0 PHY is no different than in previous USB 2.0 designs with a Type-A or Type-B connector. It serves as the physical layer between the data from USB's D+ and D– lines to UTMI+ low pin interface (ULPI) for the application processor to manage. USB 2.0 PHYs are often integrated into processors or microcontrollers; however, there are discrete PHYs available such as the TUSB1210, if needed. The configuration channel (CC) logic block was introduced in the Type-C specification and is how cable detection, orientation, and current-carrying capability are determined.

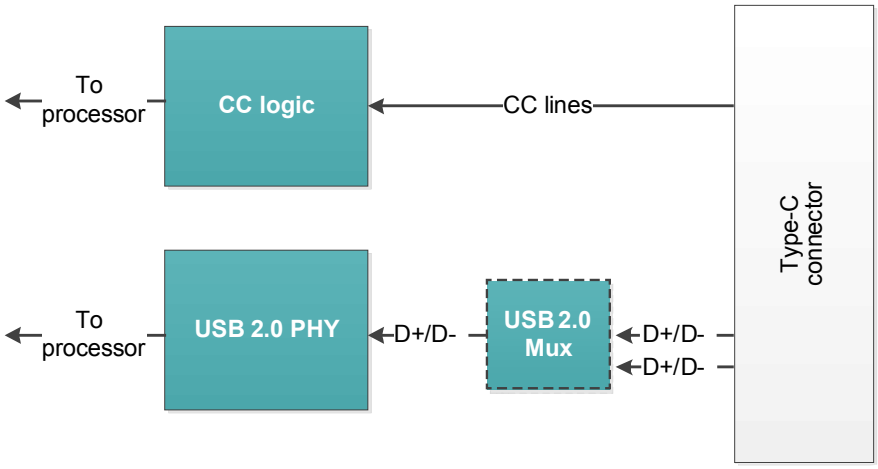

***Figure 2**. Type-C UFP USB 2.0 without PD block diagram.*

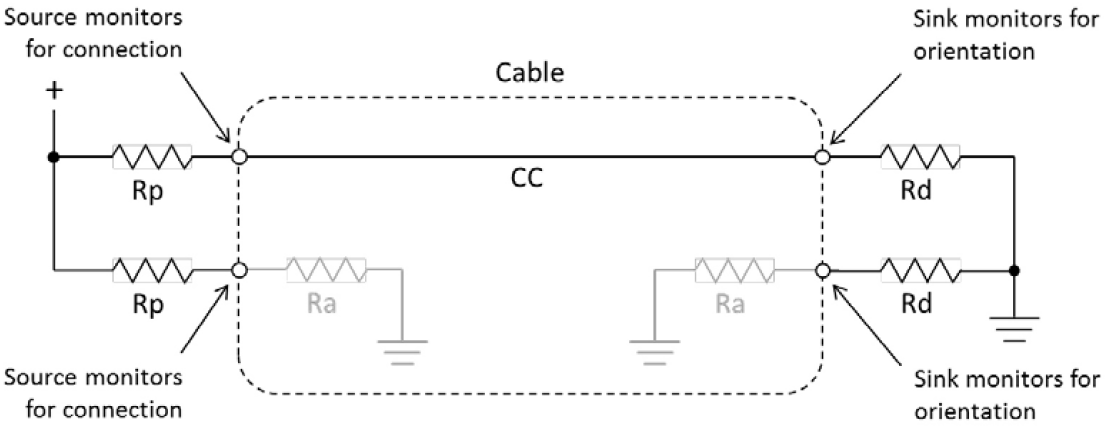

***Figure 3**. CC logic pull-up/pull-down termination.*
(Source: USB Type-C specification v1.2, Figure 4-5 pull-up/pull-down CC model)

This is how it works:

1. Illustrated in **Figure 3**, cable detection occurs when one of the two CC lines is pulled down. A DFP will have both of its CC pins pulled-up with resistors Rp and a UFP will have both of its CC pins pulled-down with resistor Rd [1]. Once a DFP detects one of its CC lines being pulled down, the DFP will know that a connection has been made.
2. Orientation can be determined based on which CC line is pulled down (in other words, if CC1 is pulled down, the cable is not flipped; but if CC2 is pulled down, the cable is flipped). For non-active cables, the remaining CC line will be left open; but for active cables, the remaining CC line will be pulled down with Ra.
3. The current-carrying capability is determined with the values of Rp. As mentioned in the introduction, USB Type-C can support either 1.5 A or 3 A natively. A DFP can advertise its current-carrying capability with a specific value pull-up resistor. A UFP has a fixed-value pull-down resistor Rd such that when connected, it forms a voltage divider with Rp. By sensing the voltage at the center tap of the voltage divider, a UFP can detect the DFP's advertised current.

The last block is a USB 2.0 MUX (often called a high-speed [HS] MUX). The dotted outline represents an optional block not required by the Type-C specification. To understand the purpose of the MUX, first you must understand how flipping the cable affects data flow. In a Type-C receptacle, we have two pairs of D+/D– lines for a single channel of USB 2.0 data. In one orientation, data flows down one of the pairs. In the flipped orientation, data flows down the other pair. The USB Type-C specification states that shorting the pairs together, D+ to D+ and D– to D–, and creating a stub is allowed. However, even though not required, some designers elect to include a USB 2.0 MUX in their system to improve signal integrity

The TI TUSB320 may be of interest for UFP applications with USB 2.0 data and no PD. This device is a compact solution for CC logic that can determine cable detection, orientation, and current-carrying capability.

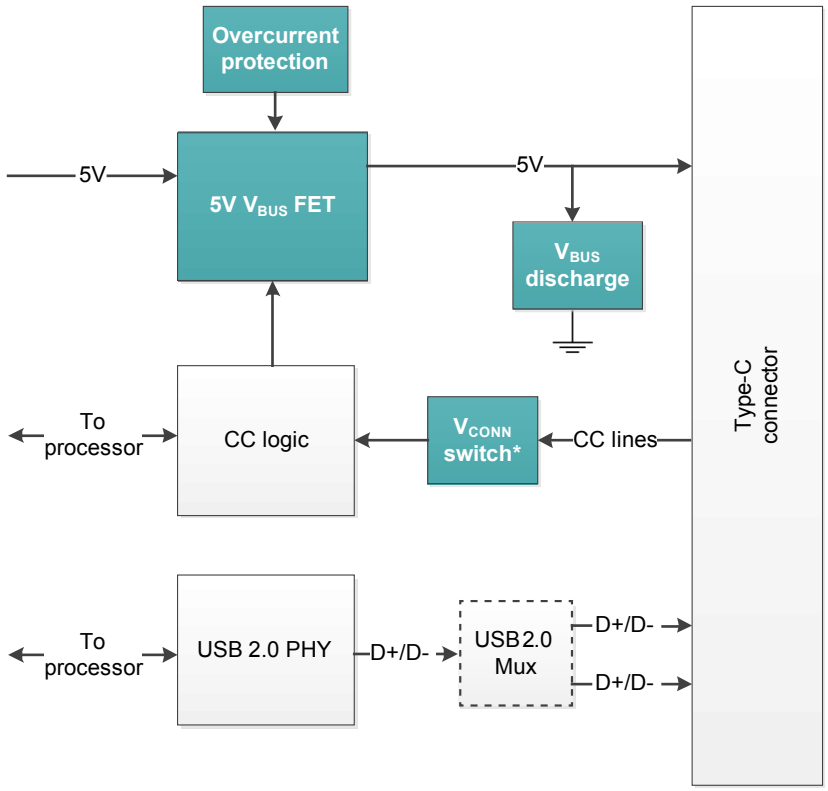

***Figure 4**. Type-C DFP USB 2.0 without PD block diagram. *V_{CONN} switch is not always required as will be discussed.*

Type-C DFP USB 2.0 without PD

Another simple and common application is a DFP USB 2.0 without PD, shown in **Figure 4**. One example is a 5V AC/DC adapter (commonly referred to as a "wall-wart").

Figure 4 represents the blocks necessary for a Type-C DFP USB 2.0 without PD. Note the similarities to **Figure 2** with a few extra blocks added, while the CC logic block is still the same. In the case of a DFP, however, the device presents Rp and monitors for a pull-down caused by Rd. Once the Rp detects a pull-down, the DFP knows there is a device connected and provides 5 V. Providing 5 V only on the V_{BUS} line after detecting a device (cold-plugging), versus always providing 5 V is a new feature introduced in USB Type-C.

The USB 2.0 ULPI PHY is the same as in the previous section. However, for applications that do not transfer data, such as the 5-V wall adapter, you can omit the USB 2.0 ULPI PHY from the design.

Because USB Type-C implements cold-plugging, in **Figure 4** we added a 5 V V_{BUS} field-effect transistor (FET). As a result, the design requires a switch for the 5-V rail. Additionally, the USB Type-C specification requires that all sources monitor current and to protect itself if a sink tries to draw in excess of what it can supply [2]. This is where the overcurrent protection block comes into play. These two blocks can be discrete integrated into the point-of-load (PoL) power converter, or integrated into the Type-C device.

Also added in **Figure 4** is the V_{BUS} discharge block. When no device is attached, V_{BUS} should sit at 0 V. As a result, the USB Type-C specification requires a source to discharge V_{BUS} within 650 ms of a detached sink [3]. V_{BUS} discharge is often integrated into a USB Type-C device, but also can be integrated with a bleeder resistor.

Lastly, the V_{CONN} switch is optional in many cases. V_{CONN} is used to power passive e-marked or active cables by switching 5 V onto the unused CC line (see Appendix). Note that electronically-marked cables are cables that support USB PD communication and provide a method for determining the cable characteristics. **Figure 3** shows that one CC line in the Type-C cable connects Rp to Rd, while the other is left floating (passive cable) or pulled down to ground with Ra (passive e-marked or active cable). V_{CONN} is required for all applications that support USB 3.1 speeds or power delivery higher than 3 A [4]. The V_{CONN} switch is also required if you want to support active cables, such as longer distance cables that require signal conditioning such as with a redriver or retimer.

Texas Instruments' designed the TPS25810, a controller that can be used for DFP USB 2.0 data without PD applications. This device includes CC logic, a 5-V V_{BUS} FET, overcurrent protection, V_{BUS} discharge, a V_{CONN} switch and more.

Type-C DRP/DRD USB 2.0 without PD

The last USB 2.0 non-PD application available is the DRP/DRD. For non-PD applications, DRD and DRP are the same. A common example is a slower speed laptop port that can send power in either direction – to charge or be charged, and act as either a host or device. Another common application for this system type is tablets and smartphones. You can see an updated block diagram in **Figure 5**.

The only noticeable change from **Figure 4** is adding the Rp/Rd switch. A DRP/DRD can present itself as either a UFP or a DFP. As a result, this design must have a method to pull the CC lines up with Rp or pull the lines down with Rd (default on a dead battery in order to charge), see **Figure 6**. Notice how the switch can toggle between pulling the CC line up (in this case with a current source to create a specific voltage across Rd), or pulling the CC line down to GND.

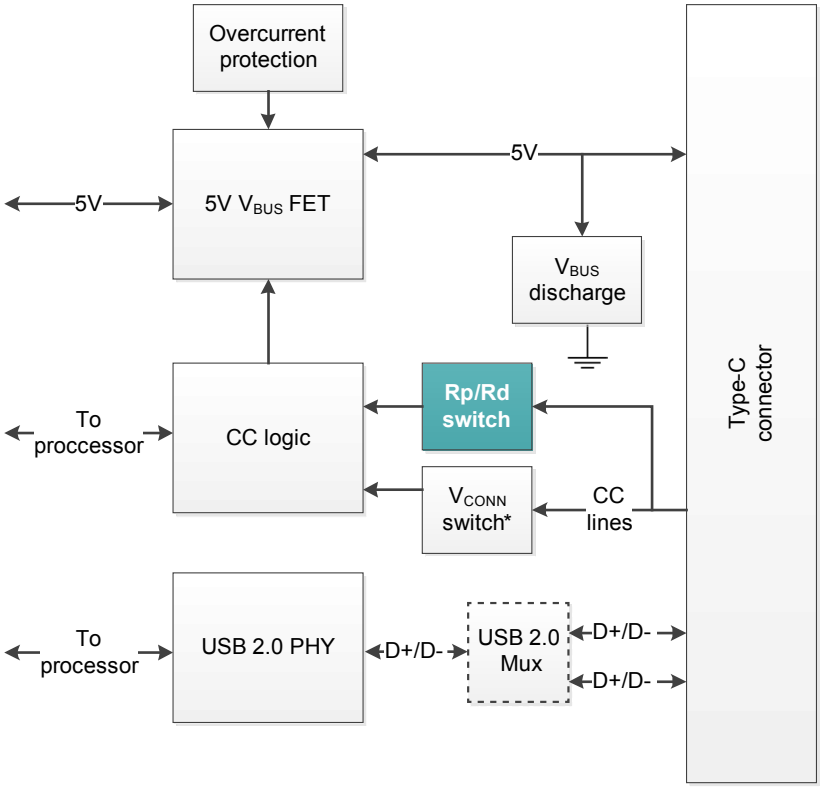

***Figure 5**. Type-C DRP/DRD USB 2.0 without PD block diagram. *V_{CONN} switch is not always required as will be discussed.*

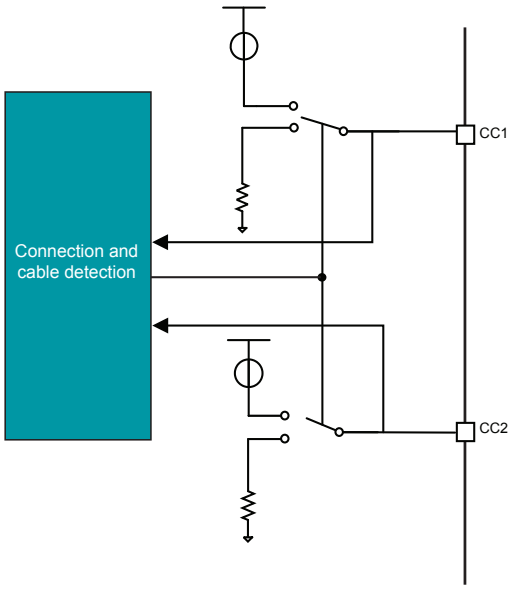

Figure 6. Rp/Rd switch schematic.

Texas Instruments TUSB32x family has several devices that address DRP/DRD USB 2.0 without PD applications. These devices integrate the CC logic, Rp/Rd switch and, depending on which device, the V_{CONN} switch.

Type-C DRP/DRD USB 2.0 with PD

Applications with increasing complexity require PD. As mentioned in the introduction, systems with PD can support power levels of up to 20 V/5 A (100 W). This is done by first increasing the voltage on V_{BUS} while holding the maximum current at 3 A. After reaching the maximum voltage of 20 V, you can increase the current up to 5 A (**Figure 7**).

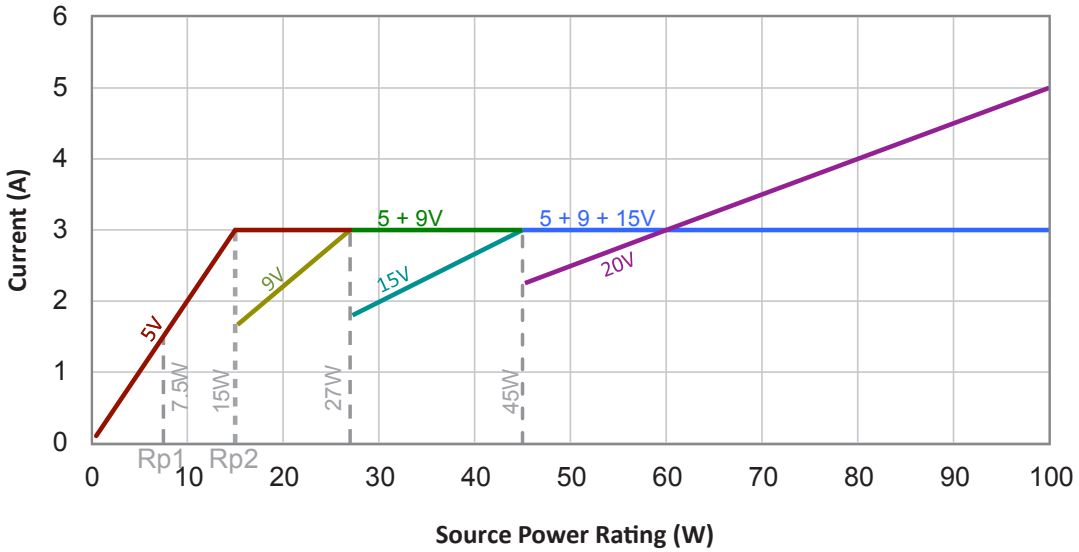

Figure 7. PD Profiles (power rails and maximum current).
(Source: Figure 10-2 in the USB PD Specification v3.0)

Figure 7 shows us that:

1. The discrete voltage levels required are 5, 9, 15 and 20 V (modified in USB PD specification v3.0).
2. The current is allowed to vary continuously, depending on the required power level (up to 3 A).
3. At any given power level, a source is required to support all previous voltages and power levels. For example, a 60-W source must be able to supply: 20 V at 3 A; 15 V at 3 A; 9 V at 3 A and 5 V at 3 A. This was updated in v3.0 of the USB PD specification to ensure that higher power supplies could support lower-powered devices. An example is a charger for both your laptop and phone.

Figure 8 highlights four new blocks that come into play for PD applications. The V_{BUS} FET introduced earlier is now able to handle 5-20 V (at discrete levels, depending on the desired power level), and potentially up to 5 A (again, only when providing 20 V). A gate

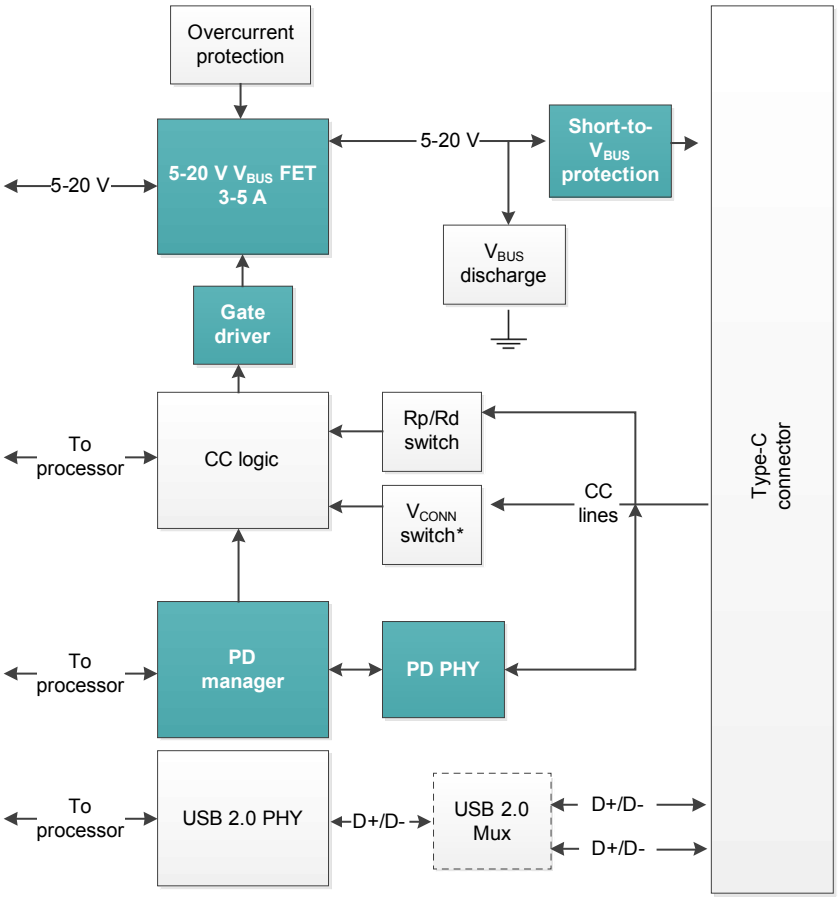

***Figure 8**. Type-C DRP/DRD USB 2.0 with PD block diagram. V_{CONN} switch is not always required as will be discussed.*

driver block is added for the higher power FET. Some devices integrate a high-power FET as well as a gate driver to drive an even higher power external FET (TPS65982, for example), while other devices integrate just the gate driver, or neither.

Up to this point, we have not discussed ESD protection in the block diagrams because it is not any different from non-Type-C USB systems outside of the higher channel count. However, the exception is with V_{BUS} to short protection. The Type-C connector has a higher pin density than legacy USB connectors. As a result, it is easier to accidentally short V_{BUS} to adjacent pins (see Appendix). With the potential of having V_{BUS} of up to 20 V, it is possible to have a short between the 20 V and a 5 V line (such as SBU, CC and so on). To protect against this potentially catastrophic event, Texas Instruments introduced the TPD8S300, a one-chip protection integrated circuit (IC).

Two other new blocks are the PD PHY and PD manager. Together, these blocks send packets of data across the CC lines which allows for communication between the DFP and UFP. This communication allows the source to advertise what power levels it can support, and the sink can then request a supported power level. Once a power level is agreed upon, voltage and current levels are adjusted.

It is important to distinguish the difference in roles between the PD manager and the PD PHY because several Type-C devices may include one but not the other. For example, the MSP430G2xx4/5 can act as a PD manager, but does not have the PD PHY. The PD PHY's responsibility is to drive the CC lines, but in itself is not intelligent.

The PD manager is the brains, containing a complex state machine to support PD negotiation and to control the PHY. (The PD manager also does the

alternate-mode negotiation – more to come on this later.) The PD manager does this by telling the PHY which packets to send, such as: advertise power level, request power level, and acknowledge channel power level. We have grossly oversimplified our description for the sake of attempted succinctness [5].

The main takeaway is that if PD is required, you need a PD PHY and a PD manager. You can implement a PD PHY and PD manager by using an integrated PD manager and PD PHY solution, implementing a PD manager on a microcontroller and using a separate PHY with a Type-C port controller (TCPC), or discretely if you are so inclined.

For DFP applications implementing PD, Texas Instruments offers the TPS25740A, a source controller that includes a gate driver for a V_{BUS} FET, overcurrent and overvoltage monitoring, CC logic, PD manager and PD PHY. This device has the ability to advertise 5 V, 9 V and/or 15 V. Texas Instruments is working on solutions for UFP, DRP and DRD PD applications.

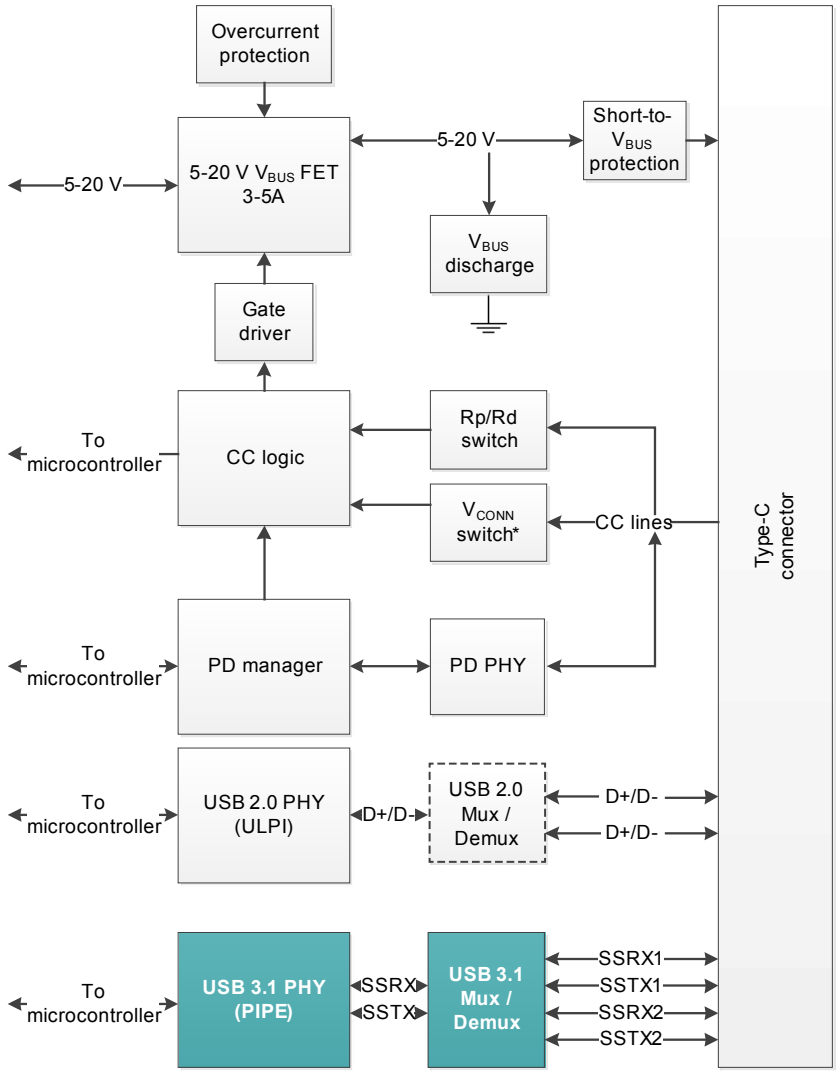

***Figure 9**. Type-C USB 3.1 block diagram. V_{CONN} switch is not always required as will be discussed.*

USB 3.1 Gen 1 (SuperSpeed) and Gen 2 (SuperSpeed+)

Applications that require faster than 480 Mbps transfer rates will need to leverage either USB 3.1 Gen 1 (SuperSpeed) or Gen 2 (SuperSpeed+). As stated in the introduction, SuperSpeed supports data transfer rates up to 5 Gbps and SuperSpeed+ supports up to 10 Gbps. However, to enable these higher transfer rates in a Type-C application, you need to include a USB 3.1 PIPE PHY (PHY interface for the PCI Express [PCIe], serial advanced technology attachment [SATA], and USB architectures), and a bidirectional differential switch that supports USB 3.1, as seen in **Figure 9**.

The USB 3.1 PIPE-compliant PHY is needed to provide a bridge between the media access control (MAC), the open systems interconnection model (OSI) layer, and the physical medium. For example, Texas Instruments TUSB1310A is a PIPE-compliant USB 3.0 PHY transceiver that supports up to 5 Gbps data rates.

The bidirectional differential switch operates in multiplexer (mux) and demultiplexer (demux) operation. Unlike USB 2.0 data, the mux/demux is not optional and is required for all applications, except USB Type-C plugs that are connected directly to a host (versus a female receptacle).

One example is a USB 3.1 flash drive with a USB Type-C plug that is physically incorporated into the device. In this type of application, the USB 3.1 data bus is fixed by design (**Figure 10**). Thus, there are only two possible connected states that exist when viewed by a Type-C host.

Figure 10 shows a host, which is required to have the USB 3.1 mux/demux route the USB 3.1 signal pairs. Type-C cables are wired such that the CC wires are position-aligned with the USB 3.1 signal pairs. As a result, the host is able to configure the switch based on which CC pins (CC1/CC2) are terminated at the receptacle.

All USB 3.1 applications that incorporate a Type-C receptacle are required to include the USB 3.1 switch. The reason for this is that when you have a Type-C cable connecting two Type-C receptacles, the cable orientation and twist is not fixed. As a result, there are four possible connected states that exist when viewed by either the Type-C host or device. These possible states are illustrated in **Figure 11**.

It does not matter if the application is for a DFP or UFP. If it incorporates a Type-C receptacle, the USB 3.1 switch is required to route the transceiver (TX) and receiver (RX) signal pairs. Texas Instruments HD3SS3212 is an example of a bidirectional passive switch that can be configured in either the mux or

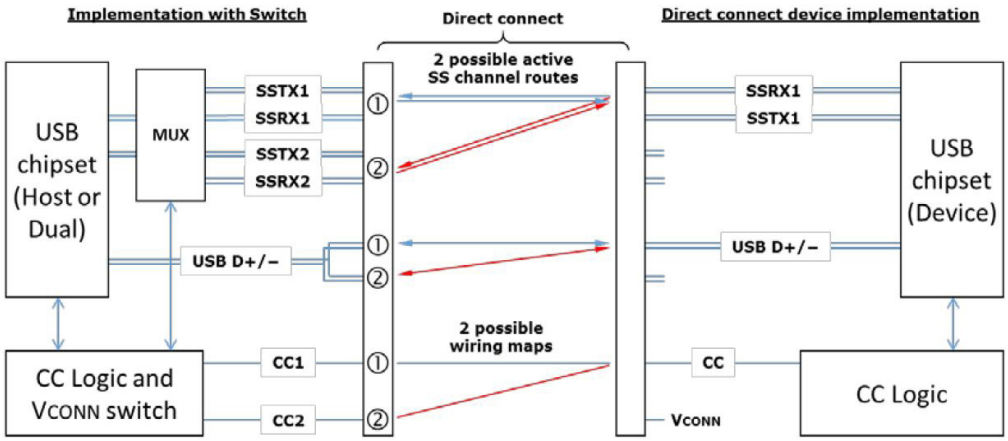

Figure 10. USB 3.1 Data bus connection for Type-C plug directly connected to Type-C Host.
(Source: Figure 4-4 in the USB Type-C Specification v1.2)

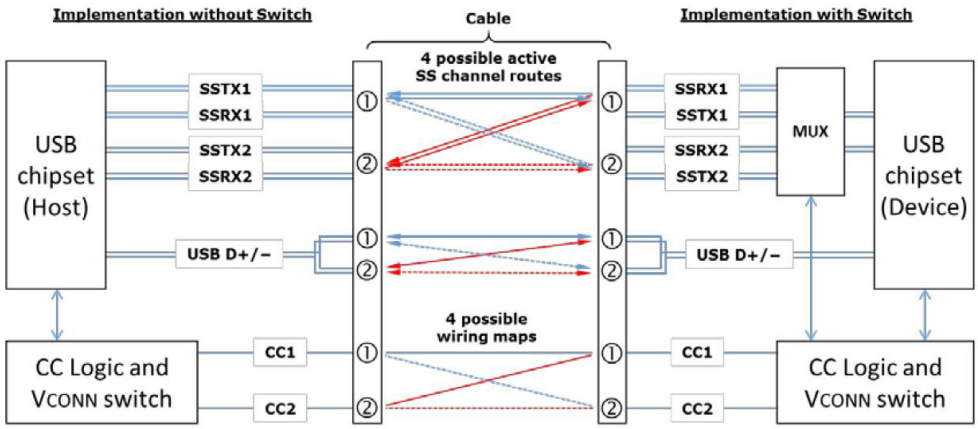

***Figure 11**. USB 3.1 data bus connection for Type-C receptacle connected to Type-C receptacle.*
(Source: Figure 4-3 in the USB Type-C Specification v1.2)

demux configuration, and can be used for USB Type-C applications supporting USB 3.1 Gen 1 and Gen 2.

As with any high-speed interface, some USB 3.1 applications may require signal conditioning to maintain signal integrity. To address this need, Texas Instruments released the TUSB542. This device incorporates both a USB 3.1 Gen 1 mux/demux as well as receiver equalization and transmitter de-emphasis in order to maintain signal integrity on both the transmit and receive data paths. Of course, signal conditioning is optional.

For USB 3.1 applications with Power Delivery, the TPS65982/6 with the HD3SS3212 offers a complete solution including the PD manager and PHY, 20 V/3 A FET, CC logic, and SuperSpeed mux.

Alternate Mode

An important benefit of USB Type-C is its ability to replace the need for nearly every cable in consumer devices (HDMI, DisplayPort/Thunderbolt™, power barrels, USB Type-A/B, and others). To do this, Type-C needed additional functionality than what was offered in USB 3.0, thus Alternate Mode was defined. Alternate mode allows USB Type-C pins (TX/RX pairs and SBU) to be repurposed for a different function [6]. Up to this point, video has been the primary focus for Alternate Mode with HDMI (via the MHL Alternate Mode) and DisplayPort/Thunderbolt Alternate Mode already announced. It is possible for 4K video to be transferred over Type-C cables, which could not be realized without an alternate mode. Note that the USB Implementers Forum requires that they both approve and certify any alternate mode. **Figure 12** highlights two new blocks required to support Alternate Mode.

The first new block is the Alternate Mode PHY. For example, with DisplayPort, you need a DisplayPort source (from GPU). The second is the Alternate Mode MUX. For a Type-C USB 3.0 system, the SuperSpeed MUX is required to support different cable orientations. Alternate Mode needs the ability to support switching in the Alternate Mode PHY while still supporting different cable orientations. These functions are typically integrated into a single MUX for this purpose, such as the HD3SS460 SuperSpeed/Alternate Mode MUX.

Two other important blocks required for Alternate Mode are the PD PHY and PD manager. It is possible to support PD and Alternate Mode at the same time (imagine a monitor that takes in HDMI video, but also charges your laptop when connected).

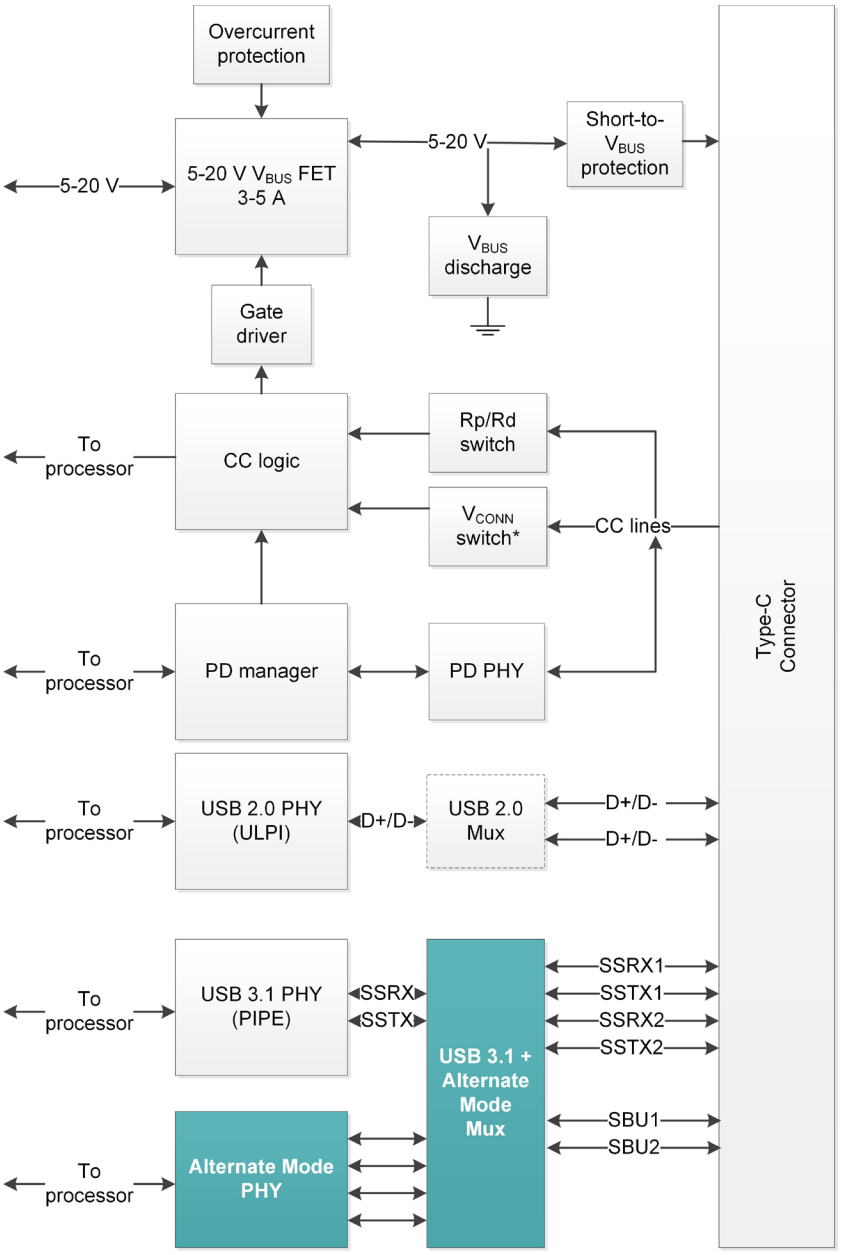

***Figure 12**. Type-C Alternate Mode block diagram. *V_{CONN} switch is not always required as will be discussed.*

However, even if PD power levels are not required, a PD PHY and PD manager must be included in the system to support Alternate Mode. This is because Alternate Mode is negotiated the same way as is PD – a vendor-defined message (VDM) over the CC line (see Type-C DRP/DRD USB 2.0 with PD). Without a PD PHY and PD manager, it would not be possible for a system to advertise and agree upon an Alternate Mode.

A final note on Alternate Mode is how to handle an incompatible connection. Imagine that a user connects their USB Type-C laptop into a Type-C monitor. Let us also assume that this laptop has two Type-C ports. One port supports PD with DisplayPort as an Alternate Mode at USB 3.1 speeds. The other supports only USB 2.0 over Type-C. In this case, it is likely that the monitor requires Alternate Mode to function, for example, DisplayPort for video. If the

user connects the monitor to the USB 2.0 Type-C port, the monitor will not work. If an Alternate Mode fails to be negotiated, there are two options:

1. Support USB functionality without Alternate Mode (strongly recommended for user experience)
2. Provide a USB billboard over the D+/D– lines to communicate information needed to identify the device. In the case of the monitor, once it sees that the USB 2.0 Type-C port cannot support DisplayPort, it will provide a billboard to communicate to the operating system (OS) that it requires DisplayPort to function. At this time, the OS could notify the user to use the other full-featured USB Type-C port on the laptop to support DisplayPort [7].

A full-featured system that supports Alternate Mode, PD, and USB 3.1 can be quite powerful, but also complex. Texas Instruments has solutions specifically addressing this need. For example, the TPS65982 integrates the PD manager and PHY, 20 V/3 A FET, CC logic, and can control an external SuperSpeed/ Alternate Mode MUX, such as the HD3SS460.

Appendix

Type-C pinout and reversibility

The USB Type-C connector includes several new pins compared to USB Type-A and Type-B connectors. These were added to enable additional Type-C features such as higher power, Alternate Mode, and reversibility. Referring to **Figure 13**, let us take a closer look into the pinout to understand how this is achieved.

Looking at **Figure 13** from left to right we have:

- GND: return path for signal.
- TX/RX: SuperSpeed twisted pairs for USB 3.1 data (5-10 Gbps).
- V_{BUS}: main system bus (5 V to 20 V).
- CC1/CC2: channel configuration lines used for cable detection, orientation, and current advertisement (see Type-C UFP USB2.0 without PDF). With PD, the CC lines can be used also to communicate higher power levels (see Type-C DRP/DRD USB 2.0 with PD) and Alternate Mode. Note that one of the CC lines may become VCONN (see Type-C DFP USB 2.0 without PD).
- SBU1/SBU2: sideband use (SBU) lines. These are low-speed lines used only for Alternate Mode and accessory mode. For example, with DisplayPort AUX+/AUX– are transmitted over the SBU lines. Also, for the audio adapter accessory mode, these lines are used for the microphone (mic) input and analog ground (GND).
- D+/D–: high-speed twisted pair for USB 2.0 data (up to 480 Mbps).

A new aspect of the Type-C connector is that the pins are almost symmetrical (both vertically and horizontally). This is what enables the connector to be reversible, so it can be inserted in either

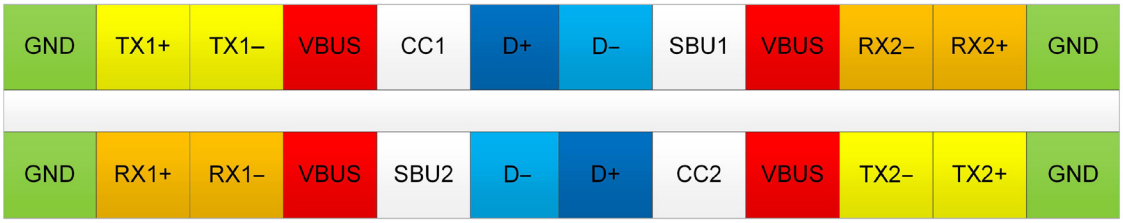

***Figure 13**. Type-C receptacle pinout.*

orientation. Unfortunately, reversibility cannot be realized just passively, so additional electronics are required for this. **Figure 14** shows that a Type-C receptacle (top) and a Type-C plug (bottom) essentially are flipped relative to each other.

Comparing the two rows (imagine stacking one on top of the other to form a connection):

- The GND and V_{BUS} lines are still in the same position.
- The D+/D– pair is also in the same orientation; however, the plug only contains one D+/D– twisted pair. The USB Type-C specification allows for the D+/D– lines to be shorted together (D+ to D+ and D– to D–) on the receptacle side. Now regardless of cable orientation, the PHY will always see the cable's D+/D– pair.
- The CC1 and CC2 lines are flipped and can be used to determine cable orientation. The orientation determines which CC line is connected and which one is left open (see Type-C UFP USB 2.0 without PD).
- The TX/RX pairs are also flipped. Resolving this was a bit more complicated. Unlike the D+/D– lines, you cannot simply short the common lines together because this will create a stub. At USB 2.0 speeds a stub is acceptable. However, at USB 3.1 speeds, it degrades signal integrity too much. To avoid this, we have two options:
  1. Use two PHYs and cable orientation detection to know which PHY to use
  2. Have a single PHY and a SuperSpeed MUX that switches the correct SuperSpeed lines to the PHY (given the known orientation). This is typically the more economical solution (see USB 3.1 SuperSpeed and SuperSpeed+).
- The SBU lines are also flipped; however, this is typically handled within the Alternate Mode PHY (remember that these are slow-speed lines).

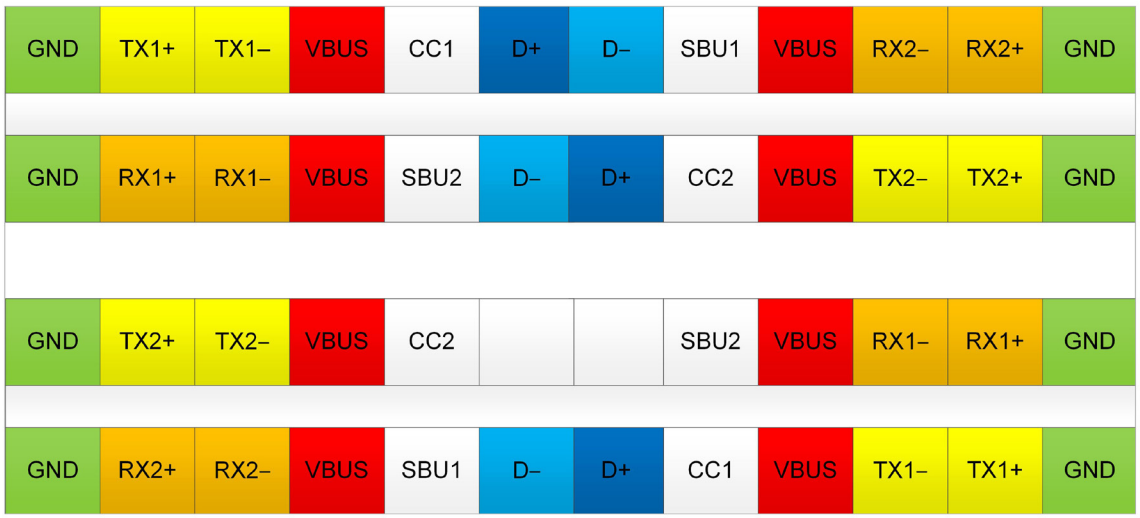

***Figure 14**. Type-C pinout – receptacle (top), plug (bottom).*

Conclusion/Summary

Although Type-C can appear to be very complicated at first, we believe that the initial learning curve is worth all the advantages highlighted in this paper. Now that we have reviewed the concepts, terms, and requirements for Type-C, you should have an understanding of what is needed to include Type-C in your next design, regardless of the application. We hope that you found this to be a great reference as you transition to Type-C, and that you will consider many of the solutions Texas Instruments has to offer for all the various Type-C applications.

For more information:

1. USB Type-C specification v1.2 for standard values of Rp and Rd, Tables 4-15 and 4-16
2. USB Type-C specification v1.2, section 4.6.2.1
3. USB Type-C specification v1.2, V_{BUS} and V_{CONN} Timing Parameters, Table 4-20
4. USB Type-C specification v1.2, USB Type-C Source Port's V_{CONN} Requirements Summary, Table 4-3
5. Deric Waters, Type-C Port Controller (TCPC) for USB-C Power Delivery, USB Developers Days 2015
6. USB Type-C specification v1.2, Figure 5-1
7. USB Type-C specification v1.2, Section 5.1

Additional information

1. Universal Serial Bus Type-C Cable and Connector Specification, Revision 1.2, March 25, 2016
2. Universal Serial Bus Power Delivery Specification, Revision 3.0, V1.0a, March 25, 2016
3. USB Type-C Version 1.2 – USB Embraces a Broader Market, Deric Waters, August 4, 2016
4. Type-C Port Controller (TCPC) for USB-C Power Delivery, Deric Waters, November 17-18, 2015

Products

Download these data sheets: TUSB320, TUSB542, TUSB1210, TUSB1310A, TPD8S300, TPS25740A, TPS65983, TPS65982, HD3SS460, HD3SS3212.

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