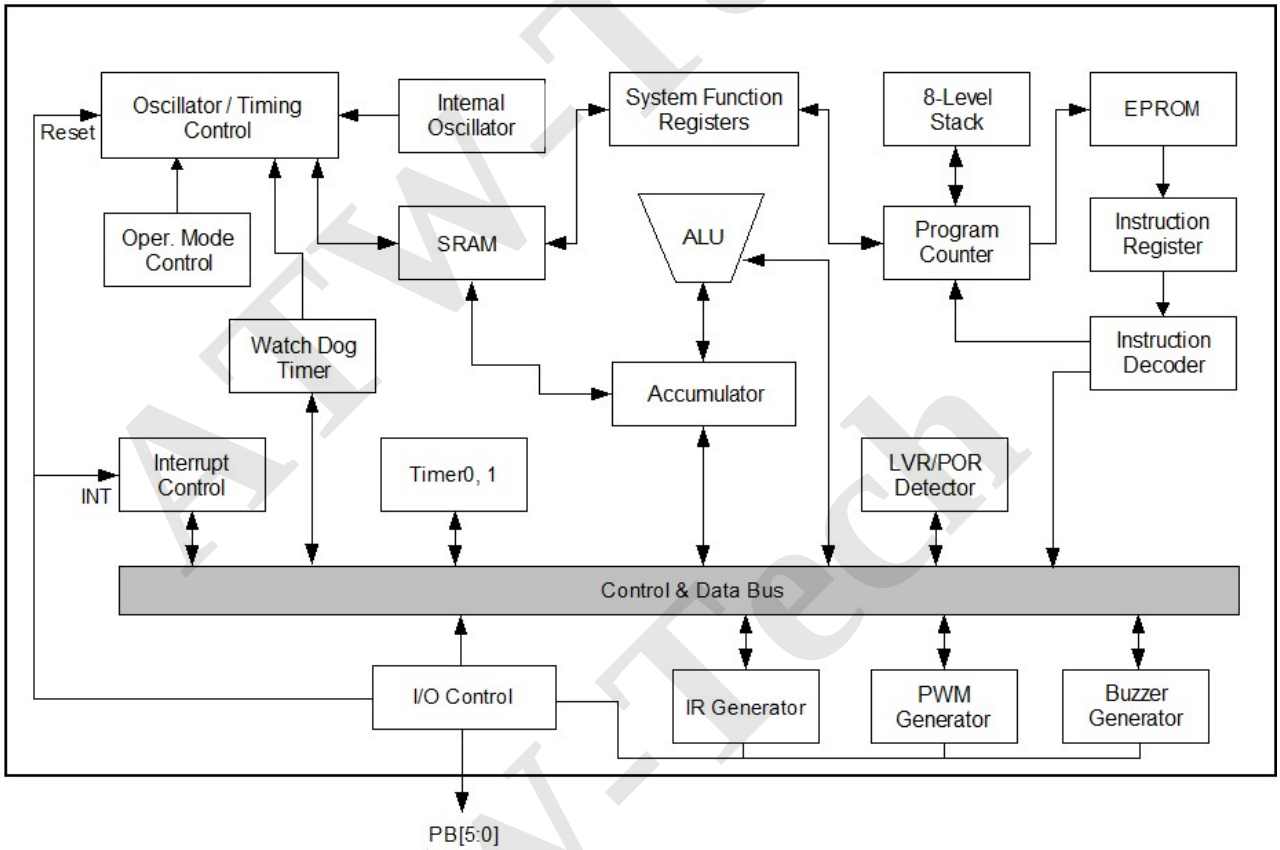
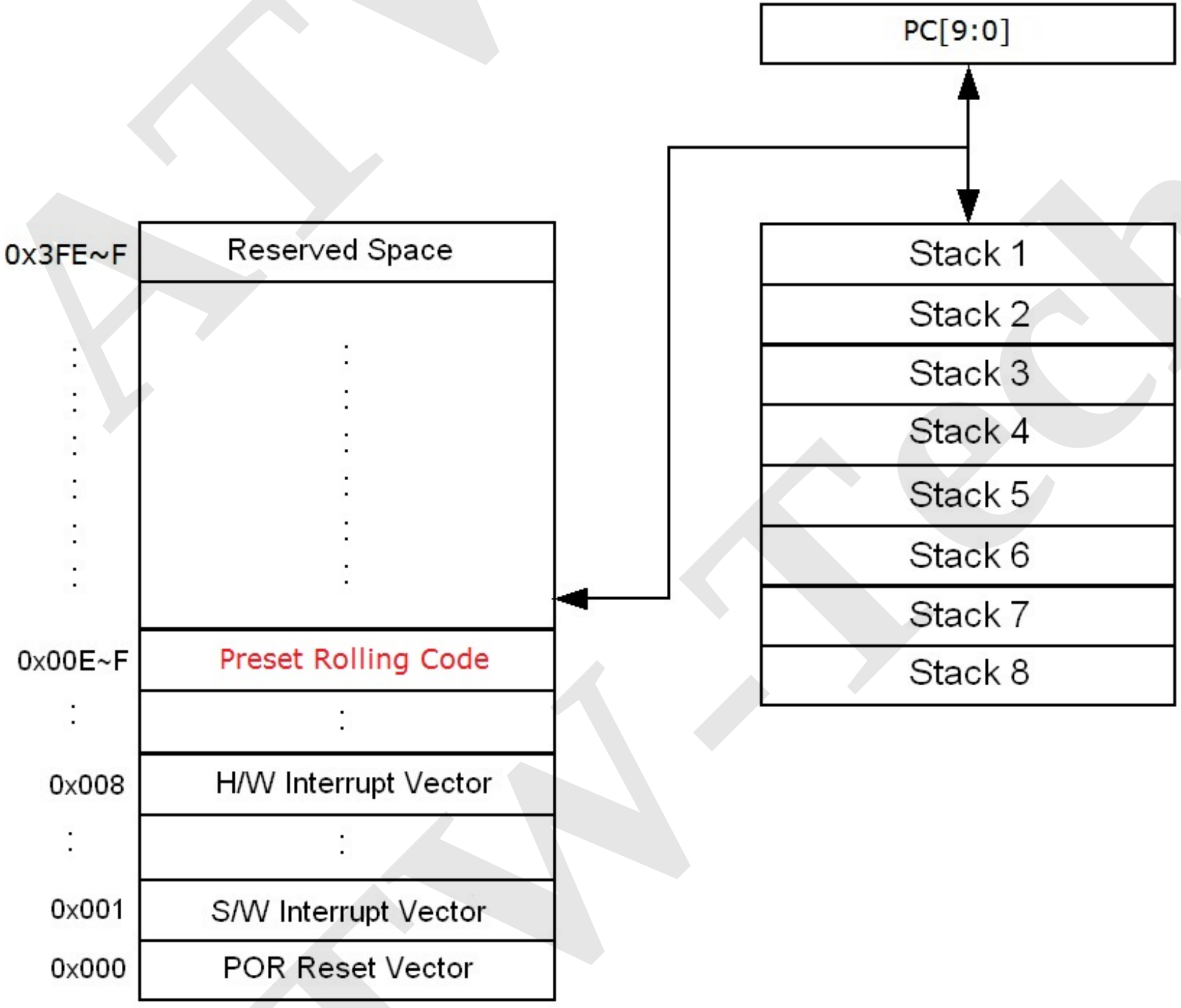


1.3 Pin Assignment

AT8A513D provides three kinds of package type which are SOP8, DIP8 and SOT23-6.

Figure 1 Package pin assignment

Pin Name	I/O	Description
PB0/ INT/ SDI	I/O	PB0 is a bidirectional I/O pin. PB0 is input pin of external interrupt when EIS=1 & INTIE=1. PB0 can be programming pad SDI.
PB1/ IR/ SDO	I/O	PB1 is a bidirectional I/O pin. If IR mode is enabled, this pin is IR carrier output. PB1 can be programming pad SDO.
PB2 / EX_CKI / PWM1 / BZ1 / SCK	I/O	PB2 is a bidirectional I/O pin. It can also be timer clock source EX_CKI. It can also be PWM output. It can also be BUZZER output. PB2 can be programming pad SCK.
PB3/ RSTb/ Vpp	I/O	PB3 is an input pin or open-drain output pin. It can be reset pin RSTb. If RSTb pin is low, it will reset AT8A513D. It can be programming pad VPP.
PB4	I/O	PB4 is a bidirectional I/O pin. PB4 also can be output of instruction clock.
PB5	I/O	PB5 is a bidirectional I/O pin.
VDD	-	Positive power supply.
VSS	-	Ground.


PC[9:0]
Stack 1
Stack 2
Stack 3
Stack 4
Stack 5
Stack 6
Stack 7
Stack 8
0x3FE~F
Reserved Space
0x00E~F
Preset Rolling Code
0x008
H/W Interrupt Vector
0x001
S/W Interrupt Vector
0x000
POR Reset Vector

The AT8A513D register name and address mapping of R-page SFR are described in the following table.

FSR[7:6] / Address	00 (Bank 0)	01 (Bank 1)	10 (Bank 2)	11 (Bank 3)
0x0	INDF	The same mapping as Bank 0		
0x1	TMR0			
0x2	PCL			
0x3	STATUS			
0x4	FSR			
0x5	-			
0x6	PORTB			
0x7	-			
0x8	PCON			
0x9	BWUCON			
0xA	PCHBUF			
0xB	BPLCON			
0xC	BPHCON			
0xD	-			
0xE	INTE			
0xF	INTF			
0x10 ~ 0x1F	General Purpose Register	Mapped to bank0		
0x20 ~ 0x3F	General Purpose Register	Mapped to bank0		

Table 1 R-page SFR Address Mapping

SFR Category / Address	F-page SFR	S-page SFR
0x0	-	TMR1
0x1	-	T1CR1
0x2	-	T1CR2
0x3	-	PWM1DUTY
0x4	-	PS1CV
0x5	-	BZ1CR
0x6	IOSTB	IRCR
0x7	-	TBHP
0x8	-	TBHD
0x9	-	-
0xA	PS0CV	-
0xB	-	-
0xC	BODCON	-
0xD	-	-
0xE	-	-
0xF	PCON1	OSCCR

Table 2 F-page and S-page SFR Address Mapping

4. Instruction Set

AT8A513D provides 55 powerful instructions for all kinds of applications.

Inst.	OP 1	OP 2	Operation	Cyc.	Flag
Arithmetic Instructions					
ANDAR	R	d	dest = ACC & R	1	Z
IORAR	R	d	dest = ACC | R	1	Z
XORAR	R	d	dest = ACC ⊕ R	1	Z
ANDIA	i		ACC = ACC & i	1	Z
IORIA	i		ACC = ACC | i	1	Z
XORIA	i		ACC = ACC ⊕ i	1	Z
RRR	R	d	Rotate right R	1	C
RLR	R	d	Rotate left R	1	C
BSR	R	bit	Set bit in R	1	-
BCR	R	bit	Clear bit in R	1	-
INCR	R	d	Increase R	1	Z
DECR	R	d	Decrease R	1	Z
COMR	R	d	dest = ~R	1	Z
Conditional Instructions					
BTRSC	R	bit	Test bit in R, skip if clear	1 or 2	-
BTRSS	R	bit	Test bit in R, skip if set	1 or 2	-
INCRSZ	R	d	Increase R, skip if 0	1 or 2	-
DECRSZ	R	d	Decrease R, skip if 0	1 or 2	-
Data Transfer Instructions					
MOVAR	R		Move ACC to R	1	-
MOVR	R	d	Move R	1	Z
MOVIA	i		Move immediate to ACC	1	-
SWAPR	R	d	Swap halves R	1	-
IOST	F		Load ACC to F-page SFR	1	-
IOSTR	F		Move F-page SFR to ACC	1	-
SFUN	S		Load ACC to S-page SFR	1	-
SFUNR	S		Move S-page SFR to ACC	1	-
T0MD			Load ACC to T0MD	1	-
T0MDR			Move T0MD to ACC	1	-
TABLEA			Read ROM	2	-

Inst.	OP 1	OP 2	Operation	Cyc.	Flag
Arithmetic Instructions					
ADDAR	R	d	dest = R + ACC	1	Z, DC, C
SUBAR	R	d	dest = R + (~ACC)	1	Z, DC, C
ADCAR	R	d	dest = R + ACC + C	1	Z, DC, C
SBCAR	R	d	dest = R + (~ACC) + C	1	Z, DC, C
ADDIA	i		ACC = i + ACC	1	Z, DC, C
SUBIA	i		ACC = i + (~ACC)	1	Z, DC, C
ADCIA	i		ACC = i + ACC + C	1	Z, DC, C
SBCIA	i		ACC = i + (~ACC) + C	1	Z, DC, C
DAA			Decimal adjust for ACC	1	C
CMPAR	R		Compare R with ACC	1	Z, C
CLRA			Clear ACC	1	Z
CLRR			Clear R	1	Z
Other Instructions					
NOP			No operation	1	-
SLEEP			Go into Halt mode	1	/TO, /PD
CLRWDT			Clear Watch-Dog Timer	1	/TO, /PD
ENI			Enable interrupt	1	-
DISI			Disable interrupt	1	-
INT			Software Interrupt	3	-
RET			Return from subroutine	2	-
RETIE			Return from interrupt and enable interrupt	2	-
RETIA	i		Return, place immediate in ACC	2	-
CALLA			Call subroutine by ACC	2	-
GOTOA			unconditional branch by ACC	2	-
CALL	adr		Call subroutine	2	-
GOTO	adr		unconditional branch	2	-
LCALL	adr		Call subroutine	2	-
LGOTO	adr		unconditional branch	2	-

Table 13 Instruction Set

5. Configuration Words

Item	Name	Options
1	High IRC Frequency	1. 1MHz 2. 2MHz 3. 4MHz 4. 8MHz 5. 16MHz 6. 20MHz
2	Instruction Clock	1. 2 oscillator period 2. 4 oscillator period
3	WDT	1. Watchdog Enable (Software control) 2. Watchdog Disable (Always disable)
4	WDT Event	1. Watchdog Reset 2. Watchdog Interrupt
5	Timer0 source	1. EX_CKI 2. I_LRC
6	PB.2	1. PB.2 is I/O 2. PB.2 is PWM 3. PB.2 is Buzzer
7	PB.3	1. PB.3 is I/O 2. PB.3 is reset
8	PB.4	1. PB.4 is I/O 2. PB.4 is instruction clock output
9	Startup Time	1. 140us 2. 4.5ms 3. 18ms 4. 72ms 5. 288ms
10	WDT Time Base	1. 3.5ms 2. 15ms 3. 60ms 4. 250ms
11	LVR Setting	1. Register Control 2. LVR Always On
12	LVR Voltage	1. 1.6V 2. 1.8V 3. 2.0V 4. 2.2V 5. 2.4V 6. 2.7V 7. 3.0V 8. 3.3V 9. 3.6V 10. 4.2V
13	VDD Voltage	1. 3.0V 2. 4.5V 3. 5.0V
14	Read Output Data	1. I/O port 2. Register
15	EX_CKI to Inst. Clock	1. Sync 2. Async
16	Startup Clock	1. I_HRC 2. I_LRC
17	Input High Voltage (VIH)	1. CMOS (0.7VDD) 2. TTL (0.5VDD)
18	Input Low Voltage (VIL)	1. CMOS (0.3VDD) 2. TTL (0.2VDD)

Table 14 Configuration Words