Embedded USB2 (eUSB2) Physical Layer Supplement to the USB Revision 2.0 Specification

Revision 1.1

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Contributors

Walter Fry	Advanced Micro Devices
Will Harris	Advanced Micro Devices
Jason Hawken	Advanced Micro Devices
Stephen Liu	Advanced Micro Devices
Joseph Scanlon	Advanced Micro Devices
Peter Teng	Advanced Micro Devices
YiChun Chen	Apple Inc.
Will Ferry	Apple Inc.
Chengyun Gao	Apple Inc
Derek Iwamoto	Apple Inc.
Scott Jackson	Apple Inc.
Ketan Sharma	Apple Inc.
Dae Woon Kang	Broadcom Corp.
Kenneth Ma	Broadcom Corp.
Desheng Ma	Broadcom Corp.
Ravi Nukala	Broadcom Corp.
Narayan Prasad Ramachandran	Broadcom Corp.
Derek Tam	Broadcom Corp.
Suresh Venkatesan	Broadcom Corp.
Jing Wang	Broadcom Corp.
Rangarajan Sundaravaradan	Cypress Semiconductor
Marcin Behrendt	Cadence Design Systems, Inc.
Pawel Eichler	Cadence Design Systems, Inc.
Jerry Chen	Genesys Logic, Inc.

Weddell Lee	Genesys Logic, Inc.
Miller Lin	Genesys Logic, Inc.
Yihsun Wu	Genesys Logic, Inc.
Alan Berkema	Hewlett Packard
Dinesh Tyagi	Innovative Logic
Kok Hong Chan	Intel Corporation
Huimin Chen	Intel Corporation
Pelle Fornberg	Intel Corporation
Abdul Ismail	Intel Corporation
Tan Kevin Beow Ee	Intel Corporation
Jia Jun Lee	Intel Corporation
Chia How Low	Intel Corporation
Tim McKee	Intel Corporation
Florence Phun	Intel Corporation
Brad Saunders	Intel Corporation
Amit Srivastava	Intel Corporation
Bih Qui Tiang	Intel Corporation
Karthi Vadivelu	Intel Corporation
Teong Guan Yew	Intel Corporation
Mark Davis	Lenovo
Dave Thompson	LSI Corporation
Srinivas Vura	LSI Corporation
Mark Bohm	Microchip - SMSC
Morgan Monks	Microchip - SMSC
Tsungyen Liu	MOAI ELECTRONICS CORPORATION
Chin Tsai	MOAI ELECTRONICS CORPORATION
Jason Chen	NXP Semiconductors
Stefan Kwaaitaal	NXP Semiconductors
Guru Prasad	NXP Semiconductors
Bart Vertenten	NXP Semiconductors
Vijendra Kuroodi	NXP Semiconductors
Philip Leung	Renesas Electronics Corp.
Kiichi Muto	Renesas Electronics Corp.
Nathalie Ballot	STMicroelectronics
Andrew Cofler	STMicroelectronics
Nicolas Darbel	STMicroelectronics
Anubhav Tripathi	STMicroelectronics
Tim Blankenship	Synaptics Inc.
Roberto Colecchia	Synaptics Inc.
Jechan Kim	Synaptics Inc.
Subramaniam Aravindhan	Synopsys, Inc.
Chandrashekar B U	Synopsys, Inc.
Bala Babu	Synopsys, Inc.
Adam Burns	Synopsys, Inc.
Morten Christiansen	Synopsys, Inc.
Eric Huang	Synopsys, Inc.
Venkataraghavan Krishnan	Synopsys, Inc.
Behram Minwalla	Synopsys, Inc.

Saleem Mohammad	Synopsys, Inc.
Matthew Myers	Synopsys, Inc.
Abhishek Chowdhary	Synopsys, Inc.
Chaitanya K	Synopsys, Inc.
Grant Ley	Texas Instruments
Win Maung	Texas Instruments
Sue Vining	Texas Instruments
Li Yang	Texas Instruments

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1 Preface

1.1 *Scope of this Revision*

This supplement defines eUSB2 PHY layer requirement and signaling attributes. Protocol behavior which is not explicitly called out in this document shall remain the same as defined in USB Revision 2.0 specification.

1.2 *Revision History*

Revision Number	Date	Description
1.0	1 August, 2014	Initial release
1.1	20 August 2018	Updated Release containing all ECNs

2 Introduction

2.1 *Acronyms and Terms*

This section lists and defines terms and abbreviations used throughout this specification.

Table 2-1: Acronyms

Acronyms	Terms
Attach	This specification makes a distinction between the words “attach” and “connect”. A downstream device is attached to an upstream port when there is a physical cable between the two
Analog Ping	An analog pulse of a differential signal with variable pulse width used by an upstream eUSB2 port in high-speed operation to indicate its presence
Connect	A downstream device is connected to an upstream port when it is attached to the upstream port, and when the downstream device has pulled either the D+ or D- data line high through a 1.5 kΩ resistor, to enter low-speed, full-speed or high-speed signaling.
D+	USB2 data+ pin
D-	USB2 data- pin
DRD	Dual role device capable of host function and device function
DSP	Downstream port
Digital Ping	A single-ended digital pulse of various pulse width used in the eUSB2 operation as a ping or an acknowledgement
Downstream	The direction of data flow from the host or away from the host. A downstream port is the port on a hub/repeater toward the Device direction that generates downstream data traffic from the hub. Downstream ports receive upstream data traffic
eD+	eUSB2 data+ pin
eD-	eUSB2 data- pin
eDSPn	Downstream eUSB2 port in native mode
eDSPp	Downstream eUSB2 port of the peripheral repeater
eDSPr	Downstream eUSB2 port facing host repeater
EOS	Electrical Over Stress
ESE1	Extended SE1
eUSBr	An eUSB port which has yet to be configured (dual-role) by its associated controller, or a downstream or upstream port which has yet to configure its repeater for host or device operation.
eUSPh	Upstream eUSB2 port of the host repeater
eUSPn	Upstream eUSB2 port in native mode
eUSPr	Upstream eUSB2 port facing peripheral repeater
FS	Full-speed
HS	High-speed
LPM	Link Power Management
LS	Low-speed
Lx	Link power management states, includes both L1 and L2.
L1	LPM-L1
L2	Suspend
POR	Power On Reset
RAP	Register Access Protocol
Redriver	Non-retiming repeater
Retimer	Retiming repeater

Acronyms	Terms
Repeater	General term of a bridge. In this specification, it refers to a non-linear eUSB2-USB2 redriver.
SCM	Start of Control Message
SDP	Standard downstream port
SE0	Single Ended Zero
SE1	Single Ended One
SoC	System-on-chip
Upstream	The direction of data flow towards the host. An upstream port is the port on a device toward the Host direction that generates upstream data traffic from the hub/repeater. Upstream ports receive downstream data traffic.
UUSP	Upstream USB2.0 port of the peripheral repeater
UDSP	Downstream USB2.0 port of the host repeater
USB OTG	USB On-the-go
USB session	The lifetime of a USB port in connected state
UTMI/UTMI+	The interface between the protocol layer and the eUSB2 PHY. Refer to the UTMI/UTMI+ specification.
Walk-up port	Ports which have physical connectivity through the connector

2.2 *Terminology*

“Shall” is normative and used to indicate mandatory requirements which are to be followed strictly in order to conform to this standard.

“Should” is normative and used to indicate a recommended option or possibility.

“May” is normative and used to indicate permitted behavior.

“Can” is informative and used to indicate behavior which is possible or may be seen.

The use of “must” and “will” is deprecated for requirements and shall only be used for statements of fact.

2.3 *Motivation*

The success of USB2.0 technology has enjoyed wide adoption in almost every computing device, with tremendous ecosystem support not only in terms of device choice to support various platform features, but also in terms of technology development with well-established hardware IP portfolios and standardized software infrastructure. It is foreseeable that the great asset of USB2.0 technology will continue to benefit the ecosystem for years to come.

As power efficiency becomes increasingly critical in today’s computing devices, there is a need for IO technology to be optimized for both active and idle power. USB2.0 technology, originally optimized for external device interconnect, is primed to be enhanced for inter-chip interconnect such that the link power can be further optimized.

Meantime, silicon technology continues to scale. Device dimensions are getting smaller and therefore more devices can be packed onto a single integrated chip. However, the device reliability challenge arising from the densely packed transistors has become more profound. The manufacturing cost for an advanced process technology to support 3.3V IO signaling has grown exponentially. A low voltage USB2.0 solution is therefore required to address the gap.

In summary, eUSB2 is introduced to address the following:

1. IO Power Efficiency
   - Improve both the link active and idle power efficiency.
2. Process scalability
   - Provide a low voltage USB2.0 PHY solution to eliminate 3.3V IO signaling requirement, which allows the process technology to continue to scale for many generations to come.
3. Implementation simplicity
   - The PHY analog content is reduced. Digital mechanisms are employed for PHY functionality, for example, device disconnect detect.
4. Support both USB2.0 inter-chip and out-of-the-box devices
   - Though eUSB2 and USB2.0 are not electrically compatible, a mechanism is defined for eUSB2 to support standard USB2.0 devices.

Table 2-2 tabulates the key attributes of eUSB2 technology in comparison to other USB interfaces.

Table 2-2: Comparison of Various USB Interfaces

	USB2	**IC-USB**	**HSIC**	**ULPI**	**eUSB2**
Interface Pin (SoC view)	2-pin	2-pin	2-pin	12-pin	2-pin
Supported data rate	low-speed, full-speed and high-speed	low-speed and full-speed	high-speed	low-speed, full-speed and high-speed	low-speed, full-speed and high-speed
Connectivity	Inter-chip and out-of-the-box	Inter-chip	Inter-chip	Inter-chip	Inter-chip and out-of-the-box USB2.0 connectivity through repeater
Signaling Voltage Requirement	Max 3.3V	Multiple voltage classes, from 1V to 3.3V	1.2V	Vendor specific. Typically 1.8V and 3.3V	Max 1V
Recommended trace length support	Long	short	short	short	Medium to long

2.4 *eUSB2 PHY Feature*

eUSB2 is fully compliant to the USB2.0 layer architecture with the following features and characteristics:

- Supports high-speed, full-speed, and low-speed operation.
  - High-speed:
    - Low voltage differential signaling
  - Low-speed/Full-speed:
    - Single-ended digital low-voltage signaling.
- Supports selected single speed configuration in native mode.
- Supports USB2.0 operation based on repeater architecture.
- Supports link power management LPM-L1 (L1) and Suspend (L2).
- eUSB2 implementation is based on UTMI/UTMI+ Parallel Mode. FS/LS Serial Mode is out of scope for eUSB2. Note that implementations based on UTMI/UTMI+ may vary. In the rest of the specification, UTMI/UTMI+ is quoted as a reference to describe the interface between the protocol layer and the eUSB2 PHY.
- Supports register access protocol (RAP) for eUSB2 device or repeater configurations.
- Fully compliant to USB2.0 base spec at the protocol layer.
- No change to USB2.0 software programming model.
- Not compatible with the physical layer defined by USB2.0.
- Not compatible with standard USB2.0 connectors defined by USB2.0 and its derivatives.

Shown in Figure 2-1 is a description of eUSB2 scope. An implementation that supports UTMI/UTMI+ as the standard interface between the protocol layer and the physical layer is used as an example.

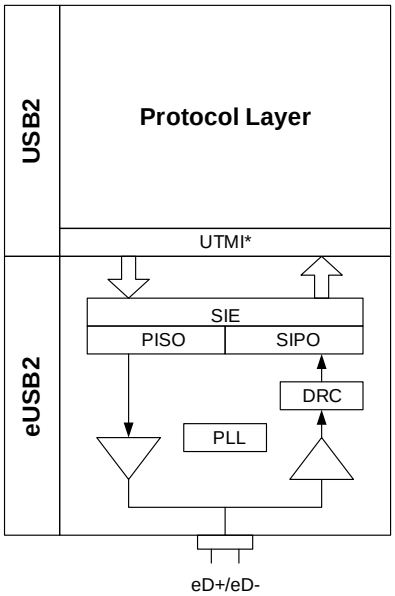


Figure 2-1: eUSB2 Under USB2.0 Layer Architecture

2.5 *eUSB2 Modes of Operation*

eUSB2 supports two modes of operation: native mode and repeater mode.

Native mode refers to a host port and a device port both implementing an eUSB2 PHY and communicating based on eUSB2 signaling. Native mode eUSB2 is used for inter-chip interconnect. Single speed configuration is allowed in native mode.

Repeater mode refers to an eUSB2 port communicating with a USB2.0 port through a repeater that translates between eUSB2 signaling and USB2.0 signaling. Repeater mode may also be used between two eUSB2 ports communicating with each other through two repeaters, such a case typically involves applications with USB2.0 receptacles at both sides of the ports.

Example usages of eUSB2 in native mode and repeater mode are shown in Figure 2-2 and Figure 2-3. Note that Figure 2-3, both the SOCs and repeaters may be dual role capable. Later sections in the specification describe the configuration and operation of this.

An eUSB2 implementation on an SoC may support both native mode and repeater mode operation with slight differences in accommodation for repeater operation. This gives the system designer the flexibility to determine the mode of operation of the eUSB2 port on an SoC.

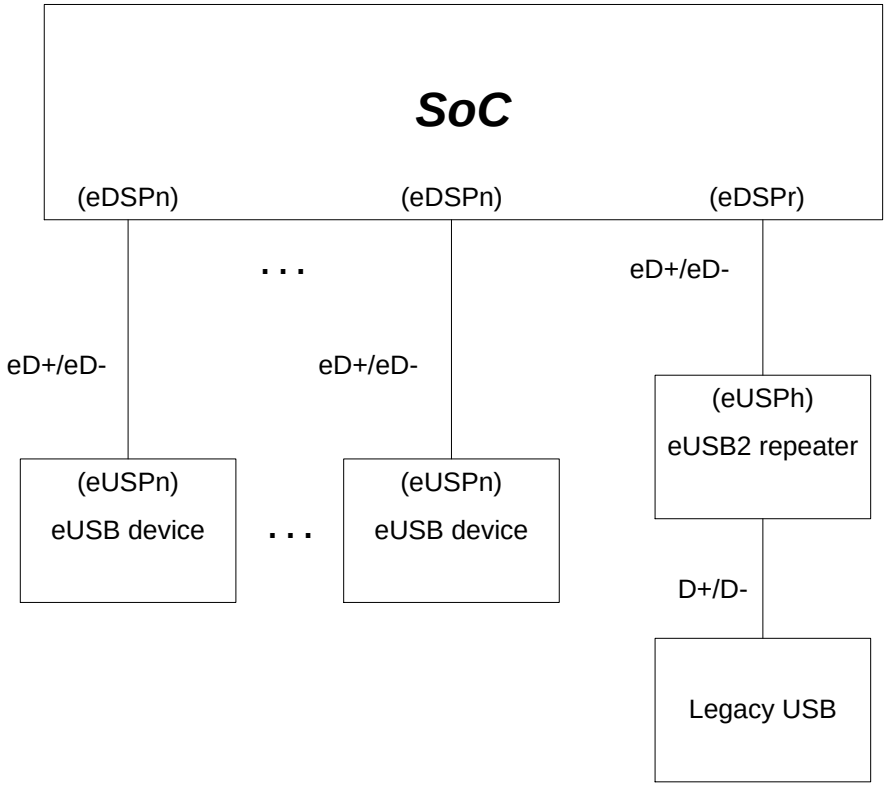


Figure 2-2: Typical eUSB2 Use Cases

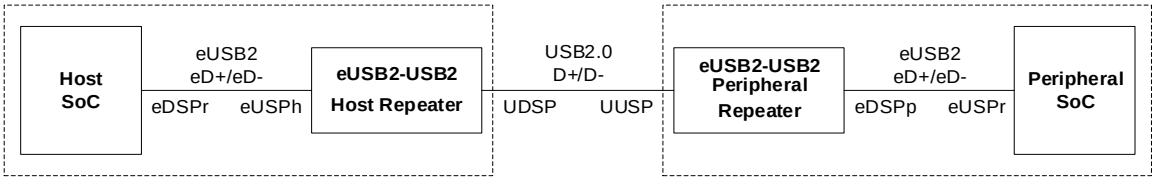


Figure 2-3: Example eUSB2 With Host and Device Side Repeaters

Table 2-3 describes the number of hubs that are supported relative to the number of eUSB2 repeaters present between the host and peripheral where all the hubs are operating at HS or all are operating at FS. It does not attempt to define mixed use cases, where one or more hubs connected at the host operate at HS and one or more at the peripheral operate at FS. Per USB 2.0, a HS-capable hub must operate at FS when its upstream-facing port is connected behind a host or hub that is operating at FS or that is not HS-capable. A legacy USB 1.x host or hub is not HS-capable and necessarily operates at FS.

Table 2-3: Number of Hubs Supported with Host and/or Peripheral Repeater

Number of eUSB2 Repeaters	Number of Hubs Operating at HS	Number of Hubs Operating at FS	Notes
1	4	2	Number of hubs operating at FS is reduced due to $T_{e\_to\_U\_DJ1}$ and T_{RJR1}. Number of hubs operating at HS is reduced due to SOP truncation and EOP dribble
2	3	1	
0	5	5	non-eUSB2 system for reference

2.6 *Related Documents*

eUSB2 only defines the physical layer. The protocol layer is defined in the USB2.0 base specification.

The following is a list or related documents:

USB2.0	Universal Serial Bus Revision 2.0 Specification including ECNs and errata.
[USB2 OTG]	On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification.
[USB Type-C]	Universal Serial Bus Type-C Cable and Connector Specification Revision 1.3
[UTMI+ v1.0]	USB 2.0 Transceiver Macrocell Interface Plus (UTMI+) Specification.

3 eUSB2 PHY Architecture and Operation

This chapter describes the eUSB2 PHY architecture and its operation. Although the focus is on native mode, most of native mode operation also applies to repeater mode.

3.1 *PHY Architecture*

A conceptual block diagram of the eUSB2 PHY is shown in Figure 3-1. It supports three data rates defined by USB2.0. A differential transceiver and a low power squelch detector is needed for data transfer at high-speed. Two pairs of single-ended CMOS buffers are employed to carry out low-speed/full-speed data transfer, control signaling during initialization and link power state transitions.

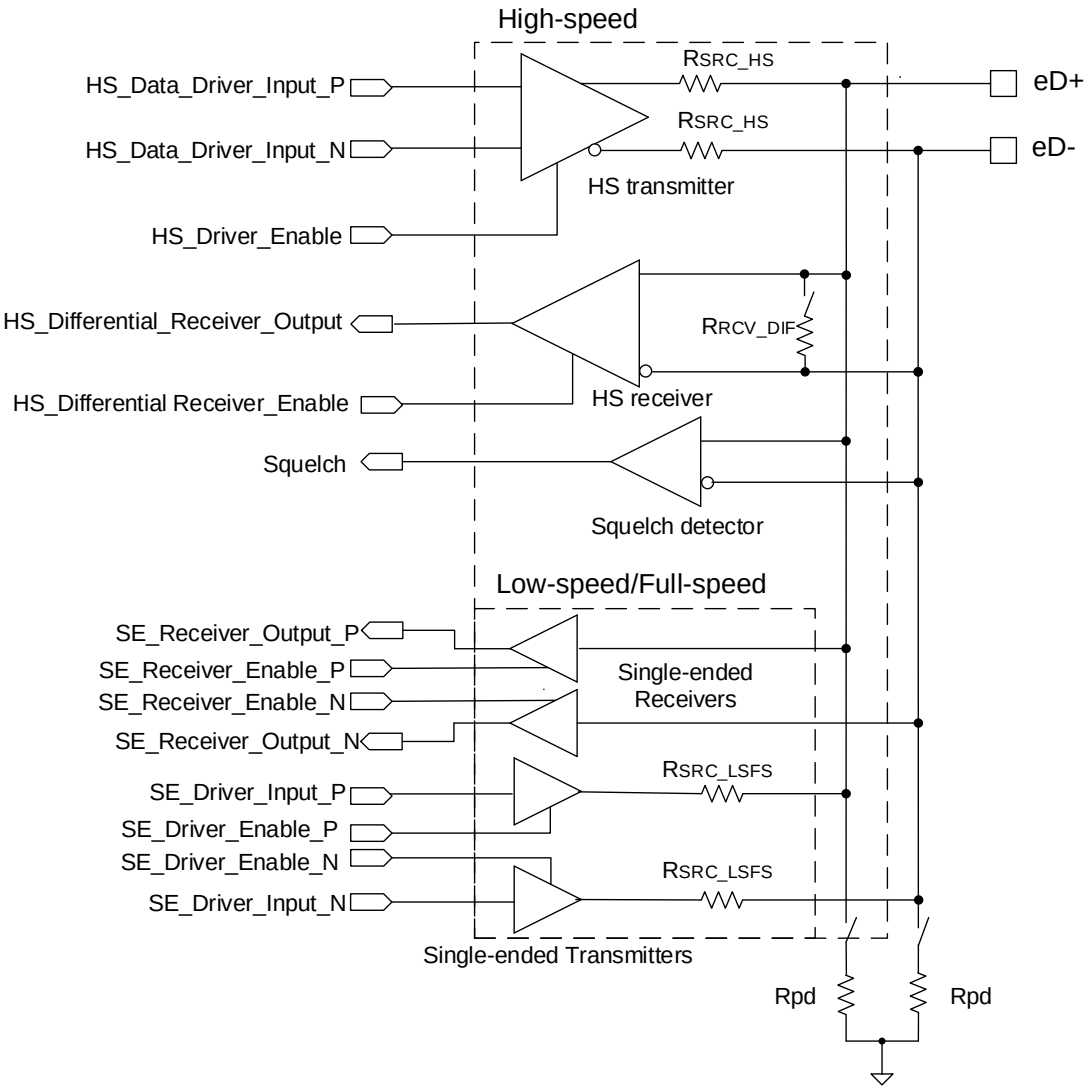


Figure 3-1: eUSB2 Physical Layer Transceiver Block Diagram

An eUSB2 implementation shall contain the following building elements:

- A port shall implement two pull-downs, R_{PD}, intended to hold the bus to ground during power-up or when the link is idle. Note: Under general scenario, upon powered up,

these pull-downs shall always be enabled. It is implementation specific to allow disabling for testing or debug.

- A low-speed/full-speed eUSB2 port is fully digital. A low-speed/full-speed transceiver shall meet the following requirements:
  - The port shall implement a pair of low-speed/full-speed single-ended transmitters.
  - The port shall implement a source-series termination at each transmitter.
  - The port shall implement a pair of low-speed/full-speed single-ended receivers.
- A high-speed transceiver shall meet the following requirements:
  - The port shall implement an analog transceiver for low swing differential signaling.
  - The port shall employ embedded clocking compliant to USB2.0.
  - The port shall implement a squelch detector.
  - The port shall implement a source-series termination at its transmitter.
  - If enabled, the port shall implement a differential receiver termination with the center tap capacitance to ground. Note that not employing ground termination of the differential receiver termination is to avoid overloading the SE (Single-ended) transmitter in HS operation when a control message may be issued during HS idle. Refer to Section 3.3.7 for control message definition.
  - The receiver termination shall always be enabled in repeater mode
  - The default receiver termination shall be disabled in native mode. A downstream port may alter the termination scheme during Port Configuration. Refer to Section 4.2.2 for the details.

3.2 *Bus State and Signaling*

3.2.1 **Low-speed/Full-speed Bus State and Signaling**

To differentiate low-speed from full-speed signaling, all low-speed signaling is the inverse of full-speed (eD+ and eD- are swapped), except for control message signaling.

Table 3-1 defines the low-speed/full-speed bus states and their associated signaling.

Table 3-1: eUSB2 Low-speed/Full-speed Bus State Representations

Bus State		Signaling Levels	
		At the Transmitter	At the Receiver
Logic ‘1’		> V_{OH}(min)	> V_{IH}(min)
Logic ‘0’		< V_{OL}(max)	< V_{IL}(max)
Single-ended 0 (SE0)[1]		Logic ‘0’ at eD-; Logic ‘0’ at eD+	
Single-ended 1 (SE1)		Logic ‘1’ at eD-; Logic ‘1’ at eD+	
Data J state[2]	FS	Logic ‘0’ at eD- Logic ‘0’ at eD+	
Data K state[2]		Logic ‘1’ at eD- Logic ‘0’ at eD+	
SE0 at D+/D- (repeater mode only)[3]		Logic ‘0’ at eD- Logic ‘1’ at eD+	
SE1 at D+/D- (repeater mode only)[4]		Logic ‘0’ at eD-; Logic ‘0’ at eD+	
Data J state	LS	Logic ‘0’ at eD- Logic ‘0’ at eD+	
Data K state		Logic ‘0’ at eD- Logic ‘1’ at eD+	
SE0 at D+/D- (repeater mode only)[3]		Logic ‘1’ at eD- Logic ‘0’ at eD+	
SE1 at D+/D- (repeater mode only)[4]		Logic ‘0’ at eD-; Logic ‘0’ at eD+	
Idle state		SE0	
Resume/Remote Wake state[5]		Data K	

Note 1: Drive to SE0 and maintain SE0 through R_{PD}.
Note 2: Valid after connect.
Note 3: For USB 2.0 Bus Reset mapping at Peripheral eD+/eD-, EOP at D+/D- mapping to EOP at eD+/eD-, SE0 detection at D+/D- for disconnect at host eD+/eD-. Refer to Section 0 for bus state mapping details in repeater operations.
Note 4: For USB 2.0 D+/D- K-J or J-K crossing to both host and peripheral eD+/eD-, or any scenario where repeater is repeating/receiving D+/D- with differential receiver and transmitting single ended signaling to eD+/eD-. Refer to Section 3.3.3 for Glitch Filtering in FS/LS repeater mode operation.
Note 5: Refer to Section 0.5 and 3.3.6 for special signaling of Resume/Remote Wake sequence in repeater operations.

3.2.2 Low-speed/Full-speed Idle State Transition

Low-speed/Full-speed idle state (SE0) is maintained by the pull-down resistors (R_{PD}) implemented at a downstream port. To ensure a swift transition to idle state (SE0) or logic ‘0’, the port shall drive the bus to SE0 or logic ‘0’ for $T_{SE0\_DR\_LSFS}$ when transitioning from a non-SE0 before disabling its transmitters to allow the pull-down resistor to hold SE0. Refer to Table 7-16 for timing detail.

3.2.3 High-speed Bus state and Signaling

High-speed bus states of J and K are maintained by driving low swing differential voltage on eD+ and eD- during terminated and un-terminated conditions. Figure 3-2 defines the high transmitting signals at eD+ and eD-, each is denoted as $V_{TX(eD+)}$ and $V_{TX(eD-)}$. The differential signal $V_{TX\_DIF\_TERM}$ (when terminated) or $V_{TX\_DIF\_UNTERM}$ (when un-terminated) and the common mode signal V_{TX_CM} are then represented by the following:

$$V_{TX\_DIF} = V_{TX(eD+)} - V_{TX(eD-)}$$

$$V_{TX\_CM} = \frac{V_{TX(eD+)} + V_{TX(eD-)}}{2}$$

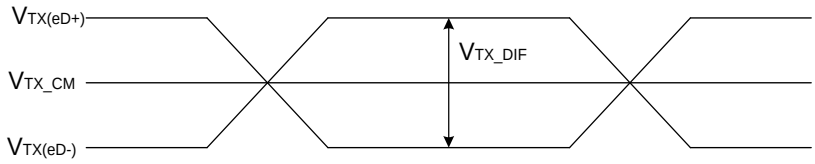


Figure 3-2: High-speed Differential Signal Representations

Accordingly, the differential and common mode signals at the receiving port can be similarly represented by the following equations:

$$V_{RX\_DIF\_UNTERM} = V_{RX(eD+)\_UNTERM} - V_{RX(eD-)\_UNTERM}$$

$$V_{RX\_DIF\_TERM} = V_{RX(eD+)\_TERM} - V_{RX(eD-)\_TERM}$$

$$V_{RX\_CM} = \frac{V_{RX(eD+)} + V_{RX(eD-)}}{2}$$

Table 3-2: eUSB2 High-speed Bus State Representations

Bus State		At the source	At the sink
Differential '1'	Terminated	$V_{TX\_DIF} > V_{TX\_DIF\_TERM}$(min)	$V_{RX\_DIF} > V_{RX\_DIF\_SENS}$(min)
	Unterminated	$V_{TX\_DIF} > V_{TX\_DIF\_UNTERM}$(min)	
Differential '0'	Terminated	$V_{TX\_DIF} < -V_{TX\_DIF\_TERM}$(min)	$V_{RX\_DIF} < -V_{RX\_DIF\_SENS}$(min)
	Unterminated	$V_{TX\_DIF} < -V_{TX\_DIF\_UNTERM}$(min)	
Squelch state		NA	AC: $V_{RX\_DIF} < V_{SQUELCH\_DIF}$(min) $V_{RX\_DIF} > -V_{SQUELCH\_DIF}$(min)
Data J state:		Differential '1'	
Data K state:		Differential '0'	
L0 idle/L1/L2 state		SE0	
Start-of-Packet (SOP)		Same as USB2.0	
End-of-Packet (EOP)		Same as USB2.0	
End-of-Packet(EOP of uSOF in Native Mode)		8 UIs	
Resume/Remote Wake		Same as FS. Refer to Section 0.5 and 3.3.6 for details.	

3.2.4 **High-speed Idle State Transition**

High-speed idle state is maintained by the pull-down resistors implemented at a downstream port. To ensure a swift transition to idle state (SE0), the port shall drive the bus to SE0 for $T_{SE0\_DR\_HS}$ when transitioning from a non-SE0 to idle (SE0) (i.e. at the end of EOP) before disabling its transmitters. Refer to Table 7-16 for timing detail.

3.2.5 **High-speed Squelch Operation**

The squelch detector is used by the port to detect high-speed line activity. It is also used under the following scenarios for eDSPn/eUSPn and eUSPh/eDSPp to control the SE receivers.

- When in un-squelched condition, an eUSPn, or eUSPh/eDSPp port receiving high-speed data may optionally disable its single-ended receivers.
- Under squelched condition, an eDSPn/eUSPn port shall turn on its single-ended receiver in anticipation of device soft disconnect or [USB 2.0] bus reset. And eUSPh or eDSPp port shall turn on its SE receivers in anticipation of a control message from eDSPr or eUSPr.

3.3 *Single-ended (SE) Signaling*

eUSB2 employs SE signaling for low-speed/full-speed packet transmission in L0. The SE signal is also used for interactions between the two ports. Interactions include connect, reset, resume, remote wake, high-speed detection and control message. The interpretation of the SE signals depends on the link state, and the start of the SE signal.

3.3.1 FS/LS SYNC and EOP

- In FS operation, an eUSB2 port shall drive the SYNC pattern on eD- while maintaining logic ‘0’ on eD+ through R_{PD}. This is illustrated in Figure 3-3.
- In LS operation, an eUSB2 port shall drive the SYNC pattern on eD+ while maintaining logic ‘0’ on eD- through R_{PD}. This is illustrated in Figure 3-3.

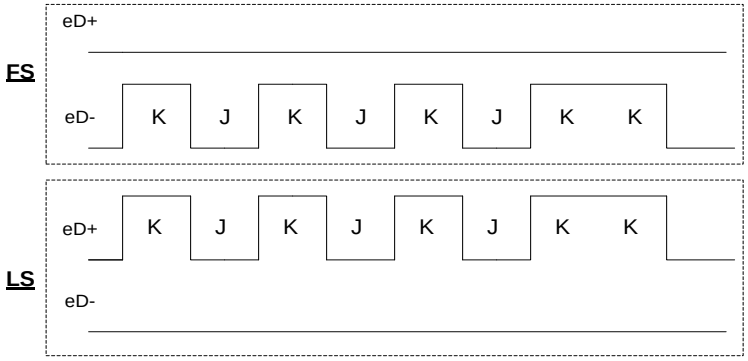


Figure 3-3: FS/LS SYNC Pattern

- A FS eUSB2 EOP, transmitted by eDSPn, eDSPr, eUSPn or eUSPr, shall be 3 UIs with the first UI of logic ‘1’, followed by the second UI of logic ‘0’, and a third UI of logic ‘1’ at eD+, while eD- is maintained at logic ‘0’ through R_{PD}. This is shown in Figure 3-4. Similarly, a LS EOP shall be 3 UIs with the first UI of logic ‘1’, followed by a second UI of logic ‘0’, and the third UI of logic ‘1’ at eD-, while eD+ is maintained at logic ‘0’ through R_{PD}. Note that the definition of EOP format is optimized towards repeater mode operation to provide timing support when an eUSB2 LS/FS EOP is converted to a USB2.0 EOP. An example eUSB2 EOP to USB2.0 EOP conversion in repeater mode is shown in Figure 3-5 and Figure 3-6.

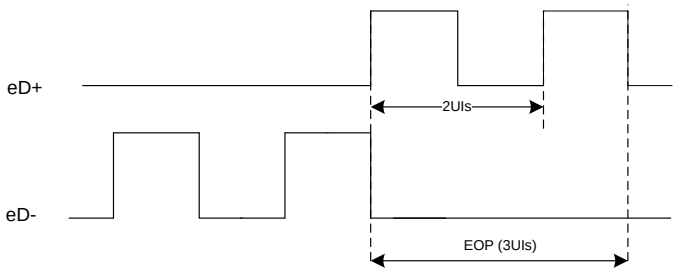


Figure 3-4: FS EOP Pattern from eDSPr/eUSPr

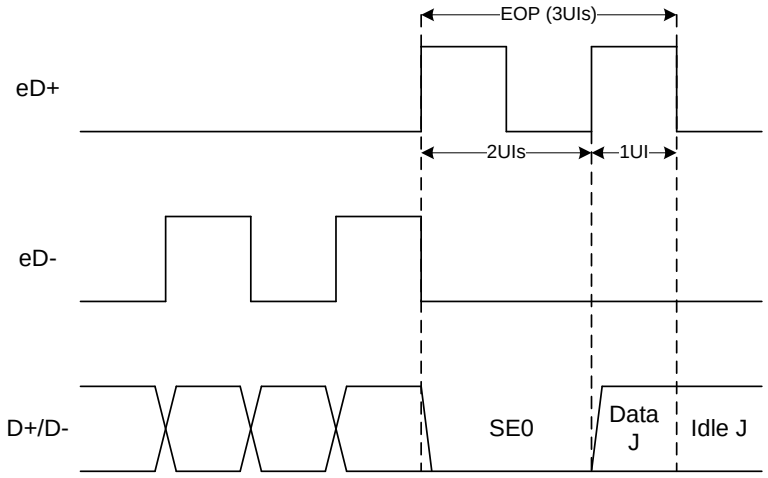
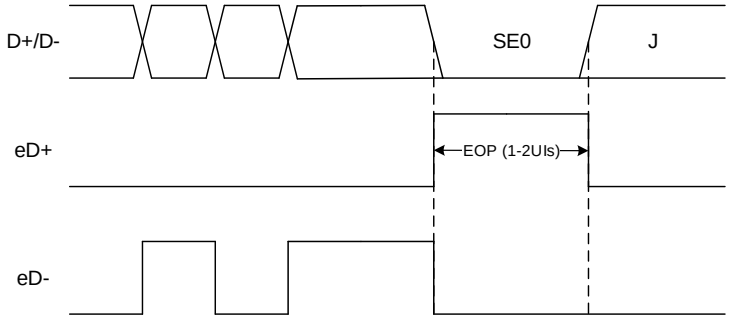
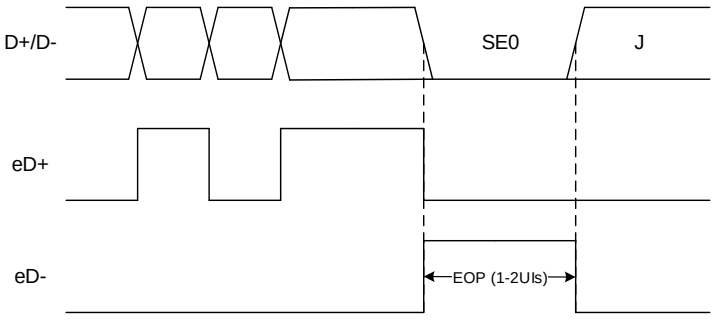


Figure 3-5: Example of eUSB2 EOP to USB2.0 EOP Conversion

- A FS EOP transmitted by eUSPh at host repeater to eDSPr, or eDSPp from peripheral repeater to eUSPr, is based on received EOP at D+/D-, which may be between 1 to 2 UIs of logic ‘1’ at eD+, and logic ‘0’ at eD-. This is shown in Figure 3-6. Similarly, a LS EOP may be between 1 and 2 UIs of logic ‘1’ at eD-, and logic ‘0’ at eD+. An eDSPr or eUSPr port shall declare the reception of a FS/LS EOP within 3 UIs upon detecting the start of the EOP.



(a). FS EOP



(b). LS EOP

Figure 3-6: FS/LS USB2 EOP to eUSB2 EOP Conversion

3.3.2 Low-speed Keep Alive

Low-speed keep alive is a specific case where LS EOP is transmitted by eDSPn or eDSPr to prevent a peripheral device from entering suspend. The low-speed keep alive signaling is the same as LS EOP.

3.3.3 Glitch Filtering in FS/LS Repeater Mode

Glitch filtering refers to preserving the USB packet integrity in FS/LS operation. It applies only to repeater mode. A FS/LS receiver at UDSP/UUSP may observe momentary SE0s or SE1s between every K-J or J-K transition within a received USB packet. This is primarily due the un-wanted asymmetry artifact introduced by the channel skew and transceiver non-ideality. Shown in Figure 3-7 is an illustration of the glitches that may be observed at eD+ as well as the wider logic '0' width on eD- which are associated with data crossover transition at D+/D-. Additionally, Figure 3-7 also illustrates the potential overlap or skew on eD+/eD- which produces an SE1 or SE0 respectively during EOP. Also, during the EOP window the eDSPr and eUSPr may observe glitches on eD- (FS) or eD+ (LS) and shall ignore these toggling.

- eUSPh/eDSPp shall adhere to USB2.0 Table 7-11 Hub/Repeater Electrical Characteristic in repeating D+/D- to eD+/eD-.
- eDSPr/eUSPr shall perform the glitch filtering as per USB 2.0 specification on eD+ (FS), or eD- (LS).

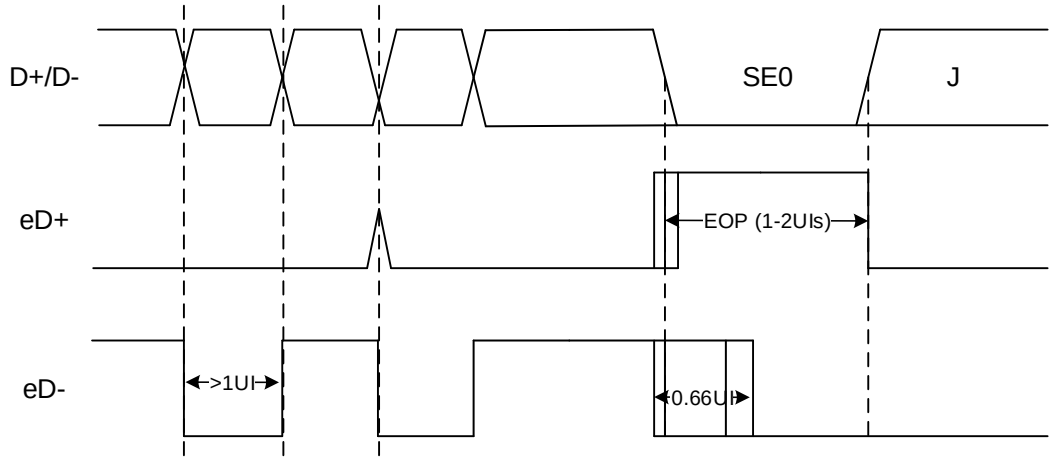


Figure 3-7: Transition glitches and asymmetry observed at eD- during FS operation

3.3.4 USB2.0 Bus Reset and End of Reset

eUSB2 signaling for USB2.0 Bus Reset is different between native mode and repeater mode, and they are described in the following sections.

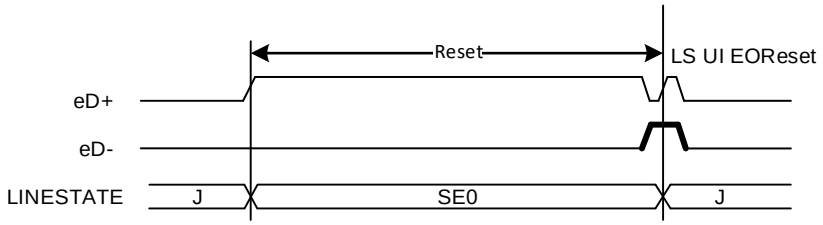
3.3.4.1 FS/LS Reset

The Reset signaling between the native mode and repeater mode operation are different.

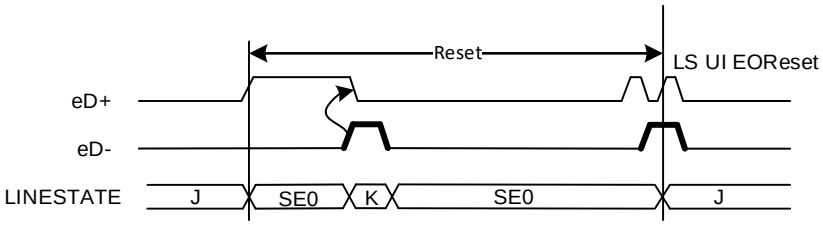
3.3.4.1.1 Native Mode

In native FS/LS mode, [USB 2.0] Bus Reset shall be transmitted by eDSPn to eUSPn based on linestate mapping as defined in

- Table 3-1.
- If it's in FS operation, eDSPn shall transmit Reset by driving logic '1' on eD+ and eUSPn shall map this as bus reset SE0 on its UTMI+ interface to its device controller.
- If it's in LS operation, eDSPn shall transmit Reset by driving logic '1' on eD- and eUSPn shall map this as bus reset SE0 on its UTMI+ interface to its device controller.
- If it's in FS operation, eDSPn shall stop driving logic '1' on eD+, and drive a logic '0', then a logic '1' (LS UI duration) on eD+ indicating end of Reset. Note that FS EOReset is defined with LS UI duration to allow repeater (consistent in Native mode) to use a lower clock frequency to detect end of reset.
- If it's in LS operation, eDSPn shall stop driving logic '1' on eD-, and drive a logic '0', then a logic '1' (LS UI duration) on eD- indicating end of Reset.
- eUSPn shall respond with a digital ping upon detecting the first falling edge of EOP and complete transmitting the digital ping on the second falling edge of EOP at the end of Reset to eDSPn. Refer to Section 4.2.3.2.1 for detail timing.
- A unique scenario may exist where a device chirp is observed from eUSPn, but the host does not return with host K-J chirp. In this case, the link will be settled in to FS with eDSPn transmitting FS EOReset.
- Refer to Figure 3-8 for FS Reset signaling.



(a) FS Reset



(b) FS Reset with HS device chirp

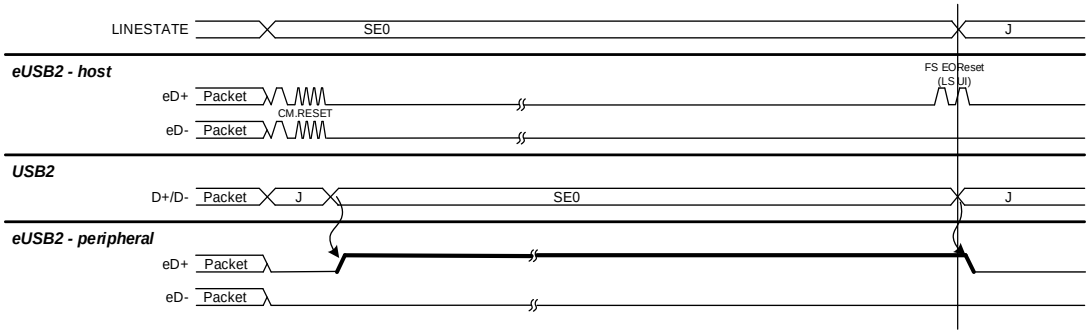
Figure 3-8: FS Reset in native mode

3.3.4.1.2 Repeater Mode

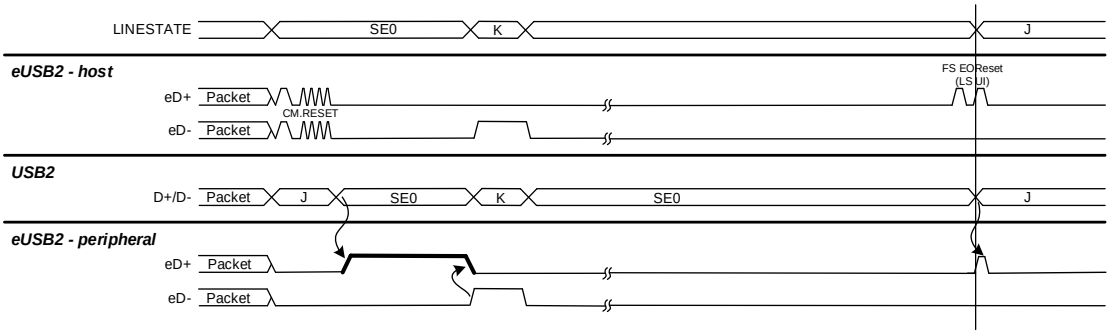
- In repeater FS/LS mode, a CM.Reset shall be transmitted by the eDSPr to the eUSPh.
- The host repeater shall initiate USB2.0 bus reset on D+/D- upon detecting CM.Reset.

In Peripheral repeater mode, [USB 2.0] Bus Reset is based on linestate mapping of SE0 at D+/D- as defined in

- Table 3-1.
- The eDSPp shall transmit a logic ‘1’ on eD+ or eD- (FS or LS mapping), to its eUSPr.
- A FS eUSB2 End of Reset (EOReset), transmitted by eDSPr, shall be 3 UIs (LS UI duration) with the first UI of logic ‘1’, followed by the second UI of logic ‘0’, and a third UI of logic ‘1’ at eD+, while eD- is maintained at logic ‘0’ through R_{PD}. Note that FS EOReset is defined with LS UI duration to allow repeater to use a lower clock frequency to detect end of reset. Similarly, a LS EOReset shall be 3 UIs (LS UI duration) with the first UI of logic ‘1’, followed by a second UI of logic ‘0’, and the third UI of logic ‘1’ at eD-, while eD+ is maintained at logic ‘0’ through R_{PD}. This is similar to data EOP described in Section 3.3.1.
- A FS and LS eUSB2 End of Reset (EOReset), transmitted by eDSPp shall be a return to SE0 from a logic ‘1’ at eD+ or eD- respectively. A unique scenario may exist where a device chirp is observed from eUSPr, but the host does not return with host K-J chirp. In this case, the link will be settled in to FS with eDSPp indicating EOReset with T_{STROBE}.
- Refer to Figure 3-9: for FS Reset signaling.



(a) FS Reset



(b) FS Reset with HS device chirp

Figure 3-9: FS Reset in repeater mode

3.3.4.2 HS Reset

The Reset signaling between the native mode and repeater mode operation are different.

3.3.4.2.1 Native Mode

- In an established HS mode, [USB 2.0] Bus Reset shall begin with eDSPn transmitting a SE1 for $T_{CM\_SE1\_8X}$ and continuously follow by a logic '1' on eD+. Note: USB2.0 Bus Reset from HS Lx shall follow FS/LS mode signaling.
- eUSPn shall map (maintain SE0 HS idle) this signaling to SE0 on its UTMI+ interface to the device controller.
- eUSPn shall transmit device chirp K as directed by its controller.
- eDSPn shall drop eD+ upon detecting a device chirp K from eUSPn.
- Upon the completion of device chirp K from eUSPn, eDSPn shall transmit host chirp K-J as directed by its host controller.
- Note: As opposed to repeater mode, eUSPn shall not transmit a Device Termination enabled to eDSPn when its controller enters HS operation.
- eDSPn shall end reset of a T_{STROBE}.
- Refer to Figure 3-10 for HS Reset signaling.

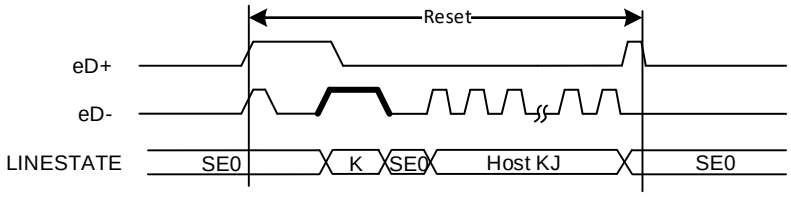


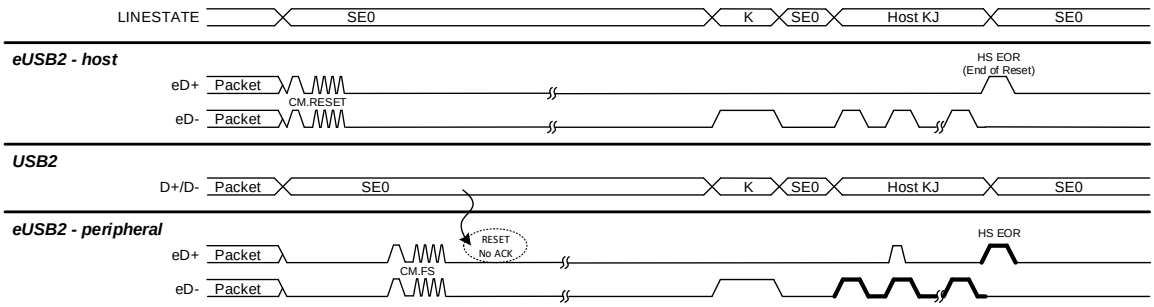
Figure 3-10: HS Reset in native mode

3.3.4.2.2 Repeater Mode

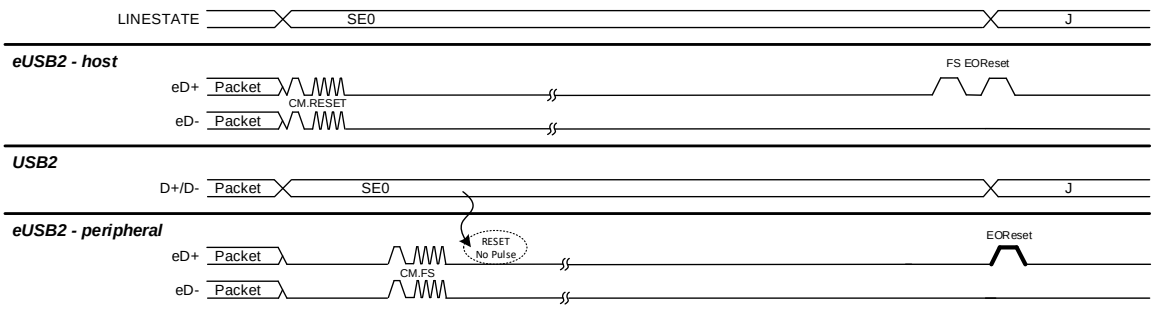
- In repeater HS mode, a CM.Reset shall be transmitted by the eDSPr to the eUSPh.
- The host repeater shall initiate USB2.0 bus reset on D+/D- upon detecting CM.Reset.

In Peripheral repeater mode, [USB 2.0] Bus Reset is based on HS link transitioning to FS with CM.FS. Note that linestate mapping of D+/D- to eD+/eD- as defined in

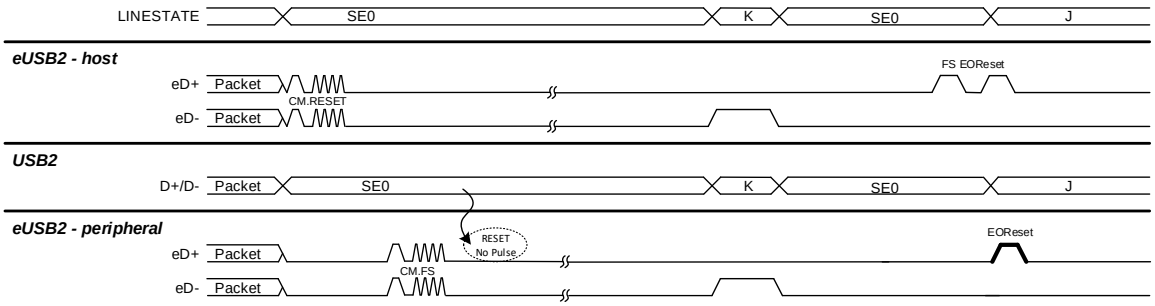
- Table 3-1 is not applicable during HS link bus reset.
- The Peripheral repeater shall declare USB2.0 Bus Reset upon detecting SE0 at D+/D- as defined in USB2.0.
- The eDSPp shall keep the eUSB lines in idle with R_{PD} upon declaring USB2.0 Bus Reset.
- The eDSPr, eUSPh, eDSPp, and eUSPr shall perform host/device chirp like HS native mode.
- A HS eUSB2 End of Reset (EOReset), transmitted by eDSPr and eDSPp, shall be T_{STROBE} of logic '1' at eD+.
- A couple of unique scenarios may exist where 1) a previously established HS link is downgraded to FS upon bus reset (Figure 3-11(b)) and 2) a device chirp is observed from eUSPr, but the host does not return with host K-J chirp (Figure 3-11(c)). In these cases, the link will be settled in to FS with eDSPp indicating EOReset with T_{STROBE}. Further note that in the scenario where an established HS link is downgraded to FS as shown in Figure 3-11(b), the peripheral repeater shall adhere to $T_{PR\_HS\_RESET\_TO\_FS}$ in recognizing USB2.0 bus reset as compared to Lx entry.
- Refer to Figure 3-11 for HS Reset signaling.



(a) HS Reset



(b) HS Reset to FS link



(c) HS Reset to FS link with device chirp

Figure 3-11: HS Reset in repeater mode

3.3.5 **Resume**

Resume in LS/FS and HS operations are both based on single-ended signaling.

3.3.5.1 FS/LS Resume

The Resume signaling between the native mode and repeater mode operation are different.

3.3.5.1.1 Native Mode

- In native mode, eDSPn shall adhere to the following rules to perform the Resume operation. Figure 3-12 shows the FS Resume signaling.
  - If it's in FS operation, it shall start Resume by driving Data K on eD- and conclude Resume with a FS EOResume on eD+ as shown in Figure 3-12. Note that a FS EOResume is the same as a LS EOP but with opposite polarity. Refer to Section 4.3.4 for details.
  - If it's in LS operation, it shall start Resume by driving Data K on eD+ and conclude Resume with a LS EOResume on eD-. Note that a LS EOResume is the same as a LS EOP. Refer to Section 4.3.4 for details.
- eUSPn shall adhere to the following rules to perform Digital Ping at the end of Resume.
  - In both FS and LS operation, it shall start transmitting the digital ping upon detecting the first falling edge of EOP and complete transmitting the digital ping on the second falling edge of EOP. Refer to Section 4.2.3.2.1 for detail timing.

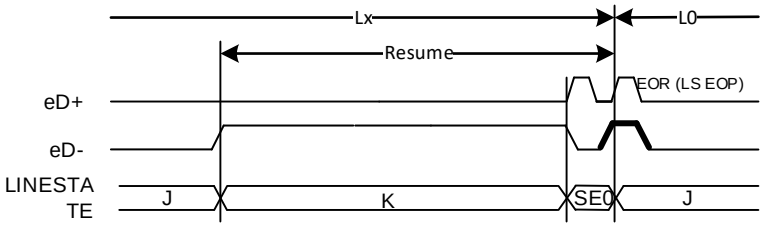


Figure 3-12: FS Resume in native mode

3.3.5.1.2 Repeater Mode

- If it's in FS host repeater mode, eDSPr/eUSPh shall adhere to the following rules to perform the Resume operation. Refer to Figure 3-13 for details of Resume.
  - eDSPr shall start Resume with SOResume followed immediately with Resume K. It shall conclude Resume with a FS EOResume. Note that SOResume is defined as SE1 for $T_{DR\_SE1\_L1/L2}$ duration, and FS EOResume is the same signaling as a LS EOP on eD+. Refer to Section 5.3.5.2 for details.
  - eUSPh, upon detecting SOResume, it shall start driving Resume K at D+/D- and conclude Resume if a FS EOResume is detected.

- If it's in LS host repeater mode, eDSPr/eUSPh shall adhere to the following rules to perform the Resume operation.
    - eDSPr shall start Resume with SOResume followed immediately with Resume K. It shall conclude Resume with a LS EOResume. Note that SOResume is defined as SE1 for $T_{DR\_SE1\_L1/L2}$ duration, and LS EOResume is the same as a LS EOP. Refer to Section 5.3.5.2 for details.
    - eUSPh, upon detecting SOResume, it shall start driving Resume K at D+/D- and conclude Resume if a LS EOResume is detected.
- If it's in FS Peripheral repeater mode, eDSPp/eUSPr shall adhere to the following rules to perform the Resume operation. Refer to Figure 3-13 for details of Resume.

eDSPp shall map Resume K at D+/D- to Resume K at eD+/eD-, as defined in

    - Table 3-1. It shall conclude Resume with a FS EOResume matching the SE0 timing at D+/D-.
    - eUSPr shall update Linestate upon detecting Resume K at eD+/eD-, it shall conclude Resume upon detecting FS EOResume.
    - Refer to Section 5.4.5.2 for details.
- If it's in LS Peripheral repeater mode, eDSPp/eUSPr shall adhere to the following rules to perform the Resume operation. Refer to Figure 3-13 for details of Resume.

eDSPp shall map Resume K at D+/D- to Resume K at eD+/eD-, as defined in

- Table 3-1. It shall conclude Resume with a LS EOResume matching the SE0 timing at D+/D-.
- eUSPr shall update Linestate upon detecting Resume K at eD+/eD-, it shall conclude Resume upon detecting LS EOResume.

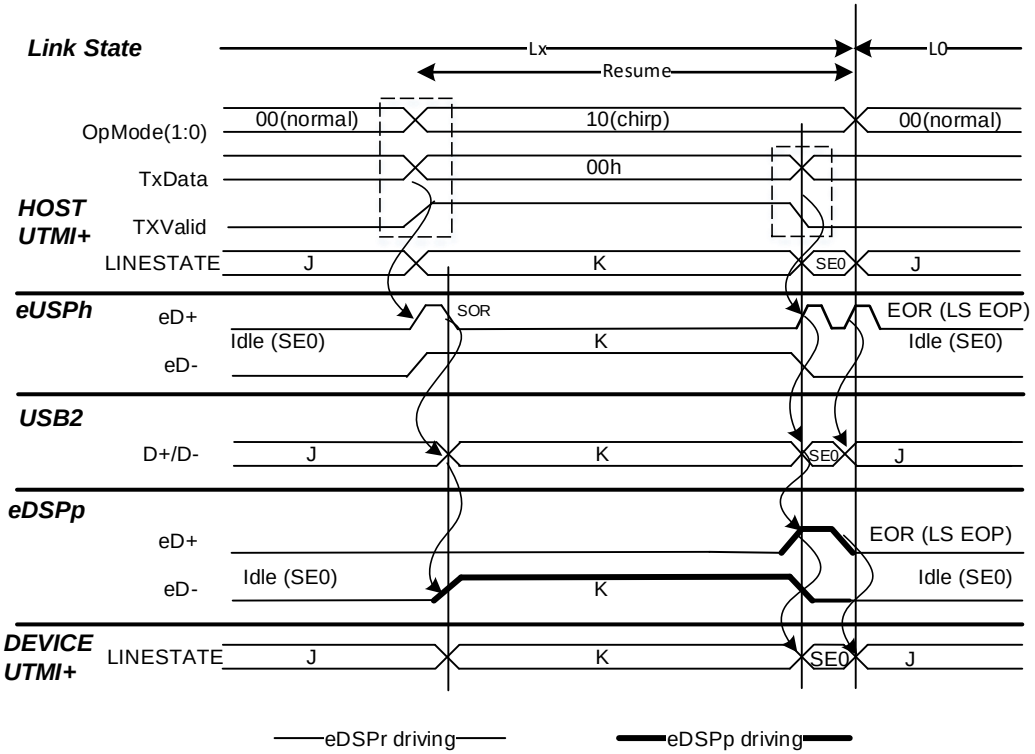


Figure 3-13: FS Resume in repeater mode operation

3.3.5.2 HS Resume

3.3.5.2.1 Native Mode

HS Resume follow the same rule of FS Resume, except EOResume.
Shown in Figure 3-14 is the native mode Resume sequence. Compare with FS EOResume, a HS EOResume is used instead and is defined as T_{STROBE}.

- eDSPn/eUSPn shall use FS LineState mapping during Resume, and switch to HS LineState mapping upon entry to L0.
- eDSPn/eUSPn shall enable its HS transceiver upon entry to L0.

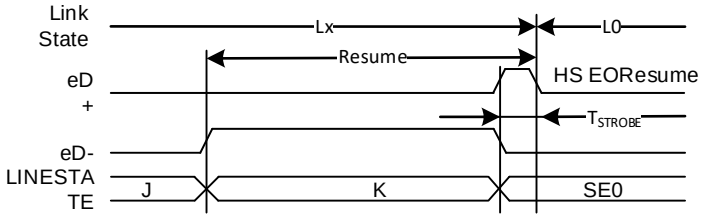


Figure 3-14: HS Resume in native mode

3.3.5.2.2 Repeater Mode

Shown in Figure 3-15 is the repeater mode Resume sequence.

- Upon transmitting or detecting SOResume, eDSPr/eUSPh shall use FS LineState mapping to start Resume, and switch to HS LineState mapping upon entry to L0.
- Upon detecting Resume at D+/D-, eDSPp shall drive Resume K to eUSPr, and conclude Resume with HS EOResume of T_{STROBE}.
- Upon detecting Resume K, eUSPr shall proceed to exit from Lx. It shall conclude Resume and transition to L0 upon the end of HS EOResume.

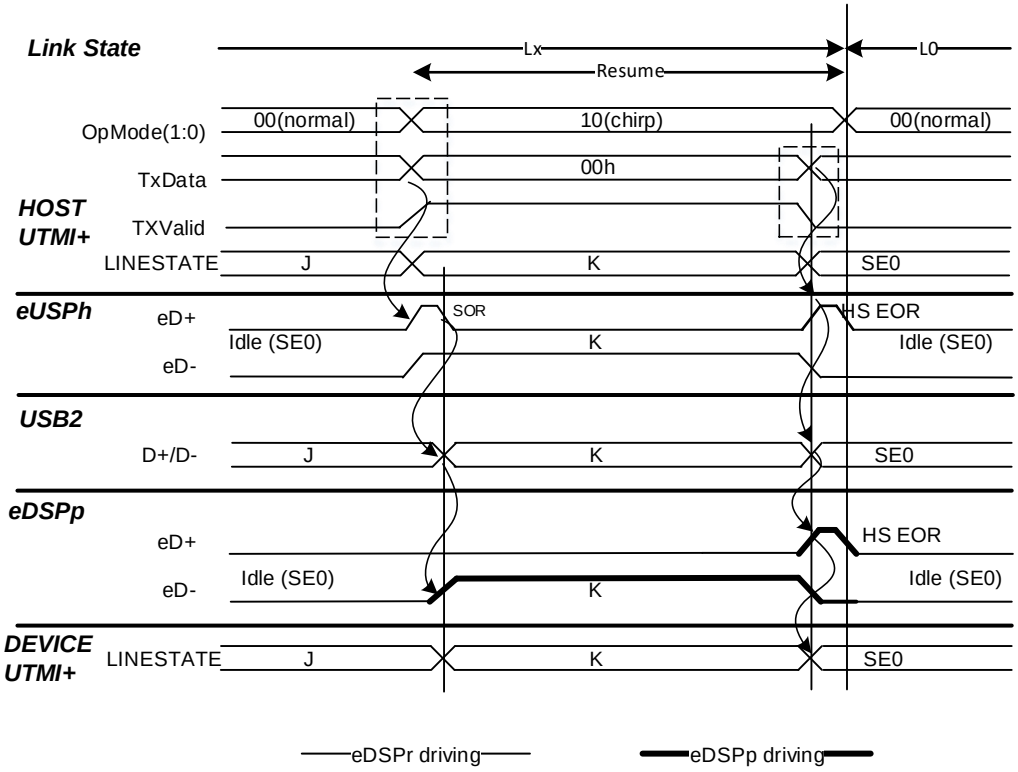


Figure 3-15: HS Resume in Repeater mode

3.3.6 **Remote Wake**

The Remote Wake signaling between the native mode and repeater mode operation are also different.

3.3.6.1 FS/LS Remote Wake

3.3.6.1.1 Native mode

- If it's in FS operation, eUSPn/eDSPn shall adhere to the following rules to perform the Remote Wake operation.
    - eUSPn shall start Remote Wake by driving FS Data K and conclude Remote Wake by disabling its SE Tx at eD-. Note that under normal operation, eDSPn has already started Resume by driving Resume K on eD-. Disabling SE Tx by eUSPn, instead of driving logic '0' to conclude Remote Wake ensures the continuation of Resume K. Note also that if an error case occurs that eDSPn does not resume, eUSPn will continue to observe Data K until residue charge on eD- is dissipated. This is shown in Figure 3-17. This behavior should be like existing USB2.0 if wake didn't follow with a resume.
    - eDSPn, upon detecting Remote Wake, shall update LineState, and start to drive Resume K when directed. It shall conclude Resume with LS EOP with the opposite polarity. Shown in Figure 3-16 is the FS Remote Wake.

- If it's in LS operation, eUSPn/eDSPn shall adhere to the following rules to perform the Remote Wake operation.
    - eUSPn shall start Remote Wake by driving LS Data K and conclude Remote Wake by disabling its SE Tx at eD+.
    - eDSPn, upon detecting Remote Wake, shall update LineState, and start to drive Resume K when directed. It shall conclude Resume with LS EOP.

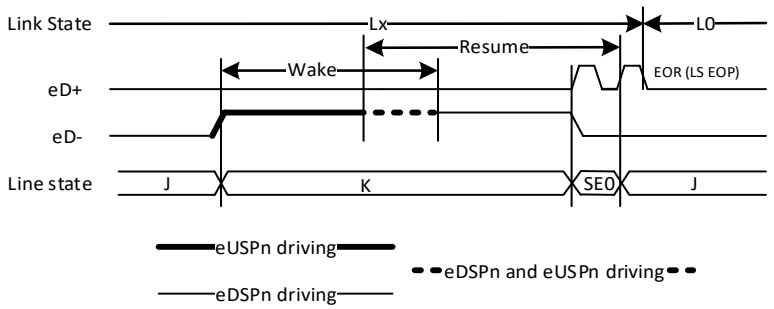


Figure 3-16: FS Remote Wake in native mode (normal)

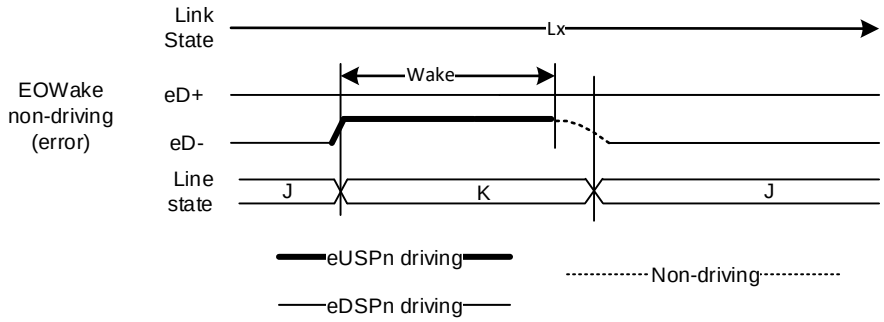


Figure 3-17: FS Remote Wake in native mode (host not responding)

3.3.6.1.2 Repeater Mode

- If it's in FS peripheral repeater mode, eUSPr/eDSPp shall adhere to the following rules to perform the Remote Wake operation. Refer to Figure 3-18 for details of Remote Wake.
    - eUSPr shall start Remote Wake with SOWake followed continuously with Remote Wake K. it shall conclude Remote Wake with a FS EOWake. Note that SOWake is defined an SE1 for $T_{DR\_K\_SE1\_1X/8X}$ duration. A FS EOWake is defined as a strobe of duration T_{STROBE} at eD+ with SE Tx at eD- disabled. During the EOWake period, it shall continue the line state mapping from eD+/eD-. Refer to Section 5.5.12 for details.
    - eDSPp, upon declaring SOWake (Refer to Table 7-16 for SOWake receive timing), shall start driving Remote Wake K at D+/D- and eD+/eD-. It shall conclude Remote Wake upon detecting the start of EOW by stop driving K at D+/D- and reflecting the line state at D+/D- to eD+/eD-. If Resume K is still observed, it shall continue to drive Resume K at eD+/eD-.
- If it's in FS host repeater mode, eDSPr/eUSPh shall adhere to the following rules to perform the Remote Wake operation. Refer to Figure 3-18 for details of Remote Wake.

eUSPh shall reflect Remote Wake K at D+/D- to Remote Wake K at eD+/eD-, as defined in

    - Table 3-1. It shall conclude Remote Wake in either one of the following conditions.
        - If SOResume (SE1 on eD+/eD-) from eDSPr is detected and the linestate at D+/D- is still maintained, it shall conclude remote wake by disabling its SE Tx, not drive logic '0' for $T_{SE0\_DR\_LSFS}$ at eD-. It shall drive Resume K at D+/D- until a FS EOResume is detected.
        - If Remote Wake K at D+/D- is concluded and no SOResume (absent of SE1 on eD+/eD-) from eDSPr (Note: This is an error case) is detected, it shall drive $T_{SE0\_DR\_LSFS}$ to allow immediate logic '1' to logic '0' transition before disabling its SE Tx at eD- and stop driving Resume K at D+/D-. Note that in this scenario, the repeater implementation will require to differentiate a remote wake K to a SYNC K (in the case where the repeater is performing a remote wake in L0) by the duration of K to drive logic '0' on eD- for $T_{SE0\_DR\_LSFS}$ (Repeater may drive logic '0' for the full J duration if it is a data J). A different implementation may have the repeater start and continue driving logic '0' on eD- upon detecting the end of remote K (K to J transition) and stops based on some non-activity timers. Refer to Section 5.5.16 and 5.5.19 for timing diagram.
    - eDSPr shall update the line state upon detecting Remote Wake. It shall start SOResume followed immediately with Resume K upon direction. It shall conclude Resume with a FS EOResume.
- If it's in LS peripheral repeater mode, eUSPr/eDSPp shall adhere to the following rules to perform the Remote Wake operation.
    - eUSPr shall start Remote Wake with SOWake followed continuously with Remote Wake K. it shall conclude Remote Wake with a LS EOWake. Note that a LS EOWake is defined as a strobe of duration T_{STROBE} at eD- with SE Tx at eD+ disabled. During the EOWake period, it shall continue the line state mapping from eD+/eD-. Refer to Section 5.5.12
    - eDSPp, upon detecting SOWake, shall start driving Remote Wake K at D+/D- and eD+/eD-. It shall conclude Remote Wake upon detecting the start of EOWake by stop driving K at D+/D- and reflecting the linestate at D+/D- to eD+/eD-. If Resume K is still observed, it shall continue to drive Resume K at eD+/eD-.
- If it's in LS host repeater mode, eDSPr/eUSPh shall adhere to the following rules to perform the Remote Wake operation.

eUSPh shall reflect Remote Wake K at D+/D- to Remote Wake K at eD+/eD-, as defined in

- Table 3-1. It shall conclude Remote Wake in either one of the following conditions.
  - If SOResume (SE1 on eD+/eD-) from eDSPr is detected and the linestate at D+/D- is still maintained, it shall conclude remote wake by disabling its SE Tx, not drive logic '0' for $T_{SE0\_DR\_LSFS}$ at eD+. It shall drive Resume K at D+/D- until a LS EOResume is detected.
  - If Remote Wake K at D+/D- is concluded and no SOResume (absent of SE1 on eD+/eD-) from eDSPr is detected, it shall drive logic '0' for $T_{SE0\_DR\_LSFS}$ to allow immediate logic '1' to logic '0' transition before disabling its SE Tx at eD+ and stop driving Resume K at D+/D-. Note that this is an error case.
- eDSPr shall update the line state upon detecting Remote Wake. It shall start SOResume followed immediately with Resume K upon direction. It shall conclude Resume with a LS EOResume.

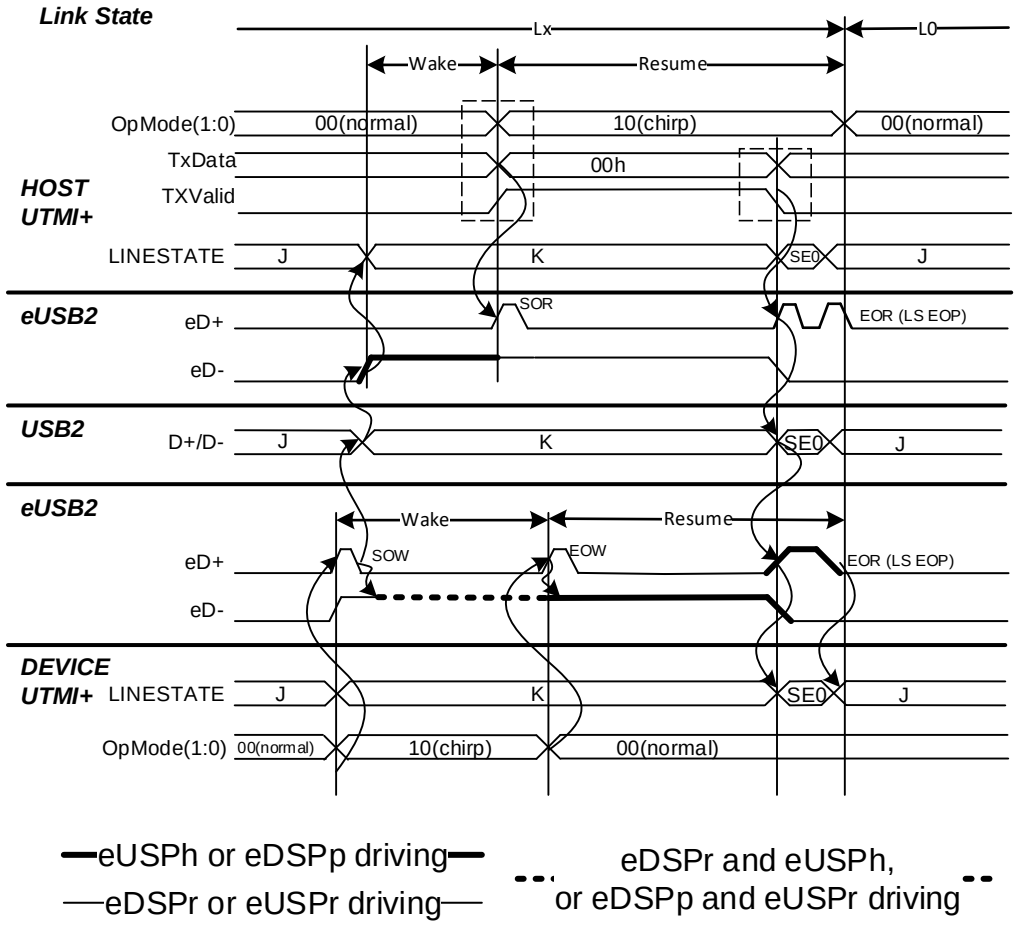


Figure 3-18: FS Remote Wake in repeater mode

3.3.6.2 HS Remote Wake

The Remote Wake signaling at HS is the same as FS. Shown in Figure 3-19 and Figure 3-20 are a timing diagrams of Remote Wake and Resume in native mode and repeater mode.

3.3.6.2.1 Native mode

As shown in Figure 3-19, a logic '1' is presented on eD- as a wake, follow by a resume and EOResume of T_{STROBE}.

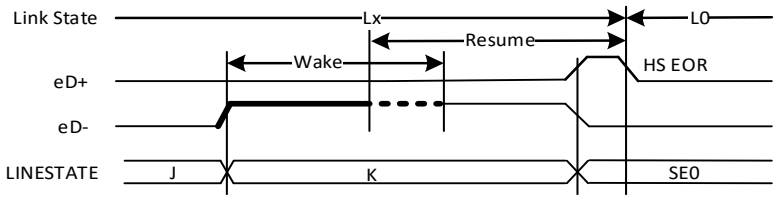


Figure 3-19: HS Remote Wake in native mode

3.3.6.2.2 Repeater mode

As shown in Figure 3-20, a wake to HS is like a FS/LS remote wake except for EOResume of T_{STROBE}.

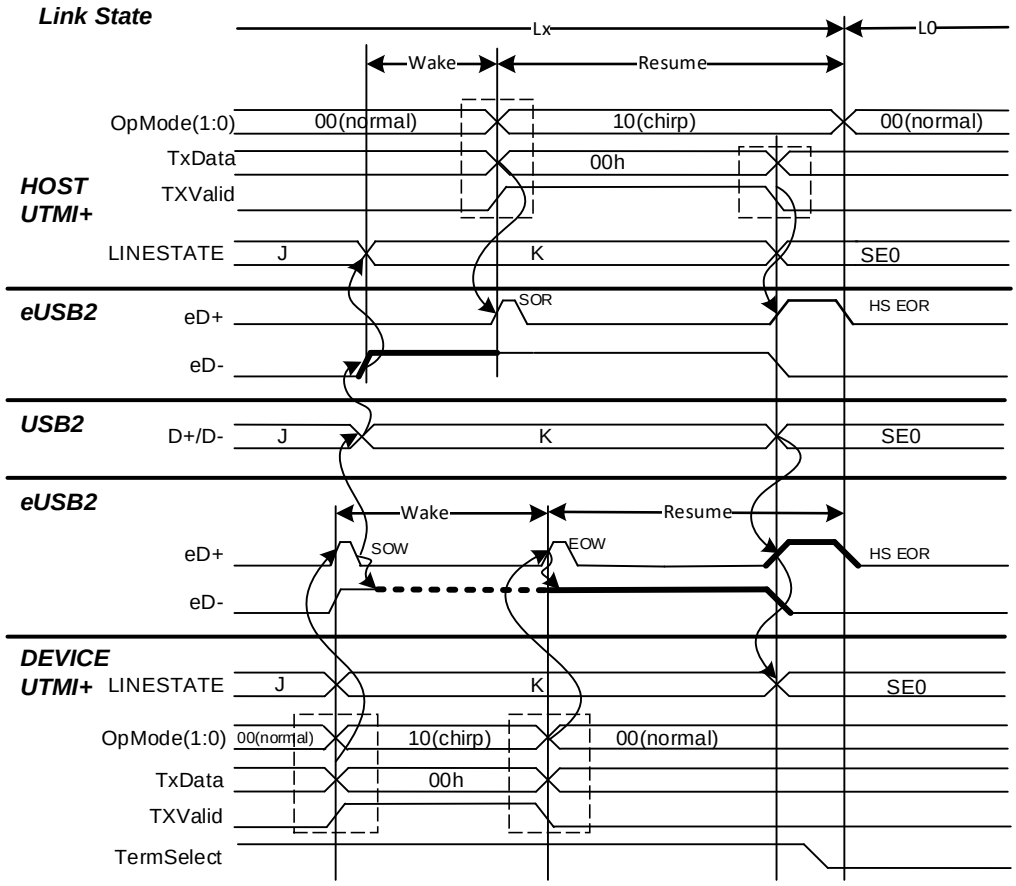


Figure 3-20: HS Remote Wake in repeater mode

3.3.7 Control Message Signaling

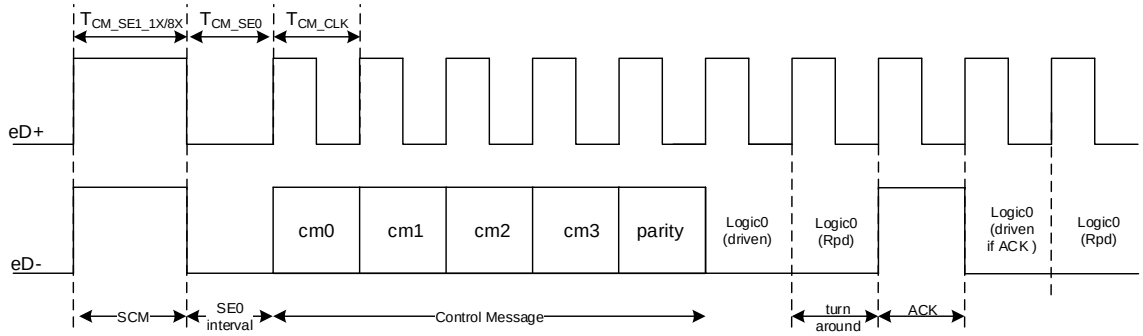
Control messages (CMs) in eUSB2 are defined for various USB2.0 and non-USB2.0 usages in native mode and repeater mode. A CM may be issued by eDSPn, eDSPr or eUSPr. It either indicates reset, entry to L1/L2, or start of register access. Note that in native mode, only CM.RAP is used by eDSPn.

The structure of the CM is shown in Figure 3-21. It contains a 4-bit control message (CM), followed by an odd parity bit. A port transmitting a CM shall adhere to the following rules:

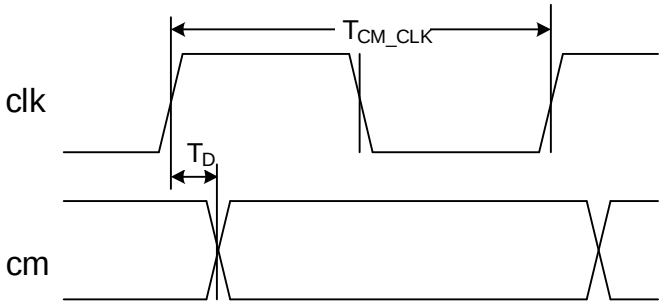
- It shall wait until the eUSB2 bus state is non-SE1 before initiating the CM.

- It shall begin CM transmission with SE1 as Start of Control Message (SCM).
- In the event of transmitting back-to-back CMs, the port shall allow an idle time T_{CMB2B} (end to start) between the CMs.
- The order of the control message is little endian.
- After transmitting the parity bit, it shall transmit five additional clock cycles at eD+, with each progressive clock cycle performing the following actions at eD- by the CM transmitter or the receiver.
    - CM transmitter drive logic ‘0’.
    - CM transmitter maintain logic ‘0’ and enable SE Rx.
    - CM transmitter check if an ACK is received. Note: The receiver to the CM message shall perform a parity check and transmit an ACK if the correct parity is detected. Note that exception apply to peripheral repeater, eDSPp in receiving CM where it shall always ACK.
    - CM receiver drive logic ‘0’ following the ACK.
    - CM transmitter and receiver maintain logic ‘0’ with R_{PD}.
- SCM of CM is defined as $T_{CM\_SE1\_1X}$ or $T_{CM\_SE1\_8X}$; SE0 of CM is defined as T_{CM_SE0}; Clock pulses of CM message is defined as T_{CM_CLK}; CM clk to data delay is defined as $T_{D.}$
- In the event of NO ACK, both TX and RX shall wait for the end of CM (not after without detecting ACK) before moving to the next operation.

Refer to Table 7-16 for the timing specification.



(a) eUSB2 Control Message Encoding



(b) eUSB2 Control Message Timing

Figure 3-21: eUSB2 Control Message

Table 3-3: Encoding of eUSB2 Control Message

CM[3:0]	Parity	Description	Control Message Name	Usage Cases
0	1	HS Host: Enter FS terminations and enter L1 power state[1]	CM.FS	Repeater mode only
		HS Peripheral: Enter FS terminations[1]		
		FS/LS: Enter L1 power state[1]	CM.L1	
1	0	Enter lowest physical power state	CM.L2	Repeater mode only
2	0	USB2.0 Bus Reset[2]	CM.Reset	Repeater mode only Note: SCM for CM.Reset is 8X longer than other CMs. Implementation may use this to distinguish CM.Reset to others.
3-6	X	Reserved	Reserved	Reserved
7	0	Enable HS terminations without enumeration (Test Mode)[4]	CM.Test	Repeater mode only For compliance use
8-14	X	Reserved	Reserved	Reserved
15	1	Start of register access[3]	CM.RAP	Native mode: For eDSPn to access the register space in eUSPn. Repeater mode: For eUSPr or eDSPr to access the register space in its associated repeater.

Note 1. Entry to L1 for native mode is based on a LPM extended transaction. Use of a control messages to indicate entry to L1 is primarily used for eUSB2 repeaters. Refer to Section 5.3.5 and 5.4.5 for details.

Note 2. Transmitted with L1/L2 timing parameters when the link is in L1/L2 (i.e. CM.L1/L2 has been transmitted)

Note 3. Indication of the start of register access protocol. Refer to Chapter 6 for details.

Note 4. Host Mode HS Compliance Test mode entry. Refer to Section 5.3.1.1 for details.

3.3.7.1 CM Retry and Recovery Rules

A port shall adhere to the following rules to retry CM if ACK is not detected.

- After transmitting, an eDSPr shall retry only once and eUSPr shall never need to retry.
- An eDSPr may retry a CM only once and then shall reset with a Port Reset as described in Section 3.3.8 if the CM is not ACKed either time.
  - While transmitting a Port Reset, the eDSPr shall signal disconnect on UTMI+.
  - When the Port Reset is received, an eUSPh will enter Default.
- An eDSPp shall always ACK a CM
  - If in L0 for all speed, regardless of parity error or undefined CM encoding detected, eDSPp shall respond with ACK.
  - If HS L0, the first CM an eDSPp receive is always CM.FS.

- If FS/LS L0, the CM an eDSPp receive is either CM.L1 or CM.L2. In the case of parity error, CM shall be treated as CM.L1 by the peripheral repeater.
- In L1 for FS/LS, if a CM is detected, an eDSPp shall treated it as CM.L1. Note that this is to allow the repeater to remain in the shallower power state.
- In unconnected (pullup has not been enabled), eDSPp shall ACK and ignore the CM. Note that the possible CM in this state is CM.L2, which the peripheral repeater should already be in this state.

3.3.8 **Extended SE1 (Port Reset)**

Extended SE1 (ESE1), shown in Figure 3-22, is defined and used under various circumstances for an eUSB2 port to announce an event of device disconnect or port reset (Note that is the not equivalent to USB2.0 bus reset). The timing of ESE1 is specified such that it shall survive any bus contention without corruption.

- An ESE1 is defined with SE1 duration of T_{EXTSE1}.
- When directed, a port shall transmit ESE1 if a non SE1 line state is observed at eD+/eD-. Note that ESE1 is defined to survive contention with any other signaling on eUSB2.
- When directed, a port may also transmit ESE1 to recover from an unrecognizable eUSB2 bus event. Note that circumstances exist where an unexpected condition is detected that may result in undefined port behavior. Under this condition, a port may transmit ESE1 to restart a new USB session. Note that this is implementation specific between controller and PHY or system level implementation to recover from this undefined port state.

ESE1 is defined to cover the following scenarios.

- As Port Reset in native mode,
  - For eDSPn to indicate power-on and ready for operation.
  - For eDSPn to terminate a USB2.0 session, or to recover an error event.
  - For eUSPn to inform eDSPn device (soft) disconnect when directed by its device controller.
  - For eUSPn to inform eDSPn to restart USB2.0 session as a mechanism for error recovery.
  - eUSPn shall not transmit ESE1 upon power-on to avoid potential EOS stress to eDSPn. Note: In the case that the device in native mode required powering off or silent disconnect once it is enabled (Port Configuration) by its associated eDSPn, system implementation shall ensure a sideband communication to inform eDSPn.
- Also as Port Reset in repeater mode,
  - For the eUSBr to indicate power-on and ready for operation to its associate repeater.
  - For eDSPr to reset the host repeater upon qualifying a logic ‘1’ on eD+ for disconnect (map to a disconnect SE0 condition on D+/D-) while operating in FS idle.
  - For eDSPr to reset the host repeater upon qualifying a logic ‘1’ on eD- for disconnect (map to a disconnect SE0 condition on D+/D-) while operating in LS idle.
  - For eDSPr or eUSPr to reset the host or peripheral repeater respectively upon directed (this is implementation specific between the controller and its physical layer).
  - For eUSPr to direct its peripheral repeater to perform device disconnect.
  - eUSPh and eDSPp shall not transmit ESE1 upon power-on. This imply that both the host and peripheral repeaters shall not power off once they have been enabled (Host/Peripheral enable) by its associated eDSPr or eUSPr. It is implementation specific to use sideband communication to inform eDSPr or eUSPr if powering down the repeater is required.

  - As Device Disconnect Announcement, for the host repeater to inform eDSPr a device disconnect event in HS L0. Refer to Section 5.3.4.3 and 5.5.7 for details. Note: A peripheral repeater shall never transmit ESE1.
- A port, upon detecting SE1 on the eUSB2 bus, shall declare the reception of ESE1 based on the T_{EXTSE1} receive timing (with exception of T_{HSDISC_SE1} for HS disconnect and T_{NATIVE_SE1}/T_{NATIVE_ESE1} in Native Mode) in Table 7-16. Note that concurrent ESE1 may exist when both link partners drive ESE1 at the same instance. Under this situation, the conclusion of ESE1 may likely be asynchronous. If the port concludes ESE1 earlier, it may drive SE0 before switching to pull-down. Contention may occur between SE0 and ESE1. It is recommended that a momentary SE1 discontinuity up to $T_{SE0\_DR\_HS}$ or $T_{SE0\_DR\_LSFS}$ be ignored.
- Upon completed transmitting Port Reset, a port shall ensure an idle time of T_{CONFIG_IDLE} before transmitting Port Configuration.
- Upon transmitting or receiving Port Reset or Device Disconnect Announcement, an eUSB2 port or repeater shall transition to Default.

Note that when Port Reset is transmitted by the eDSPn and eUSBr to the eUSPn and repeater respectively upon POR, the eUSPn and repeater may also be transitioning from POR as well. In this case, the full duration or T_{EXTSE1} receive timing of the Port Reset may not be completely detected or met by the eUSPn and repeater. As the eUSPn and repeater are in POR default state, the eUSPn and repeater may ignore or declare ESE1 (Note: The eUSPn and repeater is recommended to have a timer to distinguish between ESE1, CM.RAP and Port/Repeater Configuration) even with the potential shorter Port Reset duration. The eUSPn and repeater shall wait for Port/Repeater Configuration if the Port Reset is ignored. Also, if a controller reset or UTMI reset occur during Port Reset, the eDSPn and the eUSBr depending on implementation may choose to complete or terminate the Port Reset. If Port Reset is terminated, the eDSPn and the eUSBr shall retransmit Port Reset.

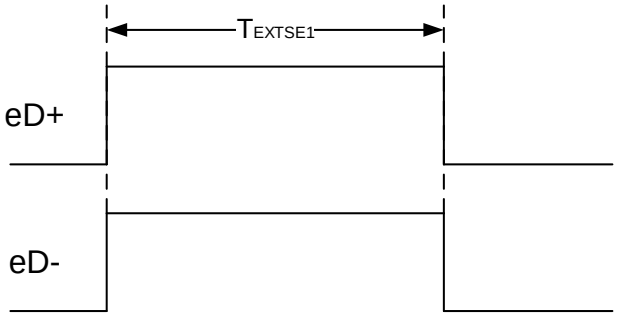


Figure 3-22: Extended SE1

3.3.9 **Port/Repeater Configuration**

Port/Repeater Configuration is a handshake defined to establish an initialization connection between link partners (eDSPn-eUSPn and eUSBr-repeater).

- Port/Repeater Configuration is issued by eDSPn/eDSPr/eUSPr and acknowledged by eUSPn/eUSPh/eDSPp respectively upon detecting the logic ‘1’ on eD+/eD-.

Port/Repeater Configuration is defined to cover the following scenarios

- To establish an initialization between eDSPn and eUSPn as well as to convey HS receiver termination setting to eUSPn.
  - A logic ‘1’ on eD+ from eDSPn to eUSPn to indicate to eUSPn to enable its HS receiver termination. And eUSPn shall acknowledge on eD-.
  - A logic ‘1’ on eD- from eDSPn to eUSPn to indicate to eUSPn to disable its HS receiver termination. And eUSPn shall acknowledge on eD+.

- To establish an initialization between eUSBr and its repeater as well as to configure its repeater for Host or Peripheral operation mode.
    - A logic ‘1’ on eD+ from eDSPr to its repeater to enable its repeater for Host operation mode. And repeater eUSPh shall acknowledge on eD-.
    - A logic ‘1’ on eD- from eUSPr to its repeater to enable its repeater for Peripheral operation mode. And repeater eDSPp shall acknowledge on eD+.
- An eDSPn/eDSPr/eUSPr shall complete Port/Repeater Configuration upon detecting an acknowledgment from the eUSPn/eUSPh/eDSPp respectively by T_{CONFIG_CMPL}.
- Refer to **Error! Reference source not found.** for signaling detail.

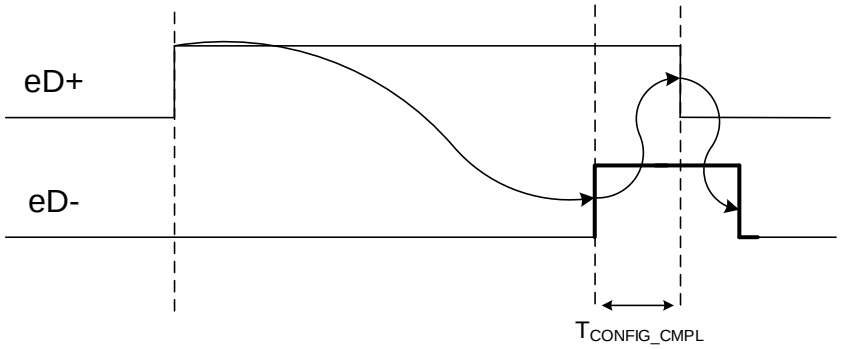


Figure 3-23: Port/Repeater Configuration

4 eUSB2 Native Mode Architecture and Operation

4.1 *eUSB2 Native Mode Configuration and Usage*

Native mode eUSB2 operation is defined to support in-box interconnect where the speed of the eUSB2 operation maybe preconfigured. This usage model may allow an opportunity for a downstream port to support only a single or selected speed configurations, and hence, implementation optimization may be possible based on port customization. However, it is a system's responsibility to be aware of a downstream port's capability and to ensure proper device configuration and interoperability.

- A customized downstream port supporting a single or selected data rates shall follow the eUSB2 specification as defined in Section 4.3 in terms of device connect, reset and speed detection. Note that a downstream port that supports high-speed only operation is still required to perform speed detection protocol, even it is known prior that a device attached is high-speed capable.

Examples of downstream port configurations include but are not limited to the following:

- LS, FS, HS
- LS, FS only
- FS, HS only
- FS only
- HS only

4.2 *eUSB2 Native Mode Protocol Signaling*

Below section describes protocol and signaling that is applicable to Native Mode only.

4.2.1 **Port Reset (ESE1)**

Port Reset (Note that is the not equivalent to USB2.0 bus reset), ESE1 signaling is defined to perform the following:

- An eUSPn shall initiate Port Reset when one of the following scenarios occur:
  - Port Reset is issued by an eUSPn when it is directed to terminate its current USB session in L0, L1 or L2 for all speed. This is also referred to as soft disconnect (only instance where Port Reset is transmitted from eUSPn).
  - eUSPn shall not initiate Port Reset upon Power-up reset. An eUSB2 port in Native mode shall be configured (UTMI+ interface) as single role (or device mode) to avoid the eventual device port (eUSPn) coming out of POR as host port (eDSPn) and transmit Port Reset.
  - In the event where an eUSPn may be disconnected without its associated eDSPn being aware or not being able to transmit Port Reset before disconnecting/powering off (especially in L1 or L2), it is implementation specific to use sideband communication to inform eDSPn. This is also referred to as silent disconnect
- An eDSPn shall initiate Port Reset under one of the following conditions:
  - Power-up reset.
  - Implementation specific HW reset on the phy or UTMI interface.

A declaration of Port Reset reception is defined below:

- An eUSPn upon POR detecting SE1 on the eUSB2 bus, shall declare the reception of ESE1 based on the T_{EXTSE1} receive timing. Note: As both eDSPn and eUSPn power up asynchronously, eUSPn may not observe enough duration of SE1 to declare Port Reset. eUSPn may ignore this and continue to wait for Port Configuration.
- If the eUSB2 port is not transmitting SE1, and upon detection of SE1 for T_{NATIVE_SE1}, the eUSB2 port shall stop and disable its current TX (if it is transmitting any data packet) to prevent contention to SE1 reception.

- The eDSPn/eUSPn port shall declare the reception of Port Reset/soft disconnect respectively upon detecting SE1 condition for T_{NATIVE_ESE1}. Note that this receive timing is shorter than repeater mode T_{EXTSE1} receive timing, to allow quicker Port Reset declaration with Native mode eUSB2 expected to have the necessary clock frequency to detect it.

4.2.2 Port Configuration

Port Configuration is a handshake defined to establish an initialization connection as well as conveying receiver termination scheme between the eDSPn and eUSPn. Port Configuration signaling is defined to perform the following:

- Port Configuration is issued by eDSPn and acknowledged by eUSPn upon detecting the logic '1' on eD+/eD-.
- Upon POR and after transmitting Port Reset, the eDSPn shall drive a logic '1' on eD+ as a Port Configuration to eUSPn. A logic '1' on eD+ Port Configuration is also an indication to eUSPn to enable its HS receiver termination. And eUSPn shall acknowledge on eD-.
- Upon POR and after transmitting Port Reset, the eDSPn shall drive a logic '1' on eD- as a Port Configuration to eUSPn. A logic '1' on eD- Port Configuration is also an indication to eUSPn to disable its HS receiver termination. And eUSPn shall acknowledge on eD+.
- An eDSPn shall complete Port Configuration upon detecting an acknowledgment from the eUSPn by T_{CONFIG_CMPL}.
- Refer to Figure 4-1 for signaling detail.

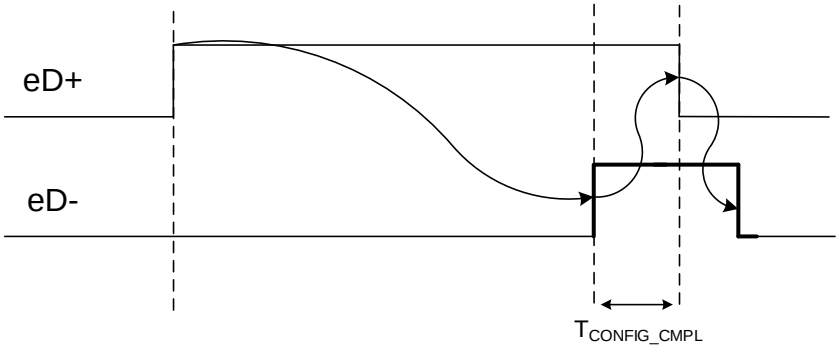


Figure 4-1: Port Configuration with HS Differential Receiver Termination Enable

4.2.3 Disconnect Detect

The mechanisms of eUSB2 disconnect detect at LS/FS and HS are different from USB2.0. Section below discussed the disconnect detection for various speeds as well as under different link state.

4.2.3.1 Low-speed/Full-speed Disconnect Detect during L0

The SE0 idle state of eUSB2 is maintained by both ports through their R_{PD} in FS/LS L0. This is different from idle state J defined in USB2.0 that allows for disconnect detect during idle state. A digital mechanism and Port Reset are defined for eUSB2 device disconnect detect during L0.

4.2.3.1.1 Digital Ping

An eUSPn in L0 periodically transmits a digital ping, as illustrates in Figure 4-2, to announce its presence. In L0, during silent disconnect, the absence of the digital ping from eUSPn within EOP of any packet transmitted to eDSPn is an indication of device disconnect. A digital ping is defined as a digital pulse of variable duration transmitted at eD- or eD+ during EOP reception.

- An eUSPn shall transmit a digital ping within the window of EOP. It shall transmit the digital ping based on the following:

    - It shall start transmitting the digital ping upon detecting the first falling edge of EOP as shown in t0 of Figure 4-2. It shall allow T_{DPING_SU} for eDSPn to sample the digital ping.
    - It shall complete transmitting the digital ping on the second falling edge of EOP as shown in t2 of Figure 4-2. It shall allow T_{DPING_SU} for eDSPn to sample the digital ping.
- An eDSPn in FS operation shall sample at eD- for digital ping on the second rising edge of EOP as shown in t1 of Figure 4-2.
- An eDSPn in LS operation shall sample at eD+ for digital ping on the second rising edge of EOP.
- eDSPn shall declare device disconnect upon detecting missing of the digital ping.

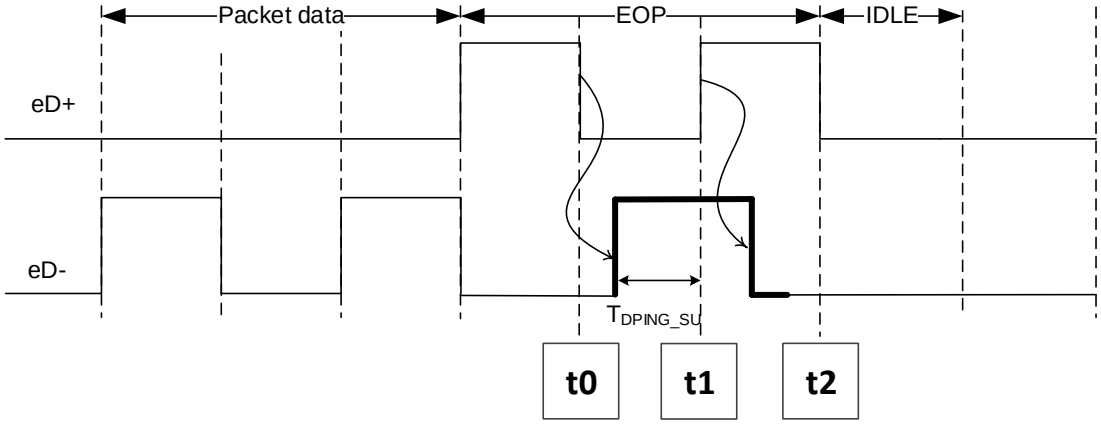


Figure 4-2: FS Digital Ping on EOP

Figure 4-3 illustrates an established FS link disconnecting with its device performing a silent disconnect.

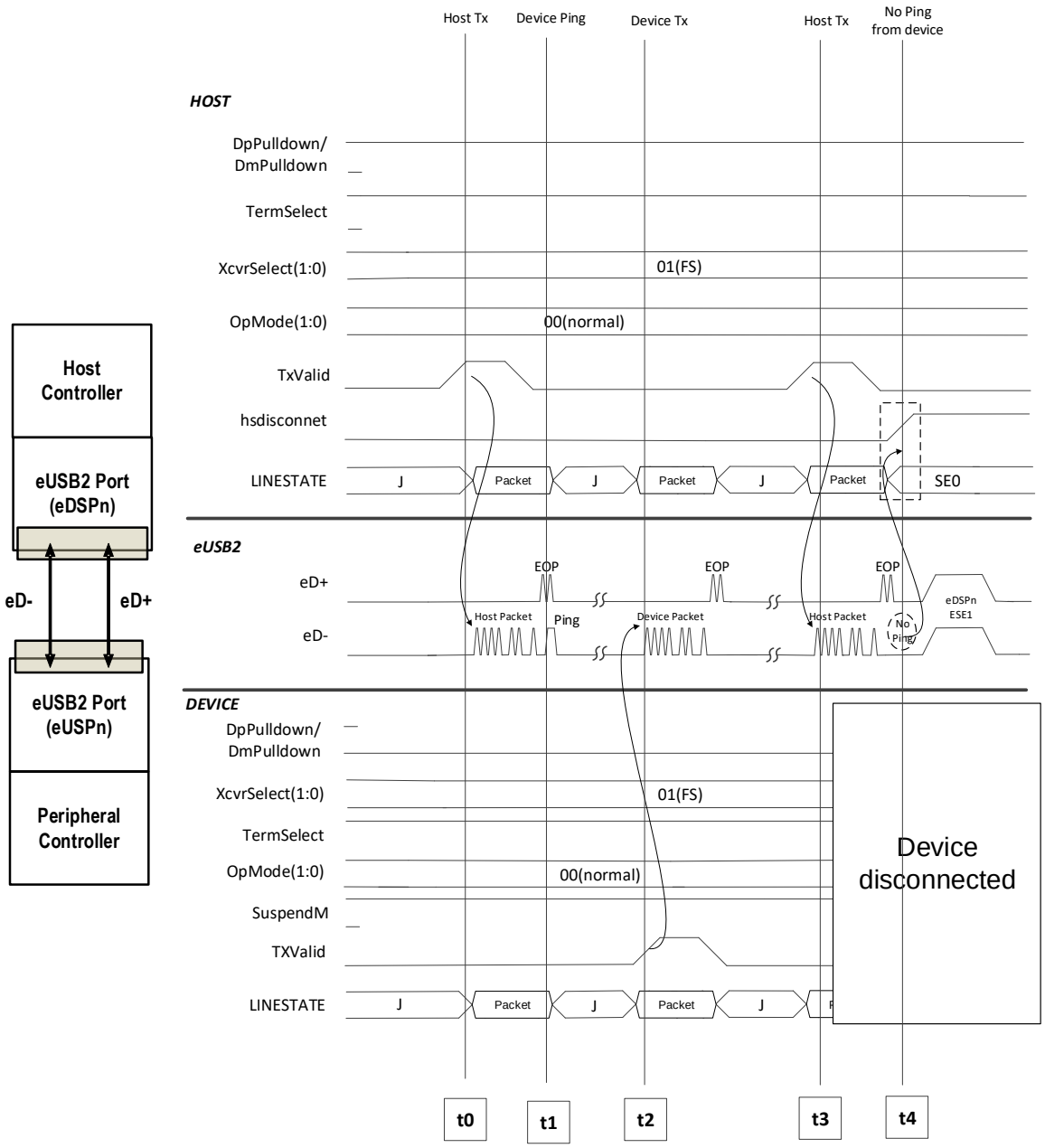


Figure 4-3: FS disconnect in L0

t0:

- eDSPn transmits data packet.

t1:

- eUSPn transmits digital ping at EOP.

t2:

- eUSPn transmits data packet.
- Digital ping not required from eDSPn.

t3:

- eDSPn transmits data packet.
- eUSPn disconnected, hence no digital ping returns to eDSPn.

t4:

- eDSPn declares device disconnect reflecting UTMI+ disconnect to its host.

- eDSPn transmits Port Reset for a potential new USB session (as an attempt to restart link in the possibility of a hang device).

4.2.3.1.2 Port Reset (ESE1)

An eUSPn and eDSPn utilize Port Reset (ESE1) to reset the link as described below:

- An eUSPn as directed by its controller to perform a soft disconnect.
-
- An eDSPn shall also declare device disconnect when a device Port Reset is received.

4.2.3.2 Low-speed/Full-speed Disconnect Detect during L1, L2, End of Resume, or End of Reset

The SE0 idle state of eUSB2 is maintained by both ports through their R_{PD} during L1 and L2. This is different from idle state J defined in USB2.0 that allows for disconnect detect during these states. A digital mechanism and Port Reset are defined for eUSB2 device disconnect detect during L1 and L2.

4.2.3.2.1 Digital Ping

An eUSPn in L1 or L2 transmits a digital ping to announce its presence within the EOResume/Reset as indication of device presence. A digital ping is defined as a digital pulse of variable duration transmitted at eD- or eD+ during EOP reception. An example of the FS digital ping transmission at the end of resume is shown in Figure 4-4.

- An eUSPn shall transmit a digital ping within the window of EOResume/Reset. It shall transmit the digital ping based on the following:
  - It shall start transmitting the digital ping upon detecting the first falling edge of EOP as shown in t1 of Figure 4-4.
  - It shall complete transmitting the digital ping on the second raising edge of EOP as shown in t3 of Figure 4-4.
  - Note that eUSPn shall ensure the assertion of digital ping before T_{DPING_SU} to ensure proper sampling by eDSPn.
- An eDSPn in FS operation shall sample at eD- for digital ping on the second rising edge of EOP as shown in t3 of Figure 4-4.
- An eDSPn in LS operation shall sample at eD+ for digital ping on the second rising edge of EOP.
- eDSPn shall declare device disconnect upon detecting missing of the digital ping.

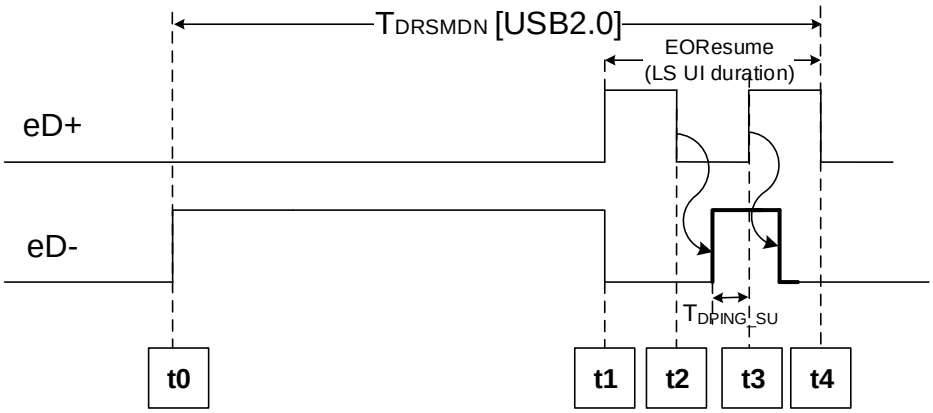


Figure 4-4: Illustration of an eUSPn Transmitting Digital Ping at the FS End of Resume

t0. eDSPn drives eD- to logic ‘1’ to start resume.
t1. eDSPn transmits FS EOResume (LS UI duration) to conclude resume.
t2. eUSPn, upon detecting EOResume, transmits a digital ping.
t3. eDSPn sample digital ping to declare device present or disconnect.
t4. Link enters L0.

4.2.3.2.2 Port Reset (ESE1)

An eUSPn and eDSPn utilize Port Reset (ESE1) to reset the link as described below:

- An eUSPn as directed by its controller to perform a soft disconnect.
-
- An eDSPn shall also declare device disconnect when a device Port Reset is received.

4.2.3.3 High-speed Disconnect Detect during L0

The SE0 idle state of eUSB2 is maintained by both ports through their R_{PD} in HS L0. An analog ping mechanism and Port Reset are defined for eUSB2 HS device disconnect detect during L0.

4.2.3.3.1 Analog Ping

For an eDSPn, high-speed disconnect detect is performed based on the eUSPn periodically transmitting an analog ping to the eDSPn to announce its presence. This is illustrated in Figure 4-5 .

- An eDSPn shall transmit an uSOF packet upon directed by its controller with 8 UIs of EOP length (instead of 40UIs as in USB2.0) to allow window for analog ping.
- An eDSPn while transmitting this 8 UIs uSOF.EOP shall maintain its interface (i.e. linestate) to its host controller as 40UIs to prevent subsequent controller’s TX during analog ping.
- An eUSPn shall transmit an analog ping after receiving the end of HS EOP as defined in Figure 4-5.
- An eUSPn may require maintaining 40UIs uSOF.EOP on its UTMI+ interface to the controller (i.e. linestate) depending on device controller implementation requirement.
- An analog ping shall be a high-speed data K with pulse width of $T_{ANALOGPING}$ as shown in Figure 4-5.
- An eUSPn shall enable its squelch detector no later than the minimum time of $T_{TURNAROUND}$ after the completion of uSOF.EOP transmission.
- An eDSPn shall declare device disconnect if It has not received any analog pings from the device after the end of HS EOP of uSOF packets.

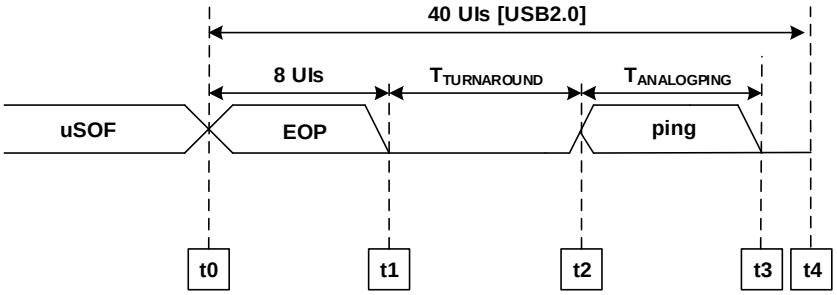


Figure 4-5: Illustration of Device Transmitting an Analog Ping

t0. eDSPn starts transmitting EOP of uSOF. Note that it is only 8 UIs instead of 40 UIs. This allows 32 UIs for the eUSB2 bus to turnaround and transmit the analog ping.
t1. eDSPn completes packet transmission and both eDSPn/eUSPn enter L0 idle.
t2. eUSPn starts transmits the analog ping to announce its presence.
t3. eUSPn completes the analog ping transmission.
t4. eDSPn/eUSPn enter L0 idle.

Figure 4-6 illustrates an established HS link disconnecting with its device performing a silent disconnect.

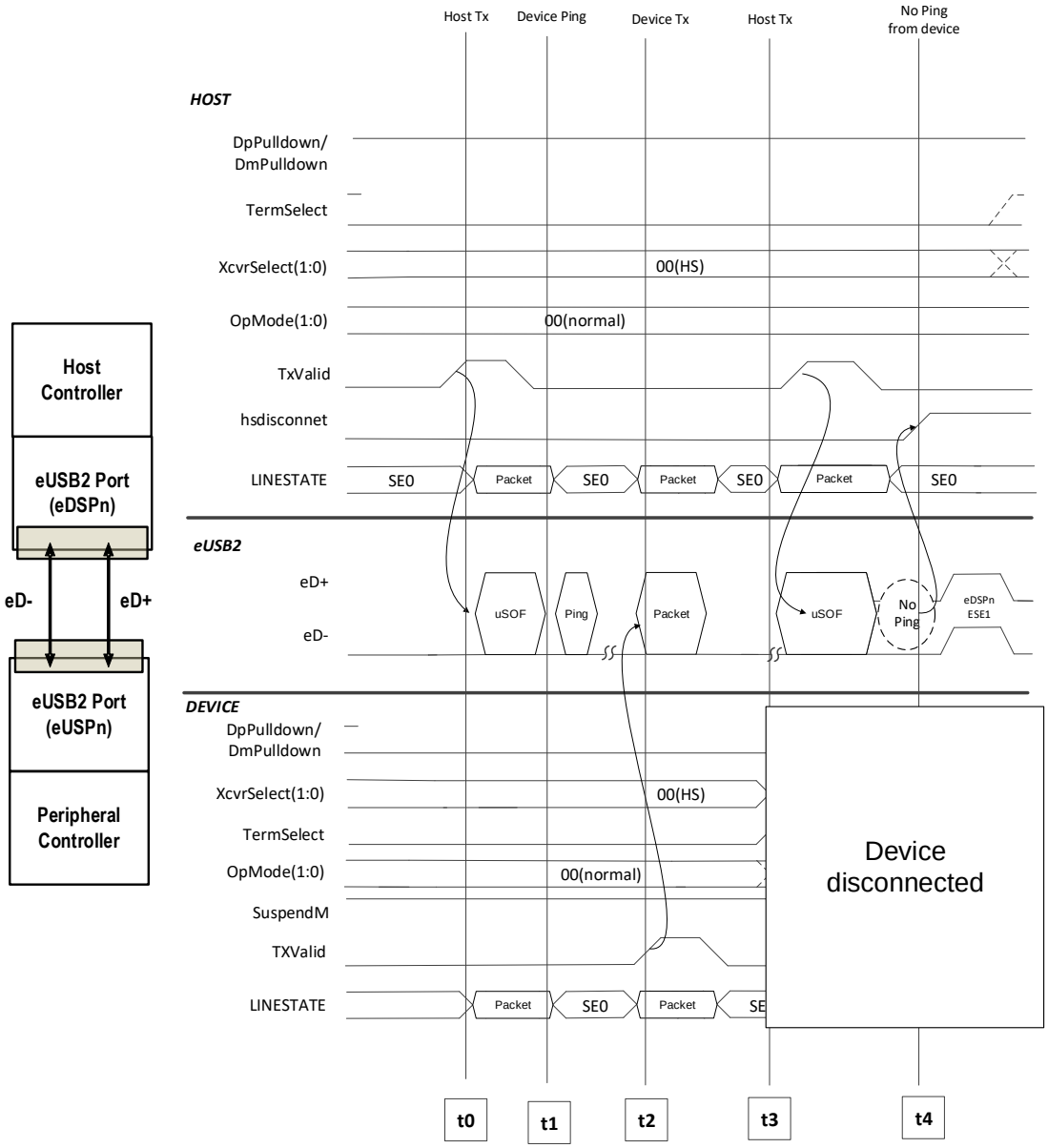


Figure 4-6: HS disconnect in L0

t0:

- eDSPn transmits uSOF packet.

t1:

- eUSPn transmits analog ping at uSOF EOP.

t2:

- eUSPn transmits data packet.
- Analog ping not required from eDSPn.

t3:

- eDSPn transmits uSOF packet.
- eUSPn disconnected, hence no analog ping returns to eDSPn.

t4:

- eDSPn declares device disconnect after not receiving analog ping on uSOFs and reflecting UTMI+ disconnect to its host.
- eDSPn transmits Port Reset for a potential new USB session (as an attempt to restart link in the possibility of a hang device).

4.2.3.3.2 Port Reset (ESE1)

An eUSPn and eDSPn utilize Port Reset (ESE1) to reset the link as described below:

- An eUSPn as directed by its controller to perform a soft disconnect.
- An eUSPn shall perform Port Reset upon reconnect if a silent disconnect occurred.
- An eDSPn shall also declare device disconnect when a device Port Reset is received.

4.2.3.4 High-speed Disconnect Detect during L1, L2, End of Resume, or End of Reset

4.2.3.4.1 Digital/Analog Ping

An eDSPn does not performs disconnect detection at the end of Reset or end of Resume to HS as opposed to FS/LS since eUSPn is not expected to transmit digital/analog ping at the end of Reset or Resume.

4.2.3.4.2 Port Reset (ESE1)

An eUSPn and eDSPn utilize Port Reset (ESE1) to reset the link as described below:

- An eUSPn as directed by its controller to perform a soft disconnect.
-
- An eDSPn shall also declare device disconnect when a device Port Reset is received.

4.3 *PHY State Transition and Power Management*

A conceptual eUSB2 PHY state machine is shown in Figure 4-7. It summarizes the basic behavior of the eUSB2 native operation during power-up, connect, reset, resume and wake, which will be described in detail in this section.

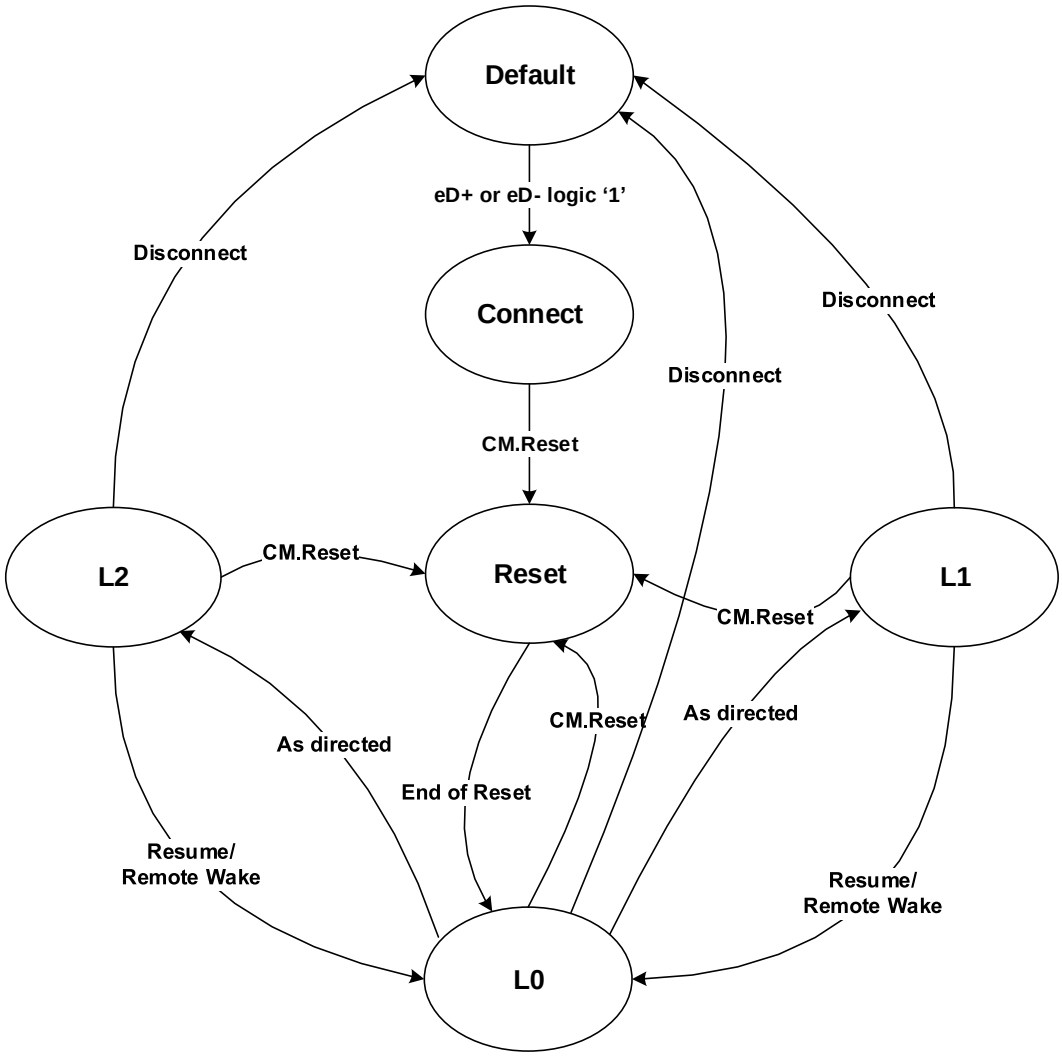


Figure 4-7: eUSB2 Native Link State Machine

4.3.1 **Default**

The power-up sequence may be asynchronous between a downstream port and an upstream port. The mechanism for connect detection is different. Refer to Figure 4-8 for a power-up timing diagram. The port shall perform the following upon power-up:
An eDSPn shall perform the following:

- It shall enable R_{PD} at eD+ and eD-.
- It shall transmit Port Reset (ESE1) as defined in Section 3.3.8 before disabling its transmitters.
- Upon completing Port Reset, it shall transmit Port Configuration as defined in Section 4.2.2 and wait for eUSPn to acknowledge.
- It shall enable its SE receivers and wait for device connection from eUSPn.

To decouple any USB2.0 protocol from CM.RAP and to avoid unnecessary contention, CM.RAP communication shall occur only in this state (prior to Port Configuration).

An eUSPn shall perform the following:

- It shall enable R_{PD} at eD+ and eD-.
- It shall not transmit Port Reset in this state (It shall not transmit Port Reset prior to acknowledging Port Configuration from eDSPn), but monitor its eUSB2 port for Port Reset, Port Configuration or CM.RAP from the eDSPn. Due to the asynchronous POR of both the eDSPn and eUSPn, the eUSPn may sample at any point of the Port Reset (ESE1), CM.RAP or Port Configuration from eDSPn coming out from POR which the eUSPn is recommended to have a timer to distinguish among ESE1, CM.RAP and Port/Repeater Configuration.
- It shall transmit an acknowledgement upon detecting eDSPn Port Configuration as defined in Section 4.2.2.

4.3.2 **Connect**

Connect is a state where the eUSPn is attaching to its eDSPn.

- An eUSPn shall perform the following after acknowledging to eDSPn Port Configuration:
  - If the port operates at full-speed/high-speed, and observes SE0 at eD+/eD-, it shall drive logic ‘1’ at eD+.
  - If the port operates at low-speed and observes SE0 at eD+/eD-, it shall drive logic ‘1’ at eD-.
  - Upon declaring an acknowledgement from the eDSPn, an eUSPn shall do the following:
    - If it operates at full-speed/high-speed it shall:
      - Drive logic ‘0’ at eD+ for $T_{SE0\_DR\_LSFS}$ and then disable its eD+ transmitter.
      - Enable its single-ended receiver at eD+.
    - If it operates at low-speed it shall:
      - Drive logic ‘0’ at eD- within $T_{SE0\_DR\_LSFS}$ and disable its transmitter.
      - Enable its single-ended receiver at eD-.

An eDSPn shall perform the following:

- Upon completing the Port Configuration, an eDSPn shall proceed for device connect detection.
- Upon detecting device connect, an eDSPn may (shall debounce with mechanical hotplug) perform debounce. The debounce period is implementation specific depending on the platform requirements. A downstream port shall declare device connect and acknowledge the device accordingly based on one of the following:
  - If it has detected logic ‘1’ at eD+ and logic ‘0’ at eD-, it shall start driving logic ‘1’ at eD-.
  - If it has detected logic ‘0’ at eD+, and logic ‘1’ at eD-, it shall start driving logic ‘1’ at eD+.
- An eDSPn shall complete the connect acknowledgement and declare the following:
  - If it is driving logic ‘1’ at eD- for acknowledgement, and observes logic ‘0’ at eD+, it shall drive logic ‘0’ at eD- and declare full-speed/high-speed device connect.
  - If it is driving logic ‘1’ at eD+ for acknowledgement, and observes logic ‘0’ at eD-, it shall drive logic ‘0’ at eD+ and declare low-speed device connect.

Refer to Figure 4-8 for a FS connect timing diagram.

4.3.3 **Reset**

In the Reset state, both eDSPn and eUSPn is performing a bus reset and speed negotiation.

An eUSPn shall perform the following:

- An eUSPn shall enter reset upon detection of logic ‘1’ on eD+ for FS device connect or logic ‘1’ on eD- for LS device connect respectively.
- An eUSPn shall transmit device chirp as defined in USB2.0, as directed by its controller.
- An eUSPn may expect host chirp K-J from eDSPn before the end of reset and shall reflect this to its UTMI+ interface to its device controller. Refer to Figure 4-9 for HS negotiation. Note: The eUSPn may not observe host K-J chirp (for a FS capable only host). In this event the eUSPn shall maintain SE0 on both eD+/eD- expecting to receive FS EOReset from eDSPn.
- An eUSPn shall end Reset and reflect this to its UTMI+ interface, if it detected EOReset as defined in Section 3.3.4.

An eDSPn shall perform the following:

- When directed by the host controller, an eDSPn shall transmit a logic ‘1’ on eD+ for FS device connect or logic ‘1’ on eD- for LS device connect respectively to initiate device reset.
- An eDSPn shall perform the speed detection as defined in USB2.0.
- An eDSPn may expect device chirp K from the eUSPn indicating HS capable upstream port.
- An eDSPn shall perform host K-J chirp as directed by its controller. Note: The eDSPn may not be directed to transmit host K-J chirp if it is not HS capable.
- An eDSPn shall perform one of the following to conclude reset as directed by its host:
    - If it operates at LS, it shall transmit a LS EOP to conclude reset.
    - If it operates at FS, it shall transmit a FS EOP (LS UI duration) to conclude reset.
    - If it operates at HS, it shall transmit a single acknowledgement pulse of T_{STROBE} at eD+ at the end of host chirp acknowledgement to conclude reset. Refer to section 3.7.3 for definition of high-speed end of reset.

4.3.3.1 FS link Reset timing diagram

Figure 4-8 below illustrate the timing flow of a native eUSB2 host and device establishing a FS link.

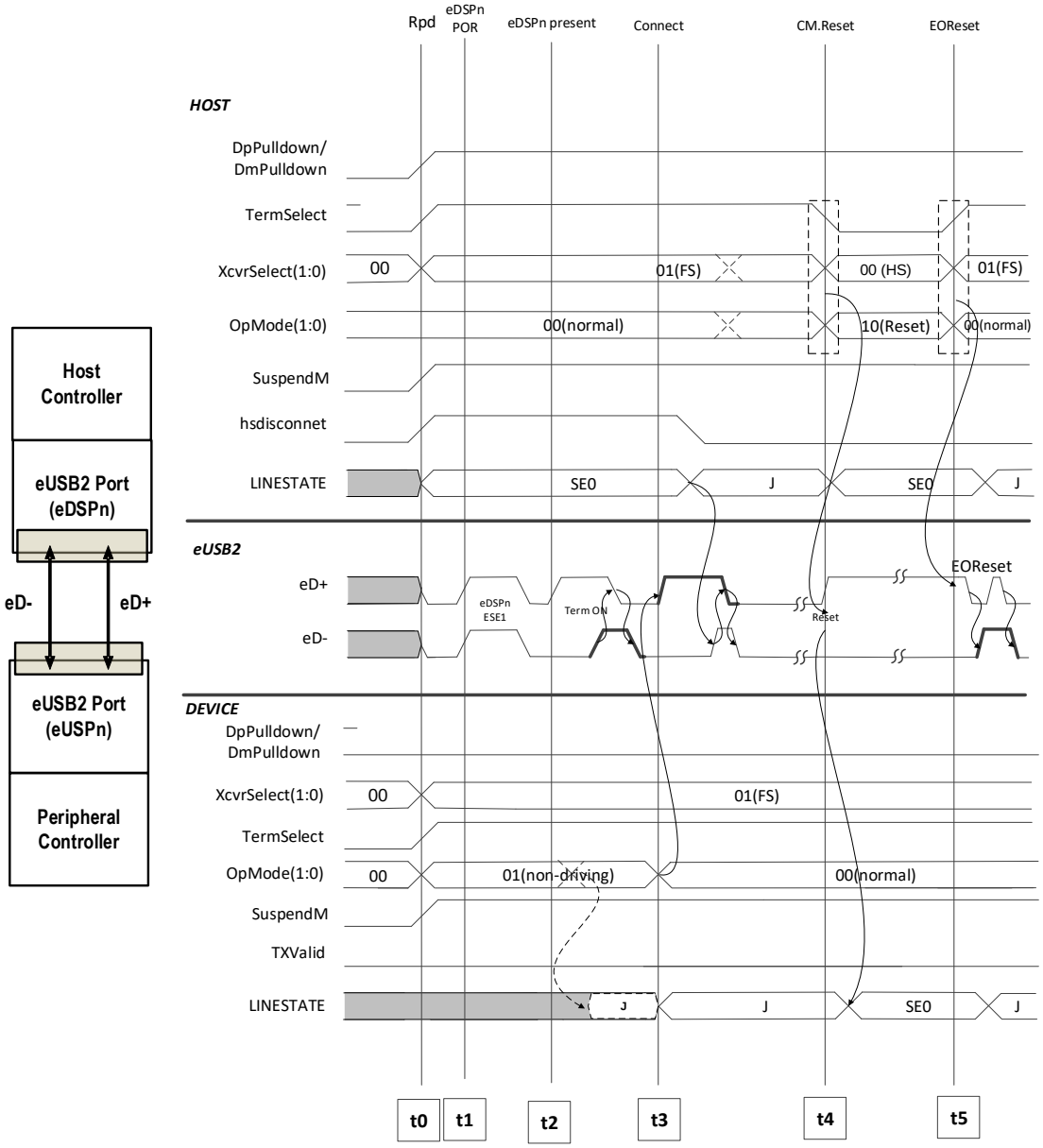


Figure 4-8: FS connect

t0:

- Both eDSPn and eUSPn power up and turning on its R_{PD} respectively. Note: This event may be asynchronous as both eDSPn and eUSPn may be powered up at a different time.

t1:

- eDSPn POR and transmit Port Reset.

t2:

- eDSPn transmit present announcement with termination enabled.
- eUSPn acknowledge present announcement.

t3:

- eUSPn signal connect with logic ‘1’ on eD+ as directed by its device controller.
- eDSPn acknowledge eUSPn device connect with a logic ‘1’ on eD- and reflect device connect on its UTMI+ interface.
- Note that, as illustrated with the dotted arrow, UTMI+ opmode may have transition to “normal” earlier (or at time zero). In this scenario, the eUSPr shall change its UTMI+ linestate to J but only transmit logic ‘1’ on eD+ after it has completed power reset announcement.
- eUSPn drive a logic ‘0’ (before releasing to R_{PD} idle), upon detecting a logic ‘1’ acknowledgement from eDSPn,
- eDSPn drive logic ‘0’ (before releasing to R_{PD} idle), upon detecting a logic ‘0’ from eUSPn.

t4:

- eDSPn drive logic ‘1’ on eD+ (R_{PD} on eD-) representing a bus reset SE0 on USB2.0. Note: Depending on implementation, UTMI+ xcvrselect and opmode may not change together with UTMI+ termselect. UTMI+ termselect may be the sole trigger for bus reset.
- eUSPn reflect bus reset to its UTMI+ interface.

t5:

- eDSPn end bus reset with Reset EOP. Note: Depending on implementation, UTMI+ xcvrselect and opmode may not change together with UTMI+ termselect. UTMI+ termselect may be the sole trigger for bus reset.
- eUSPn responds with a digital ping as defined in Section 4.2.3.2.

4.3.3.2 HS link Reset timing diagram

Figure 4-9 below illustrate the timing flow of a native eUSB2 host and device establishing a HS link.

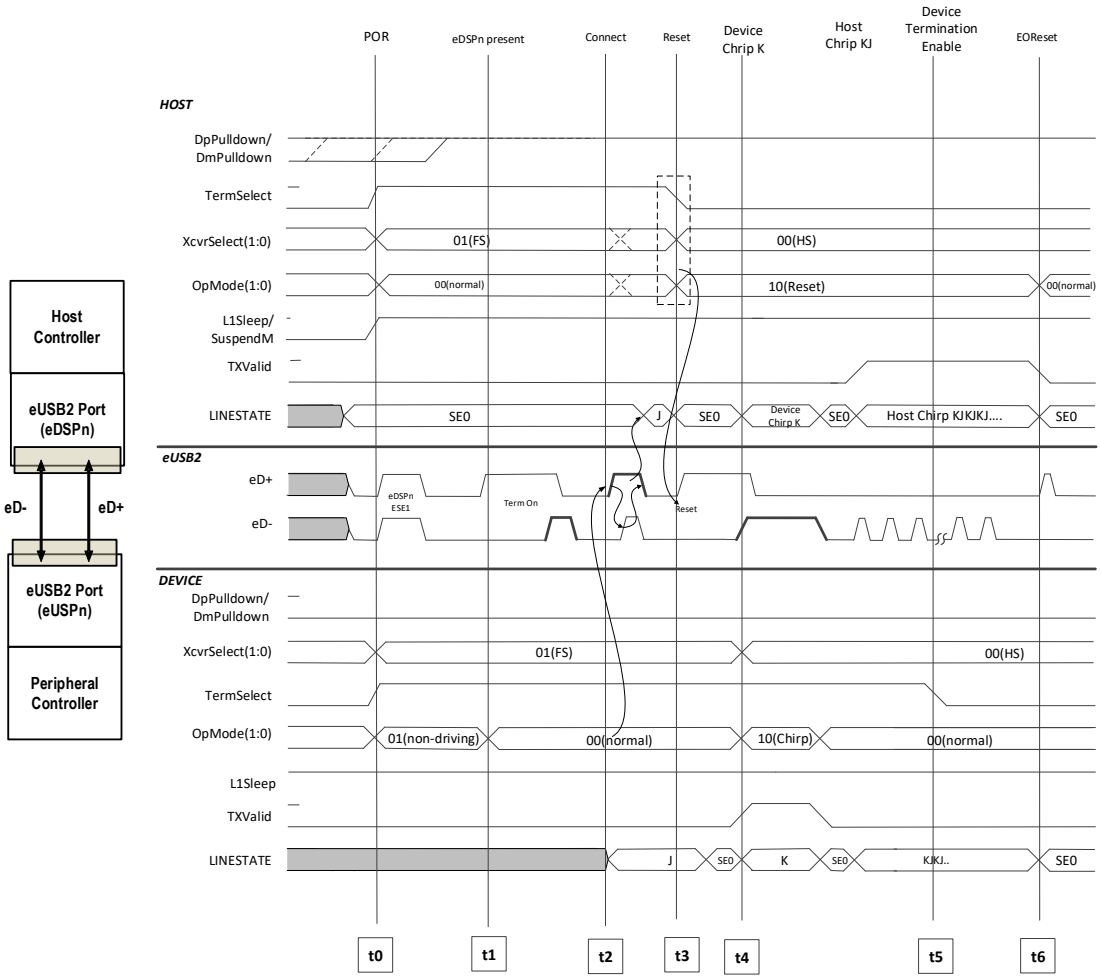


Figure 4-9: HS connect

t0:

- eDSPn POR transmit Port Reset.

t1:

- eDSPn transmit present announcement with termination enable.
- eUSPn acknowledge.

t2:

- eUSPn announces device connect with logic ‘1’ on eD+ as directed by its device controller.
- eDSPn acknowledge eUSPn device connect with a logic ‘1’ on eD- and reflect device connect on its UTMI+ interface.
- eUSPn drive a logic ‘0’ (before releasing to R_{PD} idle), upon detecting a logic ‘1’ acknowledgement from eDSPn,
- eDSPn drive logic ‘0’ (before releasing to R_{PD} idle), upon detecting a logic ‘0’ from eUSPn.

t3:

- eDSPn drive logic ‘1’ on eD+ (R_{PD} on eD-) representing a bus reset SE0 on USB2.0.

- Note: Depending on implementation, UTMI+ xcvrselect and opmode may not change together with UTMI+ termselect. UTMI+ termselect may be the sole trigger for bus reset.
- eUSPn reflect bus reset to its UTMI+ interface.

t4:

- eUSPn transmit device chirp as directed by its device controller.
- eDSPn drops eD+.
- eDSPn HS K-J chirp sequence follow.

t5:

- eUSPn enable HS termination.

t6:

- eDSPn transmit EOReset to complete speed negotiation.
- Note: Depending on implementation, UTMI+ xcvrselect and opmode may not change together with UTMI+ termselect. UTMI+ termselect may be the sole trigger for bus reset.
- Note: no digital ping transmitted from eUSPn.

4.3.4 L1, L2, Resume and Remote Wake

The policies for suspend, resume, and remote wake are like USB2.

4.3.4.1 L1, L2 and Resume

eUSB2 shall support LPM-L1 (L1) based on USB2.0 Link Power Management Addendum. The L1 entry is initiated through L1 extended transaction as described in USB2.0 Link Power Management Addendum.

For entry to L1 and L2,
An eUSPn shall perform the following:

- An upstream port shall enter suspend if it has detected link idle for the duration of 3ms as directed by its device controller for L2 entry.
- An upstream port shall enter L1 as directed by its device controller.

An eDSPn shall perform the following:

- A downstream port shall transition to L1 and L2 when directed by its controller.

For resume from L1 and L2, the port shall adhere to the following rules:
An eUSPn shall perform the following:

- Upon detecting the resume signal, an upstream port shall proceed to exit from suspend based on the following:
  - An eUSPn operating at full-speed, shall transmit a digital ping at eD- upon detecting the LS EOP at eD+ and enter L0.
  - An eUSPn operating at low-speed, shall transmit a digital ping at eD+ upon detecting the LS EOP at eD- and enter L0.
  - If it is operating at high-speed, it shall enter L0 upon detecting the end of resume.

An eDSPn shall perform the following:

- A downstream port shall initiate resume by transmitting the Resume K defined below with timing defined in USB2.0.
  - If operating at full-speed/high-speed, it shall drive the Resume K at eD-.
  - If operating at low-speed, it shall drive the Resume K at eD+.
- A downstream port shall conclude resume by performing on of the following:

- If operating at full-speed, it shall transmit a LS EOP at eD+. It shall also perform device presence detect during EOP transmission.
- If operating at low-speed, it shall transmit a LS EOP at eD-. It shall also perform device presence detect during EOP transmission.
- If operating at high-speed, it shall transmit an end of resume signal at eD+. The end of resume signal shall be the same as the digital ping with 1 UI of LS duration.
- An eDSPn resuming to full-speed or low-speed shall enter Default if it has not received the digital ping at the end of resume.

Figure 4-10 shows the timing diagram of a FS link suspend entry and resume.

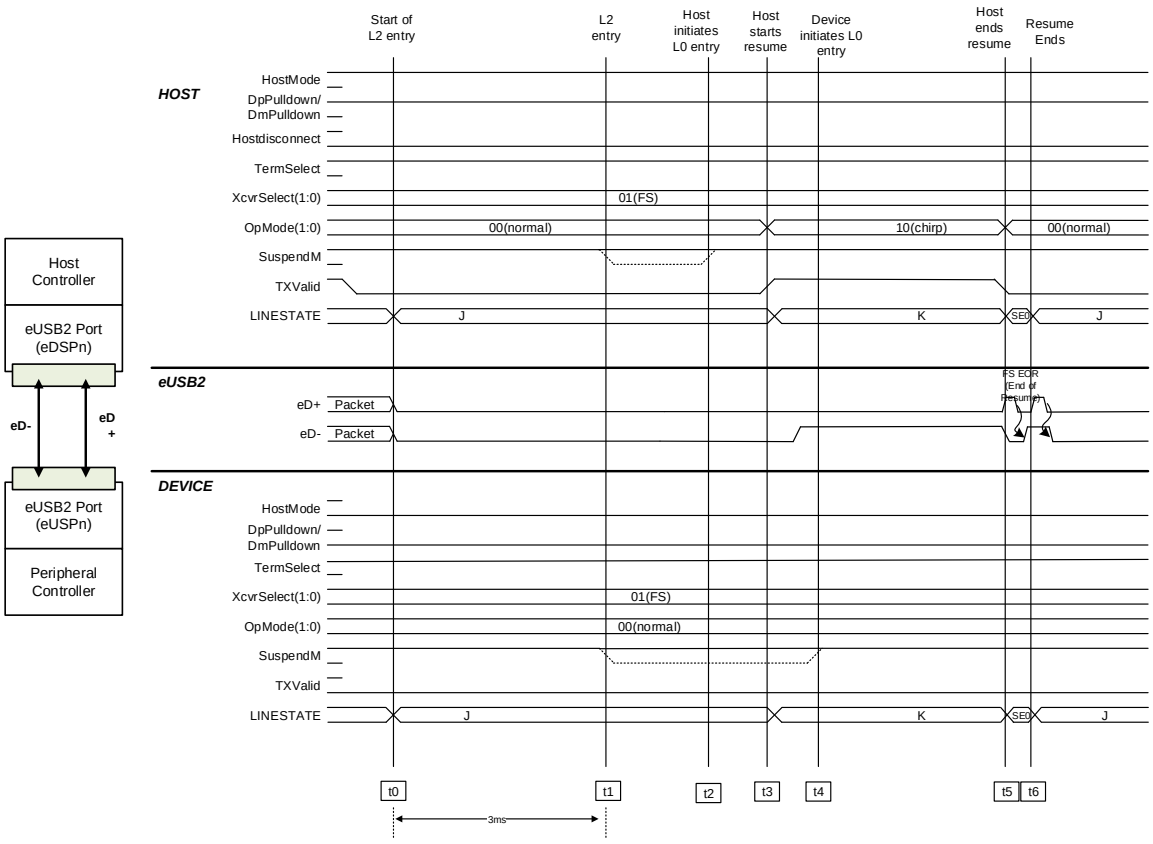


Figure 4-10: FS L2 & resume

t0:

- eDSPn initiate L2 entry as directed by its host controller with link going idle.

t1:

- eUSPn initiate L2 entry upon 3ms as directed by its device controller.
- Link enter L2.

t2:

- eDSPn initiate L0 entry as directed by its controller.

t3:

- eDSPn starts resume process as directed through its controller.
- eDSPn transmit logic ‘1’ on eD- as resume.

t4:

- eUSPn initiate L0 entry as directed by its controller.

t5:

- eDSPn end resume with EOResume.

t6:

- eUSPn responds with a digital ping as defined in Section 3.3.5.1.1.
- Both eDSPn and eUSPn enter L0.

4.3.4.2 Remote Wake from L1 and L2

For remote wake from L1 and L2, the port shall adhere to the following rules:
An eUSPn shall perform the following:

- An eUSPn port shall initiate remote wake based on the following:
  - If it is operating at full-speed/high-speed, it shall use eD- to initiate remote Wake K, the timing of which shall follow USB2.0.
  - If it is operating at low-speed, it shall use eD+ to initiate remote Wake K, the timing of which shall follow USB2.0.
  - Note that in the event of host not responding to the wake, an RC discharge would be observed on the eUSB line as illustrated in Section 3.3.6.1.1.

An eDSPn shall perform the following:

- A downstream port, upon detecting remote wake, shall acknowledge resume within T_{URSM} as defined by the USB2.0. A downstream port shall perform one of the following:
  - If it is full-speed/high-speed operation, it shall drive the resume signal at eD-, the timing of which shall follow USB2.0.
  - If it is low-speed operation, it shall drive the resume signal at eD+, the timing of which shall follow USB2.0.
  - The downstream port shall complete resume with EOResume as defined in Section 3.3.5.1.1.

Shown in Figure 4-11 is an example timing diagram of a link in FS operating from entry to L2, to an upstream port initiating remote wake, and a downstream port following up with resume.

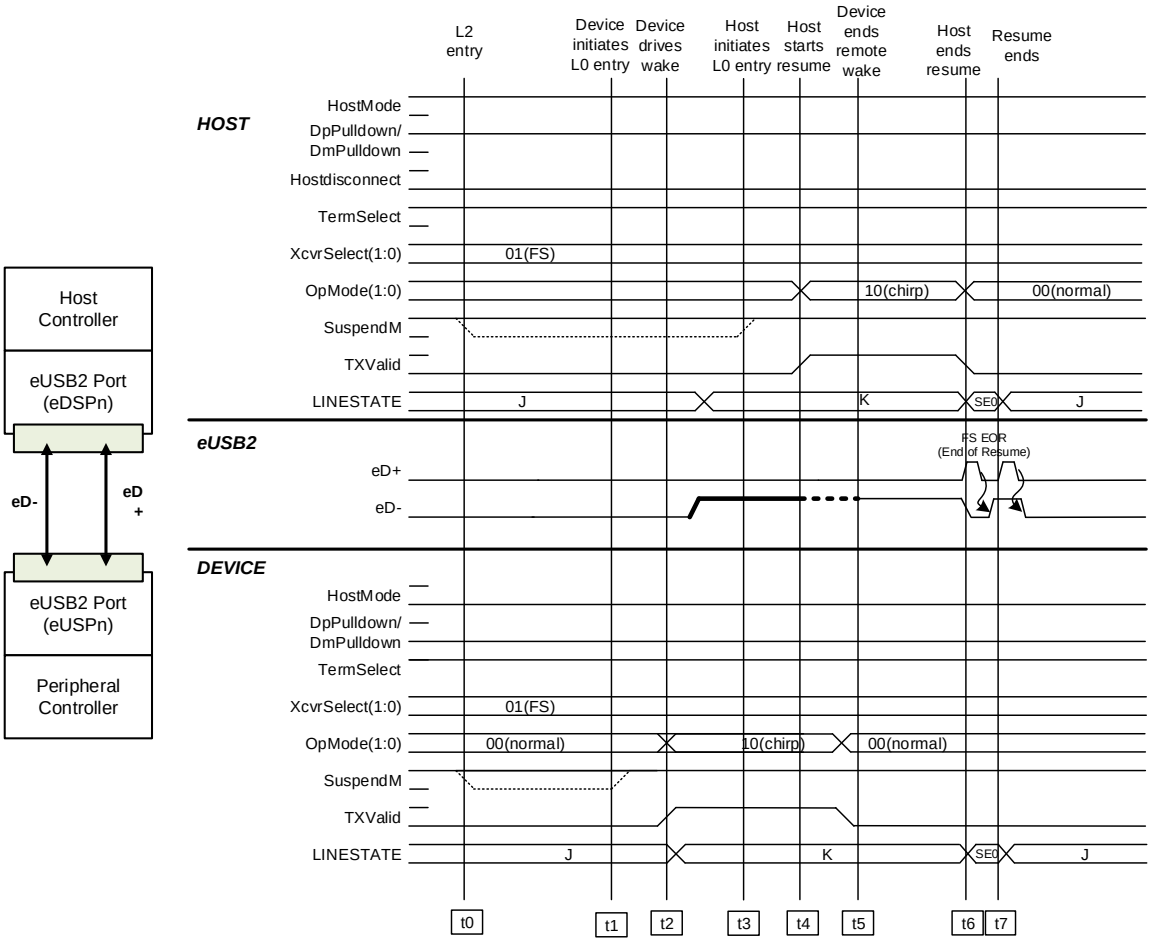


Figure 4-11: FS L2 & remote wake

t0:

- Link enter L2.

t1:

- eUSPn initiate L0 entry as directed by its controller.

t2:

- eUSPn starts remote wake process as directed through its controller.
- eUSPn transmit logic ‘1’ on eD- as wake.

t3:

- eDSPn initiate L0 entry as directed by its controller.

t4:

- eDSPn starts resume process as directed through its controller.
- eDSPn transmit logic ‘1’ on eD- as resume.

t5:

- eUSPn end remote wake as directed through its controller.

t6:

- eDSPn end wake resume with EOResume.
- eUSPn responds with a digital ping as defined in Section 3.3.5.1.1.
- Both eDSPn and eUSPn enter L0.

4.3.5 **Disconnect in L1 or L2**

As the eUSB line would remain as SE0 before and after disconnect, eUSPn and eDSPn shall perform the follow during disconnect and reconnect.

- Upon directed to perform a soft disconnect, eUSPn shall transmit a port reset announcement, ESE1 to eDSPn to terminate the current session.
- If the device is undergoing a silent disconnect, it is system level implementation to ensure a sideband communication to inform eDSPn.

4.3.6 **Reset during L0, L1 or L2**

An upstream port in L0, L1, or L2 shall enter reset if it has detected Bus Reset as defined in Section 3.3.4.

5 eUSB2 Repeater Architecture and Operation

This chapter describes the architecture and operation of an eUSB2 Repeater compliant to USB2.0 specification.

5.1 *eUSB2 Repeater*

An eUSB2 Repeater is working with an eUSB2 PHY in SOCs to support:

- USB2 host root hub DSP (Host Repeater)
- USB2 peripheral USP (Peripheral Repeater)
- USB2 Dual-role port (Dual-role Repeater)

5.1.1 Architecture and Interface

The architecture of an eUSB2 repeater is a half-duplex non-linear redriver. A simplified eUSB2 repeater block diagram is shown in **Figure 5-1**.

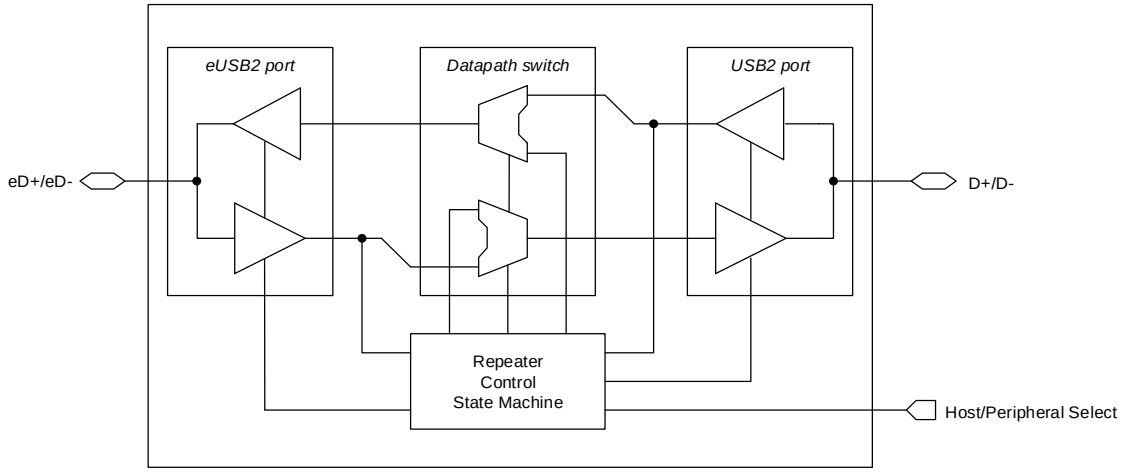


Figure 5-1: Dual-Role Repeater Architecture

5.1.2 Signaling Modes

An eUSB2 Repeater at any given time operates in one of the two signaling modes. This is shown in Figure 5-2.

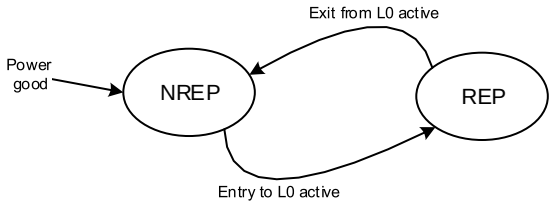


Figure 5-2: eUSB2 Repeater Operation Mode

- REP is a repeating signaling mode where packets are forwarded between eD+/eD- and D+/D-, with end to end timing preserved to meet the timing requirements defined by [USB 2.0] and eUSB2 specifications.

- NREP is a non-repeating signaling mode when the link is in one of the following states:
  - Initialization during Connect, Reset and Speed Negotiation.
  - L1 and Suspend.
  - L0 where a control message is being transmitted by local eDSPr/eUSPr to its associated Repeater. This includes CM.Reset or CM.FS. It may also include ESE1.

Timing in NREP mode is not as critical as in REP mode since the information transmitted is for control and status reporting purposes such as Control Message, Chirp, or Repeater Configuration Announcement.

5.1.3 Repeater Operation

Shown in Figure 5-3 are example block diagrams of a host repeater and a peripheral repeater with their respective host and peripheral eUSB2 port and controller. Note that the eUSB2 port and the repeater may be implemented as dual-role capable. The details of a dual-role repeater implementation are described in the following sections.

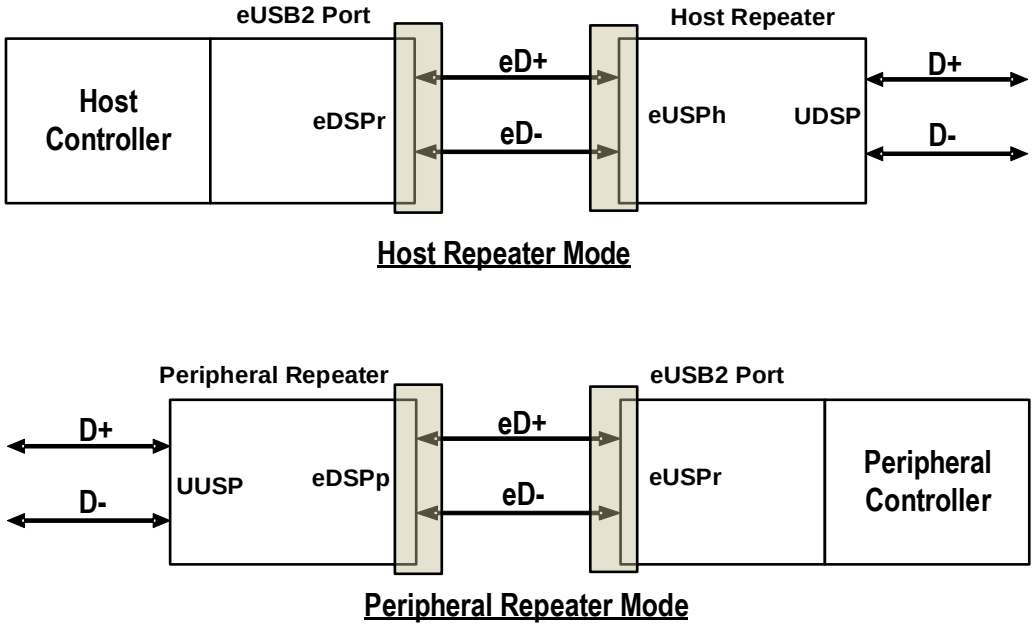


Figure 5-3: eUSB2 Repeater in Host or Peripheral Mode

5.2 *Dual-Role Repeater State Machine*

An informative two-level state machine of an eUSB2 dual-role repeater is defined. The top-level state machine defines the operation of an eUSB2 repeater from power-up. The second-level state machine defines the repeater operation in the host or peripheral mode upon entering the USB session.

5.2.1 Top Level Repeater State Machine

Shown in Figure 5-4 is the top-level dual-role repeater state machine. Note that the state machine also applies to a single-role host or peripheral repeater.

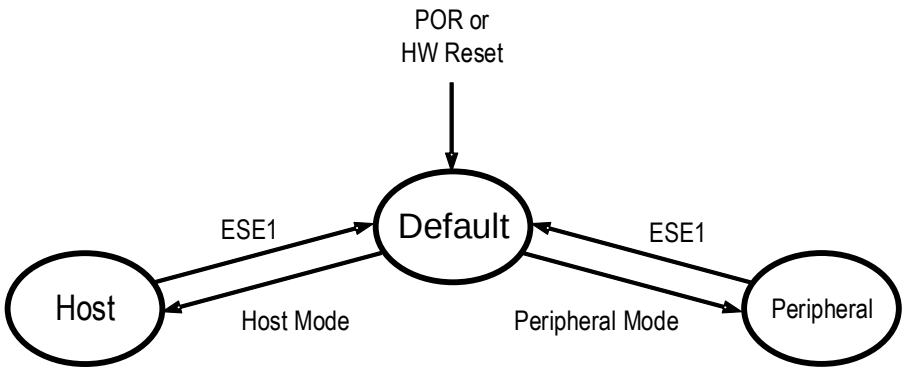


Figure 5-4: Top-Level eUSB2 State Machine

5.2.2 Default

Default is the power-on state upon POR or HW reset. In this state the repeater is waiting for configuration from the eUSBr (yet to be configured eUSB2 port). To decouple any USB2.0 protocol from CM.RAP and to avoid unnecessary contention, CM.RAP communication shall occur only in this state (prior to Repeater Configuration).

- This is a state the repeater or eUSBr shall transition to upon transmitting or receiving a Port Reset.
- A repeater in this state shall disable its USB2.0 transceiver and enable its eUSB receiver.
- The repeater's eUSB port shall be maintained as SE0 with R_{PD}.
- The repeater in this state shall not transmit any signaling but monitor its eUSB2 port for Port Reset, Repeater Configuration or CM.RAP from the eUSBr. Due to the asynchronous POR of both the repeater and the eUSBr, the repeater may sample at any point of the Port Reset (ESE1), CM.RAP or Repeater Configuration from eUSBr coming out from POR which the repeater is recommended to have a timer to distinguish among ESE1, CM.RAP and Port/Repeater Configuration.
- An eUSBr port, upon POR or HW reset, shall transmit Port Reset.
- An eUSBr port, upon completing Port Reset, shall configure the repeater by transmitting Repeater Configuration when directed. An eUSBr shall perform one of the following.
    - It shall transition to Host as eDSPr after Host repeater configuration is acknowledged.
    - It shall transition to Peripheral as eUSPr after Peripheral repeater configuration is acknowledged.
- A repeater, upon detecting Repeater Configuration, shall send an ACK and transition to Host mode or Peripheral mode operation accordingly.
- An eUSBr shall end Repeater Configuration upon detecting an acknowledgment from the repeater by T_{CONFIG_CMPL}.
- Upon completing Repeater Configuration, eUSBr shall ensure an idle time of T_{CONFIG_IDLE} before transmitting the next signaling (i.e. Connect announcement from eUSPr)
- An eUSBr shall keep its UTMI+ interface to the controller idle (i.e. SE0 on linestate) while configurating its repeater.

- The eDSPr shall reconfigure its repeater with Repeater Configuration if Port Reset is received for HS device disconnect. Note that eDSPr may utilize Port Reset to instruct its repeater to transition to default if its port is disabled (it is implementation specific how a host controller indicates port disable to its physical layer).

5.2.3 **Host**

Host is a state where an eUSB2 repeater is configured as a host repeater, and its associated eUSBr acts as an eDSPr port.

- An eDSPr port shall enter Default if one of the following conditions is met.
  - Upon completing Port Reset, if directed. Note that this is implementation specific on the interface from host controller to direct its associated PHY to perform port reset or terminate an existing USB session.
  - Upon detecting the device disconnect announcement from the host repeater.
- A host repeater shall enter Default if one of the following conditions is met.
  - Upon completing the HS device disconnect announcement.
  - Upon detecting Port Reset from the eDSPr.

5.2.4 **Peripheral**

Peripheral is a state where an eUSB2 repeater is configured as a peripheral repeater, and its associated eUSBr acts as an eUSPr port.

- An eUSPr port shall enter Default if directed and after Port Reset is transmitted.
- A peripheral repeater shall enter Default if Port Reset is received from eUSPr.

5.3 *Host Repeater Operation*

This section describes basic operations of an eUSB2 host repeater with its associated eDSPr. The operation state machine of the host mode repeater state machine is shown in Figure 5-5.

Note: eDSPr implementation may have a different state or state transition than the repeater. Below diagrams and description are an informative, not normative, guide to eDSPr implementation.

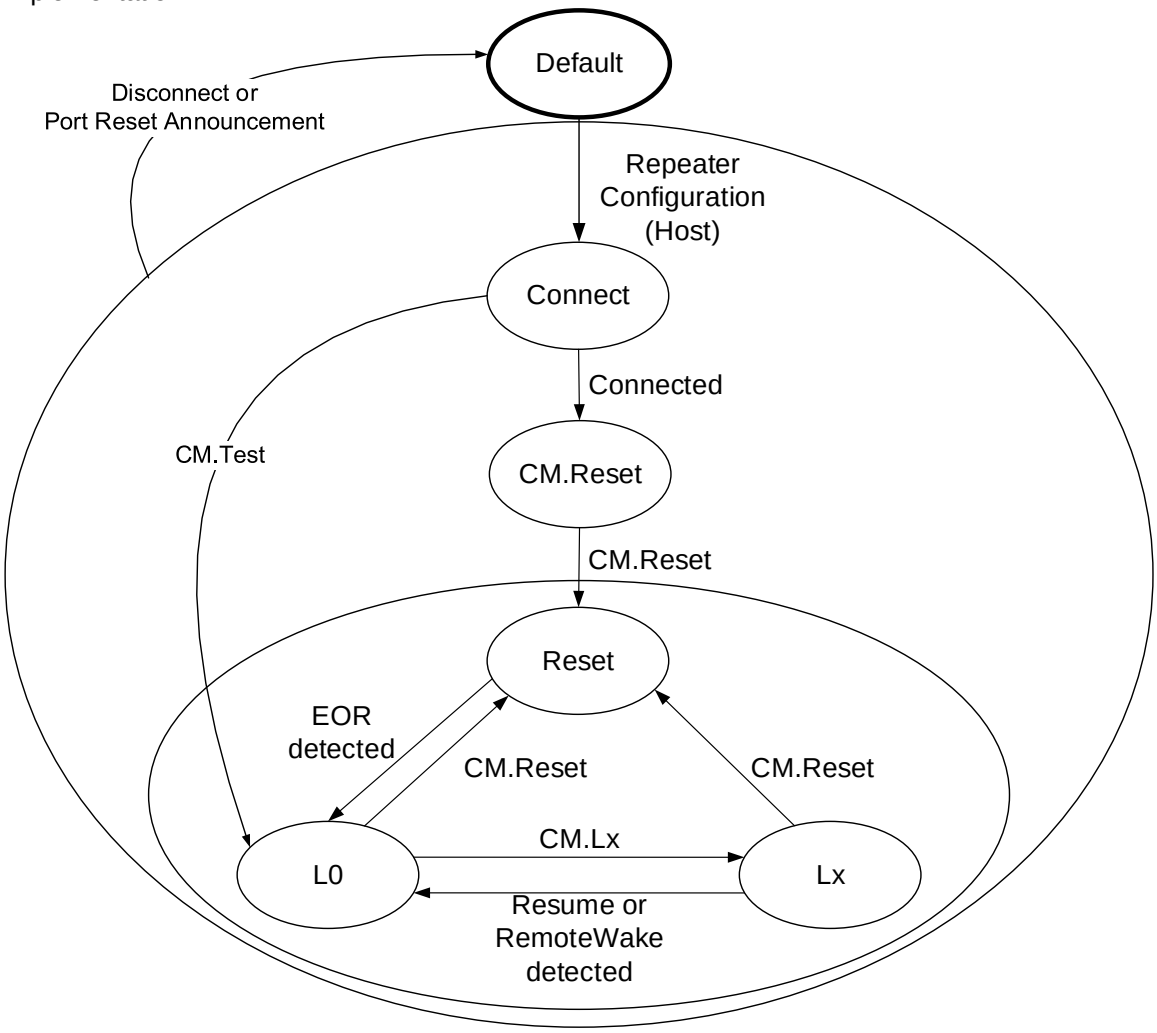


Figure 5-5: Host Mode Repeater State Machine

5.3.1 **Connect**

Connect is a state where the repeater operates under NREP mode. Repeater in this state shall monitor for device connect.

Section 5.5.1 illustrates a host repeater link detecting a FS connection upon POR.
Section 5.5.4 shows a host repeater detecting a peripheral connection and establishing a HS link upon POR.

Connect contains two substates (implementation may combine these to one state) as shown in Figure 5-6.

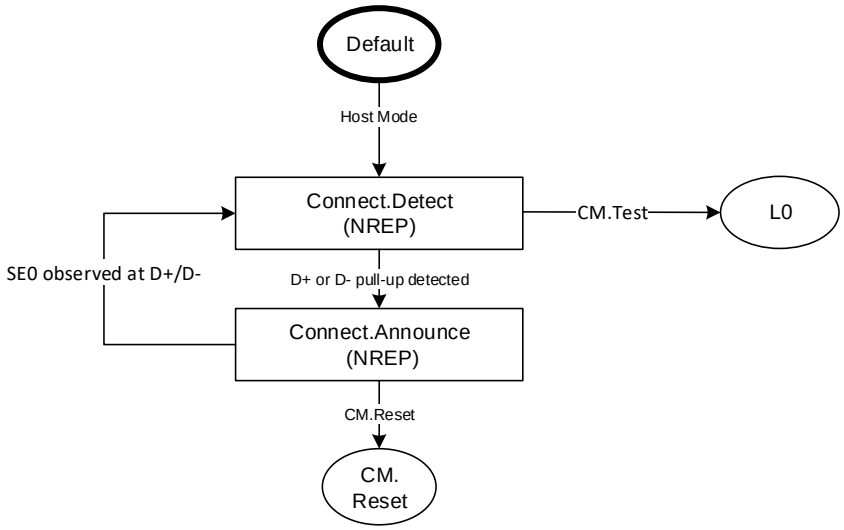


Figure 5-6: Connect Substates

5.3.1.1 Connect.Detect

Connect.Detect is a substate where the host repeater enables the FS transceiver at its UDSP in preparation for device connect.

5.3.1.1.1 Connect.Detect Requirements

The repeater shall meet the following conditions:

- It shall enable its R_{PD} at both eD+ and eD-.
- The SE receiver at its eUSB2 port shall be enabled.
- The FS transceiver at its UDSP shall be enabled.
- It shall perform USB2.0 device connect by monitoring the line state at D+/D-.
- It shall return to Default state if Port Reset is received.
- It should be in the lowest power state while monitoring for a device attach at the USB2.0 lines or port reset from eDSPr where both events are not timing critical. Note: It may turn off it UDSP SE receiver if device attach detection is performed out-of-band.
- It shall perform SCM detection and control message decoding for CM.Test.

The eDSPr shall meet the following conditions:

- It shall enable its R_{PD} at both eD+ and eD-.
- The SE receivers at its eUSB2 port shall be enabled.
- It shall transmit CM.Test as directed with the UTMI+ xcvrselect and termselect in HS and linestate is SE0. Note that different host controller implementation may have additional UTMI+ interface changed. Additionally, CM.Test shall be transmitted in an unconnected state where linestate is SE0.

5.3.1.1.2 Exit from Connect.Detect

The repeater shall perform the following tasks:

- It shall transition to Connect.Announce if D+ or D- pull-up is detected.
- It shall transition to Default if Port Reset is received.
- It shall transition to L0 and enable its HS termination for USB2.0 HS Compliance Test if CM.Test is received.

The eDSPr shall perform the following tasks:

- It shall transition to L0 and enable its HS termination for USB2.0 HS Compliance Test upon completed CM.Test to the eUSPh.

5.3.1.2 Connect.Annouce

Connect.Announce is a substate where the repeater relays the USB2.0 device connect event through its eUSB2 port to the eDSPr until it detects the host CM.Reset.

5.3.1.2.1 Connect.Announce Requirements

The repeater shall meet the following conditions:

- If D+ is pulled high and D- is pulled down, it shall drive logic '1' at eD+ and logic '0' at eD- through R_{PD}.
- If D- is pulled high and D+ is pulled down, it shall drive logic '1' at eD- and logic '0' at eD+ through R_{PD}.
- Note: it is expected that the USB2.0 D+ and D- lines may experience toggling, especially during a mechanical attach event. During this scenario, the host repeater shall perform the USB2.0 to eUSB2.0 mapping as shown in Table 5-1.
- Note: The host repeater is not required to perform debounce or de-glitching of the USB2.0 lines in any of its states.
- Note: Repeater is solely reflecting D+/D- to eD+/eD-. If disconnect occurs (prior to CM.Reset from eDSPr), repeater shall remain in this state and shall not expect a Port Reset from eDSPr.

Table 5-1: USB2.0 to eUSB2.0 mapping during connect

D+/D-	eD+/eD-	Note
SE0	SE0	eD+/eD- are being maintained with R_{PD}
SE1	SE0	The host repeater shall not produce SE1 on eUSB line. A SE1 on USB2.0 line is mapped to SE0 on eUSB2.0 with R_{PD}
High/Low	Logic '1'/R_{PD}	Indicating a FS/HS device attach
Low/High	R_{PD}/Logic '1'	Indicating a LS device attach
{High → Low}/Low	{Logic '1' → Logic '0' ($T_{SE0\_DR\_LSFS}$) → R_{PD}}/ R_{PD}	The host repeater shall drive $T_{SE0\_DR\_LSFS}$ before maintain logic '0' on eD+ with R_{PD}
Low/{High → Low}	R_{PD}/{Logic '1' → Logic '0' ($T_{SE0\_DR\_LSFS}$)} → R_{PD}	The host repeater shall drive $T_{SE0\_DR\_LSFS}$ before maintain logic '0' on eD- with R_{PD}

- The repeater shall monitor for CM.Reset coming from its eDSPr for bus reset.

The eDSPr shall meet the following conditions:

- It shall enable its R_{PD} at both eD+ and eD-.
- The SE receivers at its eUSB2 port shall be enabled.
- It shall reflect the state of eD+ and eD- from eUSPh to its UTMI+ interface to the host controller.
- The eDSPr may enter Lx when directed by its host controller, while keeping its SE receiver enabled to monitor device attach. Note that eDSPr (in the Connect state) shall not transmit any CM.Lx messages to its associated repeater for this Lx entry.

5.3.1.2.2 Exit from Connect.Announce

The repeater shall perform the following tasks:

- It shall transition to CM.Reset if it has detected CM.Reset from eDSPr.
- The repeater shall transistion to Default if it receives Port Reset.

The eDSPr shall perform the following tasks:

- It shall transition to CM.Reset when directed by it controller to perform bus reset.
- It shall stay in Connect if USB2.0 disconnect is detected.

5.3.2 **CM.Reset**

CM.Reset is a state where the repeater operates under NREP mode. In this state, the repeater is receiving CM.Reset from the eDSPr to perform a bus reset.

5.3.2.1.1 CM.Reset Requirements

The repeater shall meet the following conditions:

- It shall keep its R_{PD} enabled.
- It shall perform SCM detection and control message decoding. Note that a repeater may also receive Port Reset and shall be able to distinguish it from SCM based on its local timer.
- It shall sample D+/D- to determine the attached device speed (i.e. FS/HS if D+ is pulled high, LS if D- is pulled high) upon detecting CM.Reset.
- The UDSP of the repeater shall be in FS and continue monitoring the line state at D+/D.

The eDSPr shall meet the following conditions:

- It shall keep its R_{PD} enabled.
- The SE receivers shall be enabled.
- It shall transmit CM.Reset when directed by its Host controller on its UTMI+ interface to perform a bus reset.

5.3.2.1.2 Exit from CM.Reset

The repeater shall perform the following tasks:

- It shall transition to Reset if SE0 at eD+/eD- is detected after CM.Reset.
- The repeater shall transition to Default if it has detected Port Reset.

The eDSPr perform the following task:

- It shall transition to Reset upon completed CM.Reset.

5.3.3 **Reset**

Reset is a state where the repeater operates under NREP mode. In this state:
Reset contains multiple substates as shown in Figure 5-7. Section 5.5.8, 5.5.9, 5.5.10 and 5.5.11 shows various bus reset and speed detection timing waveform.

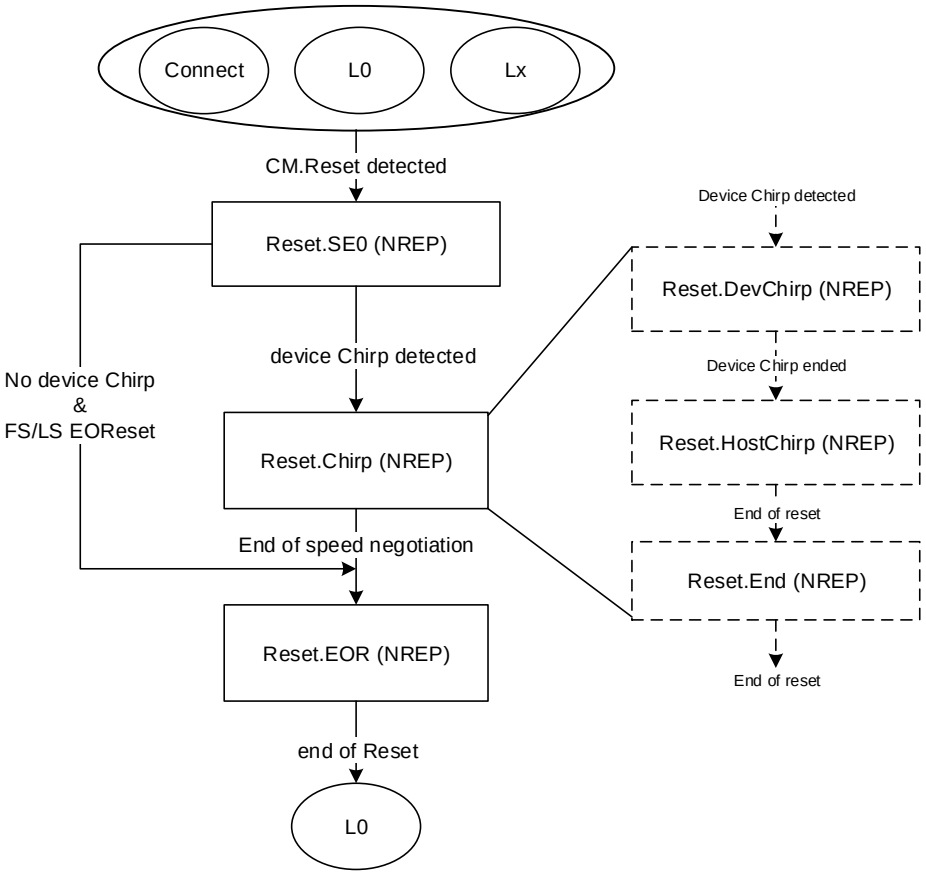


Figure 5-7: Reset Substate Machine

5.3.3.1 Reset.SE0

Reset.SE0 is a substate where the repeater is driving USB2.0 bus reset and expecting either speed negotiation or conclusion of reset.

5.3.3.1.1 Reset.SE0 Requirements

The repeater shall meet the following condition:

- It shall keep its SE receivers enabled on eUSB2 lines.
- The UDSP of the repeater shall drive USB2.0 bus reset and monitor for device chirp to start speed negotiation.

The eDSPr shall meet the following condition:

- It shall keep its SE receivers enabled in the event of device chirp.

5.3.3.1.2 Exit from Reset.SE0

The repeater shall perform the following tasks:

- The repeater shall transition to Reset.Chirp if device chirp is detected at UDSP.
- The repeater shall transition to Reset.EOR if it is in FS operation and has detected logic ‘1’ at eD+.

- The repeater shall transition to Reset.EOR if it is in LS operation and has detected logic '1' at eD-.

The eDSPr shall perform the following tasks:

- It shall transition to Reset.Chirp if logic '1' is detected on eD-.
- It shall transition to Reset.EOR when directed to end USB2.0 bus reset.

5.3.3.2 Reset.Chirp

Reset.Chirp is a substate where a high-speed device is connected, and the speed negotiation is performed. There are multiple stages of operations within Reset.Chirp to complete the speed negotiation, as shown in Figure 5-7. Section 5.5.4 shows the timing waveform of the reset chirp sequence.

5.3.3.2.1 Reset.Chirp Requirements

The repeater shall meet the following conditions:

- It shall enable its SE transmitter to transmit logic '1' at eD-.
- It shall enable its SE receiver at eD+/eD-.
- It shall disable it high-speed transceivers and terminations at eD+/eD- during speed negotiation.
- The UDSP shall meet the requirements defined by USB2.0. The operation of speed negotiation shall meet the following conditions. The repeater shall perform the following during device Chirp K detection, reception, and forwarding:
  - If the device Chirp K is received, it shall drive logic '1' at eD-.
  - If the device Chirp K is concluded, it shall drive logic '0' at eD- for $T_{SE0\_DR\_FSLS}$ before switching to pull-down.
  - Upon completion of device Chirp K forwarding, it shall disable its SE transmitter.
- The repeater shall perform the following to forward the K-J chirps from eDSP:
  - It shall drive Chirp K at D+/D- if it has detected logic '1' at eD-.
  - It shall drive Chirp J at D+/D- if it has detected logic '0' at eD-.
  - Note: The repeater may not observe host K-J chirp (for a FS capable only host). In this event the repeater shall maintain SE0 on both eD+/eD- and D+/D- and expect a FS EOReset from eDSP. Refer to Section 5.5.10 for timing diagram of Bus Reset of with FS Host and HS capable device.

The eDSPr shall meet the following conditions:

- It shall enable its SE receiver on eD- for logic '1' device chirp.
- Once device chirp is concluded on eD-, and eDSPr is directed by its host controller, it shall drive logic '1' on eD- for host Chirp K and logic '0' on eD- for host Chirp J.
- Note: In the event that the host controller is only FS capable, the eDSPr shall maintain SE0 on eD+/eD- expecting to end bus reset to FS as directed by its controller. Refer to Section 5.5.10 for Bus Reset of a FS Host timing diagram.

5.3.3.2.2 Exit from Reset.Chirp

The repeater shall perform the following:

- The repeater shall enter Reset.EOR upon completion of K-J Chirp forwarding and has detected EOReset (logic '0' at eD-, and logic '1' at eD+).
- In the event where the Host does not perform chirp K-J (e.g. A FS/LS capable only or a downgraded HS Host), the host repeater shall differentiate (implementation specific) them through the reset sequences expecting a FS EOReset and enter Reset.EOR accordingly.
- Refer to Section 5.5.8, 5.5.9, 5.5.10 and 5.5.11 for various link speeds bus reset timing diagram.

The eDSPr shall perform the following:

- It shall enter Reset.EOR as directed on UTMI+ upon completing K-J Chirp.
- Note: In the event that the host controller is only FS capable, the eDSPr shall maintain SE0 on eD+/eD- expecting a FS EOReset to end bus reset to FS as directed by its controller. Refer to Section 5.5.10 for Bus Reset of a FS Host timing diagram.

5.3.3.3 Reset.EOR

Reset.EOR is a substate where the eUSB2 host port concludes USB2.0 bus reset.

5.3.3.3.1 Reset.EOR Requirement

The repeater shall meet the following conditions:

- For LS/FS operation, the repeater shall perform the eUSB2 EOReset to USB2.0 EOReset mapping like the conversion of LS/FS eUSB2 EOP to USB2.0 EOP. Refer to Section 3.3.1 for details.
- For HS operation, the repeater shall meet the following conditions:
  - It shall drive SE0 at UDSP upon detecting rising edge of eD+.
  - It shall enable its HS transceivers and squelch detectors at its eUSPh and UDSP upon detecting the falling edge of eD+.

The eDSPr shall meet the following conditions:

- For LS/FS operation, it shall perform the eUSB2 EOReset as described in Section 3.3.1.
- For HS operation, it shall meet the following conditions:
  - It shall drive logic ‘1’ for T_{STROBE} duration on eD+ indicating EOReset.
  - It shall disable its transmitter and maintain SE0 with its R_{PD} upon completing EOReset and enable its HS transceivers and squelch detectors at its eUSB port.

5.3.3.3.2 Exit from Reset.EOR

The repeater and the eDSPr shall enter L0 upon completing the EOReset transmission.

Note: It shall determine and keep the established HS, FS, or LS link speed based on the Connect and Reset handshake for subsequent L0 HS or FS/LS data forwarding, line mapping, Lx entry, and disconnect detection operations.

5.3.4 **L0**

L0 is a state where the repeater forwards packets between eUSB2 and USB2.0. L0 contains three substates as shown in Figure 5-8.

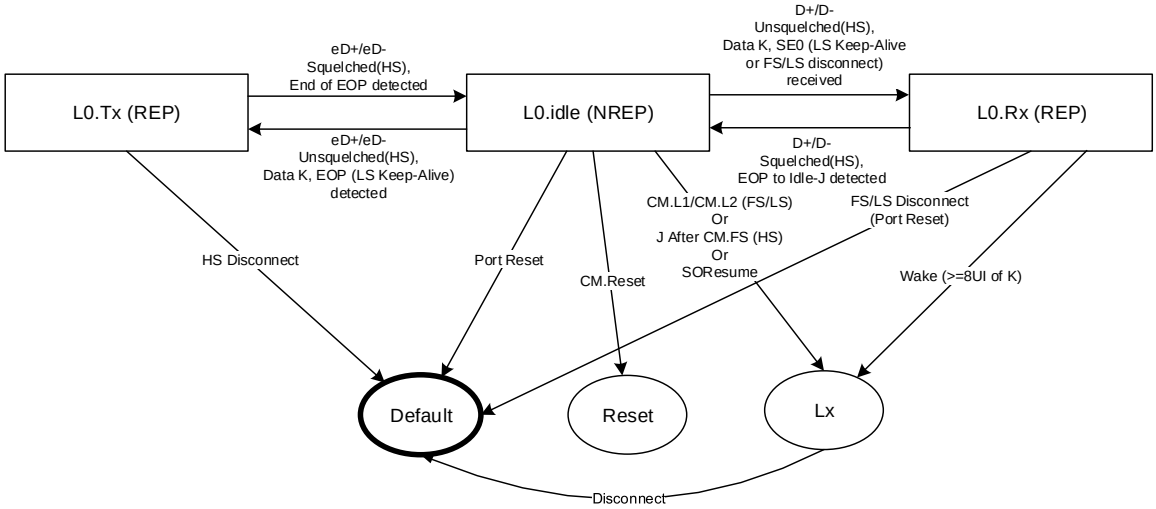


Figure 5-8: L0 Substate Machine

5.3.4.1 L0.Idle

L0.Idle is a substate where the link is idle. The repeater transitions from this substate to L0.Tx/L0.Rx based on the incoming signals from eUSPh and UDSP. If it's SE1, it remains in this substate and determines if it's SCM or ESE1. If it's non SE1, it implies an incoming packet, resume or remote wake (in the FS/LS case where the repeater stays in L0, but the link is in Lx) that needs to be forwarded.

5.3.4.1.1 L0.Idle Requirements

The repeater shall meet the following conditions:

- Its UDSP shall meet the condition defined by USB2.0.
- The eUSPh shall meet the following requirements:
  - It shall enable its SE receivers at eD+/eD-.
  - It shall enable its SE1 detector for CM.Reset, CM.L1, CM.L2, CM.FS, Port Reset, or SOResume. Note: Scenario could exist where eDSPr may not transmit CM.Lx to the repeater. In this event, the repeater would remain in L0.Idle while eDSPr is in Lx. Other than a potential minor power impact, link shall remain operational and repeater in L0 shall be able to distinguish between an incoming eUSB2 packet, or USB2.0 packet and a resume or wake. For wake, it may implement a timer to differentiate wake event from data packet (maximum length of 8 UI running K). And in the event where a wake without host resume occurs in L0, the repeater shall transition to Lx upon declaring the EOWake. Note that SOResume is a SE1 condition which the repeater can identify without a timer.
  - If HS, it shall enable its squelch detectors on eUSPh and on UDSP.
  - Upon receiving CM.FS in high-speed operation, the repeater shall perform the following:
    - It shall switch to NREP mode.
    - It shall reconfigure to FS termination.
  - If CM.Test is received, it shall enable it HS termination for HS Compliance Test. Note: Exiting a Compliance Test condition may be a power cycle or Port Reset depending on Implementation.

The eDSPr shall meet the following conditions:

- It shall enable its SE receivers at eD+/eD-.
- It shall enable its SE1 detector in HS operation for Port Reset detection.
- If HS, it shall enable its squelch detector.
- If CM.Test is transmitted, it shall enable it HS termination for HS Compliance Test.

Implementation note:
Due to intra-pair skew defined as T_{SE1_SKEW} in Table 7-16 between eD+ and eD-, a SE1, upon reaching the eDSPr/eUSPh, may be distorted, as shown Figure 5-9.

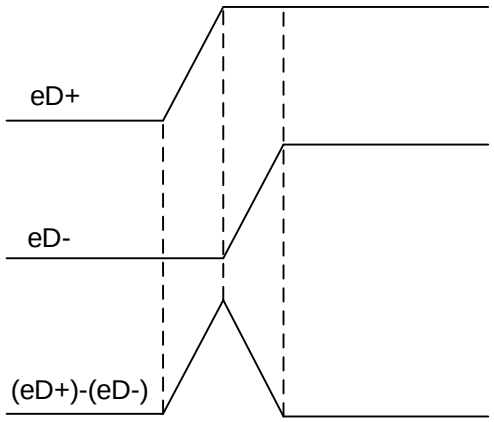


Figure 5-9: SCM Distortion Observed by eUSB2 Repeater

This distortion may exhibit one of the following false conditions to the eUSB2 repeater:

1. If the rising edge of eD+ precedes the rising edge of eD-, it may initially present itself as the first bit of SYNC in LS operation.
2. If the rising edge of eD- precedes the rising edge of eD+, it may present itself as the first bit of SYNC in FS operation, or a LS keep-alive in LS operation.
3. If either of the above two mentioned conditions occur during HS operation (L0.Idle), it may present itself as a HS K or J that may lead to HS squelch detector exiting from squelched condition.

It is highly recommended for an implementation to apply proper filtering mechanisms to avoid unintended action to those false conditions. Some possible mechanisms include, but are not limited to the following:

1. For FS/LS operation it shall adhere to USB2.0 FS/LS hub repeater timing, with the exception of next transition jitter from eUSB2 to USB 2.0 and paired transition in both directions. The jitter to next transition follows eUSB2 parameter $T_{e\_to\_U\_DJ1}$, instead of the corresponding USB 2.0 parameter T_{HDJ1}. T_{HDJ1} still applies to USB 2.0 to eUSB2. The jitter to paired transition follows eUSB2 parameter T_{DJ2}, instead of the corresponding USB 2.0 parameter T_{HDJ2}.
2. For HS operation, reduce the squelch detector sensitivity to not respond to the short pulse, and have the SE1 detector disable squelch detector upon declaring SE1 detection.

The eUSB2 channel construction shall meet the requirements defined in Table 7-6 (Electrical).

5.3.4.1.2 Exit from L0.Idle

The repeater shall perform the following tasks:

- It shall transition to L0.Tx if an un-squelched condition (HS) or idle J (LS/FS) to K (logic '1' at eD- for FS or eD+ for LS) or EOP (LS Keep-Alive) transition is detected at eD+/eD-.
- It shall transition to L0.Rx if an un-squelched condition (HS) or an idle J to K or SE0 (LS Keep-Alive) transition is detected at D+/D-.
- It shall transition to Lx if CM.L1/CM.L2/SOResume (Lx.Resume) is received at eD+/eD-.
- It shall transition to FS (Note: this is a transitional state in which the HS link shall eventually enter Lx when a J is detected at UDSP) if CM.FS is received for a HS link operation.
- It shall transition to Reset if CM.Reset is received at eD+/eD-.
- It shall transition to Default if one of the following conditions is met:
  - Port Reset is received.
  - A device (in FS/LS operation) disconnect announcement (Port Reset) is received from eDSPr upon detecting a USB2.0 device disconnect. Section 5.5.4 illustrates the timing flow of detecting FS disconnect and reconnecting.

The eDSPr shall perform the following tasks:

- It shall transition to L0.Tx if directed by its host to transmit data packet.
- It shall transition to L0.Rx if an un-squelched condition (HS) or an idle J to K transition at eD- (FS) or eD+ (LS) is detected.
- In FS/LS mode, it shall transition to Lx once completing CM.L1/CM.L2 to its repeater, if directed by its host through UTMI+ interface to perform a Lx entry.
- In HS mode, it shall transition to FS (Note: this is a transitional state in which the HS link shall eventually enter Lx if a pulse is detected within $T_{PR\_HS\_RESET\_TO\_FS}$ at eDSPr) once completing CM.FS to its repeater, if directed by its host through UTMI+ interface to enter FS mode. Note that the eUSB link between eDSPr and eUSPh shall not be fully transition to FS until the peripheral transition to FS and T_{STROBE} is driven out from eUSPh to eDSPr.
- It shall transition to Reset once completing CM.Reset if directed by its host through UTMI+ interface to perform a bus reset.
- If in FS mode, it shall transition to Default and transmit Port Reset to eUSPh if a logic '1' on eD+ (FS mapping as SE0 on D+/D-) is received and qualified as device disconnect.
- If in LS mode, it shall transition to Default and transmit Port Reset to eUSPh if a logic '1' on eD- (LS mapping as SE0 on D+/D-) is received and qualified as device disconnect.
- If in HS mode, it shall transition to Default if a device disconnect announcement is received. The eDSPr shall not respond with Port Reset to repeater's device disconnect announcement.

5.3.4.2 L0.Rx

L0.Rx is a substate where a USB packet is received and forwarded from the UDSP to the eUSPh.

5.3.4.2.1 L0.Rx Requirements

The repeater shall meet the following conditions:

- It shall operate at REP mode.
- In HS operation, it shall forward the USB packets upon detection of the un-squelched condition at the UDSP. Note: The repeater can consume 4 SYNC bits on the exit from Squelch. While forwarding USB packets from UDSP to eUSPh, the repeater may transmit the 1st bit (within the 4 allowable SYNC bits that a repeater can consume) of the SYNC pattern with random UI duration and add EOP dribble up to 4 random (SE0 or K or J) bit duration.
- In FS/LS operation, it shall perform packet forwarding based on FS mapping described in Section 3.3.1 upon detection of K (including Wake) or SE0 (LS Keep-Alive or FS/LS disconnect) condition at the UDSP.

The eDSPr shall meet the following conditions:

- In HS operation, it shall receive differential data packets from eUSPh.
- In HS operation, it shall filter squelch for up to 4 UI to ignore SE0 from the repeater during EOP dribble.
- In FS/LS operation, it shall receive SE data packets or SE0 (LS Keep-Alive) from eUSPh.

5.3.4.2.2 Exit from L0.Rx

The repeater shall perform the following tasks:

- In HS operation, it shall transition to L0.Idle upon completion of the packet forwarding, detecting a squelched condition at UDSP.
- In FS/LS operation shall transition to L0.Idle upon completing the packet forwarding, including EOP, and detecting an idle J condition at UDSP. If forwarding SE0 (LS Keep-Alive), it will do so until it detects an idle J at UDSP.
- Note: Scenario could exist where eDSPr may not transmit CM.Lx to the repeater. In this event, the eDSPr is in Lx while the repeater would remain in L0.Idle. Other than a potential minor power impact, link shall remain operational and repeater in L0.Rx shall be able to distinguish between an incoming eUSB2 packet, or USB2 packet and wake, for which it may implement a timer to differentiate wake event from data packet (maximum length of 8 UI running K) and transition to Lx (Lx.Wake).
- In FS/LS operation, it shall transition to Default if Port Reset (disconnect) is detected from eDSPr.

The eDSPr shall perform the following tasks:

- In HS operation, it shall transition to L0.Idle upon detecting a squelched condition.
- In FS operation, it shall transition to L0.Idle upon detecting an EOP (at least 1 FS UI of logic ‘1’ at eD+ followed by a SE0).
- In LS operation, it shall transition to L0.Idle upon detecting an EOP (at least 1 LS UI of logic ‘1’ at eD- followed by a SE0).

5.3.4.3 L0.Tx

L0.Tx is a substate where a USB packet is received and forwarded from the eUSPh to the UDSP.

5.3.4.3.1 L0.Tx Requirements

The repeater shall meet the following conditions:

- It shall operate in REP mode.
- In FS operation, it shall forward packet based on FS mapping described in Section 3.3.1 upon detection of logic ‘1’ condition (idle J to K) at eD- from eDSPr.
- In LS operation, it shall forward packet based on LS mapping described in Section 3.3.1 upon detection of logic ‘1’ condition (idle J to K) at eD+ from eDSPr.
- Also, in LS operation, it shall forward LS Keep-Alive, which is a LS EOP, on UDSP as described in Section 3.3.1.
- In HS operation, it shall forward the USB packets upon detection of the un-squelched condition at the eUSPh. Note: The repeater can consume 4 SYNC bits on the exit from Squelch. While forwarding USB packets from eUSPh to UDSP, the repeater may transmit the 1st bit (within the 4 allowable SYNC bits that a repeater can consume) of the SYNC pattern with random UI duration and add EOP dribble up to 4 random (K or J) bit duration.
- In HS operation, it shall enable its high-speed disconnect detector at UDSP and shall adhere to T_{DISC_DLY} in announcing HS disconnect to its associated eDSPr. Refer to Section 5.5.7 that describes the timing flow of host repeater and its associated eDSPr detecting device disconnect in HS link.

Implementation note:

High-speed disconnect detect in L0 is performed by a downstream port during EOP of uSOF. It is the responsibility of the repeater to identify the EOP of an uSOF. A repeater may implement a digital filter based on its local clock to detect the EOP of an uSOF, and subsequently control the operation of the high-speed disconnect detector. A repeater may sample the disconnect detector output upon detection of the squelched condition at eUSPh.

The eDSPr shall meet the following conditions:

- In HS operation, it shall transmit differential data packets to eUSPh.
- In FS operation, it shall transmit SE data packets to eUSPh on eD- follow by an EOP as described in Section 3.3.1 on eD+.
- In LS operation, it shall be transmitting SE data packets to eUSPh on eD+ follow by an EOP as described in Section 3.3.1 on eD-.

5.3.4.3.2 Exit from L0.Tx

The repeater shall perform the following tasks:

- The repeater shall transition to L0.Idle if the following conditions are met:
  - It has completed the transmission of the USB packet at its UDSP.
  - It has detected squelched condition at its eUSPh, if it is in HS operation.
  - It has detected EOP as described in Section 3.3.1 on eD+ at its eUSPh, if it is in FS operation.
  - It has detected EOP as described in Section 3.3.1 on eD- at its eUSPh, if it is in LS operation.
- In HS operation, it shall transition to Default if a device disconnect announcement is sent to the eDSPr upon detecting USB2.0 device disconnect.

The eDSPr shall perform the following tasks:

- It shall transition to L0.Idle if it has completed the transmission of the USB packet.
- In HS operation, it shall declare device disconnect as defined by T_{HSDISC_SE1} and transition to Default if a device disconnect announcement is received from the eUSPh. Note that eDSPr is not recommended to transmit Port Reset after receiving eUSPh device disconnect announcement.

5.3.5 **Lx**

Lx is a state where the repeater is in power saving mode, depending on whether it was entered due to receiving CM.Lx or CM.FS or detecting remote wake on UDSP that was not resumed. Only CM.Lx receipt would necessarily put it into a power saving mode. The repeater power management may be different between L1 and L2 depending on implementation. Section 5.5.12, 5.5.13 shows the timing sequence of the FS L1 and L2 entry, while Section 5.5.18 shows the L2 entry of a HS link. Additionally, Section 5.5.20, 5.5.21, and 5.5.22 illustrate device disconnect detection during Lx entry. The Lx substate machine is shown in Figure 5-10.

- The repeater shall be in NREP mode. Note: As described in Section 5.3.4.1.2 where the repeater in LS/FS operation may stay in L0 (although the link is in Lx), which is in REP mode.

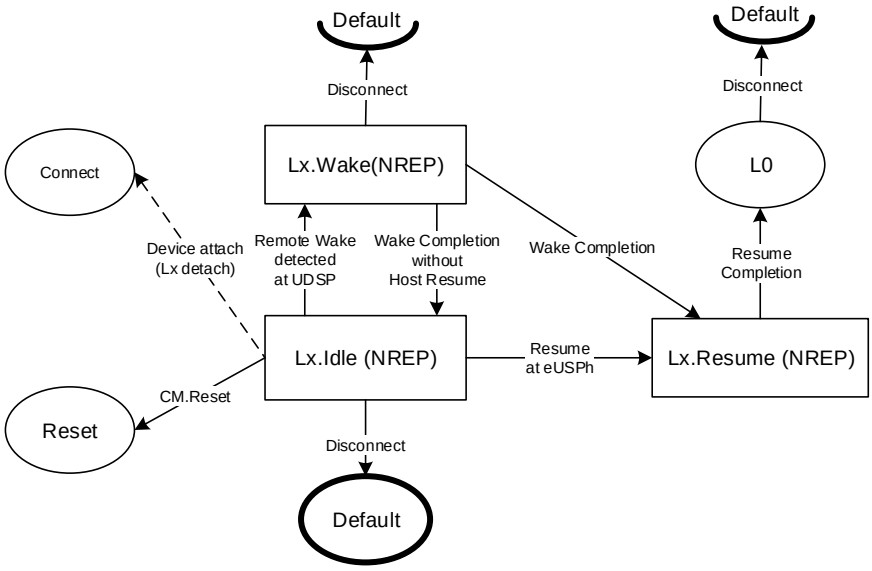


Figure 5-10: Lx Substate Machine

5.3.5.1 Lx.Idle

Lx.Idle is a substate where the repeater is in logical low power idle state.

5.3.5.1.1 Lx.Idle Requirements

The repeater shall meet the following conditions:

- It shall enable its SE receivers at eD+/eD- in expectation of SE1.
- It shall disable its high-speed transceivers.
- The UDSP shall meet the requirements defined by USB2.0.

The eDSPr shall meet the following conditions:

- It shall enable its SE receivers at eD+/eD- in expectation of remote-wake or device disconnect. Note: Scenario could exist where eDSPr may not transmit CM.Lx to the repeater. In this event, the eDSPr is in Lx while the repeater would remain in L0.Idle. Other than a potential minor power impact, link shall remain operational and repeater in L0 shall be able to distinguish between an incoming eUSB2 packet, or USB2 packet and a resume or wake, for which it may implement a timer to differentiate resume/wake event from data packet (maximum length of 8 UI running K).
- It shall disable its high-speed transceivers.

5.3.5.1.2 Exit from Lx.Idle

The repeater shall perform the following tasks:

- It shall transition to Lx.Resume if it has detected resume at eUSPh.
- It shall enter Lx.Wake if it has detected remote wake at UDSP.
- It shall transition to Reset if it has received CM.Reset.
- Note: In the unlikely event where both Reset and Wake occur concurrently a link error condition may occur. eDSPr may issue Port Reset as an attempt to recover from the error condition.
- It shall transition to Default if a device disconnect announcement (Port Reset) is detected. Note that the eDSPr declares USB2.0 device disconnect based on repeater mapping linestate from UDSP to eUSPh.

The eDSPr shall perform the following tasks:

- It shall transition to Lx.Resume if directed by it host on the UTMI+ to perform resume.
- It shall enter Lx.Wake if it has detected remote wake from the eUSPh.
- It shall transition to CM.Reset if directed by it host on the UTMI+ to perform bus reset.
- In FS Lx, it shall transmit Port Reset and transition to Default if a logic ‘1’ is detected on eD+ and qualified as a device disconnect. Note that the eDSPr declares USB2.0 device disconnect based on repeater mapping linestate from UDSP to eUSPh.
- In LS Lx, it shall transmit Port Reset and transition to Default if a logic ‘1’ is detected on eD- and qualified as a device disconnect. Note that the eDSPr declares USB2.0 device disconnect based on repeater mapping linestate from UDSP to eUSPh.

Note: Although implementation specific, given the likely window where role swap occurs during Lx, eDSPr shall transmit Port Reset and transition to Default in the event of role swapping where the UTMI+ interface changed from host to peripheral mode. This is then followed by a Repeater Configuration to reconfigure the repeater to peripheral mode operation.

5.3.5.2 Lx.Resume

Lx.Resume is a substate where the host starts exiting from L1 or L2. Sections 5.5.12 and 5.5.13 show the timing sequence of the FS resume from L1 and L2, while Section 5.5.17 shows the resume to back to HS.

5.3.5.2.1 Lx.Resume Requirements

The repeater shall meet the following conditions:

- It shall monitor the eUSBh resume until its completion.
- It drives the resume signal at its UDSP defined by USB2.0 while the eUSB2 resume signal is asserted.
- It shall end resume at its UDSP upon detecting EOResume at its eUSPh. Refer to Section 3.3.5 for EOP transmission.

The eDSPr shall meet the following conditions:

- In FS/LS Lx, it shall drive resume as defined in Section 3.3.5.1.2 to its eUSPh when directed by its controller.

5.3.5.2.2 Exit from Lx.Resume

The repeater shall perform the following tasks:

- It shall enter L0.Idle upon detecting EOResume from its eDSPr and complete resume signaling on UDSP.

The eDSPr shall perform the following tasks:

- Resuming to FS/LS, it shall transition to L0.Idle upon completing EOResume as defined in Section 3.3.5.1.2 to its repeater.
- Resuming to HS, it shall transition to L0.Idle upon completing EOResume as defined in Section 3.3.5.2.2 to its repeater.

5.3.5.3 Lx.Wake

Lx.Wake is a substate where a USB2.0 device initiates remote wake to resume the USB2.0 operation. Section 5.5.12 and 5.5.18 shows the timing waveform of L2 wake to FS and HS respectively. Additionally, Section 5.5.16 and 5.5.19 provides timing sequences of a FS and HS wake from L2 without the host resume being triggered.

5.3.5.3.1 Lx.Wake Requirements

The repeater shall meet the following conditions:

- It shall follow the eUSB2 remote wake protocol as shown in Sections 5.5.12 and 5.5.18.
- The UDSP shall perform the remote wake from L2 as defined by USB2.0. The repeater shall do the following:
    - Upon detecting remote wake at its UDSP, it shall drive remote wake at its eUSPh. Note: Delay in repeater forwarding remote wake shall meet related USB2.0 hub timing parameters.
    - It shall drive the resume signal at its UDSP upon detecting the start of host resume at eUSPh until its conclusion.
    - It shall conclude the eUSB2 remote wake signal upon detection of eUSB2 resume signal.
- The UDSP shall perform the remote wake from L1 as defined by USB2.0 Link Power Management Addendum. The repeater shall do the following:
    - Upon detecting remote wake at its UDSP, the repeater shall drive the eUSB2 remote wake at its eUSPh.
    - The repeater shall drive the resume signal at its UDSP upon detecting the start of host resume at eUSPh until its conclusion.
    - The repeater shall conclude the eUSB2 remote wake signal upon detection of eUSB2 resume signal.

The eDSPr shall meet the following conditions:

- It shall reflect remote wake received at eD+/eD- to its UTMI+ interface.
- It shall drive resume signal as defined in Section 3.3.5 when directed by its host through the UTMI+ interface.

5.3.5.3.2 Exit from Lx.Wake

The repeater shall perform the following tasks:

- It shall enter Lx.Resume upon detecting SOResume at its eUSPh. Note: A successful remote wake shall follow with resume. The repeater shall transition to Lx if resume K is not detected.
- In an unlikely error event that no host resume is observed, it shall stop driving logic '1' on eD- and conclude wake with logic '0' on eD- for $T_{SE0\_DR\_LSFS}$.
- It shall transition to Default if Port Reset is received on eUSPh.
    - The repeater shall transmit logic '1' on eD+ for FS or eD- for LS if SE0 is presented on UDSP in the event of a device disconnect during wake (UDSP transitions from K to SE0), which results in Port Reset from eDSPr.

The eDSPr shall perform the following tasks:

- Resuming to FS/LS, it shall transition to Lx.Resume as directed as defined in Section 3.3.5.1.2. Note: A successful remote wake shall follow with resume.

- Resuming to HS, it shall transition to L0.Idle upon completing EOResume as defined in Section 3.3.5.2.2. Note: A successful remote wake shall follow with resume.
- It shall transition to Default and transmit Port Reset upon detecting a device disconnect during wake (i.e. a logic '1' on eD+ for FS Lx indicating a SE0 condition at UDSP).

5.4 *Peripheral Repeater Operation*

This section describes basic operations of an eUSB2 peripheral repeater associated with an eUSPr. The state machine of an eUSB2 repeater in peripheral mode is like host mode but with different transition conditions. The peripheral mode repeater state machine is shown in Figure 5-11.

Note: eUSPr implementation may not have the exact states or state transitions as the repeater. Below diagrams and description serve as an informative guide to eUSPr implementation.

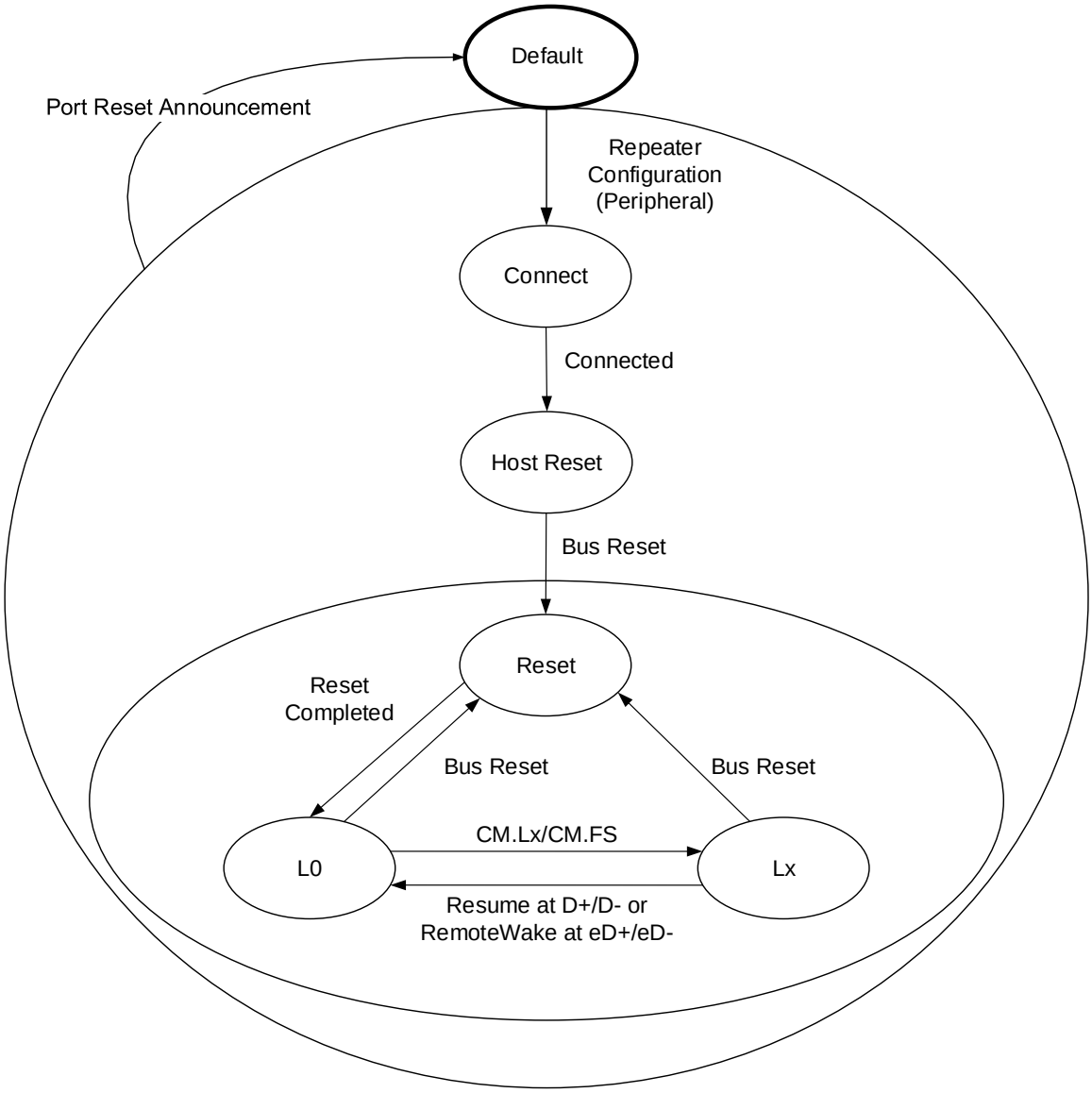


Figure 5-11: Peripheral Mode eUSB2 State Machine

5.4.1 Connect

Connect is a state where a peripheral repeater is ready for device connect directed by its eUSPr. Section 5.5.2 illustrates a peripheral repeater link initiating a FS connection upon POR. Section 5.5.4 show a peripheral repeater connecting to a host and establishing a HS link upon POR.

Connect contains two substates shown in Figure 5-12.

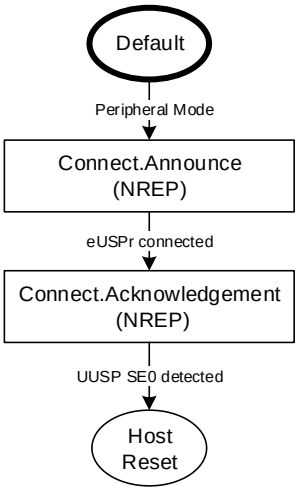


Figure 5-12: Connect Substate Machine

5.4.1.1 Connect.Announce

Connect.Announce is a substate where the eDSPp is expecting device connect from eUSPr.

5.4.1.1.1 Connect.Announce Requirements

The repeater shall meet the following conditions:

- The eDSPp of the peripheral repeater shall meet the following conditions:
  - It shall enable its R_{PD} to maintain SE0 at eUSB2 bus.
  - It shall enable its SE receivers.
- The UUSP of the peripheral repeater shall have its transceivers disabled.
- The repeater should be in the lowest power state monitoring for eUSPr connect.

The eUSPr shall meet the following conditions:

- It shall enable its R_{PD} at both eD+ and eD-.
- It shall, when directed by its device controller, drive logic ‘1’ at eD+ to instruct its repeater to pull-up at D+.
- It shall, when directed by its device controller, drive logic ‘1’ at eD- to instruct its repeater to pull-up at D-.

5.4.1.1.2 Exit from Connect.Announce

The repeater shall transition to Connect.Acknwledge if one of the following conditions is met:

- It has enabled FS transceiver at UUSP and pull-up at D+ upon detecting logic ‘1’ at eD+ for FS/HS operation.
- It has enabled LS transceiver at UUSP and pull-up at D- upon detecting logic ‘1’ at eD- for LS operation.

5.4.1.2 Connect.Acknowledge

Connect.Acknowledge is a substate where the repeater is relaying device connect from its eDSPp to UUSP, and acknowledging the connect completion to eUSPr.

5.4.1.2.1 Connect.Acknowledge Requirements

The repeater shall meet the following conditions:

- It shall acknowledge the connect completion to eUSPr by performing the following.
  - It shall drive logic ‘1’ at eD-, upon completing the FS transceiver configuration at UUSP with D+ pull-up and after having observed logic ‘1’ at D+ that is a result of the pull-up.
  - It shall drive logic ‘1’ at eD+, upon completing the LS transceiver configuration at UUSP with D- pull-up and after having observed logic ‘1’ at D- that is a result of the pull-up.
- It shall complete the connect acknowledgement to eUSPr by performing the following.
  - It shall drive and maintain logic ‘0’ at eD-, upon detecting logic ‘0’ at eD+ indicating eUSPr concluding the connect announcement. Note that the repeater shall maintain the FS transceiver configuration at UUSP with D+ pull-up throughout this substate.
  - It shall drive and maintain logic ‘0’ at eD+, upon detecting logic ‘0’ at eD- indicating eUSPr concluding the connect announcement. Note that the repeater shall maintain the LS transceiver configuration at UUSP with D- pull-up throughout this substate.

The eUSPr shall meet the following conditions:

- It shall conclude the connect announcement by performing the following.
  - It shall drive logic ‘0’ at eD+ if it has detected the connect acknowledgment at eD- from the repeater and disable its SE transmitter.
  - It shall drive logic ‘0’ at eD- if it has detected the connect acknowledgment at eD+ from the repeater and disable its SE transmitter.
- It shall monitor the conclusion of the connect acknowledgement from the repeater.

5.4.1.2.2 Exit from Connect.Acknowledge

The repeater shall transition to Host Reset upon completing the connect acknowledgement. Refer to Section 5.5.2 timing diagram for details of the operation.

The eUSPr shall transition to Host Reset upon concluding the connect announcement. Refer to Section 5.5.2 timing diagram for details of the operation.

Note: Repeater’s Linestate mapping is applicable only after establishing a connection (exiting Connect.Acknowledge and entering Host Reset).

5.4.2 **Host Reset**

In the Host Reset state, the repeater monitors its UUSP for SE0 indicating USB2.0 bus reset. Sections 5.5.2, 5.5.3 and 5.5.4 describe the reset flow in a LS, FS and HS new connection respectively.

Note: The peripheral repeater is not required to perform debounce or de-glitching of the USB2.0 lines in any of its states.

5.4.2.1 Host Reset Requirements

The repeater shall meet the following conditions:

- It shall monitor its linestate at UUSP and eDSPp. Note that the repeater shall not sample D+/D- until D+ (FS/HS) or D- (LS) is pulled-up.

It shall perform the linestate mapping based on LF/FS operation as defined in

- Table 3-1. Refer to Section 5.5.8 for FS link reset timing diagram.

The eUSPr shall meet the following conditions:
It shall perform the linestate mapping based on LF/FS operation as defined in

Table 3-1.

5.4.2.2 Exit from Host Reset

The repeater shall transition to Reset upon SE0 detection at UUSP.

The eUSPr transition to Reset upon detecting a logic ‘1’ at eD+/eD- (for FS/LS respectively) or SE0 at eD+/eD- for HS (not observing a pulse/acknowledge on eD+).

5.4.3 **Reset**

Reset is a state where host port performs the USB2.0 bus reset and speed detection. Reset contains multiple substates as shown in Figure 5-13.

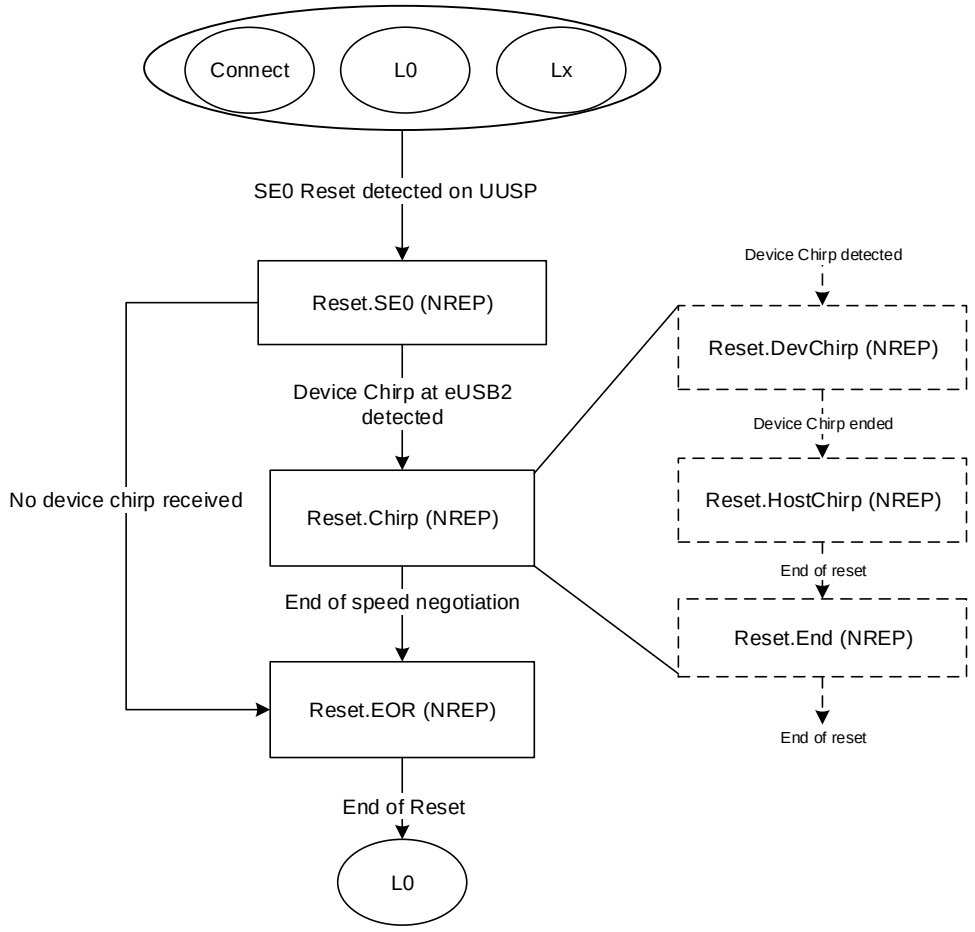


Figure 5-13: Reset Substate Machine

5.4.3.1 Reset.SE0

Reset.SE0 is a substate where the repeater performs a USB2.0 bus reset and prepares for speed negotiation.

5.4.3.1.1 Reset.SE0 Requirements

The eDSPp of the repeater shall meet the following conditions:

- It shall keep its R_{PD} at eD+/eD-.
- It shall enable its SE receivers.
- If entry to Reset is from HS L0 idle, and the linestate at UUSP remains SE0 after the repeater has configured its transceiver to FS at UUSP, It shall maintain SE0 (not pulse/acknowledge on eD+) at eD+/eD- with R_{PD}, in preparation for Reset.Chirp or Reset.EOR (in the event that a previously established HS link decided to downgrade in which either device chirp or host K-J chirp is not transmitted, the eDSPp shall transmit EOReset upon observing a SE0 to J transition on UUSP.). Refer to Section 5.5.8, 5.5.9, 5.5.10 and 5.5.11 for details timing diagram.
- If entry to Reset is from FS/LS Connect, L0 or Lx, it shall continue the linestate mapping from UUSP to eDSPp based on LS/FS linestate mapping defined in

- Table 3-1. Note that a repeater may not receive CM.FS or CM.L2 from eUSPr even when the link is in L1 or L2. Under this situation, a repeater will remain in L0. It may implement a timer to differentiate and track the USB2 bus reset SE0 from data packet SE0 to stay in-sync with eUSPr. Refer to Section 5.5.8 for Bus Reset during FS Link.

The eUSPr shall meet the following conditions:
In a FS/LS link, it shall perform the linestate mapping based on LF/FS operation as defined in

- Table 3-1.
- In an established HS link, it shall expect SE0 (not observing a pulse/acknowledge on eD+) for $T_{PR\_HS\_RESET\_TO\_FS}$ indicating USB2.0 bus reset (Note: eDSPp shall transmit a pulse/acknowledge on eD+ within $T_{PR\_HS\_RESET\_TO\_FS}$ for a Lx entry). Refer to Section 5.5.9 for timing diagram.

5.4.3.1.2 Exit from Reset.SE0

The repeater shall perform the following tasks:

- It shall transition to Reset.Chirp if device chirp is detected at its eDSPp.
- It shall transition to Reset.EOR if it has detected data J at its UUSP.

The eUSPr shall perform the following tasks:

- It shall transition to Reset.Chirp and transmit a logic '1' on eD- when directed to start HS negotiation.
- It shall transition to Reset.EOR if it has detected a logic '1' on eD+ as EOReset for a FS link.
- It shall transition to Reset.EOR if it has detected a logic '1' on eD- as EOReset for a LS link.

5.4.3.2 Reset.Chirp

Reset.Chirp is a substate where a high-speed eUSB2 device is connected, and the speed negotiation is performed. Section 5.5.4 shows the timing waveform of the reset chirp sequence. There are multiple stages of operation within Reset.Chirp to complete the speed negotiation, as shown in Figure 5-13.

5.4.3.2.1 Reset.Chirp Requirements

The repeater shall meet the following conditions:

- The eDSPp of the repeater shall be ready for speed negotiation by having its SE receivers enabled.
- The USB2.0 port shall enable its HS transceiver to forward device chirp K and host K-J chirp acknowledgment.
- It shall stop transmitting logic '1' on eD+ to conclude SE0 linestate mapping from UUSP to eDSPp upon detecting device chirp at eD-.
- It shall forward the eUSB2 device chirp based on the following:
    - It shall drive a chirp K at UUSP if eD- is logic '1'.
    - It shall conclude chirp K at UUSP if eD- is logic '0'.
  - It shall perform the following to forward the K-J chirps from the host:
    - It shall drive logic '1' at eD- if it has detected a Chirp K at D+/D-.
    - It shall drive logic '0' at eD- if it has detected a Chirp J at D+/D-.
  - In the event where the device started HS negotiation, but Host does not perform chirp K-J (e.g. a FS capable only or downgraded HS Host), the peripheral repeater shall differentiate (implementation specific) them through the reset sequences and enter Reset.EOR accordingly. Refer to Section 5.5.10 for Bus Reset of a FS Host timing diagram.
  - It shall enable its HS receiver termination at UUSP if it has detected a pulse at eD+. Note that this is a pulse sent by an eUSPr to inform the peripheral repeater to turn on its HS device termination at UUSP.
  - If SE0 (Note: This shall be the first SE0 condition after Host Chirp K-J; The repeater shall distinguish this Reset.EOR with the SE0 in between Device and Host Chirp) is detected at D+/D-, it shall conclude speed negotiation by performing Reset.EOR as described in Section 3.3.4.
  - Upon completion of high-speed negotiation, the repeater shall be ready for HS operation.

The eUSPr shall meet the following conditions:

- It shall transmit logic ‘1’ on eD- as directed by its device controller for device chirp.
- It shall return the eUSB line to SE0 by driving logic ‘0’ at eD- for $T_{SE0\_DR\_LSFS}$ before disabling its TX (SE0 maintains by R_{PD}) upon completion of device chirp.
- It shall map logic ‘1’ and logic ‘0’ toggling lineate D- as the host K-J chirp respectively and reflect these to its UTMI+ interface to the device controller. Note: The eUSPr may observe continuous SE0 if the host doesn’t transmit chirp. Refer to Section 5.5.10 for Bus Reset of a FS Host timing diagram.
- In the event where the device started HS negotiation, but Host does not perform chirp K-J (e.g. a FS capable only or downgraded HS Host), it shall transition to Reset.EOR upon detecting a logic ‘1’ at eD+ as EOReset. Refer to Section 5.5.10 for Bus Reset of a FS Host timing diagram.
- It shall pulse eD+ as directed by its device controller to instruct the repeater to enable HS termination. Refer to Section 5.5.4 for timing diagram.

5.4.3.2.2 Exit from Reset.Chirp

The repeater shall perform the following tasks:

- It shall transition to Reset.EOR if SE0 is detected at UUSP.

The eUSPr shall perform the following tasks:

- It shall transition to Reset.EOR if a logic ‘1’ is observed at eD+ as EOReset for HS.

5.4.3.3 Reset.EOR

Reset.EOR is a substate where the USB2.0 bus reset is concluded. Reset.EOR does not contain any substate.

5.4.3.3.1 Reset.EOR Requirement

The repeater shall meet the following conditions:

- The repeater in LS/FS operation shall stop transmitting logic ‘1’ at eD-/eD+ to end reset.
- If it’s HS operation, the repeater shall meet the following conditions:
  - It shall drive logic ‘1’ at eD+ for T_{STROBE} to conclude speed negotiation and USB2.0 bus reset, upon SE0 detection at UUSP.
  - It shall enable its HS transceivers and squelch detectors at its eUSPh and UDSP upon detecting the falling edge of eD+.
  - In the event where the device started HS negotiation, but Host does not perform chirp K-J (e.g. a FS capable only or downgraded HS Host) in which the link return to an idle J condition at UUSP, the peripheral repeater shall differentiate (implementation specific) them through the reset sequences and transmit FS Reset.EOR for T_{STROBE} accordingly. Refer to Section 5.5.10 for Bus Reset of a FS Host timing diagram.
- It shall enter L0 upon completion of EOReset transmission.

The eUSPr shall meet the following conditions:

- It shall reflect a logic ‘1’ on eD+ to the UTMI+ as an EOReset and L0 entry for FS and HS.
- It shall reflect a logic ‘1’ on eD- to the UTMI+ as an EOReset and L0 entry for LS.

5.4.3.3.2 Exit from Reset.EOR

- The repeater and eUSPr shall transition to L0 upon completion of the EOReset transmission at eUSB2 port.

Note: The repeater shall determine and keep the established HS, FS, or LS link state based on the Connect and Reset handshake for subsequent L0 HS or FS/LS data forwarding, linestate mapping, and Lx entry.

5.4.4 **L0**

L0 is a state where the repeater is forwarding the USB packets between eDSPp and UUSP. Note that in peripheral mode, L0.Tx refers to packets forwarding from UUSP to eDSPp, and L0.Rx refers to packets forwarding from eDSPp to UUSP.
L0 contains three substates as shown in **Error! Reference source not found.**.

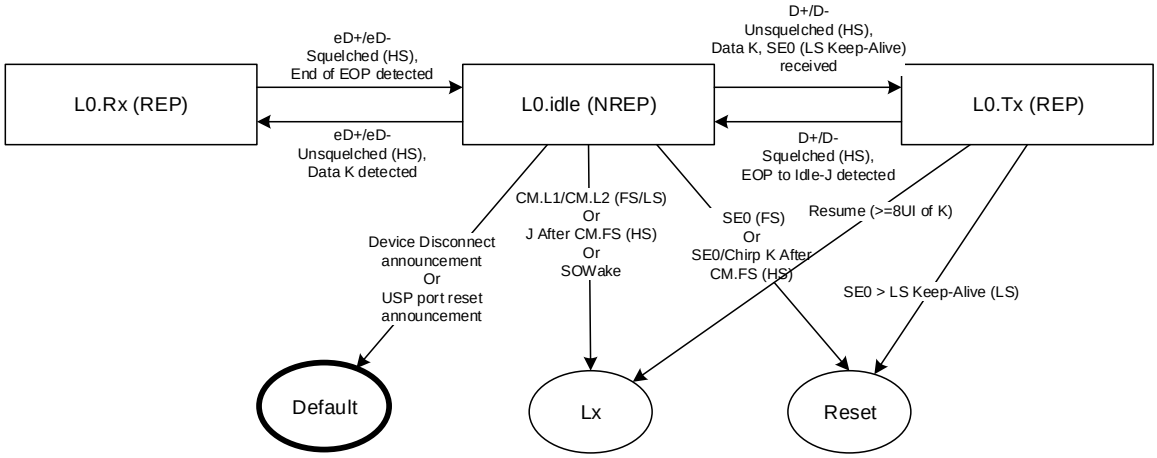


Figure 5-14: L0 Substate Machine

5.4.4.1 L0.Idle

L0.Idle is a substate where the link is idle. The repeater transitions from this substate to L0.Tx/L0.Rx based on the incoming signals from eUSB2 bus and USB2.0 bus. If it's SCM, it remains in this substate. If it's non SCM, it implies an incoming packet, resume or remote wake (in the FS/LS case where the repeater stays in L0, but the link is in Lx) that needs to be forwarded.
A repeater is in peripheral mode will only receive SCM from an eUSB2 peripheral device to return to FS termination from HS for Lx entry.

5.4.4.1.1 L0.Idle Requirements

The repeater shall perform the following tasks:

- The UUSP shall meet the requirements defined by USB2.0.
- The eDSPp of the repeater shall meet the following requirements:
  - It shall enable its SE0 receivers at eD+/eD-.
  - It shall enable its SE1 detector for Port Reset or SOWake.
  - If HS, it shall enable its squelch detector on both sides.
- Upon receiving CM.FS in high-speed operation, the repeater shall perform the following:
  - It shall switch to NREP mode.
  - It shall reconfigure to FS termination.
  - It shall start a $T_{PR\_HS\_RESET\_TO\_FS}$ timer to differentiate L2 or host reset entry by monitoring the linestate at D+/D-. Refer to Section 5.5.9 and 5.5.17 for timing diagram.
- In LS/FS operation, it shall distinguish between Resume and an incoming packet at UUSP. Note that due to different controller behavior, the repeater may or may not receive CM.FS and CM.L2 from eUSPr, and thus situations exists where the host and device may have entered L1 or L2 and the repeater remains in L0 idle. Under this situation, the repeater shall implement a timer to differentiate between host Resume and a LS/FS

packet while forwarding the signal. Also, the repeater in LS/FS operation shall detect SOWake from eUSPr without a timer. And in the event where a wake without host resume occurs in L0, the repeater shall transition to Lx upon detection of EOWake.

The eUSPr shall meet the following conditions:

- It shall enable its SE0 receivers at eD+/eD-.
- It shall enable its SE1 detector for soft disconnect.
- If HS, it shall enable its squelch detector on both sides.

5.4.4.1.2 Exit from L0.Idle

The repeater shall perform the following tasks:

- It shall transition to L0.Rx if one of the following conditions is met:
  - A high-speed un-squelched condition is detected at eDSPp.
  - A LS/FS data K is detected at eDSPp.
- It shall transition to L0.Tx if one of the following conditions is met:
  - A high-speed un-squelched condition is detected at UUSP.
  - A LS/FS data K (including host Resume) or SE0 (LS Keep-Alive) is detected at UUSP.
- It shall transition to Lx if the following condition is met:
  - In an established HS link upon receiving CM.FS and having completed the following actions:
    - It has removed HS termination, switched to FS (Note that this is a transitional state and repeater shall maintain HS mapping) and observed idle J within $T_{PR\_HS\_RESET\_TO\_FS}$ at its UUSP.
    - It has transmitted a pulse of T_{STROBE} after idle J at its UUSP.
  - In an established FS/LS link upon meeting any one of the following conditions:
    - It has received CM.L1/CM.L2 at eDSPp.
    - It has detected SOWake (transition to Lx.Wake) at eDSPp.
- In HS operation, it shall transition to Reset if CM.FS is received and SE0 at UUSP remains unchanged for $T_{PR\_HS\_RESET\_TO\_FS}$ or a Device Chirp K is detected at the eDSPp after switching to FS. Refer to Section 5.4.3 for details.
- In FS operation, it shall transition to Reset if it has detected SE0 at UUSP. Note: During a mechanical connect event where UUSP may experience toggling, repeater may be transitioning between Reset and L0.Idle.
- In LS operation, it shall transition to L0.Tx if it has detected SE0 (LS Keep-Alive or Reset) at UUSP.

The eUSPr shall perform the following tasks:

- The eUSPr shall transition to L0.Tx if directed by its device controller to transmit data packet.
- The eUSPr shall transition to L0.Rx un-squelched (HS) or logic ‘1’ on eD-/eD+ (FS/LS) condition is detected.
- The eUSPr in FS/LS mode, shall transition to L1/L2 once completing CM.Lx to its repeater, if directed by its controller through UTMI+ interface to perform a Lx entry.
- The eUSPr in HS mode, shall transition to FS after completing CM.FS to its repeater and having received a pulse as an indication of idle J at its repeater’s UUSP, if directed by its controller through UTMI+ interface to enter FS mode.
- The eUSPr in HS mode, shall transition to Reset once completing CM.FS to its repeater and having not received T_{STROBE} wide pulse indicating an idle J condition at its repeater’s UUSP, if directed by its controller through UTMI+ interface to enter FS mode.

5.4.4.2 L0.Tx

L0.Tx is a substate where a USB2.0 packet is received from UUSP and forwarded directly to the eDSPp.

5.4.4.2.1 L0.Tx Requirements

The repeater shall meet the following conditions:

- It shall operate at REP mode.
- It shall forward the USB2.0 packets upon detection of a high-speed un-squelch condition or a LS/FS data K (including host Resume) or SE0 (LS Keep-Alive) at UUSP. Note: The repeater can consume 4 SYNC bits on the exit from Squelch. While forwarding USB packets from UUSP to eDSPp, the repeater may transmit the 1st bit (within the 4 allowable SYNC bits that a repeater can consume) of the SYNC pattern with random UI duration and add EOP dribble up to 4 random (SE0 or K or J) bit duration.

The eUSPr (in Rx) shall meet the following conditions:

- In HS operation, it shall be receiving differential data packets from eDSPp.
- In HS operation, it shall filter squelch for up to 4 UI to ignore SE0 from the repeater during EOP dribble.
- In FS/LS operation, it shall be receiving SE data packets from eDSPp.

5.4.4.2.2 Exit from L0.Tx

The repeater shall perform the following tasks:

- It shall transition to L0.Idle upon detection of a squelch condition or detection of SE0 for EOP followed by idle J at UUSP and the USB2.0 packet forwarding at eDSPp is completed.
- It shall transition to Reset if SE0 exceeded duration for LS Keep-Alive or link is FS.
- It shall transition to Lx (Lx.Resume) if host Resume is detected. Note: Scenario could exist where eUSPr may not transmit CM.Lx to the repeater. In this event, the eUSPr is in Lx while the repeater would remain in L0.Idle. Other than a potential minor power impact, link shall remain operational and repeater in L0.Tx shall be able to distinguish between an incoming eUSB2 packet, or USB2 packet and resume, for which it may implement a timer to differentiate resume event from data packet (maximum length of 8 UI running K) and transition to Lx (Lx.Resume).

The eUSPr (in Rx) shall perform the following tasks:

- In HS operation, it shall transition to L0.Idle upon detecting a squelched condition at eUSP.
- In FS operation, it shall transition to L0.Idle upon detecting an EOP (logic ‘1’ on eD+) condition at eUSP with duration required by USB 2.0 to declare EOP and not SE0 during cross-over.
- In LS operation, it shall transition to L0.Idle upon detecting an EOP (logic ‘1’ on eD-) condition at eUSP with duration required by USB 2.0 to declare EOP and not SE0 during cross-over.

5.4.4.3 L0.Rx

L0.Rx is a substate where a USB2.0 packet is received from eDSPp and forwarded directly to UUSP.

5.4.4.3.1 L0.Rx Requirements

The repeater shall meet the following conditions:

- It shall operate at REP mode.
- It shall forward the USB2.0 packets upon detection of a high-speed un-squelch condition or a LS/FS data K at eDSPp. Note: The repeater can consume 4 SYNC bits on the exit

from Squelch. While forwarding USB packets from eDSPp to UUSP, the repeater may transmit the 1st bit (within the 4 allowable SYNC bits that a repeater can consume) of the SYNC pattern with random UI duration and add EOP dribble up to 4 random (K or J) bit duration.

The eUSPr (in Tx) shall meet the following conditions:

- In HS operation, it shall be transmitting differential data packets to eDSPp.
- In FS operation, it shall be transmitting SE data packets to eDSPp on eD- followed by an EOP as described in Section 3.3.1 on eD+.
- In LS operation, it shall be transmitting SE data packets to eDSPp on eD+ followed by an EOP as described in Section 3.3.1 on eD-.

5.4.4.3.2 Exit from L0.Rx

The repeater shall perform the following tasks:

- The repeater shall transition to L0.Idle if the following conditions are met:
  - It has completed the transmission of USB2.0 packet at D+/D-.
  - It has detected a squelched condition or EOP at eD+/eD-.

The eUSPr (in Tx) shall perform the following tasks:

- The eUSPr shall transition to L0.Idle if it has completed the transmission of the USB packet at its eUSB2 interface.

5.4.5 **Lx**

Lx is a state where the repeater is in power saving mode. The repeater power management maybe different between L1 and L2, but there is no difference with respect to the operation and mechanism of repeater state transition. Section 5.5.12, 5.5.13 shows the timing sequence of the FS L1 and L2 entry, while Section 5.5.17 shows the L2 entry of a HS link. Lx substate machine is shown in Figure 5-15.

- The repeater shall be in NREP mode.

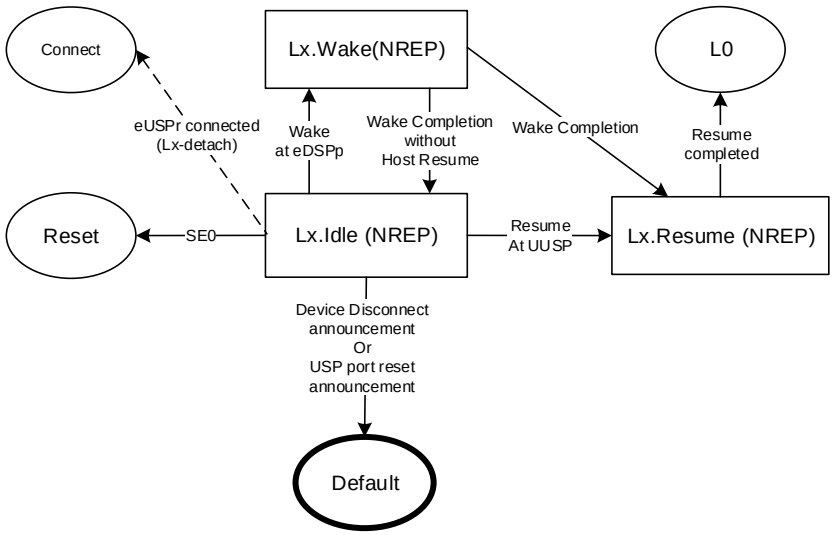


Figure 5-15: Lx Substate Machine

5.4.5.1 Lx.Idle

Lx.Idle is a substate where the repeater is in low power idle state.

5.4.5.1.1 Lx.Idle Requirements

The repeater shall meet the following requirements:

- It shall maintain SE0 at eDSPp by enabling its R_{PD} at eD+/eD-.
- It shall enable its SE receivers at eDSPp.
- It shall disable its high-speed transceivers.
- The USB2.0 port of the repeater shall meet the requirements defined by USB2.0.

The eUSPr shall meet the following conditions:

- It shall enable its SE receivers at eD+/eD- in expectation of resume. Note: Scenario could exist where eUSPr may not transmit CM.Lx to the repeater. In this event, the eUSPr is in Lx while the repeater remains in L0.Idle. Other than a potential minor power impact, link shall remain operational and repeater in L0 shall be able to distinguish between an incoming eUSB2 packet, or USB2 packet and a resume or wake. It may implement a timer to differentiate a resume event from data packet (maximum length of 8 UI running K). SOWake is a SE1 condition and can be distinguished without a timer.
- It shall disable its high-speed transceivers.

5.4.5.1.2 Exit from Lx.Idle

The repeater performs the following tasks:

- It shall transition to Lx.Resume if it has detected resume at UUSP.
- It shall transition to Lx.Wake if it has detected remote wake at eDSPp.
- It shall transition to Default if Port Reset is received.

The eUSPr perform the following tasks:

- It shall transition to Lx.Wake if to perform remote-wake.
- It shall enter Lx.Resume if it has detected host resume from the repeater.
- It shall transition to Reset if has detected logic ‘1’ on eD+/eD- (FS/LS Lx) as bus reset. Note: In the unlikely event where both Bus Reset and Wake occur concurrently which may result in a link error condition, implementation may utilize Port Reset to recover.
- It shall transmit Port Reset if directed by its controller to perform a soft disconnect.
- Note: Although implementation specific, given the possible window where role swap occurs during Lx, eUSPr shall transmit Port Reset and transition to Default in the event of role swapping where the UTMI+ interface changed from peripheral to host mode. This is then followed by Repeater Configuration to reconfigure the repeater to host mode operation.

5.4.5.2 Lx.Resume

Lx.Resume is a substate where the host starts exiting from L1 or L2.

5.4.5.2.1 Lx.Resume Requirements

The repeater shall meet the following conditions:

- It shall monitor the resume at UUSP, and drive the eUSB2 resume at eDSPp as defined in Section 5.5.12 and 5.5.13 for FS resume from L1 and L2 respectively, and Section 5.5.17 for HS resume from L2, until its completion.
- It shall monitor the resume at UUSP until its completion.
- It shall end resume at its eDSPp upon detecting EOResume at its UUSP. Refer to Section 3.3.5 for EOResume transmission.

The eUSPr shall meet the following conditions:

- It shall reflect resume to its UTMI+ interface indicating host resume.
- It shall reflect to its UTMI+ interface the end of resume upon detecting EOResume.

5.4.5.2.2 Exit from Lx.Resume

- The repeater and eUSPr shall transition to L0 upon completion of resume.

5.4.5.3 Lx.Wake

Lx.Wake is a substate where an eUSB2 peripheral device initiates remote wake to resume the USB traffic. Section 5.5.12 and 5.5.18 shows the timing waveform of L2 wake to FS and HS respectively. Additionally, Section 5.5.16 and 5.5.19 provides timing sequences of a FS and HS wake from L2 without the host resume being triggered.

5.4.5.3.1 Lx.Wake Requirements

The repeater shall meet the following conditions:

- It shall follow the eUSB2 remote wake protocol as defined in Section 5.5.12 and 5.5.18.
- The UUSP shall perform remote wake defined by USB2.0.
- It shall drive remote wake at UUSP while the remote wake signal at eDSPp is observed. Note Delay in repeater forwarding remote wake shall meet related USB2.0 hub timing parameters.

While driving remote wake at UUSP, the repeater shall map the lineatate at UUSP to eUSPr in repeating mode as defined in

- Table 3-1.
- Upon detecting EOWake (a logic ‘0’ to logic ‘1’ transition on eD+(FS/HS) or eD-(LS) indicating the end of remote wake signaling from eUSPr), the repeater shall perform the following.
    - It shall stop driving remove wake at UUSP.
    - It shall monitor the linestate at UUSP and map the linestate from UUSP to eDSPp.
    - With host resume seen on UUSP, repeater continue to map resume K on UUSP to logic ‘1’ on eD- (FS/HS) or eD+ (LS) until the end of host resume.
    - If host resume is not observed, the repeater shall filter any SE0 seen during cross over on UUSP while D+/D- transition from K to Idle J to eUSPr. And due to the repeater filtering, K may continue to be presented on eD- (FS) or eD+ (LS) beyond the completion of EOWake. The repeater may require a timer to disable SE0 filtering in expectation of EOResume SE0. The eUSPr shall not declare as host resume (host resume shall be declared as K to SE0 EOResume). Refer to Section 3.3.6 for wake signaling. Note that in this event that no host resume is observed, a repeater may disable its UUSP, terminate resume, and returns to Lx. To recover the link from an unresponsive host, a repeater may provide an option to issue Port Reset to start a new USB session.

The eUSPr shall meet the following conditions:

- In FS Lx, it shall drive remote wake as defined in Section 3.3.6.1.2 at eD+/eD- when directed by its controller.
- In LS Lx, it shall drive remote wake as defined in Section 3.3.6.1.2 at eD+/eD- when directed by its controller.
- It may continue to observe K on eD- beyond the completion EOWake, even if host resume is not returned after wake. In this scenario, it shall observe a K to Idle J transition which it shall not declare as host resume (host resume shall be declared as K to SE0 EOResume).

5.4.5.3.2 Exit from Lx.Wake

The repeater shall perform the following tasks:

- It shall transition to Lx.Resume upon completion of wake and detected a resume K at UUSP. Note: A successful remote wake shall follow with resume. The repeater shall transition to Lx if resume K is not detected. Refer to Section 5.5.15 for wake from suspend.

The eUSPr shall perform the following tasks:

- It shall transition to Lx.Resume upon completion of wake and detected a resume K at eD+/eD-. Note: A successful remote wake shall follow with resume.

5.5 *Host-Peripheral Repeater Mode Link Operation*

This section illustrates the various Host-Peripheral repeater mode link operation.

5.5.1 **Host Mode Repeater POR and Configuration**

Figure 5-16 shows the timing diagram of a host mode repeater sequencing through Port Reset, Default, Connect, Reset and L0.

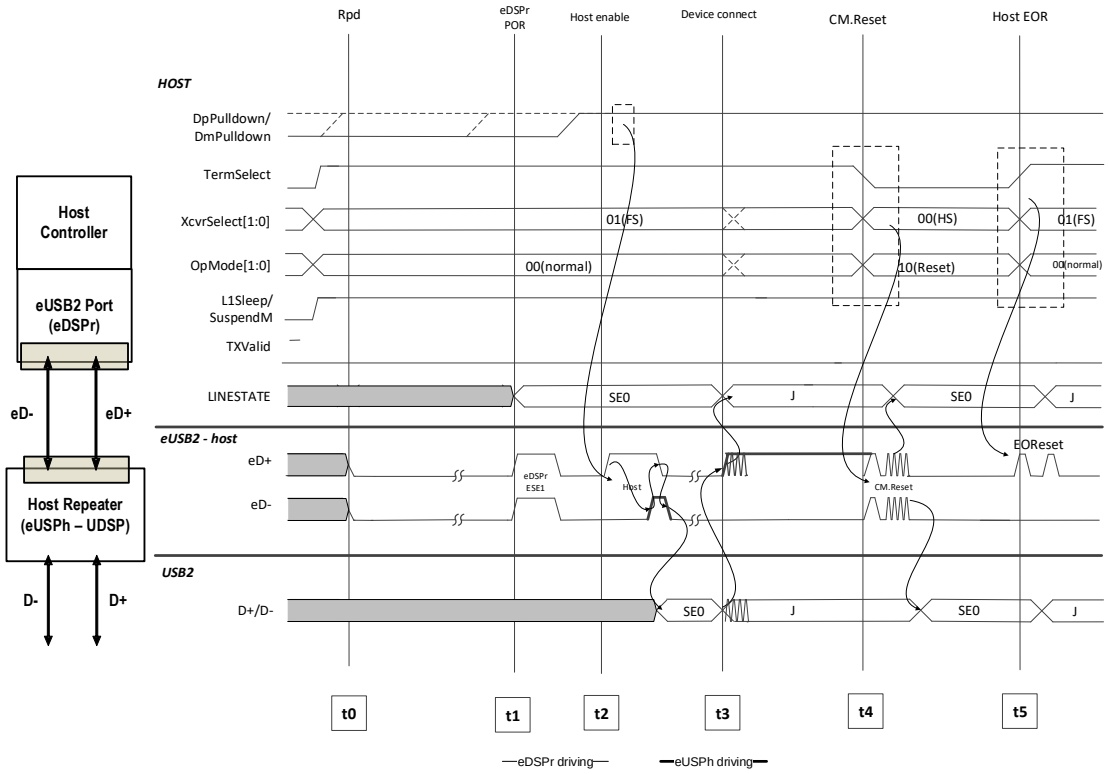


Figure 5-16: Host Mode Repeater Configuration

t0:

- Rpd

t1:

- eDSPr POR and transmits ESE1 as Port Reset.

t2:

- eDSPr transmits Repeater Configuration with logic ‘1’ on eD+, to its associated repeater for host mode operation. Note: UTMI+ pulldown indicating host mode operation may have been stable or static at time zero. Transmission of Repeater Configuration shall not depend on a change on UTMI+ pulldown. This is implementation specific on when to transmit this announcement where eDSPr/eUSPr may sample the UTMI+ pulldown state upon completion of ESE1. If UTMI+ pulldown indicator changes after or in the middle of transmitting Repeater Configuration, eDSPr and eUSPr shall transmit ESE1 as Port Reset, follow by Repeater Configuration to re-configure its repeater.
- eUSPh acknowledge eDSPr Repeater Configuration upon POR. Note: eUSPh POR is asynchronous to eDSPr. If eDSPr coming out from POR prior to eUSPh, eDSPr shall transmit Port Reset announcement follow by Repeater Configuration and monitor for eUSPh acknowledgement. On the other hand, if eUSPh comes out of POR first, it shall stay in default pending eDSPr Port Reset and Repeater Configuration.

t3:

- Device connect with Pullup-J on D+/D-.
- Host repeater transmits logic ‘1’ on eD+ to eDSPr to announce device connect.
- Note that USB2.0 D+/D- is shown experiencing a signaling bounce. These bounces are mapped to the eUSB2 line as defined in Section 5.3.1.

t4:

- CM.Reset from eDSPr. Note: Depending on implementation, UTMI+ xcvrselect and opmode may not change together with UTMI+ termselect. UTMI+ termselect may be the sole trigger for CM.Reset.
- eUSPh drops logic ‘1’ on eD+ and declare a FS (or HS depending on chirp handshake during bus reset) connection.

t5:

- EOReset (LS UI duration) from eDSPr. Note: Depending on implementation, UTMI+ xcvrselect and opmode may not change together with UTMI+ termselect. UTMI+ termselect may be the sole trigger for EOReset.
- Link enter FS L0 operation.

5.5.2 **Peripheral Mode Repeater POR and Configuration**

Figure 5-17 shows the timing diagram of a peripheral mode repeater sequencing through Port Reset, Default, Connect, Reset and L0.

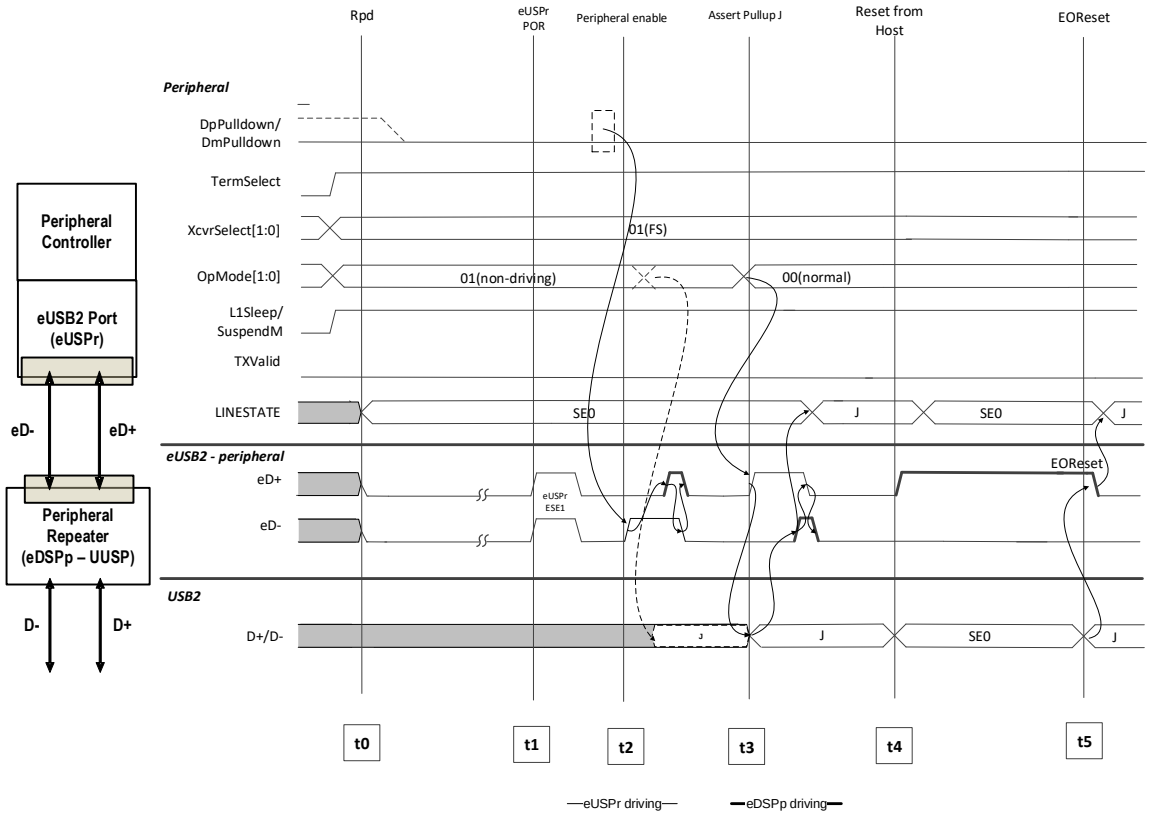


Figure 5-17: Peripheral Mode Repeater Configuration

t0:

- Rpd

t1:

- eUSPr POR and transmits ESE1 as Port Reset.

t2:

- eUSPr transmits Repeater Configuration with logic ‘1’ on eD-, to its associated repeater for peripheral mode operation. Note: UTMI+ pulldown indicating peripheral mode operation may have been stable or static at time zero. Transmission of Repeater Configuration shall not depend on a change on UTMI+ pulldown. This is implementation specific on when to transmit this announcement where eDSPr/eUSPr may sample the UTMI+ pulldown state upon completion of ESE1. If UTMI+ pulldown indicator changes after or in the middle of transmitting Repeater Configuration, eDSPr and eUSPr shall transmit ESE1 as Port Reset, follow by Repeater Configuration to re-configure its repeater.
- eDSPp POR and acknowledge to eUSPr. Note: eDSPp POR is asynchronous to eUSPr. If eUSPr coming out from POR prior to eDSPp, eUSPr shall transmit Port Reset announcement follow by Repeater Configuration and monitor for eDSPp acknowledgement. On the other hand, if eDSPp comes out of POR first, it shall stay in default pending eUSPr Port Reset and Repeater Configuration.

t3:

- eUSPr transmits logic ‘1’ on eD+ to its associated repeater to enable pullup J.

- Peripheral repeater asserts Pullup-J on D+/D-. Note that, as illustrated with the dotted arrow, UTMI+ opmode may have transition to “normal” earlier (or at time zero). In this scenario, the eUSPr shall change its UTMI+ linestate to J but only transmit logic ‘1’ on eD+ after it has received Repeater Configuration.
- eDSPp pulses eD-, eUSPr drops eD+ and eDSPp drops eD-.
- Linestate on eUSPr change from SE0 to J.

t4:

- Reset from Host results in SE0 on D+/D-.
- eDSPp maps D+/D- SE0 to logic ‘1’ on eD+.

t5:

- EOReset from host with J on D+/D-.
- eDSPp maps D+/D- J to SE0 on eD+/eD-.
- Link enters FS L0 operation.

5.5.3 **Establishing LS Link**

In the scenario where a host and LS peripheral is connected, Figure 5-18 shows the sequence of a Host and Peripheral repeater with its associated eDSPr/eUSPr connecting, bus reset and eventually entering L0.

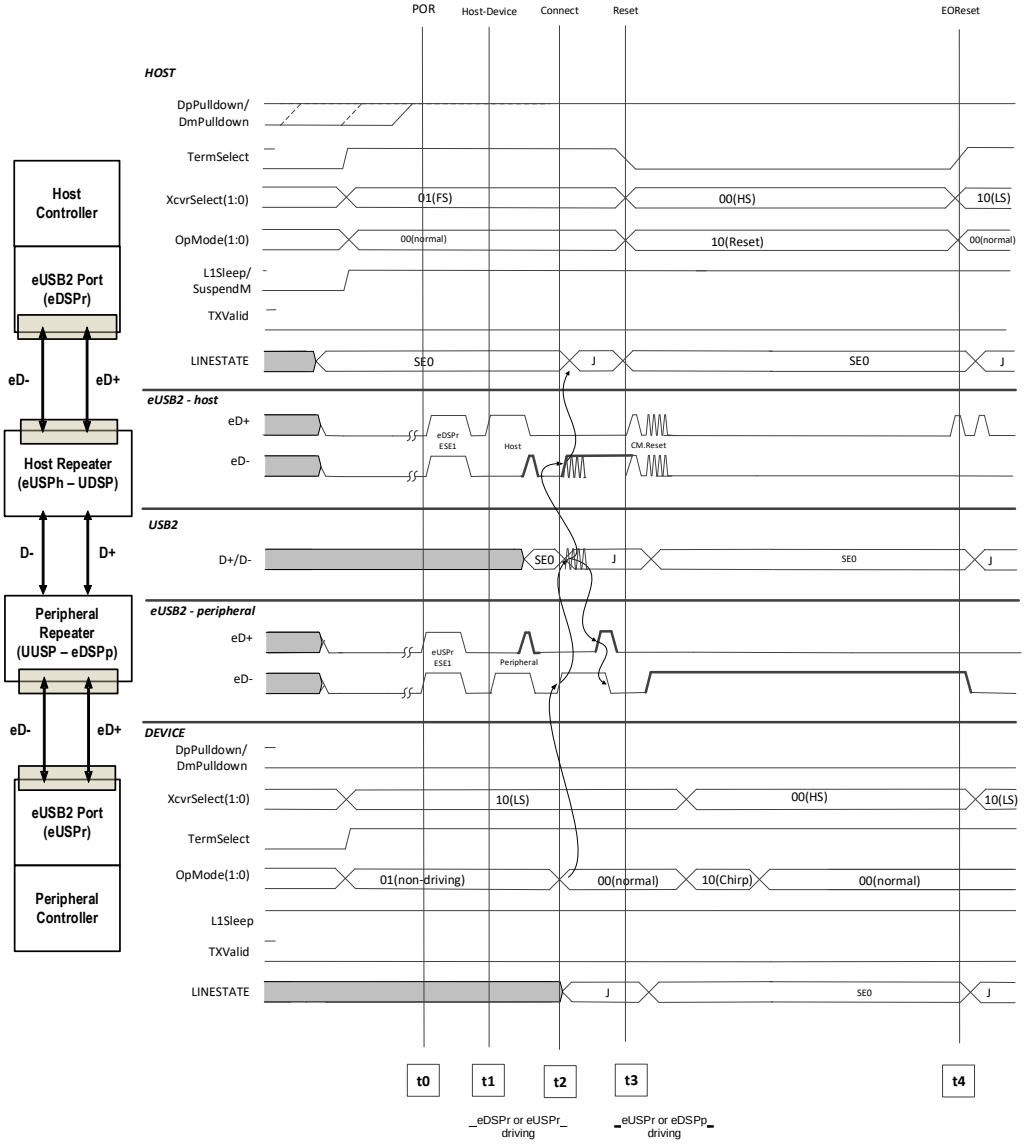


Figure 5-18: Establishing LS Link

t0:

- eDSPr and eUSPr POR with Port Reset announcement.
- Note that these PORs are asynchronous.

t1:

- eUSPr and eDSPr configuring peripheral and host mode operation respectively with Repeater Configuration.
- eDSPp and eUSPh acknowledge.
- Note that these events are asynchronous.

t2:

- eUSPr asserts logic ‘1’ on eD- to enable pull up J for device attach.

- Device attach event propagates to eDSPr.
- Note that USB2.0 D+/D- is shown experiencing a signaling bounce. These bounces are mapped to the eUSB2 line as defined in Section 5.3.1.

t3:

- eDSPr transmits CM.Reset to eUSPh for bus reset.
- eUSPh drops logic ‘1’ on eD- and declare a LS connection.
- eDSPp maps SE0 on D+/D- to logic ‘1’ on eD-.

t4:

- EOReset from eDSPr resulted with a LS J on D+/D-. Note: Depending on implementation, UTMI+ xcvrselect and opmode may not change together with UTMI+ termselect. UTMI+ termselect may be the sole trigger for EOReset.
- eDSPp maps D+/D- J to SE0 on eD+/eD-.
- Link enters LS L0 operation.

5.5.4 **Establishing HS Link**

In the scenario where a HS capable host and peripheral is connected, Figure 5-19 shows the sequence of a Host and Peripheral repeater with its associated eDSPr/eUSPr connecting, chirping and eventually entering L0.

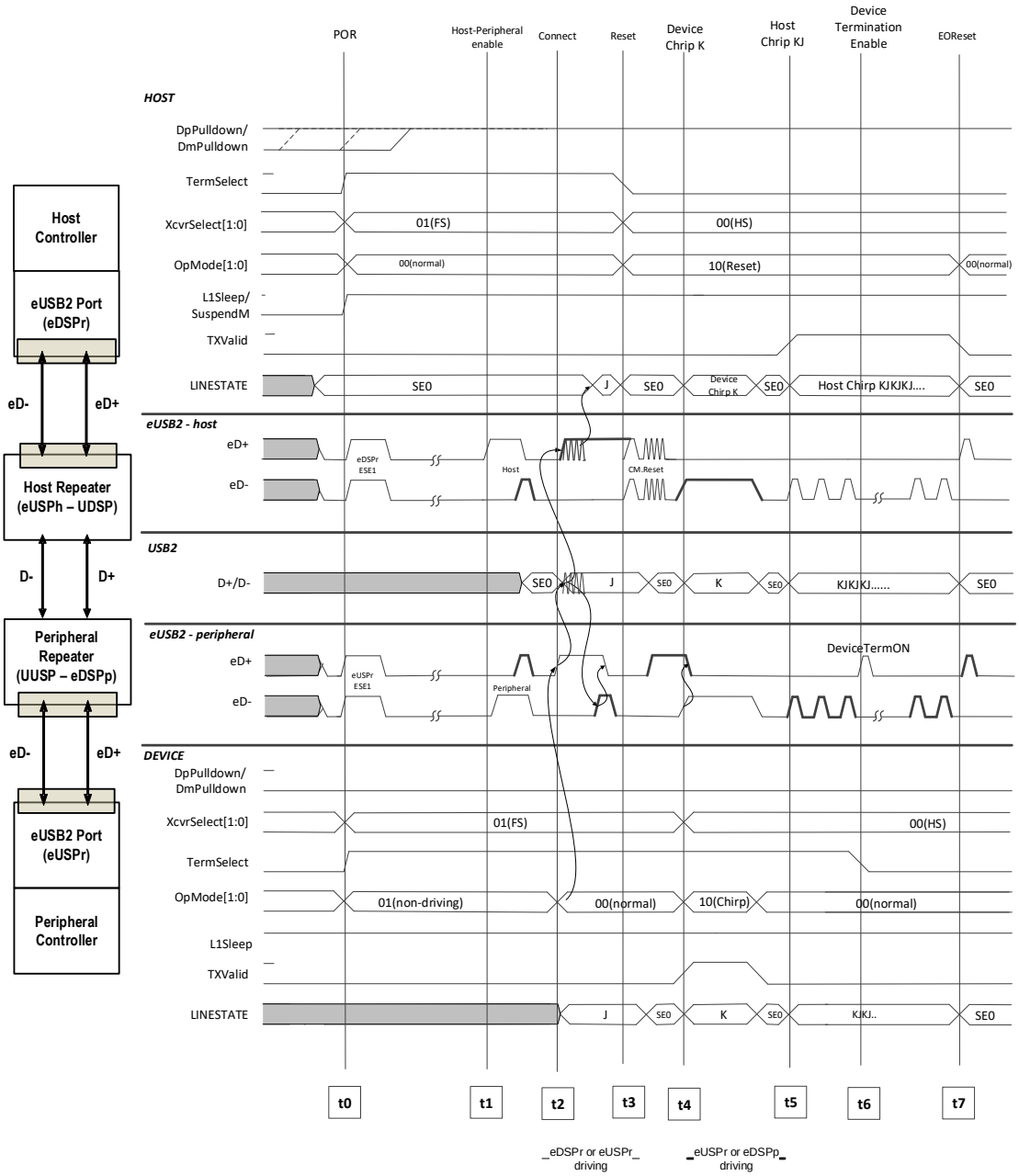


Figure 5-19: Establishing HS Link

t0:

- eDSPr and eUSPr POR with Port Reset announcement.
- Note that these PORs are asynchronous.

t1:

- eUSPr and eDSPr configuring peripheral and host mode operation respectively with Repeater Configuration.

- eDSPp and eUSPh acknowledge.
- Note that these events are asynchronous.

t2:

- eUSPr asserts logic ‘1’ on eD+ to enable pull up J for device attach.
- Device attach event propagates to eDSPr.
- Note that USB2.0 D+/D- is shown experiencing a signaling bounce. These bounces are mapped to the eUSB2 line as defined in Section 5.3.1.

t3:

- eDSPr transmits CM.Reset to eUSPh for bus reset.
- eUSPh drops logic ‘1’ on eD+ and declare a FS (or HS depending on chirp handshake during bus reset) connection.
- eDSPp maps SE0 on D+/D- to logic ‘1’ on eD+.
- Note: This same flow of event is applicable for a FS idle link (where an idle J transition to SE0 on D+/D- is mapped to a SE0 on eD+/eD- transition to logic ‘1’ on eD+) being reset and eventual established as HS (in the case of FS upgrading to HS).

t4:

- eUSPr transmits device chirp K.
- eDSPp drops eD+ upon receiving device chirp K.

t5:

- Host chirp K-J follows.

t6:

- eUSPr pulses eD+ to eDSPp to indicate transition to HS.
- eDSPp enables HS termination.

t7:

- EOReset and enter L0.

5.5.5 LS Link Disconnect and Reconnect

This flow, as shown in Figure 5-20, describes the process where Host and Peripheral disconnecting from an established a LS link, and finally reconnecting.

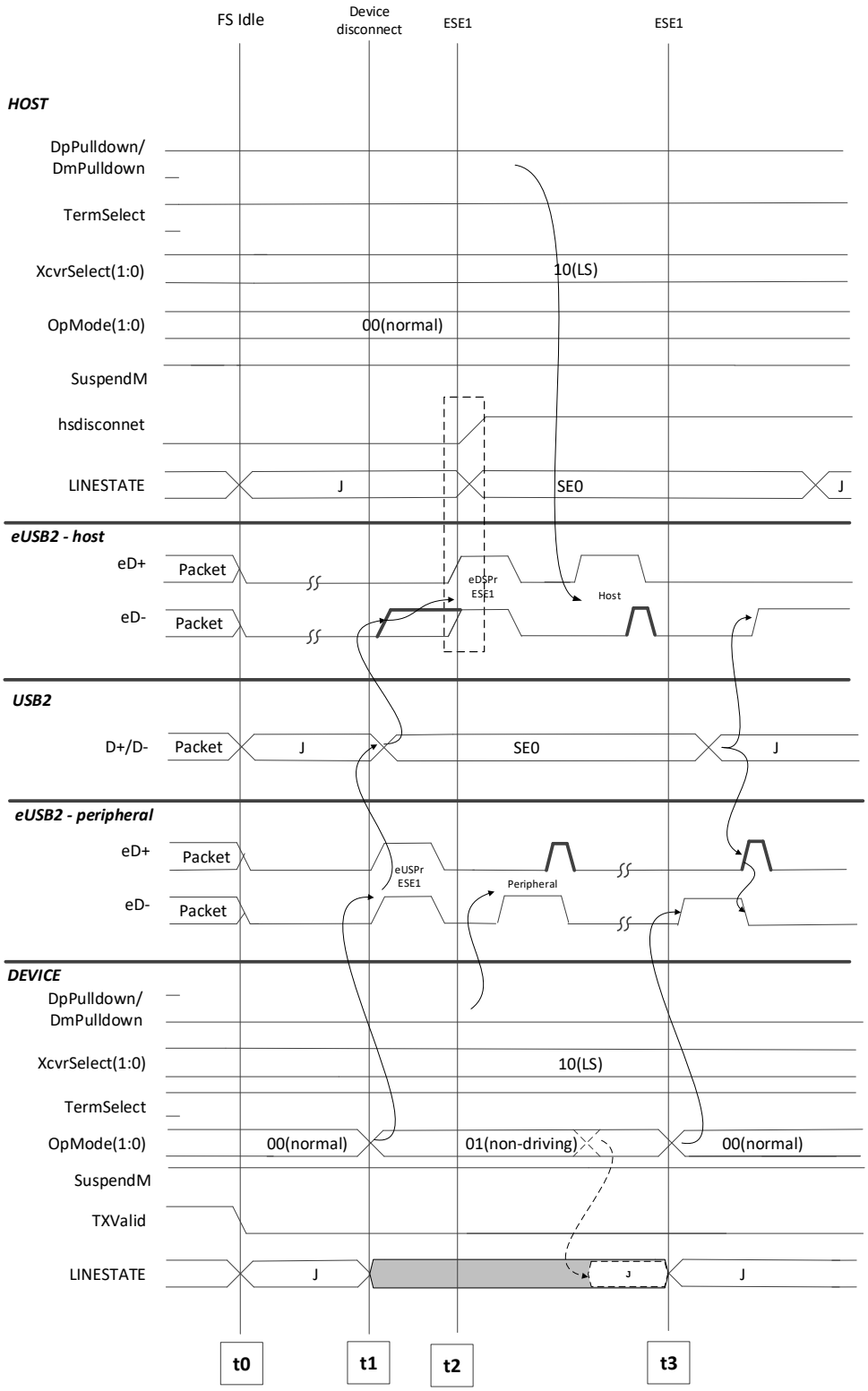


Figure 5-20: LS Link Disconnect and Reconnect

t0:

- LS idle with pull J on D+/D-.
- LS idle with SE0 on eD+/eD-.

t1:

- eUSPr triggers soft disconnect with UTMI+ opmode changed. Note: physical device detach would behave similarly with D+/D- becoming SE0.
- eUSPr transmit ESE1 to eDSPp to remove pullup J.
- D+/D- becomes SE0 and eUSPh maps this to logic ‘1’ on eD-. Note: Host Repeater does not qualify this SE0 as device disconnect but rather mapping D+/D- SE0 to logic ‘1’ on eD-. It is the responsibility of the eDSPr to qualify logic ‘1’ on eD- and declare device disconnect.

t2:

- Upon detecting logic ‘1’ on eD- and declaring device disconnect, eDSPr transmits ESE1 to eUSPh to indicate device disconnect.
- At the same time, eDSPr’s UTMI+ interface reflecting device disconnect.
- eUSPh stop driving logic ‘1’ on eD- upon receiving ESE1 from eDSPr.
- Both eUSPh and eDSPp return to default mode, and Repeater Configuration follows to re-enable operation.
- Note: UTMI+ pulldown may be static as indicated in Figure 5-20, hence transmitting Repeater Configuration shall not be triggered with the UTMI+ pulldown transition. This is implementation specific on when to transmit this announcement where eDSPr/eUSPr may sample the UTMI+ pulldown state upon completion of ESE1. If UTMI+ pulldown indicator changes after or in the middle of transmitting Repeater Configuration, eDSPr and eUSPr shall transmit ESE1 as Port Reset, follow by Repeater Configuration to re-configure its repeater.

t3:

- eUSPr transmitting logic ‘1’ on eD- as directed by its controller to initiate a new connection.
- Note that, as illustrated with the dotted arrow, UTMI+ opmode may have transition to “normal” earlier (or at time zero). In this scenario, the eUSPr shall change it UTMI+ linestate to J but only transmit logic ‘1’ on eD- after it has received Repeater Configuration.

5.5.6 **FS Link Disconnect and Reconnect**

This flow, as shown in Figure 5-21, describes the process where Host and Peripheral disconnecting from an established a FS link, and finally reconnecting

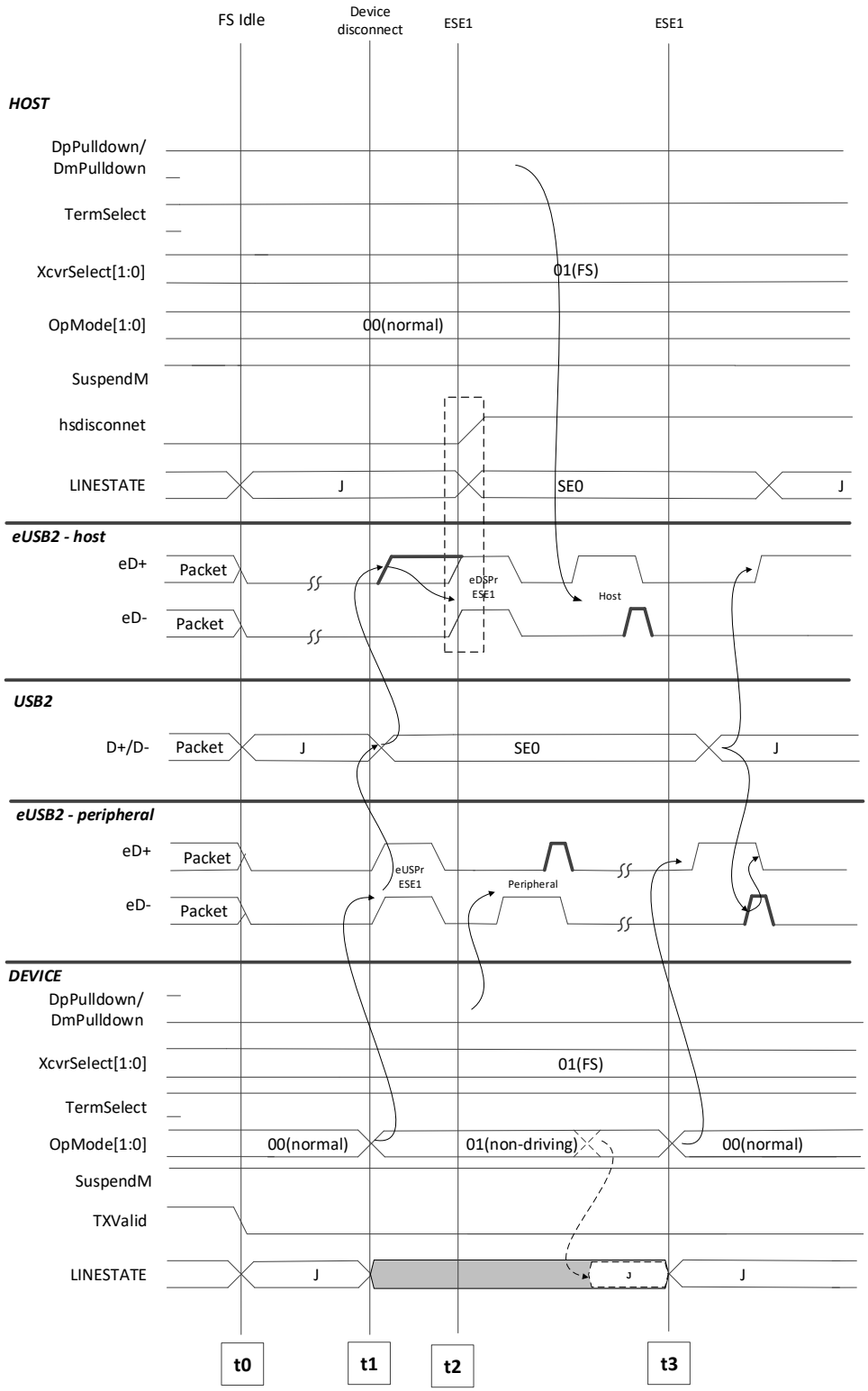


Figure 5-21: FS Link Disconnect and Reconnect

t0:

- FS idle with pull J on D+/D-.
- FS idle with SE0 on eD+/eD-.

t1:

- eUSPr triggers soft disconnect with UTMI+ opmode changed. Note: physical device detach would behave similarly with D+/D- becoming SE0.
- eUSPr transmit ESE1 to eDSPp to remove pullup J.
- D+/D- becomes SE0 and eUSPh maps this to logic ‘1’ on eD+. Note: Host Repeater does not qualify this SE0 as device disconnect but rather mapping D+/D- SE0 to logic ‘1’ on eD+. It is the responsibility of the eDSPr to qualify logic ‘1’ on eD+ and declare device disconnect.

t2:

- Upon detecting logic ‘1’ on eD+ and declaring device disconnect, eDSPr transmits ESE1 to eUSPh to indicate device disconnect.
- At the same time, eDSPr’s UTMI+ interface reflecting device disconnect.
- eUSPh stop driving logic ‘1’ on eD+ upon receiving ESE1 from eDSPr.
- Both eUSPh and eDSPp return to default mode, and Repeater Configuration follows to re-enable operation.
- Note: UTMI+ pulldown may be static as indicated in Figure 5-21, hence transmitting Repeater Configuration shall not be triggered with the UTMI+ pulldown transition. This is implementation specific on when to transmit this announcement where eDSPr/eUSPr may sample the UTMI+ pulldown state upon completion of ESE1. If UTMI+ pulldown indicator changes after or in the middle of transmitting Repeater Configuration, eDSPr and eUSPr shall transmit ESE1 as Port Reset, follow by Repeater Configuration to re-configure its repeater.

t3:

- eUSPr transmitting logic ‘1’ on eD+ as directed by its controller to initiate a new connection.
- Note that, as illustrated with the dotted arrow, UTMI+ opmode may have transition to “normal” earlier (or at time zero). In this scenario, the eUSPr shall change it UTMI+ linestate to J but only transmit logic ‘1’ on eD+ after it has received Repeater Configuration.

5.5.7 **Disconnecting from HS Link**

As oppose to FS/LS where declaring disconnect (ESE1) is the responsibility of the eDSP, detecting and declaring HS disconnect is performed by the host repeater. Figure 5-22 shows the sequence of which the host repeater declaring a HS disconnect.

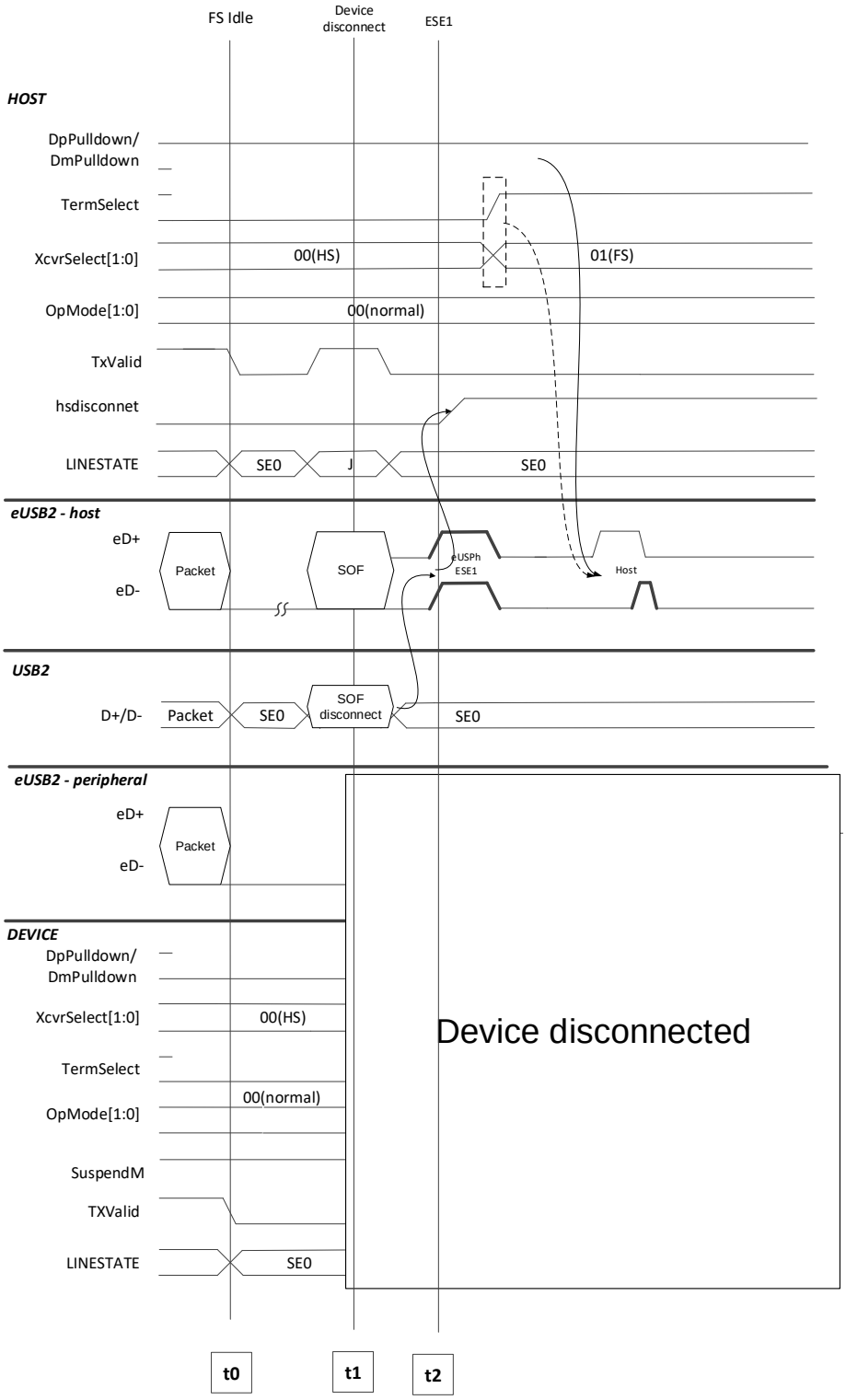


Figure 5-22: HS disconnect

t0:

- HS idle with SE0 on both D+/D- and eD+/eD-.

t1:

- Device disconnected with SOF amplitude changed.

t2:

- eUSPh transmits ESE1 to indicate HS device disconnect.
- eDSPr reflects disconnect to UTMI+ interface. Note that eDSPr shall not transmits Port Reset after receiving eUSPh ESE1 device disconnect.
- eUSPh returns to default mode of operation and Repeater Configuration follow to re-enable it.
- Note: Implementation may utilize termselect and xcvrselect change to and pulldown and transmit Repeater Configuration.

5.5.8 **Bus Reset during FS Link**

Once a FS link is established and a bus reset is triggered, Figure 5-23, shows the transition of the events and eventually re-establishing a link.

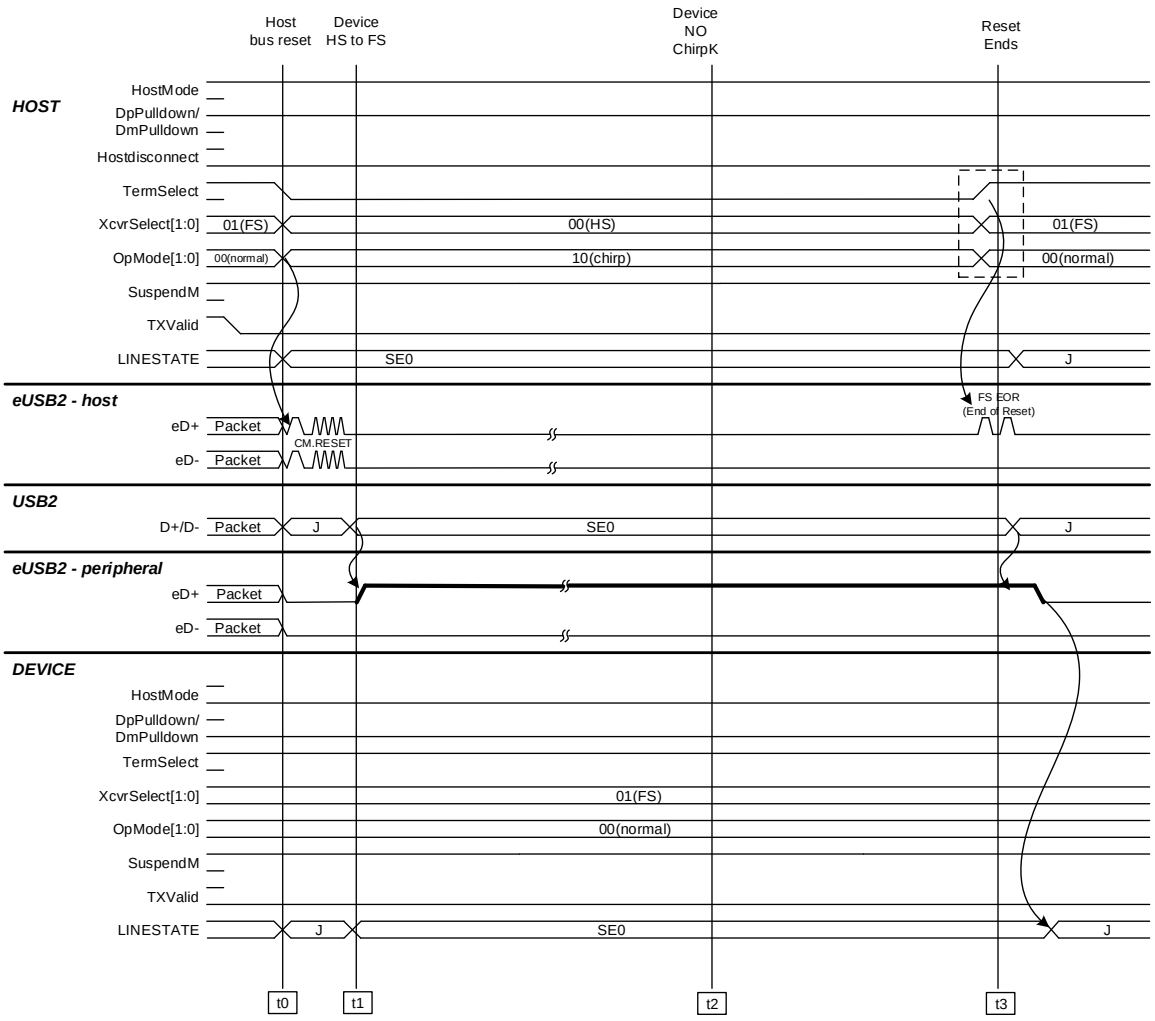


Figure 5-23: FS Link Bus Reset

t0:

- eDSPr HS bus reset with CM.Reset.

t1:

- eUSPh receives CM.Reset; directs its UDSP to apply HS terminations and drive the USB line to SE0
- UUSP observes J to SE0 transition on USB lines; eDSPp performs FS mapping and drives eD+ high.
- eUSPr reflects this condition as SE0 on its linestate output.

t2:

- eUSPr does not transmit device chirp K.

t3:

- eDSPr transmits FS EOReset.
- UDSP removes the driven SE0 condition on USB line
- UUSP after observing a J on USB lines, directs its eDSPp to stop driving the eD+ line
- eUSPr changes its linestate output to J from SE0

5.5.9 **Bus Reset during HS Link**

Once a HS link is established and a bus reset is triggered, Figure 5-24, shows the transition of the events and eventually re-establishing a link.

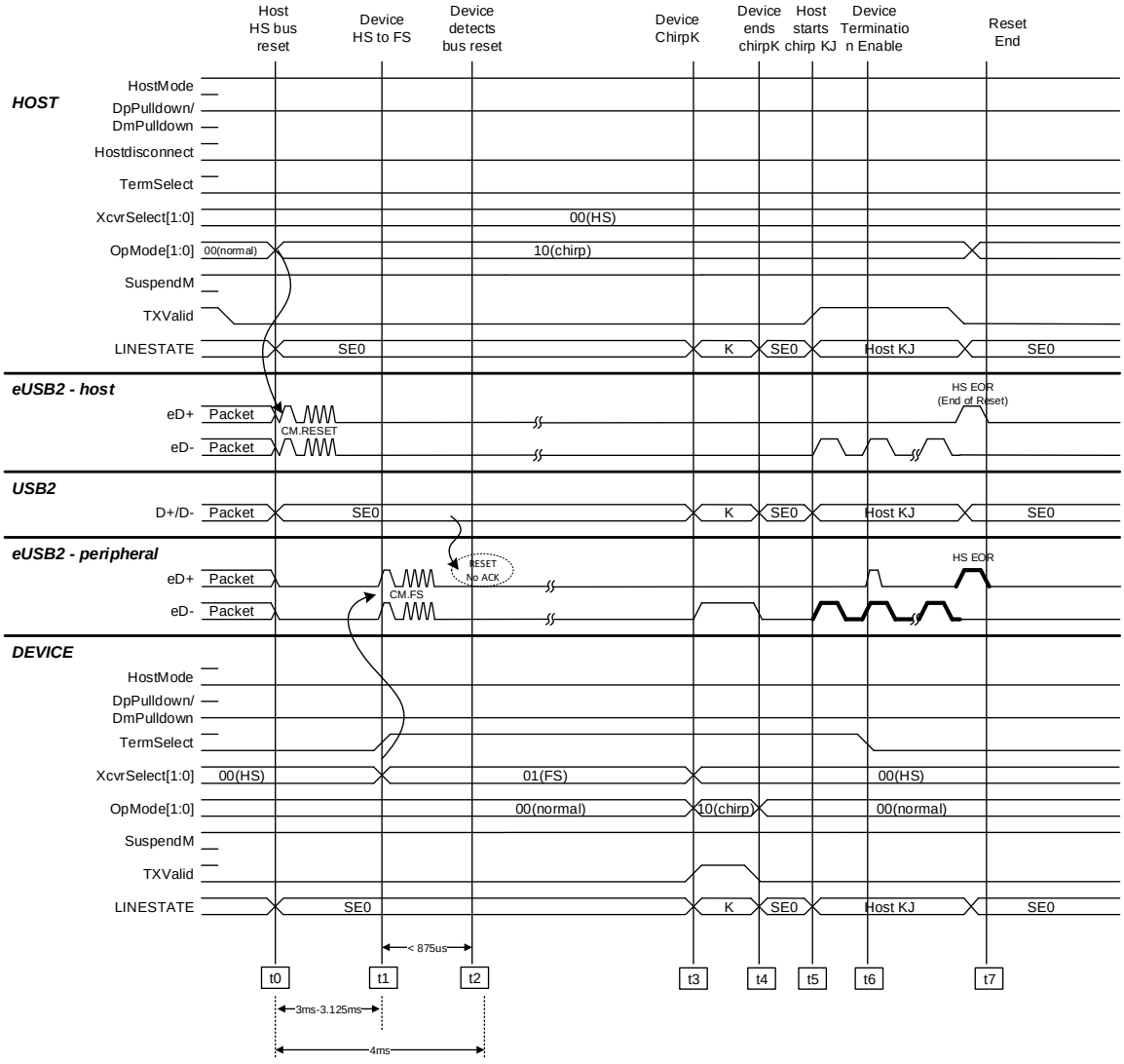


Figure 5-24: HS Link Bus Reset

t0:

- eDSPr HS bus reset with CM.Reset.

t1:

- eUSPr sends CM.FS after 3ms to check for reset or suspend
- Peripheral repeater starts $T_{PR\_HS\_RESET\_TO\_FS}$ timer and at its UUSP removes HS terminations and apply J pull-up. During this time, the peripheral repeater shall disable HS repeating but remain in HS mapping at eDSPp.

t2:

- Peripheral repeater detected SE0 at UUSP indicating bus reset. eDSPp sends no pulse/acknowledge on eD+. Note: $T_{PR\_HS\_RESET\_TO\_FS}$ timer shall continue to run to distinguish bus reset to HS or FS.

t3:

- eUSPr transmits device chirp K.

t4:

- eUSPr ends device chirp K.

t5:

- eDSPr transmits host chirp K.

t6:

- eDSPr and eUSPr transmits HS termination acknowledgement.

t7:

- eDSPr and eDSPp transmits EOReset.

5.5.10 **Bus Reset to FS with HS capable device and FS capable host**

Figure 5-25 shows the transition of the events of a bus reset during with a HS capable device connecting to a FS capable host.

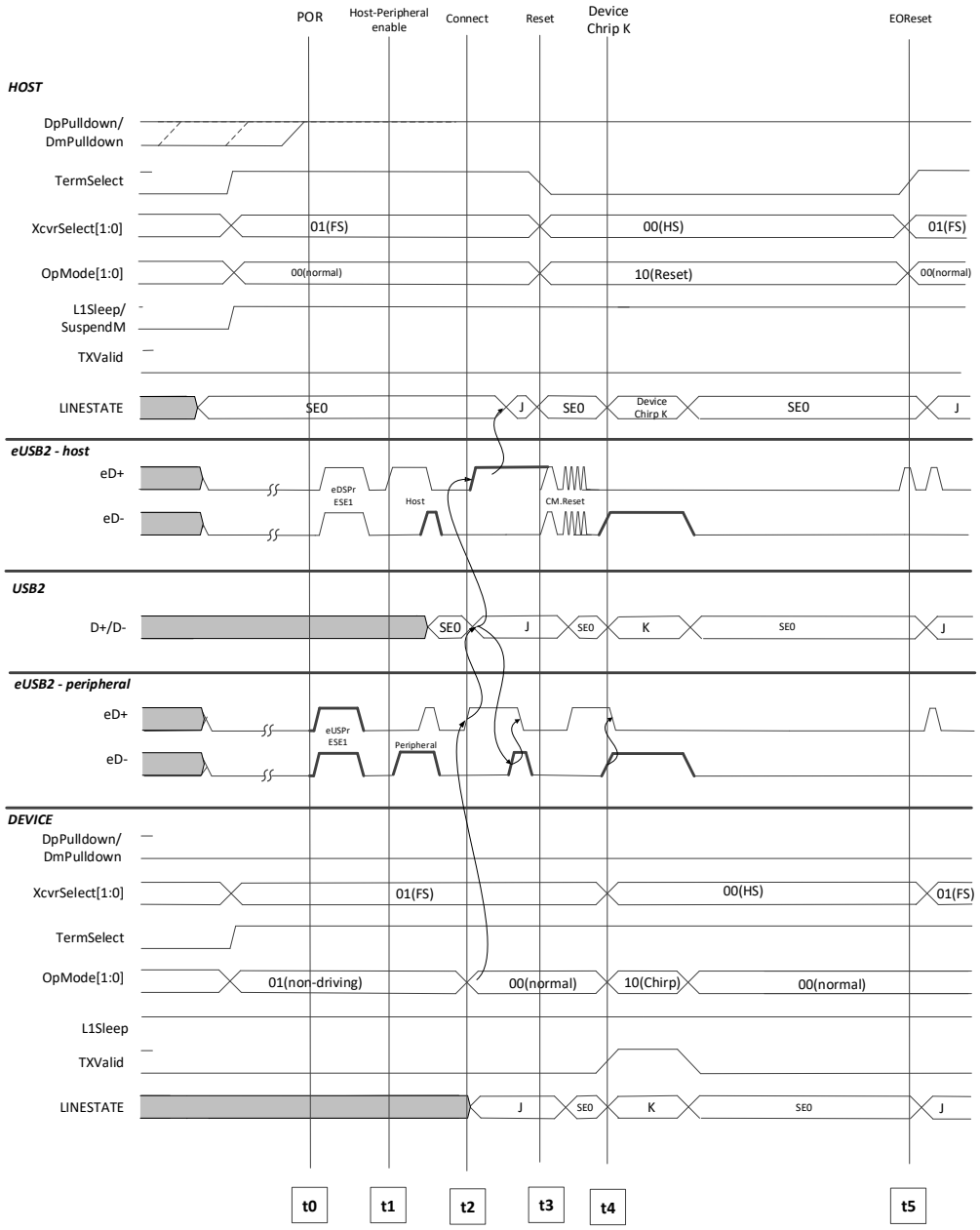


Figure 5-25: FS Link Bus Reset with FS host and HS device

t0:

- eDSPr and eUSPr POR with Port Reset.
- Note that these PORs are asynchronous.

t1:

- eUSPr and eDSPr configuring peripheral and host mode operation respectively with Repeater Configuration.
- eDSPp and eUSPh acknowledge upon POR.
- Note that these events are asynchronous.

t2:

- eUSPr asserts logic ‘1’ on eD+ to enable pull up J for device attach.
- Device attach event propagates to eDSPr.

t3:

- eDSPr transmits CM.Reset to eUSPh for bus reset.
- eUSPh drops logic ‘1’ on eD+ and declare a FS (or HS depending on chirp handshake during bus reset) connection.
- eDSPp maps SE0 on D+/D- to logic ‘1’ on eD+.
- Note: This same flow of event is applicable for a FS idle link (where an idle J transition to SE0 on D+/D- is mapped to a SE0 on eD+/eD- transition to logic ‘1’ on eD+) being reset and eventual established as HS (in the case of FS upgrading to HS).

t4:

- eUSPr transmits device chirp K.
- eDSPp drops eD+ upon receiving device chirp K.
- Note: Observed not host K-J chirp.

t5:

- eDSPr transmits EOReset (LS UI) and transition to FS L0.
- eDSPp upon observing SE0 to J transition on UUSP, transmits EOReset to eUSPr to end bus reset and enter FS L0.

5.5.11 **Bus Reset to FS during HS Link**

Figure 5-26 shows the transition of the events of a bus reset during HS link with the eventual re-established to FS.

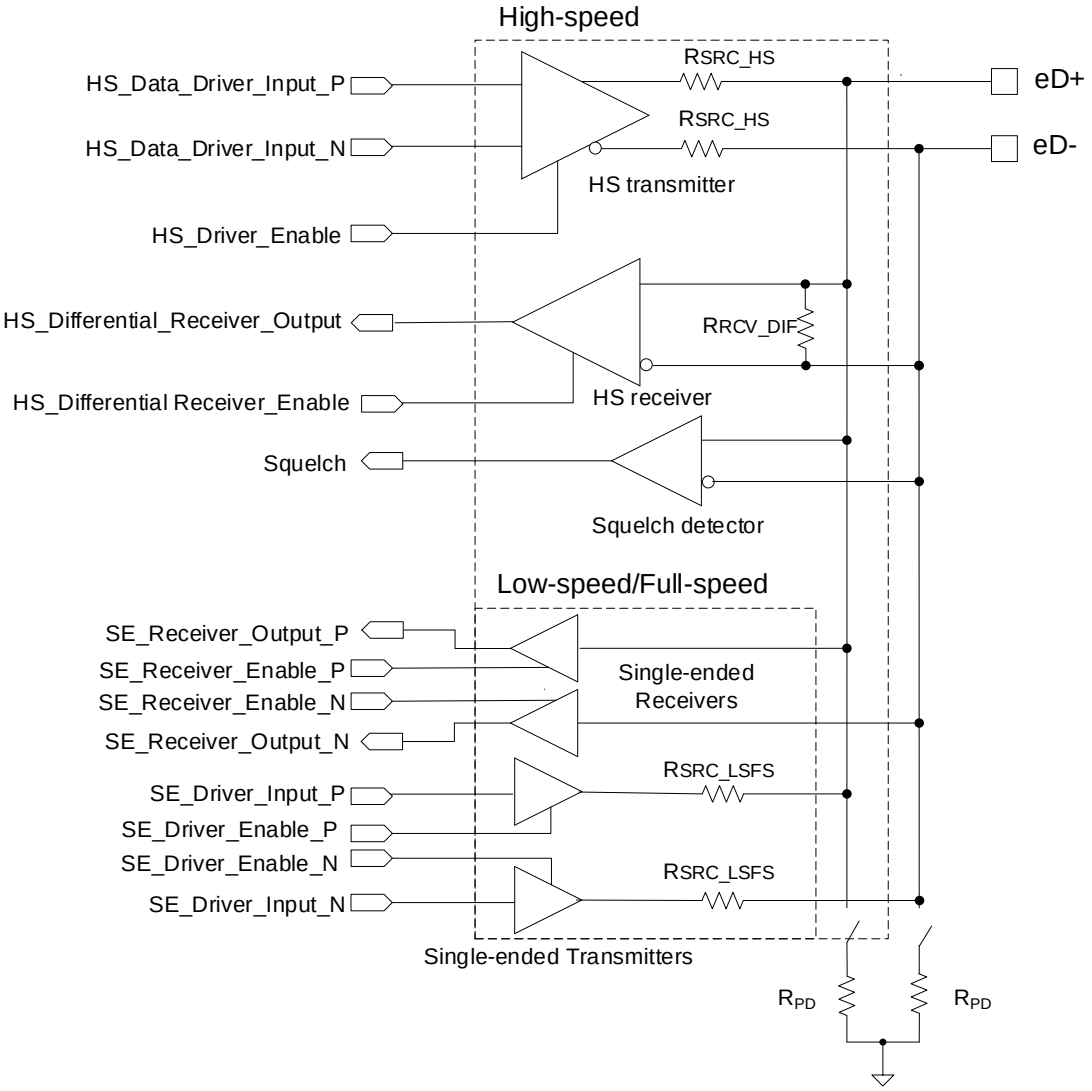


Figure 5-26: HS Link Bus Reset to FS

t0:

- eDSPr HS bus reset with CM.Reset.

t1:

- eUSPr sends CM.FS after 3ms to check for reset or suspend.
- Peripheral repeater starts $T_{PR\_HS\_RESET\_TO\_FS}$ timer and at its UUSP removes HS terminations and apply J pull-up. During this time, the peripheral repeater shall disable HS repeating but remain in HS mapping at eDSPp.

t2:

- Peripheral repeater detected Idle J at UUSP indicating bus reset. Note: In this scenario where an established HS link is downgraded to FS, the peripheral repeater shall adhere to $T_{PR\_HS\_RESET\_TO\_FS}$ in recognizing USB2.0 bus reset where in this case Idle J shall not be presented at UUSP as compared to Lx entry as illustrated in Section 5.5.17.

- UUSP samples SE0 on D+/D-
- eDSPp sends no pulse/acknowledge on eD+.

t3:

- eUSPr does not transmit device chirp K. Note: Transition is applicable if device transmits chirp K but host doesn't not perform chirp K-J.

t4:

- eDSPr transmits FS EOReset (LS UI).
- UDSP removes the driven SE0 condition on USB line
- UUSP after observing a J on USB lines, directs its eDSPp to send T_{STROBE} EOReset pulse
- eUSPr changes its linestate output to J from SE0

5.5.12 **FS Link L1 entry and resume**

FS link L1 entry and resume sequences are illustrated in Figure 5-27 below.

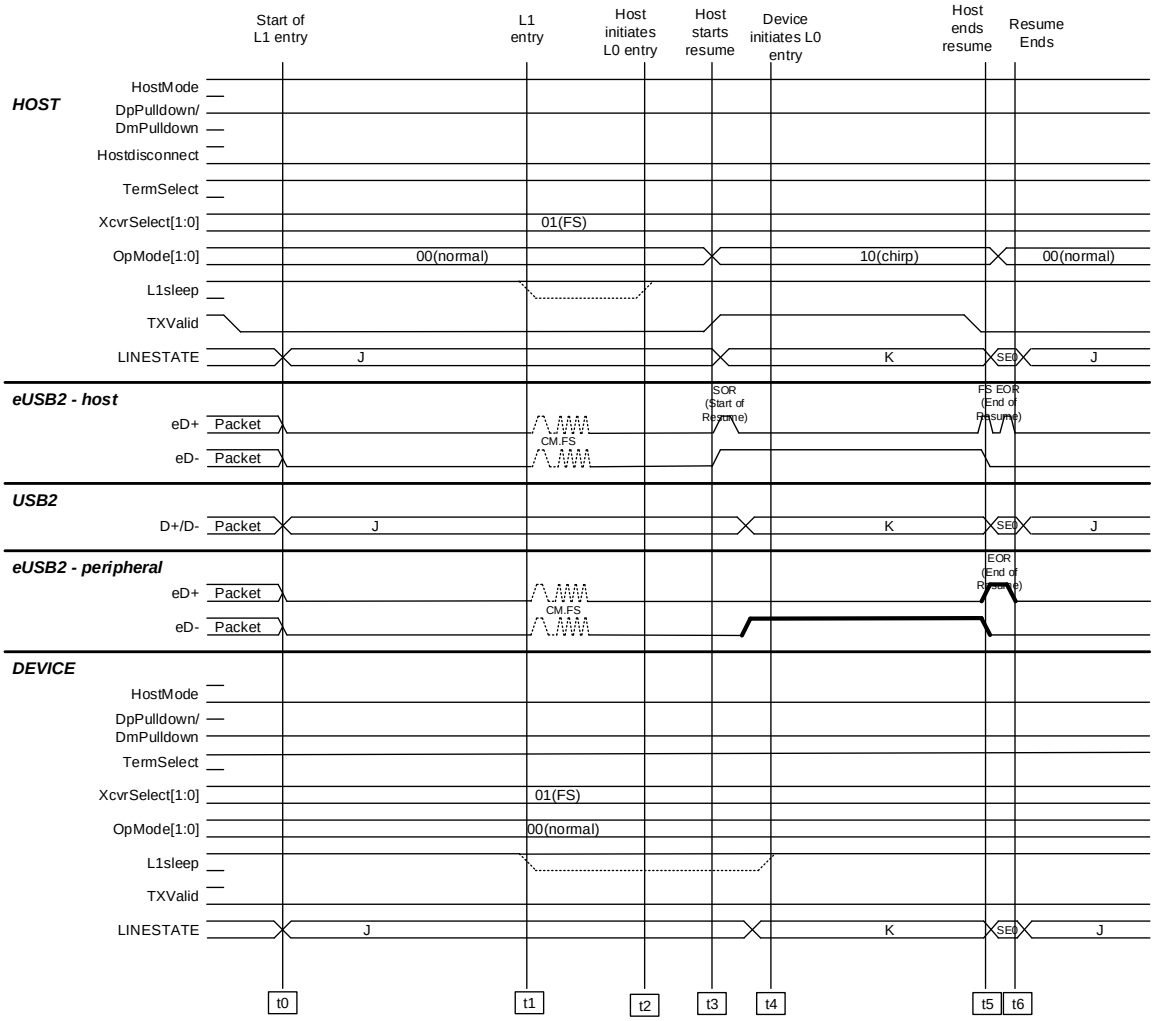


Figure 5-27: FS Link L1 entry and resume

t0:

- eDSPr initiates suspend, stops driving anything on the line

t1:
- eDSPr and eUSPr declare bus L1 entry after L1 token exchange
- Respective controllers may or may not assert L1sleep
- If L1sleep asserted, eUSB port sends CM.FS to its repeater

t2:
- eDSPr controller initiates L0 entry

t3:
- eDSPr starts sending resume,
- eUSPh detects SE1 followed by logic ‘1’ on eD-; eUSPh stops FS mapping mode
- UDSP sends resume on USB lines after SE1 followed by logic ‘1’ on eD- is detected.
- eDSPp enters repeat mode after detecting K on USB lines and drives eD- to logic ‘1’
- eUSPr changes linestate to K

t4:
- eUSPr controller de-asserts suspend if required

t5:
- eDSPr ends resume with EOResume
- eDSPp exits repeat mode after observing EOP on USB lines and sends EOP on eD+ line

t6:
- resume completes

5.5.13 FS Link L2 entry and resume

FS link L2 entry and resume sequences are illustrated in Figure 5-28 below.

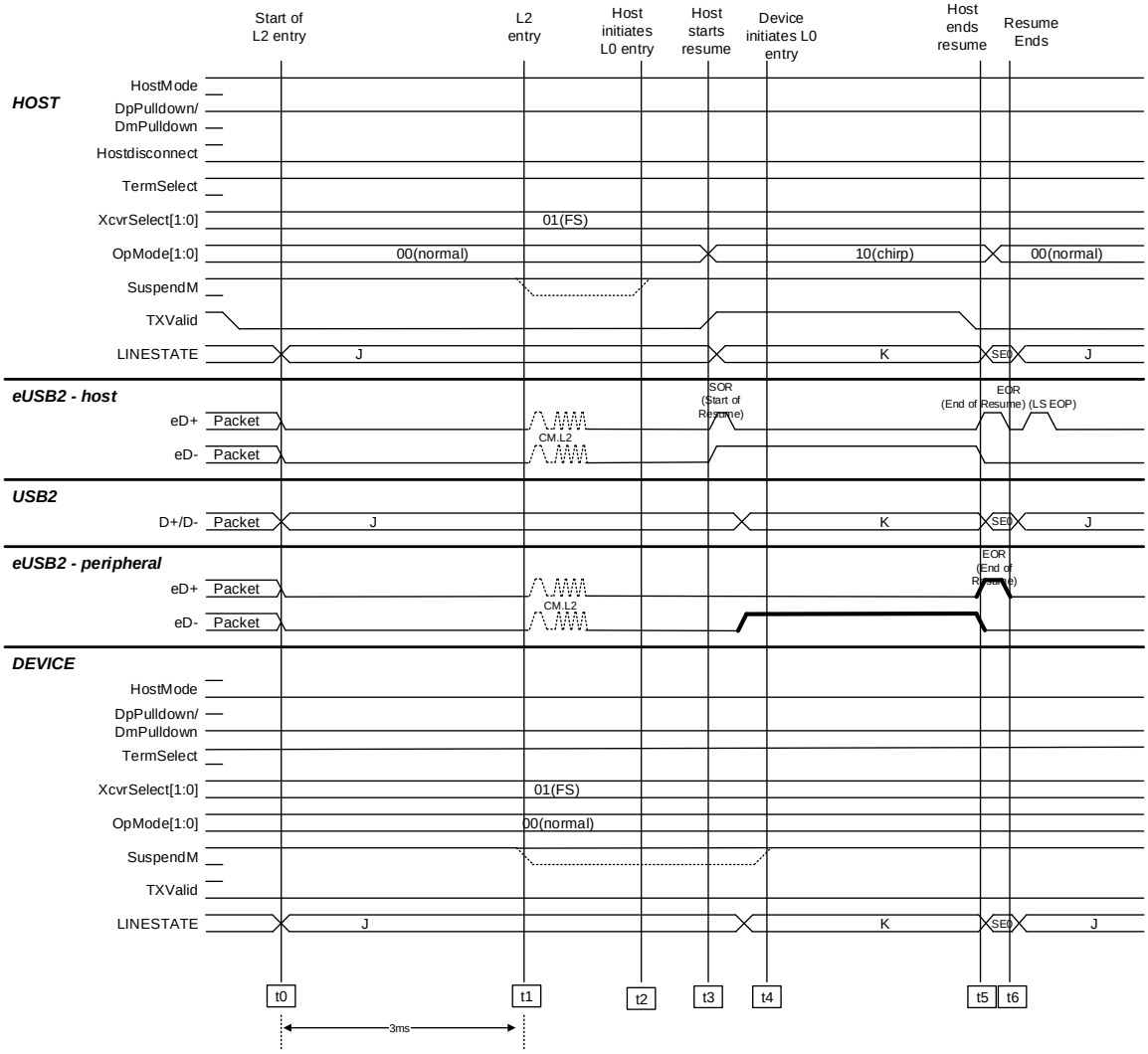


Figure 5-28: FS Link L2 entry and resume

t0:

- eDSPr initiates suspend, stops driving anything

on the line

t1:

- eDSPr and eUSPr declare bus suspend after 3ms
- Respective controllers may or may not assert suspendM
- If suspend asserted, eUSB port sends CM.L2 to its repeater

t2:

- eDSPr controller initiates L0 entry

t3:

- eDSPr starts sending resume,
- eUSPh detects SE1 followed by logic ‘1’ on eD-; eUSPh stops FS mapping mode
- UDSP sends resume on USB lines after SE1 followed by logic ‘1’ on eD- is detected.
- eDSPp enters repeat mode after detecting K on USB lines and drives eD- to logic ‘1’
- eUSPr changes linestate to K

t4:

- eUSPr controller de-asserts suspend if required

t5:

- eDSPr ends resume with EOResume
- eDSPp exits repeat mode after observing EOP on USB lines and sends EOP on eD+ line

t6:

- resume completes

5.5.14 **LS Link wake and resume from L2**

Link exiting L2 with a peripheral wake and host resume is shown in Figure 5-29.

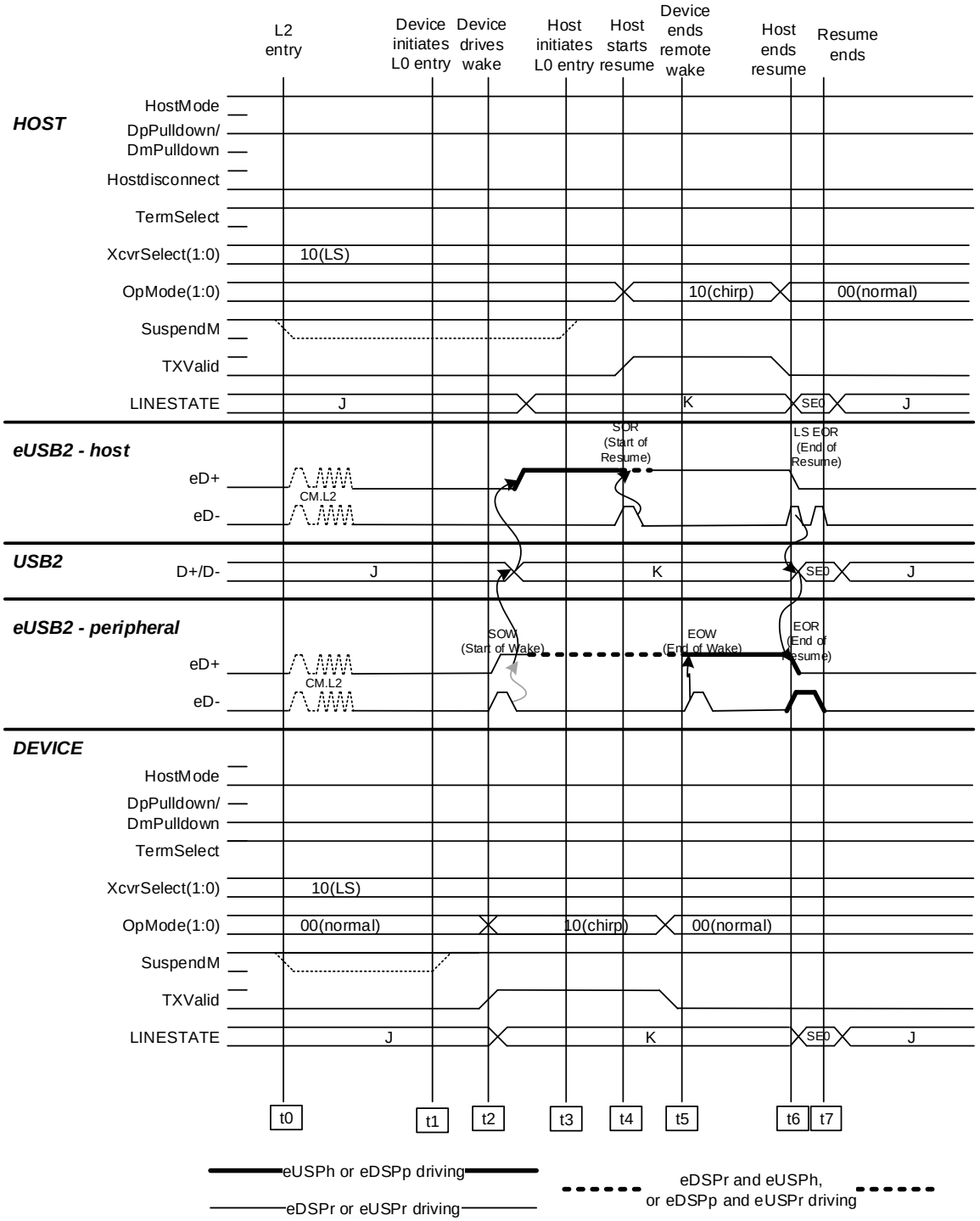


Figure 5-29: LS device wake and host resume

t0:

- Link in L2

t1:
- eUSPr controller initiates L0 entry

t2:
- eUSPr starts sending remote-wakeup
- eDSPp detects SE1 followed by a logic ‘1’ on eD+, detects it as a remote-wake signal; UUSP sends remote-wake on USB lines
- eDSPp remains in LS mapping mode and maps K on USB lines as a driven logic ‘1’ on eD+
- eUSPh enters repeat mode after detecting a K on the USB lines and drives eD+ to logic ‘1’
- eDSPr reflects it as resume K on its linestate output; after observing linestate change from J to K

t3:
- eDSPr initiates L0 entry

t4:
- eDSPr starts sending resume
- eUSPh detects SE1 followed by logic ‘1’ on eD+; eUSPh stops repeating mode.
- Note: eD+ is now driven by both eDSPr and eUSPh.
- UUSP sends resume on USB lines after SE1 followed by logic ‘1’ on eD+ is detected.

t5:
- eUSPr stops sending remote-wakeup
- eDSPp after detecting a logic ‘0’ to logic ‘1’ on eD-, stops LS mapping mode and enters repeating mode
- UDSP stops driving K on USB lines
- eDSPp sends K on USB lines in repeating mode on eD+ lines

t6:
- eDSPr ends resume with EOResume
- eDSPp exits repeat mode after observing EOP on USB lines and sends EOP on eD- line

t7:
- resume completes

5.5.15 **FS Link wake and resume from L2**

Link exiting L2 with a peripheral wake and host resume is shown in Figure 5-30.

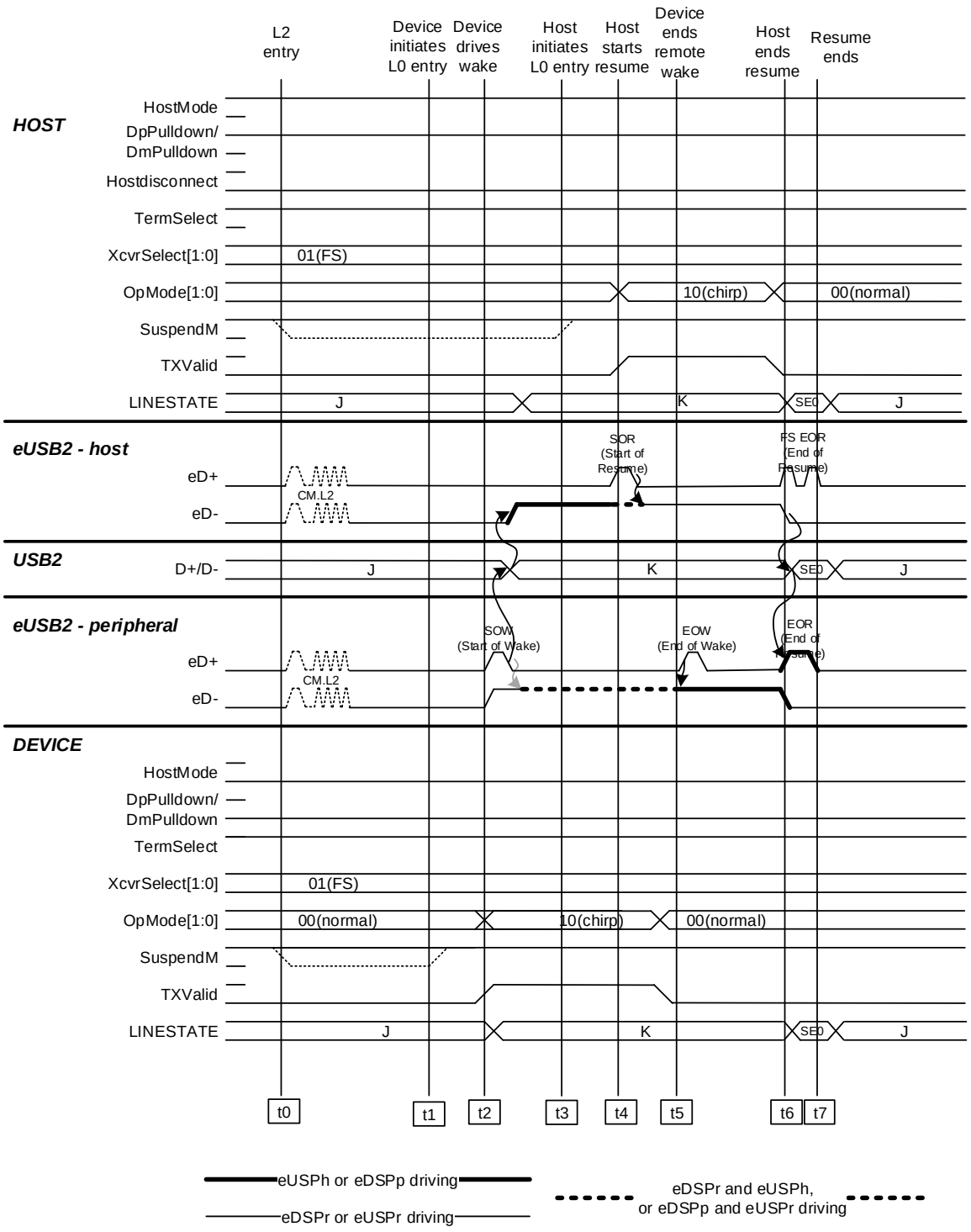


Figure 5-30: FS device wake and host resume

t0:

- Link in L2

t1:
- eUSPr controller initiates L0 entry

t2:
- eUSPr starts sending remote-wakeup
- eDSPp detects SE1 followed by a logic ‘1’ on eD-, detects it as a remote-wake signal; UUSP sends remote-wake on USB lines
- eDSPp remains in FS mapping mode and maps K on USB lines as a driven logic ‘1’ on eD-
- eUSPh enters repeat mode after detecting a K on the USB lines and drives eD- to logic ‘1’
- eDSPr reflects it as resume K on its linestate output; after observing linestate change from J to K

t3:
- eDSPr initiates L0 entry

t4:
- eDSPr starts sending resume
- eUSPh detects SE1 followed by logic ‘1’ on eD-; eUSPh stops repeating mode.
- Note: eD- is now driven by both eDSPr and eUSPh.
- UUSP sends resume on USB lines after SE1 followed by logic ‘1’ on eD- is detected.

t5:
- eUSPr stops sending remote-wakeup
- eDSPp after detecting a logic ‘0’ to logic ‘1’ on eD+, stops FS mapping mode and enters repeating mode
- UDSP stops driving K on USB lines
- eDSPp sends K on USB lines in repeating mode on eD- lines

t6:
- eDSPr ends resume with EOResume
- eDSPp exits repeat mode after observing EOP on USB lines and sends EOP on eD+ line

t7:
- resume completes

5.5.16 **FS Link wake without resume from L2**

Figure 5-31 illustrates the scenario where a device initiates a wake from L2, however, host resume is not triggered.

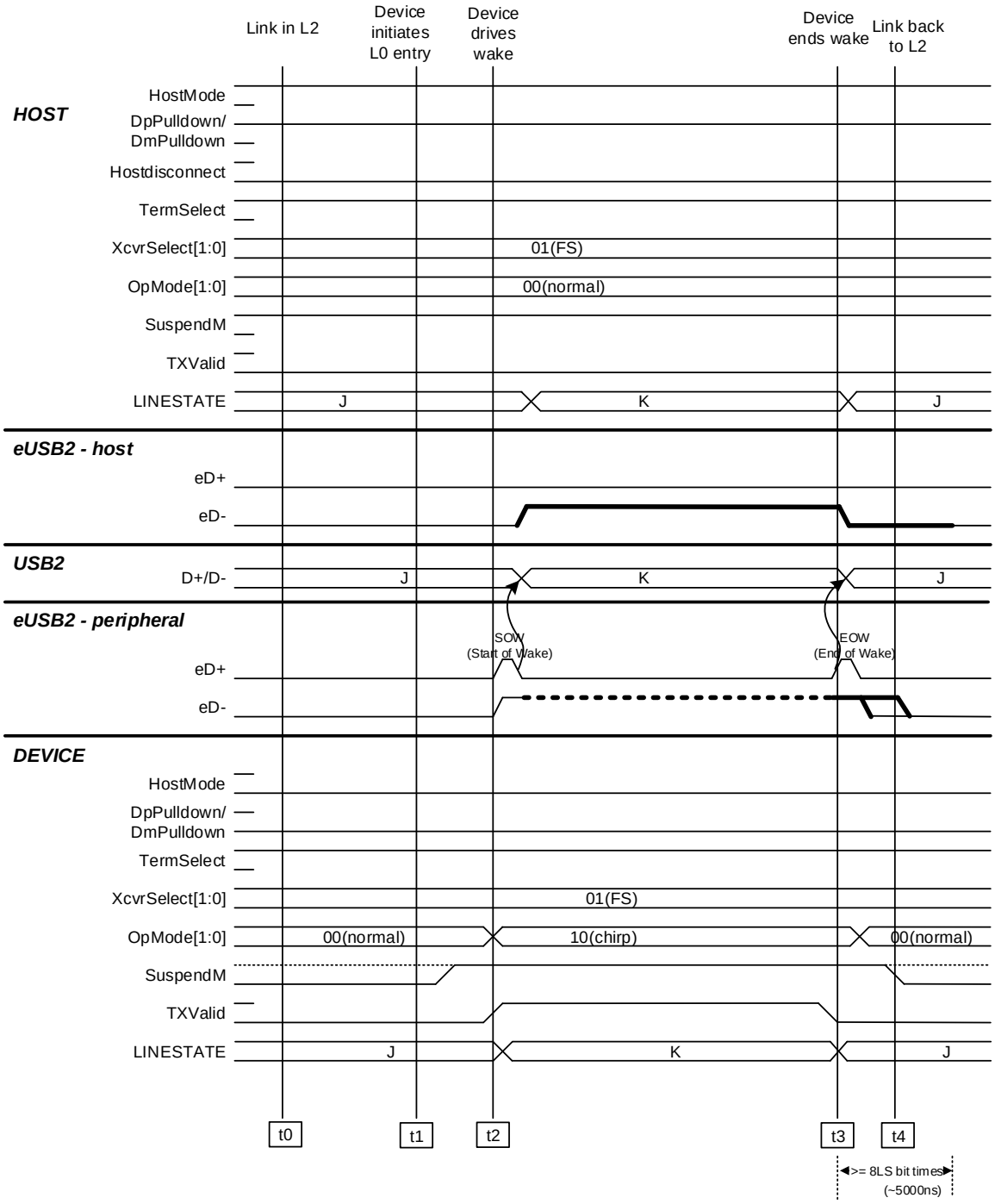


Figure 5-31: FS Link device wake without host resume

t0-t2:

- Link in L2 with eUSPr initiates L0 entry with remote wake.

t3:

- eUSPr stops sending remote-wakeup
- UDSP stops driving K on USB lines
- eDSPp enters FS mapping mode, and maps USB J as driven SE0 on eUSB lines. Note: K may continue to be presented on eD- after the completion EOWake before transition to J. In this case, the K to J transition shall not be declared as a host resume instead it shall be a K to SE0 (EOResume).
- eUSPh keeps forwarding J on USB lines assuming this being a data J state. It starts a non-activity timer (>8LS bit times)

t4:

- eUSPh non-activity timer expires where it determines this being an end of remote wake without host resume.
- eUSPh stops driving eD- line and transition back to L2

5.5.17 **HS Link L2 entry and resume**

HS link L2 entry and resume sequences are illustrated in Figure 5-32 below.

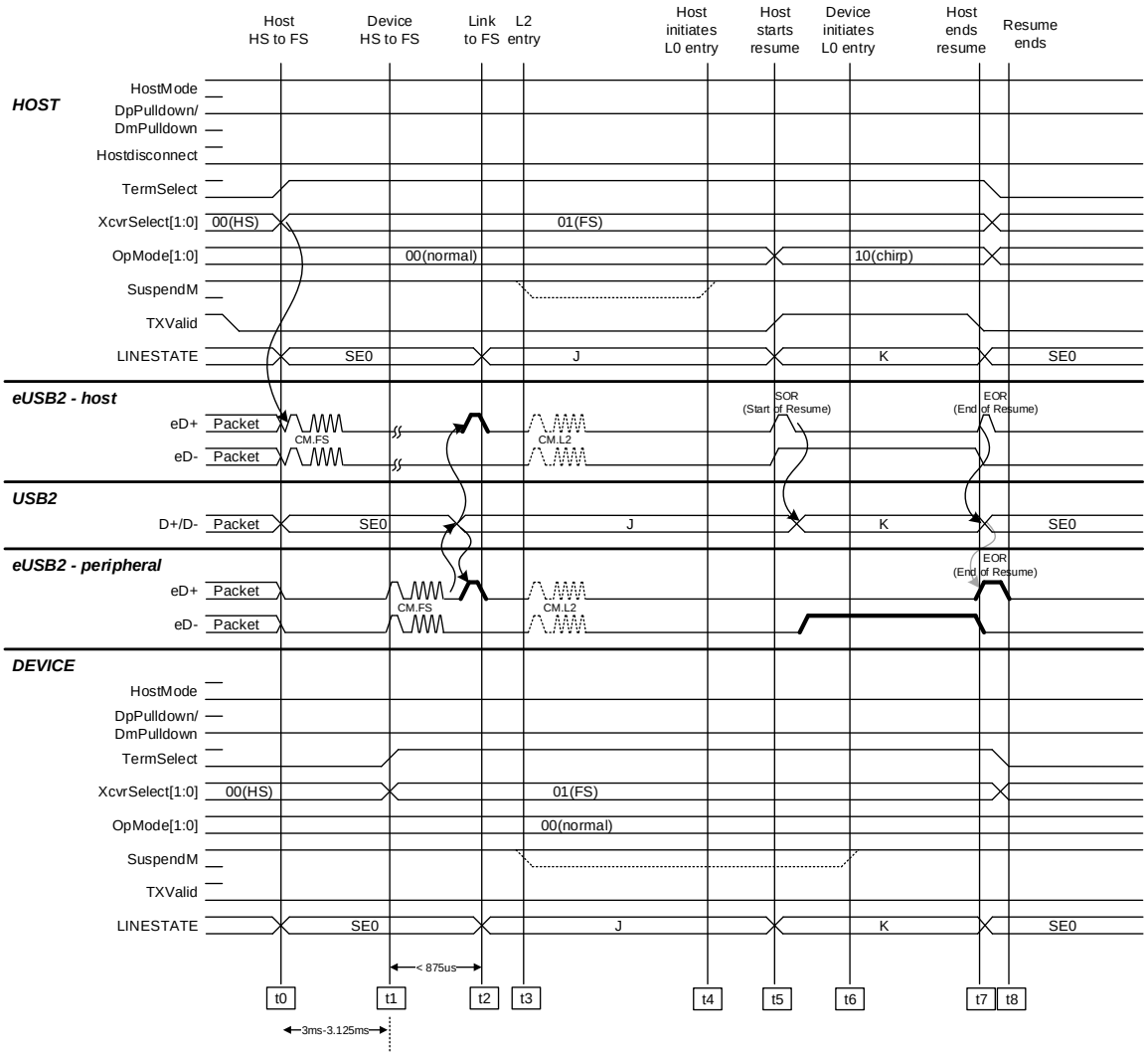


Figure 5-32: HS Link L2 entry and resume

t0:
- eDSPr initiates suspend, sends CM.FS, starts 4ms timer
- Host repeater at its UDSP removes HS terminations

t1:
- eUSPr sends CM.FS after 3ms to check for reset or suspend
- Peripheral repeater starts $T_{PR\_HS\_RESET\_TO\_FS}$ timer and at its UUSP removes HS terminations and apply J pull-up. During this time, the peripheral repeater shall disable HS repeating but remain in HS mapping at eDSPp.

t2:
- Peripheral repeater detected Idle J at UUSP before $T_{PR\_HS\_RESET\_TO\_FS}$ expired indicating suspend entry and sends a pulse to eUSPr and enter FS mapping.
- eUSPr changes linestate to J
- eUSPh also sends a pulse to eDSPr in case it observes J pull up; eUSPh enters FS mapping mode
- eDSPr changes linestate to J, eDSPr stops 4ms timer

t3:
- eDSPr controller may or may not assert suspend; eDSPr sends CM.L2 if suspendM asserted
- eUSPr controller may or may not assert suspend; eUSPr sends CM.L2 if suspendM asserted

t4:
- eDSPr controller initiates L0 entry

t5:
- eDSPr starts sending resume,
- eUSPh detects SE1 followed by logic ‘1’ on eD-; eUSPh stops FS mapping mode
- UDSP sends resume on USB lines after SE1 followed by logic ‘1’ on eD- is detected.
- eDSPp enters repeat mode after detecting K on USB lines and drives eD- to logic ‘1’
- eUSPr changes linestate to K

t6:
- eUSPr controller de-asserts suspend if required

t7:
- eDSPr ends resume with EOResume
- eDSPp exits repeat mode after observing EOP on USB lines and sends EOP on eD+ line
- eDSPp and eUSPh both enter HS mode within 2LS bit times

t8:
- resume completes

5.5.18 **HS Link wake and resume from L2**

Link exiting L2 with a peripheral wake and host resume is shown in Figure 5-33.

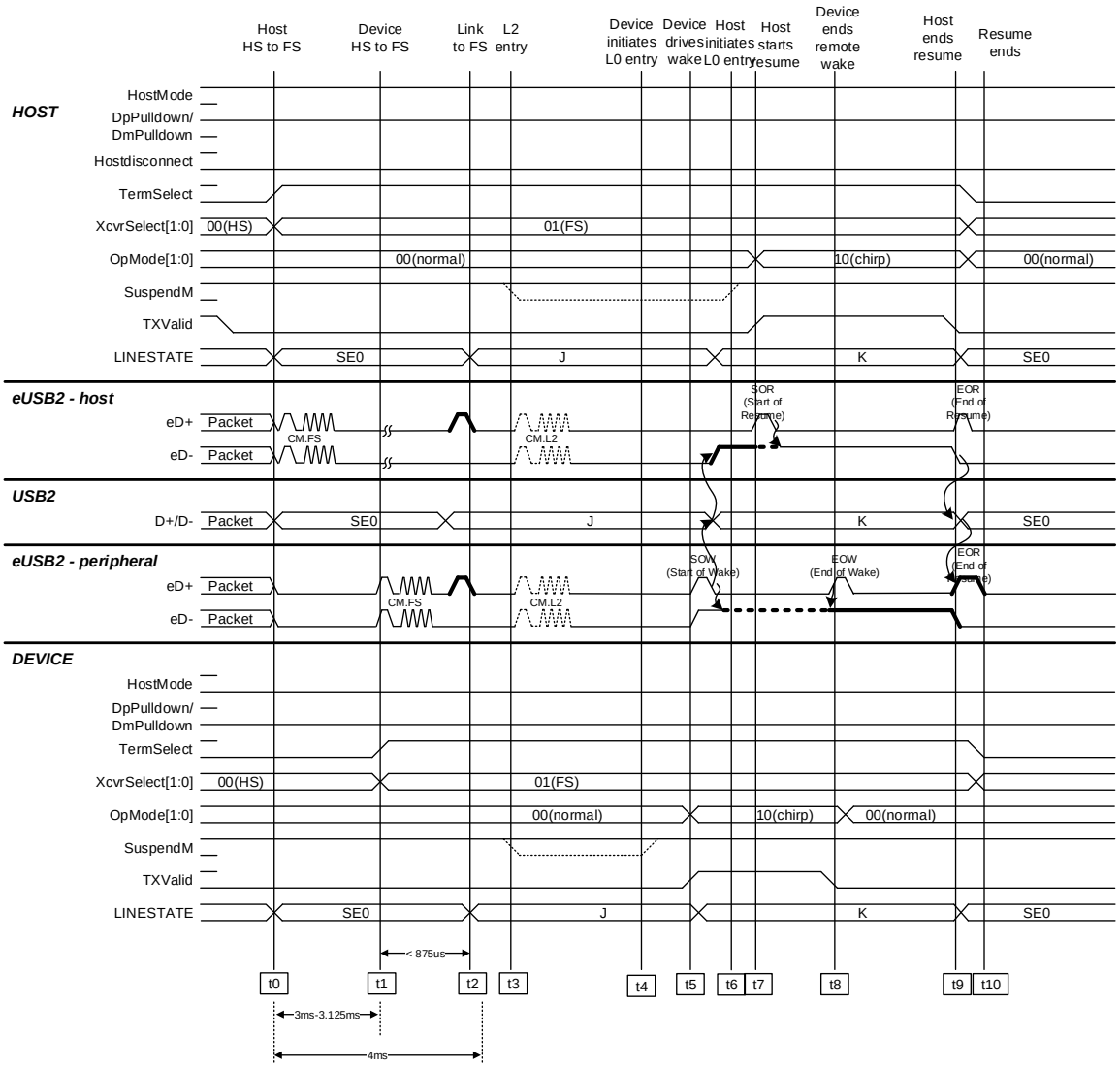


Figure 5-33: HS Link device wake and host resume

t0-t3:

- HS Link L2 entry.

t4:

- eUSPr controller initiates L0 entry

t5:

- eUSPr starts sending remote-wakeup
- eDSPp detects SE1 followed by a logic ‘1’ on eD-, detects it as a remote-wake signal; UDSP sends remote-wake on USB lines
- eDSPp remains in FS mapping mode and maps K on USB lines as a driven logic ‘1’ on eD-
- eUSPh enters repeat mode after detecting a K on the USB lines and drives eD- to logic ‘1’

- eDSPr reflects it as resume K on its linestate output; after observing linestate change from J to K

t6:

- eDSPr initiates L0 entry

t7:

- eDSPr starts sending resume
- eUSPh detects SE1 followed by logic ‘1’ on eD-; eUSPh stops repeating mode
- UDSP sends resume on USB lines after SE1 followed by logic ‘1’ on eD- is detected.

t8:

- eUSPr stops sending remote-wakeup
- eDSPp after detecting a logic ‘0’ to logic ‘1’ on eD+, stops FS mapping mode and enters repeating mode
- UDSP stops driving K on USB lines
- eDSPp sends K on USB lines in repeating mode on eD- lines

t9:

- eDSPr ends resume with EOResume
- eDSPp exits repeat mode after observing EOP on USB lines and sends EOP on eD+ line
- eDSPp and eUSPh both enter HS mode within 2LS bit times

t10:

- resume completes

5.5.19 **HS Link wake and without resume from L2**

Figure 5-34 illustrates the scenario where a device initiates a wake from L2, however, host resume is not triggered

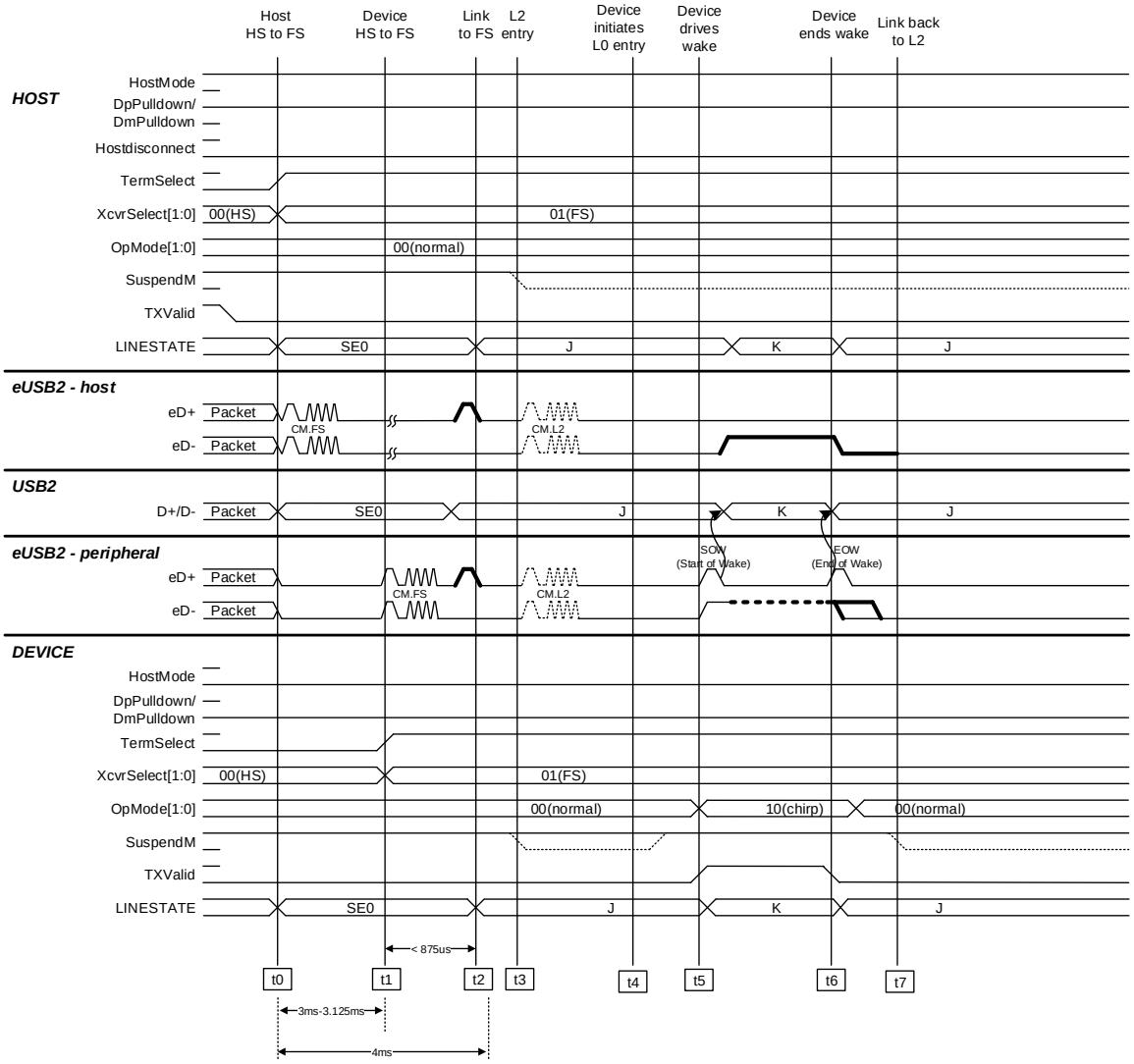


Figure 5-34: HS Link device wake without host resume

t0-t4:

- HS Link L2 entry.

t5:

- eUSPr initiates remote-wakeup.

t6:

- eUSPr stops sending remote-wakeup
- UDSP stops driving K on USB lines
- eDSPp enters FS mapping mode, and maps USB J as undriven SE0 on eUSB lines. Note: K may continue to be presented on eD- after the completion EOWake before transiting to Idle J. In this case, the K to J transition shall not be declared as a host resume (host resume shall be a K to SE0 EOResume).
- eUSPh keeps forwarding J on USB lines as a data J. it starts a non-activity timer (>8LS bit times).

t7:

- eUSPh non-activity timer expires; it stops driving eD- line and moves back to FS mapping mode.
- Link back to L2

5.5.20 **HS Link disconnect during L2 entry**

Figure 5-35 illustrates the scenario where a device is disconnected during L2 entry.

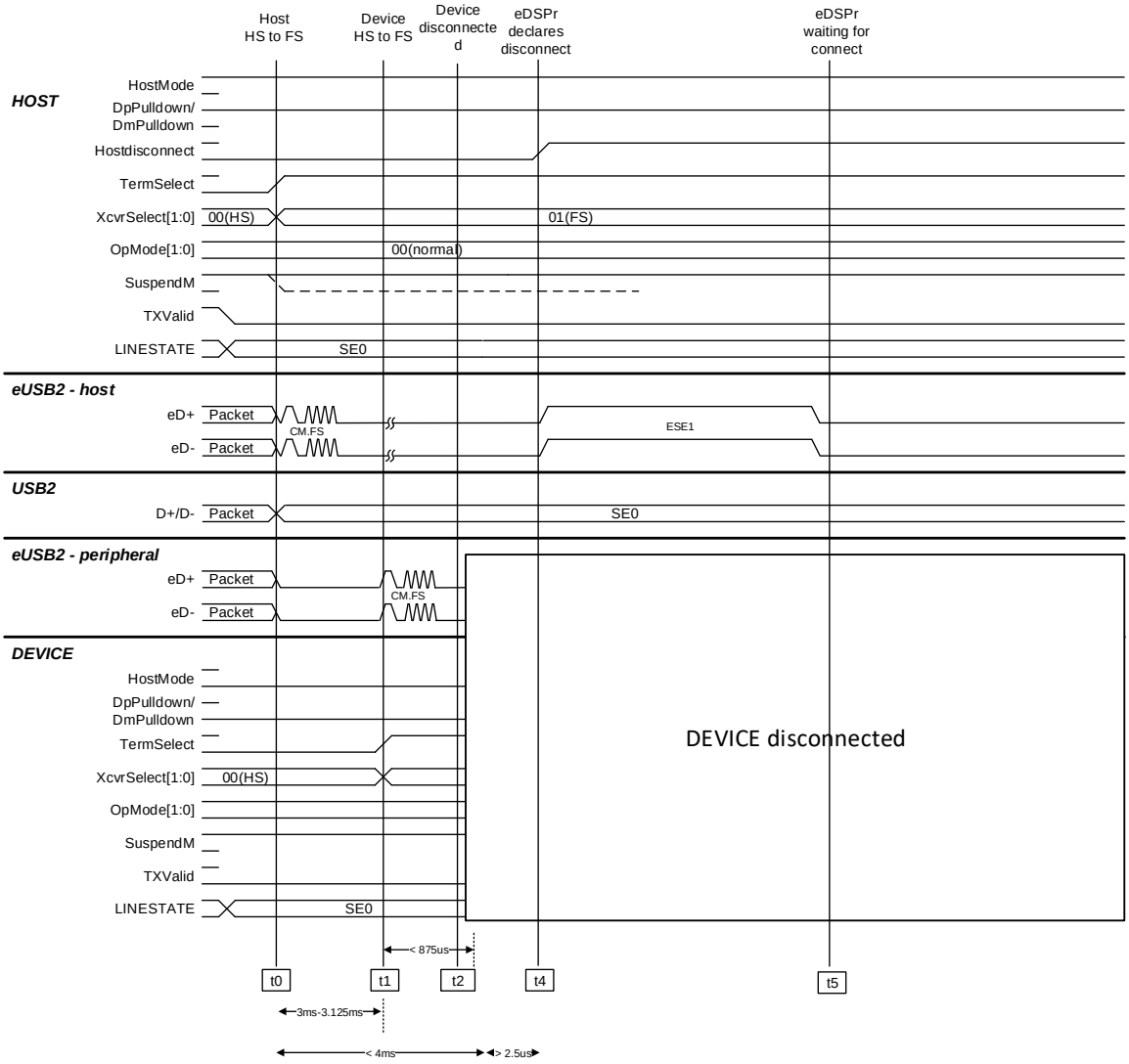


Figure 5-35: HS Link disconnect during L2 entry

t0:

- eDSPr initiates suspend, sends CM.FS, starts 4ms timer.
- eUSPh directs its UDSP to remove HS terminations.

t1:

- eUSPr sends CM.FS after 3ms to check for reset or suspend.
- eDSPp directs its UUSP to remove HS terminations and apply J pull up.

t2:

- Peripheral disconnected on USB lines before a J pull could be applied

t3:

- UDSP never sees a J, thus eUSPh never sends a pulse; eUSPh is not completely in FS mode, thus it is not performing any disconnect detection
- After 4ms, disconnect recovery timer is complete. eDSPr observes the linestate as SE for more than 2.5us and declares disconnect, eDSPr also sends ESE1 to eUSPh

t4:

- eDSPr waiting for a connect from eUSPh

5.5.21 **HS Link disconnect in L2 (before CM.L2)**

Figure 5-36 illustrates the scenario where a device is disconnected in L2 entry before the CM.L2.

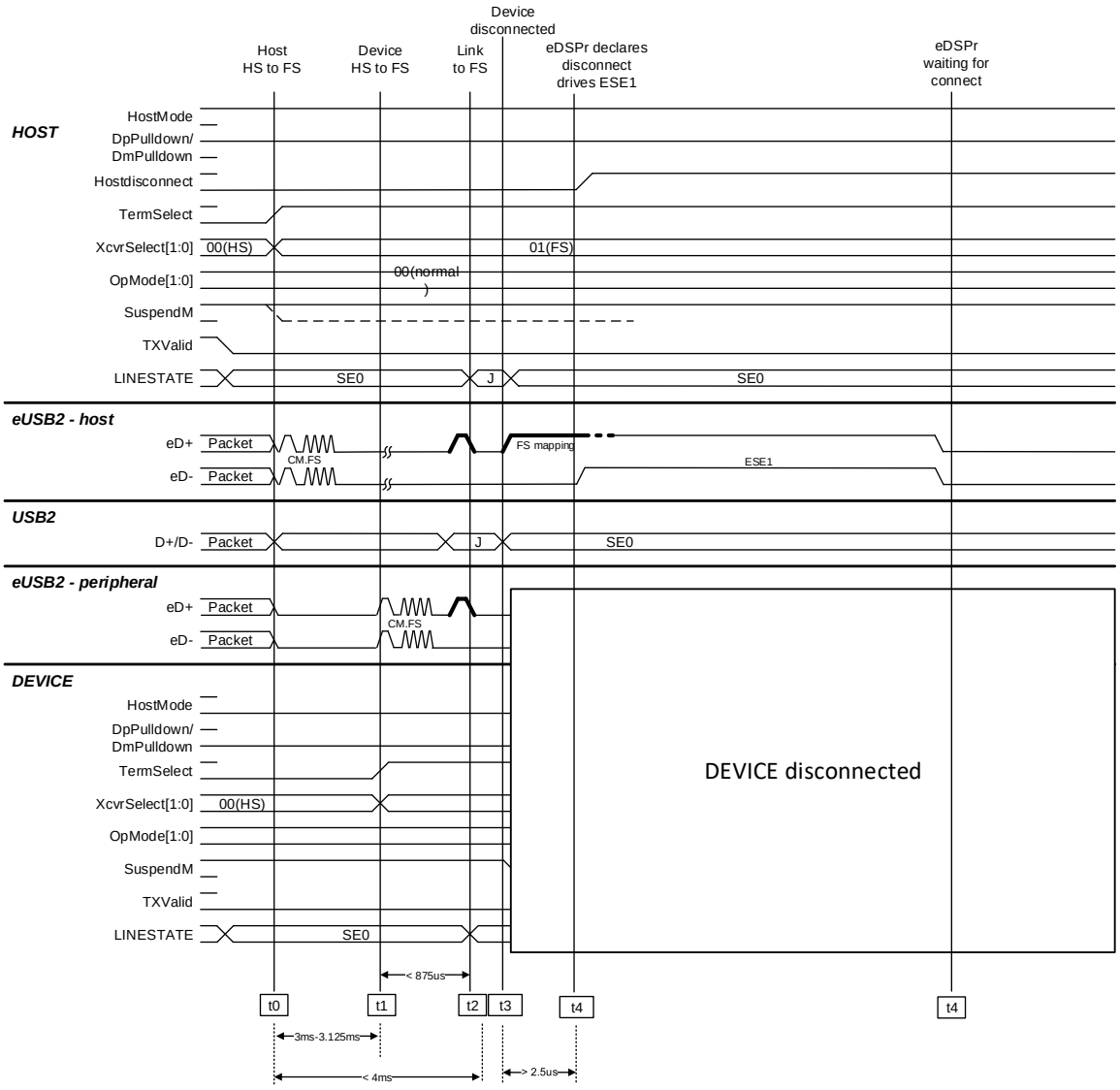


Figure 5-36: HS Link disconnect in L2 entry (before CM.L2)

t0:

- eDSPr initiates suspend, sends CM.FS, starts 4ms timer.
- eUSPh directs its UDSP to remove HS terminations.

t1:

- eUSPr sends CM.FS after 3ms to check for reset or suspend.
- eDSPp directs its UUSP to remove HS terminations and apply J pull up.

t2:

- UDSP sees a J, thus eUSPh sends a pulse; eUSPh enters FS mode, enables its FS mapping.
- eDSPr receives pulse, disables its 4ms timer, changes linestate to J.

t3:

- Peripheral disconnected on USB lines; eUSPh drives eD+ to ‘1’ based on FS mapping.

- eDSPr receives a ‘1’ on eD+, changes linestate to SE0, asserts hostdisconnect, drives ESE1.

t4:

- eDSPr waiting for a connect from eUSPh.

5.5.22 **HS Link disconnect in L2 (during CM.L2)**

Figure 5-37 illustrates the scenario where a device is disconnected in L2 entry after the CM.L2.

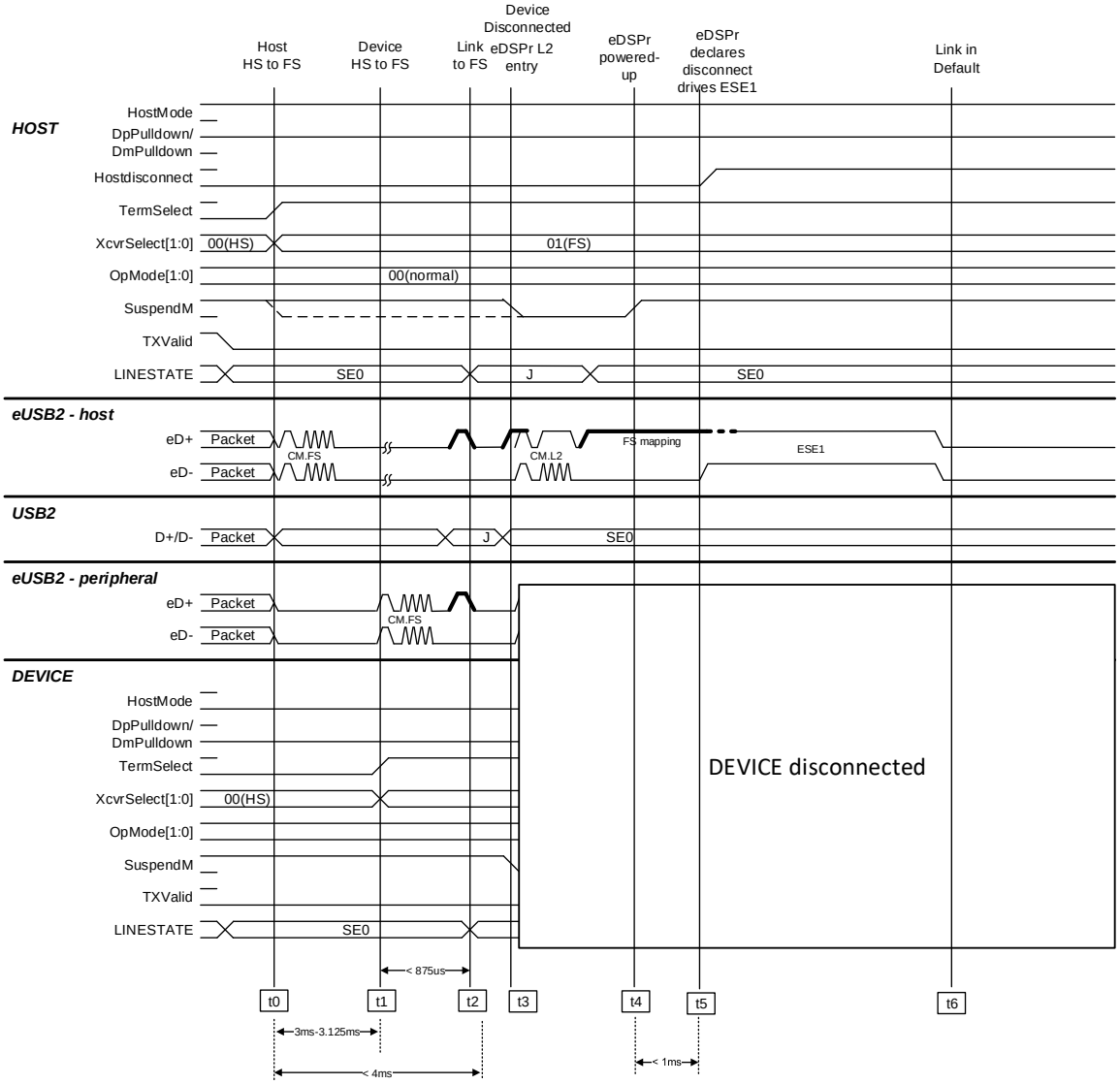


Figure 5-37: HS Link disconnect in L2 entry (during CM.L2)

t0:

- eDSPr initiates suspend, sends CM.FS, starts 4ms timer
- eUSPh directs its UDSP to remove HS terminations

t1:

- eUSPr sends CM.FS after 3ms to check for reset or suspend.
- eDSPp directs its UUSP to remove HS terminations and apply J pull up.

t2:

- UDSP sees a J, thus eUSPh sends a pulse; eUSPh enters FS mode, enables its FS mapping.

- eDSPr receives pulse, disables its 4ms timer, changes linestate to J.

t3:

- eDSPr controller observes J and asserts suspend.
- eDSPr sends CM.L2.
- Device disconnect occurs the same time as CM.L2. Hence, CM.L2 coincide with logic ‘1’ on eD+ (indicating SE0 on D+/D-).
- eUSPh stops driving logic ‘1’ on eD+ to service CM.L2 (observes SE1 SCM of CM.L2).
- eUSPh redrives logic ‘1’ on eD+ indicating device disconnect.

t4:

- eDSPr exits L2 as directed by its controller to service device disconnect.

t5:

- eDSPr transmit ESE1 to its associated repeater as Port Reset.

t6:

- Link transition to Default for reconfiguration.

6 Register Access Protocol

The register access protocol (RAP) is optional. It is defined for control and configuration in the following two operation modes:

- In repeater mode, for an eDSPr/eUSPr to access the register space in its associated repeater.
- In native mode, for an eDSPn to access the register space in an eUSB2 peripheral port.

Given that register access protocol (RAP) is optional, it is the system architecture and implementation to ensure if RAP is required, hence both the eDSPr/eUSPr and its associated repeater (in repeater mode) or eDSPn and eUSPn (in native mode) support this feature.

In the event of transmitting back-to-back CM.RAP, the port shall allow an idle time T_{CMB2B} (end to start) between the CMs.

The RAP bus is a point to point interconnect based on eD+ and eD-. The RAP clocking architecture is forwarded clock. The electrical requirement of the RAP is compatible with LS/FS operation defined in Chapter 6.
The RAP supports 6-bit addressing based on 2-bit command for the following byte operations:

- Read: single-byte read.
- Write: single byte write.
- Set: to perform bit-wise logic “OR” with the registered data.
- Clear: to perform bit-wise reset to the registered data with the mask.

6.1 *RAP Bus Definition and Operation*

An example RAP configuration is shown in Figure 6-1. A RAP initiator is a port initiating the register access, and it is always implemented in an eUSB2 port. A RAP receptor is a port that has its register space implemented, and it is either implemented in an eUSB2 device, or in an eUSB2 repeater.

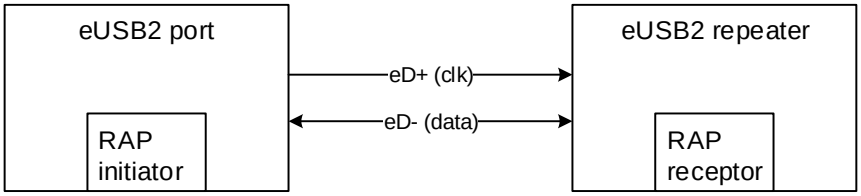


Figure 6-1: RAP Block Diagram

The RAP bus shares the eUSB2 bus. Therefore, the RAP can only be initiated when the bus is idle and no eUSB2 traffic is expected during the period of operation. The RAP shall be initiated upon power up in Default and before Port/Repeater Configuration only.

Note that it is the responsibility of the RAP initiator to manage the RAP operation without contending with the eUSB2 operation. The policy of the RAP initiation and contention avoidance is out of the scope of this document.
As shown in Figure 6-1, RAP bus is constructed based on eD+/eD-. eD+ is repurposed to carry the forwarded clock. eD- is repurposed to carry half-duplex bi-directional data. The bus clocking and operation shall meet the following requirements:

- A RAP initiator shall supply a forwarded clock to a RAP receptor for data sampling, command decoding and its associated data processing.
- The RAP bus clocking shall be based on single data rate with the data transmitted on the rising edge of the clock and received and sampled on the falling edge of the clock. This is

true irrespective of whether it is a RAP initiator or RAP receptor. (Refer to section 5.3 for timing requirements).

- The data bus turnaround time for data read shall be between three to sixty-four clock cycles. A RAP receptor shall first drive one cycle of logic '1' and follow with the data.
- The transmission of the RAP shall start with CM.RAP and follow with the RAP command, the register address, and if the command is read, write, clear or set the data. The bit order shall be least significant bit first. Shown in Figure 6-2 is a general RAP format.
- For write operation, the RAP initiator shall drive logic '0' at eD- for two clock cycles after the last bit of data (d7).
    - Note: Although some operations may not need two clock cycles, two clock cycles are required for all CM.RAP for consistent implementation.
- For read operation, the RAP initiator shall drive logic '0' at eD- for one clock cycle after the last bit of address (a5) is transmitted before switching to pull-down. The RAP receptor shall drive logic '0' at eD- for one clock cycle after the last bit of data (d7) is transmitted before disabling its transmitter with the second clock cycle.
- For back to back RAP operation, the RAP initiator shall have a minimum of two cycle idle time.
- The timing of CM.RAP shall be based on $T_{CM\_UI\_Lx}$ if the link is in Lx, or $T_{CM\_UI\_L0}$ otherwise.

CM.RAP	Address						Data							
CM.15	a0	a1	a2	a3	a4	a5	d0	d1	d2	d3	d4	d5	d6	d7

Figure 6-2: RAP Format

6.2 *RAP Command and Features*

The RAP supports four register operation defined in Table 6-1.

Table 6-1: The RAP Command Definition

CMD (b1~0)	Operation	Description
00	Write	Data is written to the register address
01	Read	Data is read from the register address
10	Clear	Active high bit-wise clear with the data on the register address.
11	Set	Bit-wise OR with the data on the register address

An example of a write operation is shown in Figure 6-3.

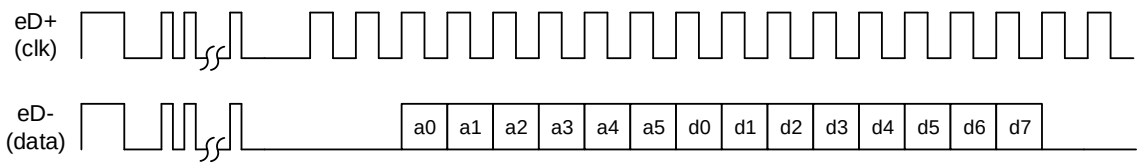


Figure 6-3: RAP Format: Write

An example of a read operation in shown in Figure 6-4.

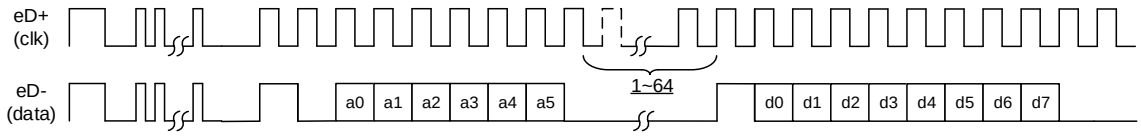


Figure 6-4: RAP Format: Read

An example of a clear operation in shown in Figure 6-5.

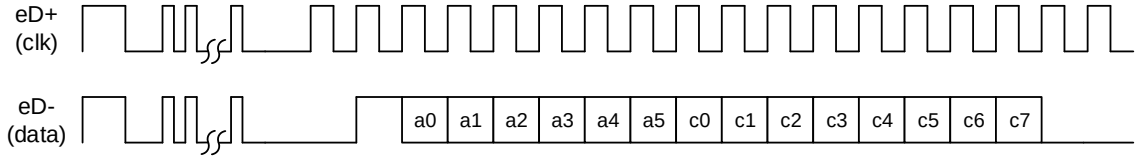


Figure 6-5: RAP Format: Clear

An example of a set operation in shown in Figure 6-6.

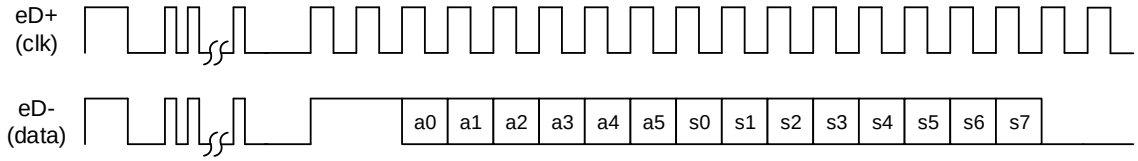


Figure 6-6: RAP Format: Set

6.3 *RAP Timing Requirement*

Shown in Figure 6-7 and Figure 6-8 are definitions of RAP Initiator and Receptor timing respectively. The values of the parameters are listed in Table 6-2.

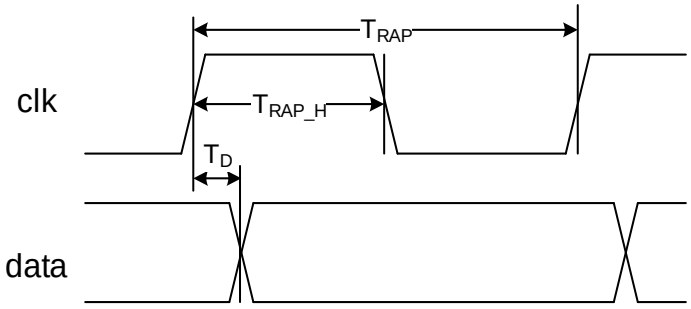


Figure 6-7: Transmitter Timing at RAP Initiator and Receptor

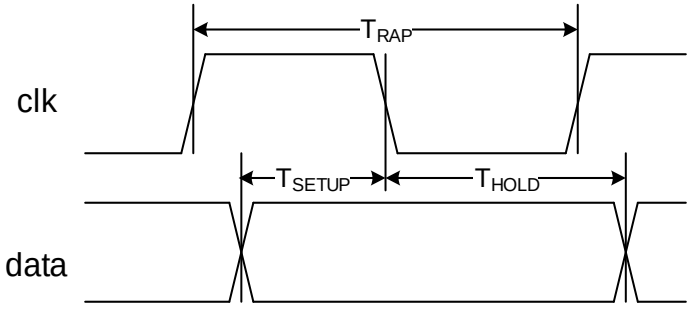


Figure 6-8: Receiver Timing at RAP Initiator and Receptor

Table 6-2: The RAP Timing Specification

Parameters	Min	Max	Units
T_{RAP}		2	FS UI
T_{RAP_H}	1		FS UI
T_D	0	25	ns
T_{SETUP}	25		ns
T_{HOLD}	25		ns

7 Electrical Specifications

This chapter describes the electrical specification of eUSB2.

7.1 *High-speed*

Figure 7-1 shows an example of an eUSB2 transceiver circuit. R_{SRC_HS} is the transmitter source termination. V_{TX_DIF} is the peak differential swing across the Tx eD+ and eD- pads. R_{RCV_DIF} represents the optional receiver differential termination. C_{RX_CM} is an on-die capacitor, which is recommended to suppress AC common mode fluctuation seen by the receiver. The fact that eUSB2 is a half-duplex interconnect where transmitter and receiver share the pad are omitted from the drawing in Figure 7-1.

The high-speed transceiver implements low swing differential signaling. The transmitter is required to be source terminated to deliver good signal integrity. The receiver could be differentially terminated or un-terminated. The requirement for receiver termination depends on the use case and channel characteristics. Receiver termination is a requirement for repeater mode of operation but optional for native mode.

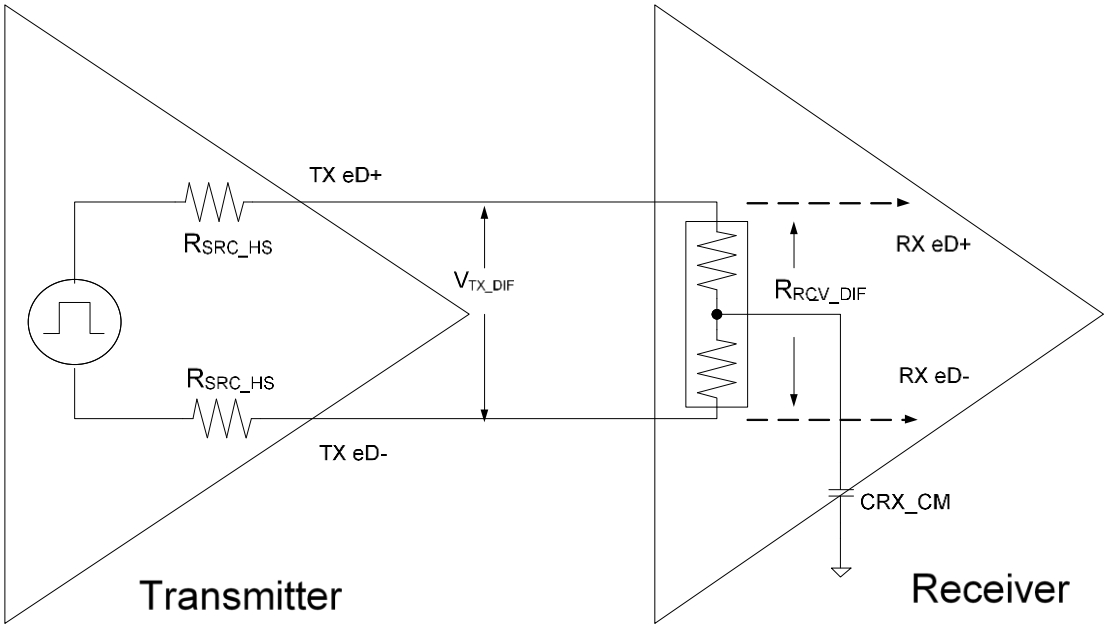


Figure 7-1: Example eUSB2 Transmitter and Receiver Circuit Structure

It is important to constrain the source impedance mismatch, ΔR_{SRC}, between Tx eD+ and eD-. The mismatch will manifest itself into common mode voltage variation which impacts both receiver functionality and system EMI performance.

The eUSB2 receiver circuit is required to extract the clock information from the incoming data stream and perform data recovery. There is no requirement to implement common clocking architecture for 2 eUSB2 devices. The clock source inaccuracy shall be less than +/- 500 ppm as defined in USB2.0. Spread spectrum clocking is not allowed.

The squelch circuit is implemented as an amplitude envelope detection circuit to differentiate between valid signal and wire noise. It is also used by the repeater to perform data traffic flow control. Therefore, a robust squelch circuit design is critical to guarantee correct functionality.

7.1.1 High-speed Tx Electrical Specification

This section describes values at the TX pad.

Table 7-1: High-speed Transmitter DC Specifications

Parameter	Symbol	Min	Typ	Max	Units	Notes
Transmit differential (terminated)	$V_{TX\_DIF\_TERM}$	165		245	mV	1,5
Transmit differential (un-terminated)	$V_{TX\_DIF\_UNTERM}$	360		440	mV	2,5
Transmit common mode	V_{TX_CM}	170		230	mV	3,6
Transmit source termination impedance	R_{SRC_HS}	32	40	48	Ω	6
Source impedance mismatch	ΔR_{SRC_HS}			4	Ω	4,5

Notes:

1) The transmitter must maintain the specified differential swing after accounting for the transmit voltage supply and source termination variation at both eD+ and eD-. An ideal 80Ω Rx differential termination is used as the test load.
2) The transmitter must maintain the specified differential swing after accounting for the transmit voltage supply and source termination variation at both eD+ and eD-, an 80kΩ differential termination is used as the test load.
3) The specified number does not include AC noise component.
4) The source impedance mismatch between eD+ and eD- shall not vary more than the specified max value. This impedance mismatch could result from process random variation, systematic layout offset and other sources of error.
5) The specified numbers are Informative.
6) The specified numbers are Normative.

Table 7-2: High-speed Transmitter AC Specifications

Parameter	Symbol	Min	Typ	Max	Units	Notes
Transmit CM AC (50MHz-480MHz)	$V_{TX\_CM\_AC}$			30	+/- mV_{PEAK}	1,3
Transit rise and fall time (20%-80%)	$T_{RISE\_FALL\_TRM}$	100			ps	1,3
Transmit rise/fall mismatch				25	%	1,2

Notes:

1) Defined under an ideal 80Ω Rx differential termination with maximum supply voltage variation.
2) Rise/fall mismatch = absolute delta of (rise – fall time) / (average of rise and fall time).
3) This parameter is informative, not normative.

7.1.2 High-speed Rx Electrical Specification

Table 7-3: High-speed Receiver DC Specifications

Parameter	Symbol	Min	Typ	Max	Units	Notes
Receive common mode range	V_{RX_CM}	120		280	mV	1,4
Receive center-tapped capacitance	C_{RX_CM}	15		50	pF	informative
Receive sensitivity (peak differential)	$V_{RX\_DIF\_SENS}$	60			+/- mV	4,5
Differential receiver termination	R_{RCV_DIF}	64	80	96	Ω	2,4
Differential receiver termination (repeater)		72	80	88	Ω	3,4
Squelch detect threshold (peak differential)	$V_{SQUELCH\_DIF}$	60		110	mV	4

Notes:

1) The number includes common mode variation due to Tx source impedance mismatch and GND shall be within 4% of VCC of each other at all times on both receive and transmit sites. However, it does not account for receiver AC common mode variation.
2) High-speed differential receiver termination for native mode operation only
3) A tighter termination tolerance is defined for repeater mode operation to minimize accumulated jitter when propagating downstream through the repeater.
4) This parameter is normative.
5) It is the minimum input amplitude a receiver can detect.

Table 7-4: High-speed Receiver AC Specifications

Parameter	Symbol	Min	Typ	Max	Units	Notes
Receiver AC common mode (50MHz-480MHz)	$V_{CM\_RX\_AC}$			60	+/-mVpk	informative

7.1.3 High-speed Signal Pad Capacitance Recommendation

Table 7-5: Capacitance (Informative)

Parameter	Symbol	Min	Typ	Max	Units	Note
Tx Pad Capacitance	C_{TX}			2.5	pF	
Rx Pad Capacitance	C_{RX}			2.5	pF	

7.1.4 **High-speed Channel Requirement**

Native mode and repeater mode channel topologies are shown in Figure 7-2 andFigure 7-3. The informative specifications are summarized in Table 7-6.

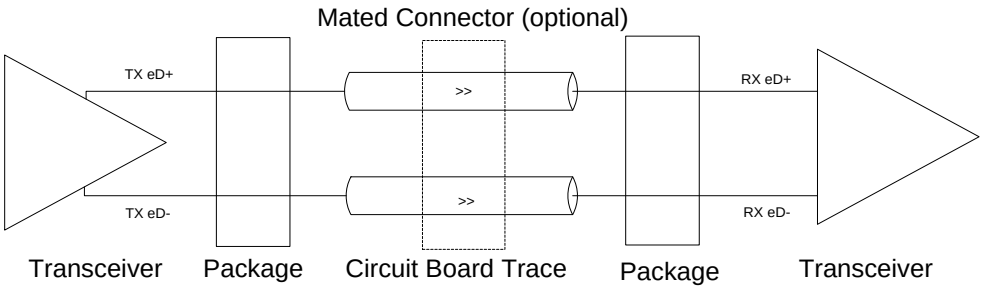


Figure 7-2: Native Mode Channel Topology

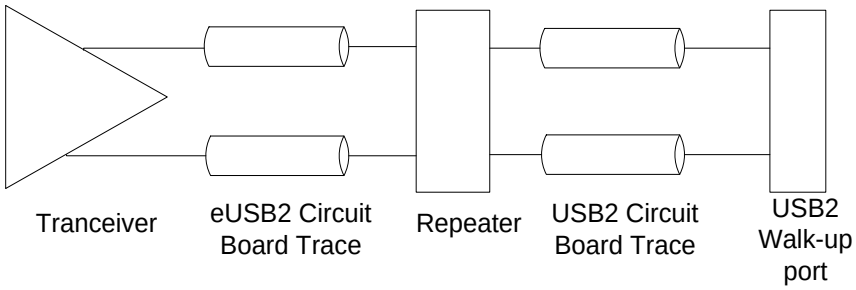


Figure 7-3: Repeater Mode Channel Topology

Table 7-6: Channel Specification (normative)

Parameter	Symbol	Min	Typ	Max	Units	Note
Trace Differential Impedance	Z_{DIFF}		85		Ω	
Trace Differential Impedance Tolerance	ΔZ_{DIFF}			15	%	
Host-to-device insertion loss, Native Mode	IL_{NATIVE}			-1.7	dB	1,2
Host-to-repeater insertion loss, Repeater Mode	IL_{H2RPT}			-1.2	dB	1,3
Repeater-to-connector insertion loss, Repeater Mode	$IL_{RPT2CON}$			-2	dB	1,3

Notes:

1) The number is specified at 240MHz frequency.
2) Refer to Figure 7-2 for the topology setup.
3) Refer to Figure 7-3 for the topology setup.

7.1.5 **High-speed Eye Diagram and Jitter Allocation**

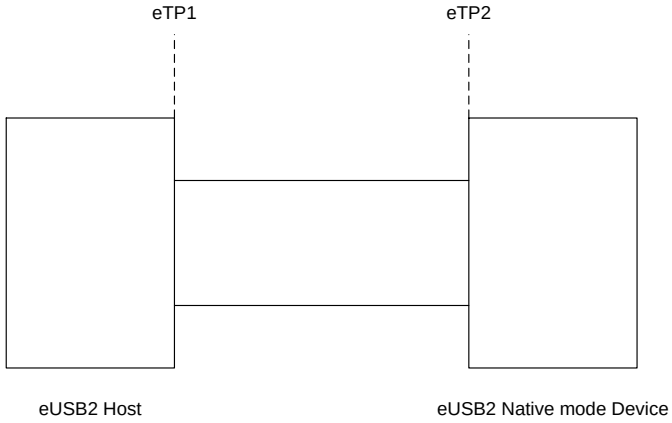


Figure 7-4: Measurement Plane for Native Mode

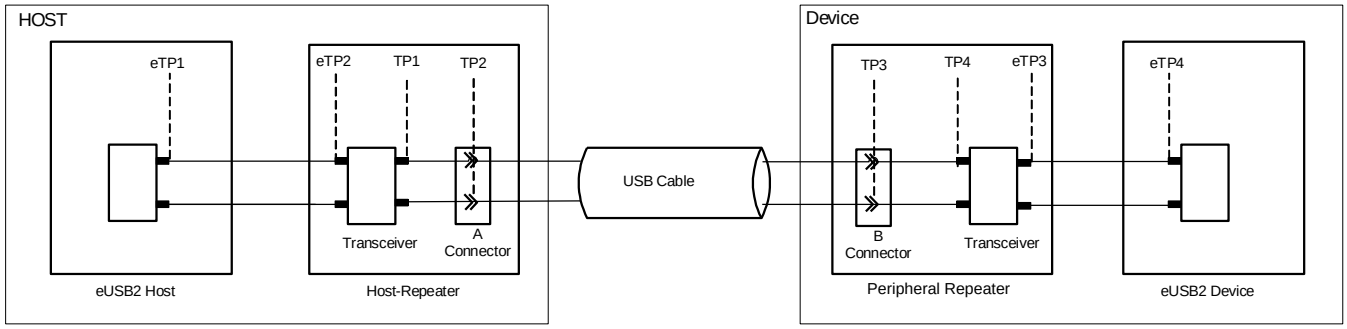


Figure 7-5: Measurement Plane for Repeater Mode

Figure 7-6 defines 4 additional test planes[1] eTP1, eTP2, eTP3 & eTP4. Definition of TP2 and TP3 remains the same as specified by USB2.0, section 7.1.2.2.

- eTP1 and eTP2 are the points where the IC pins of the eUSB2 Host and eUSB2 host repeater are respectively soldered to the circuit board.
- eTP3 and eTP4 are the points where the IC pins of eUSB2 Repeater and eUSB2 Device are respectively soldered to the circuit board.

Two additional templates have been defined by the eUSB2 specification. eUSB2 jitter budgeting assumes jitter at TP2 & TP3 remain the same as defined in USB2.0. USB2.0 Template1 & Template 4 are normative specifications. eUSB2 Template 1 & eUSB2 Template 2 are informative specifications only during repeater mode. Conformance to eUSB2 Template 1 and 2 is required for eUSB2 Host and eUSB2 device in native mode.

eUSB2 Template 1: Transmit waveform requirement for an eUSB2 host measured at eTP1.
eUSB2 Template 2: Receiver sensitivity requirements for an eUSB2 device when signal is applied at eTP2 (native mode) or eTP4 (repeater mode).

Note1: eUSB2 templates have been defined assuming signal flow where eUSB2 Host in transmit mode is transmitting to eUSB2 device in receive mode. Host repeater's eUSPh is in receiving

mode & D+/D- side in transmit mode while Peripheral repeater's eDSPp is in transmit mode & D+/D- side is in receiving mode. Jitter allocation for a repeater is 50ps.

7.1.5.1 eUSB2 Template 1

Figure 7-6 defines the setup for the simulation/measurement. The circuit board trace should be kept less than one inch, and R_L differential termination resistor should be 80kΩ+/- 1% for unterminated mode and 80Ω +/- 1% for terminated mode.

Figure 7-7 shows the transmit waveform requirement for an eUSB2 host measured at eTP1. It should be read together with Table 7-7 or Table 7-11 depending on the application. Table 7-8 and Table 7-9 define V-T limits for un-terminated and terminated load respectively.

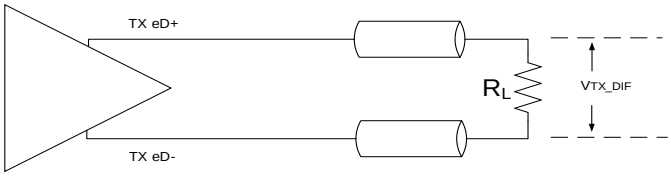


Figure 7-6: High-speed Transmit Eye Diagram Test Setup

Table 7-7: High-speed Transmit Eye Test Load Definition

Termination	R_L
Terminated	80Ω
Unterminated	80kΩ

Note: for measurement at pin.

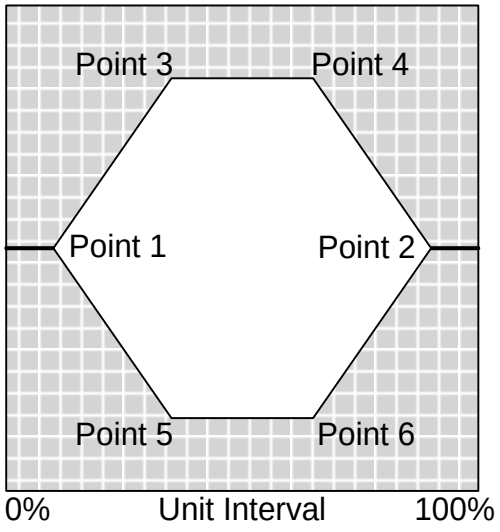


Figure 7-7: eUSB2 Template 1 Eye Mask

Table 7-8: eUSB2 Template 1 V-T Table (Un-terminated)

	80kΩ test load	
	Voltage Level (eD+ - eD-)	Time (% of UI)
Point 1	0V	10
Point 2	0V	90
Point 3	180mV	35
Point 4	180mV	65
Point 5	-180mV	35
Point 6	-180mV	65

Table 7-9: eUSB2 Template 1 V-T Table (Terminated)

	80Ω test load	
	Voltage Level (eD+ - eD-)	Time (% of UI)
Point 1	0V	4
Point 2	0V	96
Point 3	150mV	35
Point 4	150mV	65
Point 5	-150mV	35
Point 6	-150mV	65

7.1.5.2 eUSB2 Template 2

Receiver eye patterns specify the minimum and maximum limits, as well as limits on timing jitter, measured at the 80Ω differential test load at the end of the channel. Figure 7-8 shows the Receiver sensitivity requirements for an eUSB2 device when signal is applied at eTP2 (Native mode), and for an eUSB2 device with repeater when signal is applied at eTP4 defines the V-T limits of the eye mask.

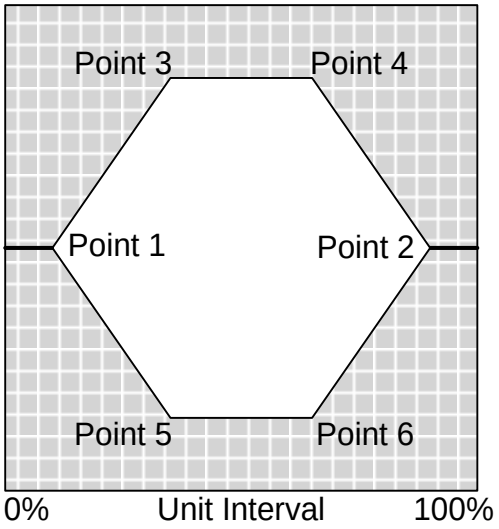


Figure 7-8: eUSB2 Template 2 Eye Mask

Table 7-10: eUSB2 Template 2 V-T Table

	Voltage Level (eD+ - eD-)	Time (% of UI)
Point 1	0V	21.2
Point 2	0V	79.8
Point 3	110mV	41.2
Point 4	110mV	58.8
Point 5	-110mV	41.2
Point 6	-110mV	58.8

7.1.5.3 High-speed Repeater Mode Jitter Allocation

USB2 Tx and Rx Eye Diagram compliance requirements dictate the total jitter allocation available to the transmitter, repeater and the channel.

A redriver is recommended if the channel topology between the SoC and walk-up port is meeting the specification outlined in section 6.1.4. For applications that require channel route beyond the specification, a retimer is required.

A redriver is required to comply with Template 1 (in the case of host repeater) & Template 4 (in the case of peripheral repeater) as defined in USB2.0, Section 6.1.2.2, when repeater signals

either to upstream or downstream. A detailed system level Jitter Budget is given in Table 7-11. The baseline for this jitter budget is maintaining the same jitter budget as TP2 & TP4 as defined in USB2.0 Template 1 & Template 4. Note that this requirement does not apply to a retimer. A retimer should be treated like a typical USB2.0 hub from jitter budgeting perspective.

Table 7-11: System Level Jitter Budgeting with Host & Peripheral Redriver

Jitter Source	Tj (ps)	UI (%)	Note
eUSB2 Tx	166.5	8	1
Host Channel	96	4.6	2
Host-Redriver	50	2.4	3
USB Cable	312.5	15	
Device Channel	208.3	10	2
Peripheral Redriver	50	2.4	3
Total	883.3	42.4	4,6

Notes:

1. Silicon TX jitter budget is informative.
2. Channel jitter is informative.
3. Repeater jitter is normative and measured during test mode using Test Packet.
4. Total jitter at eTP4 is informative.
5. Total jitter at TP2 & TP3 is normative and complies with USB2.0 Template 1 & Template 3 as defined in USB2.0.
6. Receiver must tolerate an additional 2.4% jitter.

7.2 *Low-speed/Full-speed*

Low-speed/Full-speed used single-ended CMOS signaling to communicate between the link partners. A relatively loose source termination is required if compared to High-speed. The receiver is un-terminated. Limits are defined for rise and fall time to avoid excessive overshoot and undershoot observed at both the transmitter and receiver end.

7.2.1 **Full-speed/Low-speed Electrical Specification**

Table 7-12: Low-speed /Full-speed DC Specifications for 1.0V +/- 10%

Parameter	Symbol	Min	Typ	Max	Units	Notes
Supply Voltage for eD+/eD-	VCC	0.9	1.0	1.1	V	1, 2
Transmit single-ended output low	V_{OL}			0.15 x VCC	V	
Transmit single-ended output high	V_{OH}	0.85 x VCC		VCC	V	
Transmit output impedance	R_{SRC_LSFS}	28		60	Ω	3
Input low voltage	V_{IL}	-0.1		0.35* VCC	V	
Input high voltage	V_{IH}	0.65 x VCC		1.05 x VCC	V	
Receive single-ended hysteresis voltage	V_{HYS}	0.04 x VCC			V	

Notes:
1) VCC shall be within 150 mV (15%) of each other at all times on both receive and transmit sites
2) GND shall be within 40 mV (4%) of each other at all times on both receive and transmit sites
3) Shall be met up to V_{OL} when driving low and above V_{OH} when driving high

Table 7-13: Low-speed /Full-speed DC Specifications for 1.2V +/- 10%

Parameter	Symbol	Min	Typ	Max	Units	Notes
Supply Voltage for eD+/eD-	VCC	1.08	1.2	1.32	V	1, 2
Transmit single-ended output low	V_{OL}			0.15 x VCC	V	
Transmit single-ended output high	V_{OH}	0.85 x VCC		VCC	V	
Transmit output impedance	R_{SRC_LSFS}	28		60	Ω	3
Input low voltage	V_{IL}	-0.1		0.35* VCC	V	
Input high voltage	V_{IH}	0.65 x VCC		1.05 x VCC	V	
Receive single-ended hysteresis voltage	V_{HYS}	0.04 x VCC			V	

Notes:
1) VCC shall be within 180 mV (15%) of each other at all times on both receive and transmit sites
2) GND shall be within 48 mV (4%) of each other at all times on both receive and transmit sites
Shall be met up to V_{OL} when driving low and above V_{OH} when driving high
3) To get better system performance try to match termination impedance as close as possible

Table 7-14: Low-speed /Full-speed AC Specifications

Parameter	Symbol	Min	Typ	Max	Units	Notes
Transmit rise and fall time (10%-90%)	$T_{RISE\_FALL\_TRM}$	2		6	ns	1
Transmit rise/fall mismatch				25	%	2
eUSB2 to USB 2.0 repeater FS jitter to next transition	$T_{e\_to\_U\_DJ1}$	-6.0		+6.0	ns	3
repeater FS paired transition jitter in both directions	T_{DJ2}	-1.5		+1.5	ns	4
eUSBr receiver FS jitter tolerance	T_{RJR1}	-15.5		+15.5	ns	5

Notes:
1) Measured with 2.5pF test load at eUSB2 device/eUSB2 repeater end and assuming 10-inch channel trace in between eUSB2 Host and eUSB2 repeater/eUSB2 device.
2) Rise/fall mismatch = absolute delta of (rise – fall time) / (average of rise and fall time).
3) USB 2.0 to eUSB2 repeater jitter to next transition follows USB 2.0 parameter T_{HDJ1}
4) Relaxed relative to T_{HDJ2} defined by USB 2.0
5) = abs(T_{JR1}) – abs(T_{HDJ1}) where T_{JR1} and T_{HDJ1} are defined by USB 2.0

7.3 *Pull-down*

A much stronger pull-down is defined for eUSB2 than USB2.0. Pull-downs are used during device connect detect. It is also used to hold the line to ground when the link is idle.

Table 7-15: Host and Device Pull-up and Pull-down Specification

Parameter	Symbol	Min	Typ	Max	Units	Notes
Pull-down	R_{PD}	4		10	kΩ	

7.4 Timing Specification

Table 7-16: Timing Specification

Parameter	Symbol	Tx Min	Tx Max	Rx Min	Rx Max	Units	Notes
The amount of time that an active driver shall remain idle for Back to back CM.	T_{CMB2B}	10		NA	NA	µs	a) This is measured from end to start. b) CM.RAP included
The amount of time that an active driver shall drive the wire to transition from non-SE0 to SE0, before letting the weak pull-down to hold the wire in SE0 idle, for low-speed and full-speed mode.	$T_{SE0\_DR\_LSFS}$	20	70	NA	NA	ns	
The amount of time that an active driver shall drive the wire to transition from non-SE0 to SE0, before letting the weak pull-down to hold the wire in SE0 idle, for high-speed mode.	$T_{SE0\_DR\_HS}$	1	4	NA		HS UI	a) Shall be less than $T_{HSIPDOD}$ USB2.0. b) Equal to USB 2.0 squelch delay to naturally drive back to SE0 while repeating. c) May be driven by SE TX or HS TX.

Parameter	Symbol	Tx Min	Tx Max	Rx Min	Rx Max	Units	Notes
1X Start of Control Message	$T_{CM\_SE1\_1X}$	4	4			FS UI	For CM.FS, CM. L2 and CM.RAP
8X Start of Control Message	$T_{CM\_SE1\_8X}$	32	32			FS UI	Only for CM.Test and CM.Reset.
Control message SE0 interval	T_{CM_SE0}	4	4			FS UI	
Control Message Internal Clock Period	T_{CM_CLK}	2	2			FS UI	
Start of message to drive K for wake or resume if CM.L2 was not issued to repeater	$T_{DR\_K\_SE1\_1X}$	4	4			FS UI	Link could be in L0 during wake or resume.
Start of message to drive K for wake or resume if CM.L2 was issued to repeater	$T_{DR\_K\_SE1\_8X}$	32	32			FS UI	If UTMI+ suspend is asserted and CM.L2 is send to repeater.
Time duration to end Port/Repeater Configuration upon detecting ACK	T_{CONFIG_CMPL}				1	LS UI	
Time duration for transmitting ESE1 and declaring reception of ESE1	T_{EXTSE1}	2	4	0.45		ms	2 ms needed for native device to announce graceful disconnect while host is in low power state with clocks off.
Idle (SE0) time after transmitting ESE1 or Port/Repeater Configuration	T_{CONFIG_IDLE}			1		LS UI	This is measured from the end of ACK

Parameter	Symbol	Tx Min	Tx Max	Rx Min	Rx Max	Units	Notes
Time duration to declare reception of SE1 for Native mode	T_{NATIVE_SE1}			1		FS UI	A short duration to allow declaring SE1 reception and subsequently to block any signal transmission to allow a clean detection of eUSB2 protocol (i.e. ESE1, CM message)
Time duration for declaring reception of ESE1 for Native mode	T_{NATIVE_ESE1}			8		LS UI	
Time to detect HS disconnect by eDSPr/eDSPn in L0	T_{HSDISC_SE1}	NA	NA	16	50	HS UI	The reason for a short receive timing is to ensure disconnect detection within HS IPG (88UIs)
Delay for eUSPh to start signaling HS disconnect to eDSPr after end of uSOF	T_{DISC_DLY}		32			HS UI	Together with T_{HSDISC_SE1}, ensure disconnect detection within HS IPG (88UIs)
Duration of all strobes. End of Reset and Resume when going to HS, end of Wake from eUSPr, enable HS term during chirp from eUSPr and reporting DP pull up detection by repeater.	T_{STROBE}	0.5	1.5	0.01		µs	Roughly 1-2 LS UI

Parameter	Symbol	Tx Min	Tx Max	Rx Min	Rx Max	Units	Notes
A setup time to sample Digital Ping	T_{DPING_SU}			0.75		FS UI	
Bus turnaround before analog ping	$T_{TURNAROUND}$	12	24		10	HS UI	
Width of analog ping	$T_{ANALOGPING}$	8	8	2	7	HS UI	RX timing is meant as a possible received width at the output of squelch receiver (Not as the input to the eDSPn receivers)
Differential Skew	T_{SE1_SKEW}		500	600		ps	a) Measured at 50% cross-over point b) Rx min is a guideline, not a requirement.
Time for peripheral repeater to recognize reset from HS to FS	$T_{PR\_HS\_RESET\_TO\_FS}$	NA	NA	64	128	µs	After the end of CM.FS, if a peripheral repeater detects its DP pullup beyond this time, it will declare reset to FS instead of L1 or L2 from HS.

Appendix A: Skew and Rise/Fall time Break-ups

The skew and rise/fall time break-up for T_{SE_SKEW} can be found below. Refer to **Error! Reference source not found.** for skew sources in the communication channel.

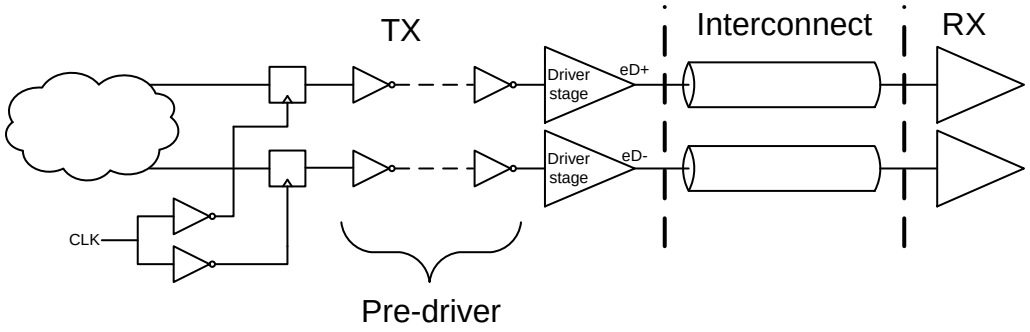


Figure A-1: eUSB2 Driver and Interconnect

- Total skew: 340ps
  - Total driver induced skew=270ps.
    - Main driver induced skew=50ps + 60ps due to mismatch (+/- 3 sigma) = 110ps.
    - Pre-driver + Clock path skew + mismatch = 100ps + 60ps = 160ps.
  - Interconnect skew = 70ps (176 ps/inch FR4; or 70 ps/cm); Assuming 1cm mismatch in the trace for 20cm trace width.
- The rise and fall times must be between the min and max of $T_{RISE\_FALL\_TRM}$ (2ns and 6ns) and matched to within max 25%. The following two cases show a 25% max matching for rise and fall times that are at the min and the max of $T_{RISE\_FALL\_TRM}$.
  - Case 1: eD+ rise @4.8ns & eD- rise @6ns.
  - Case 2: eD+ rise @2.5ps & eD- rise @2ns.
- Additional 160ps guard band assumed in current specification