UNIVERSITATEA TEHNICĂ
DIN CLUJ-NAPOCA

SAIC PROJECT

Design of an Analog Interface with the Following Stages: Amplifier, Filter, PGA, and Rectifier

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1. Project Theme

This project involves the design, simulation, and characterization of an analog interface system comprising four stages:

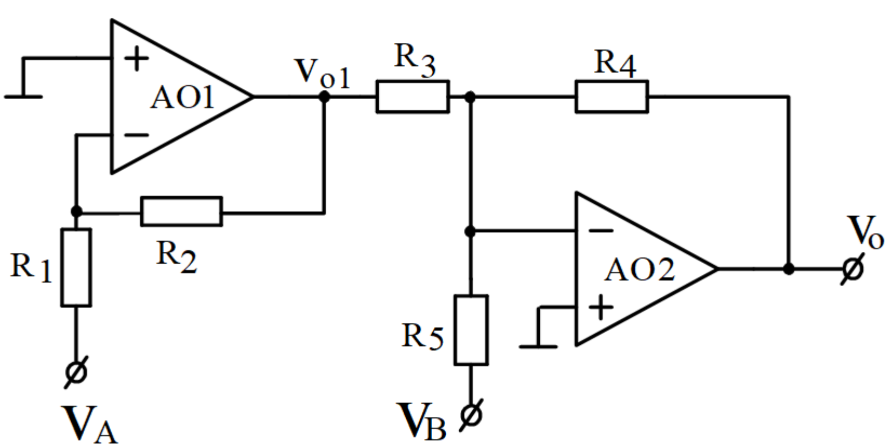
1. **Stage 1**: Instrumentation Amplifier with two operational amplifiers.
2. **Stage 2**: Rauch Low-Pass Filter.
3. **Stage 3**: Programmable Gain Amplifier (PGA).
4. **Stage 4**: Full-Wave Rectifier with operational amplifiers and diodes.

Operational Amplifier Used: OP482 with ±15 V supply voltage.
Input Signal Source: Differential signal.
Objective: Correctly design, simulate, and analyze the system to meet the specified requirements.

2. Dimensioning of Stages

Stage 1 - Instrumentation Amplifier

Etaj 1					
Tip Sursa semnal	amplitudine minima (pt castig maxim PGA)	amplitudine maxima (pt castig minim PGA)	unitate masura	Tip Etaj 1	|Castig| etaj 1 (liniar)
2	1.37E-01	2.73E-01	V(differential)	5	11



- **Purpose**: Amplify a differential input signal while rejecting common-mode noise.
- **Circuit**: Inverting configuration with two operational amplifiers.
- **Design Equations**:

  Using the gain equation: $A = \frac{v_0}{v_A - v_B} = \frac{\frac{R_2 R_4}{R_1 R_3} v_A - \frac{R_4}{R_5} v_B}{v_A - v_B}$ $\quad A = \frac{R_4}{R_5} \frac{v_A - v_B}{v_A - v_B} = \frac{R_4}{R_5}$

OA1:

$$v^- = v^+$$

$$v^+ = 0$$

$$v^- = \frac{\frac{v_A}{R_1} + \frac{v_{01}}{R_2}}{\frac{1}{R_1} + \frac{1}{R_2}} = \frac{v_A R_2 + v_{01} R_1}{R_1 R_2} \frac{R_1 R_2}{R_1 + R_2} = \frac{v_A R_2 + v_{01} R_1}{R_1 + R_2} \Rightarrow v_{01} = -\frac{R_2}{R_1} v_A$$

OA2:

$$v^- = v^+$$

$$v^+ = 0$$

$$v^- = \frac{\frac{v_B}{R_5} + \frac{v_{01}}{R_3} + \frac{v_0}{R_4}}{\frac{1}{R_5} + \frac{1}{R_3} + \frac{1}{R_4}} \Rightarrow v_0 = -\frac{R_4}{R_5} v_B - \frac{R_4}{R_3} v_{01} \Rightarrow \frac{R_2 R_4}{R_1 R_3} v_A - \frac{R_4}{R_5} v_B$$

<u>Input signal:</u>

Maximum amplitude:

0.137

Minimum amplitude :

0.273

source:

differential

$V_A - V_B = Amax$

Choose VA=2V and VB=1.727V

Differential gain so we have R1*R3=R2*R5 and RinA=R1, RinB=R5 therefore R1=R5. With these two statements we can say that R1=R5 and R2=R3

Component Values:

$R_1 = 2k$

$R_2 = 2k$

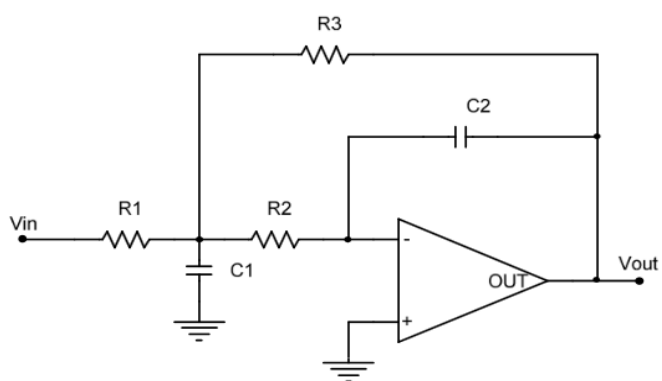
$R_3 = 2k$

$R_4 = 22k$

$R_5 = 2k$

Stage 2 - Rauch Low-Pass Filter

Etaj 2				
Tip Etaj 2	**|H0| castig liniar in banda de trecere**	**Rintrare minim**	**Banda**	**Q**
2	1	1kΩ	4000	0.707



- **Purpose**: Filter high-frequency noise, ensuring only low-frequency signals pass through.

- **Design Equations**:

$$H(s)=\frac{V_{Out}}{V_{In}}=-\frac{R_3}{R_1}\cdot\frac{\frac{1}{R_2R_3C_1C_2}}{s^2+s\cdot\frac{1}{C_1}\cdot\left(\frac{1}{R_1}+\frac{1}{R_2}+\frac{1}{R_3}\right)+\frac{1}{R_2R_3C_1C_2}}$$

$$H_0=\frac{R_3}{R_1};\omega_0=\frac{1}{\sqrt{R_2R_3C_1C_2}};Q=\sqrt{\frac{C_1}{C_2}}\frac{R_1\sqrt{R_2R_3}}{R_1(R_2+R_3)+R_2R_3}$$

Sizing strategy: Choose R1=R2=R3=R => $H_0=1;\ \omega_0=\frac{1}{R\sqrt{C_1C_2}};\ Q=\frac{1}{3}\sqrt{\frac{C_1}{C_2}}$

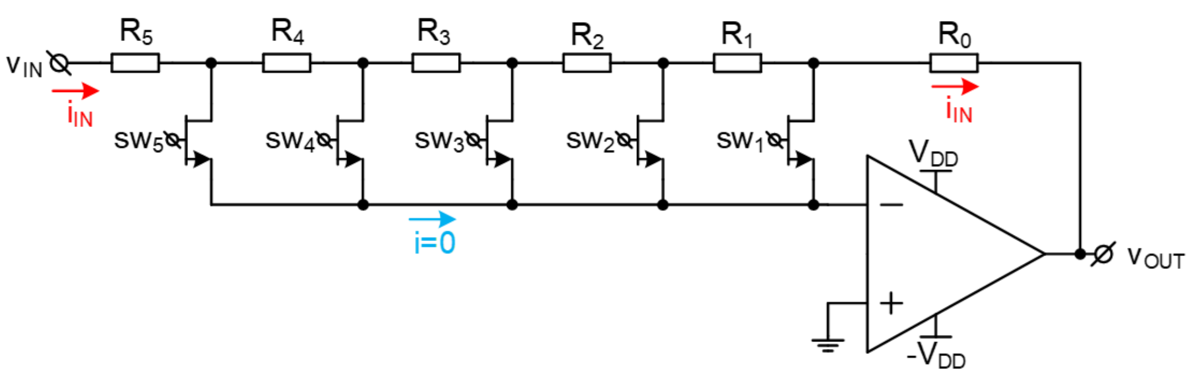
$$C_1=\frac{3Q}{\omega_0 R};C_2=\frac{C_1}{9Q^2}=\frac{1}{3Q\omega_0 R}.$$

- **Component Values**:

  C1/C2=4.5 => C1=4.5nF, C2=1nF

  R1=R2=R3=20K

Stage 3 - Programmable Gain Amplifier (PGA)



- **Purpose**: Provide gain adjustments with four programmable steps.
- **Specifications**:
  - Gain Range: 0 dB to 6 dB
  - Resolution: 2 dB/step2
  - Steps number: 4 (4 switches)

- Rin minim = 2500 = > R5=2500

- **Design Equations**:
  Gain equation:

$$Av = -\frac{R_f}{Rg}$$

where Rf is the feedback resistance and Rg the gain resistance.

SW1	SW2	SW3	SW4	Rg[Ω]	Rf[Ω]	Av[V/V]	Av[dB]
VDD	0	0	0	R2+R3+R4+R5	R1	1	0
0	VDD	0	0	R3+R4+R5	R1+R2	1.26	2
0	0	VDD	0	R4+R5	R1+R2+R3	1.58	4
0	0	0	VDD	R5	R1+R2+R3+R4	2	6

$R_5 = 2500$

$$\begin{cases} 1 = \dfrac{R_1}{R_2 + R_3 + R_4 + R_5} \\ 1{,}26 = \dfrac{R_1 + R_2}{R_3 + R_4 + R_5} \\ 1{,}58 = \dfrac{R_1 + R_2 + R_3}{R_4 + R_5} \\ 2 = \dfrac{R_1 + R_2 + R_3 + R_4}{R_5} \end{cases}$$

$\Rightarrow R_1 + R_2 + R_3 + R_4 = 5000$

$3750 + R_2 + R_3 + R_4 = 5000$

$R_2 + R_3 + R_4 = 1250$

$R_3 + R_4 = 1250 - R_2$

$R_1 = R_2 + R_3 + R_4 + 2500$

$2500 = R_1 - R_2 - R_3 - R_4$

$\boxed{R_1 = 2500 + R_2 + R_3 + R_4}$

$5000 = R_1 + R_1 - 2500$

$2R_1 = 7500$

$\boxed{R_1 = 3750}$

$1{,}26 = \dfrac{R_1 + R_2}{R_3 + R_4 + R_5}$

$1{,}26 = \dfrac{3750 + R_2}{1250 - R_2 + 2500}$

$4725 - 1{,}26 R_2 = 3750 + R_2$

$2{,}26 R_2 = 1000$

$\boxed{R_2 = 442{,}5\,\Omega}$

$R_3 + R_4 = 1250 - 442{,}5$

$R_3 + R_4 = 807{,}5$

$R_3 = 807{,}5 - R_4$

$R_3 = 807{,}5 - 407$

$\boxed{R_3 = 400{,}5}$

$$1,58 = \frac{R_1 + R_2 + R_3}{R_4 + R_5}$$

$$1,58 = \frac{3750 + 442,5 + 807,5 - R_4}{R_4 + 2500}$$

$$1,58 R_4 + 3950 = 5000 - R_4$$

$$2,58 R_4 = 1050$$

$$R_4 = \frac{1050}{2,58} = 406,97 \cong 407$$

- **Component Values** (for each gain setting):

$R_1 = 3.75k$

$R_2 = 442.5$

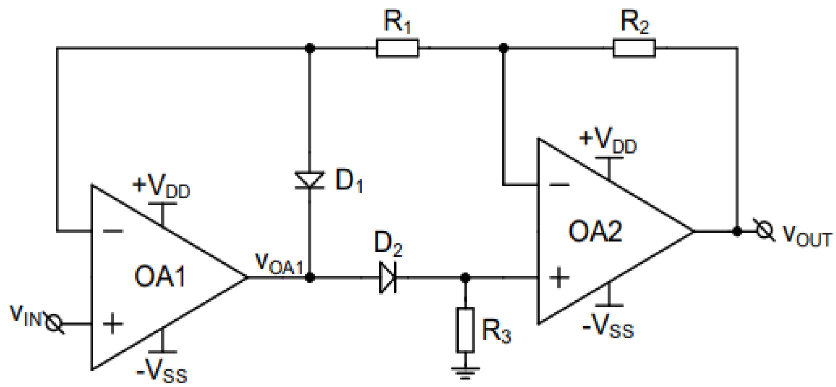
$R_3 = 400.5$

$R_4 = 407$

$R_5 = 2.5k$

Stage 4 - Full-Wave Rectifier with Unity Gain

Schematic



Advantage:
High input impedance

Transfer function

Assume D_1, D_2 = OFF
OA2 in negative feedback loop => $V_2^- = V_2^+ = 0$; $i_{R1} = 0$ (no closed circuit loop) => $V_1^- = 0$;

Vin<0
$V_1^+ < 0$ & $V_1^- = 0$; => $V_{OA1} \searrow V_{OL}$ =>
D_1 = ON; D_2 = OFF
OA1 has negative feedback through D1
$\Rightarrow V_1^- = V_1^+ = Vin$
D_2 = OFF => $V_2^+ = 0$
OA2 and R1&R2 implement an inverting amplifier
=> $\mathbf{V_{Out} = -Vin\ (R2/R1)}$

Condition for operating as a FWR:
$(R_2)/R_1 = 1 \Rightarrow R_1 = R_2$

Vin>0
$V_1^+ > 0$ & $V_1^- = 0$; => $V_{OA1} \nearrow V_{OH}$
=> D_1 = OFF; D_2 = ON
OA2 has a negative feedback loop through D2, as
$V_2^+ = V_2^-$ => $V_1^- = V_1^+ = Vin$ => $i_{R1} = Vin/R_1$
$i_{R1} = 0$ (still no closed circuit loop) => $V_2^- = V_1^- = Vin$
$i_{R2} = 0$ (no closed circuit loop) => $\mathbf{V_{Out} = Vin}$

$$Vout = \begin{cases} V_{In} & \text{if } V_{In} > 0 \\ -V_{In} & \text{if } V_{In} < 0 \end{cases}$$

- **Component Values** :

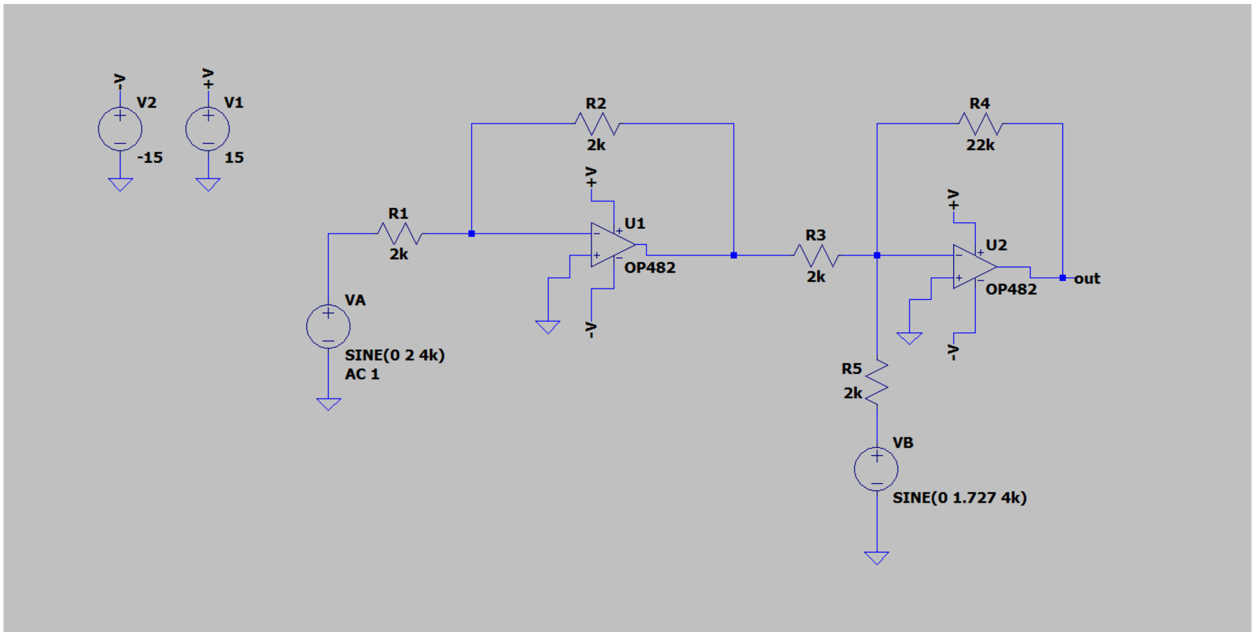
$$R_1 = 1k$$

$$R_2 = 1k$$

$$R_3 = 20$$

3. The characterization of stages.

STAGE 1. Instrumentation Amplifier



DC - DCOP - Static Operating Point

To verify if the output voltage of the instrumentation amplifier matches the calculated value, I apply DC voltage signals with amplitudes equal to those calculated during the design of stage 1.

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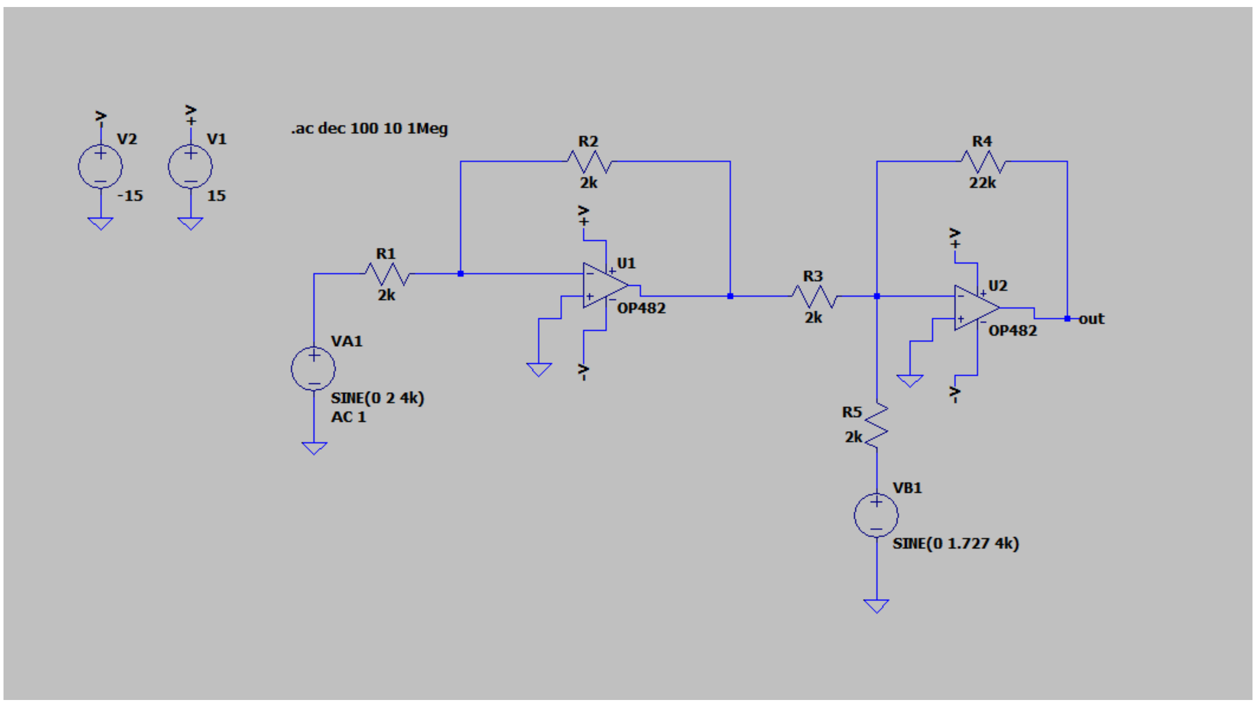
```
       --- Operating Point ---

V(+v):          15              voltage
V(-v):          -15             voltage
V(n001):        0.000232176     voltage
V(n004):        0               voltage
V(n002):        0.000464355     voltage
V(n003):        0.000232247     voltage
V(out):         0.000233807     voltage
V(n005):        0               voltage
I(R1):          1.16088e-07     device_current
I(R2):          1.1609e-07      device_current
I(R3):          -1.16054e-07    device_current
I(R4):          7.0913e-11      device_current
I(R5):          -1.16123e-07    device_current
I(V1):          -0.00200826     device_current
I(V2):          0.00200826      device_current
I(Vb):          1.16123e-07     device_current
I(Va):          1.16088e-07     device_current
Ix(u1:1):       7.9025e-13      subckt_current
Ix(u1:2):       1.87025e-12     subckt_current
Ix(u1:3):       0.00100413      subckt_current
Ix(u1:4):       -0.00100413     subckt_current
Ix(u1:5):       -2.32144e-07    subckt_current
Ix(u2:1):       7.9025e-13      subckt_current
Ix(u2:2):       1.87025e-12     subckt_current
Ix(u2:3):       0.00100413      subckt_current
Ix(u2:4):       -0.00100413     subckt_current
Ix(u2:5):       -7.0913e-11     subckt_current
```

AC - Low-Frequency Gain

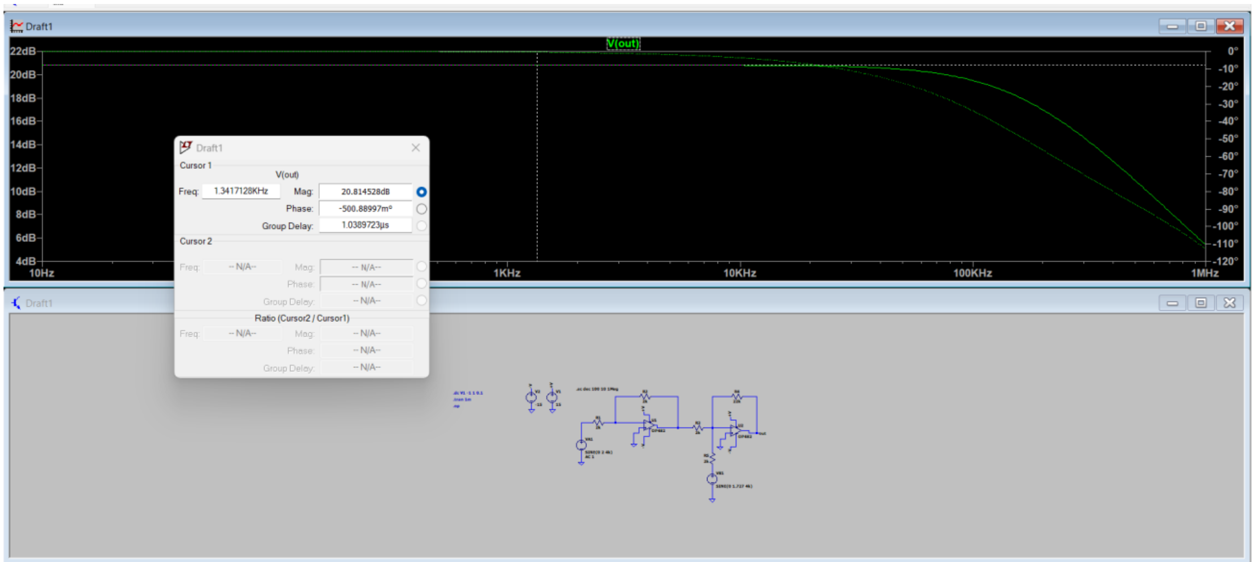
According to the specifications, the gain value must be equal to 11 in the linear domain, corresponding to 20.8 dB. To verify this value, we will set up a decade AC analysis. The simulation result will consist of two frequency characteristics: magnitude and phase.

```
.ac dec 100 .01 10Meg
```

We are interested in the gain value, which must match the one specified in the individual specifications (20.8 dB).



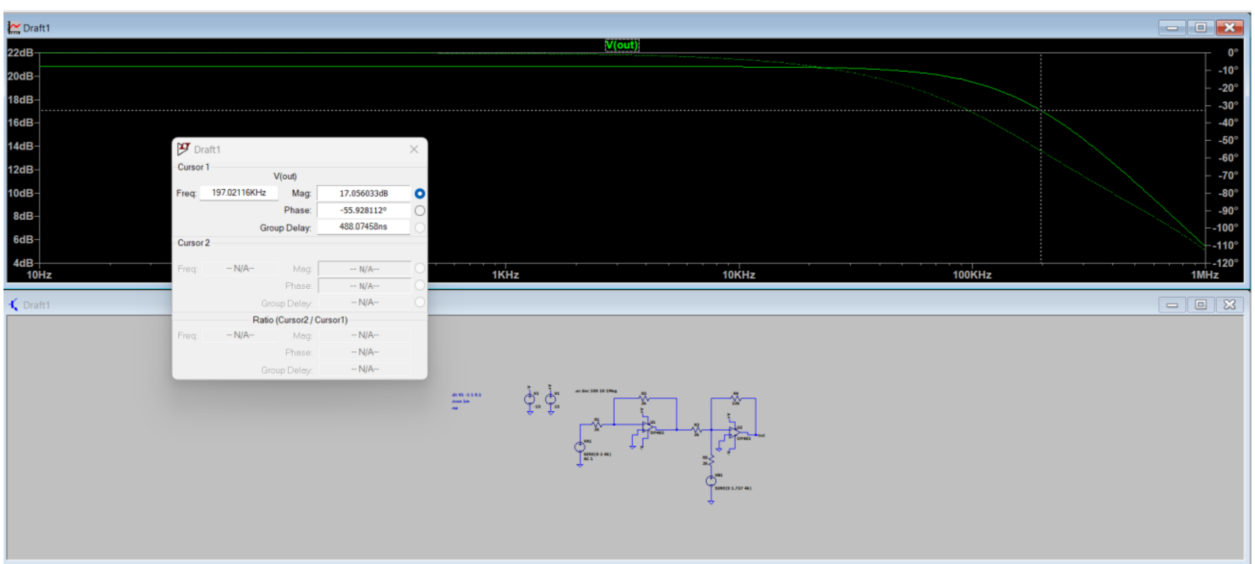
GAIN = 20.8dB = 11



AC - Bandwidth > Filter Bandwidth

We are interested in the bandwidth, which must be greater than the filter bandwidth (4000 Hz). We will use the previously set analysis.

The bandwidth is defined as the frequency at which the gain decreases by 3 dB, so we will position the cursor at 17 dB to determine it.



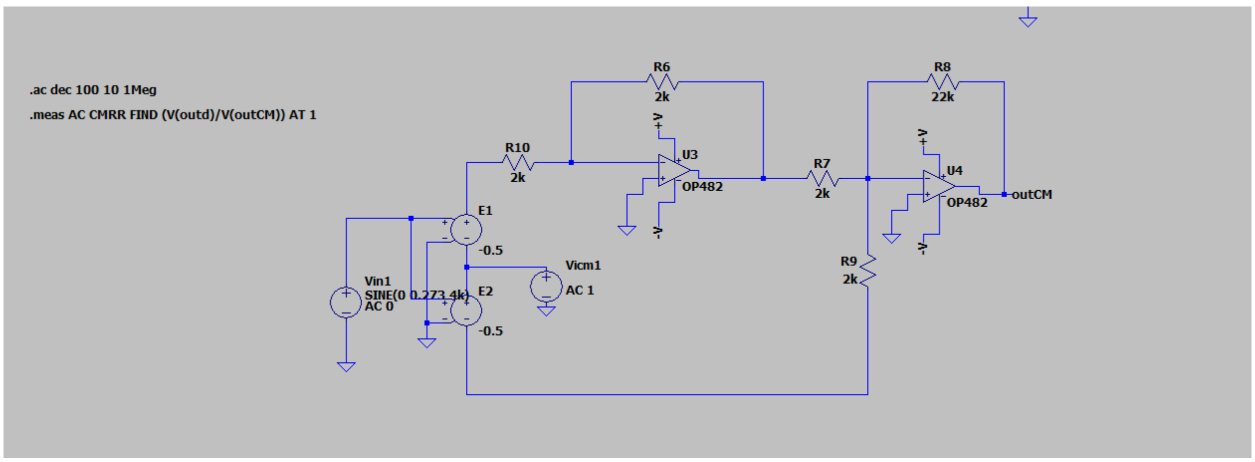
It can be observed that the bandwidth is equal to 197 kHz, a value that is greater than the filter bandwidth (4 kHz) => bandwidth > filter bandwidth.

AC - CMRR, PSRR

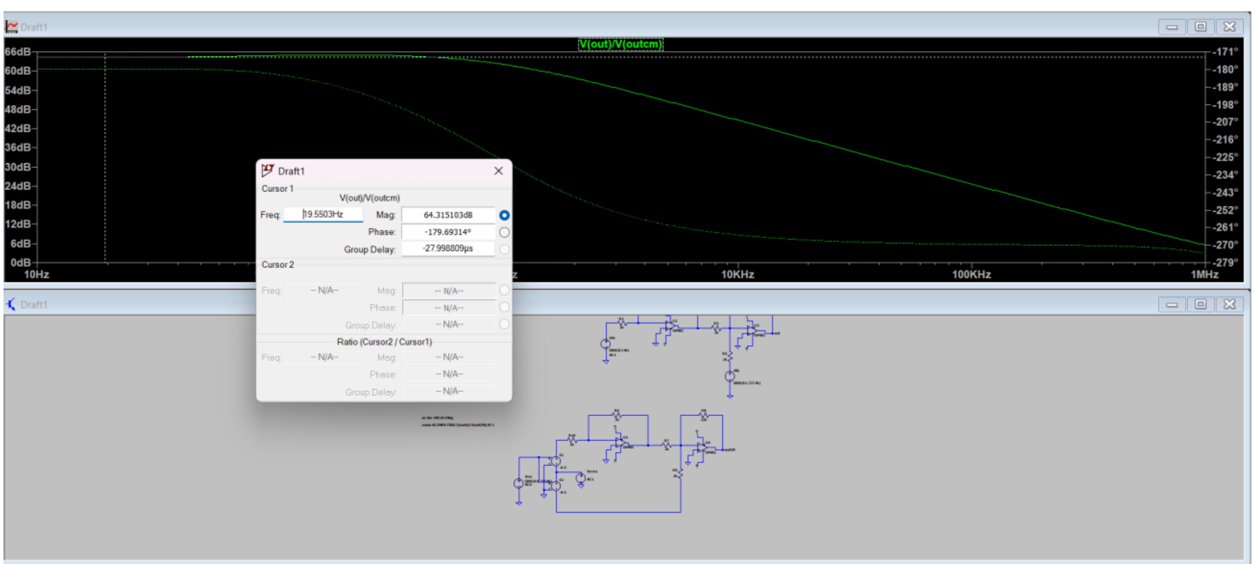
- **CMRR** = Variation of the offset voltage due to changes in the common-mode input voltage.

To measure CMRR, we will use the directive. Additionally, we will apply a common-mode voltage source at the input of the instrumentation amplifier, setting its AC component to 1.

```
.meas AC CMRR FIND (V(outd)/V(outCM)) AT 1
```



To determine the CMRR, we will display the ratio V(out)/V(outCM).

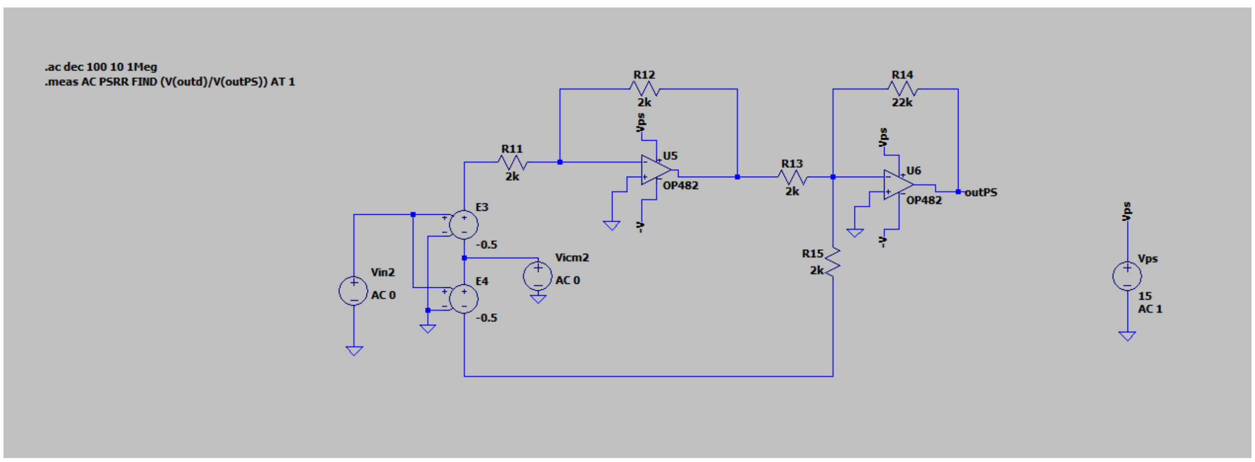


From the measurements, we obtain **CMRR = 64 dB**.

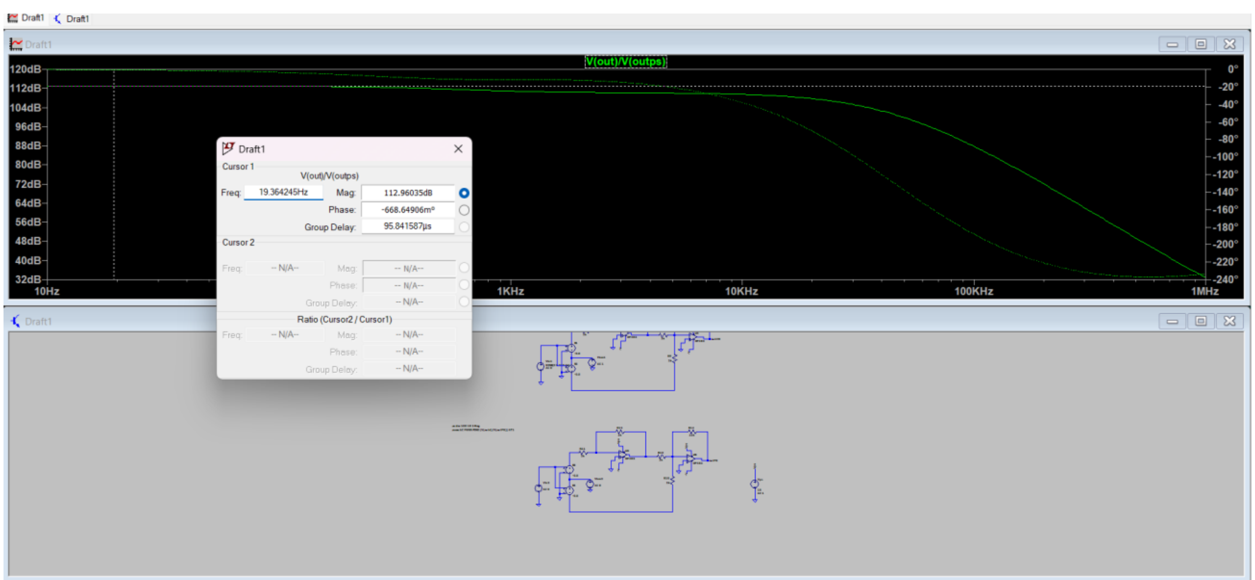
- **PSRR** = Variation of the offset voltage due to changes in the supply voltage.

To measure the PSRR, we will use the directive. Additionally, we will apply a voltage source Vsupply to the positive supply of the instrumentation amplifier, setting its AC component to 1.

```
.meas AC PSRR FIND (V(outd)/V(outPS)) AT 1
```



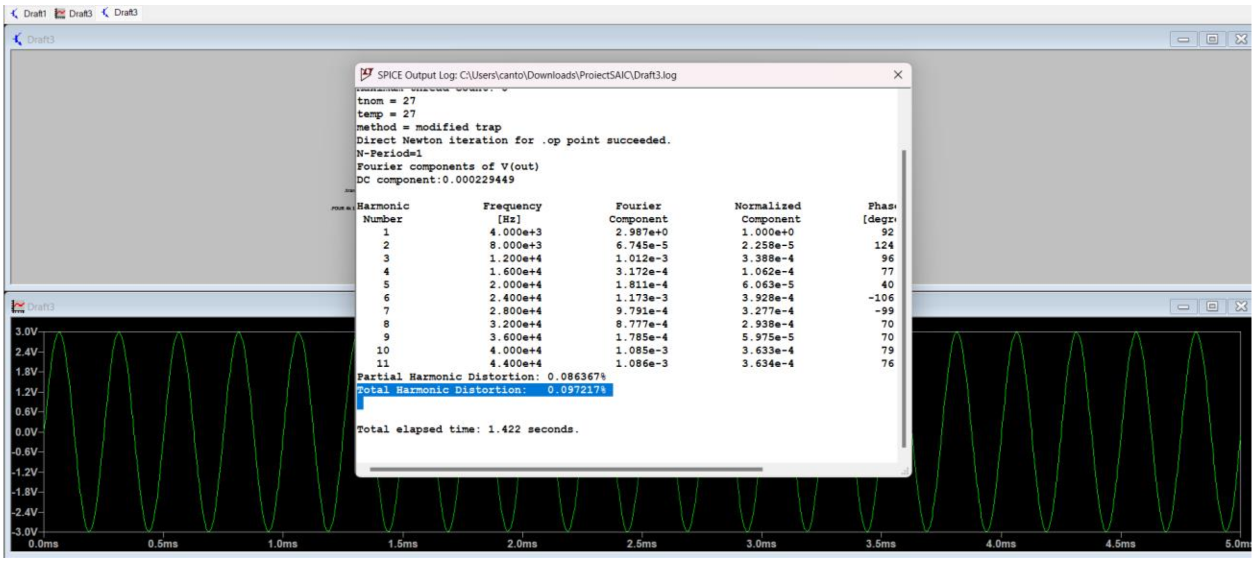
To determine the PSRR, we will display the ratio V(out)/V(outPS)



From the measurements, we obtain **PSRR = 113 dB**.

Transient – Linearity > Specs (for THD < 1%)

To verify the THD value, we will run a transient analysis along with the .FOUR analysis. If the THD value exceeds 1%, we will adjust the signal amplitude until this parameter stabilizes. Initially, an input signal with a maximum amplitude of 0.273 will be applied, which will then be modified based on the THD value.



For the amplitude applied to the input of the instrumentation amplifier, **THD = 0.09721% < 1%**, which means there is no need to adjust the input voltage.

Stage 2 - Rauch Low-Pass Filter

At the input of the filter, we will apply the sinusoidal signal from stage 1, amplified with a gain of 11, and set its frequency to fin_max=4000 Hz

DC - DCOP - Static Operating Point

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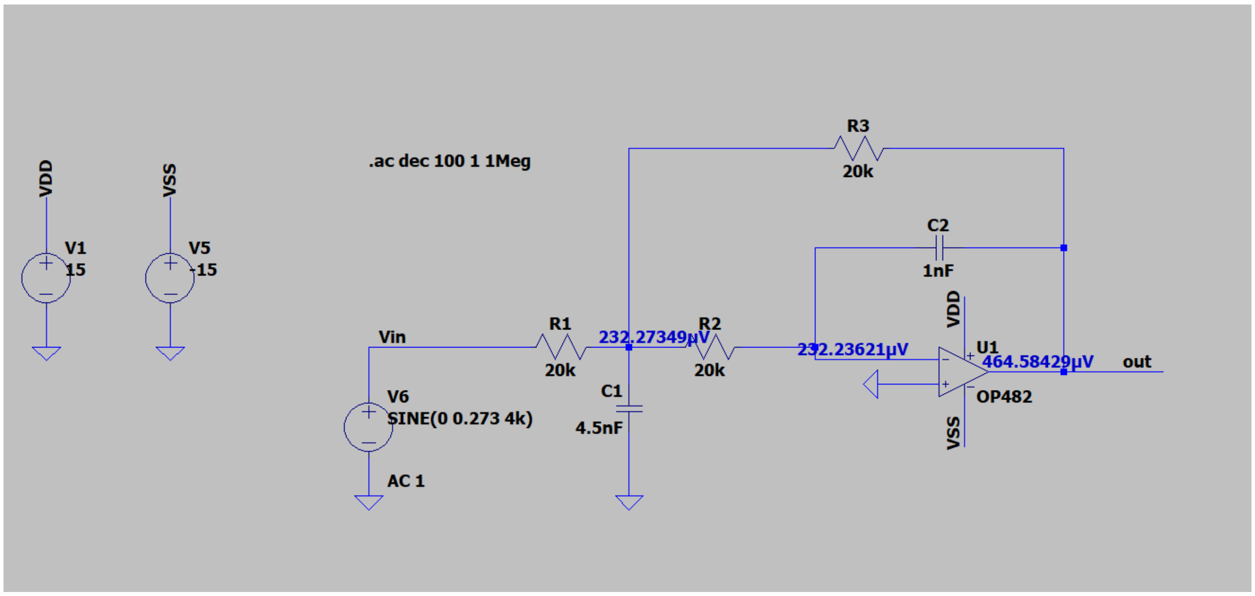
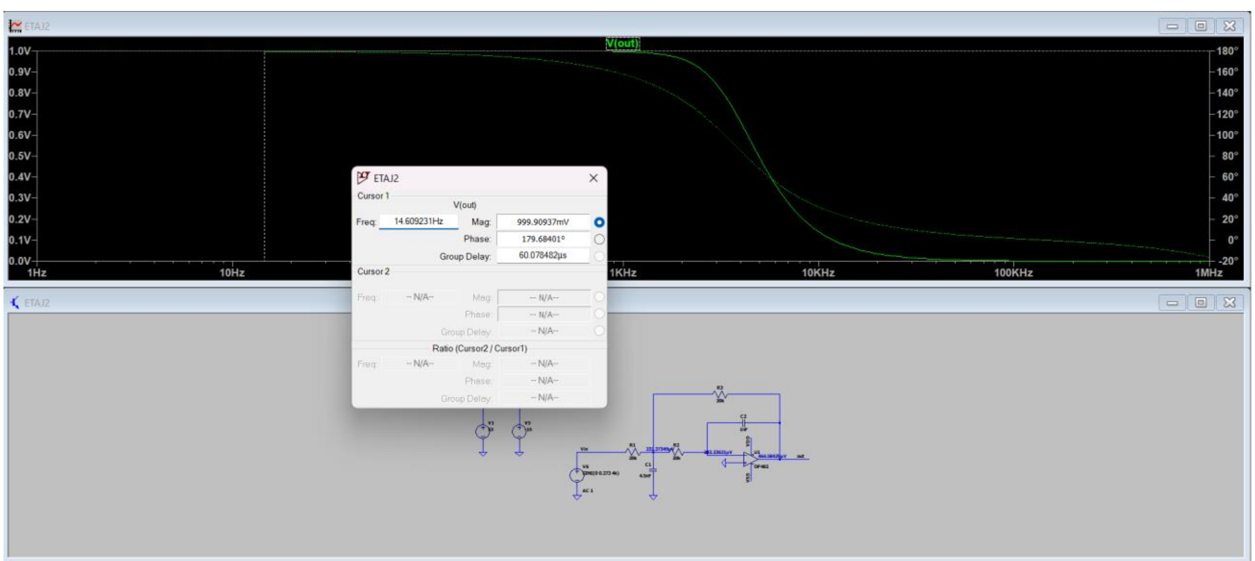
```
       --- Operating Point ---

V(out):          0.000464357    voltage
V(n002):         0.000232176    voltage
V(n001):         0.000232178    voltage
V(vin):          0              voltage
V(vdd):          15             voltage
V(vss):          -15            voltage
I(C2):           2.32181e-28    device_current
I(C1):           -1.0448e-27    device_current
I(R1):           2.32178e-07    device_current
I(R2):           -1.89199e-12   device_current
I(R3):           2.3218e-07     device_current
I(V1):           -0.00100413    device_current
I(V5):           0.00100413     device_current
I(V6):           2.32178e-07    device_current
Ix(u1:1):        7.9025e-13     subckt_current
Ix(u1:2):        1.87025e-12    subckt_current
Ix(u1:3):        0.00100413     subckt_current
Ix(u1:4):        -0.00100413    subckt_current
Ix(u1:5):        -2.3218e-07    subckt_current
```

AC – Gain in the low-pass = Specs

To measure the gain of a low-pass filter, H0 we need the amplitude characteristic of the filter. The gain value corresponding to the center frequency is H0.

From the individual specifications, the required gain is H0=1.

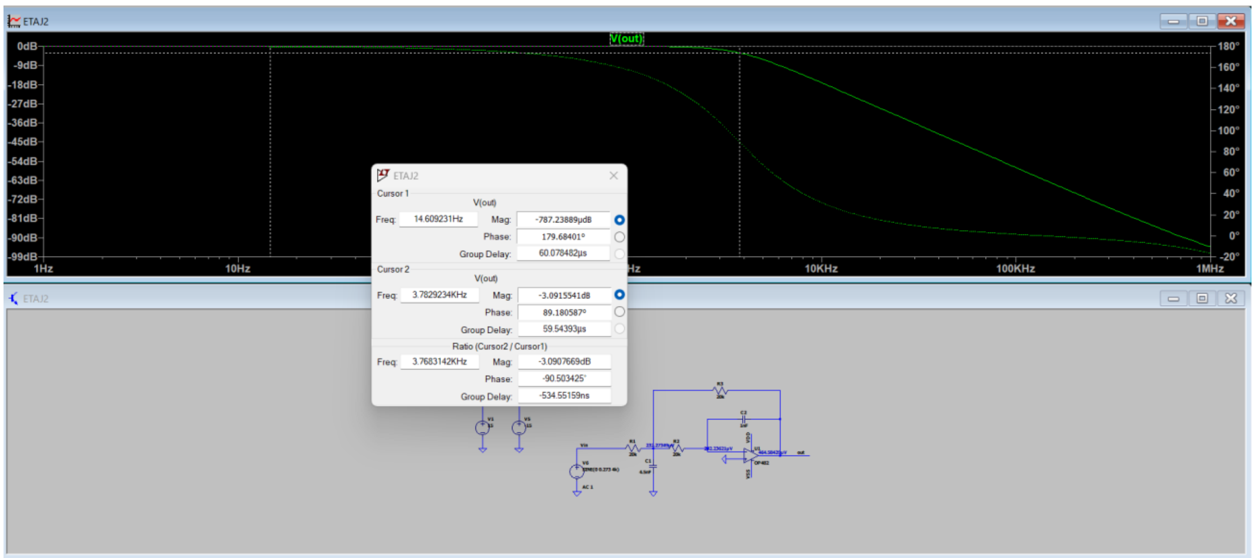




From the simulation, we obtain: H0 approximately 1V (999.9mV)

AC – Bandwidth = Specs

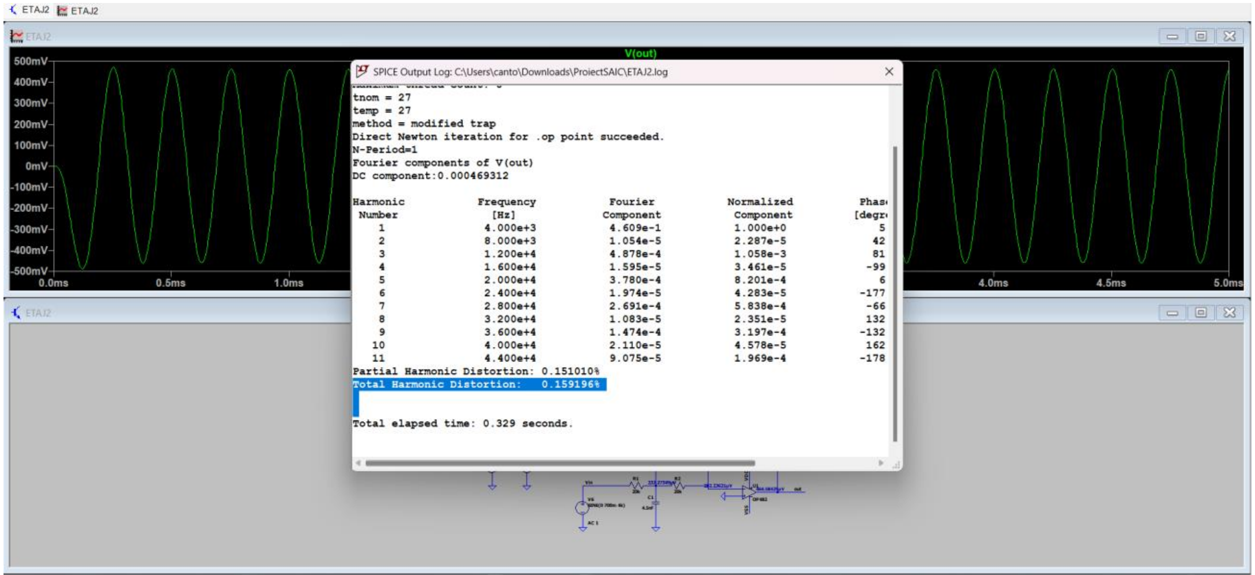
To measure the bandwidth of the low-pass filter, we need two cursors to determine fHIGH and fLOW . These two frequencies are measured at a magnitude of $H0-3$ dB, on either side of the center frequency.



From the measurements, we obtained **BW = 3.76 kHz**.

Transient – Linearity > Specs (for THD < 1%)

```
.FOUR 4k 11 V(out)
.tran 5m
```



From the .FOUR analysis, we obtained **THD = 0.159% < 1%**

Stage 3 – PGA (Programmable Gain Amplifier) Switches Outside the Signal Path - Inverting Configuration

DCOP – Static Operating Point

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```
       --- Operating Point ---

V(vdd):        15             voltage
V(n001):       0.000232206    voltage
V(in):         0              voltage
V(out):        0.000696408    voltage
V(n004):       0.000348091    voltage
V(s1):         0              voltage
V(s2):         0              voltage
V(s3):         0              voltage
V(n002):       0.000269917    voltage
V(n003):       0.000307041    voltage
V(s4):         1              voltage
V(n005):       0.000232207    voltage
V(vss):        -15            voltage
I(R5):         9.28826e-08    device_current
I(R1):         9.28844e-08    device_current
I(R4):         9.2656e-08     device_current
I(R3):         9.26937e-08    device_current
I(R2):         9.27685e-08    device_current
I(S4):         2.2655e-10     device_current
I(S3):         -3.77108e-11   device_current
I(S2):         -7.48347e-11   device_current
I(S1):         -1.15885e-10   device_current
I(V2):         -0.00100413    device_current
I(V4):         0              device_current
I(V5):         0              device_current
I(V6):         0              device_current
I(Vin):        9.28826e-08    device_current
```

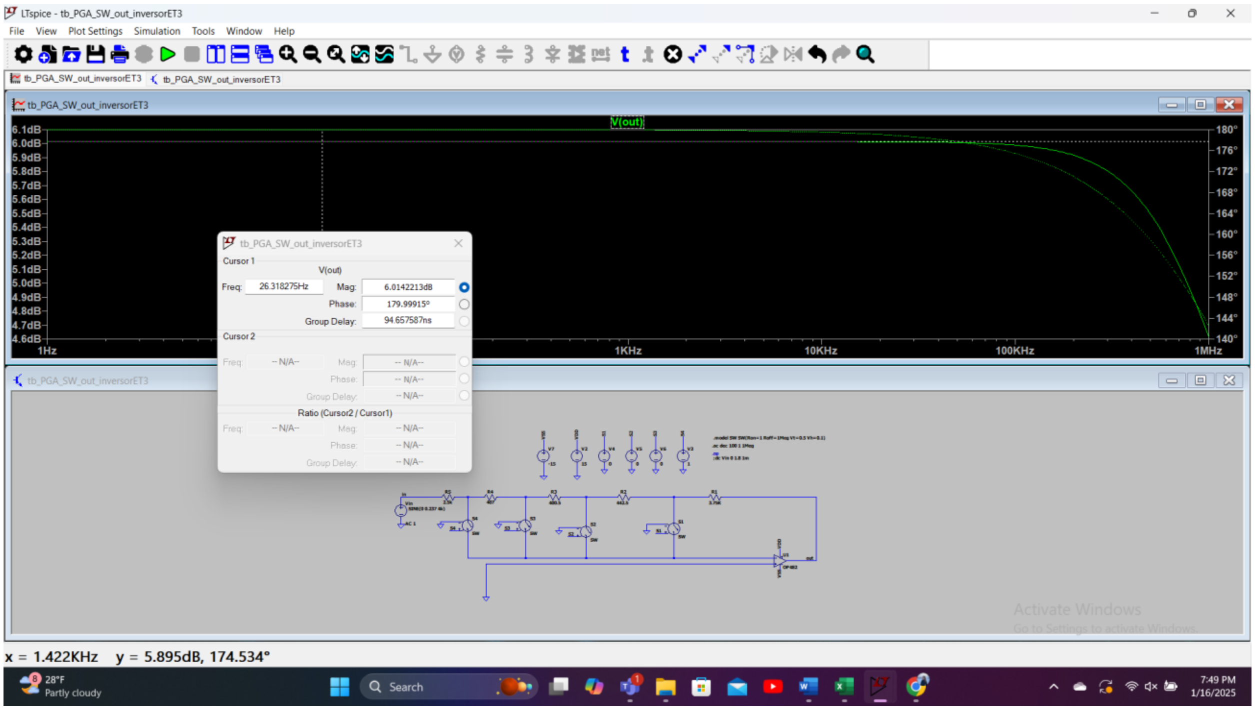
AC – All Gain Steps from Specs Implemented

The gain steps that this circuit must implement are as follows:

AdB ∈ {0dB, 2dB, 4dB, 6dB}.

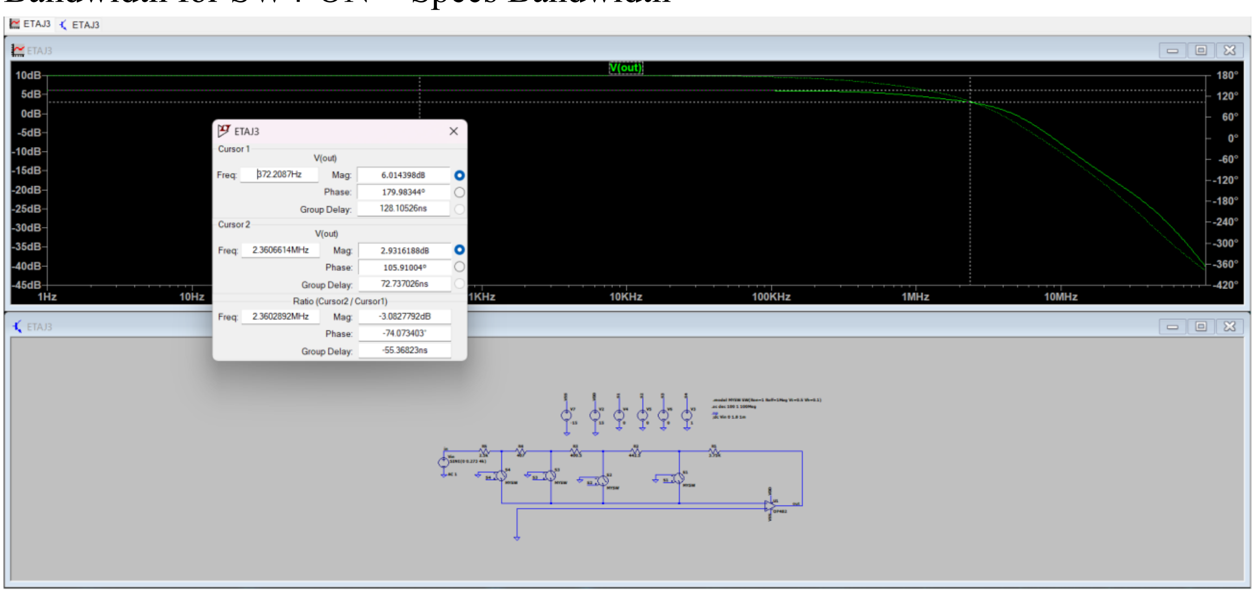
- SW4 ON , SW1 = SW2 = SW3 = OFF

Maximum Amplitude



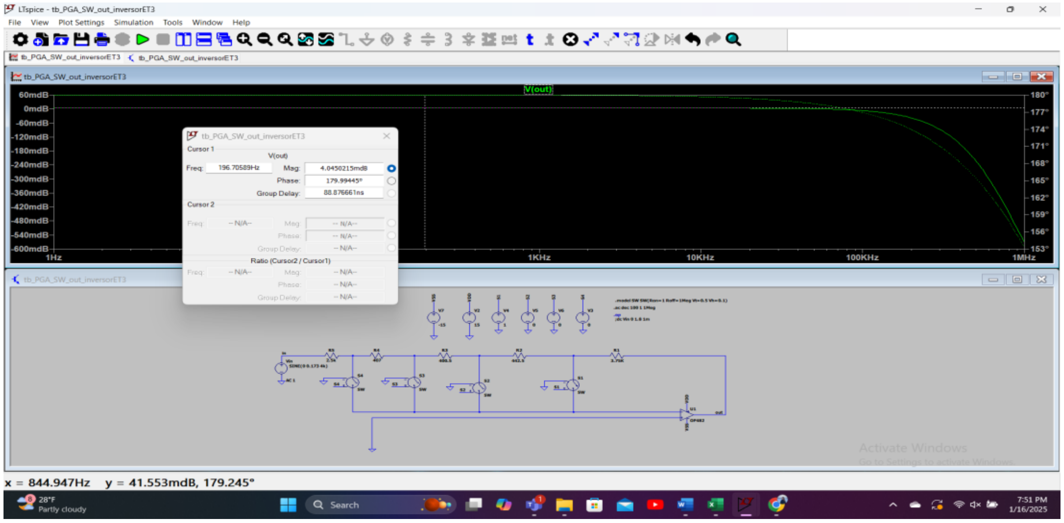
From the specifications: AdB=6 dB.
From the simulation: AdB=6.01 dB.

Bandwidth for SW4-ON > Specs Bandwidth



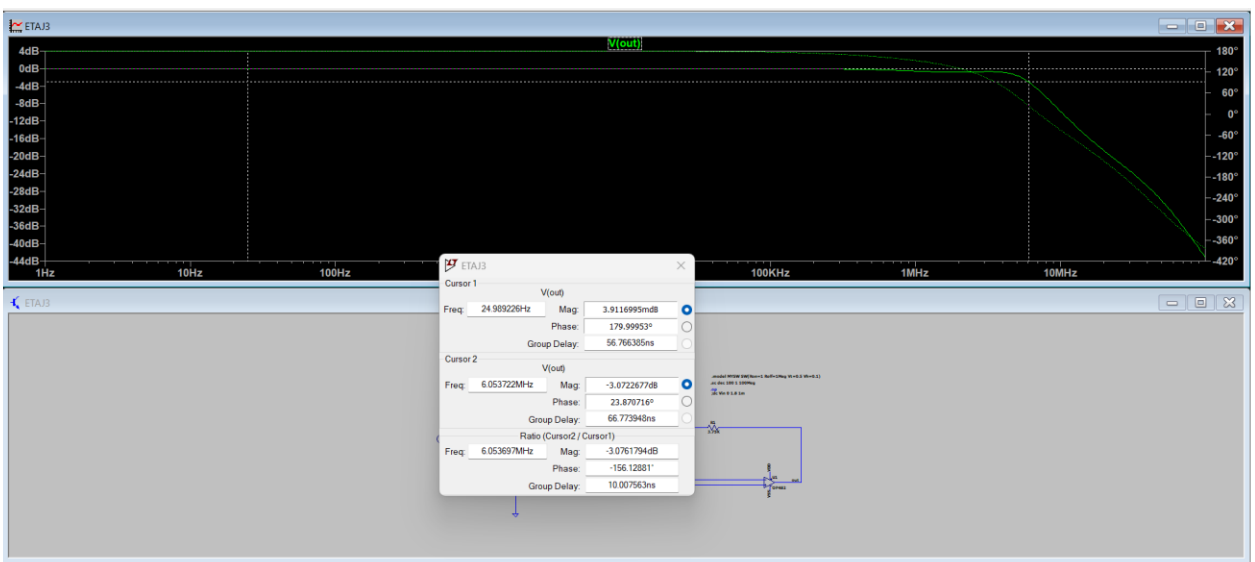
- SW1= ON , SW2 = SW4 = SW4 = OFF

Minimum amplitude

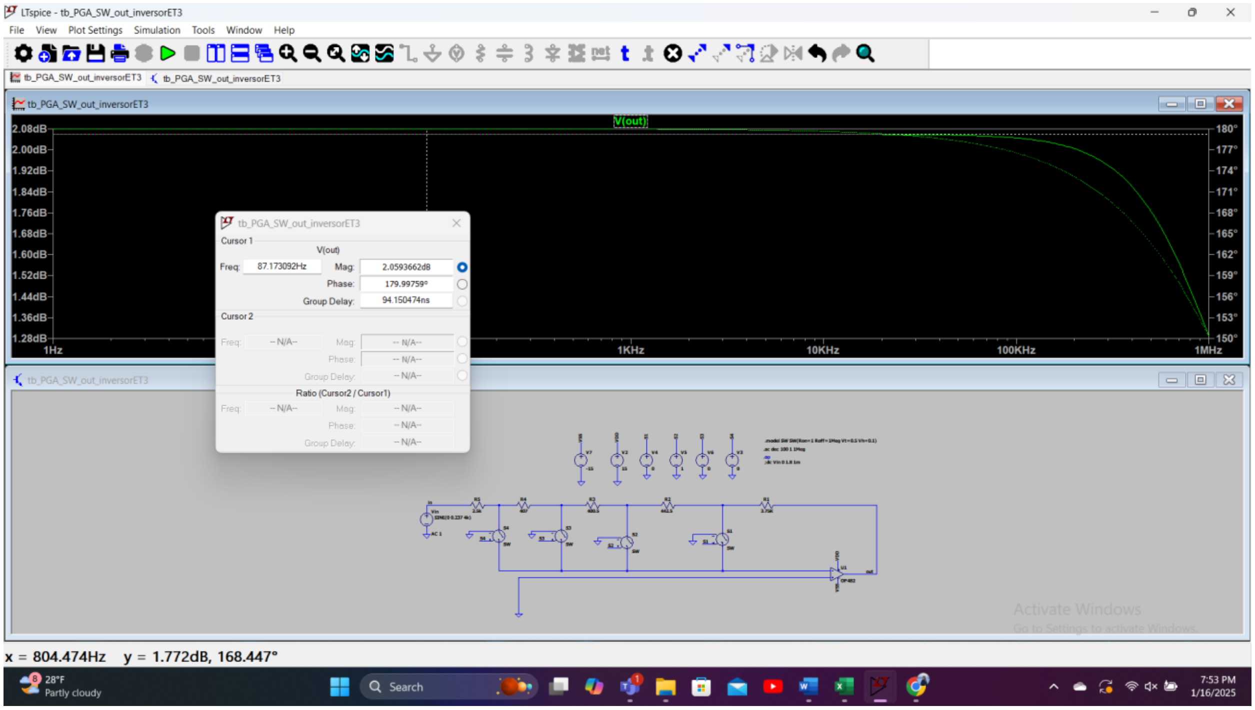


From the specifications: AdB=0 dB.
From the simulation: AdB=4.04mdB.

Bandwidth for SW1-ON > Specs Bandwidth

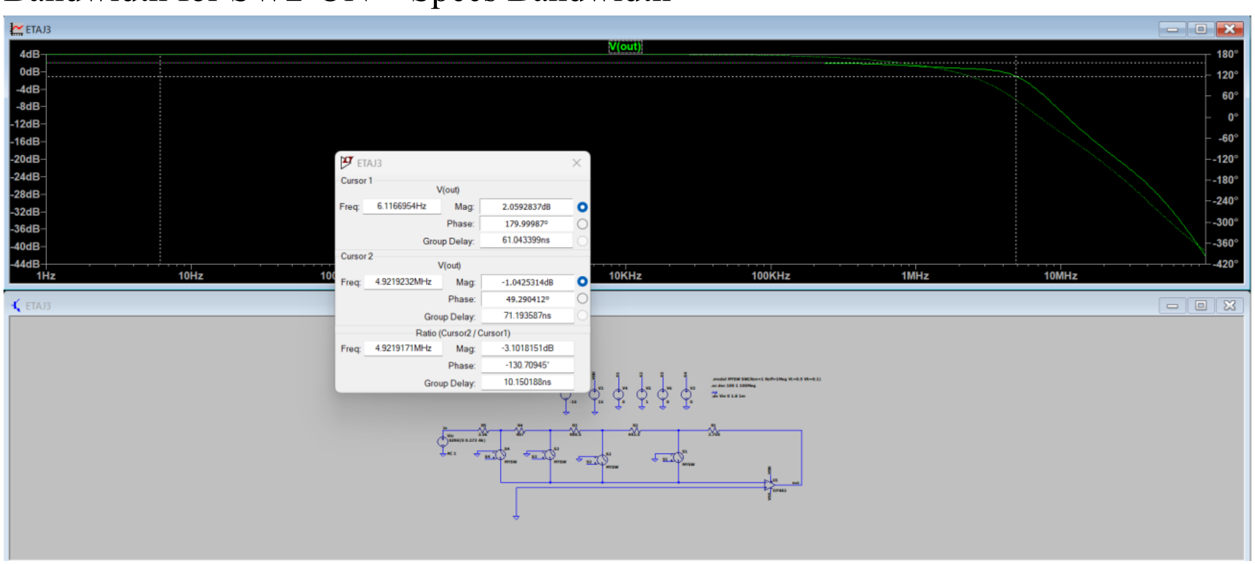


- SW2= ON , SW1 = SW3 = SW4 = OFF

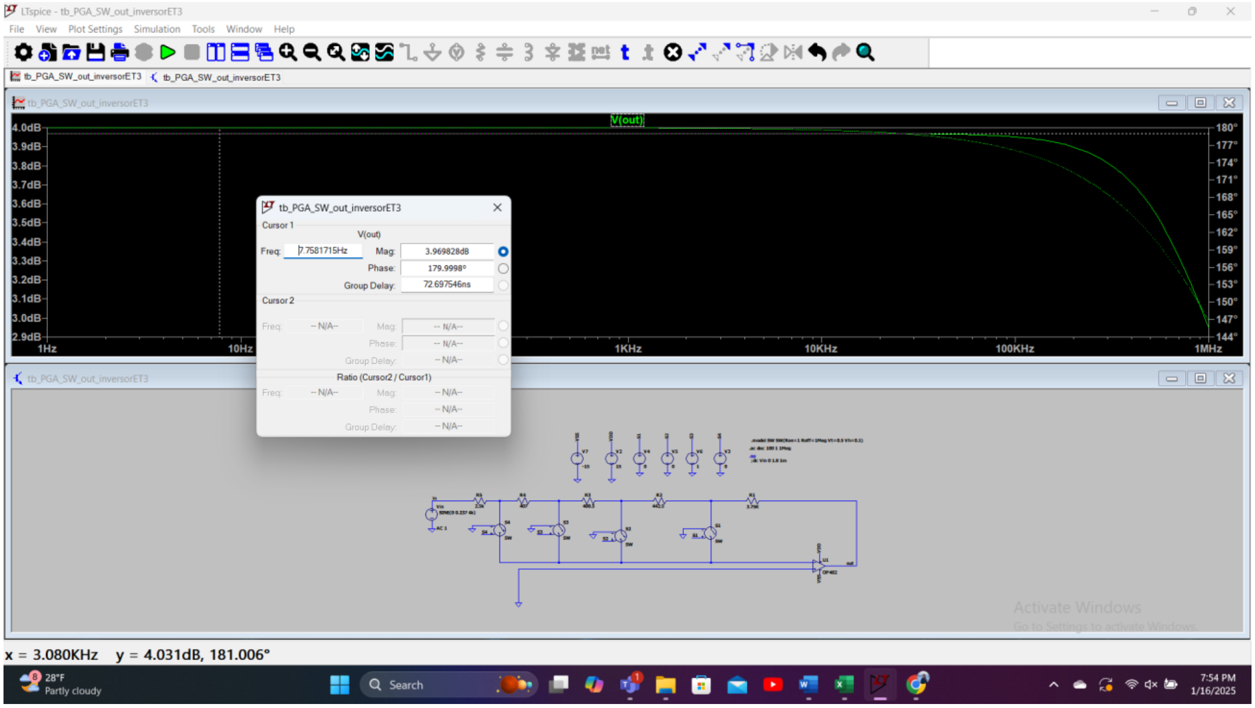


From the specifications: AdB=2 dB.
From the simulation: AdB=2.05dB

Bandwidth for SW2-ON > Specs Bandwidth



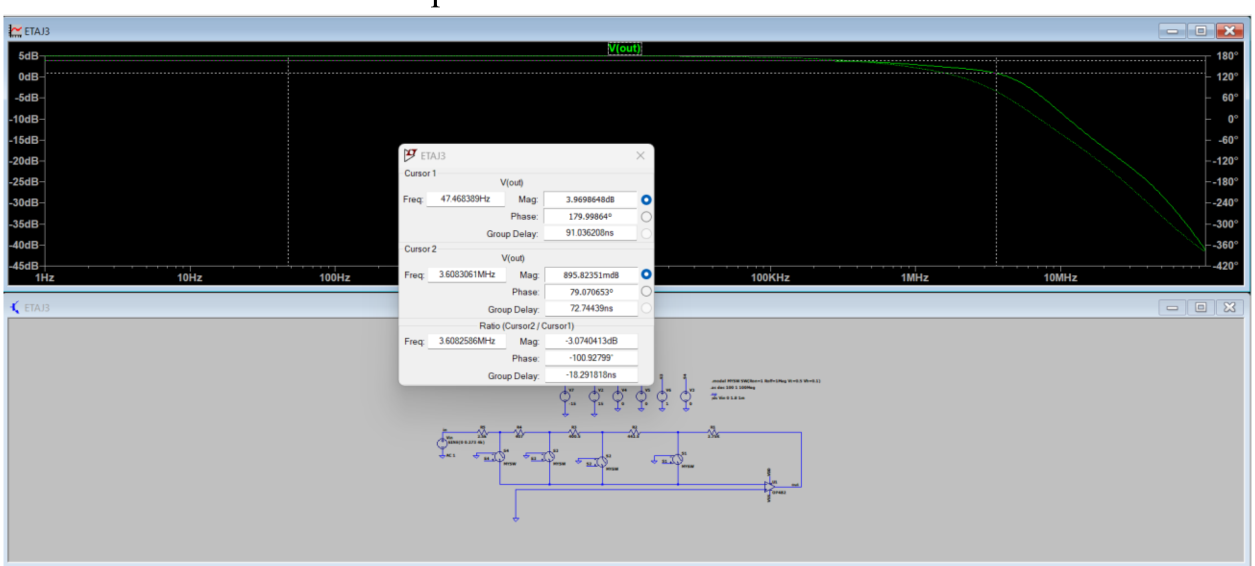
- SW3= ON , SW1 = SW2 = SW4 = OFF



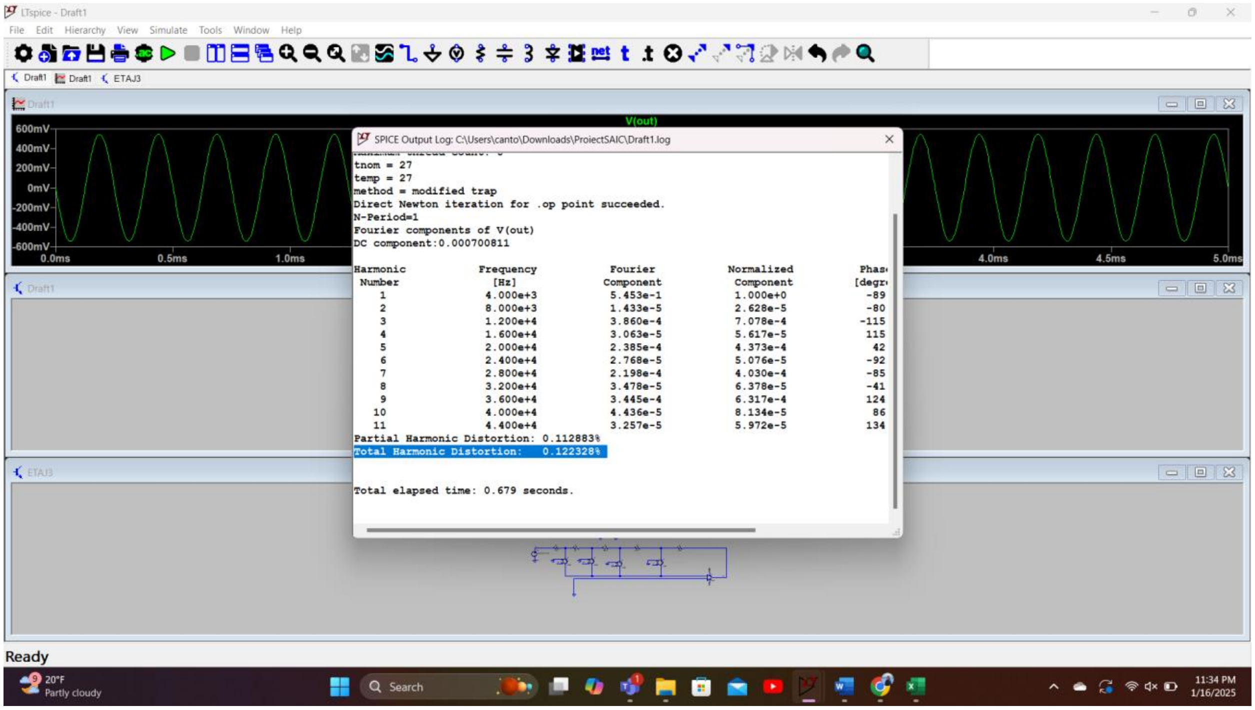
From the specifications: AdB=4 dB.

From the simulation: AdB=3.96dB

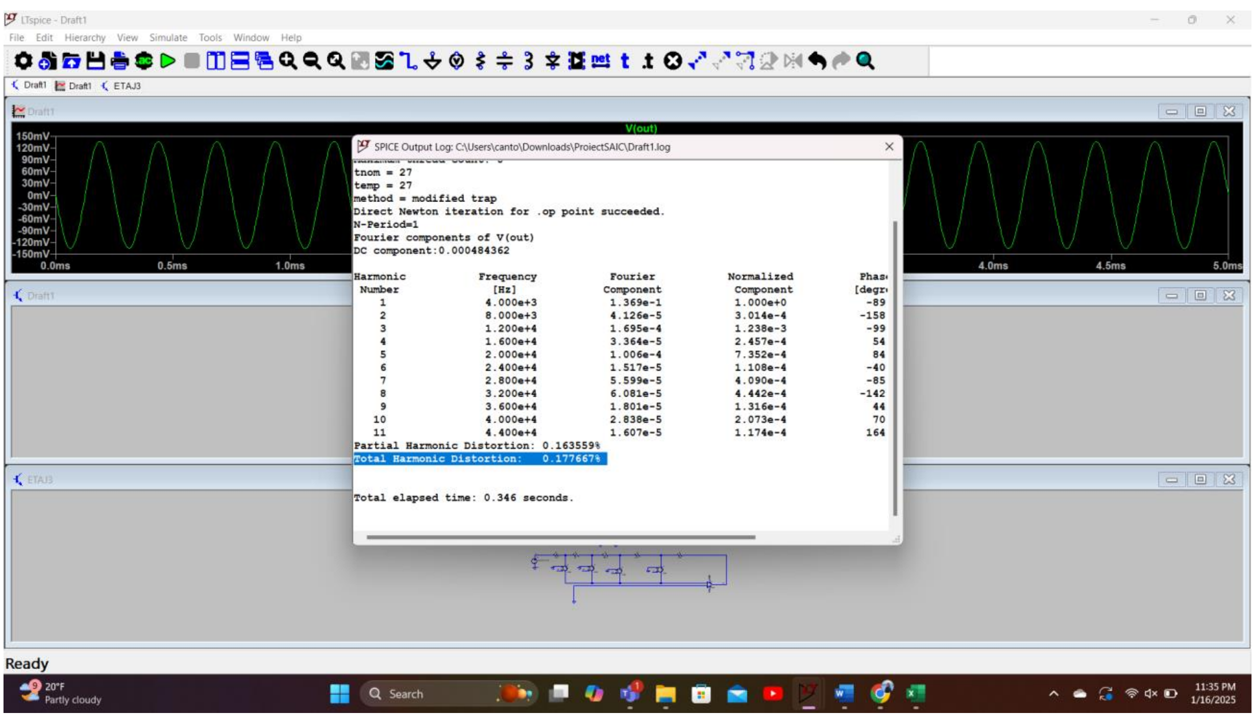
Bandwidth for SW2-ON > Specs Bandwidth



THD < 1% for Maximum Gain

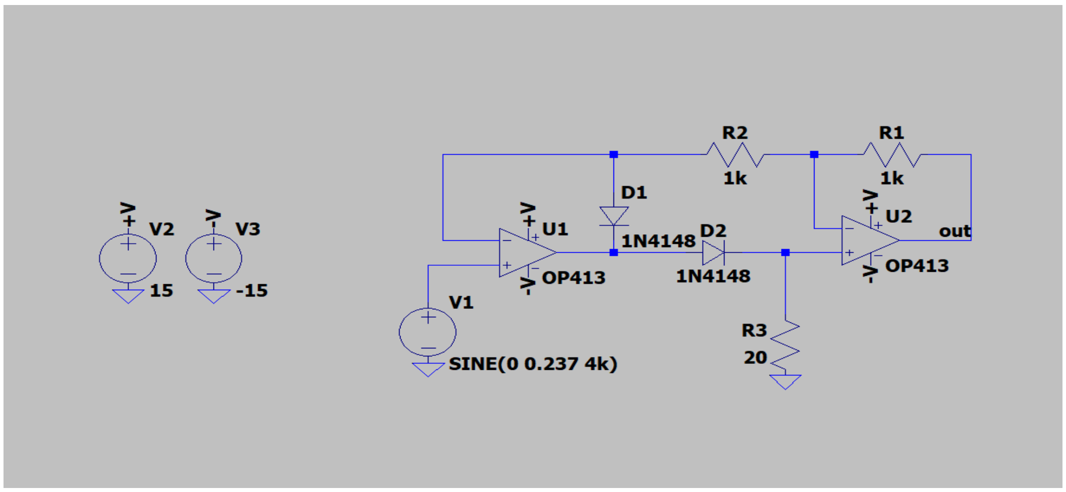


THD < 1% for Minimum Gain



Stage 4 – Full-Wave Rectifier

Following the simulations, we observed that, due to the operational amplifier used (OP482), the circuit is unstable. For this reason, we replaced the OP482 amplifier with the OP413 and reran all simulations using this component.

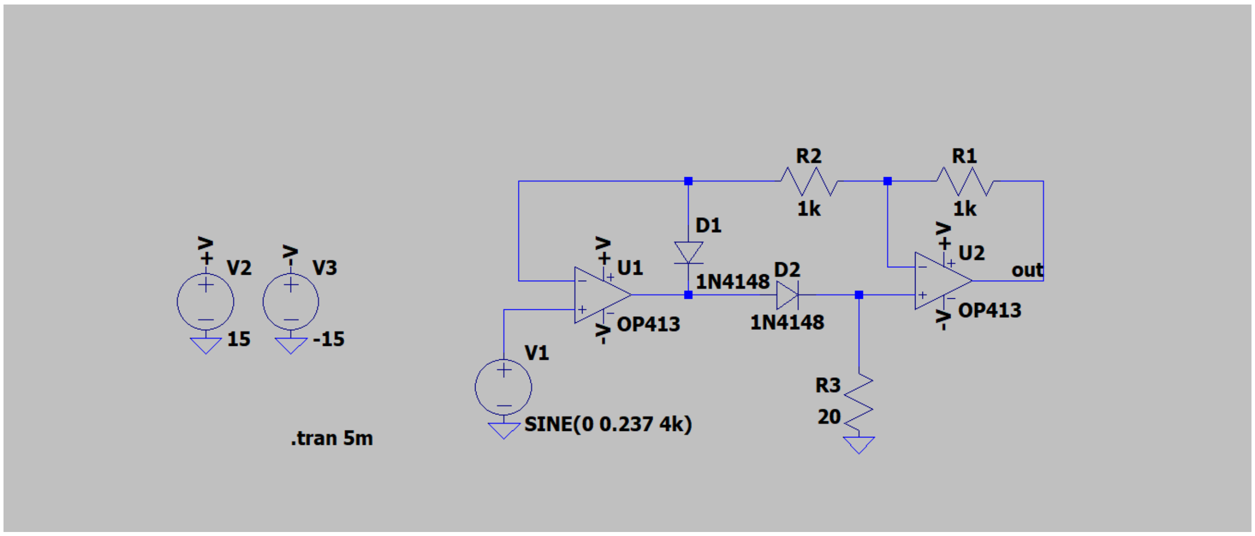


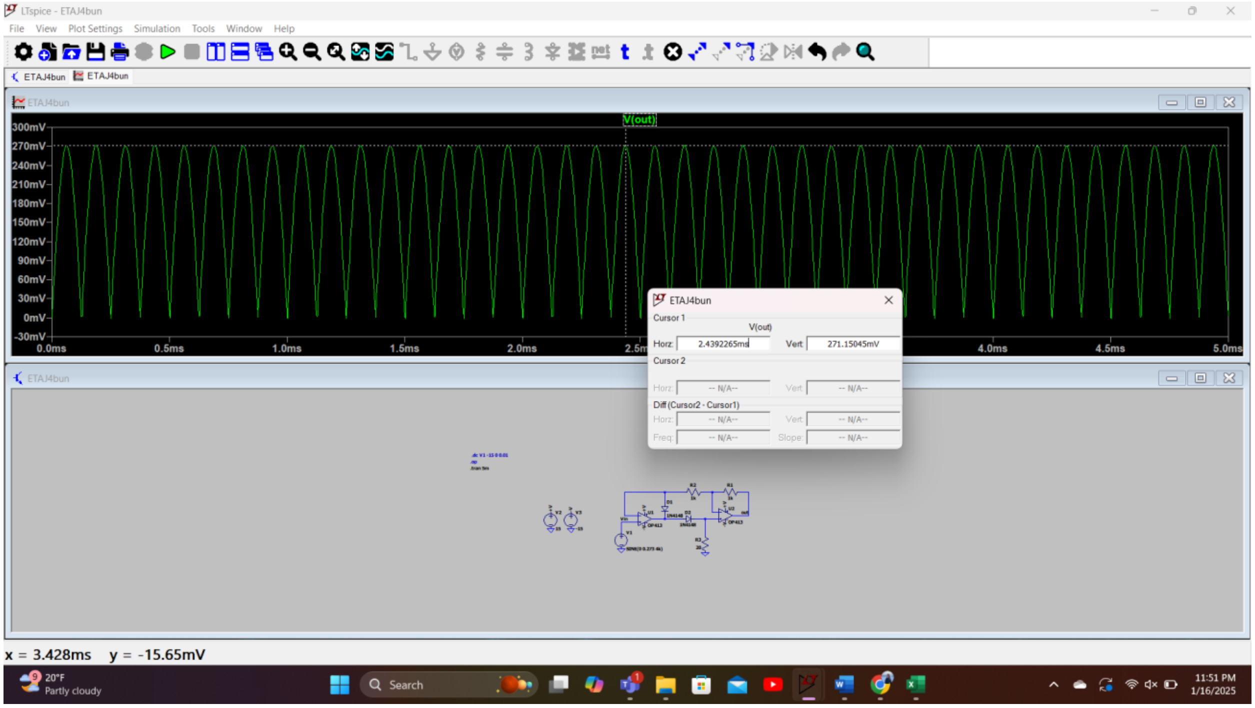
DCOP – Static Operating Point

```
* C:\Users\canto\Downloads\ProiectSAIC\ETAJ4bun.asc

       --- Operating Point ---

V(-v):          -15             voltage
V(+v):          15              voltage
V(n001):        -2.52621e-05    voltage
V(vin):         0               voltage
V(n003):        -0.203082       voltage
V(n002):        -2.00232e-05    voltage
V(n004):        5.24624e-06     voltage
V(out):         -0.00022959     voltage
I(D1):          2.20045e-07     device_current
I(D2):          -2.49169e-09    device_current
I(R1):          -2.09567e-07    device_current
I(R2):          5.23893e-09     device_current
I(R3):          -2.62312e-07    device_current
I(V1):          2.64804e-07     device_current
I(V2):          -0.0033502      device_current
I(V3):          0.00334967      device_current
Ix(u1:3):       -2.64804e-07    subckt_current
Ix(u1:2):       -2.14806e-07    subckt_current
Ix(u1:7):       0.00167519      subckt_current
Ix(u1:4):       -0.00167493     subckt_current
Ix(u1:6):       2.22537e-07     subckt_current
Ix(u2:3):       -2.64804e-07    subckt_current
Ix(u2:2):       -2.14806e-07    subckt_current
Ix(u2:7):       0.00167501      subckt_current
Ix(u2:4):       -0.00167474     subckt_current
Ix(u2:6):       2.09567e-07     subckt_current
```

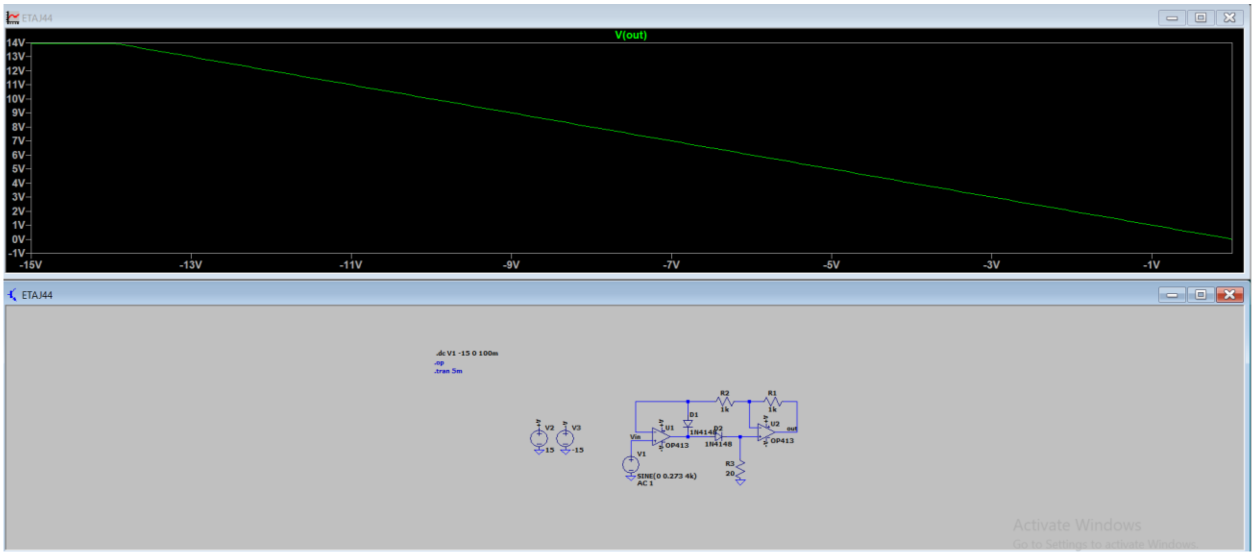
DC Sweep + Transient – Gain = Specs

Since the gain is 1, the output should produce a signal with an amplitude equal to the value of the input signal amplitude (0.273 V).





DC SWEEP

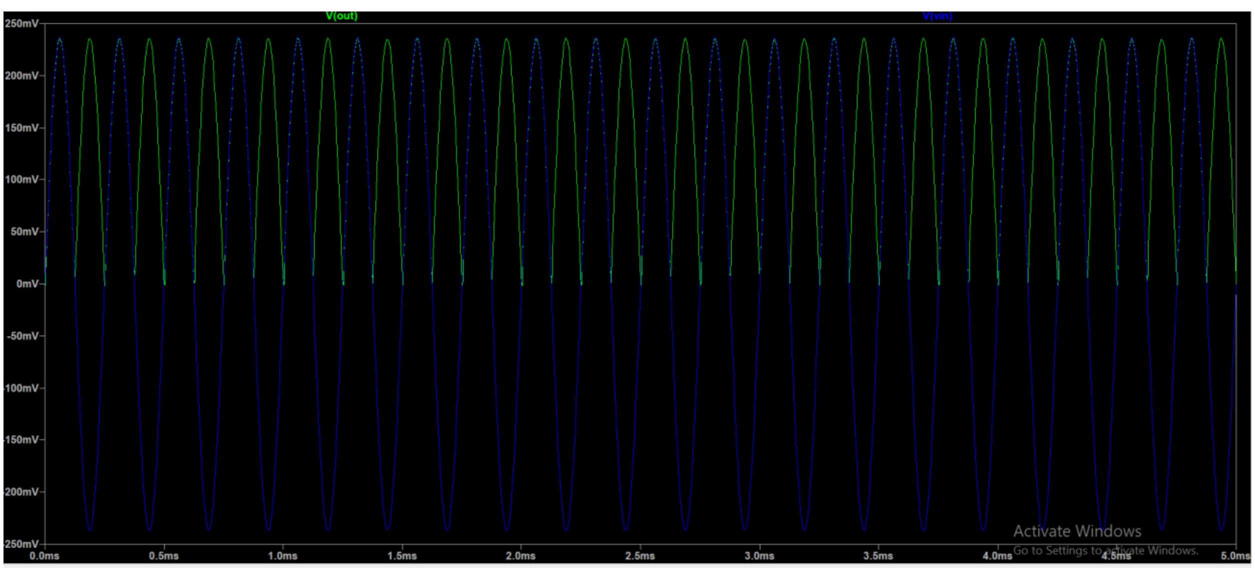


Transient – Circuit Function Implementation

We have a full-wave rectifier for which we calculated:

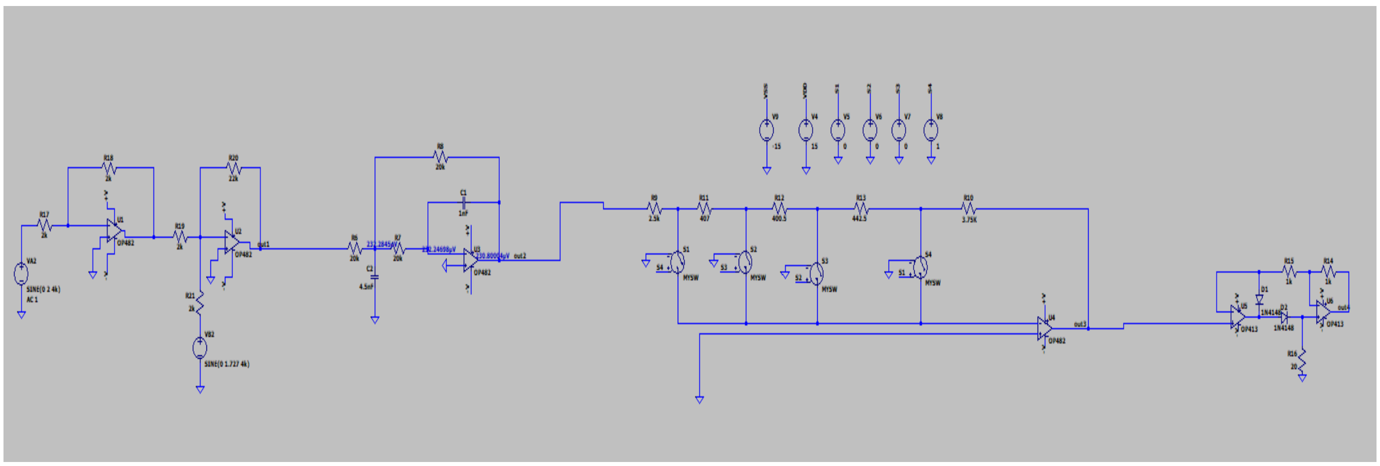
$$V_{out} = \begin{cases} -\frac{R_2}{R_1}V_{in}, & V_{in} > 0 \\ 0, & V_{in} > 0 \end{cases} \Longrightarrow \begin{cases} V_{out} = V_{in}, & V_{in} < 0 \\ 0, & V_{in} < 0 \end{cases}$$

From the calculations, we observe that at the output, we only have the positive alternation.

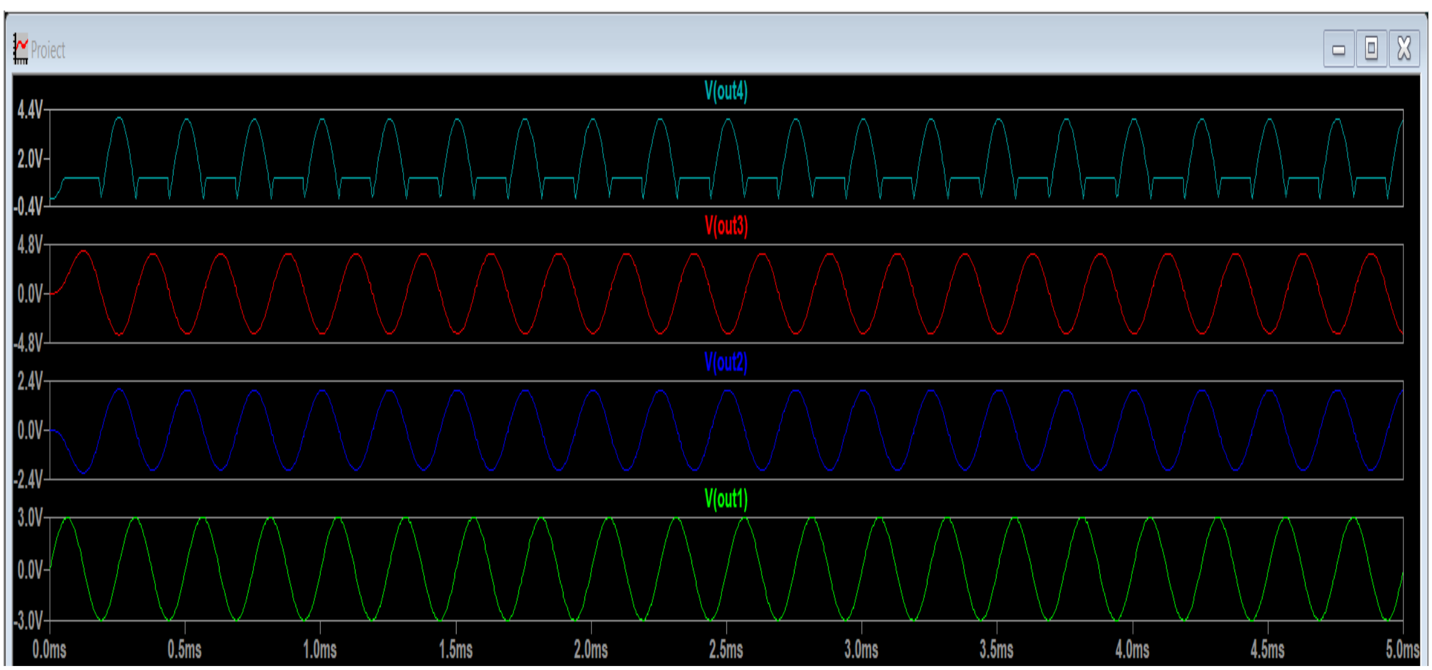


4. Verification and Characterization of the Analog Interface

To verify the functionality of the circuit, we will perform a transient analysis. At the input of the analog interface, a sinusoidal signal with a frequency of 4 kHz and an amplitude equal to the maximum value specified in the project specifications (0.273) will be applied.



The outputs for each stage are generated below.



4.CONCLUSIONS

ETAJUL 1

Specificatii individuale				Masuratori			
|Castig|	Banda (etaj 2)	SR	Liniaritate	Castig	Banda	SR	Liniaritate
11(= 20.8dB)	4000Hz	-	fara distorsiuni la fin_max pt ampl_in*castig (SR, THD<1%)	20.8dB	197kHz	-	THD = 0.0192% (pt amplit. in 0.273)

ETAJUL 2

Specificatii individuale			Masuratori		
|H0| (castig liniar in banda de trecere)	Banda	Liniaritate	|H0| (castig liniar in banda de trecere)	Banda	Liniaritate
1	7000Hz	amplitudinea de la iesire = (amplitudinea de la intrare)X(castigul in banda de trecere) pentru un semnal armonic cu frecventa = frecventa centrala LPF	999.9mV	3.78KHz	THD = 0.159%

ETAJUL 3

Specificatii individuale (Castig)				Masuratori (Castig)			
SW1 ON	SW2 ON	SW3 ON	SW4 ON	SW1 ON	SW2 ON	SW3 ON	SW4 ON
0dB	2dB	4dB	6dB	4.04mdB	2.05dB	3.96dB	6.01dB

Specificatii individuale (Banda)				Masuratori (banda)			
SW1 ON	**SW2 ON**	**SW3 ON**	**SW4 ON**	**SW1 ON**	**SW2 ON**	**SW3 ON**	**SW4 ON**
>4kHz	>4kHz	>4kHz	>4kHz	6.05MHz	4.92MHz	3.6MHz	2.36MHz

Specificatii Individuale		Masuratori	
Liniaritate		**Liniaritate**	
Castig minim	Castig maxim	Castig minim	Castig maxim
fara distorsiuni la fin_max pt ampl_in_min*castig_max_PGA	fara distorsiuni la fin_max pt ampli_in_max*castig_min_PGA	THD = 0.177% (pt amplit. in 1.25V)	THD = 0.122% (pt amplit. in 0.44V)

ETAJUL 4

Specificatii Individuale		Masuratori	
|Castig|	**Liniaritate**	**Castig|**	**Liniaritate**
1(=0dB)	circuitul are functia dorita pe domeniul= vin_max*castig	1	