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# 

# Теоретическая часть

## Вариант 15

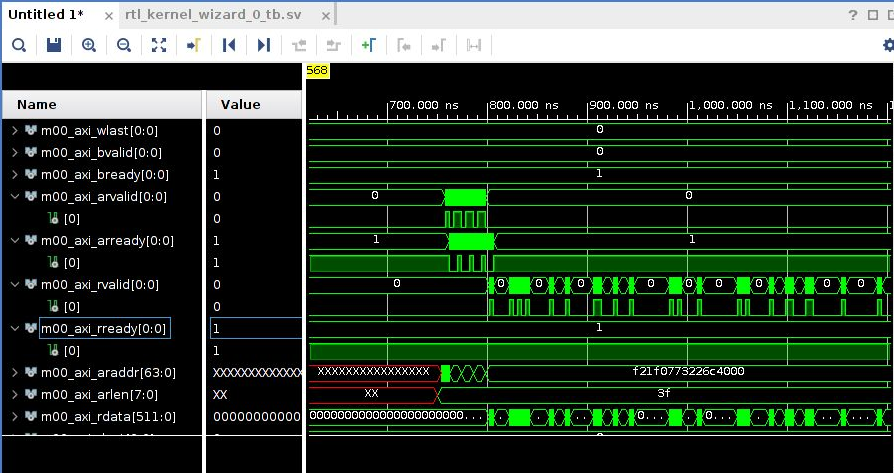


# Практическая часть

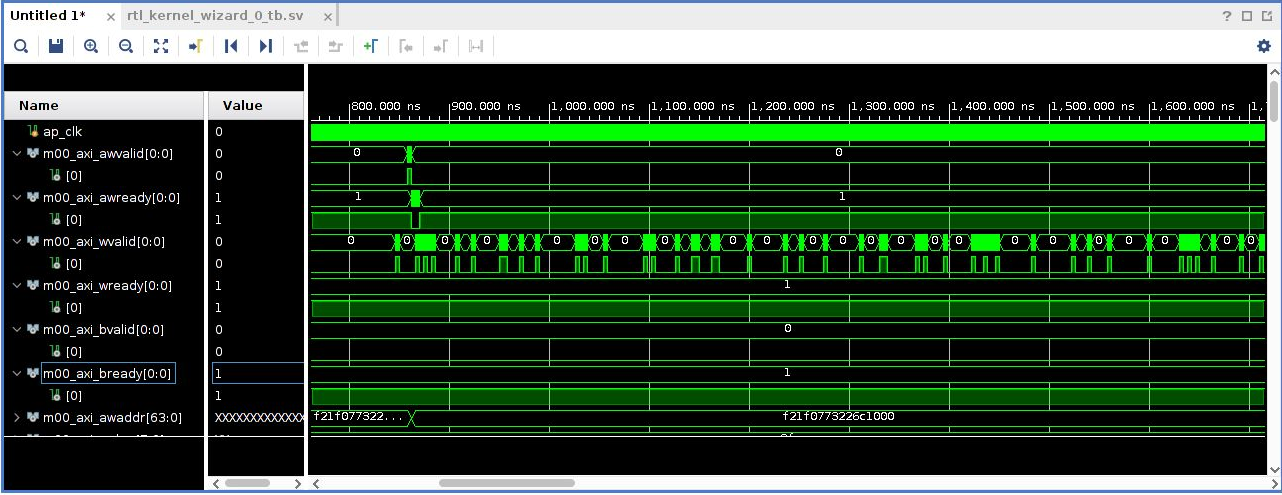
## Общее задание

### Диаграммы

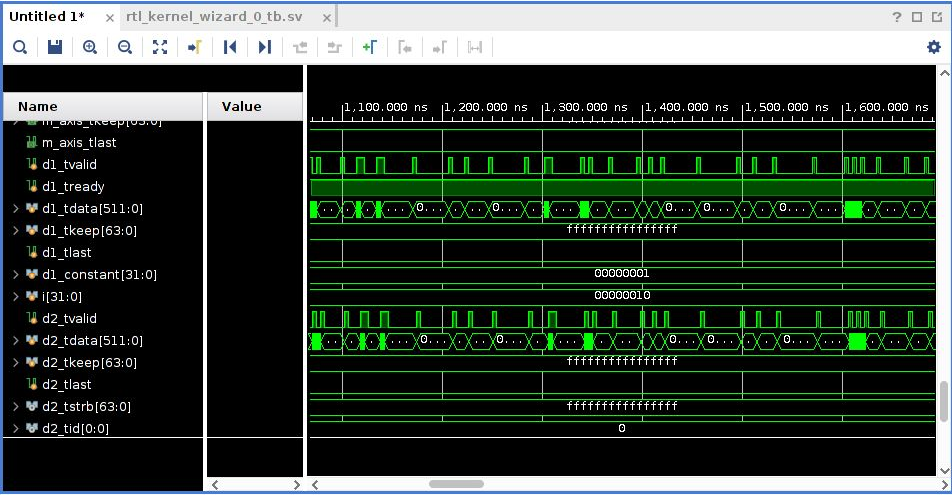
#### Транзакция чтения данных



#### Транзакция записи результата



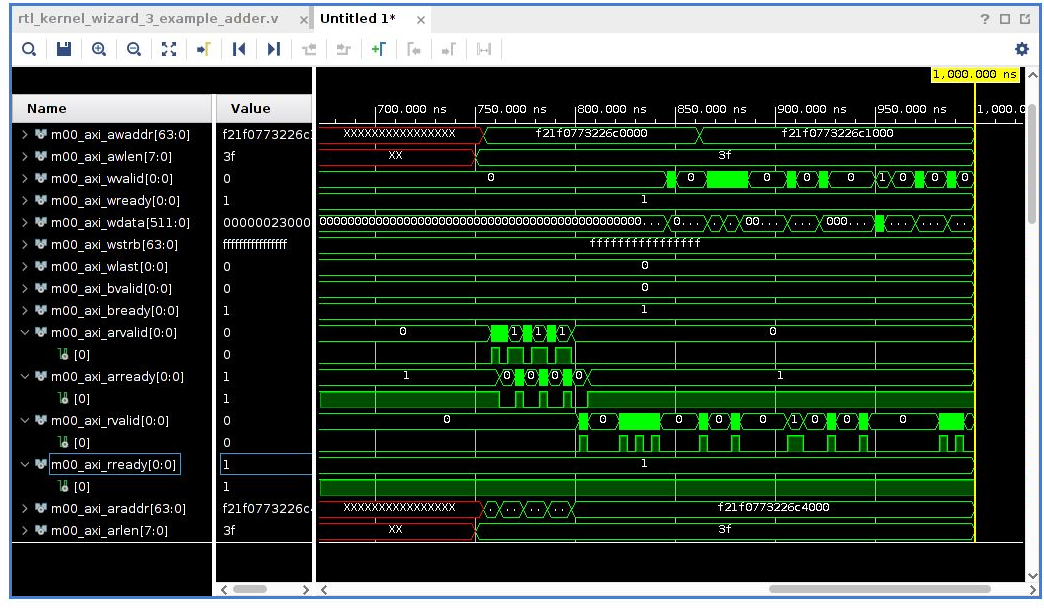
#### Инкремент данных



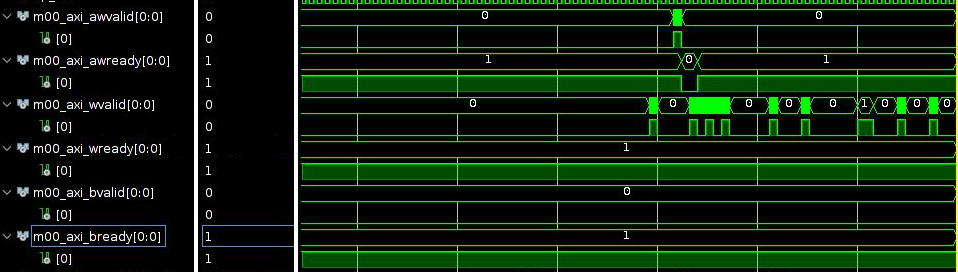
## Индивидуальное задание

### Диаграммы

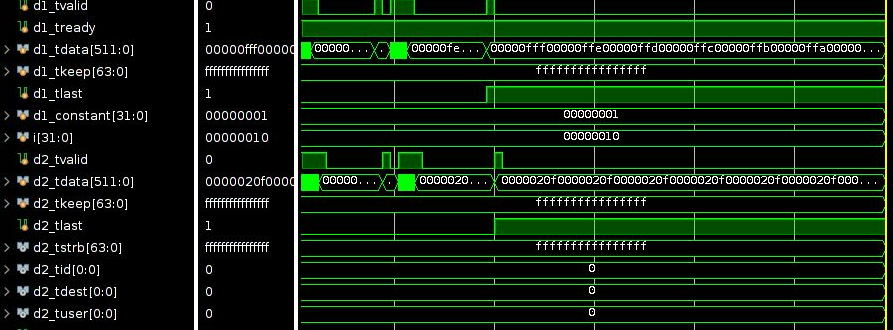
#### Транзакция чтения данных



#### Транзакция записи результата



#### Инкремент данных



### Листинги

#### Конфигурационный файл

[connectivity]

nk=rtl\_kernel\_wizard\_2:1:vinc0

slr=vinc0:SLR1

sp=vinc0.m00\_axi:DDR[2]

sp=vinc0.m00\_axi:PLRAM[0]

[vivado]

prop=run.impl\_1.STEPS.OPT\_DESIGN.ARGS.DIRECTIVE=Explore

prop=run.impl\_1.STEPS.PLACE\_DESIGN.ARGS.DIRECTIVE=Explore

prop=run.impl\_1.STEPS.PHYS\_OPT\_DESIGN.IS\_ENABLED=true

prop=run.impl\_1.STEPS.PHYS\_OPT\_DESIGN.ARGS.DIRECTIVE=AggressiveExplore

prop=run.impl\_1.STEPS.ROUTE\_DESIGN.ARGS.DIRECTIVE=Explore

#### v++\*.log

INFO: [v++ 60-1306] Additional information associated with this v++ link can be found at:

Reports: /iu\_home/iu7075/workspace/\_x/reports/link

Log files: /iu\_home/iu7075/workspace/\_x/logs/link

INFO: [v++ 60-1548] Creating build summary session with primary output /iu\_home/iu7075/workspace/out/vinc.xclbin.link\_summary, at Sun Dec 5 14:57:19 2021

INFO: [v++ 60-1316] Initiating connection to rulecheck server, at Sun Dec 5 14:57:20 2021

INFO: [v++ 60-1315] Creating rulecheck session with output '/iu\_home/iu7075/workspace/\_x/reports/link/v++\_link\_vinc\_guidance.html', at Sun Dec 5 14:57:43 2021

INFO: [v++ 60-895] Target platform: /opt/xilinx/platforms/xilinx\_u200\_xdma\_201830\_2/xilinx\_u200\_xdma\_201830\_2.xpfm

INFO: [v++ 60-1578] This platform contains Device Support Archive '/opt/xilinx/platforms/xilinx\_u200\_xdma\_201830\_2/hw/xilinx\_u200\_xdma\_201830\_2.dsa'

INFO: [v++ 74-74] Compiler Version string: 2020.2

INFO: [v++ 60-1302] Platform 'xilinx\_u200\_xdma\_201830\_2.xpfm' has been explicitly enabled for this release.

INFO: [v++ 60-629] Linking for hardware target

INFO: [v++ 60-423] Target device: xilinx\_u200\_xdma\_201830\_2

INFO: [v++ 60-1332] Run 'run\_link' status: Not started

INFO: [v++ 60-1443] [14:58:59] Run run\_link: Step system\_link: Started

INFO: [v++ 60-1453] Command Line: system\_link --xo /iu\_home/iu7075/workspace/deniska\_lab\_04\_kernels/vivado\_rtl\_kernel/rtl\_kernel\_wizard\_2\_ex/exports/rtl\_kernel\_wizard\_2.xo --config /iu\_home/iu7075/workspace/\_x/link/int/syslinkConfig.ini --xpfm /opt/xilinx/platforms/xilinx\_u200\_xdma\_201830\_2/xilinx\_u200\_xdma\_201830\_2.xpfm --target hw --output\_dir /iu\_home/iu7075/workspace/\_x/link/int --temp\_dir /iu\_home/iu7075/workspace/\_x/link/sys\_link

INFO: [v++ 60-1454] Run Directory: /iu\_home/iu7075/workspace/\_x/link/run\_link

INFO: [SYSTEM\_LINK 60-1316] Initiating connection to rulecheck server, at Sun Dec 5 14:59:17 2021

INFO: [SYSTEM\_LINK 82-70] Extracting xo v3 file /iu\_home/iu7075/workspace/deniska\_lab\_04\_kernels/vivado\_rtl\_kernel/rtl\_kernel\_wizard\_2\_ex/exports/rtl\_kernel\_wizard\_2.xo

INFO: [SYSTEM\_LINK 82-53] Creating IP database /iu\_home/iu7075/workspace/\_x/link/sys\_link/\_sysl/.cdb/xd\_ip\_db.xml

INFO: [SYSTEM\_LINK 82-38] [14:59:21] build\_xd\_ip\_db started: /data/Xilinx/Vitis/2020.2/bin/build\_xd\_ip\_db -ip\_search 0 -sds-pf /iu\_home/iu7075/workspace/\_x/link/sys\_link/xilinx\_u200\_xdma\_201830\_2.hpfm -clkid 0 -ip /iu\_home/iu7075/workspace/\_x/link/sys\_link/iprepo/mycompany\_com\_kernel\_rtl\_kernel\_wizard\_2\_1\_0,rtl\_kernel\_wizard\_2 -o /iu\_home/iu7075/workspace/\_x/link/sys\_link/\_sysl/.cdb/xd\_ip\_db.xml

INFO: [SYSTEM\_LINK 82-37] [15:00:03] build\_xd\_ip\_db finished successfully

Time (s): cpu = 00:00:44 ; elapsed = 00:00:42 . Memory (MB): peak = 1557.895 ; gain = 0.000 ; free physical = 190649 ; free virtual = 318780

INFO: [SYSTEM\_LINK 82-51] Create system connectivity graph

INFO: [SYSTEM\_LINK 82-102] Applying explicit connections to the system connectivity graph: /iu\_home/iu7075/workspace/\_x/link/sys\_link/cfgraph/cfgen\_cfgraph.xml

INFO: [SYSTEM\_LINK 82-38] [15:00:04] cfgen started: /data/Xilinx/Vitis/2020.2/bin/cfgen -nk rtl\_kernel\_wizard\_2:1:vinc0 -slr vinc0:SLR1 -sp vinc0.m00\_axi:DDR[2] -sp vinc0.m00\_axi:PLRAM[0] -dmclkid 0 -r /iu\_home/iu7075/workspace/\_x/link/sys\_link/\_sysl/.cdb/xd\_ip\_db.xml -o /iu\_home/iu7075/workspace/\_x/link/sys\_link/cfgraph/cfgen\_cfgraph.xml

INFO: [CFGEN 83-0] Kernel Specs:

INFO: [CFGEN 83-0] kernel: rtl\_kernel\_wizard\_2, num: 1 {vinc0}

INFO: [CFGEN 83-0] Port Specs:

INFO: [CFGEN 83-0] kernel: vinc0, k\_port: m00\_axi, sptag: DDR[2]

INFO: [CFGEN 83-0] kernel: vinc0, k\_port: m00\_axi, sptag: PLRAM[0]

INFO: [CFGEN 83-0] SLR Specs:

INFO: [CFGEN 83-0] instance: vinc0, SLR: SLR1

INFO: [CFGEN 83-2228] Creating mapping for argument vinc0.axi00\_ptr0 to DDR[2] for directive vinc0.m00\_axi:DDR[2]

INFO: [SYSTEM\_LINK 82-37] [15:00:39] cfgen finished successfully

Time (s): cpu = 00:00:34 ; elapsed = 00:00:35 . Memory (MB): peak = 1557.895 ; gain = 0.000 ; free physical = 190674 ; free virtual = 318812

INFO: [SYSTEM\_LINK 82-52] Create top-level block diagram

INFO: [SYSTEM\_LINK 82-38] [15:00:39] cf2bd started: /data/Xilinx/Vitis/2020.2/bin/cf2bd --linux --trace\_buffer 1024 --input\_file /iu\_home/iu7075/workspace/\_x/link/sys\_link/cfgraph/cfgen\_cfgraph.xml --ip\_db /iu\_home/iu7075/workspace/\_x/link/sys\_link/\_sysl/.cdb/xd\_ip\_db.xml --cf\_name dr --working\_dir /iu\_home/iu7075/workspace/\_x/link/sys\_link/\_sysl/.xsd --temp\_dir /iu\_home/iu7075/workspace/\_x/link/sys\_link --output\_dir /iu\_home/iu7075/workspace/\_x/link/int --target\_bd pfm\_dynamic.bd

INFO: [CF2BD 82-31] Launching cf2xd: cf2xd -linux -trace-buffer 1024 -i /iu\_home/iu7075/workspace/\_x/link/sys\_link/cfgraph/cfgen\_cfgraph.xml -r /iu\_home/iu7075/workspace/\_x/link/sys\_link/\_sysl/.cdb/xd\_ip\_db.xml -o dr.xml

INFO: [CF2BD 82-28] cf2xd finished successfully

INFO: [CF2BD 82-31] Launching cf\_xsd: cf\_xsd -disable-address-gen -bd pfm\_dynamic.bd -dn dr -dp /iu\_home/iu7075/workspace/\_x/link/sys\_link/\_sysl/.xsd

INFO: [CF2BD 82-28] cf\_xsd finished successfully

INFO: [SYSTEM\_LINK 82-37] [15:00:59] cf2bd finished successfully

Time (s): cpu = 00:00:17 ; elapsed = 00:00:20 . Memory (MB): peak = 1557.895 ; gain = 0.000 ; free physical = 190584 ; free virtual = 318710

INFO: [v++ 60-1441] [15:01:00] Run run\_link: Step system\_link: Completed

Time (s): cpu = 00:01:57 ; elapsed = 00:02:00 . Memory (MB): peak = 1585.129 ; gain = 0.000 ; free physical = 190636 ; free virtual = 318757

INFO: [v++ 60-1443] [15:01:00] Run run\_link: Step cf2sw: Started

INFO: [v++ 60-1453] Command Line: cf2sw -sdsl /iu\_home/iu7075/workspace/\_x/link/int/sdsl.dat -rtd /iu\_home/iu7075/workspace/\_x/link/int/cf2sw.rtd -nofilter /iu\_home/iu7075/workspace/\_x/link/int/cf2sw\_full.rtd -xclbin /iu\_home/iu7075/workspace/\_x/link/int/xclbin\_orig.xml -o /iu\_home/iu7075/workspace/\_x/link/int/xclbin\_orig.1.xml

INFO: [v++ 60-1454] Run Directory: /iu\_home/iu7075/workspace/\_x/link/run\_link

INFO: [v++ 60-1441] [15:01:23] Run run\_link: Step cf2sw: Completed

Time (s): cpu = 00:00:22 ; elapsed = 00:00:24 . Memory (MB): peak = 1585.129 ; gain = 0.000 ; free physical = 190536 ; free virtual = 318669

INFO: [v++ 60-1443] [15:01:23] Run run\_link: Step rtd2\_system\_diagram: Started

INFO: [v++ 60-1453] Command Line: rtd2SystemDiagram

INFO: [v++ 60-1454] Run Directory: /iu\_home/iu7075/workspace/\_x/link/run\_link

INFO: [v++ 60-1441] [15:01:37] Run run\_link: Step rtd2\_system\_diagram: Completed

Time (s): cpu = 00:00:00.02 ; elapsed = 00:00:14 . Memory (MB): peak = 1585.129 ; gain = 0.000 ; free physical = 190052 ; free virtual = 318182

INFO: [v++ 60-1443] [15:01:38] Run run\_link: Step vpl: Started

INFO: [v++ 60-1453] Command Line: vpl -t hw -f xilinx\_u200\_xdma\_201830\_2 --remote\_ip\_cache /iu\_home/iu7075/workspace/.ipcache --output\_dir /iu\_home/iu7075/workspace/\_x/link/int --log\_dir /iu\_home/iu7075/workspace/\_x/logs/link --report\_dir /iu\_home/iu7075/workspace/\_x/reports/link --config /iu\_home/iu7075/workspace/\_x/link/int/vplConfig.ini -k /iu\_home/iu7075/workspace/\_x/link/int/kernel\_info.dat --webtalk\_flag Vitis --temp\_dir /iu\_home/iu7075/workspace/\_x/link --no-info --iprepo /iu\_home/iu7075/workspace/\_x/link/int/xo/ip\_repo/mycompany\_com\_kernel\_rtl\_kernel\_wizard\_2\_1\_0 --messageDb /iu\_home/iu7075/workspace/\_x/link/run\_link/vpl.pb /iu\_home/iu7075/workspace/\_x/link/int/dr.bd.tcl

INFO: [v++ 60-1454] Run Directory: /iu\_home/iu7075/workspace/\_x/link/run\_link

\*\*\*\*\*\* vpl v2020.2 (64-bit)

\*\*\*\* SW Build (by xbuild) on 2020-11-18-05:13:29

\*\* Copyright 1986-2020 Xilinx, Inc. All Rights Reserved.

INFO: [VPL 60-839] Read in kernel information from file '/iu\_home/iu7075/workspace/\_x/link/int/kernel\_info.dat'.

INFO: [VPL 74-74] Compiler Version string: 2020.2

INFO: [VPL 60-423] Target device: xilinx\_u200\_xdma\_201830\_2

INFO: [VPL 60-1032] Extracting hardware platform to /iu\_home/iu7075/workspace/\_x/link/vivado/vpl/.local/hw\_platform

WARNING: /data/Xilinx/Vitis/2020.2/tps/lnx64/jre9.0.4 does not exist.

[15:08:06] Run vpl: Step create\_project: RUNNING...

[15:08:00] Run vpl: Step create\_project: Started

Creating Vivado project.

[15:08:34] Run vpl: Step create\_project: Completed

[15:08:34] Run vpl: Step create\_bd: Started

[15:10:13] Run vpl: Step create\_bd: RUNNING...

[15:11:51] Run vpl: Step create\_bd: RUNNING...

[15:13:21] Run vpl: Step create\_bd: RUNNING...

[15:15:03] Run vpl: Step create\_bd: RUNNING...

[15:16:40] Run vpl: Step create\_bd: RUNNING...

[15:18:15] Run vpl: Step create\_bd: RUNNING...

[15:19:24] Run vpl: Step create\_bd: Completed

[15:19:24] Run vpl: Step update\_bd: Started

[15:19:27] Run vpl: Step update\_bd: Completed

[15:19:27] Run vpl: Step generate\_target: Started

[15:21:02] Run vpl: Step generate\_target: RUNNING...

[15:22:34] Run vpl: Step generate\_target: RUNNING...

[15:24:01] Run vpl: Step generate\_target: RUNNING...

[15:25:33] Run vpl: Step generate\_target: RUNNING...

[15:26:57] Run vpl: Step generate\_target: RUNNING...

[15:28:28] Run vpl: Step generate\_target: RUNNING...

[15:29:53] Run vpl: Step generate\_target: RUNNING...

[15:31:24] Run vpl: Step generate\_target: RUNNING...

[15:32:37] Run vpl: Step generate\_target: Completed

[15:32:37] Run vpl: Step config\_hw\_runs: Started

[15:34:13] Run vpl: Step config\_hw\_runs: RUNNING...

[15:34:19] Run vpl: Step config\_hw\_runs: Completed

[15:34:19] Run vpl: Step synth: Started

[15:36:51] Block-level synthesis in progress, 0 of 66 jobs complete, 8 jobs running.

[15:37:29] Block-level synthesis in progress, 0 of 66 jobs complete, 8 jobs running.

[15:38:10] Block-level synthesis in progress, 0 of 66 jobs complete, 8 jobs running.

[15:38:47] Block-level synthesis in progress, 0 of 66 jobs complete, 8 jobs running.

[15:39:27] Block-level synthesis in progress, 0 of 66 jobs complete, 8 jobs running.

[15:40:05] Block-level synthesis in progress, 0 of 66 jobs complete, 8 jobs running.

[15:40:48] Block-level synthesis in progress, 0 of 66 jobs complete, 8 jobs running.

[15:41:25] Block-level synthesis in progress, 0 of 66 jobs complete, 8 jobs running.

[15:42:05] Block-level synthesis in progress, 0 of 66 jobs complete, 8 jobs running.

[15:42:44] Block-level synthesis in progress, 0 of 66 jobs complete, 8 jobs running.

[15:43:26] Block-level synthesis in progress, 0 of 66 jobs complete, 8 jobs running.

[15:44:01] Block-level synthesis in progress, 0 of 66 jobs complete, 8 jobs running.

[15:44:40] Block-level synthesis in progress, 0 of 66 jobs complete, 8 jobs running.

[15:45:16] Block-level synthesis in progress, 1 of 66 jobs complete, 7 jobs running.

[15:45:55] Block-level synthesis in progress, 6 of 66 jobs complete, 2 jobs running.

[15:46:30] Block-level synthesis in progress, 7 of 66 jobs complete, 1 job running.

[15:47:07] Block-level synthesis in progress, 7 of 66 jobs complete, 3 jobs running.

[15:47:42] Block-level synthesis in progress, 7 of 66 jobs complete, 8 jobs running.

[15:48:20] Block-level synthesis in progress, 7 of 66 jobs complete, 8 jobs running.

[15:48:56] Block-level synthesis in progress, 8 of 66 jobs complete, 7 jobs running.

[15:49:36] Block-level synthesis in progress, 8 of 66 jobs complete, 7 jobs running.

[15:50:14] Block-level synthesis in progress, 9 of 66 jobs complete, 7 jobs running.

[15:50:54] Block-level synthesis in progress, 9 of 66 jobs complete, 7 jobs running.

[15:51:31] Block-level synthesis in progress, 10 of 66 jobs complete, 6 jobs running.

[15:52:09] Block-level synthesis in progress, 10 of 66 jobs complete, 7 jobs running.

[15:52:44] Block-level synthesis in progress, 10 of 66 jobs complete, 8 jobs running.

[15:53:21] Block-level synthesis in progress, 11 of 66 jobs complete, 7 jobs running.

[15:53:56] Block-level synthesis in progress, 11 of 66 jobs complete, 7 jobs running.

[15:54:40] Block-level synthesis in progress, 11 of 66 jobs complete, 8 jobs running.

[15:55:17] Block-level synthesis in progress, 11 of 66 jobs complete, 8 jobs running.

[15:56:04] Block-level synthesis in progress, 12 of 66 jobs complete, 7 jobs running.

[15:56:42] Block-level synthesis in progress, 15 of 66 jobs complete, 4 jobs running.

[15:57:23] Block-level synthesis in progress, 17 of 66 jobs complete, 3 jobs running.

[15:57:58] Block-level synthesis in progress, 17 of 66 jobs complete, 6 jobs running.

[15:58:38] Block-level synthesis in progress, 17 of 66 jobs complete, 7 jobs running.

[15:59:16] Block-level synthesis in progress, 17 of 66 jobs complete, 8 jobs running.

[15:59:58] Block-level synthesis in progress, 17 of 66 jobs complete, 8 jobs running.

[16:00:34] Block-level synthesis in progress, 17 of 66 jobs complete, 8 jobs running.

[16:01:17] Block-level synthesis in progress, 17 of 66 jobs complete, 8 jobs running.

[16:01:53] Block-level synthesis in progress, 17 of 66 jobs complete, 8 jobs running.

[16:02:33] Block-level synthesis in progress, 18 of 66 jobs complete, 7 jobs running.

[16:03:08] Block-level synthesis in progress, 19 of 66 jobs complete, 6 jobs running.

[16:03:48] Block-level synthesis in progress, 19 of 66 jobs complete, 6 jobs running.

[16:04:26] Block-level synthesis in progress, 19 of 66 jobs complete, 8 jobs running.

[16:05:03] Block-level synthesis in progress, 20 of 66 jobs complete, 7 jobs running.

[16:05:38] Block-level synthesis in progress, 21 of 66 jobs complete, 6 jobs running.

[16:06:18] Block-level synthesis in progress, 22 of 66 jobs complete, 5 jobs running.

[16:06:55] Block-level synthesis in progress, 25 of 66 jobs complete, 4 jobs running.

[16:07:35] Block-level synthesis in progress, 25 of 66 jobs complete, 4 jobs running.

[16:08:13] Block-level synthesis in progress, 26 of 66 jobs complete, 5 jobs running.

[16:08:50] Block-level synthesis in progress, 27 of 66 jobs complete, 6 jobs running.

[16:09:27] Block-level synthesis in progress, 29 of 66 jobs complete, 5 jobs running.

[16:10:02] Block-level synthesis in progress, 29 of 66 jobs complete, 5 jobs running.

[16:10:38] Block-level synthesis in progress, 30 of 66 jobs complete, 6 jobs running.

[16:11:12] Block-level synthesis in progress, 30 of 66 jobs complete, 7 jobs running.

[16:11:58] Block-level synthesis in progress, 30 of 66 jobs complete, 8 jobs running.

[16:12:39] Block-level synthesis in progress, 31 of 66 jobs complete, 7 jobs running.

[16:13:20] Block-level synthesis in progress, 31 of 66 jobs complete, 7 jobs running.

[16:14:02] Block-level synthesis in progress, 31 of 66 jobs complete, 8 jobs running.

[16:14:34] Block-level synthesis in progress, 31 of 66 jobs complete, 8 jobs running.

[16:15:23] Block-level synthesis in progress, 33 of 66 jobs complete, 6 jobs running.

[16:15:58] Block-level synthesis in progress, 33 of 66 jobs complete, 6 jobs running.

[16:16:52] Block-level synthesis in progress, 34 of 66 jobs complete, 7 jobs running.

[16:17:28] Block-level synthesis in progress, 34 of 66 jobs complete, 7 jobs running.

[16:18:17] Block-level synthesis in progress, 34 of 66 jobs complete, 8 jobs running.

[16:18:56] Block-level synthesis in progress, 36 of 66 jobs complete, 6 jobs running.

[16:19:38] Block-level synthesis in progress, 36 of 66 jobs complete, 6 jobs running.

[16:20:14] Block-level synthesis in progress, 36 of 66 jobs complete, 8 jobs running.

[16:20:54] Block-level synthesis in progress, 36 of 66 jobs complete, 8 jobs running.

[16:21:41] Block-level synthesis in progress, 36 of 66 jobs complete, 8 jobs running.

[16:22:34] Block-level synthesis in progress, 37 of 66 jobs complete, 7 jobs running.

[16:23:23] Block-level synthesis in progress, 37 of 66 jobs complete, 8 jobs running.

[16:24:10] Block-level synthesis in progress, 40 of 66 jobs complete, 5 jobs running.

[16:24:48] Block-level synthesis in progress, 40 of 66 jobs complete, 5 jobs running.

[16:25:32] Block-level synthesis in progress, 41 of 66 jobs complete, 7 jobs running.

[16:26:16] Block-level synthesis in progress, 42 of 66 jobs complete, 7 jobs running.

[16:26:58] Block-level synthesis in progress, 42 of 66 jobs complete, 7 jobs running.

[16:27:43] Block-level synthesis in progress, 43 of 66 jobs complete, 7 jobs running.

[16:28:28] Block-level synthesis in progress, 43 of 66 jobs complete, 8 jobs running.

[16:29:05] Block-level synthesis in progress, 43 of 66 jobs complete, 8 jobs running.

[16:29:51] Block-level synthesis in progress, 43 of 66 jobs complete, 8 jobs running.

[16:30:30] Block-level synthesis in progress, 43 of 66 jobs complete, 8 jobs running.

[16:31:13] Block-level synthesis in progress, 44 of 66 jobs complete, 7 jobs running.

[16:31:51] Block-level synthesis in progress, 46 of 66 jobs complete, 6 jobs running.

[16:32:33] Block-level synthesis in progress, 47 of 66 jobs complete, 5 jobs running.

[16:33:11] Block-level synthesis in progress, 48 of 66 jobs complete, 7 jobs running.

[16:33:54] Block-level synthesis in progress, 50 of 66 jobs complete, 5 jobs running.

[16:34:33] Block-level synthesis in progress, 51 of 66 jobs complete, 5 jobs running.

[16:35:14] Block-level synthesis in progress, 52 of 66 jobs complete, 6 jobs running.

[16:35:52] Block-level synthesis in progress, 53 of 66 jobs complete, 6 jobs running.

[16:36:35] Block-level synthesis in progress, 54 of 66 jobs complete, 6 jobs running.

[16:37:11] Block-level synthesis in progress, 54 of 66 jobs complete, 7 jobs running.

[16:37:56] Block-level synthesis in progress, 54 of 66 jobs complete, 8 jobs running.

[16:38:32] Block-level synthesis in progress, 54 of 66 jobs complete, 8 jobs running.

[16:39:16] Block-level synthesis in progress, 54 of 66 jobs complete, 8 jobs running.

[16:39:54] Block-level synthesis in progress, 54 of 66 jobs complete, 8 jobs running.

[16:40:34] Block-level synthesis in progress, 54 of 66 jobs complete, 8 jobs running.

[16:41:13] Block-level synthesis in progress, 54 of 66 jobs complete, 8 jobs running.

[16:41:53] Block-level synthesis in progress, 55 of 66 jobs complete, 7 jobs running.

[16:42:32] Block-level synthesis in progress, 57 of 66 jobs complete, 5 jobs running.

[16:43:12] Block-level synthesis in progress, 58 of 66 jobs complete, 5 jobs running.

[16:43:51] Block-level synthesis in progress, 59 of 66 jobs complete, 4 jobs running.

[16:44:35] Block-level synthesis in progress, 60 of 66 jobs complete, 3 jobs running.

[16:45:13] Block-level synthesis in progress, 60 of 66 jobs complete, 5 jobs running.

[16:46:01] Block-level synthesis in progress, 62 of 66 jobs complete, 3 jobs running.

[16:46:38] Block-level synthesis in progress, 62 of 66 jobs complete, 3 jobs running.

[16:47:22] Block-level synthesis in progress, 62 of 66 jobs complete, 3 jobs running.

[16:47:59] Block-level synthesis in progress, 62 of 66 jobs complete, 3 jobs running.

[16:48:42] Block-level synthesis in progress, 62 of 66 jobs complete, 3 jobs running.

[16:49:20] Block-level synthesis in progress, 62 of 66 jobs complete, 3 jobs running.

[16:50:00] Block-level synthesis in progress, 62 of 66 jobs complete, 3 jobs running.

[16:50:38] Block-level synthesis in progress, 62 of 66 jobs complete, 3 jobs running.

[16:51:19] Block-level synthesis in progress, 62 of 66 jobs complete, 3 jobs running.

[16:51:57] Block-level synthesis in progress, 63 of 66 jobs complete, 2 jobs running.

[16:52:37] Block-level synthesis in progress, 63 of 66 jobs complete, 2 jobs running.

[16:53:13] Block-level synthesis in progress, 63 of 66 jobs complete, 2 jobs running.

[16:53:56] Block-level synthesis in progress, 63 of 66 jobs complete, 2 jobs running.

[16:54:34] Block-level synthesis in progress, 63 of 66 jobs complete, 2 jobs running.

[16:55:14] Block-level synthesis in progress, 63 of 66 jobs complete, 2 jobs running.

[16:55:52] Block-level synthesis in progress, 63 of 66 jobs complete, 2 jobs running.

[16:56:32] Block-level synthesis in progress, 63 of 66 jobs complete, 2 jobs running.

[16:57:10] Block-level synthesis in progress, 63 of 66 jobs complete, 2 jobs running.

[16:57:50] Block-level synthesis in progress, 63 of 66 jobs complete, 2 jobs running.

[16:58:32] Block-level synthesis in progress, 63 of 66 jobs complete, 2 jobs running.

[16:59:13] Block-level synthesis in progress, 63 of 66 jobs complete, 2 jobs running.

[16:59:51] Block-level synthesis in progress, 63 of 66 jobs complete, 2 jobs running.

[17:00:32] Block-level synthesis in progress, 63 of 66 jobs complete, 2 jobs running.

[17:01:09] Block-level synthesis in progress, 64 of 66 jobs complete, 1 job running.

[17:01:50] Block-level synthesis in progress, 64 of 66 jobs complete, 1 job running.

[17:02:30] Block-level synthesis in progress, 64 of 66 jobs complete, 1 job running.

[17:03:10] Block-level synthesis in progress, 64 of 66 jobs complete, 1 job running.

[17:03:51] Block-level synthesis in progress, 64 of 66 jobs complete, 1 job running.

[17:04:32] Block-level synthesis in progress, 64 of 66 jobs complete, 1 job running.

[17:05:10] Block-level synthesis in progress, 64 of 66 jobs complete, 1 job running.

[17:05:51] Block-level synthesis in progress, 64 of 66 jobs complete, 1 job running.

[17:06:31] Block-level synthesis in progress, 64 of 66 jobs complete, 1 job running.

[17:07:13] Block-level synthesis in progress, 65 of 66 jobs complete, 0 jobs running.

[17:07:53] Block-level synthesis in progress, 65 of 66 jobs complete, 0 jobs running.

[17:08:35] Block-level synthesis in progress, 65 of 66 jobs complete, 1 job running.

[17:09:17] Block-level synthesis in progress, 65 of 66 jobs complete, 1 job running.

[17:10:00] Block-level synthesis in progress, 65 of 66 jobs complete, 1 job running.

[17:10:44] Block-level synthesis in progress, 65 of 66 jobs complete, 1 job running.

[17:11:28] Block-level synthesis in progress, 65 of 66 jobs complete, 1 job running.

[17:12:08] Block-level synthesis in progress, 65 of 66 jobs complete, 1 job running.

[17:12:54] Block-level synthesis in progress, 65 of 66 jobs complete, 1 job running.

[17:13:36] Block-level synthesis in progress, 65 of 66 jobs complete, 1 job running.

[17:14:17] Block-level synthesis in progress, 65 of 66 jobs complete, 1 job running.

[17:14:58] Block-level synthesis in progress, 65 of 66 jobs complete, 1 job running.

[17:15:42] Block-level synthesis in progress, 65 of 66 jobs complete, 1 job running.

[17:16:26] Block-level synthesis in progress, 65 of 66 jobs complete, 1 job running.

[17:17:10] Block-level synthesis in progress, 65 of 66 jobs complete, 1 job running.

[17:17:50] Block-level synthesis in progress, 65 of 66 jobs complete, 1 job running.

[17:18:36] Block-level synthesis in progress, 65 of 66 jobs complete, 1 job running.

[17:19:18] Block-level synthesis in progress, 66 of 66 jobs complete, 0 jobs running.

[17:20:05] Block-level synthesis in progress, 66 of 66 jobs complete, 0 jobs running.

[17:20:46] Top-level synthesis in progress.

[17:21:31] Top-level synthesis in progress.

[17:22:12] Top-level synthesis in progress.

[17:22:57] Top-level synthesis in progress.

[17:23:42] Top-level synthesis in progress.

[17:24:34] Top-level synthesis in progress.

[17:25:18] Top-level synthesis in progress.

[17:26:10] Top-level synthesis in progress.

[17:26:46] Top-level synthesis in progress.

[17:27:44] Top-level synthesis in progress.

[17:28:24] Top-level synthesis in progress.

[17:29:21] Top-level synthesis in progress.

[17:30:00] Top-level synthesis in progress.

[17:30:51] Top-level synthesis in progress.

[17:31:30] Top-level synthesis in progress.

[17:32:38] Run vpl: Step synth: Completed

[17:32:38] Run vpl: Step impl: Started

[18:39:04] Finished 2nd of 6 tasks (FPGA linking synthesized kernels to platform). Elapsed time: 03h 37m 10s

[18:39:04] Starting logic optimization..

[18:46:07] Phase 1 Generate And Synthesize MIG Cores

[19:24:48] Phase 2 Generate And Synthesize Debug Cores

[19:51:43] Phase 3 Retarget

[19:54:43] Phase 4 Constant propagation

[19:56:11] Phase 5 Sweep

[20:01:42] Phase 6 BUFG optimization

[20:03:43] Phase 7 Shift Register Optimization

[20:05:07] Phase 8 Post Processing Netlist

[20:19:39] Finished 3rd of 6 tasks (FPGA logic optimization). Elapsed time: 01h 40m 35s

[20:19:39] Starting logic placement..

[20:25:26] Phase 1 Placer Initialization

[20:25:26] Phase 1.1 Placer Initialization Netlist Sorting

[20:39:10] Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device

[20:49:32] Phase 1.3 Build Placer Netlist Model

[21:02:08] Phase 1.4 Constrain Clocks/Macros

[21:03:55] Phase 2 Global Placement

[21:03:55] Phase 2.1 Floorplanning

[21:07:01] Phase 2.1.1 Partition Driven Placement

[21:07:01] Phase 2.1.1.1 PBP: Partition Driven Placement

[21:10:01] Phase 2.1.1.2 PBP: Clock Region Placement

[21:14:07] Phase 2.1.1.3 PBP: Compute Congestion

[21:15:13] Phase 2.1.1.4 PBP: UpdateTiming

[21:17:29] Phase 2.1.1.5 PBP: Add part constraints

[21:18:22] Phase 2.2 Update Timing before SLR Path Opt

[21:18:22] Phase 2.3 Global Placement Core

[21:48:47] Phase 2.3.1 Physical Synthesis In Placer

[22:11:25] Phase 3 Detail Placement

[22:12:07] Phase 3.1 Commit Multi Column Macros

[22:12:07] Phase 3.2 Commit Most Macros & LUTRAMs

[22:16:49] Phase 3.3 Small Shape DP

[22:16:49] Phase 3.3.1 Small Shape Clustering

[22:19:04] Phase 3.3.2 Flow Legalize Slice Clusters

[22:19:43] Phase 3.3.3 Slice Area Swap

[22:24:12] Phase 3.4 Place Remaining

[22:25:00] Phase 3.5 Re-assign LUT pins

[22:26:25] Phase 3.6 Pipeline Register Optimization

[22:26:25] Phase 3.7 Fast Optimization

[22:30:54] Phase 4 Post Placement Optimization and Clean-Up

[22:30:54] Phase 4.1 Post Commit Optimization

[22:39:48] Phase 4.1.1 Post Placement Optimization

[22:40:31] Phase 4.1.1.1 BUFG Insertion

[22:40:31] Phase 1 Physical Synthesis Initialization

[22:42:47] Phase 4.1.1.2 BUFG Replication

[22:46:49] Phase 4.1.1.3 Replication

[22:53:58] Phase 4.2 Post Placement Cleanup

[22:53:58] Phase 4.3 Placer Reporting

[22:53:58] Phase 4.3.1 Print Estimated Congestion

[22:56:39] Phase 4.4 Final Placement Cleanup

[00:07:04] Finished 4th of 6 tasks (FPGA logic placement). Elapsed time: 03h 47m 24s

[00:07:04] Starting logic routing..

[00:13:14] Phase 1 Build RT Design

[00:23:28] Phase 2 Router Initialization

[00:23:28] Phase 2.1 Fix Topology Constraints

[00:24:16] Phase 2.2 Pre Route Cleanup

[00:24:53] Phase 2.3 Global Clock Net Routing

[00:27:27] Phase 2.4 Update Timing

[00:41:35] Phase 2.5 Update Timing for Bus Skew

[00:41:35] Phase 2.5.1 Update Timing

[00:46:56] Phase 3 Initial Routing

[00:46:56] Phase 3.1 Global Routing

[00:52:57] Phase 4 Rip-up And Reroute

[00:52:57] Phase 4.1 Global Iteration 0

[01:12:46] Phase 4.2 Global Iteration 1

[01:19:00] Phase 4.3 Global Iteration 2

[01:24:20] Phase 5 Delay and Skew Optimization

[01:24:20] Phase 5.1 Delay CleanUp

[01:24:20] Phase 5.1.1 Update Timing

[01:30:18] Phase 5.2 Clock Skew Optimization

[01:30:57] Phase 6 Post Hold Fix

[01:30:57] Phase 6.1 Hold Fix Iter

[01:30:57] Phase 6.1.1 Update Timing

[01:35:34] Phase 7 Route finalize

[01:35:34] Phase 8 Verifying routed nets

[01:36:56] Phase 9 Depositing Routes

[01:40:13] Phase 10 Route finalize

[01:40:59] Phase 11 Post Router Timing

[01:46:58] Finished 5th of 6 tasks (FPGA routing). Elapsed time: 01h 39m 53s

[01:46:58] Starting bitstream generation..

[03:41:49] Creating bitmap...

[04:27:05] Writing bitstream ./pfm\_top\_i\_dynamic\_region\_my\_rm\_partial.bit...

[04:27:05] Finished 6th of 6 tasks (FPGA bitstream generation). Elapsed time: 02h 40m 06s

[04:31:44] Run vpl: Step impl: Completed

[04:31:53] Run vpl: FINISHED. Run Status: impl Complete!

INFO: [v++ 60-1441] [04:32:46] Run run\_link: Step vpl: Completed

Time (s): cpu = 00:51:09 ; elapsed = 13:31:09 . Memory (MB): peak = 1585.129 ; gain = 0.000 ; free physical = 100479 ; free virtual = 253638

INFO: [v++ 60-1443] [04:32:46] Run run\_link: Step rtdgen: Started

INFO: [v++ 60-1453] Command Line: rtdgen

INFO: [v++ 60-1454] Run Directory: /iu\_home/iu7075/workspace/\_x/link/run\_link

INFO: [v++ 60-991] clock name 'clkwiz\_kernel\_clk\_out1' (clock ID '0') is being mapped to clock name 'DATA\_CLK' in the xclbin

INFO: [v++ 60-991] clock name 'clkwiz\_kernel2\_clk\_out1' (clock ID '1') is being mapped to clock name 'KERNEL\_CLK' in the xclbin

INFO: [v++ 60-1230] The compiler selected the following frequencies for the runtime controllable kernel clock(s) and scalable system clock(s): Kernel (DATA) clock: clkwiz\_kernel\_clk\_out1 = 300, Kernel (KERNEL) clock: clkwiz\_kernel2\_clk\_out1 = 500

INFO: [v++ 60-1453] Command Line: cf2sw -a /iu\_home/iu7075/workspace/\_x/link/int/address\_map.xml -sdsl /iu\_home/iu7075/workspace/\_x/link/int/sdsl.dat -xclbin /iu\_home/iu7075/workspace/\_x/link/int/xclbin\_orig.xml -rtd /iu\_home/iu7075/workspace/\_x/link/int/vinc.rtd -o /iu\_home/iu7075/workspace/\_x/link/int/vinc.xml

INFO: [v++ 60-1652] Cf2sw returned exit code: 0

INFO: [v++ 60-2311] HPISystemDiagram::writeSystemDiagramAfterRunningVivado, rtdInputFilePath: /iu\_home/iu7075/workspace/\_x/link/int/vinc.rtd

INFO: [v++ 60-2312] HPISystemDiagram::writeSystemDiagramAfterRunningVivado, systemDiagramOutputFilePath: /iu\_home/iu7075/workspace/\_x/link/int/systemDiagramModelSlrBaseAddress.json

INFO: [v++ 60-1618] Launching

INFO: [v++ 60-1441] [04:33:02] Run run\_link: Step rtdgen: Completed

Time (s): cpu = 00:00:14 ; elapsed = 00:00:15 . Memory (MB): peak = 1585.129 ; gain = 0.000 ; free physical = 100631 ; free virtual = 253790

INFO: [v++ 60-1443] [04:33:02] Run run\_link: Step xclbinutil: Started

INFO: [v++ 60-1453] Command Line: xclbinutil --add-section DEBUG\_IP\_LAYOUT:JSON:/iu\_home/iu7075/workspace/\_x/link/int/debug\_ip\_layout.rtd --add-section BITSTREAM:RAW:/iu\_home/iu7075/workspace/\_x/link/int/partial.bit --force --target hw --key-value SYS:dfx\_enable:true --add-section :JSON:/iu\_home/iu7075/workspace/\_x/link/int/vinc.rtd --append-section :JSON:/iu\_home/iu7075/workspace/\_x/link/int/appendSection.rtd --add-section CLOCK\_FREQ\_TOPOLOGY:JSON:/iu\_home/iu7075/workspace/\_x/link/int/vinc\_xml.rtd --add-section BUILD\_METADATA:JSON:/iu\_home/iu7075/workspace/\_x/link/int/vinc\_build.rtd --add-section EMBEDDED\_METADATA:RAW:/iu\_home/iu7075/workspace/\_x/link/int/vinc.xml --add-section SYSTEM\_METADATA:RAW:/iu\_home/iu7075/workspace/\_x/link/int/systemDiagramModelSlrBaseAddress.json --output /iu\_home/iu7075/workspace/out/vinc.xclbin

INFO: [v++ 60-1454] Run Directory: /iu\_home/iu7075/workspace/\_x/link/run\_link

XRT Build Version: 2.8.743 (2020.2)

Build Date: 2020-11-16 00:19:11

Hash ID: 77d5484b5c4daa691a7f78235053fb036829b1e9

Creating a default 'in-memory' xclbin image.

Section: 'DEBUG\_IP\_LAYOUT'(9) was successfully added.

Size : 440 bytes

Format : JSON

File : '/iu\_home/iu7075/workspace/\_x/link/int/debug\_ip\_layout.rtd'

Section: 'BITSTREAM'(0) was successfully added.

Size : 40693374 bytes

Format : RAW

File : '/iu\_home/iu7075/workspace/\_x/link/int/partial.bit'

Section: 'MEM\_TOPOLOGY'(6) was successfully added.

Format : JSON

File : 'mem\_topology'

Section: 'IP\_LAYOUT'(8) was successfully added.

Format : JSON

File : 'ip\_layout'

Section: 'CONNECTIVITY'(7) was successfully added.

Format : JSON

File : 'connectivity'

Section: 'CLOCK\_FREQ\_TOPOLOGY'(11) was successfully added.

Size : 274 bytes

Format : JSON

File : '/iu\_home/iu7075/workspace/\_x/link/int/vinc\_xml.rtd'

Section: 'BUILD\_METADATA'(14) was successfully added.

Size : 3018 bytes

Format : JSON

File : '/iu\_home/iu7075/workspace/\_x/link/int/vinc\_build.rtd'

Section: 'EMBEDDED\_METADATA'(2) was successfully added.

Size : 2759 bytes

Format : RAW

File : '/iu\_home/iu7075/workspace/\_x/link/int/vinc.xml'

Section: 'SYSTEM\_METADATA'(22) was successfully added.

Size : 5692 bytes

Format : RAW

File : '/iu\_home/iu7075/workspace/\_x/link/int/systemDiagramModelSlrBaseAddress.json'

Section: 'IP\_LAYOUT'(8) was successfully appended to.

Format : JSON

File : 'ip\_layout'

Successfully wrote (40715579 bytes) to the output file: /iu\_home/iu7075/workspace/out/vinc.xclbin

Leaving xclbinutil.

INFO: [v++ 60-1441] [04:33:04] Run run\_link: Step xclbinutil: Completed

Time (s): cpu = 00:00:00.63 ; elapsed = 00:00:02 . Memory (MB): peak = 1585.129 ; gain = 0.000 ; free physical = 100594 ; free virtual = 253831

INFO: [v++ 60-1443] [04:33:04] Run run\_link: Step xclbinutilinfo: Started

INFO: [v++ 60-1453] Command Line: xclbinutil --quiet --force --info /iu\_home/iu7075/workspace/out/vinc.xclbin.info --input /iu\_home/iu7075/workspace/out/vinc.xclbin

INFO: [v++ 60-1454] Run Directory: /iu\_home/iu7075/workspace/\_x/link/run\_link

INFO: [v++ 60-1441] [04:33:08] Run run\_link: Step xclbinutilinfo: Completed

Time (s): cpu = 00:00:03 ; elapsed = 00:00:04 . Memory (MB): peak = 1585.129 ; gain = 0.000 ; free physical = 100551 ; free virtual = 253788

INFO: [v++ 60-1443] [04:33:08] Run run\_link: Step generate\_sc\_driver: Started

INFO: [v++ 60-1453] Command Line:

INFO: [v++ 60-1454] Run Directory: /iu\_home/iu7075/workspace/\_x/link/run\_link

INFO: [v++ 60-1441] [04:33:08] Run run\_link: Step generate\_sc\_driver: Completed

Time (s): cpu = 00:00:00.02 ; elapsed = 00:00:00.06 . Memory (MB): peak = 1585.129 ; gain = 0.000 ; free physical = 100546 ; free virtual = 253782

INFO: [v++ 60-244] Generating system estimate report...

INFO: [v++ 60-1092] Generated system estimate report: /iu\_home/iu7075/workspace/\_x/reports/link/system\_estimate\_vinc.xtxt

INFO: [v++ 60-586] Created /iu\_home/iu7075/workspace/out/vinc.ltx

INFO: [v++ 60-586] Created out/vinc.xclbin

INFO: [v++ 60-1307] Run completed. Additional information can be found in:

Guidance: /iu\_home/iu7075/workspace/\_x/reports/link/v++\_link\_vinc\_guidance.html

Timing Report: /iu\_home/iu7075/workspace/\_x/reports/link/imp/impl\_1\_xilinx\_u200\_xdma\_201830\_2\_bb\_locked\_timing\_summary\_routed.rpt

Vivado Log: /iu\_home/iu7075/workspace/\_x/logs/link/vivado.log

Steps Log File: /iu\_home/iu7075/workspace/\_x/logs/link/link.steps.log

INFO: [v++ 60-2343] Use the vitis\_analyzer tool to visualize and navigate the relevant reports. Run the following command.

vitis\_analyzer /iu\_home/iu7075/workspace/out/vinc.xclbin.link\_summary

INFO: [v++ 60-791] Total elapsed time: 13h 36m 31s

INFO: [v++ 60-1653] Closing dispatch client.

#### \*.xclbin.info

==============================================================================

XRT Build Version: 2.8.743 (2020.2)

Build Date: 2020-11-16 00:19:11

Hash ID: 77d5484b5c4daa691a7f78235053fb036829b1e9

==============================================================================

xclbin Information

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Generated by: v++ (2020.2) on 2020-11-18-05:13:29

Version: 2.8.743

Kernels: rtl\_kernel\_wizard\_2

Signature:

Content: Bitstream

UUID (xclbin): e1a54d44-5776-417e-9ff2-6f7b196a7b16

Sections: DEBUG\_IP\_LAYOUT, BITSTREAM, MEM\_TOPOLOGY, IP\_LAYOUT,

CONNECTIVITY, CLOCK\_FREQ\_TOPOLOGY, BUILD\_METADATA,

EMBEDDED\_METADATA, SYSTEM\_METADATA,

GROUP\_CONNECTIVITY, GROUP\_TOPOLOGY

==============================================================================

Hardware Platform (Shell) Information

-------------------------------------

Vendor: xilinx

Board: u200

Name: xdma

Version: 201830.2

Generated Version: Vivado 2018.3 (SW Build: 2568420)

Created: Tue Jun 25 06:55:20 2019

FPGA Device: xcu200

Board Vendor: xilinx.com

Board Name: xilinx.com:au200:1.0

Board Part: xilinx.com:au200:part0:1.0

Platform VBNV: xilinx\_u200\_xdma\_201830\_2

Static UUID: c102e7af-b2b8-4381-992b-9a00cc3863eb

Feature ROM TimeStamp: 1561465320

Clocks

------

Name: DATA\_CLK

Index: 0

Type: DATA

Frequency: 300 MHz

Name: KERNEL\_CLK

Index: 1

Type: KERNEL

Frequency: 500 MHz

Memory Configuration

--------------------

Name: bank0

Index: 0

Type: MEM\_DDR4

Base Address: 0x4000000000

Address Size: 0x400000000

Bank Used: No

Name: bank1

Index: 1

Type: MEM\_DDR4

Base Address: 0x5000000000

Address Size: 0x400000000

Bank Used: No

Name: bank2

Index: 2

Type: MEM\_DDR4

Base Address: 0x6000000000

Address Size: 0x400000000

Bank Used: Yes

Name: bank3

Index: 3

Type: MEM\_DDR4

Base Address: 0x7000000000

Address Size: 0x400000000

Bank Used: No

Name: PLRAM[0]

Index: 4

Type: MEM\_DRAM

Base Address: 0x3000000000

Address Size: 0x20000

Bank Used: No

Name: PLRAM[1]

Index: 5

Type: MEM\_DRAM

Base Address: 0x3000200000

Address Size: 0x20000

Bank Used: No

Name: PLRAM[2]

Index: 6

Type: MEM\_DRAM

Base Address: 0x3000400000

Address Size: 0x20000

Bank Used: No

==============================================================================

Kernel: rtl\_kernel\_wizard\_2

Definition

----------

Signature: rtl\_kernel\_wizard\_2 (uint scalar00, int\* axi00\_ptr0)

Ports

-----

Port: s\_axi\_control

Mode: slave

Range (bytes): 0x1000

Data Width: 32 bits

Port Type: addressable

Port: m00\_axi

Mode: master

Range (bytes): 0xFFFFFFFFFFFFFFFF

Data Width: 512 bits

Port Type: addressable

--------------------------

Instance: vinc0

Base Address: 0x1800000

Argument: scalar00

Register Offset: 0x010

Port: s\_axi\_control

Memory: <not applicable>

Argument: axi00\_ptr0

Register Offset: 0x018

Port: m00\_axi

Memory: bank2 (MEM\_DDR4)

==============================================================================

Generated By

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Command: v++

Version: 2020.2 - 2020-11-18-05:13:29 (SW BUILD: 0)

Command Line: v++ --config deniska.cfg --connectivity.nk rtl\_kernel\_wizard\_2:1:vinc0 --connectivity.slr vinc0:SLR1 --connectivity.sp vinc0.m00\_axi:DDR[2] --connectivity.sp vinc0.m00\_axi:PLRAM[0] --input\_files ./deniska\_lab\_04\_kernels/vivado\_rtl\_kernel/rtl\_kernel\_wizard\_2\_ex/exports/rtl\_kernel\_wizard\_2.xo --link --optimize 0 --output out/vinc.xclbin --platform xilinx\_u200\_xdma\_201830\_2 --report\_level 0 --target hw --vivado.prop run.impl\_1.STEPS.OPT\_DESIGN.ARGS.DIRECTIVE=Explore --vivado.prop run.impl\_1.STEPS.PLACE\_DESIGN.ARGS.DIRECTIVE=Explore --vivado.prop run.impl\_1.STEPS.PHYS\_OPT\_DESIGN.IS\_ENABLED=true --vivado.prop run.impl\_1.STEPS.PHYS\_OPT\_DESIGN.ARGS.DIRECTIVE=AggressiveExplore --vivado.prop run.impl\_1.STEPS.ROUTE\_DESIGN.ARGS.DIRECTIVE=Explore

Options: --config deniska.cfg

--connectivity.nk rtl\_kernel\_wizard\_2:1:vinc0

--connectivity.slr vinc0:SLR1

--connectivity.sp vinc0.m00\_axi:DDR[2]

--connectivity.sp vinc0.m00\_axi:PLRAM[0]

--input\_files ./deniska\_lab\_04\_kernels/vivado\_rtl\_kernel/rtl\_kernel\_wizard\_2\_ex/exports/rtl\_kernel\_wizard\_2.xo

--link

--optimize 0

--output out/vinc.xclbin

--platform xilinx\_u200\_xdma\_201830\_2

--report\_level 0

--target hw

--vivado.prop run.impl\_1.STEPS.OPT\_DESIGN.ARGS.DIRECTIVE=Explore

--vivado.prop run.impl\_1.STEPS.PLACE\_DESIGN.ARGS.DIRECTIVE=Explore

--vivado.prop run.impl\_1.STEPS.PHYS\_OPT\_DESIGN.IS\_ENABLED=true

--vivado.prop run.impl\_1.STEPS.PHYS\_OPT\_DESIGN.ARGS.DIRECTIVE=AggressiveExplore

--vivado.prop run.impl\_1.STEPS.ROUTE\_DESIGN.ARGS.DIRECTIVE=Explore

==============================================================================

User Added Key Value Pairs

--------------------------

<empty>

==============================================================================

#### host\_example.cpp

// This is a generated file. Use and modify at your own risk.

////////////////////////////////////////////////////////////////////////////////

/\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Vendor: Xilinx

Associated Filename: main.c

#Purpose: This example shows a basic vector add +1 (constant) by manipulating

# memory inplace.

\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*/

#include <fcntl.h>

#include <stdio.h>

#include <iostream>

#include <stdlib.h>

#include <string.h>

#include <math.h>

#ifdef \_WINDOWS

#include <io.h>

#else

#include <unistd.h>

#include <sys/time.h>

#endif

#include <assert.h>

#include <stdbool.h>

#include <sys/types.h>

#include <sys/stat.h>

#include <CL/opencl.h>

#include <CL/cl\_ext.h>

#include "xclhal2.h"

////////////////////////////////////////////////////////////////////////////////

#define NUM\_WORKGROUPS (1)

#define WORKGROUP\_SIZE (256)

#define MAX\_LENGTH 8192

#define MEM\_ALIGNMENT 4096

#if defined(VITIS\_PLATFORM) && !defined(TARGET\_DEVICE)

#define STR\_VALUE(arg) #arg

#define GET\_STRING(name) STR\_VALUE(name)

#define TARGET\_DEVICE GET\_STRING(VITIS\_PLATFORM)

#endif

////////////////////////////////////////////////////////////////////////////////

cl\_uint load\_file\_to\_memory(const char \*filename, char \*\*result)

{

cl\_uint size = 0;

FILE \*f = fopen(filename, "rb");

if (f == NULL) {

\*result = NULL;

return -1; // -1 means file opening fail

}

fseek(f, 0, SEEK\_END);

size = ftell(f);

fseek(f, 0, SEEK\_SET);

\*result = (char \*)malloc(size+1);

if (size != fread(\*result, sizeof(char), size, f)) {

free(\*result);

return -2; // -2 means file reading fail

}

fclose(f);

(\*result)[size] = 0;

return size;

}

int main(int argc, char\*\* argv)

{

cl\_int err; // error code returned from api calls

cl\_uint check\_status = 0;

const cl\_uint number\_of\_words = 4096; // 16KB of data

cl\_platform\_id platform\_id; // platform id

cl\_device\_id device\_id; // compute device id

cl\_context context; // compute context

cl\_command\_queue commands; // compute command queue

cl\_program program; // compute programs

cl\_kernel kernel; // compute kernel

cl\_uint\* h\_data; // host memory for input vector

char cl\_platform\_vendor[1001];

char target\_device\_name[1001] = TARGET\_DEVICE;

cl\_uint\* h\_axi00\_ptr0\_output = (cl\_uint\*)aligned\_alloc(MEM\_ALIGNMENT,MAX\_LENGTH \* sizeof(cl\_uint\*)); // host memory for output vector

cl\_mem d\_axi00\_ptr0; // device memory used for a vector

// if (argc != 2) {

// printf("Usage: %s xclbin\n", argv[0]);

// return EXIT\_FAILURE;

// }

// Fill our data sets with pattern

h\_data = (cl\_uint\*)aligned\_alloc(MEM\_ALIGNMENT,MAX\_LENGTH \* sizeof(cl\_uint\*));

for(cl\_uint i = 0; i < MAX\_LENGTH; i++) {

h\_data[i] = i;

h\_axi00\_ptr0\_output[i] = 0;

}

// Get all platforms and then select Xilinx platform

cl\_platform\_id platforms[16]; // platform id

cl\_uint platform\_count;

cl\_uint platform\_found = 0;

err = clGetPlatformIDs(16, platforms, &platform\_count);

if (err != CL\_SUCCESS) {

printf("ERROR: Failed to find an OpenCL platform!\n");

printf("ERROR: Test failed\n");

return EXIT\_FAILURE;

}

printf("INFO: Found %d platforms\n", platform\_count);

// Find Xilinx Plaftorm

for (cl\_uint iplat=0; iplat<platform\_count; iplat++) {

err = clGetPlatformInfo(platforms[iplat], CL\_PLATFORM\_VENDOR, 1000, (void \*)cl\_platform\_vendor,NULL);

if (err != CL\_SUCCESS) {

printf("ERROR: clGetPlatformInfo(CL\_PLATFORM\_VENDOR) failed!\n");

printf("ERROR: Test failed\n");

return EXIT\_FAILURE;

}

if (strcmp(cl\_platform\_vendor, "Xilinx") == 0) {

printf("INFO: Selected platform %d from %s\n", iplat, cl\_platform\_vendor);

platform\_id = platforms[iplat];

platform\_found = 1;

}

}

if (!platform\_found) {

printf("ERROR: Platform Xilinx not found. Exit.\n");

return EXIT\_FAILURE;

}

// Get Accelerator compute device

cl\_uint num\_devices;

cl\_uint device\_found = 0;

cl\_device\_id devices[16]; // compute device id

char cl\_device\_name[1001];

err = clGetDeviceIDs(platform\_id, CL\_DEVICE\_TYPE\_ACCELERATOR, 16, devices, &num\_devices);

printf("INFO: Found %d devices\n", num\_devices);

if (err != CL\_SUCCESS) {

printf("ERROR: Failed to create a device group!\n");

printf("ERROR: Test failed\n");

return -1;

}

//iterate all devices to select the target device.

for (cl\_uint i=0; i<num\_devices; i++) {

err = clGetDeviceInfo(devices[i], CL\_DEVICE\_NAME, 1024, cl\_device\_name, 0);

if (err != CL\_SUCCESS) {

printf("ERROR: Failed to get device name for device %d!\n", i);

printf("ERROR: Test failed\n");

return EXIT\_FAILURE;

}

printf("CL\_DEVICE\_NAME %s\n", cl\_device\_name);

if(strcmp(cl\_device\_name, target\_device\_name) == 0) {

device\_id = devices[i];

device\_found = 1;

printf("Selected %s as the target device\n", cl\_device\_name);

}

}

if (!device\_found) {

printf("ERROR:Target device %s not found. Exit.\n", target\_device\_name);

return EXIT\_FAILURE;

}

// Create a compute context

//

context = clCreateContext(0, 1, &device\_id, NULL, NULL, &err);

if (!context) {

printf("ERROR: Failed to create a compute context!\n");

printf("ERROR: Test failed\n");

return EXIT\_FAILURE;

}

// Create a command commands

commands = clCreateCommandQueue(context, device\_id, CL\_QUEUE\_PROFILING\_ENABLE | CL\_QUEUE\_OUT\_OF\_ORDER\_EXEC\_MODE\_ENABLE, &err);

if (!commands) {

printf("ERROR: Failed to create a command commands!\n");

printf("ERROR: code %i\n",err);

printf("ERROR: Test failed\n");

return EXIT\_FAILURE;

}

cl\_int status;

// Create Program Objects

// Load binary from disk

unsigned char \*kernelbinary;

// char \*xclbin = argv[1];

char \*xclbin = "/iu\_home/iu7075/workspace/out/vinc.xclbin";

//------------------------------------------------------------------------------

// xclbin

//------------------------------------------------------------------------------

printf("INFO: loading xclbin %s\n", xclbin);

cl\_uint n\_i0 = load\_file\_to\_memory(xclbin, (char \*\*) &kernelbinary);

if (n\_i0 < 0) {

printf("ERROR: failed to load kernel from xclbin: %s\n", xclbin);

printf("ERROR: Test failed\n");

return EXIT\_FAILURE;

}

size\_t n0 = n\_i0;

// Create the compute program from offline

program = clCreateProgramWithBinary(context, 1, &device\_id, &n0,

(const unsigned char \*\*) &kernelbinary, &status, &err);

free(kernelbinary);

if ((!program) || (err!=CL\_SUCCESS)) {

printf("ERROR: Failed to create compute program from binary %d!\n", err);

printf("ERROR: Test failed\n");

return EXIT\_FAILURE;

}

// Build the program executable

//

err = clBuildProgram(program, 0, NULL, NULL, NULL, NULL);

if (err != CL\_SUCCESS) {

size\_t len;

char buffer[2048];

printf("ERROR: Failed to build program executable!\n");

clGetProgramBuildInfo(program, device\_id, CL\_PROGRAM\_BUILD\_LOG, sizeof(buffer), buffer, &len);

printf("%s\n", buffer);

printf("ERROR: Test failed\n");

return EXIT\_FAILURE;

}

// Create the compute kernel in the program we wish to run

//

kernel = clCreateKernel(program, "rtl\_kernel\_wizard\_2", &err);

if (!kernel || err != CL\_SUCCESS) {

printf("ERROR: Failed to create compute kernel!\n");

printf("ERROR: Test failed\n");

return EXIT\_FAILURE;

}

// Create structs to define memory bank mapping

cl\_mem\_ext\_ptr\_t mem\_ext;

mem\_ext.obj = NULL;

mem\_ext.param = kernel;

mem\_ext.flags = 1;

d\_axi00\_ptr0 = clCreateBuffer(context, CL\_MEM\_READ\_WRITE | CL\_MEM\_EXT\_PTR\_XILINX, sizeof(cl\_uint) \* number\_of\_words, &mem\_ext, &err);

if (err != CL\_SUCCESS) {

std::cout << "Return code for clCreateBuffer flags=" << mem\_ext.flags << ": " << err << std::endl;

}

if (!(d\_axi00\_ptr0)) {

printf("ERROR: Failed to allocate device memory!\n");

printf("ERROR: Test failed\n");

return EXIT\_FAILURE;

}

err = clEnqueueWriteBuffer(commands, d\_axi00\_ptr0, CL\_TRUE, 0, sizeof(cl\_uint) \* number\_of\_words, h\_data, 0, NULL, NULL);

if (err != CL\_SUCCESS) {

printf("ERROR: Failed to write to source array h\_data: d\_axi00\_ptr0: %d!\n", err);

printf("ERROR: Test failed\n");

return EXIT\_FAILURE;

}

// Set the arguments to our compute kernel

// cl\_uint vector\_length = MAX\_LENGTH;

err = 0;

cl\_uint d\_scalar00 = 0;

err |= clSetKernelArg(kernel, 0, sizeof(cl\_uint), &d\_scalar00); // Not used in example RTL logic.

err |= clSetKernelArg(kernel, 1, sizeof(cl\_mem), &d\_axi00\_ptr0);

if (err != CL\_SUCCESS) {

printf("ERROR: Failed to set kernel arguments! %d\n", err);

printf("ERROR: Test failed\n");

return EXIT\_FAILURE;

}

size\_t global[1];

size\_t local[1];

// Execute the kernel over the entire range of our 1d input data set

// using the maximum number of work group items for this device

global[0] = 1;

local[0] = 1;

err = clEnqueueNDRangeKernel(commands, kernel, 1, NULL, (size\_t\*)&global, (size\_t\*)&local, 0, NULL, NULL);

if (err) {

printf("ERROR: Failed to execute kernel! %d\n", err);

printf("ERROR: Test failed\n");

return EXIT\_FAILURE;

}

clFinish(commands);

// Read back the results from the device to verify the output

//

cl\_event readevent;

err = 0;

err |= clEnqueueReadBuffer( commands, d\_axi00\_ptr0, CL\_TRUE, 0, sizeof(cl\_uint) \* number\_of\_words, h\_axi00\_ptr0\_output, 0, NULL, &readevent );

if (err != CL\_SUCCESS) {

printf("ERROR: Failed to read output array! %d\n", err);

printf("ERROR: Test failed\n");

return EXIT\_FAILURE;

}

clWaitForEvents(1, &readevent);

// Check Results

for (cl\_uint i = 0; i < number\_of\_words; i++) {

if (((h\_data[i] + 128)/8) != h\_axi00\_ptr0\_output[i]) {

printf("ERROR in rtl\_kernel\_wizard\_2::m00\_axi - array index %d (host addr 0x%03x) - input=%d (0x%x), output=%d (0x%x)\n", i, i\*4, h\_data[i], h\_data[i], h\_axi00\_ptr0\_output[i], h\_axi00\_ptr0\_output[i]);

check\_status = 1;

}

// printf("i=%d, input=%d, output=%d\n", i, h\_axi00\_ptr0\_input[i], h\_axi00\_ptr0\_output[i]);

}

//--------------------------------------------------------------------------

// Shutdown and cleanup

//--------------------------------------------------------------------------

clReleaseMemObject(d\_axi00\_ptr0);

free(h\_axi00\_ptr0\_output);

free(h\_data);

clReleaseProgram(program);

clReleaseKernel(kernel);

clReleaseCommandQueue(commands);

clReleaseContext(context);

if (check\_status) {

printf("ERROR: Test failed\n");

return EXIT\_FAILURE;

} else {

printf("INFO: Test completed successfully.\n");

return EXIT\_SUCCESS;

}

} // end of main

### Результаты запуска

