Laboratory Assignment #2

Due: 15/11/2021, 11:30 am

2-bit Comparator circuit implementation on FPGA

Requirements:

You are required to design 2-bit comparator circuit in Vivado using Verilog.

Inputs: X_1X_0, Y_1Y_0

Outputs: LT, EQ, GT

LT becomes 1 when X_1X_0 is less than Y_1Y_0. Otherwise, it is 0.

EQ becomes 1 when X_1X_0 equal to Y_1Y_0. Otherwise, it is 0.

GT becomes 1 when X_1X_0 is greater than Y_1Y_0. Otherwise, it is 0.

You need to use K-map optimizations to derive Boolean expressions for the outputs. You need to run a simulation and show that your design is working as expected in all possible input combinations. Then, you should zip your project directory with a lab report that contains K-map optimizations. Submit the zip file until 15 November 2021, 11:30 am.

We are going to have in-lab sessions in the week of 15 November. In order to get full credit, you must attend your lab session in FENS 1033. You need to implement your design on the FPGA and finish the assignment.