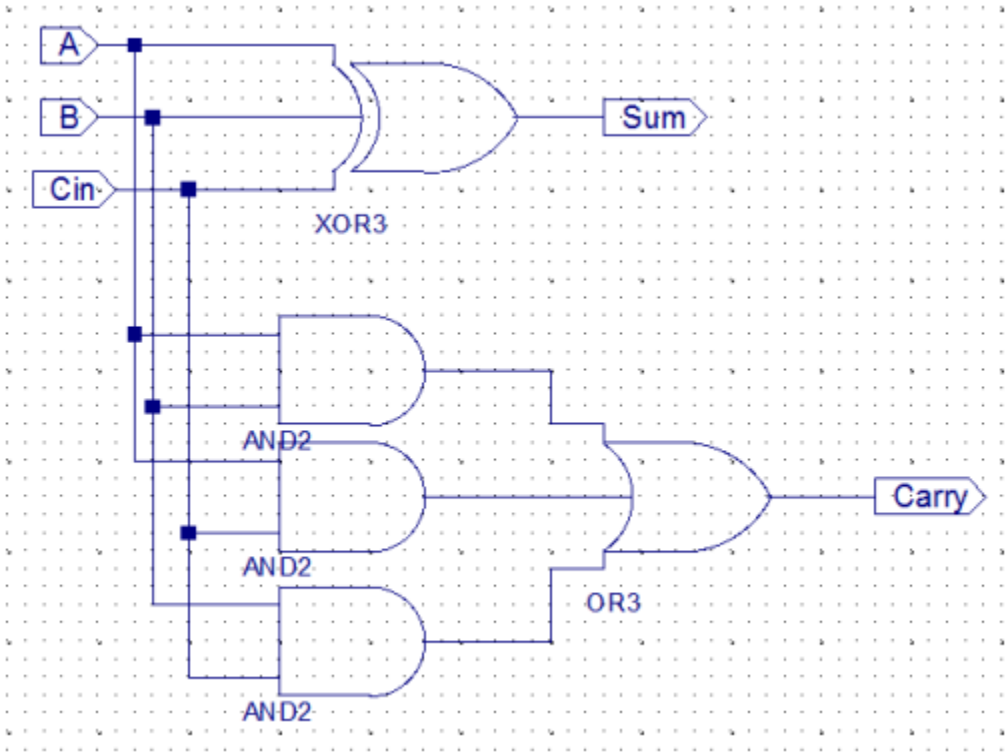
Laboratory Assignment #1

Due: 25/10/2021, 11:30

Full Adder implementation on FPGA

Requirements:

You are required to design the following circuit in Vivado using Verilog.



You can follow the tutorial (Xilinx Vivado 2018.2 Design Tool Guide (Simulation)) on SUCourse to implement this circuit. You need to run a simulation and show that your design is working as expected in all possible input combinations. Then, you should zip your project directory (if your project path is D:\Xilinx\lab1, then zip directory lab1) and submit the zip file until 25 October 2021, 11:30.

We are going to have in-lab sessions in the week of 25 October. In order to get full credit, you must attend your lab session in FENS 1033. TAs will show you how to program FPGA. You need to implement your design on the FPGA and finish the assignment.

Hints:

1. You can check the truth table of the full adder to use it on the simulation stage.
2. You may use more than 2 operands in an assignment.(e.g, S = A ^ B ^ C)
3. In Verilog, XOR => ^ OR => | AND => &