Laboratory Assignment #1

Due: End of the lab section.

Follow the design steps below during the lab session:

1) Obtain the truth table and derive the corresponding K-map (*made as quiz*)
2) Obtain optimized Boolean expression from the K-map (*made as quiz*)
3) Draw the corresponding gate level circuit using any logical gates you want.
4) Enter your design using schematic editor in Xilinx ISE Design tool.
5) Simulate all possible input combinations in Xilinx ISE Design tool and make sure your design functions correctly in simulation. Check the correctness of your circuit using truth table.
6) For better visualization, group your inputs/outputs via "New Virtual Bus" option. Then, rename and change the radix of your virtual bus accordingly.
7) **Demonstrate your work to TA.**
8) Zip your project file and submit it to the SUCourse+.

Note that you must zip and submit your project directory (not just schematic file or testbench) to Lab#1 assignment. You must submit it until the end of your lab section (e.g. if your lab section is between 17:40-19:30, your deadline for submission is 19:30.).