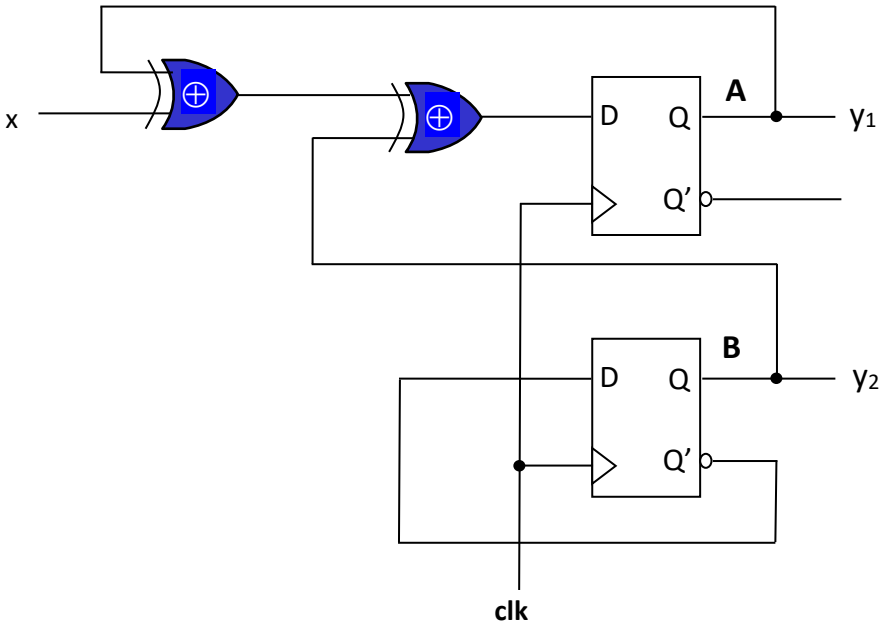
1) Answer the following questions for the circuit given below.



a. Obtain the next state and output equations, and the state table.

Present State		Input	Next State		Output	
A	B	x	A(t+1)	B(t+1)	y_1	y_2
0	0	0	0	1	0	0
0	0	1	1	1	0	0
0	1	0	1	0	0	1
0	1	1	0	0	0	1
1	0	0	1	1	1	0
1	0	1	0	1	1	0
1	1	0	0	0	1	1
1	1	1	1	0	1	1

x \ AB	00	01	11	10
0	0	1	0	1
1	1	0	1	0

$A(t+1) = x \oplus A \oplus B$

x \ AB	00	01	11	10
0	1	0	0	1
1	1	0	0	1

$B(t+1) = B'$

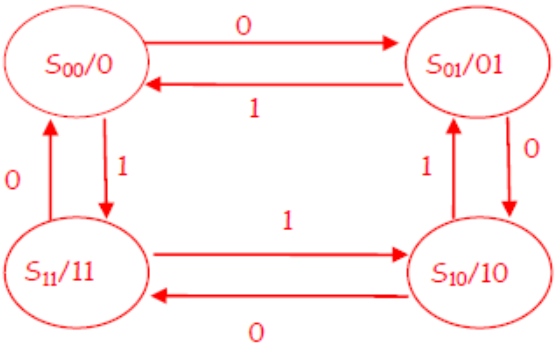
x \ AB	00	01	11	10
0	0	0	1	1
1	0	0	1	1

$y_1 = A$

x \ AB	00	01	11	10
0	0	1	1	0
1	0	1	1	0

$y_2 = B$

b. Draw the state diagram.



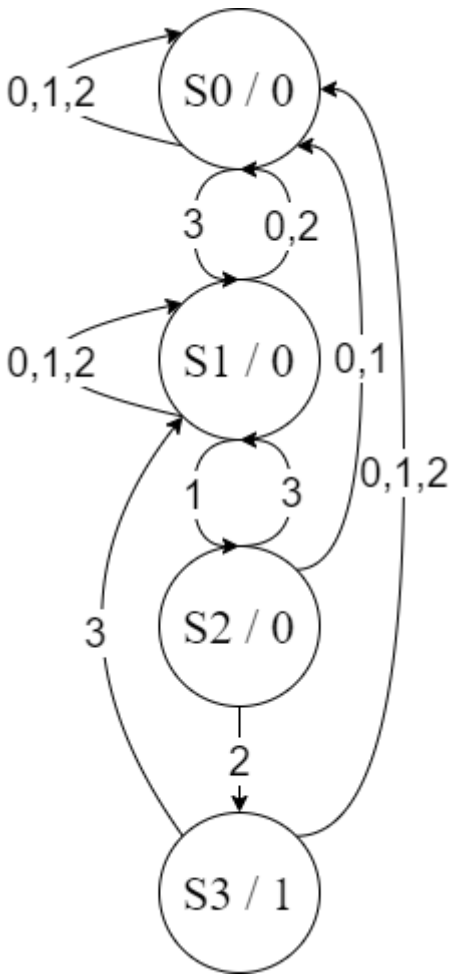
c. What does this circuit do?

Counts up when input is 0 and counts down when input is 1.

2) A sequential circuit has two inputs (A1,A0) and one output (B). The output B=1 every time the input pattern "312" (11/01/10) is observed. Otherwise B is 0.

a. Assuming the circuit is implemented as a Moore machine, draw the corresponding state diagram. (Also, implement using Mealy machine for exercise)

State encoding: S0: (00), S1: (01), S2: (10), S3: (11)



b. Obtain the stage diagram (use binary encoding to represent states)

Current State		Input		Next State		Output
S1	S0	A1	A0	S1(t+1)	S0(t+1)	B
0	0	0	0	0	0	0
0	0	0	1	0	0	0
0	0	1	0	0	0	0
0	0	1	1	0	1	0
0	1	0	0	0	0	0
0	1	0	1	1	0	0
0	1	1	0	0	0	0
0	1	1	1	0	1	0
1	0	0	0	0	0	0
1	0	0	1	0	0	0
1	0	1	0	1	1	0
1	0	1	1	0	1	0
1	1	0	0	0	0	1
1	1	0	1	0	0	1
1	1	1	0	0	0	1
1	1	1	1	0	1	1

c. Derive flip-flop and output equations (using D flip-flops).

S_1S_0 \ A_1A_0	00	01	11	10
00	0	0	0	0
01	0	1	0	0
11	0	0	0	0
10	0	0	0	1

$S_1(t+1) = S_1'S_0A_1'A_0 + S_1S_0'A_1A_0'$

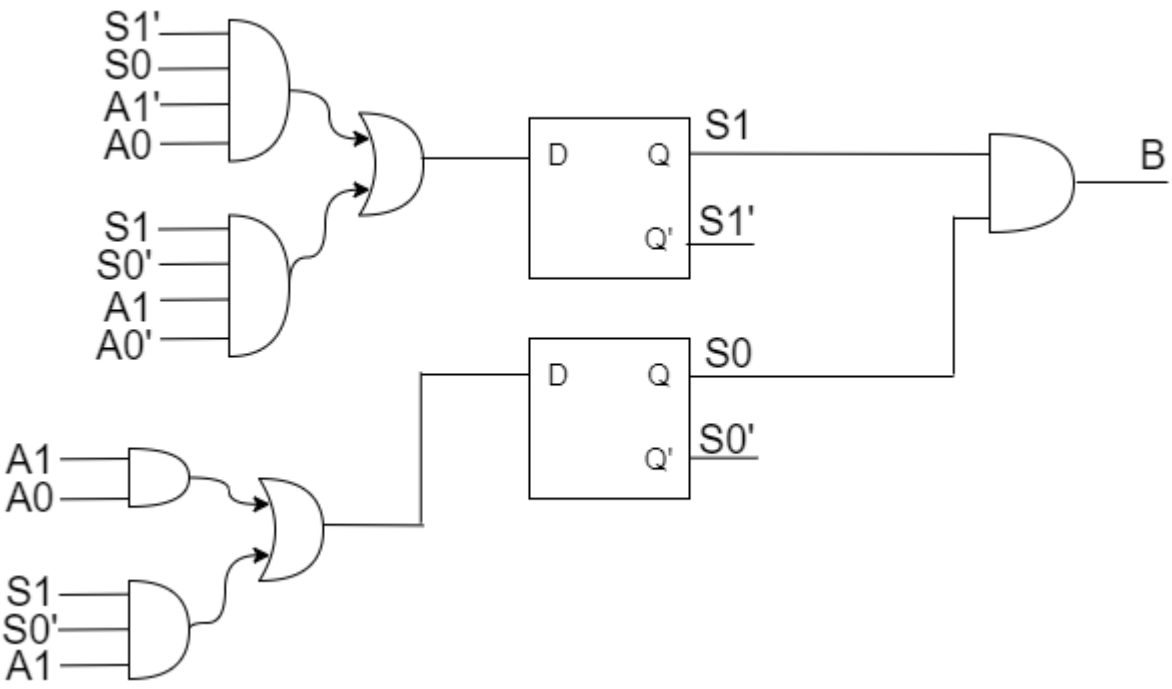
S_1S_0 \ A_1A_0	00	01	11	10
00	0	0	1	0
01	0	0	1	0
11	0	0	1	0
10	0	0	1	1

$S_0(t+1) = A_1A_0 + S_1S_0'A_1$

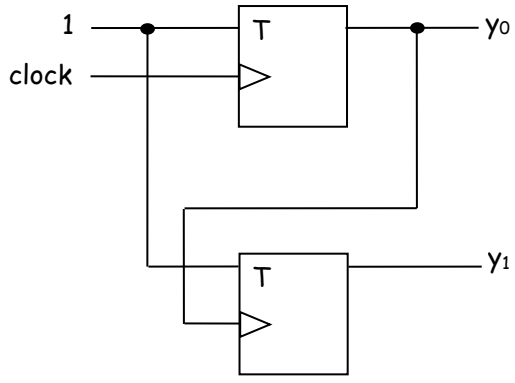
S_1S_0 \ A_1A_0	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	1	1	1	1
10	0	0	0	0

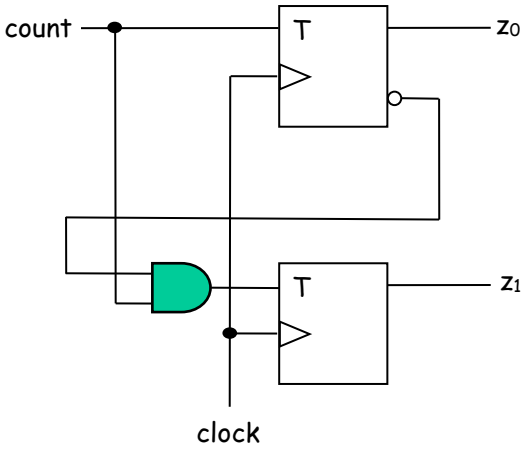
$B = S_1.S_0$

d. Draw the corresponding circuit.

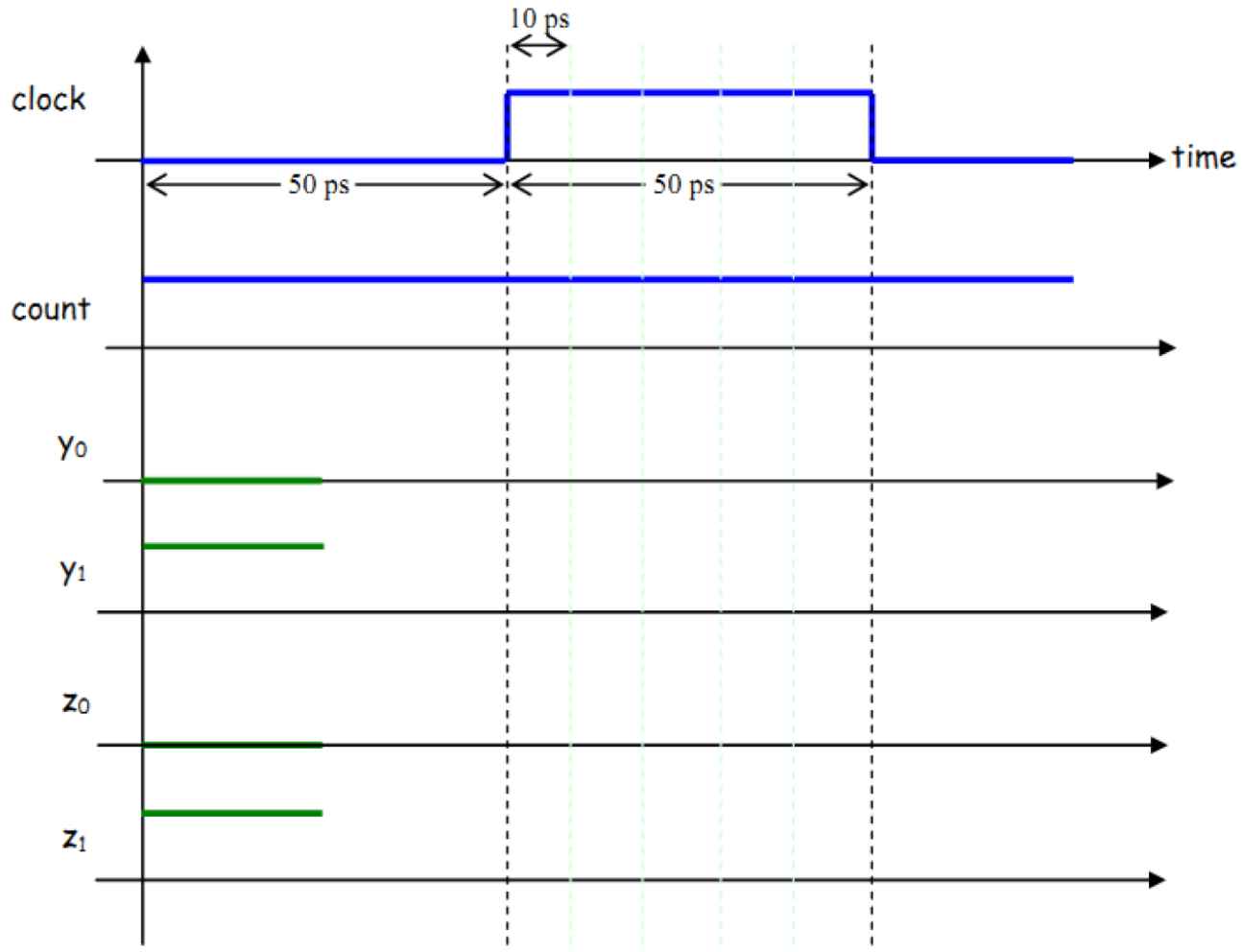


3) Consider the following two sequential circuits:

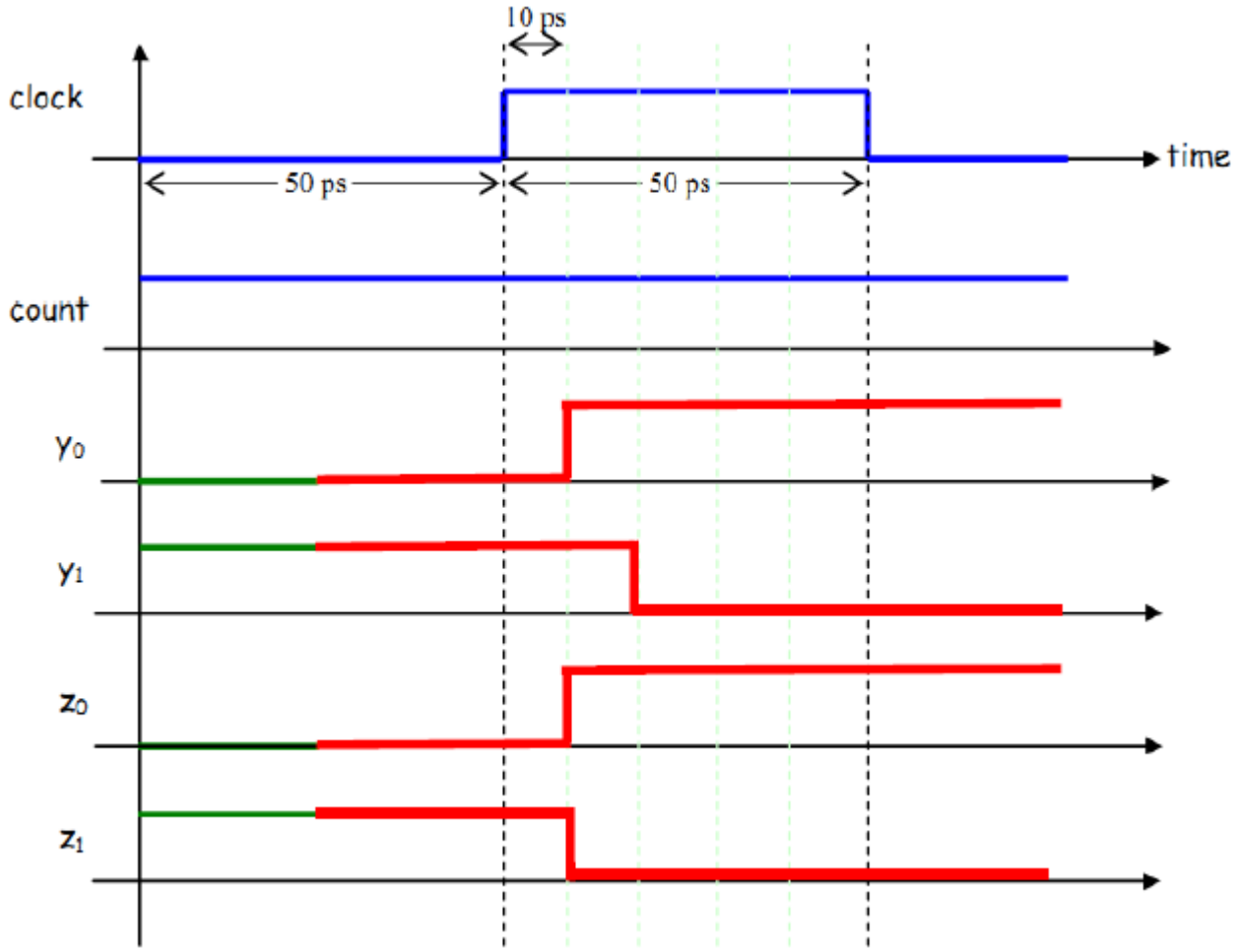




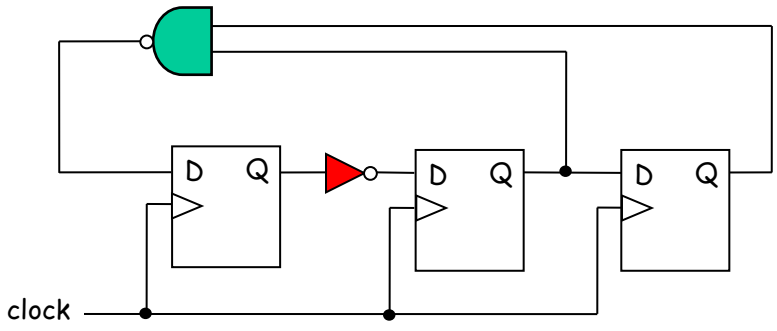
The propagation delay of T flip-flop is $t_{P,FF}$ = 10 ps. The propagation delay of AND gate is $t_{P,AND}$ = 10 ps. Two circuits are using the same clock. Fill the following timing diagram.



Answer:



4) Determine the minimum clock period and maximum clock frequency for the circuit given below. The propagation delay of D flip-flop is $t_{P,FF}$ = 3 ns. The setup time of D flip-flop is t_s = 1 ns. The propagation delay of NAND gate is $t_{P,NAND}$ = 3 ns. The propagation delay of NOT gate is $t_{P,NOT}$ = 1 ns.

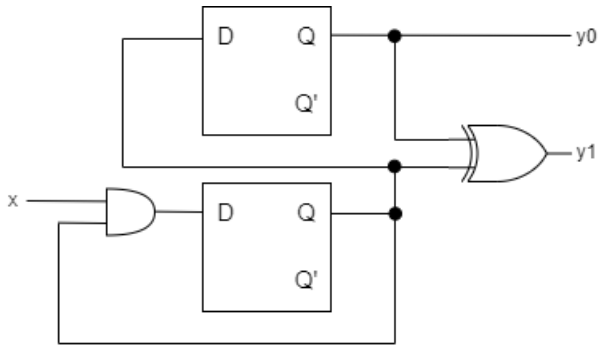


$T_{min} = t_{P,NAND} + t_{P,FF} + t_S$

$T_{min} = 3 + 3 + 1 = 7$ ns

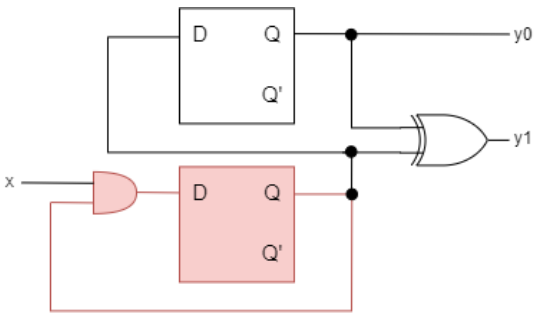
$F_{max} = (1/ T_{min}) = \frac{1}{7}$ ns $= \frac{1}{7}$ GHz = 142.85... MHz

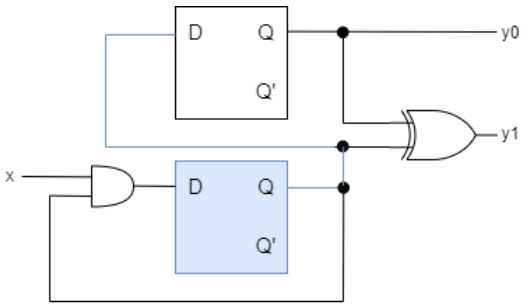
5) Consider the following sequential circuit and the timing values $t_{P,FF} = t_{P,XOR} = 200.0$ps, $t_{P,AND} = t_s = 100.0$ ps and $t_h = 150.0$ ps.



a. Find the maximum clock frequency that can be applied to the circuit.

There are two path we need to evaluate (red and blue given below).





Time for red path → $t_{P,FF} + t_{P,AND} + t_s = 200$ ps + 100 ps + 100 ps = 400 ps
Time for blue path → $t_{P,FF} + t_s = 200$ ps + 100 ps = 300 ps

For determining clock frequency, we need to take longest path which is red.

Then, maximum clock frequency is 1/T = 1/(400 ps) = 2.5 GHz

b. Is hold time violated in the circuit? Why or why not? Express the hold time violation condition.

Hold time should meet the condition: $t_{P;FF} + t_{P;COMB}$ (for shortest path) > t_h

In the circuit above, we need to satisfy $t_{P,FF} > t_h$ (200 ps > 150 ps) which si satisfied. So, there is NO hold time violation.

Hold time violation condition is $t_{P,FF} < t_h$

5) Design a counter with D flip-flops that goes through the following repeated sequence: 0, 1, 2, 4, 5, 6, 0, 1, 2, ... Treat unused states 011 and 111 as don't care conditions, i.e. we don't care what their next states are. Draw its logic diagram.

Present State			Next State			FFs (same as next state)		
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0	D_2	D_1	D_0
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	0
0	1	0	1	0	0	1	0	0
0	1	1	X	X	X	X	X	X
1	0	0	1	0	1	1	0	1
1	0	1	1	1	0	1	1	0
1	1	0	0	0	0	0	0	0
1	1	1	X	X	X	X	X	X

Q_2 \ Q_1Q_0	00	01	11	10
0	0	0	X	1
1	1	1	X	0

$D_2 = Q_1 \oplus Q_2$

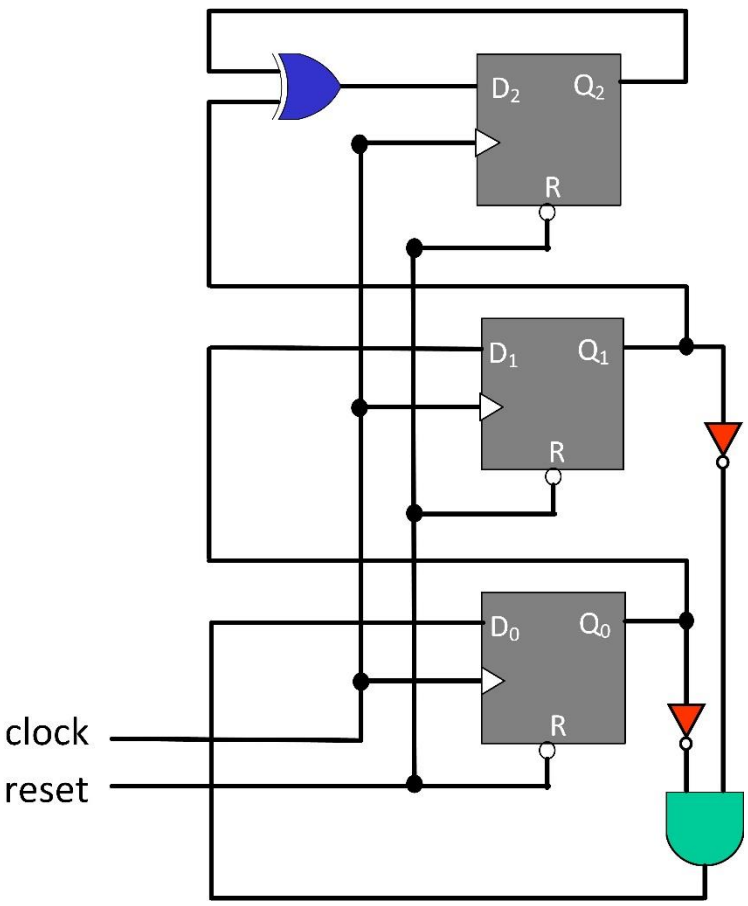
Q_2 \ Q_1Q_0	00	01	11	10
0	0	1	X	0
1	0	1	X	0

$D_1 = Q_0$

Q_2 \ Q_1Q_0	00	01	11	10
0	1	0	X	0
1	1	0	X	0

$D_0 = Q_0'.Q_1'$

Circuit: Counter outputs are (Q_2, Q_1, Q_0)



6) Draw logic diagram of the circuit that would result from synthesizing the following Verilog module.

```
module sample_question (A, B, clk, result);
  input [2:0] A, B;
  input clk;
  output [2:0] result;
  reg [2:0] result;

  always @ (posedge clk)
    if (A == B) result <= A;
    else result <= B;
endmodule
```

(A==B) can be represented as ((A[0] ⊕ B[0]) + (A[1] ⊕ B[1]) + (A[2] ⊕ B[2]))’

Circuit: