Homework Assignment #3

Assigned: 02/12/2020
**Due:** 17/12/2020, 23:59
Late Due: 18/12/2020, 23:59

NOTE: Convert and merge your solutions into one PDF file. Then, submit this file.

1) F(x, y, z, t) = $\prod$ (0, 1, 4, 6, 8, 9, 10, 12, 14, 15) **(20pts)**

   a. Implement the circuit using a decoder and an or gate.

   b. Implement the circuit using one 1-to-8 multiplexer (do not use any other logical elements).

2) Consider the following circuit with three inputs (A, B, C) and one output (F) **(20 pts)**.

   a. Derive the Boolean expression of the signals F1, F2, F3 and the output function F.
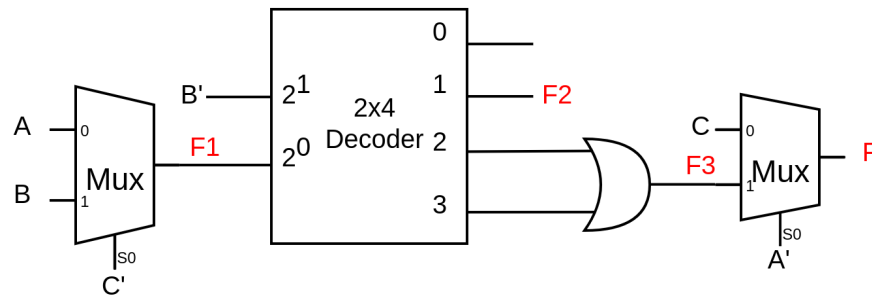
   b. Complete the following Verilog code part so that it implements the output F.

F;

always @ (   )
begin

end

3) Consider the sequential circuit with the following next state and output equations **(20 pts)**:

A(t+1) = x'+B
B(t+1) = b(x⊕A)
y = x + A

      a. Fill the state transition table below.

Present State		Input	Next State		Output
A	B	x	A(t+1)	B(t+1)	y

      b. Draw the state diagram of the state table.

4) Design a state machine for a 16-bit counter circuit.
- If the "up" button is pressed, the circuit will count up by 1.
- If the "down" button is pressed, the circuit will count down by 1.
- If both buttons are pressed at the same time, the circuit will count up by 10.
- If "reset" button is pressed, the counter will become 0.
- Maximum value for this counter is 60000. After 60000, counter will circle back to 0.

Draw the state diagram of this circuit. Draw a high-level design of this circuit **(20 pts)**.

5) Design a 4-bit signed/unsigned adder/subtractor circuit. Circuit will have a signed_unsigned input pin to determine the signed/unsigned operation and a adder_subtractor bin to determine adder/subtractor operation. Draw the circuit diagram **(20 pts)**.