WEEK 1 TASK 1

* For the counter task, I changed the code a little bit and observed the changes in the RISC-V machine code.

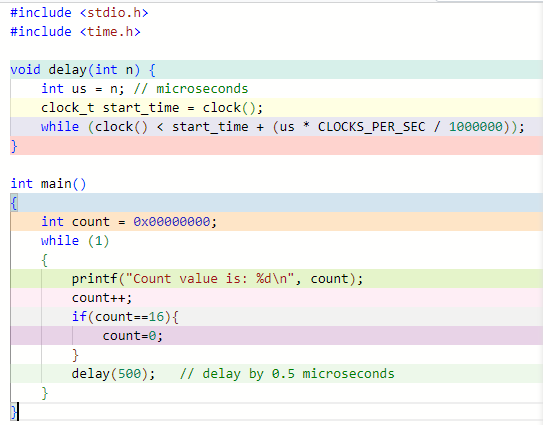
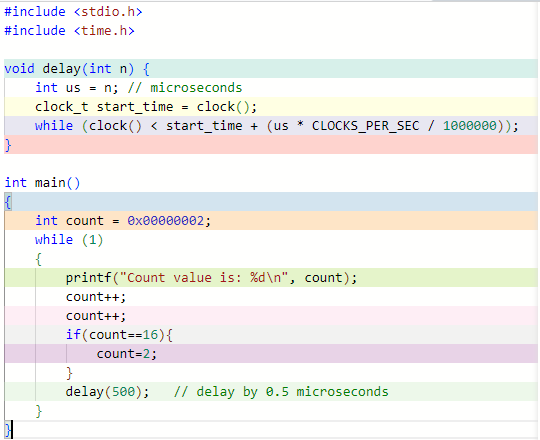
 

Figure : counter C codes

In the Figure, the code on the left hand side counts one by one and starts at zero, while the code on the right hand side, counter is incremented by twice at each step and starts from 2.

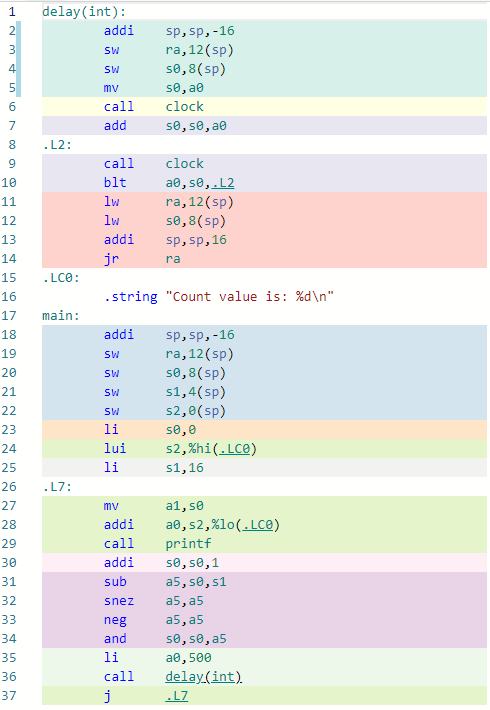
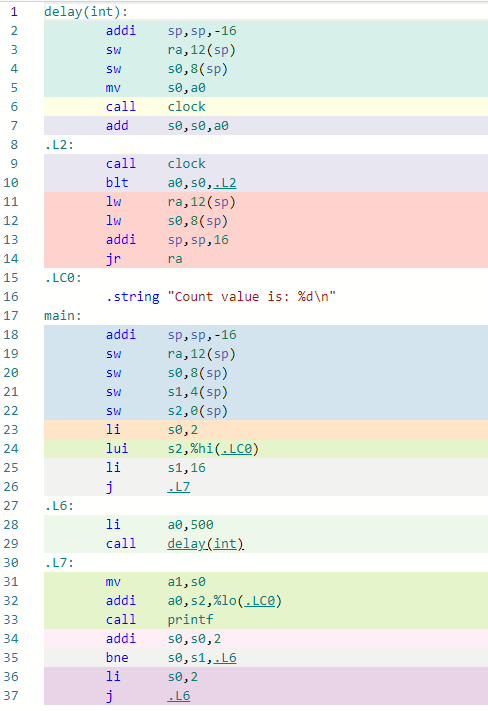
 

Figure : RISC-V GCC Figure 3: RISC-V GCC

We can observe that initial value of the count variable is loaded on the 23rd line in figure 2 and figure 3. ‘li’ instruction loads initial value to s2 register.

Increment of the count variable is done by ‘addi’ instruction. It can be seen that while in figure 2 on 30th line, it is incremented by one, and in figure 3 on 34th line it is incremented by two.

When I changed the loaded value in the if statement, ‘bne’ instruction is used and can be seen in figure 3 on 35th line. It compares register s0 with s1.

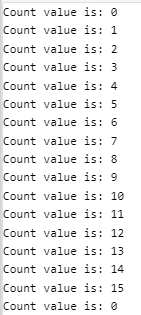
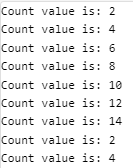
 

Figure 4: Executor Result

[Godbolt link to increment 1 counter](https://godbolt.org/z/71aKGzcxT)

[Godbolt link to increment by 2 counter](https://godbolt.org/z/zaKKP4977)