YAMAHA L S i

YMZ284

Software-controlled Sound Generator  
(SSGL)

* OVERVIEW

The YMZ284(SSGL) is a melody and effect sound generator LSI, having square wave, noise and envelope genera­tors.

The YMZ284 is packaged in 16-pin DIP with easy control, eliminating the I/O port and improving CPU interface from the YM2149(SSG).

* FEATURES
* Three sequence square wave generators and one noise generator, software-compatible with the YM2149(SSG)

0 3 built-in 5-bit D/A convertors and mixed output

* CPU interface through /CS, /WR control signal and 8 bit data bus
* Wide voicing range of 8 octaves
* Smooth attenuation by wide dynamic range envelope generator
* Power down mode
* +5V single power supply, silicon gate CMOS process
* 16-pin plastic DIP(YMZ284-D) or 16-pin plastic SOP (YMZ284-M).

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**YMZ284 CATALOG  
CATALOG No. : -LSI 4MZ2843  
1994. 11**

YMZ284

■ PIN OUT DIAGRAM

ZWR

/CS

AO

VDD

SO

GND

</> M

/IO

1 16

2 15

3 14

4 13

5 12

6 11

7 10

8 9

DO

D 1

D2

D3

D4

D5

D6

D7

Top View (16pin DIP, 16pin SOP)

■ PIN DESCRIPTION

|  |  |  |  |
| --- | --- | --- | --- |
| No | Name | I/O | Function |
| 1 | /WR | I | CPU interface Write enable |
| 2 | Zes | I | CPU interface Chip select |
| 3 | AO | I | CPU interface Address/Data select |
| 4 | VDD | — | +5V power supply |
| 5 | SO | o | D/A convertor output for SSG |
| 6 | GND | — | Ground |
| 7 | </> M | I | Master clock input |
| 8 | ZIC | 1+ | Initial clear input |
| 9 | D7 | I | CPU interface data bus (MSB) |
| 10 | D6 | I | CPU interface data bus |
| 11 | D5 | I | CPU interface data bus |
| 12 | D4 | I | CPU interface data bus |
| 13 | D3 | I | CPU interface data bus |
| 14 | D2 | I | CPU interface data bus |
| 15 | D 1 | I | CPU interface data bus |
| 16 | DO | I | CPU interface data bus (LSB) |

Note) 1+ : Built-in pull-up register

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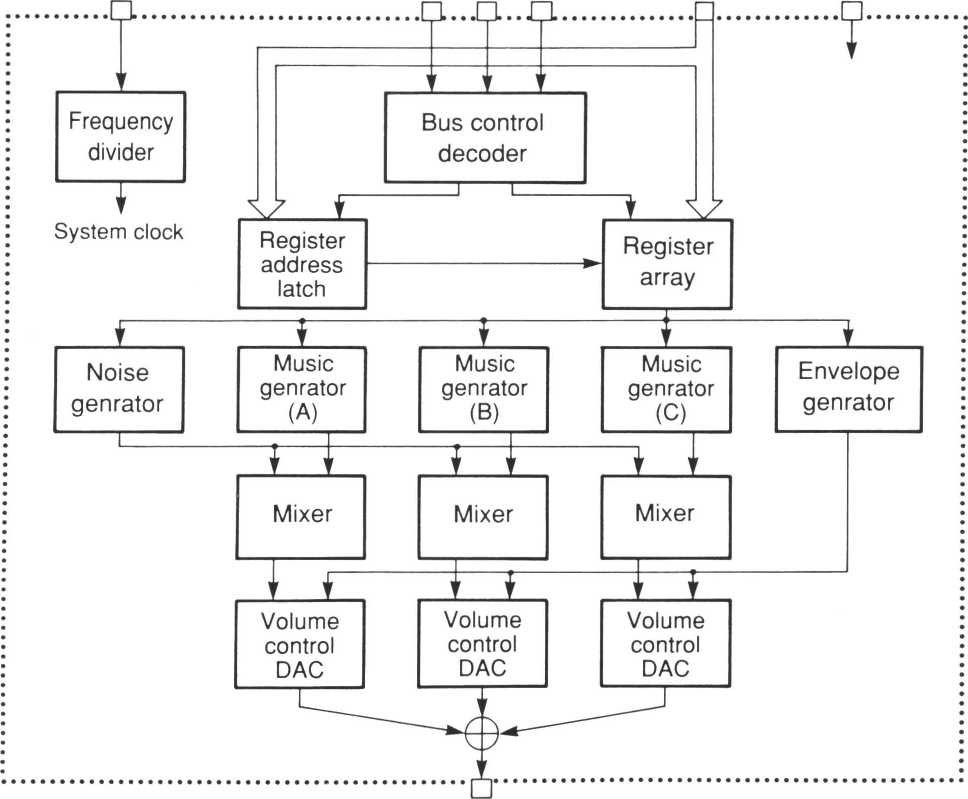
■ BLOCK DIAGRAM

ZIC

AO ZCS ZWR

*<f>* M

D0-D7



SO

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YMZ284

■ FUNCTIONS

1. . 4>M

Master clock input pin.

Frequency is 1MHz to 4MHz.

1. . D0-D7

8 bit data bus.

3 . ZCS • ZWR • A 0

Control write address and data from 8 bit data bus.

|  |  |  |  |
| --- | --- | --- | --- |
| ZCS | ZWR | AO | Function |
| L | L | L | Address write mode |
| L | L | H | Data write mode |

4. ZlC

‘L’ level resets the system clearing all register values.

1. SO

Analog output pin

1. VDD

+5V power supply pin

1. GND

Ground pin

■ FUNCTION DESCRIPTION

All functions of SSGL are controlled by the 15 internal registers.

Music generator Generates square waves of a different frequencies for each channel (A, B, and C).

Noise generator Generates pseudo-random waveforms (variable frequency).

Mixer Mixes 3-channels (A, B, and C) music and 1-channel noise generator output.

Volume control Constant level or variable level is given for each of the three channels (A, B, and C).

Constant levels are controlled by the CPU, and variable levels by the envelope generator.

Envelope generator Generates various types of attenuation.

D/A convertor Outputs mixed analog signal.

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■ REGISTER ARRAY

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| ADDR | Function | D7 | D6 | D5 | D4 | D3 | D2 | D 1 | DO |
| $00 | Channel A frequency | 8 bit fine tone adjustment | | | | | | | |
| $01 |  | | | | 4 bit rough tone adjustment | | | |
| $02 | Channel B frequency | 8 bit fine tone adjustment | | | | | | | |
| $03 |  | | | | 4 bit rough tone adjustment | | | |
| $04 | Channel C frequency | 8 bit fine tone adjustment | | | | | | | |
| $05 |  | | | | 4 bit rough tone adjustment | | | |
| $06 | Noise frequency |  | | | 5 bit noise frequency | | | | |
| $07 | Mixer setting |  | | Noise | | | Tone | | |
| C | B | A | C | B | A |
| $08 | Channel A level |  | | | M | L3 | L2 | LI | LO |
| $09 | Channel B level |  | | | M | L3 | L2 | LI | LO |
| $ 0A | Channel C level |  | | | M | L3 | L2 | LI | LO |
| $ OB | Envelope frequency | 8 bit fine adjustment | | | | | | | |
| $oc | 8 bit rough adjustment | | | | | | | |
| $ OD | Envelope shape |  | | | | CONT | ATT | ALT | HOLD |
| $ OF | Control power | ‘0’ | ‘0’ | ‘0’ | ‘0’ |  | | | |

Note) 1 I D7, D6, D5, and D4 bit of register $0F must be ‘0’ .

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■ REGISTER FUNCTION

• Music frequency setting ($00~$05)

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| The frequency f? of the square wave generated by each music generator (A, B, and C) is calculated by the following equation. | $00 (CH-A)  $02 (CH-B)  $04 (CH-C) | D7 | D6 | D5 | D4 | D3 | D2 | D 1 | DO |
| TP 7 | TP6 | TP 5 | TP 4 | TP 3 | TP 2 | TP 1 | TPO |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **fMaster**  fT = $01 (CH-A)  32TP $03 (CH-B)  $05 (CH-C) | D7 D6 D5 D4 | D3 | D2 | DI | DO |
|  | TP11 | TP10 | TP9 | TP8 |

fM™ is the frequency of master clock.

TP-TP11 \* 2" +TP10 \* 2'° + TP9 \* 29 + TP8 \* 28 + TP7 \* 27 + TP6 \* 26 + TP5 \* 25 + TP4 \* 24 + TP3 \* 2' + TP2 \* 22 +

TP1 \*2 + TP0

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| • Noise generator setting ($06) |  | | | | | | | | |
| The noise frequency fN is calculated by the following equation.  fMasler  fN- | D | 7 D6 | | D5 | D4 | D3 | D2 | D 1 | DO |
| $06 |  |  |  | : ; NP4 | NP3 | NP2 | NP 1 | NPO |

32NP

fMasm is the frequency of the master clock.

NP=NP4 \* 24 + NP3 \* 2’+ NP2 \* 22 + NP1 \* 2 + NPO

• Mixer setting ($07)

Setting ‘0’ enables sound output.

Mixed sound is output when both Noise and Tone outputs are set for the same channel.

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| $07 | D7 | D6 | D5 | D4 | D3 | D2 | DI | DO |
|  | | Noise | | | Tone | | |
| C | B | A | C | B | A |

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• Volume control and D/A convertor ($08~$0A)

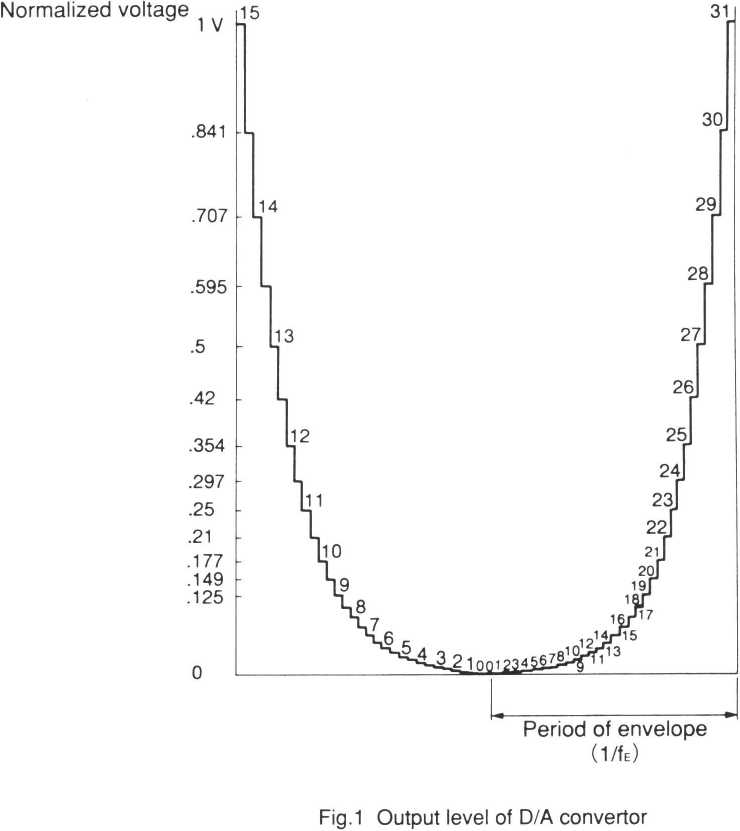
|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| The audio output level from the D/A convertors for the three channels (A, B, and C) is controlled as follows.  When M=0, the output level is deter­mined by the 4 bits of L3, L2, LI and | $08 (CH-A) $09 (CH-B) $ OA (CH-C) | D7 | D6 | D5 | D4 | D3 | D2 | DI | DO |
|  | | | M | L3 | L2 | LI | LO |

LO.

When M=l, the output level is determined by the 5 bits of E4, E3, E2, El and EO of the envelope generator of the

SSGL. (This output level is variable as E4—E0 change over time.)

When the maximum amplitude of the 5-bit D/A convertor is normalized to IV, the output levels shown in Fig.l are obtained.



The left half of the diagram shows fixed levels set by L3, L2, LI and LO bits.

The right half of the diagram shows output levels set by E4, E3, E2, El and EO bits.

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• Envelope frequency setting ($0B~$0C)

The envelope repetition frequency fE is  
calculated by the following equation.

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| $ OB | D7 | D6 | D5 | D4 | D3 | D2 | DI | DO |
| EP 7 | EP6 | EP 5 | EP 4 | EP 3 | EP 2 | EPl | EPO |

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| $0C | D7 | D6 | D5 | D4 | D3 | D2 | D 1 | DO |
| EP15 | EPl 4 | EP13 | EPl 2 | EPl 1 | EP10 | EP9 | EP 8 |

fE =

512EP

fMMer is the frequency of the master clock.

EP=EP15 \* 2I5 + EP14\* 2'4 + EP13 \* 2'3 + EP12 \* 2,2 + EPl 1 \* 2"+ EP10 \* 2,0 + EP9 \* 29 + EP8 \* 28 + EP7 \* 27 + EP6 \* *T* + EP5 \* *T* + EP4 \* 24 + EP3 \* 2’ + EP2 \* 22 + EP 1 \* 2 + EPO

The period of the actual frequency fE\* used for the nvelope generated is 1/32 of the envelope repetition period (1 /fE).

• Envelope shape control (SOD)

The envelope generator counts the enve­lope clock fEA 32 times for each envelope pattern cycle. The envelope level is determined by the 5 bit output (E4 — E0) of the counter.

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Sod | D7 | D6 | D5 | D4 | D3 | D2 | D 1 | DO |
|  | | | | CONT | ATT | ALT | HOLD |

The shape of this envelope is created by increasing, decreasing, stopping, or repeating this counter.

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wk

• Volume control and D/A convertor ($08~$0A)

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| The audio output level from the D/A convertors for the three channels (A, B, and C) is controlled as follows.  When M=0, the output level is deter­mined by the 4 bits of L3, L2, LI and | $08 (CH-A) $09 (CH-B) $ 0A (CH-C) | D7 | D6 | D5 | D4 | D3 | D2 | D 1 | DO |
|  | | | M | L3 | L2 | LI | LO |

LO.

When M=l, the output level is determined by the 5 bits of E4, E3, E2, El and EO of the envelope generator of the

SSGL. (This output level is variable as E4~E0 change over time.)

When the maximum amplitude of the 5-bit D/A convertor is normalized to IV, the output levels shown in Fig.l are obtained.

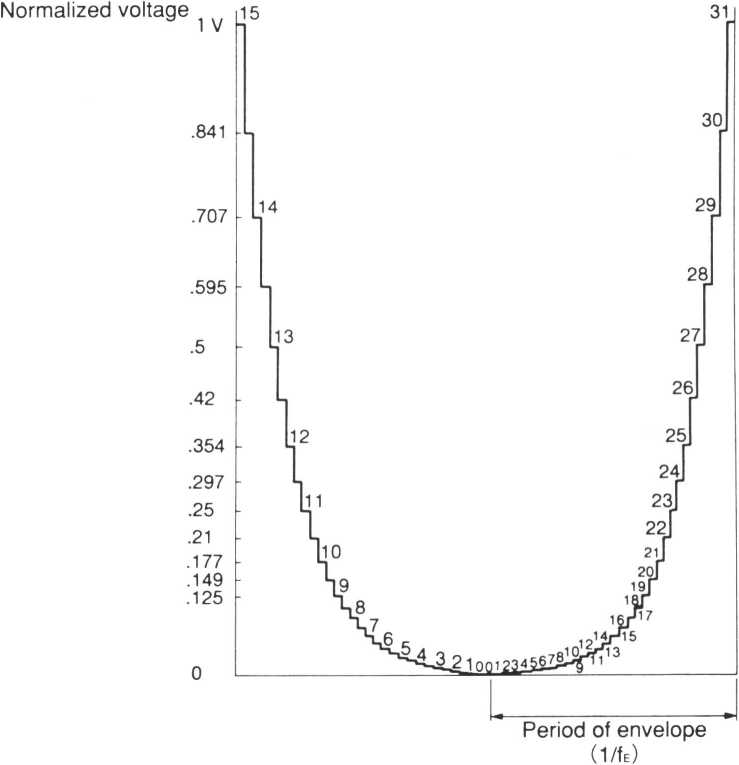


Fig.1 Output level of D/A convertor

The left half of the diagram shows fixed levels set by L3, L2, LI and LO bits.

The right half of the diagram shows output levels set by E4, E3, E2, El and EO bits.

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Below envelope types are selected by CONT, ATT, ALT and HOLD setting.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| D. | Dz | D, | Do | Envelope shape |
| CONT | ATT | ALT | HOLD |
| o | o | x | x |  |
| o | 1 | x | x |  |
|  |  |  |  |  |
| 1  1 | 0  0 | 0  o | 0  1 |  |
|  |  |  |  |  |
| 1 | 0 | 1 | 0 |  |
| 1 | 0 | 1 | 1 |  |
| 1 | 1 | 0 | 0 |  |
| 1 | 1 | 0 | 1 |  |
| 1 | 1 | 1 | 0 |  |
| 1 |  |  |  | ' 1 |
|  |  |  |  |  |

I 1 / fE I— Repetition period of envelope

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■ ELECTRICAL CHARACTERISTICS

1. Absolute maximum ratings

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Item | Symbol | Rating | | Unit |
| Power supply voltage | V DD | -0.3 - | - 7.0 | V |
| Input voltage | V. | Vss-0.3 ~ | - Voo+0.3 | V |
| Storage temperature | Tstg | -50 - | - 125 | °C |

2. Recommended operating conditions

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Item | Symbol | Min. | Typ. | Max. | Unit |
| Power supply voltage | Vdd | 4.75 | 5 | 5.25 | V |
| Operation temperature | Top | 0 | 25 | 70 | °C |

3. DC Characteristics (Conditions : Ta = 0~70 ”C, Voo = 5.0±0.25V)

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Item | Symbol | Condition | Min. | Typ. | Max. | Unit |
| Input highlevel voltage | VlH | \* 1 | 2.2 |  |  | V |
| Input lowlevel voltage | V1L | \* 1 |  |  | 0.8 | V |
| Input highlevel voltage | VlH | \*2 | 3.5 |  |  | V |
| Input lowlevel voltage | V1L | \*2 |  |  | 1.0 | V |
| Input leak current | lu | V, = 0-5V, \*1 | -10 |  | 10 | pA |
| Pull-up registance | Ru | \*2 | 60 | 250 | 600 | kfi |
| Input capacity | Ci | \*3 |  |  | 10 | PF |
| Power supply current | Idd |  |  |  | 10 | mA |

Note) \* 1 : Applied to all input pins except /IC.

* 2 : Applied to /IC.
* 3 : Applied to all input pins.

4. Analog Characteristics (Conditions : Ta=0~70°C, Voo=5.0±0.25V)

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Item | Symbol | Condition | Min. | Typ. | Max. | Unit |
| Analog output voltage | VOA | \* 1 | 1.50 | 1.70 | 1.90 | V |

Note) \* 1 : Applied to SO pin. Maximum volume, Rl=1 k ST, peak to peak.

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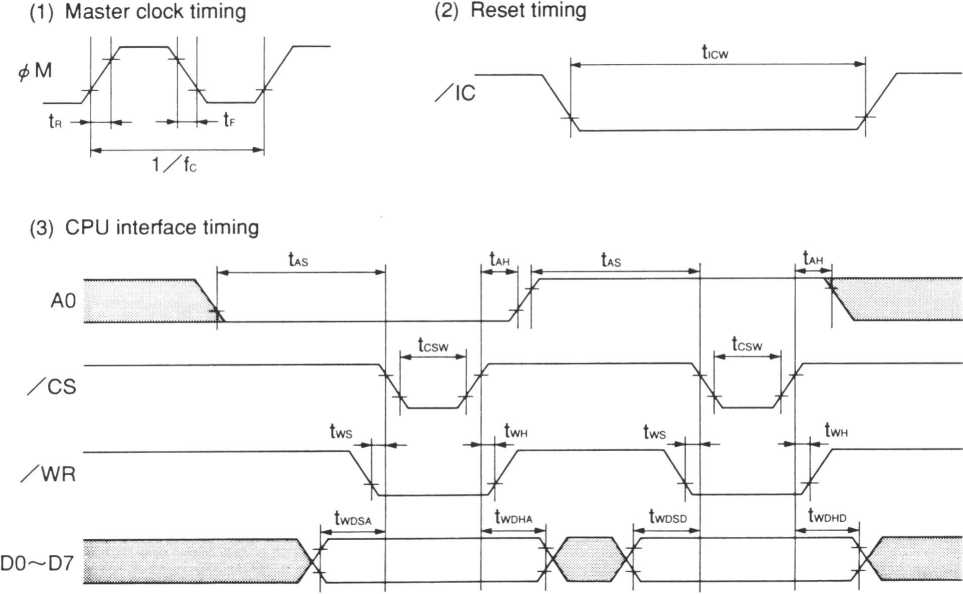
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MM

5. AC Characteristics (Conditions : Ta = 0~70°C, Voo = 5.0±0.25V)

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Item | Symbol | Min. | Typ. | Max. | Unit |
| Master clock frequency | **fc** | I |  | 4 | MHz |
| Master clock duty | D | 40 |  | 60 | % |
| Master clock rise time |  |  |  | 20 | ns |
| Master clock fall time | **b** |  |  | 20 | ns |
| Reset pulse width | **ticw** | 5 |  |  | X/s |
| Address setup time | **Us** | 20 |  |  | ns |
| Address hold time | IaH | 10 |  |  | ns |
| Chip select write width | **tcsw** | 30 |  |  | ns |
| Write pulse write width | **tws** | 0 |  |  | ns |
| Write data hold time | **twH** | 0 |  |  | ns |
| Write data setup time (Address) | **twDSA** | 10 |  |  | ns |
| Write data setup time (Data) | **twDSD** | 10 |  |  | ns |
| Write data hold time (Address) | **twDHA** | 10 |  |  | ns |
| Write data hold time (Data) | **twDHD** | 10 |  |  | ns |

6. Timing diagram

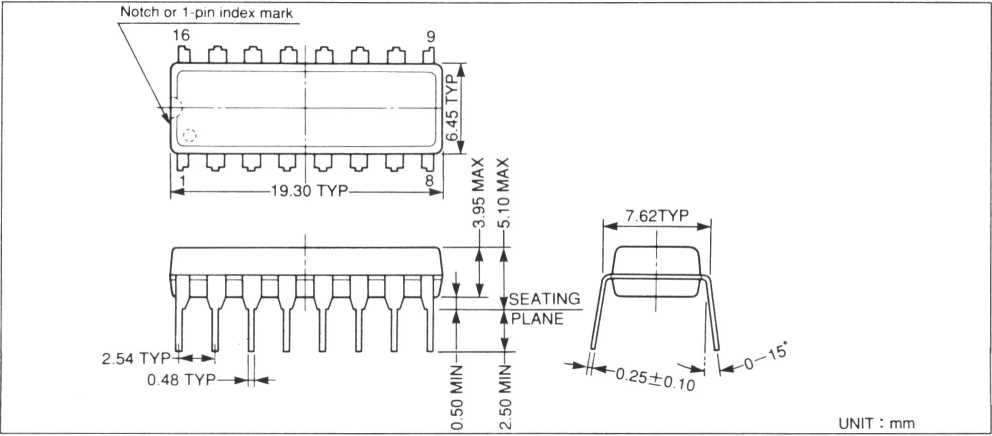


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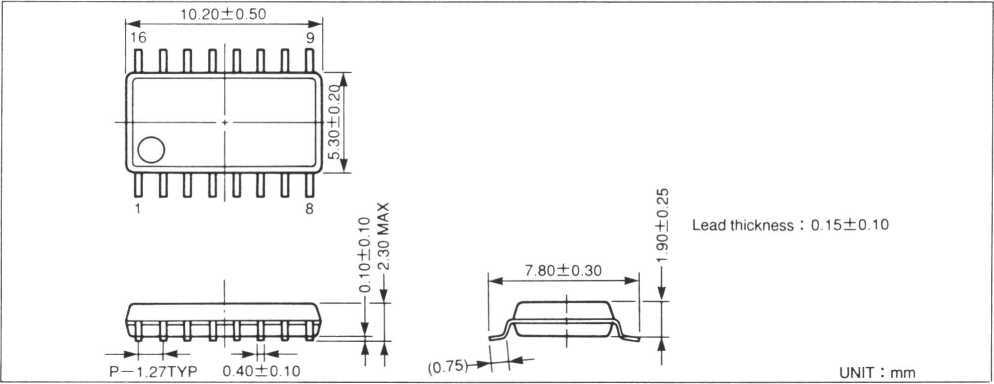
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■ EXTERNAL DIMENSIONS

• YMZ284-D



• YMZ284-M



The specifications of this product are subject to improvement changes without prior notice.



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