**HM5117805 Series**

16 M EDO DRAM (2-Mword x 8-bit)

2 k Refresh

***ELPIDA***

E0156H10 (Ver. 1.0)

(Previous ADE-203-630D (Z))

Jun. 27, 2001

Description

The HM5117805 is a CMOS dynamic RAM organized 2,097,152-word x 8-bit. It employs the most advanced CMOS technology for high performance and low power. The HM5117805 offers Extended Data Out (EDO) Page Mode as a high speed access mode. Multiplexed address input permits the HM5117805 to be packaged in standard 28-pin plastic SOJ and 28-pin TSOP.

Features

* Single 5 V (±10%)
* Access time: 50 ns/60 ns/70 ns (max)
* Power dissipation
* Active mode: 605 mW/550 mW/495 mW (max)
* Standby mode : 11 mW (max)

: 0.83 mW (max) (L-version)

* EDO page mode capability
* Long refresh period

— 2048 refresh cycles : 32 ms

: 128 ms (L-version)

• 4 variations of refresh

* RAS-only refresh
* CAS-before-RAS refresh
* Hidden refresh
* Self refresh (L-version)

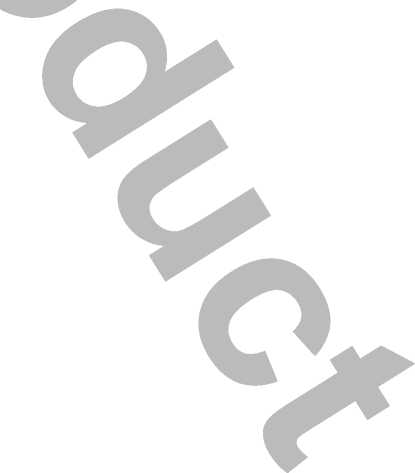
• Battery backup operation (L-version)

Elpida Memory, Inc. is a joint venture DRAM company of NEC Corporation and Hitachi, Ltd.

**HM5117805 Series**

Ordering Information

|  |  |  |
| --- | --- | --- |
| **Type No.** | **Access time** | **Package** |
| HM5117805J-5 | 50 ns | 400-mil 28-pin plastic SOJ (CP-28DA) |
| HM5117805J-6 | 60 ns |  |
| HM5117805J-7 | 70 ns |  |
| HM5117805LJ-5 | 50 ns |  |
| HM5117805LJ -6 | 60 ns |  |
| HM5117805LJ -7 | 70 ns |  |
| HM5117805S-5 | 50 ns | 300-mil 28-pin plastic SOJ (CP-28DNA) |
| HM5117805S-6 | 60 ns |  |
| HM5117805S-7 | 70 ns |  |
| HM5117805LS-5 | 50 ns |  |
| HM5117805LS-6 | 60 ns |  |
| HM5117805LS-7 | 70 ns |  |
| HM5117805TT-5 | 50 ns | 400-mil 28-pin plastic TSOP II (TTP-28DA) |
| HM5117805TT-6 | 60 ns |  |
| HM5117805TT-7 | 70 ns |  |
| HM5117805LTT-5 | 50 ns |  |
| HM5117805LTT-6 | 60 ns |  |
| HM5117805LTT-7 | 70 ns |  |
| HM5117805TS-5 | 50 ns | 300-mil 28-pin plastic TSOP II (TTP-28DB) |
| HM5117805TS-6 | 60 ns |  |
| HM5117805TS-7 | 70 ns |  |
| HM5117805LTS-5 | 50 ns |  |
| HM5117805LTS-6 | 60 ns |  |
| HM5117805LTS-7 | 70 ns |  |



Data Sheet E0156H10 ***ELPIDA***

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**HM5117805 Series**

Pin Arrangement

HM5117805J/LJ Series

HM5117805S/LS Series

HM5117805TT/LTT Series

HM5117805TS/LTS Series

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| VCC | | 1 | 28 | VSS | | VCC | — | 1 o | 28 | — | VSS |
| I/O0 |  | 2 | 27 |  | I/O7 | I/O0 |  | 2 | 27 |  | I/O7 |
| I/O1 |  | 3 | 26 |  | I/O6 | I/O1 |  | 3 | 26 |  | I/O6 |
| I/O2 |  | 4 | 25 |  | I/O5 | I/O2 |  | 4 | 25 |  | I/O5 |
| I/O3 |  | 5 | 24 |  | I/O4 | I/O3 |  | 5 | 24 |  | I/O4 |
| WE |  | 6 | 23 |  | CAS | WE |  | 6 | 23 |  | CAS |
| RAS |  | 7 | 22 |  | OE | RAS |  | 7 | 22 |  | OE |
| NC |  | 8 | 21 |  | A9 | NC |  | 8 | 21 |  | A9 |
| A10 |  | 9 | 20 |  | A8 | A10 |  | 9 | 20 |  | A8 |
| A0 |  | 10 | 19 |  | A7 | A0 |  | 10 | 19 |  | A7 |
| A1 |  | 11 | 18 | — | A6 | A1 |  | 11 | 18 |  | A6 |
| A2 |  | 12 | 17 | — | A5 | A2 |  | 12 | 17 |  | A5 |
| A3 |  | 13 | 16 | — | A4 | A3 |  | 13 | 16 |  | A4 |
| VCC | — | 14 | 15 | — | VSS | VCC | r | 14 | 15 |  | VSS |

(Top view)

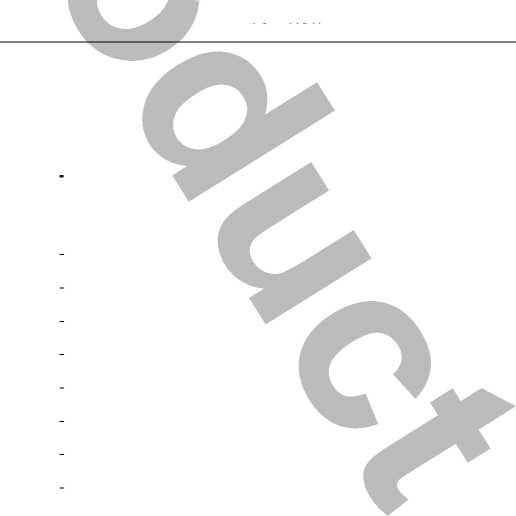
Pin Description

|  |  |
| --- | --- |
| **Pin name** | **Function** |
| A0 to A10 | Address input  — Row/Refresh address A0 to A10  — Column address A0 to A9 |
| I/O0 to I/O7 | Data input/Data output |
| RAS | Row address strobe |
| CAS | Column address strobe |
| WE | Read/Write enable |
| OE | Output enable |
| VCC | Power supply |
| VSS | Ground |
| NC | No connection |

(Top view)

Data Sheet E0156H10 ***ELPIDA***

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**HM5117805 Series**

Block Diagram

RAS

CAS

WE

OE

Timing and control

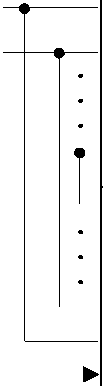
A0

A1

to

A9

A10



Column

address

buffers

Row

address

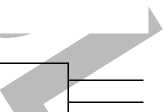
buffers

|  |  |  |  |
| --- | --- | --- | --- |
|  | Column decoder |  | |
|  |
|  | 2M array |  | => |
|  | 2M array | M— | => |
|  | 2M array |  | k, |
| jepooep mo^j | 2M array |  | => |
| 2M array | M— | => |
| 2M array |  | k, |
|  | 2M array | «= | => |
|  | 2M array | M— | => |

|  |  |
| --- | --- |
|  | I/O0 |
| I/O buffers | to |
|  | I/O7 |
|  |  |

Data Sheet E0156H10 ***ELPIDA***

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|  |  |  |  |
| --- | --- | --- | --- |
|  | | **HM5117805 Series** | |
| **Absolute Maximum Ratings**  **Parameter** | **Symbol** | **Value** | **Unit** |
| Voltage on any pin relative to VSS | *Vt* | -1.0 to +7.0 | V |
| Supply voltage relative to VSS | *VCC* | -1.0 to +7.0 | V |
| Short circuit output current | *Iout* | 50 | mA |
| Power dissipation | *PT* | 1.0 | W |
| Operating temperature | *Topr* | 0 to +70 | °C |
| Storage temperature | Tstg | -55 to +125 | °C |

**Recommended DC Operating Conditions** (Ta = 0 to +70°C)

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Parameter** | **Symbol** | **Min** | **Typ** | **Max** | **Unit** | **Note** |
| Supply voltage | Vcc | 4.5 | 5.0 | 5.5 | V | 1 |
| Input high voltage | VIH | 2.4 | — | 6.5 | V | 1 |
| Input low voltage | Vil | -1.0 | — | 0.8 | V | 1 |

Note: 1. All voltage referred to VSS.



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**HM5117805 Series**

**DC Characteristics** (Ta = 0 to +70°C, VCC = 5 V ± 10%, VSS = 0 V)

**HM5117805**

**-5 -6 -7**

|  |  |
| --- | --- |
| **Parameter** | **Symbol Min Max Min Max Min Max Unit Test conditions** |
| Operating current\*1, \*2 | I cci — 110 — 100 — 90 mA tRc = min |
| Standby current | I CC2 — 2 — 2 — 2 mA TTL interface  RAS, CAS = VIH |

Dout = High-Z

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  | — | 1 | — | 1 | — | 1 | mA | CMOS interface  RAS, CAS > VCC - 0.2 V  Dout = High-Z |
| Standby current (L-version) | ICC2 | — | 150 | — | 150 | — | 150 | pA | CMOS interface  RAS, CAS > VCC - 0.2 V  Dout = High-Z |
| RAS-only refresh current\*2 | ICC3 | — | 110 | — | 100 | — | 90 | mA | tRC = min |
| Standby current\*1 | ICC5 | — | 5 | — | 5 | — | 5 | mA | RAS = VIH CAS = VIL Dout = enable |
| CAS-before-RAS refresh current | ICC6 | — | 110 | — | 100 | — | 90 | mA | tRC = min |
| EDO page mode current\*1, \*3 | ICC7 | — | 100 | — | 90 | — | 85 | mA | tHPC = min |
| Battery backup current\*4 (Standby with CBR refresh) (L-version) | ICC10 | — | 500 | — | 500 | — | 500 | pA | CMOS interface Dout = High-Z CBR refresh: tRC = 62.5 ps tRAS £ 0.3 ps |
| Self refresh mode current (L-version) | ICC11 | — | 300 | — | 300 | — | 300 | pA | CMOS interface  RAS, CAS £ 0.2V  Dout = High-Z |
| Input leakage current | ILI | -10 | 10 | -10 | 10 | -10 | 10 | pA | 0 V £ Vin £ 7 V |
| Output leakage current | ILO | -10 | 10 | -10 | 10 | -10 | 10 | pA | 0 V £ Vout £ 7 V  Dout = disable |
| Output high voltage | VOH | 2.4 | VCC | 2.4 | VCC | 2.4 | VCC | V | High Iout = -2 mA |
| Output low voltage | VOL | 0 | 0.4 | 0 | 0.4 | 0 | 0.4 | V | Low Iout = 2 mA |

Notes: 1. ICC depends on output load condition when the device is selected. ICC max is specified at the output open condition.

2. Address can be changed once or less while RAS = VIL.

3. Address can be changed once or less while CAS = VIH.

4. CAS = L (£ 0.2 V) while RAS = L (£ 0.2 V).

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**HM5117805 Series**

**Capacitance** (Ta = 25°C, VCC = 5 V ± 10%)

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Parameter** | **Symbol** | **Typ** | **Max** | **Unit** | **Notes** |
| Input capacitance (Address) | C|1 | *—* | 5 | PF | 1 |
| Input capacitance (Clocks) | CI2 | *—* | *7* | pF | 1 |
| Output capacitance (Data-in, Data-out) | *CI/O* | *—* | *7* | PF | 1,2 |

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.

2. CAS = VIH to disable Dout.

**AC Characteristics** (Ta = 0 to +70°C, VCC = 5 V ±10%, VSS = 0 V)\*1, \*2, \*18

**Test Conditions**

* Input rise and fall time: 2 ns
* Input levels: VIL = 0 V, VIH = 3 V
* Input timing reference levels: 0.8 V, 2.4 V
* Output timing reference levels: 0.8 V, 2.0 V
* Output load: 1 TTL gate + CL (100 pF) (Including scope and jig)



Data Sheet E0156H10 ***ELPIDA***

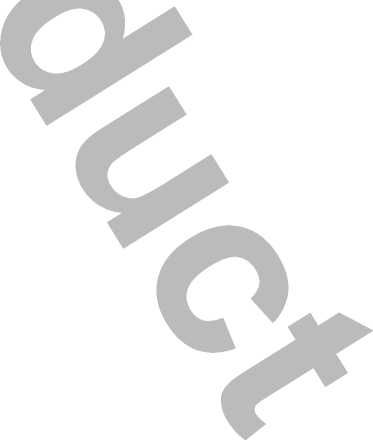
7

**HM5117805 Series**

**Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)**

**HM5117805**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Parameter** | **Symbol** | **-5** | | **-6** | | **-7** | | **Unit** | **Notes** |
| **Min** | **Max** | **Min** | **Max** | **Min** | **Max** |
| Random read or write cycle time | tRC | 84 | — | 104 | — | 124 | — | ns |  |
| RAS precharge time | tRP | 30 | — | 40 | — | 50 | — | ns |  |
| CAS precharge time | tCP | 7 | **—** | 10 | — | 13 | — | ns |  |
| RAS pulse width | tRAS | 50 | 10000 | 60 | 10000 | 70 | 10000 | ns |  |
| CAS pulse width | tCAS | 7 | 10000 | 10 | 10000 | 13 | 10000 | ns |  |
| Row address setup time | tASR | 0 | **—** | 0 | — | 0 | — | ns |  |
| Row address hold time | tRAH | 7 |  | 10 | — | 10 | — | ns |  |
| Column address setup time | tASC | 0 | **—** | 0 | — | 0 | — | ns |  |
| Column address hold time | tCAH | 7 |  | 10 | — | 13 | — | ns |  |
| RAS to CAS delay time | tRCD | 11 | 37 | 14 | 45 | 14 | 52 | ns | 3 |
| RAS to column address delay time | tRAD | 9 | 25 | 12 | 30 | 12 | 35 | ns | 4 |
| RAS hold time | tRSH | 10 | — | 13 | — | 13 | — | ns |  |
| CAS hold time | tCSH | 35 | — | 40 | — | 45 | — | ns |  |
| CAS to RAS precharge time | tCRP | 5 | **—** | 5 | **—** | 5 | — | ns |  |
| OE to Din delay time | tOED | 13 | — | 15 | — | 18 | — | ns | 5 |
| OE delay time from Din | tDZO | 0 |  | 0 |  | 0 | — | ns | 6 |
| CAS delay time from Din | tDZC | 0 |  | 0 |  | 0 | — | ns | 6 |
| Transition time (rise and fall) | tT | 2 | 50 | 2 | 50 | 2 | 50 | ns | 7 |



Data Sheet E0156H10 ***ELPIDA***

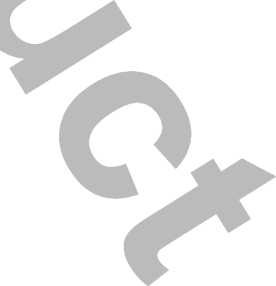
8

**HM5117805 Series**

**Read Cycle**

**HM5117805**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  | **-5** |  | **-6** |  | **-7** |  |  |  |
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Unit** | **Notes** |
| Access time from RAS | tRAC | — | 50 | — | 60 | — | 70 | ns | 8, 9 |
| Access time from CAS | tCAC | — | 13 | — | 15 | — | 18 | ns | 9, 10, 17 |
| Access time from address | tAA | — | 25 | — | 30 | — | 35 | ns | 9, 11, 17 |
| Access time from OE | tOEA | — | 13 | — | 15 | — | 18 | ns | 9 |
| Read command setup time | tRCS | 0 | — | 0 | — | 0 | — | ns |  |
| Read command hold time to CAS | tRCH | 0 | — | 0 | — | 0 | — | ns | 12 |
| Read command hold time from RAS | tRCHR | 50 | — | 60 | — | 70 | — | ns |  |
| Read command hold time to RAS | tRRH | 0 | — | 0 | — | 0 | — | ns | 12 |
| Column address to RAS lead time | tRAL | 25 | — | 30 | — | 35 | — | ns |  |
| Column address to CAS lead time | tCAL | 15 | — | 18 | — | 23 | — | ns |  |
| CAS to output in low-Z | tCLZ | 0 | — | 0 | — | 0 | — | ns |  |
| Output data hold time | tOH | 3 | — | 3 | — | 3 | — | ns | 20 |
| Output data hold time from OE | tOHO | 3 | — | 3 | — | 3 | — | ns |  |
| Output buffer turn-off time | tOFF | — | 13 | — | 15 | — | 15 | ns | 13, 20 |
| Output buffer turn-off to OE | tOEZ | — | 13 | — | 15 | — | 15 | ns | 13 |
| CAS to Din delay time | tCDD | 13 | — | 15 | — | 18 | — | ns | 5 |
| Output data hold time from RAS | tOHR | 3 | — | 3 | — | 3 | — | ns | 20 |
| Output buffer turn-off to RAS | tOFR | — | 13 | — | 15 | — | 15 | ns | 20 |
| Output buffer turn-off to WE | tWEZ | — | 13 | — | 15 | — | 15 | ns |  |
| WE to Din delay time | tWED | 13 | — | 15 | — | 18 | — | ns |  |
| RAS to Din delay time | tRDD | 13 | — | 15 | — | 18 | — | ns |  |
| RAS next CAS delay time | tRNCD | 50 | — | 60 | — | 70 | — | ns |  |



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**HM5117805 Series**

**Write Cycle**

**HM5117805**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Parameter** | **Symbol** | **-5** | | **-6** | | **-7** | | **Unit** | **Notes** |
| **Min** | **Max** | **Min** | **Max** | **Min** | **Max** |
| Write command setup time | tWCS | 0 | — | 0 | — | 0 | — | ns | 14 |
| Write command hold time | tWCH | 7 | — | 10 | — | 13 | — | ns |  |
| Write command pulse width | tWP | 7 | — | 10 | — | 10 | — | ns |  |
| Write command to RAS lead time | tRWL | 7 | — | 10 | — | 13 | — | ns |  |
| Write command to CAS lead time | tCWL | 7 | — | 10 | — | 13 | — | ns |  |
| Data-in setup time | tDS | 0 | — | 0 | — | 0 | — | ns | 15 |
| Data-in hold time | tDH | 7 | — | 10 | — | 13 | — | ns | 15 |
| **Read-Modify-Write Cycle** | | | | | | | | | |

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Parameter** | **Symbol** | **-5** | **-6** | **-7** | | |
| **Min** | **Max Min** | **Max Min** | **Max Unit** | **Notes** |
| Read-modify-write cycle time | tRWC | 111 | — 135 | — 161 | — ns |  |
| RAS to WE delay time | tRWD | 67 | — 79 | — 92 | — ns | 14 |
| CAS to WE delay time | tCWD | 30 | — 34 | — 40 | — ns | 14 |
| Column address to WE delay time | tAWD | 42 | — 49 | — 57 | — ns | 14 |
| OE hold time from WE | tOEH | 13 | — 15 | — 18 | — ns |  |

**Refresh Cycle**

**HM5117805**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
|  |  | **-5** | **-6** |  | **-7** |  |  |
| **Parameter** | **Symbol** | **Min** | **Max Min** | **Max** | **Min** | **Max Unit** | **Notes** |
| CAS setup time (CBR refresh cycle) tCSR | | 5 | — 5 | — | 5 | —ns |  |
| CAS hold time (CBR refresh cycle) | tCHR | 7 | — 10 | — | 10 | — ns |  |
| WE setup time (CBR refresh cycle) | tWRP | 0 | —0 | — | 0 | —ns |  |
| WE hold time (CBR refresh cycle) | tWRH | 7 | — 10 | — | 10 | — ns |  |
| RAS precharge to CAS hold time | tRPC | 5 | —5 | — | 5 | —ns |  |

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**HM5117805 Series**

**EDO Page Mode Cycle**

**HM5117805**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Parameter** | **Symbol** | **-5** | | **-6** | | **-7** | | **Unit** | **Notes** |
| **Min** | **Max** | **Min** | **Max** | **Min** | **Max** |
| EDO page mode cycle time | tHPC | 20 | — | 25 | — | 30 | — | ns | 19 |
| EDO page mode RAS pulse width | tRASP | — | 100000 | — | 100000 | — | 100000 | ns | 16 |
| Access time from CAS precharge | tCPA | — | 28 | — | 35 | — | 40 | ns | 9, 17 |
| RAS hold time from CAS precharge tCPRH | | 28 | — | 35 | — | 40 | — | ns |  |
| Output data hold time from CAS low tDOH | | 3 | — | 3 | — | 3 | — | ns | 9, 17 |
| CAS hold time referred OE | tCOL | 7 | — | 10 | — | 13 | — | ns |  |
| CAS to OE setup time | tCOP | 5 | — | 5 | — | 5 | — | ns |  |
| Read command hold time from CAS tRCHC precharge | | 28 | — | 35 | — | 40 | — | ns |  |

**EDO Page Mode Read-Modify-Write Cycle**

**HM5117805**

|  |  |  |  |
| --- | --- | --- | --- |
|  | **1-5** | **-6** | **-7** |
| **Parameter Symbol** | **Min** | **Max Min** | **Max Min Max Unit Notes** |
| EDO page mode read- modify-write tHPRWC | 57 | — 68 | — 79 ns |
| cycle time |  |  |  |
| WE delay time from CAS precharge tCPW | 45 | — 54 | — 62 ns 14 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Refresh** | | | **Unit** | **Note** |
| **Parameter** | **Symbol** | **Max** |
| Refresh period | tREF | 32 | ms | 2048 cycles |
| Refresh period (L-version) | tREF | 128 | ms | 2048 cycles |



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**HM5117805 Series**

**Self Refresh Mode (L-version)**

**HM5117805L**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Parameter** | **Symbol** | **-5** | **-6** | | **-7** | | |
| **Min** | **Max Min** | **Max** | **Min** | **Max Unit** | **Notes** |
| RAS pulse width (self refresh) | tRASS | 100 | — 100 | — | 100 | — ps |  |
| RAS precharge time (self refresh) | tRPS | 90 | — 110 | — | 130 | — ns |  |
| CAS hold time (self refresh) | tCHS | -50 | — -50 | — | -50 | — ns |  |

Notes: 1. AC measurements assume tT = 2 ns.

1. An initial pause of 200 ps is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing RAS-only refresh or CAS-before-RAS refresh). If the internal refresh counter is used, a minimum of eight CAS-before-RAS refresh cycles are required.
2. Operation with the tRCD (max) limit insures that tRAC (max) can be met, tRCD (max) is specified as a reference point only; if tRCD is greater than the specified tRCD (max) limit, then access time is controlled exclusively by tCAC.
3. Operation with the tRAD (max) limit insures that tRAC (max) can be met, tRAD (max) is specified as a reference point only; if tRAD is greater than the specified tRAD (max) limit, then access time is controlled exclusively by tAA.
4. Either tOED or tCDD must be satisfied.
5. Either tDZO or tDZC must be satisfied.
6. VIH (min) and VIL (max) are reference levels for measuring timing of input signals. Also, transition times are measured between VIH (min) and VIL (max).
7. Assumes that tRCD £ tRCD (max) and tRAD £ tRAD (max). If tRCD or tRAD is greater than the maximum recommended value shown in this table, tRAC exceeds the value shown.
8. Measured with a load circuit equivalent to 1 TTL loads and 100 pF.
9. Assumes that tRCD > tRCD (max) and tRAD < tRAD (max).
10. Assumes that tRCD < tRCD (max) and tRAD tRAD (max).
11. Either tRCH or tRRH must be satisfied for a read cycles.
12. tOFF (max) and tOEZ (max) define the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
13. tWCS, tRWD, tCWD, tAWD and tCPW are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if tWCS > tWCS (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if tRWD> tRWD(min), tCWD > tcwD (min), and t

AWD S tAWD (min), or tCWD > tcwD (min), t

AWD S tAWD (min) and t CPW > tcpw (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

1. These parameters are referred to CAS leading edge in early write cycles and to WE leading edge in delayed write or read-modify-write cycles.
2. tRASP defines RAS pulse width in EDO page mode cycles.
3. Access time is determined by the longest among tAA, tCAC and tCPA.
4. In delayed write or read-modify-write cycles, OE must disable output buffer prior to applying data to the device.
5. tHPC (min) can be achieved during a series of EDO page mode write cycles or EDO page mode read cycles. If both write and read operation are mixed in a EDO page mode RAS cycle (EDO page mode mix cycle (1), (2)), minimum value of CAS cycle (tCAS + tCP + 2 tT) becomes greater than the specified tHPC (min) value.The value of CAS cycle time of mixed EDO page mode is shown in EDO page mode mix cycle (1) and (2).

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**HM5117805 Series**

1. Data output turns off and becomes high impedance from later rising edge of RAS and CAS . Hold time and turn off time are specified by the timing specifications of later rising edge of RAS and CAS between tOHR and tOH and between tOFR and tOFF.
2. Please do not use tRASS timing, 10 ps < tRASS < 100 ps. During this period, the device is in transition state from normal operation mode to self refresh mode. If tRASS > 100 ps, then RAS precharge time should use tRPS instead of tRP.
3. If you use RAS only refresh or CBR burst refresh mode in normal read/write cycles, 2048 cycles of distributed CBR refresh with 15.6 ps interval should be executed within 32 ms immediately after exiting from and before entering into the self refresh mode.
4. If you use distributed CBR refresh mode with 15.6 ps interval in normal read/write cycle, CBR refresh should be executed within 15.6 ps immediately after exiting from and before entering into self refresh mode.
5. Repetitive self refresh mode without refreshing all memory is not allowed. Once you exit from self fresh mode, all memory cells need to be refreshed before re-entering the self refresh mode again.
6. XXX: H or L (H: VIH (min) £ VIN £ VIH (max), L: VIL (min) £ VIN £ VIL (max))

///////: Invalid Dout

When the address, clock and input pins are not described on timing waveforms, their pins must be applied VIH or VIL.



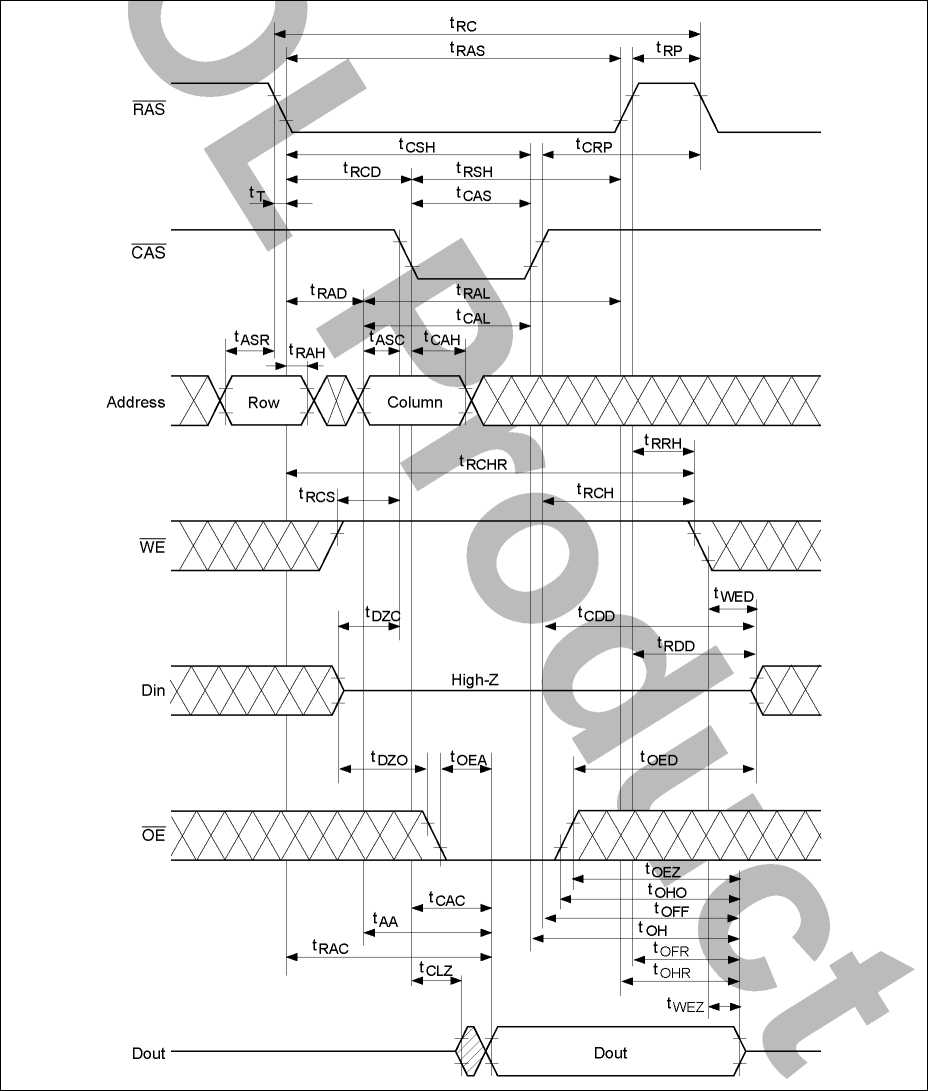
Data Sheet E0156H10 ***ELPIDA***

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**HM5117805 Series**

Timing Waveforms\*25

**Read Cycle**

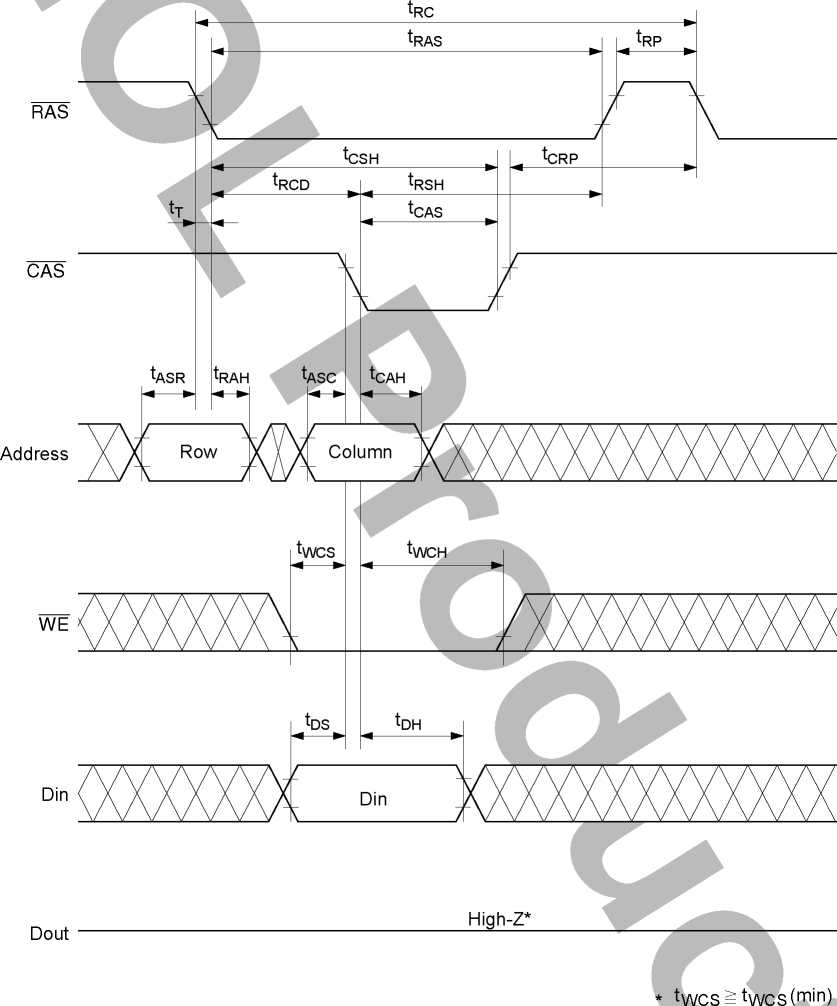


Data Sheet E0156H10 ***ELPIDA***

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**HM5117805 Series**

Early Write Cycle



Data Sheet E0156H10 ***ELPIDA***

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**HM5117805 Series**

Delayed Write Cycle\*18

RAS

CAS

Address



tRP

tRC tRAS

tCRP

tRCD

tASR

tRAH

tASC

tCAH

Row

tRSH

tCAS



Column

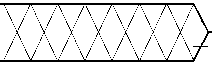
tRCS

WE

KW

tDZC

Din



tDZO

tCSH

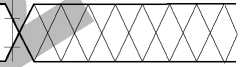
tCWL tRWL tWP

tDS

tDH



Din



tOED

tOEH

Xxxxxxxxx;

Dout

**tOEZ**

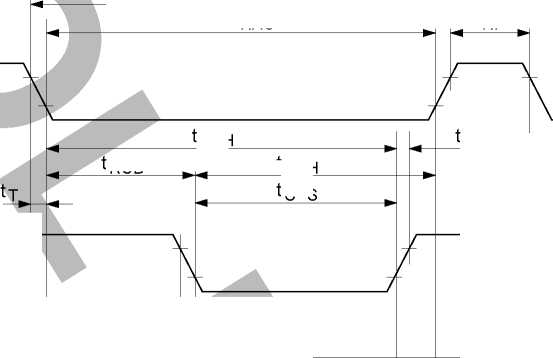
tCL

High-Z

Invalid Dout

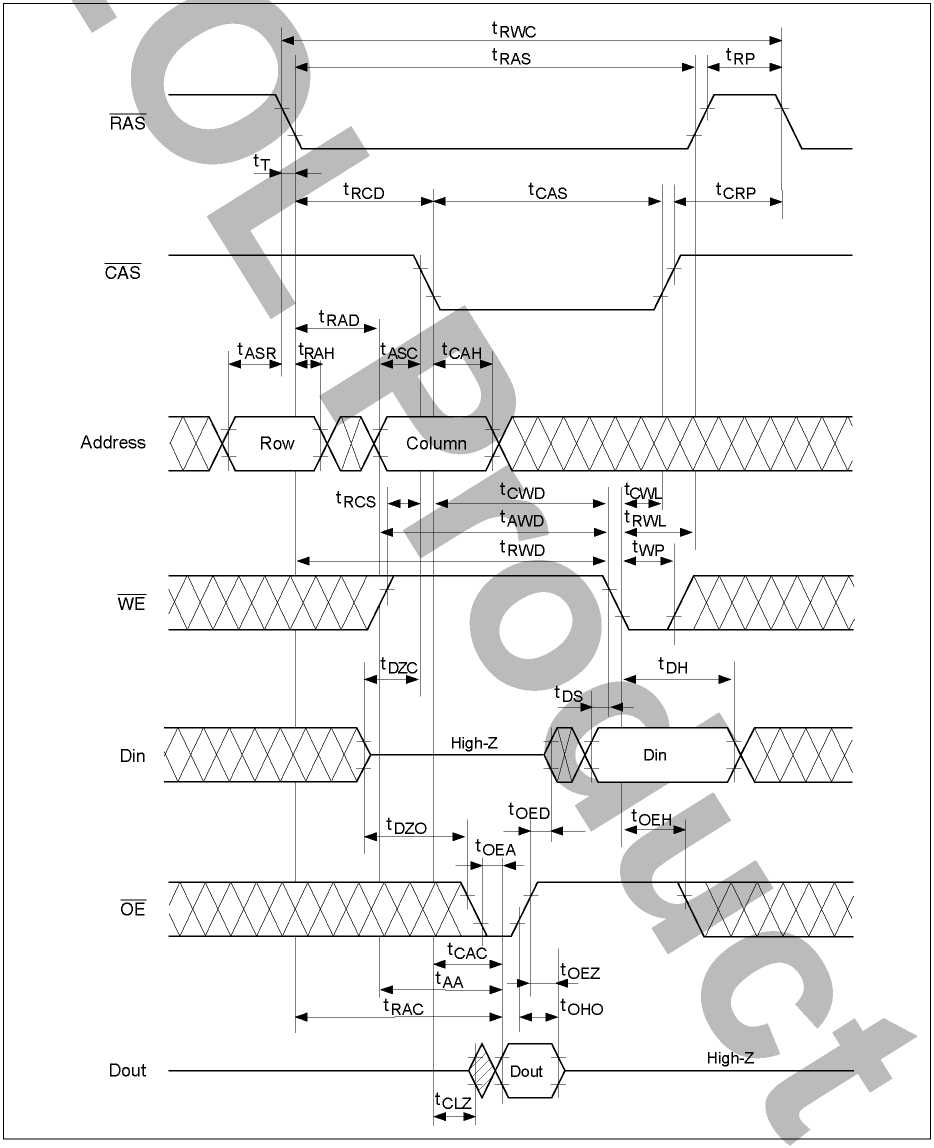
Data Sheet E0156H10 ***ELPIDA***

16



**HM5117805 Series**

**Read-Modify-Write Cycle**\*18

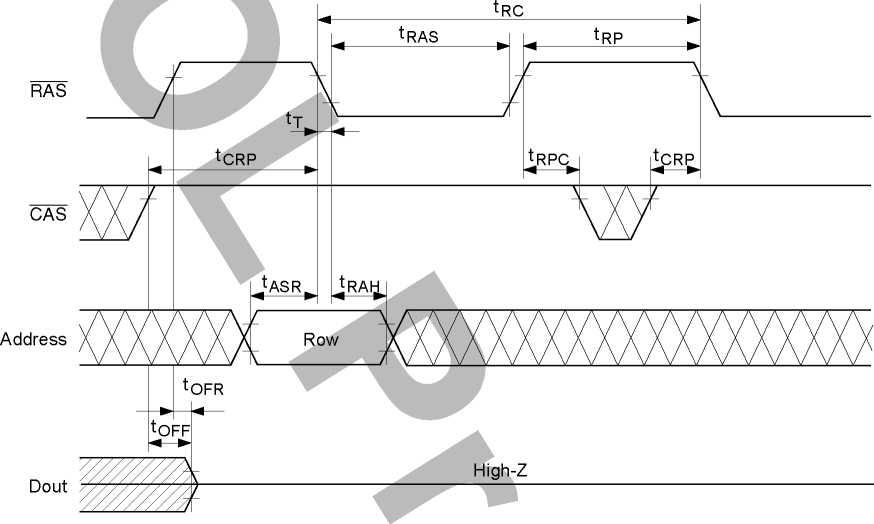


Data Sheet E0156H10 ***ELPIDA***

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**HM5117805 Series**

RAS-Only Refresh Cycle





Data Sheet E0156H10 ***ELPIDA***

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**HM5117805 Series**

CAS-Before-RAS Refresh Cycle

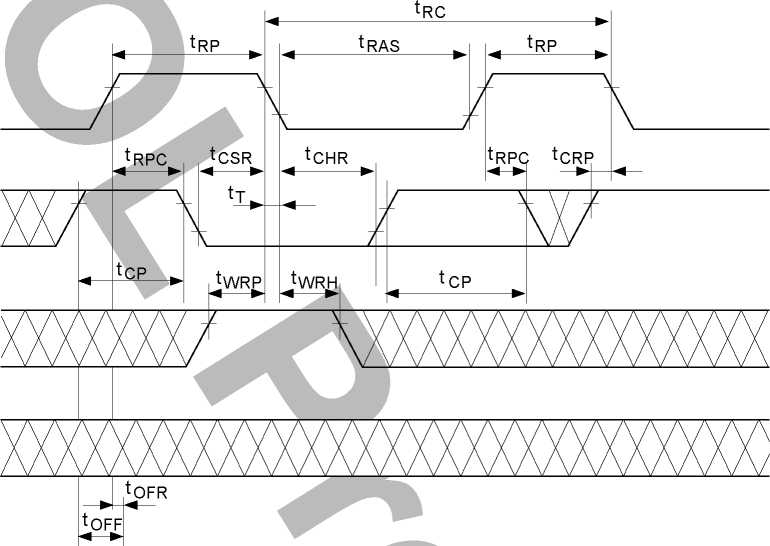
Dout

RAS

CAS

WE

Address



High-Z

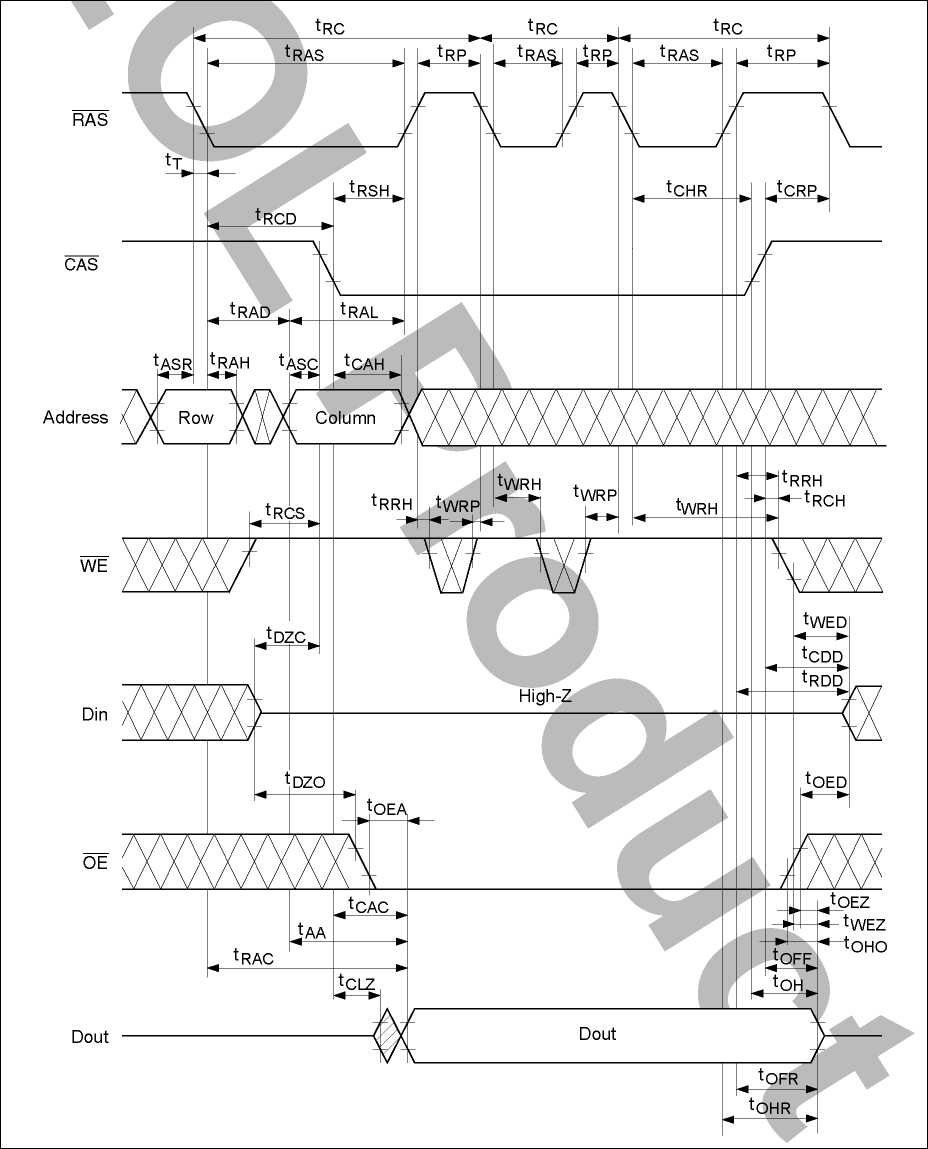


Data Sheet E0156H10 ***ELPIDA***

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**HM5117805 Series**

**Hidden Refresh Cycle**

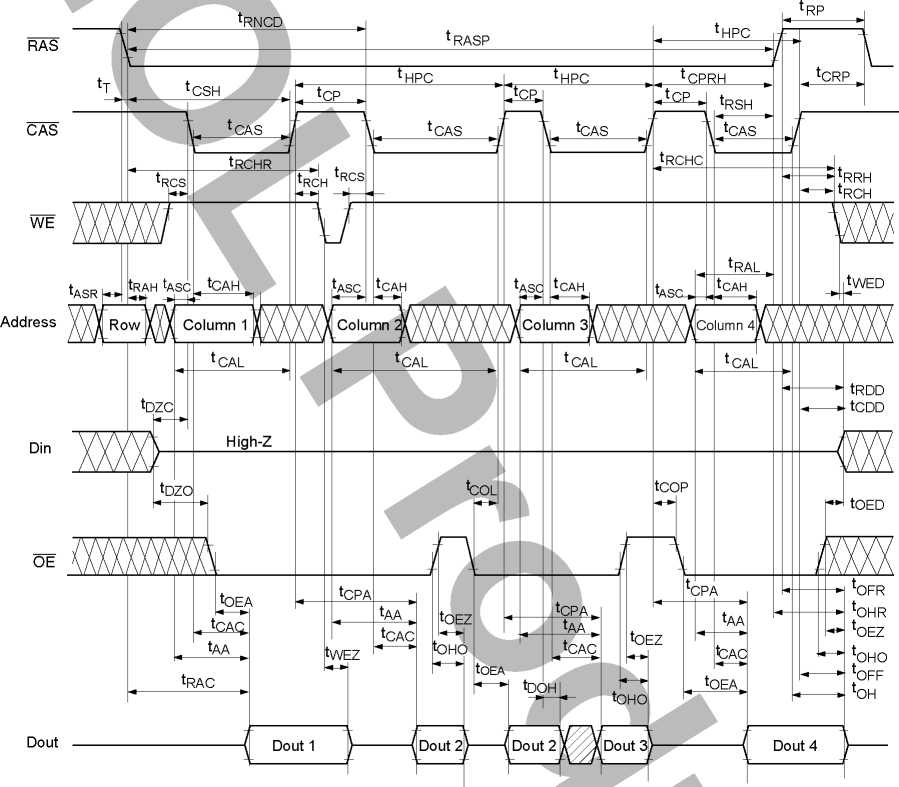


Data Sheet E0156H10 ***ELPIDA***

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**HM5117805 Series**

EDO Page Mode Read Cycle



"b

Data Sheet E0156H10 ***ELPIDA***

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**HM5117805 Series**

EDO Page Mode Early Write Cycle

RAS

CAS

tRASP

tRP

tCP

RSH  
tCAS

tCSH

tRCD \_

tHPC

I I tCAS

tCAS

tCP

tCRP

tRAH

tASR

tASC

tCAH

tASC

tCAH

tCAH

tASC

Address

Row

Column 1

Column 2

Column N

tWCH

tWCH

tWCS

tWCS

tWCS

tWCH



tDS

tDH

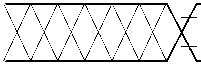
tDS

tDH

tDS

tDH

Din



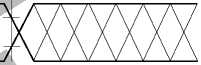
Din 1



Din 2



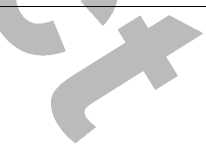
Din N



Dout

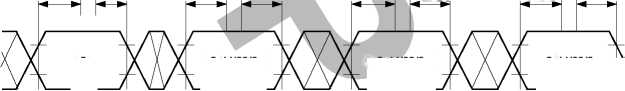
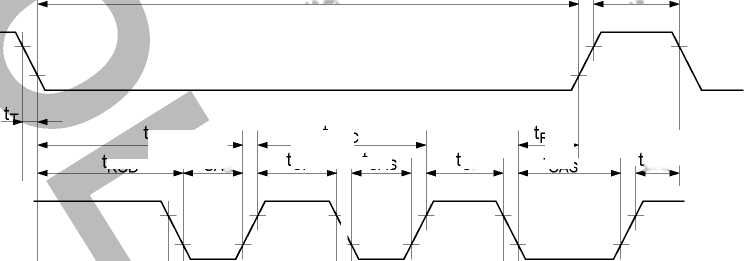
High-Z

\* tWCStWCs(min)



Data Sheet E0156H10 ***ELPIDA***

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**HM5117805 Series**

EDO Page Mode Delayed Write Cycle\*18

tRASP

RAS

CAS

tASR,

Column 1

Address

tCWL

tCWL

tRCS

WE

Din

Dout

tASC JCAH

tCRP

tRCD

tCWL

in

tDZO

tOED

tOED

tCLZ

,tOEZ

High-Z

Invalid Dout

Invalid Dout

Invalid Dout

tRSH  
tCAS

tCLZ

tOEZ

tCLZ  
,tOEZ

in

2

in

N

tCSH

tCAS

tHPC

tCAS

tRAD

tRAH

Row

tRCS

tWP

tDZC tDS

tRCS

tDH

tDZO

tDZO

tASC

tCAH

Column 2

tWP

tDZCtDS



tD

tASC

tCAH

Column N

tWP

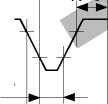
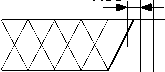
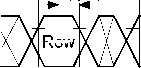
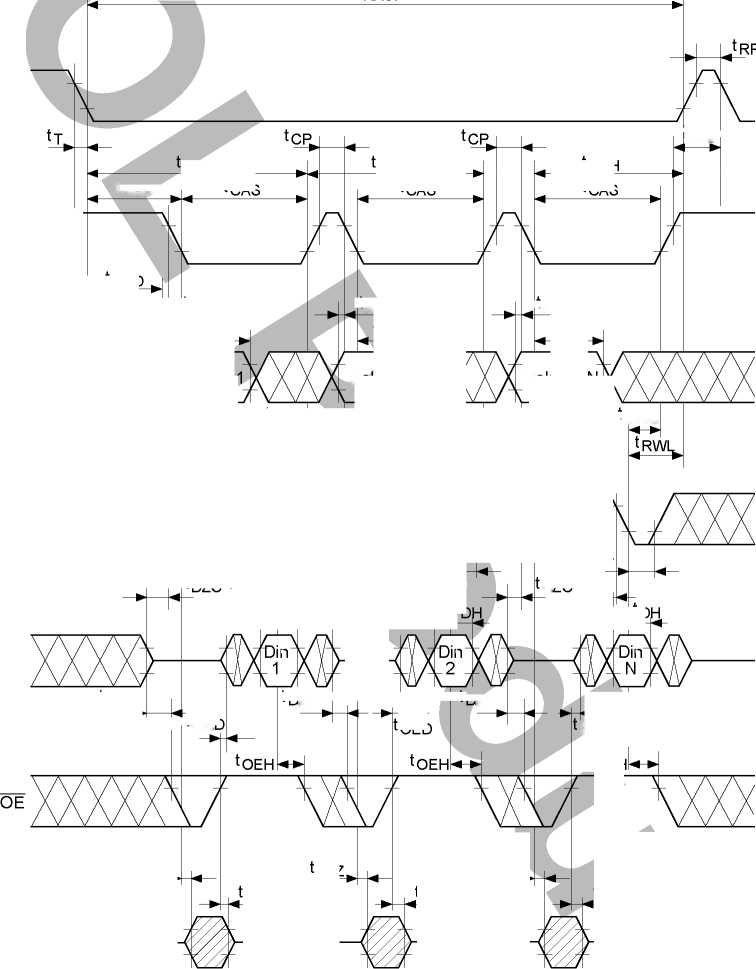
tDZC tDS

OED

tD

Data Sheet E0156H10 ***ELPIDA***

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**HM5117805 Series**

EDO Page Mode Read-Modify-Write Cycle\*18

tRASP

RAS

CAS

tCP

tCRP

tRCD

tCAS

tCAS

tCAS

tASR,

tASC  
tCAH

tASC  
tCAH

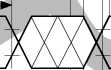
tHPRWC  
tCP

tRSH

tRAD

\_ tASC  
tRAH

Row



tCWL



tCWL

tCAH

Column 1

Column 2

Column N

Address

tRWD

tCPW

tCPW

tRCS

tRCS

WE

Din

Dout

tWP  
tDZC t DS

tAWD  
tCWD

tAWD  
tCWD

tAWD

tCWD

tDH

tDH

tDZO

tOEA

\*OEZ

tOEZ

tCLZ

tCLZ

High-Z

tAA  
tCPA-<

tOEA

tcAc-«->

\*Aa|^—

tCPA-<

tCWL

tRWL

tRCS,

tOED

tDZO

tWP

tDZC tDS

tWP

tDZC t DS^

tOED

tDH

tDZO

tOED

tOEA  
tCAQ«-\*-

tAA^

tRAC

tCLZ

tOEZ

Dout 1

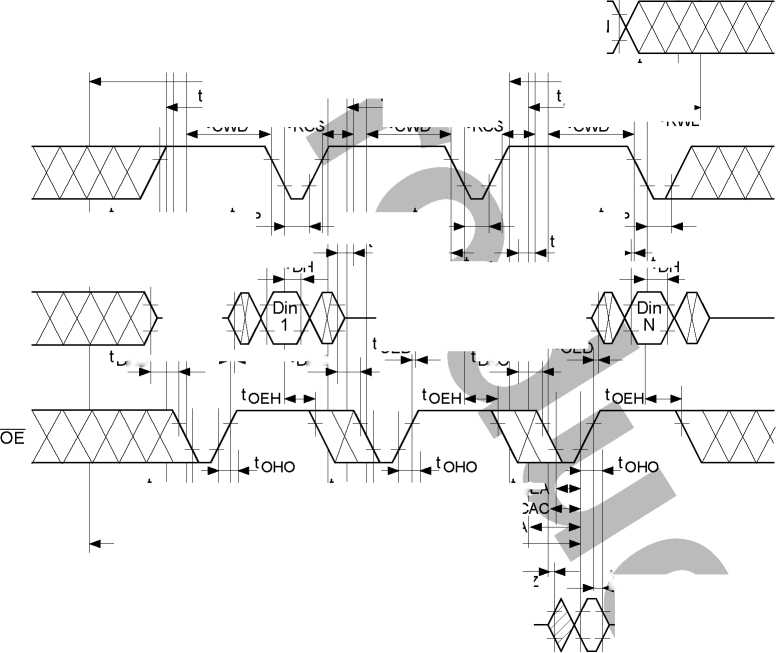
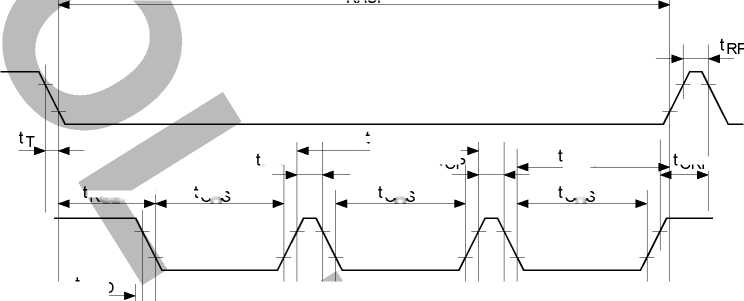


Dout 2

Dout N

Data Sheet E0156H10 ***ELPIDA***

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**HM5117805 Series**

EDO Page Mode Mix Cycle (1)

RAS

CAS

WE

tCAS

t RASP

tCP

tRCS

tRCS

tASC

tRCD

tWCS

tCAS

tRSH

tCAS

tCSH

tWCH |„



Address

Din

Dout

OE

tASC

tCAH

tCAH

tCAL

tDH

tCAL

tDS

*t* tDH

Din 1

tCAH

tDS

tOED

tCPA

tAA

tOEZ

tOHO

tRAL

tCAH

tCRP



tRRH  
tRCH



- I tASC tCAH tASC tCAH tAScU ICAHj

Colum-'^^^^^ XColu^^^^''^^ ^3Coium"^^ XCoh^^""n^4X'''''/'

tCAL

High-Z

tCPA tAA \* tOEA

tCAC



tDOH

Dout 2

tCAC



tRDD

tCDD

tCAL

tCAC

’”1 tWED

WED

tCPA

tAA

\* F

tOEA

tOFR  
tWEZ

tOEZ

tOHO

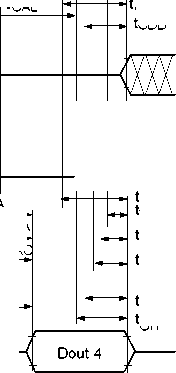
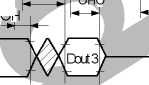
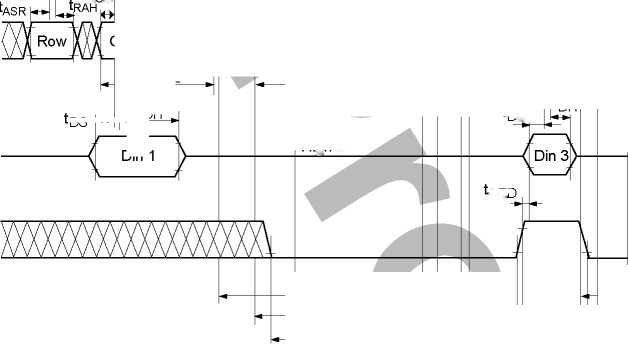
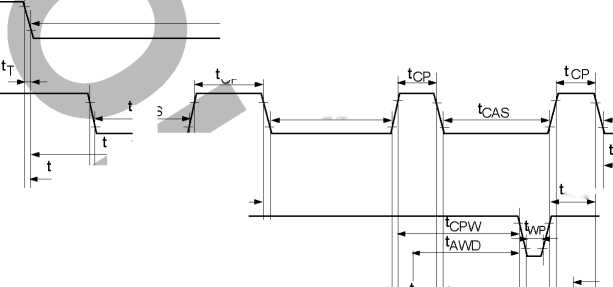
tOFF

tOH

"b

Data Sheet E0156H10 ***ELPIDA***

25



**HM5117805 Series**

EDO Page Mode Mix Cycle (2)

RAS

CAS

WE

tRNCD

t RASP

tCAS

tRCS

tASC

tCAH

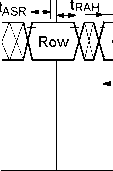
tCSH

V tCAS  
tRCD

Address

Din

tASC



Column 1

Dout

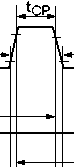
tRCHR

tRCH

tWCS

tWCH

tRCS



tCAS

tCPW

tASC

tCP

tRCS

JWp

tCAS

tRSH

tRAL

tRP

tCRP

tRRH  
tRCH





tCAH

Column 2

tCAH

U.SC

Column^xxxXx

tCAH

CoiU™wXXXXW

OE

tCAL

tCAL

tCAL

tDS

tDH

High-Z

tCOP

tDH

tOED

tOED

tOEA

lCPA

tCPA

tAA

tOEZ

tOEZ

tCAC

tRAC

tOHO

tOHO

tAA \_

[tCAC  
JOEA

AA

tOEA

tCAC ’

tCAL

tRDD

tCDD

H tWED



Dout 4

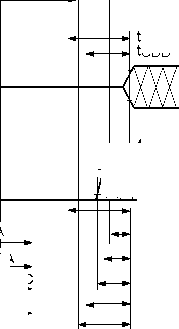
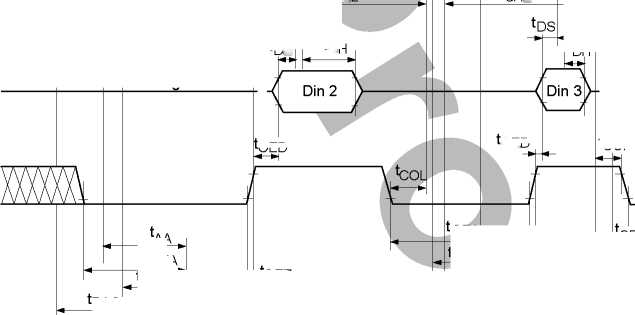
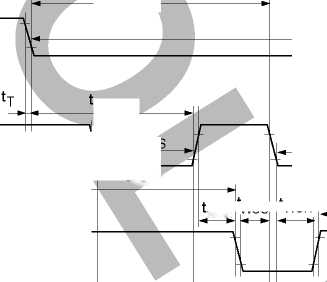
tOFR twEZ tOEZ tOHO tOFF tOH



o

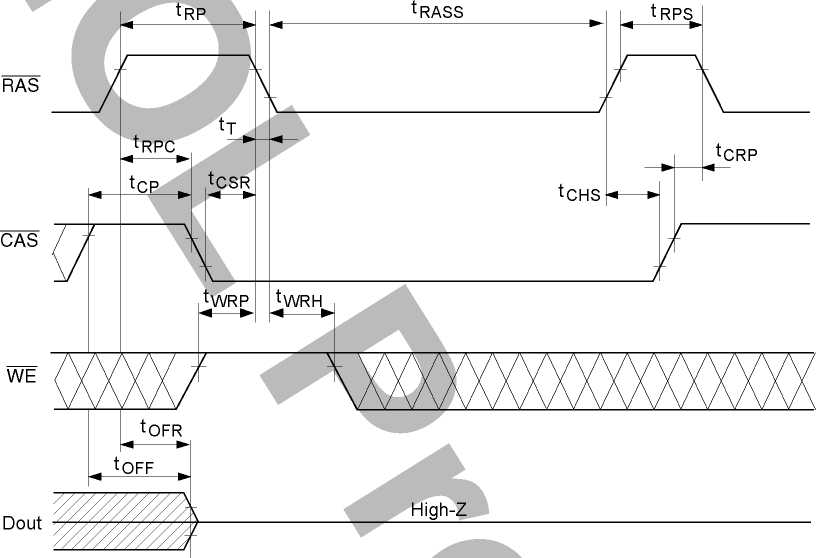
Data Sheet E0156H10 ***ELPIDA***

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**HM5117805 Series**

**Self Refresh Cycle** (L-version) \*21, 22, 23, 24





Data Sheet E0156H10 ***ELPIDA***

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**HM5117805 Series**

Package Dimensions

**HM5117805J/LJ Series** (CP-28DA)

Unit: mm

18.17

18.54 Max

0.74

1.27

9.40 ± 0.25

0.43 ± 0.10

0.41 ± 0.08

Hitachi Code

JEDEC

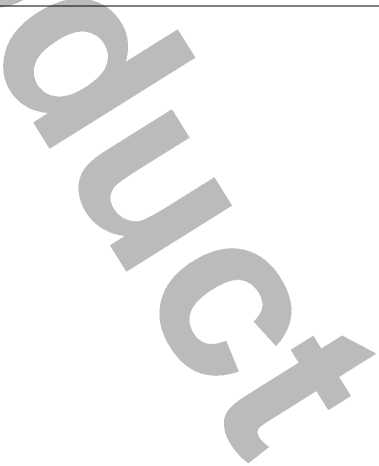
EIAJ

Weight (reference value)

1.30 Max

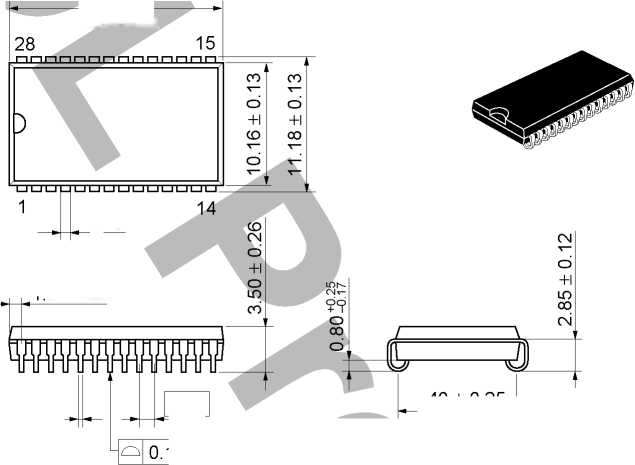
Dimension including the plating thickness  
Base material dimension

CP-28DA Conforms Conforms 1.16 g



Data Sheet E0156H10 ***ELPIDA***

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**HM5117805 Series**

**HM5117805S/LS Series** (CP-28DNA)

Unit: mm

28

18.41 .

18.84 Max ’

15

14

6.79 ± 0.18

1.27 |

LN0.10

0.43 ± 0.10

0.41 ± 0.08

0.74

1.165 Max

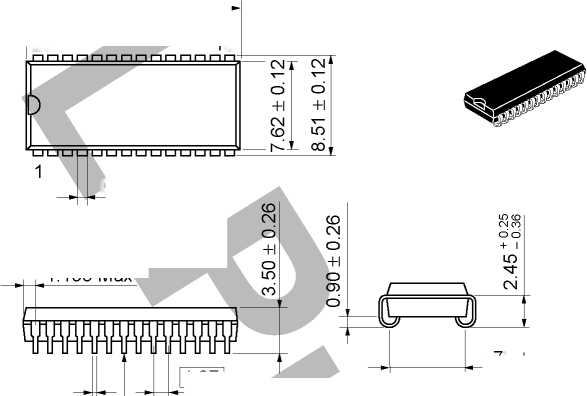
Dimension including the plating thickness  
Base material dimension

|  |  |
| --- | --- |
| Hitachi Code | CP-28DNA |
| JEDEC | — |
| EIAJ | — |
| Weight (reference value) | 0.95 g |



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**HM5117805 Series**

**HM5117805TT/LTT Series** (TTP-28DA)

Unit: mm

**innr**

0.21 (Ml

1.15 Max

il

0.42 ± 0.08

0.40 ± 0.06

18.41

18.81 Max

28 15

nnnnnnnnnnnnnn

.76 ± 0.20

0.10

CM

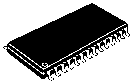
Dimension including the plating thickness  
Base material dimension

o  
IT

1

u u u u u u u

J1.27 | 14



0° - 5°

0.50 ± 0.10

0.80

Hitachi Code

JEDEC

EIAJ

Weight (reference value)

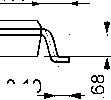
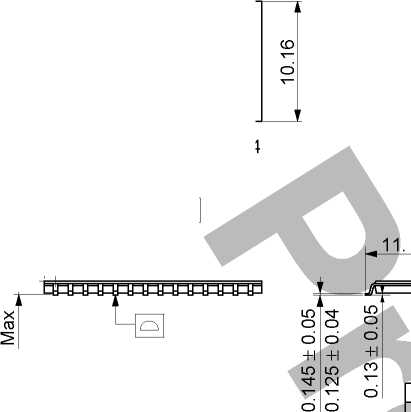
TTP-28DA Conforms

0.43 g



Data Sheet E0156H10 ***ELPIDA***

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**HM5117805 Series**

**HM5117805TS/LTS Series** (TTP-28DB)

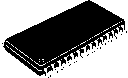
Unit: mm

18.41

" 18.81 Max -

28 15

n n n n n n n n n n n n n n



0° - 5°

0.42 ± 0.08

0.40 ± 0.06'

9.22 ± 0.2

Dimension including the plating thickness  
Base material dimension

^H0|O.21(M)

1.15 Max

0.80

0.50 ± 0.10

Hitachi Code TTP-28DB

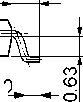
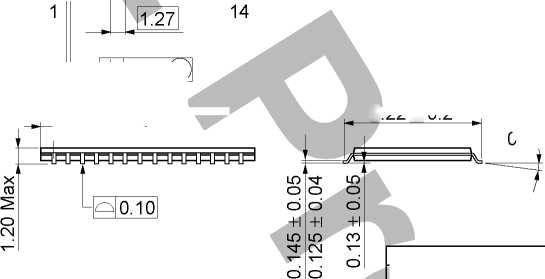
JEEIADJEC ——

Weight (reference value) 0.35 g



Data Sheet E0156H10 ***ELPIDA***

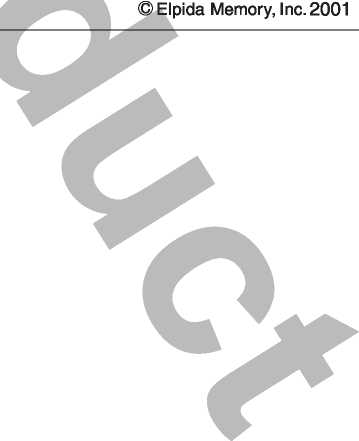
31



**HM5117805 Series**

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