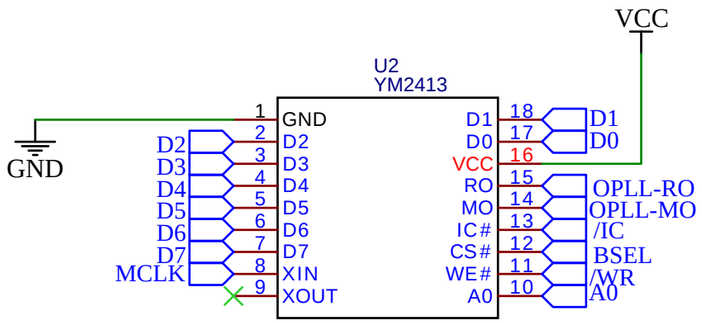
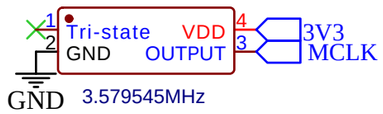
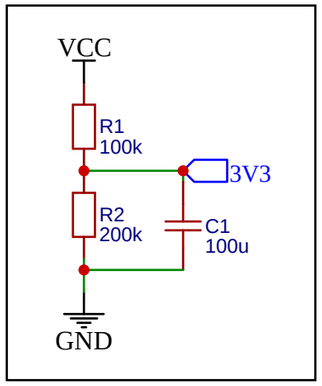
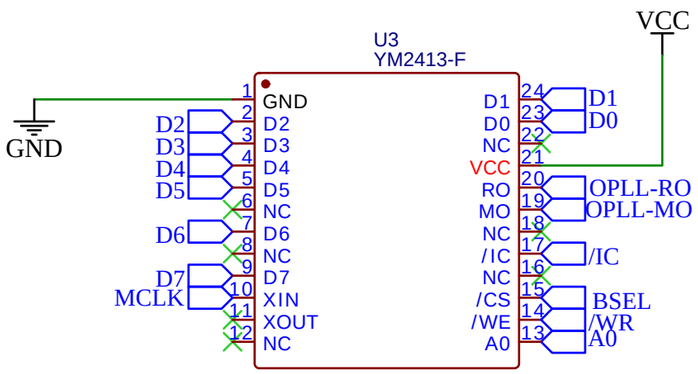


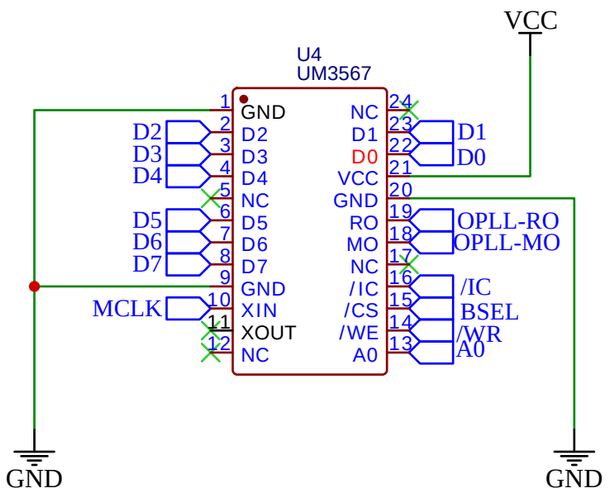
MO,RO一定不能通过数据总线路径



晶振：3225有源贴片或直插







2023.12.21 v0.1

1.差分放大电路已验证，对OPLL采取一级放大

2.Vbias过缓冲之后再使用

3.已优化3D模型

4.已添加JLC标志

5.双晶振选择：贴片或直插

6.时钟选择：主板SCK或板上晶振

2023.12.21 v0.2

1.发现某些电容封装错误

2.添加下拉电容以增加低频。

3.第二个开关连接错误

4.RO音量小

5.已精简电源滤波电容

6.添加立体声切换开关

2024.1.24 v0.2a

1.删除SCK

2.精简电容

3.添加立体声切换开关

4.添加宽立体声开关

5.添加文档

2024.9.29 v0.5

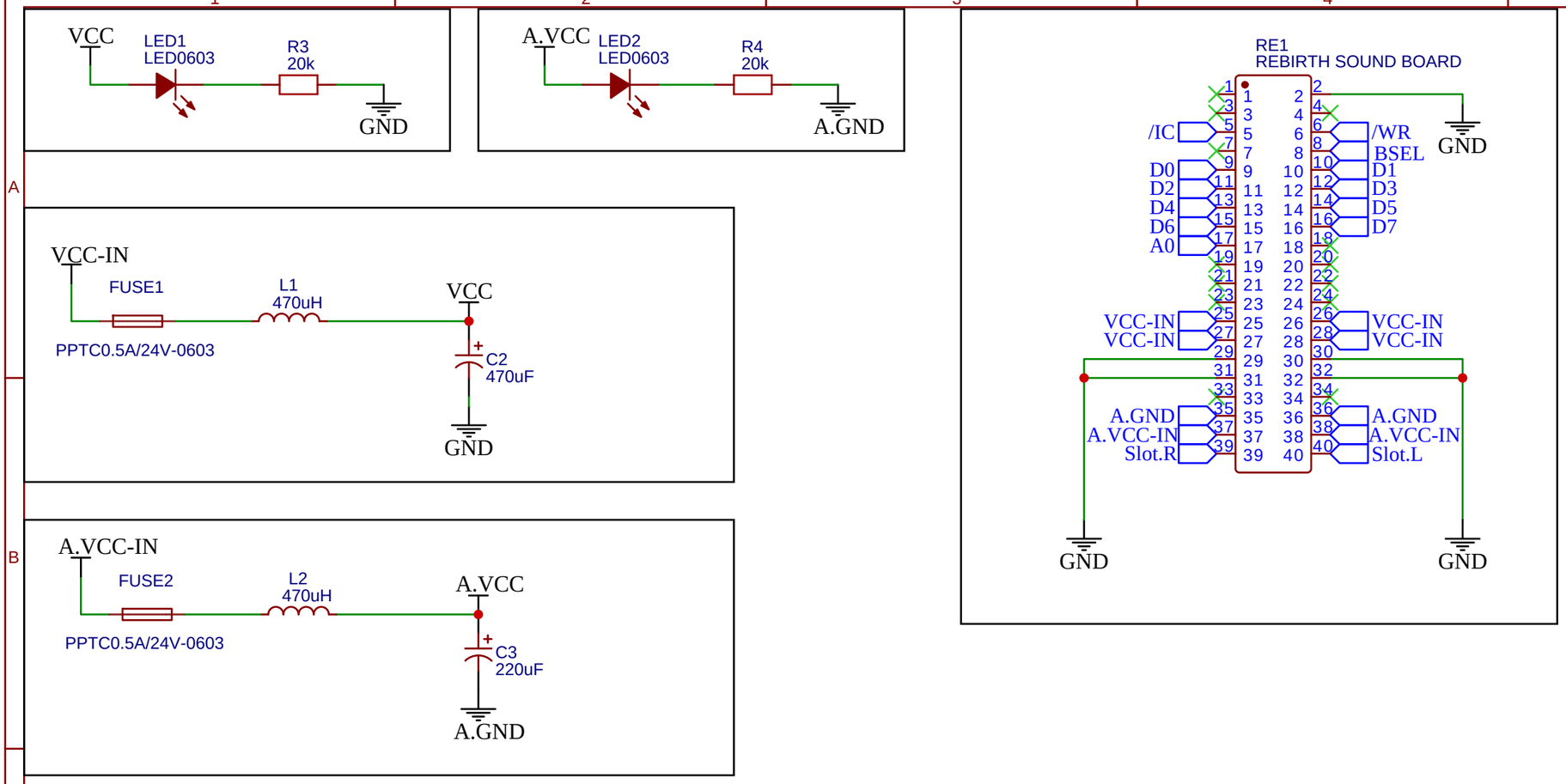
1.删除多余电容

2.删除音量减小的开关

3.删除第二个偏置电压

4.删除宽立体声选项

TITLE: Sheet_1	REV: 1.0
嘉立创EDA Company: Your Company	Sheet: 1/1
Date: 2023-12-16 Drawn By: Denjhang	



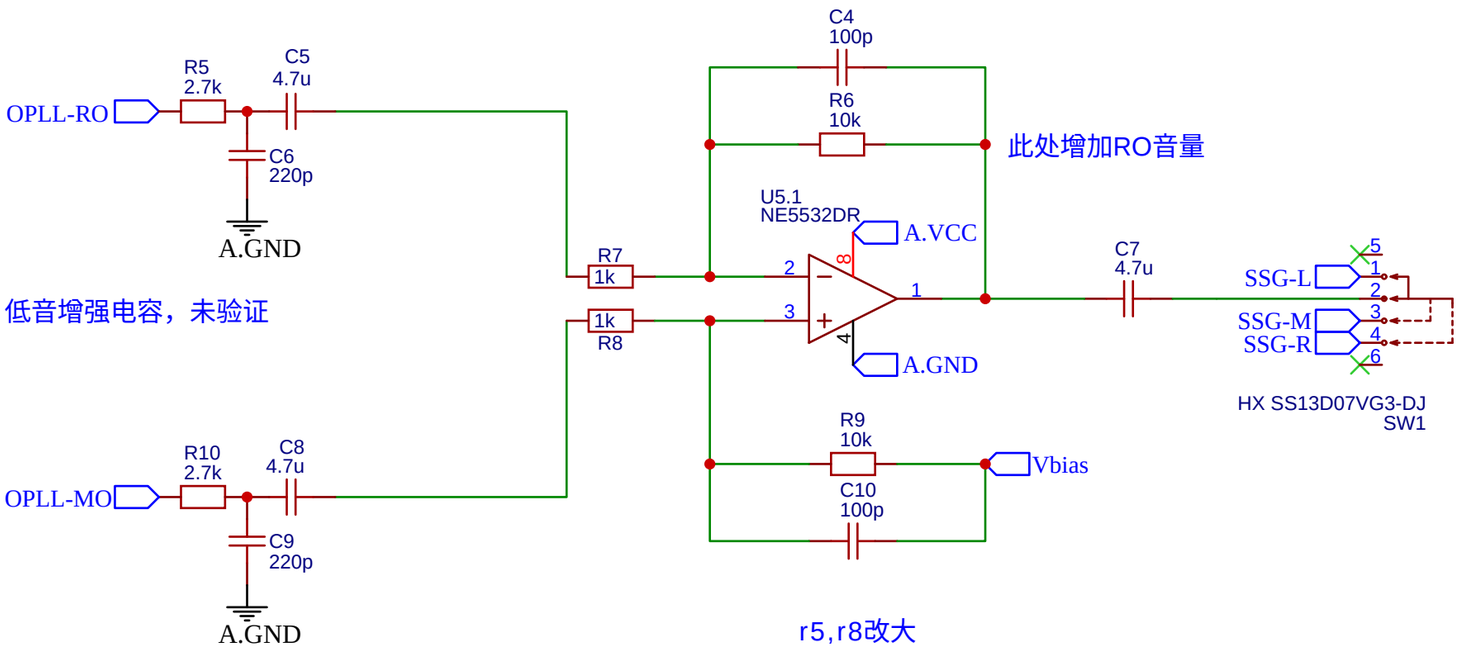
去掉二极管，那个会引起压降

TITLE: Sheet_1		REV: 1.0
嘉立创EDA	Company: Your Company	Sheet: 1/1
	Date: 2023-12-16 Drawn By: Denjhang	

此处电容减小以加强高频

此处电容不要超过0.5n

120-390p



r5,r8改大

此电路效果不错，可让YM2413产生的总线噪音大部分被抵消

因此可听数据量大的VGM曲目，如Bad Apple CSM人声版

面包板上的线一定要连接牢固，这样才能够有更好的降噪

对于OPLL，最好仅使用一级放大，级数越多就越多噪音

此版本唯一的缺陷是没加MO和RO的下拉电容，加了电容可以加强低频

差分放大器（减法器）电路

此处利用减法器原理，由于OPLL的MO和RO正好是共模信号

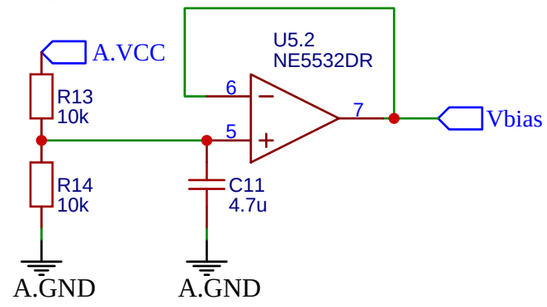
使用减法器恰好可抵消MO和RO发出的总线噪音

反馈电阻使用470k时削波，破音

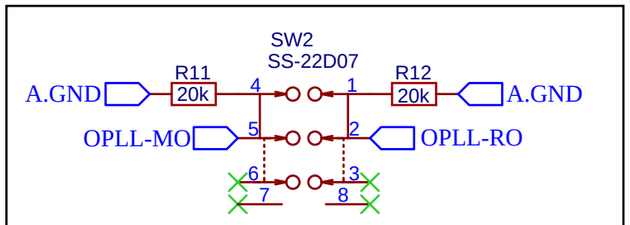
放大倍数越大，噪音越不明显

此处音量调节效果还可以

原版电路是1k



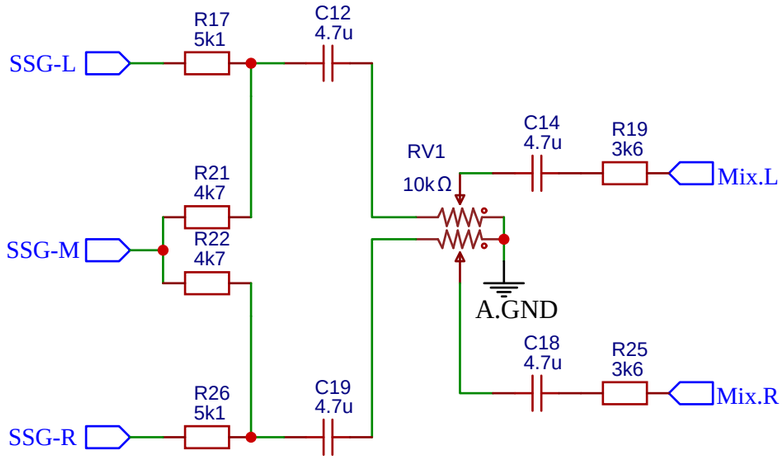
偏置电压



下拉电阻切换：1/4原装,3/6克隆

YM2413原装/克隆芯片混音电路切换

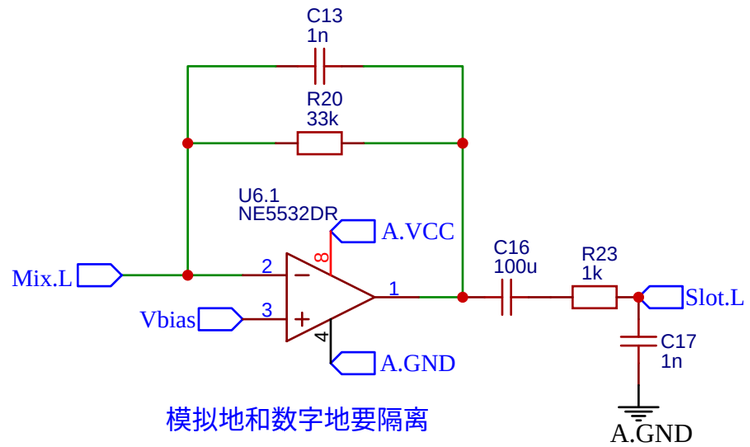
TITLE: Sheet_1	REV: 1.0
嘉立创EDA Company: Your Company	Sheet: 1/1
Date: 2023-12-16 Drawn By: Denjhang	



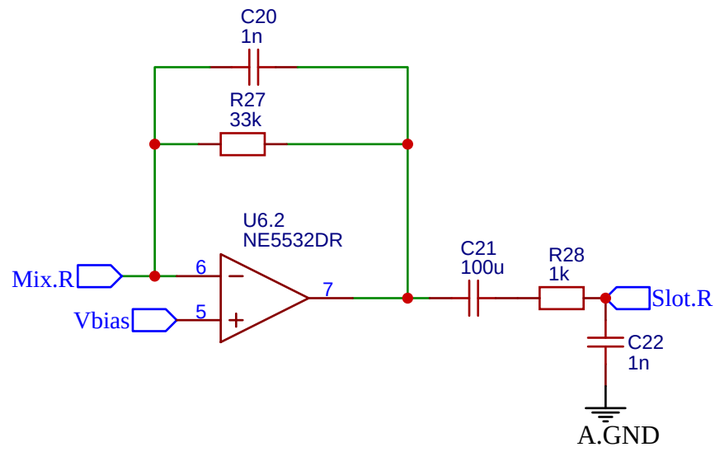
可能都用4k7

加电位器之后必须加电容

R16,R22填上导线



模拟地和数字地要隔离



TITLE: Sheet_1		REV: 1.0
嘉立创EDA	Company: Your Company	Sheet: 1/1
	Date: 2024-01-24 Drawn By: Denjhang	