YAMAHA *L 3 i*

YACS12

2-Channel Floating D/A Converter

* OUTLINE

The YAC512 is a floating D/A converter with 10-bit mantissa and 7-step exponent.

It can produce analog output of 16-bit dynamic range.

It is suitable for YMF262 (OPL3) and other stereo sound source LSI.

* FEATURES
* 2-channel floating D/A converter.
* 16-bit dynamic range.
* 16-bit digital data is converted to floating data internally.
* Analog output is easily available by external buffer operational amplifiers.
* Built-in analog switches for sample-hold.
* Si-gate C-MOS process and accurate thin film resistor.
* 5V single power supply.
* 16-pin plastic SOP (YAC512-M).

YAMAHA CORPORATION

■ ‘I'mSSEM 00020L0 IT? ■ |

YAC512 CATALOG  
CATALOG No.: LSI-4ACS124  
1994.04

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**YAC512**

■ PIN CONFIGURATION

|  |  |  |  |
| --- | --- | --- | --- |
| vdd[2 | I O | I6 | Jcv |
| VSS [2 | 2 | I5 | JTST2 |
| vdd|2 | 3 | I4 | 2] MP |
| D'nE | 4 | I3 | 3 AOUT |
| clk[2 | 5 | I2 | 2] SWIN |
| FSEl[2 | 6 | I | | JCH2 |
| SMP2 |  | I O | 3 CHI |
| SMPI Q | 8 | 9 | TSTI |

< I 6S0P Top View >

■ PIN FUNCTION

|  |  |  |  |
| --- | --- | --- | --- |
| No. | Name | I/O | Function |
| 1 | VDD | — | + 5V power supply |
| 2 | VSS | — | Ground |
| 3 | VDD | — | + 5V power supply |
| 4 | DIN | I | Digital data input serial data |
| 5 | CLK | . I | bit clock |
| 6 | FSEL | I | Data format select CH’; offset binary, ’L’; 2’s complement) |
| 7 | SMP2 | I | Digital data input CHI latch/CH2 sample signal |
| 8 | SMPI | I | CH2 latch/CHl sample signal |
| 9 | TSTI | I | LSI test terminal (connect to VDD terminal normally) |
| 10 | CHI | OA | Analog switch CHI output |
| 11 | CH2 | OA | Analog switch CH2 output |
| 12 | SWIN | IA | Analog switch CH1/CH2 common input |
| 13 | AOUT | OA | CH1/CH2 analog output (connect to SWIN terminal via OP-AMP.) |
| 14 | MP | IA | Analog shifter reference voltage input (bias with 1/2VDD) |
| 15 | TST2 | O | LSI test terminal (disconnect normally) |
| 16 | CV | -A | DAC center voltage terminal (connect to MP terminal via OP-AMP.) |

Note) A; Analog terminal

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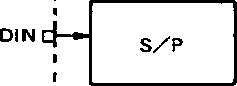
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**YAC512**

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■ BLOCK DIAGRAM

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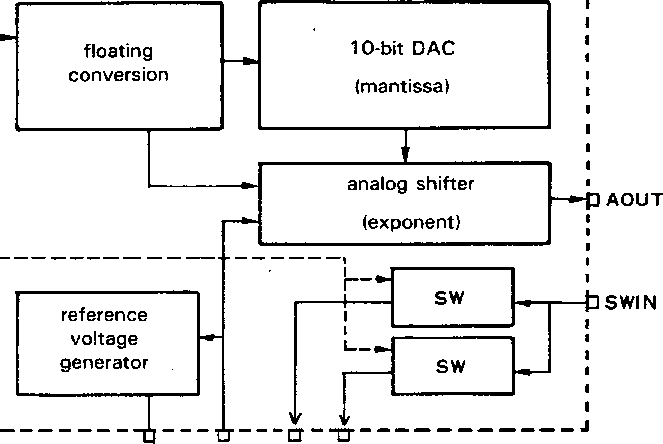


CLKQ—\*  
[ timing  
SMP I q—generator -

SMP2Q-►  
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CL — CM

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* FUNCTION DESCRIPTION

16-bit serial data synchronized with CLK clock is inputted to DIN terminal and latched when SMP1 and SMP2 fall.

Inputted data is converted to floating data and its mantissa and exponent are sent to 10-bit DAC and 7-step analog shifter respectively.

D/A voltage determined by this floating data is outputted from AOUT terminal and inputted to SWIN terminal via buffer operational amplifier for sample-hold.

Built-in CHI (CH2) analog switch is ON when SMP1-’H’ (SMP2=’H’) and analog signals are outputted to CHI and CH2 terminal.

CHI (CH2) output voltage is held with external capacitor connected to CHI (CH2) terminal when SMP1 =’L’ (SMP2=’L’).

CV terminal voltage is 1/2VDD determined by internal resistors.

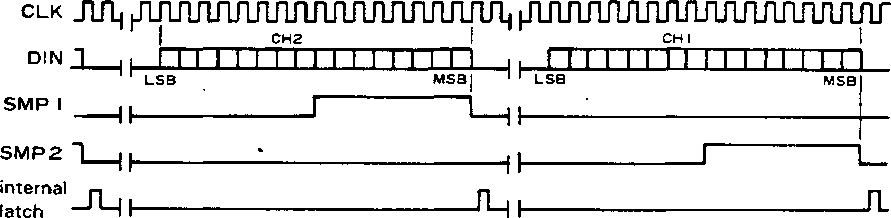
Put 10/zF external capacitor for stabilizing and connect CV to MP terminal via operational amplifier.

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**YAC512**

* INPUT FORMAT



AOUT

CHI Analog output

CH2 Analog outpuF

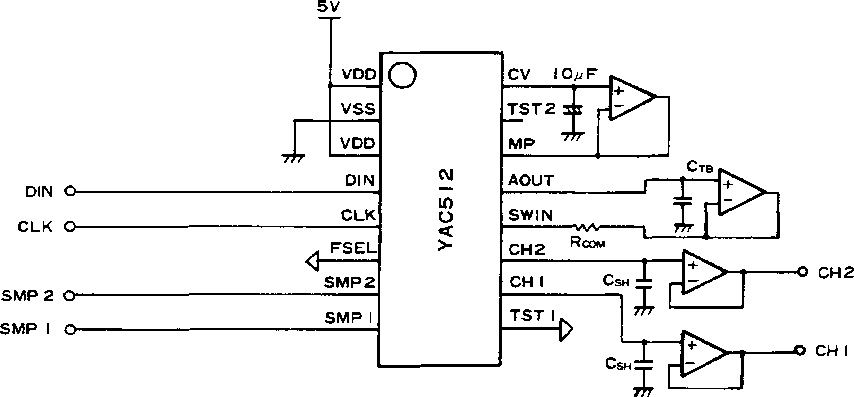




sampling ———|

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■ SAMPLE CIRCUIT



• Recommended conditions

1. Use regulated and low output impedance power supply such as 78 x05 series regulator.
2. NJM4560, NJM2100 and compatible buffer OP-AMPs are recommended.

offset: within ±2.0mV

through rate: 4V7*p* s or more

1. Recommended circuit values

CSH=2700pF (sample-hold capacitor)

CTB=33~68pF

RCOM=33Q

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**YAC512**

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■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

|  |  |  |  |
| --- | --- | --- | --- |
| Parameter | Symbol | Rating | Unit |
| Power supply voltage | Vdd | -0.3-7.0 | V |
| Input voltage | Vi | — 0.3 — VDD4-0.3 | V |
| Operating voltage | Top | 0-70 | °C |
| Storing temperature | Tstg | -50-125 | °C |

2. Recommended Operating Conditions

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Parameter | Symbol | Min. | Typ. | Max. | Unit |
| Power supply voltage | Vdd | 4.75 | 5.00 | 5.25 | V |
| Operating voltage | Top | 0 | 25 | 70 | °C |

3. DC Characteristics (Conditions; Ta=0-70°C, Vdd=5.0±0.25V)

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Parameter | Symbol | Condition | Min. | Typ- | Max. | Unit |
| Power consumption | W | Vdd=5.0V |  |  | 30 | mW |
| Input voltage H level | VlH | ♦1 | 0.66VDD |  |  | V |
| Input voltage L level | VlL | \*1 |  |  | 0.30VDD | V |
| Input leakage current | Ilk | \*1 |  |  | 0.001 | gA |
| Input capacitance | Ci | \*1 |  |  | 5 | PF |

\*1) Applicable to CLK, DIN, SMP1, SMP2

*4. DC* Characteristics (Conditions; Ta=0~70°C, Vdd=5.0± 0.25V)

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Parameter | Symbol | Min. | Typ. | Max. | Unit |
| CLK clock frequency | fc | 0.65 | 3.2 | 6.0 | MHz |
| H level time | tH | 100 |  |  | ns |
| rise time | tr |  |  | 30 | ns |
| fall time | tf |  |  | 30 | ns |
| DIN, SMP1, SMP2 |  |  |  |  |  |
| setup time | tDS | 50 |  |  | ns |
| transition time | tDT |  |  | 30 | ns |

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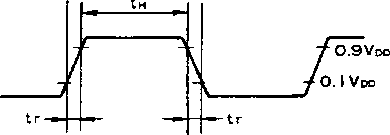
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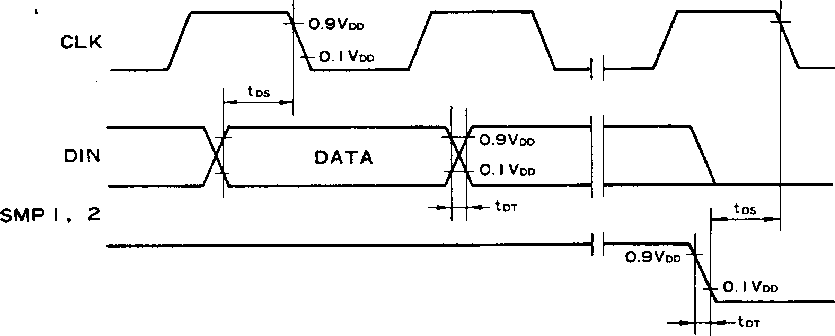
**YAC512**

• CLK timing

CLK



• DIN, SMP1, SMP2 timing



5. Analog Characteristics (Conditions; Ta=25°C, Vdd=5.0V, measured by sample circuit)

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
| Maximum output amplitude | Vo |  |  | 2.5 |  | V |
| Total harmonic distortion | THD 0 | 1 KHz, OdB |  | 0.09 | 0.18 | % |
|  | THD20 | 1 KHz, — 20dB |  | 0.07 | 0.20 | % |
|  | THD40 | 1 KHz, — 40dB |  | 0.25 | 0.65 | % |
| Dynamic range | DR |  |  | 16 |  | bit |
| Signal noise ratio | S/N | 1 KHz, OdB |  | 86 |  | dB |
| Cross talk | CT | 1 KHz, OdB |  | -72 |  | dB |

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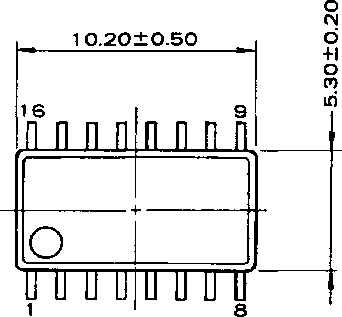
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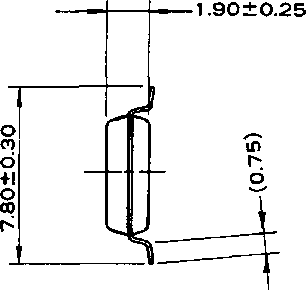
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warn

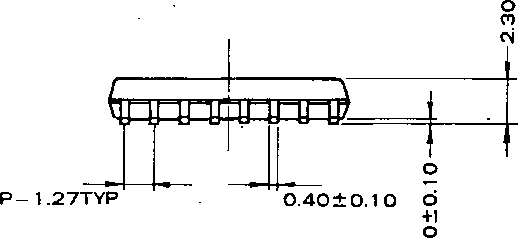
■ EXTERNAL DIMENSIONS

• YAC512-M





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UNIT: mm

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**YAC512**

The specifications of this product are subject to improvement changes without prior notice.

AGENCY

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