

A

B

C

D

A

B

C

D

vga\_r\_o[2]-IO\_T14  
vga\_r\_o[1]-IO\_T15  
vga\_r\_o[0]-IO\_R16  
dac\_r\_o-IO\_P15  
dac\_l\_o-IO\_P16  
ps2\_mouse\_clk\_io-IO\_N15  
ps2\_mouse\_data\_io-IO\_N16  
dip\_i[3]-I\_M15  
dip\_i[4]-I\_M16  
ps2\_data\_io-IO\_L15  
ps2\_clk\_io-IO\_L16  
joy1\_up\_io-IO\_P11  
joy1\_p6\_io-IO\_N11  
3V3  
GND  
joy1\_down\_io-IO\_N12  
joy1\_p7\_io-IO\_P14  
joy1\_left\_io-IO\_N14  
joy1\_p8\_io-IO\_L13  
joy1\_right\_io-IO\_K16  
esp\_tx\_i-IO\_J15  
slot\_RESET\_io-IO\_J16  
esp\_rx\_o-IO\_L14  
joy2\_up\_io-IO\_J14  
joy2\_p6\_io-IO\_K15  
joy2\_down\_io-IO\_F16  
joy2\_p7\_io-IO\_G15  
joy2\_left\_io-IO\_F15  
dip\_i[5]-I\_E16  
joy2\_p8\_io-IO\_D16  
joy2\_right\_io-IO\_D15

AC1  
AC608核心板

IO\_R14  
IO\_T13  
IO\_R13  
IO\_T12  
IO\_R12  
IO\_T11  
IO\_R11  
IO\_T10  
IO\_R10  
IO\_T9  
IO\_R9  
IO\_T8  
IO\_R8  
IO\_T7  
IO\_R7  
IO\_T6  
IO\_R6  
GND  
VDD3.3  
IO\_T5  
IO\_R5  
IO\_T4  
IO\_R4  
IO\_T3  
IO\_R3  
IO\_T2  
IO\_R1  
LVDS\_TX5\_P  
LVDS\_TX5\_N  
LVDS\_TX4\_P  
LVDS\_TX4\_N  
LVDS\_TX3\_P  
LVDS\_TX3\_N  
LVDS\_TX2\_P  
LVDS\_TX2\_N  
LVDS\_TX1\_P  
LVDS\_TX1\_N  
IO\_M10  
IO\_P9  
IO\_N9  
IO\_L8  
IO\_N8  
IO\_P8  
GND  
VDD3.3  
IO\_M8  
IO\_M7  
IO\_P6  
VDD1.2  
GND  
IO\_N6  
IO\_L7  
IO\_P3  
IO\_N5  
IO\_N3  
IO\_M6  
IO\_L4  
IO\_K5  
TDO  
VDD2.5

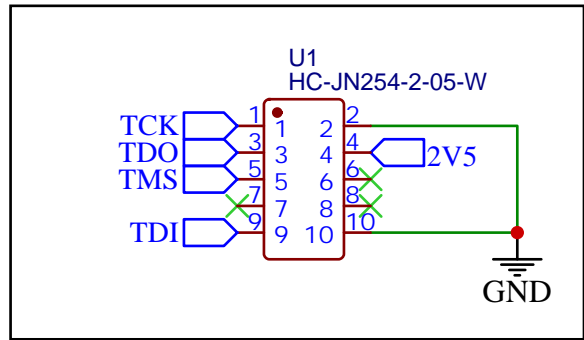
核心板共124个 Pad  
85个通用双向IO  
5对LVDS IO（也可作为双向通用IO使用）  
1对LVDS时钟输入IO  
12个时钟输入IO（不含LVDS时钟输入IO）  
5个GND（硬件连通）  
4个VDD3.3输入（硬件连通）  
1个VDD2.5输出  
1个VDD1.2输出  
4个JTAG IO  
板载50MHz有源时钟，由E15管脚输入  
板载W25Q16，16M的SPI FLASH，兼容EPCS16  
SDRAM占用的39个IO完全独立，不与邮票孔任何IO共享  
时钟输入信号，仅能作为时钟和普通信号输入，  
不能作为输出，不支持上下拉。不使用时建议接地，  
另外92和93可作为LVDS差分时钟输入  
LVDS功能管脚，如需使用LVDS管脚，需保证核心板上R9空焊，  
R8使用OR或磁珠短接。如需作为通用IO，  
则R9使用OR电阻或磁珠短接，R8空焊（此为核心板出厂默认方式）  
核心板JTAG IO。  
核心板GND，所有GND都是连通的  
电源管脚：  
VDD3.3为外部3.3V输入电源。由底板提供给核心板，  
所有VDD3.3都是连通的  
VDD2.5电压输出，可作为小功率电源输出到底板，  
如给JTAG口供电  
VDD1.2电压输出，可作为小功率电源输出到底板

IO\_C16  
IO\_C15  
IO\_B16  
IO\_J13  
IO\_G16  
IO\_F8  
IO\_F13  
IO\_F14  
IO\_F9  
IO\_E11  
IO\_E10  
IO\_A9  
IO\_B9  
IO\_C9  
IO\_A8  
IO\_D9  
IO\_B8  
VDD3.3  
GND  
IO\_E1  
IO\_B1  
IO\_C2  
IO\_D1  
IO\_F3  
IO\_F2  
IO\_F1  
IO\_G5  
IO\_G2  
IO\_G1  
TCK  
TDI  
TMS  
sd\_sw\_i-IO\_C16  
sd\_miso\_i-IO\_C15  
sd\_sclk\_o-IO\_B16  
sd\_mosi\_o-IO\_J13  
sd\_cs\_n\_o-IO\_G16  
slot\_BUSDIR\_i-IO\_F8  
slot\_SLOT3\_o-IO\_F13  
slot\_INT\_i-IO\_F14  
slot\_CS2\_o-IO\_F9  
slot\_CS1\_o-IO\_E11  
dip\_i[8]-I\_A9  
dip\_i[7]-I\_B9  
slot\_CS12\_o-IO\_C9  
dip\_i[6]-I\_A8  
slot\_SLOT2\_o-IO\_D9  
btm\_n\_i[1]-I\_B8  
3V3  
GND  
btm\_n\_i[2]-I\_E1  
slot\_REFRESH\_i-IO\_B1  
slot\_SLOT1\_o-IO\_C2  
slot\_MREQ\_o-IO\_D1  
slot\_RD\_o-IO\_F3  
slot\_MI\_o-IO\_F2  
slot\_IOREQ\_o-IO\_F1  
slot\_A\_o[9]-IO\_G5  
slot\_WR\_o-IO\_G2  
slot\_A\_o[11]-IO\_G1  
TCK  
TDI  
TMS

LVDS\_RXCLK\_P  
LVDS\_RXCLK\_N  
LVDS\_TX3\_P  
LVDS\_TX3\_N  
LVDS\_TX2\_P  
LVDS\_TX2\_N  
LVDS\_TX1\_P  
LVDS\_TX1\_N

93  
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slot\_D\_io[0]-LVDS\_TX1\_P  
slot\_WAIT\_i-LVDS\_TX1\_N  
slot\_DATA\_OE\_o-IO\_M10  
slot\_D\_io[1]-IO\_P9  
slot\_A\_o[4]-IO\_N9  
slot\_DATA\_DIR\_o-IO\_L8  
slot\_A\_o[2]-IO\_N8  
slot\_A\_o[0]-IO\_P8  
GND  
3V3  
slot\_A\_o[5]-IO\_M8  
slot\_A\_o[13]-IO\_M7  
slot\_A\_o[3]-IO\_P6  
GND  
slot\_A\_o[8]-IO\_N6  
slot\_A\_o[1]-IO\_L7  
slot\_A\_o[6]-IO\_P3  
slot\_A\_o[14]-IO\_N5  
slot\_A\_o[10]-IO\_N3  
slot\_A\_o[12]-IO\_M6  
slot\_A\_o[15]-IO\_L4  
slot\_A\_o[7]-IO\_K5  
TDO  
2V5

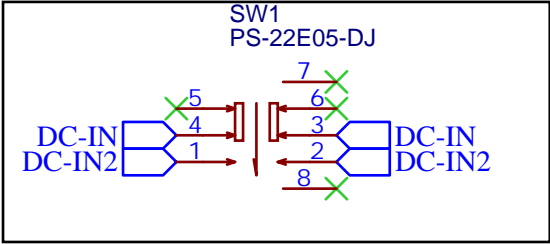
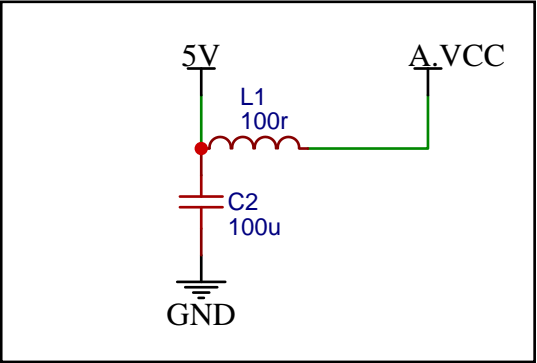
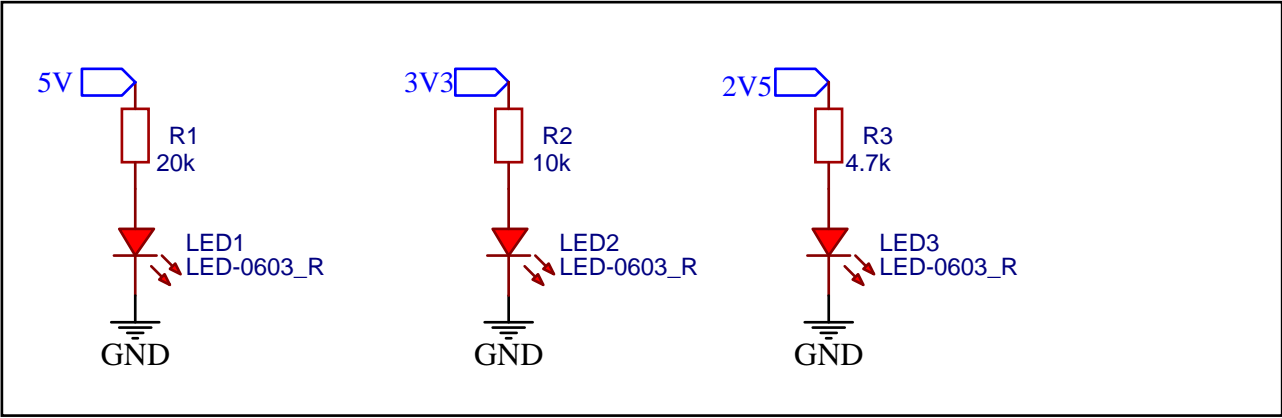
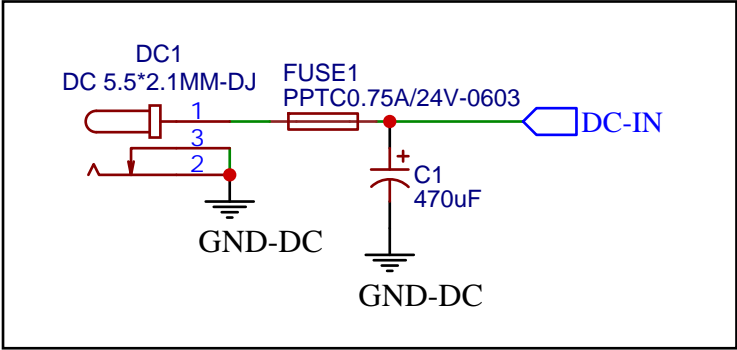
EG1  
100\*100mm 边框



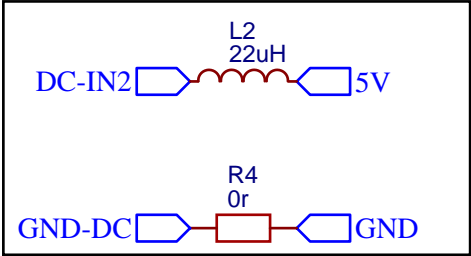
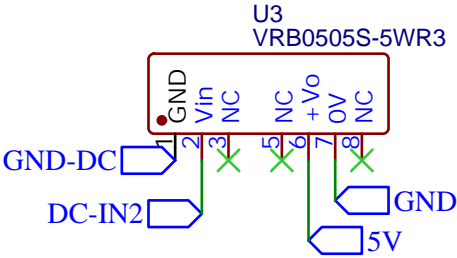
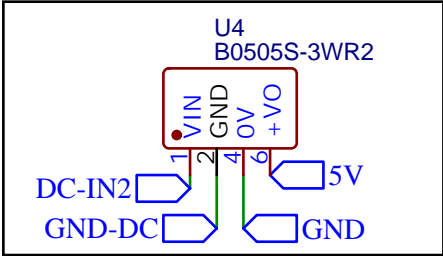
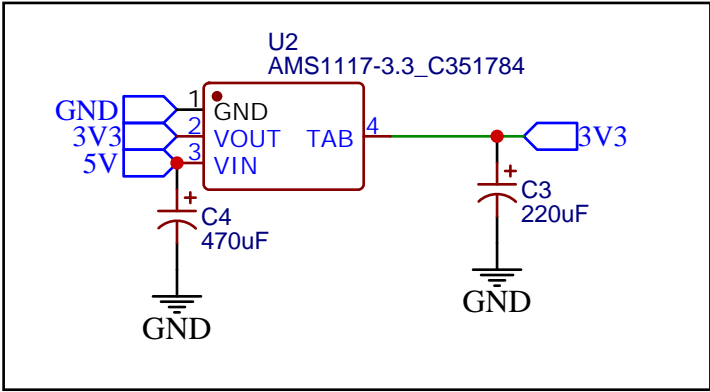
2024.3.31

- 1.改开关线路，按下开机
- 2.加核心音频直流耦合电容
- 3.修正VGA接线
- 4.添加VGA电解电容
- 5.修正短接电源模块线路

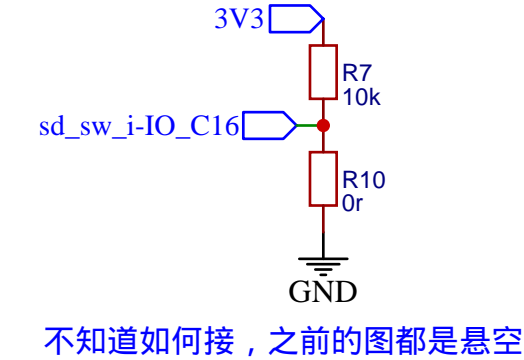
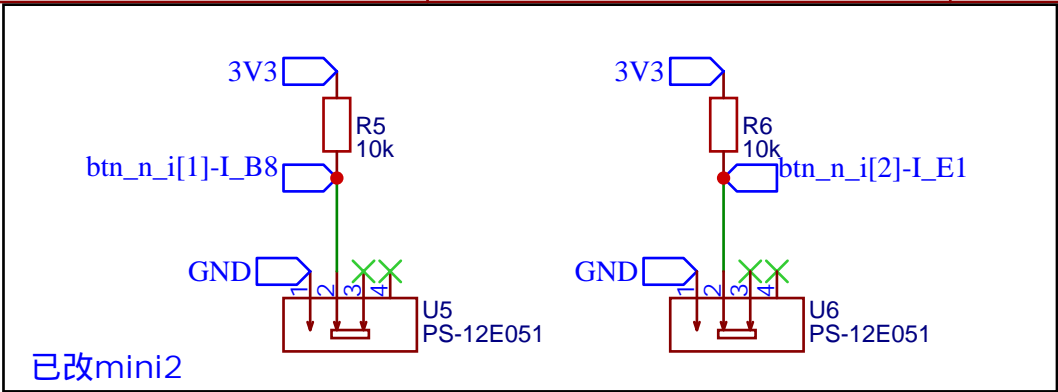
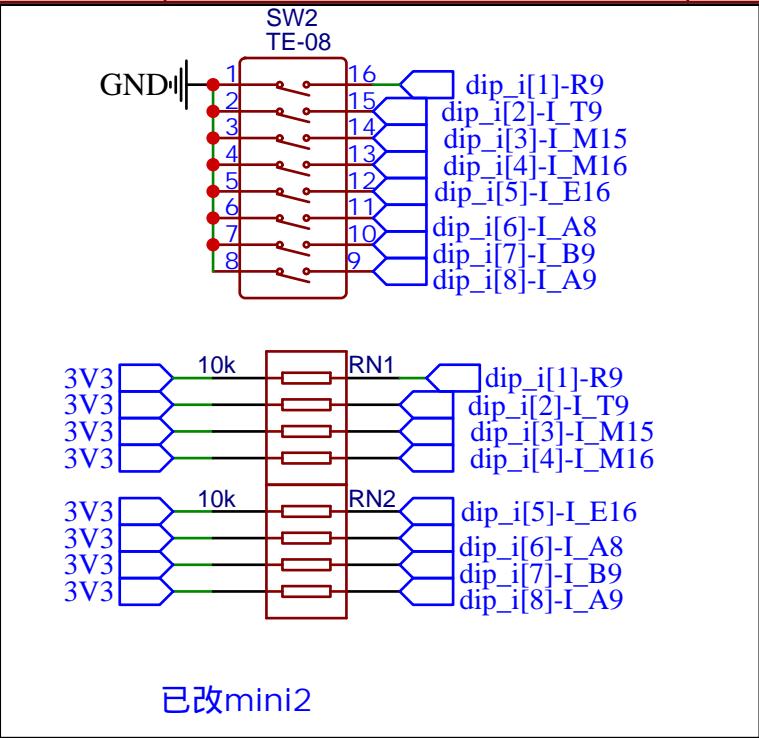
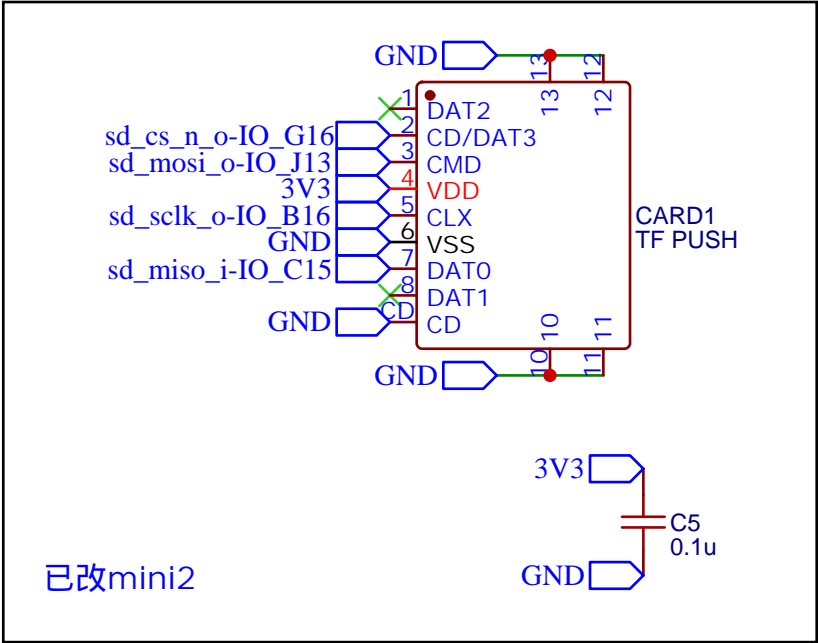
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嘉立创EDA	Company: Your Company	Sheet: 1/1
	Date: 2024-03-23	Drawn By: Denjhang



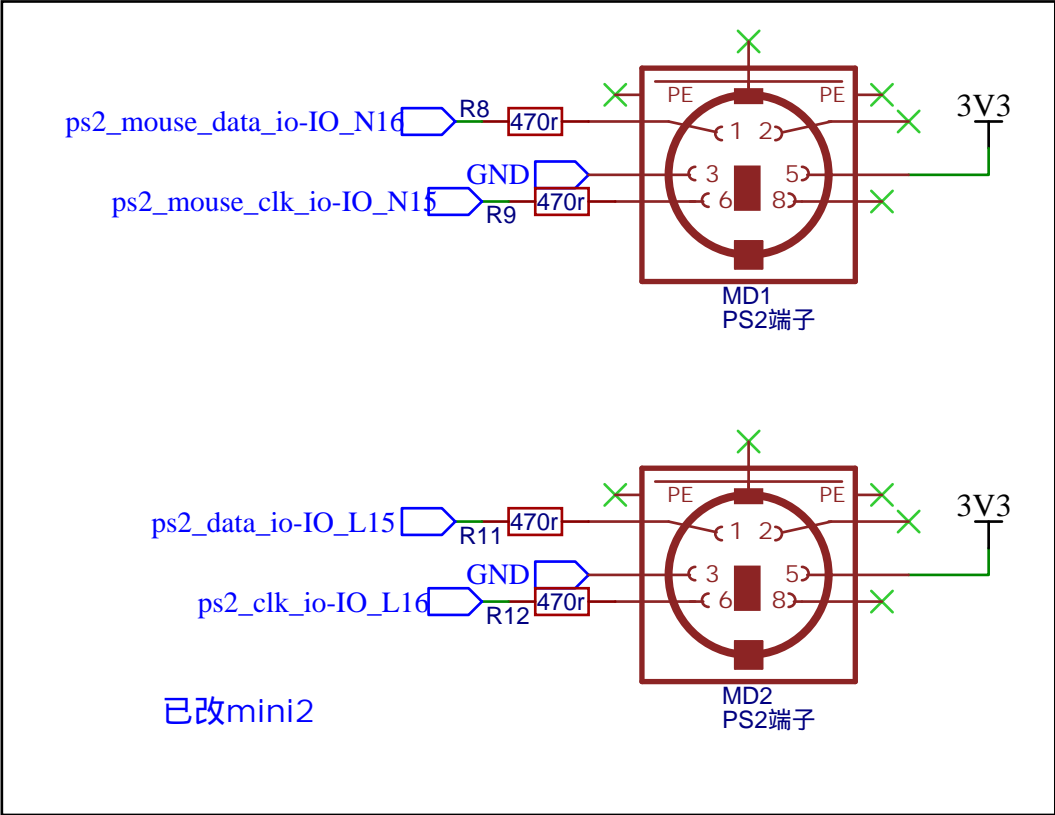
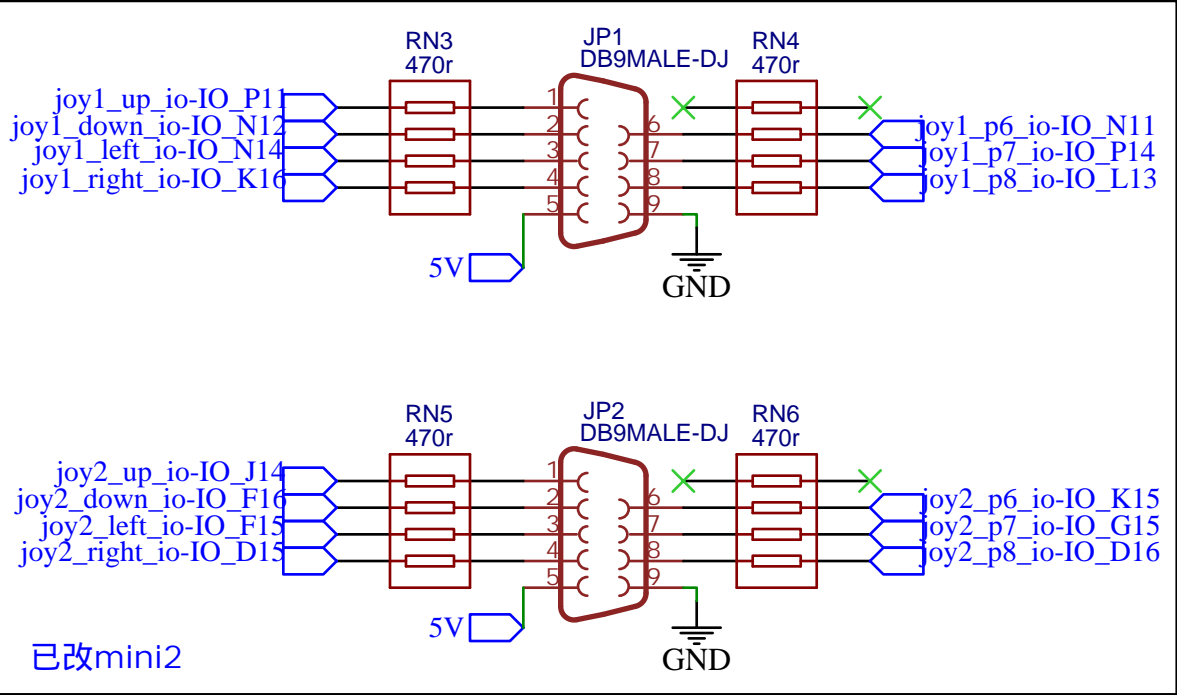
开关设计错误，符号封装错误,已修正



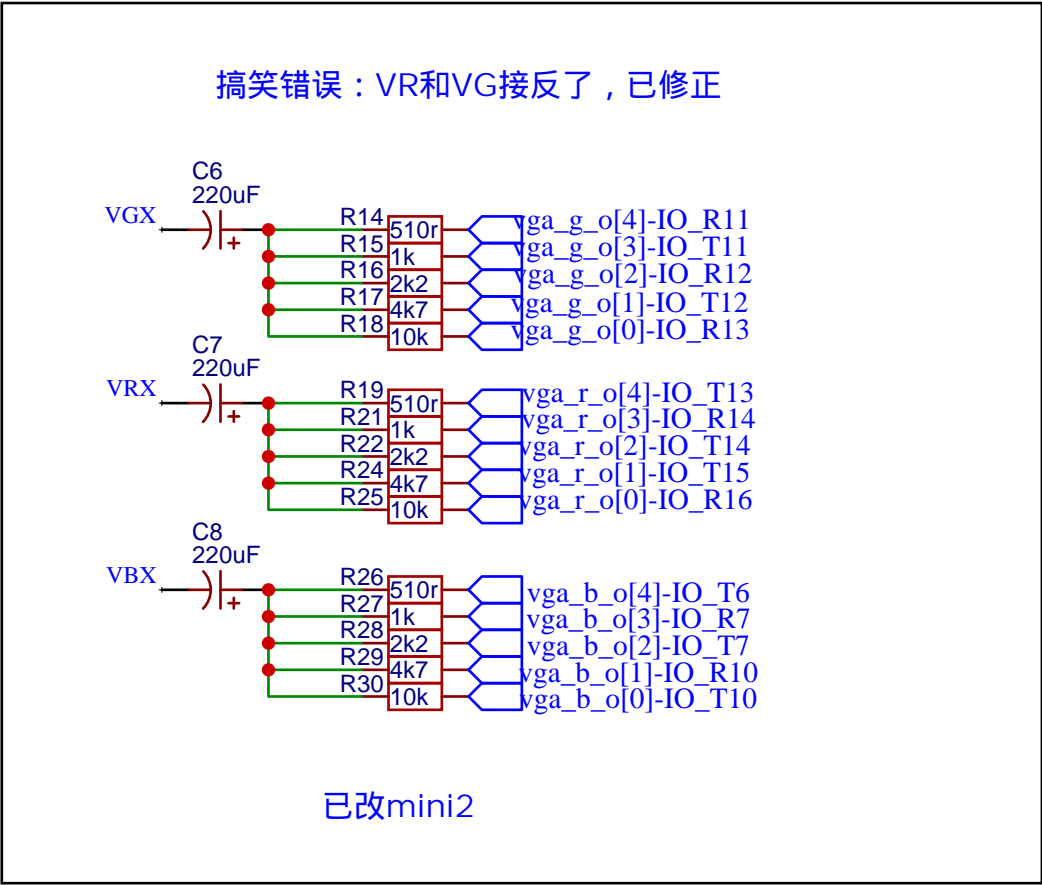
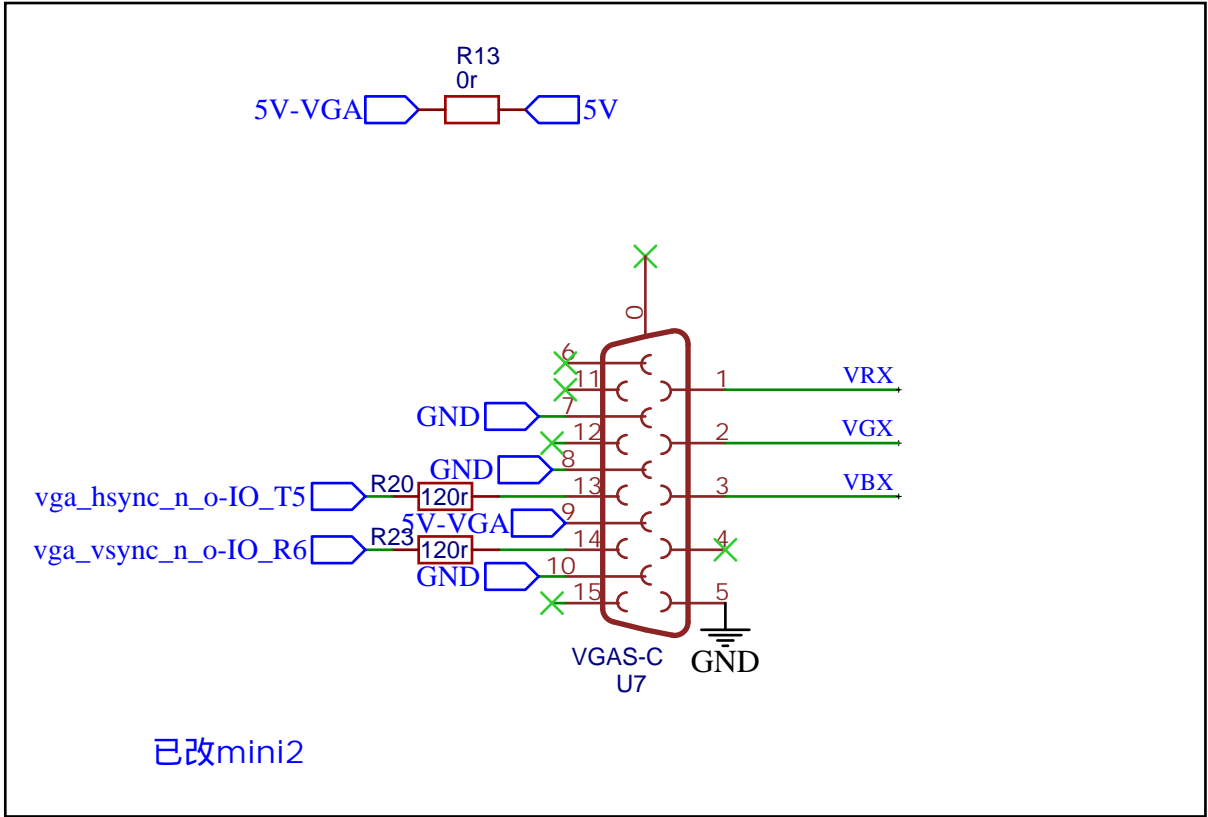
不使用隔离模块时短路原边和副边  
短接致命错误，已修正

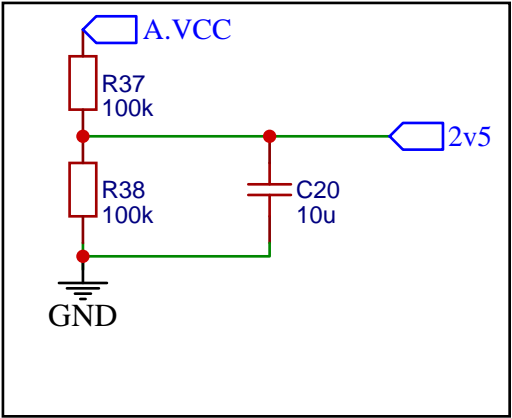
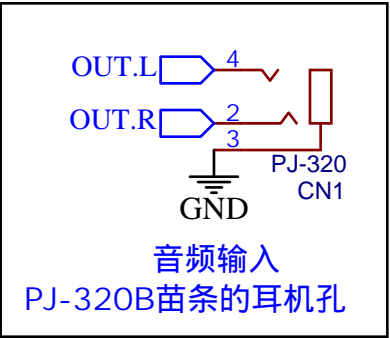
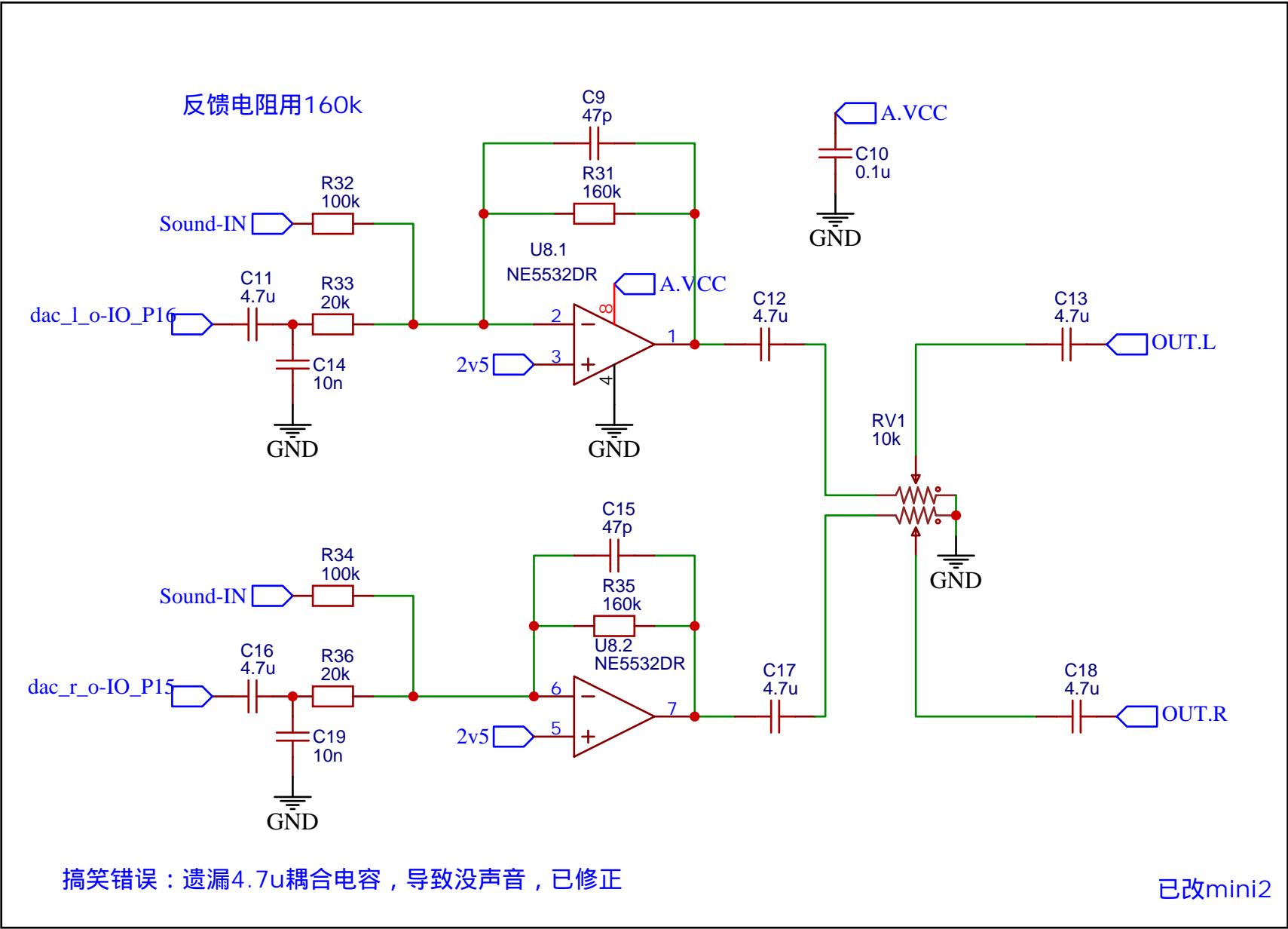


忽略EAR功能，根本不用



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嘉立创EDA	Company: Your Company	Sheet: 1/1
	Date: 2024-03-23	Drawn By: Denjhang





TITLE: Sheet_1		REV: 1.0
嘉立创EDA	Company: Your Company	Sheet: 1/1
	Date: 2024-03-24	Drawn By: Denjhang

