AC1

AC608核心板

核心板共124个 Pad
85个通用双向IO
5对LVDS IO （也可作为双向通用IO使用）
1对LVDS时钟输入IO
12个时钟输入IO（不含LVDS时钟输入IO）
5个GND（硬件连通）
4个VDD3.3输入（硬件连通）
1个VDD2.5输出
1个VDD1.2输出
4个JTAG IO

板载50MHz有源时钟，由E15管脚输入
板载W25Q16，16M的SPI FLASH，兼容EPCS16
SDRAM占用的39个IO完全独立，不与邮票孔任何IO共享

时钟输入信号，仅能作为时钟和普通信号输入，
不能作为输出，不支持上下拉。不使用时建议接地，
另外92和93可作为LVDS差分时钟输入

LVDS功能管脚，如需使用LVDS管脚，需保证核心板上R9空焊，
R8使用0R或磁珠短接。如需作为通用IO，
则R9使用0R电阻或磁珠短接，R8空焊（此为核心板出厂默认方式）

核心板JTAG IO。

核心板GND，所有GND都是连通的

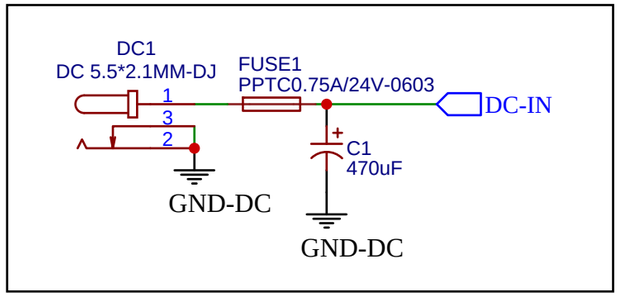
电源管脚：
VDD3.3为外部3.3V输入电源。由底板提供给核心板，
所有VDD3.3都是连通的
VDD2.5电压输出，可作为小功率电源输出到底板，
如给JTAG口供电
VDD1.2电压输出，可作为小功率电源输出到底板

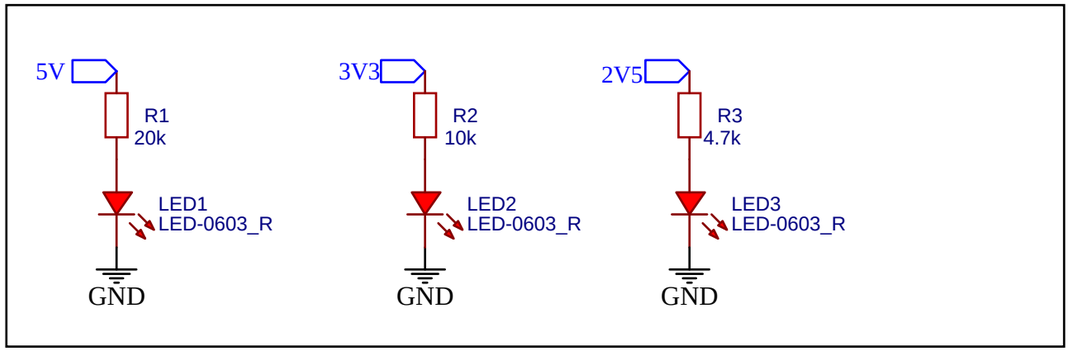
EG1
100*100mm 边框

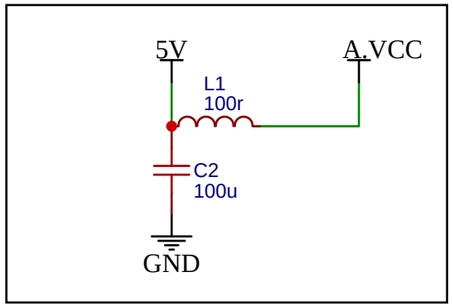
U1
HC-JN254-2-05-W

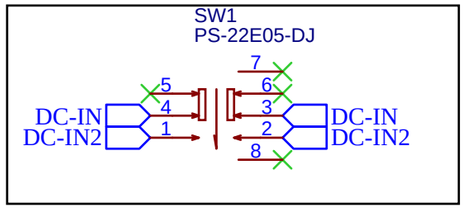
2024.3.31
1.改开关线路，按下开机
2.加核心音频直流耦合电容
3.修正VGA接线
4.添加VGA电解电容
5.修正短接电源模块线路

TITLE: Sheet_1	REV: 1.0
Company: Your Company	Sheet: 1/1
Date: 2024-03-23 Drawn By: Denjhang	

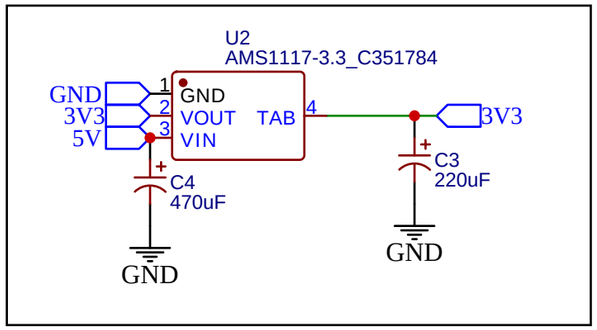




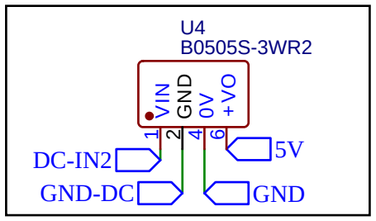


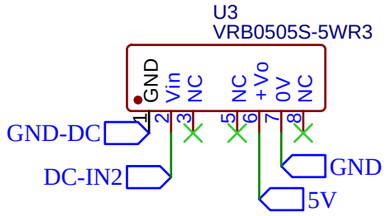


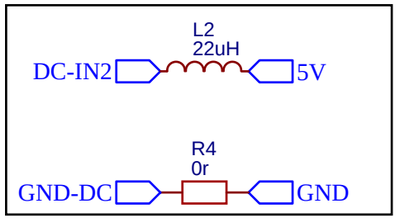
开关设计错误，符号封装错误,已修正



也可以使用VRB0505-6W但是贵







不使用隔离模块时短路原边和副边短接致命错误，已修正

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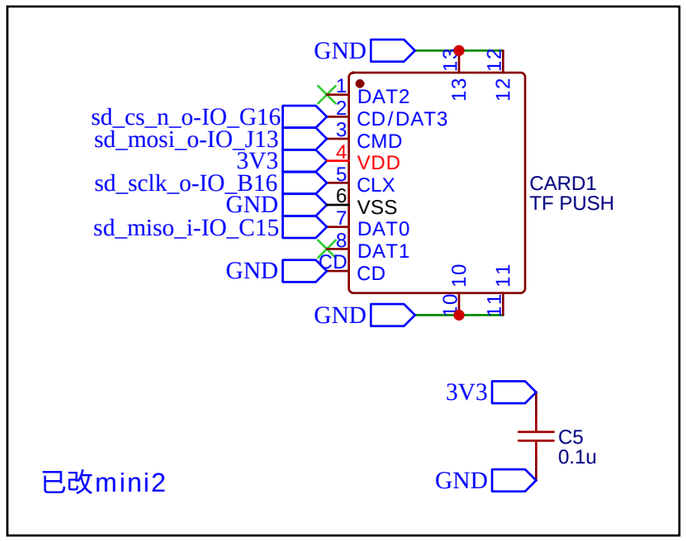
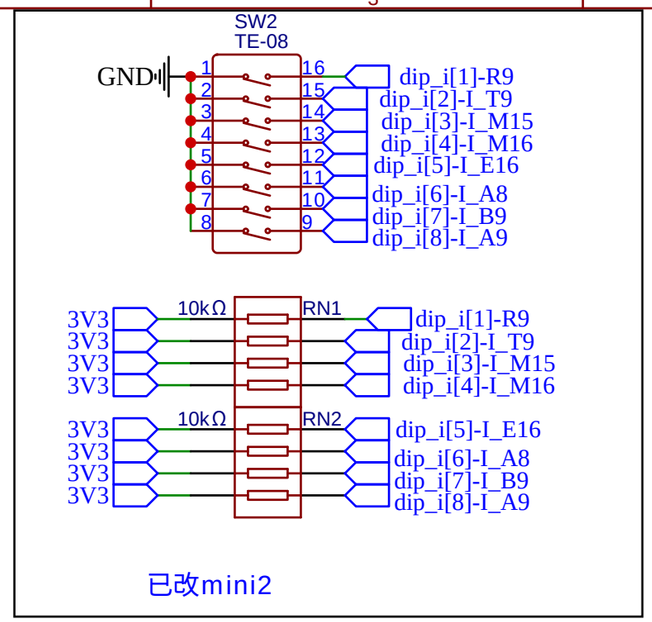
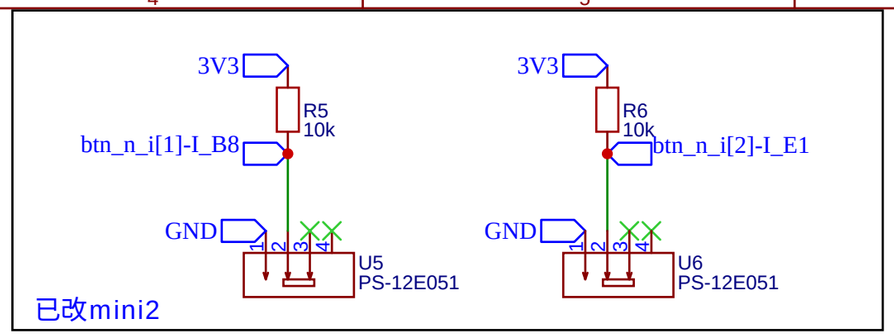
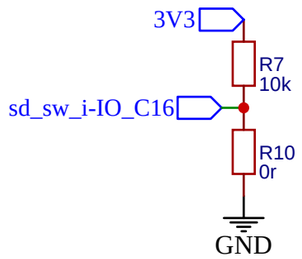


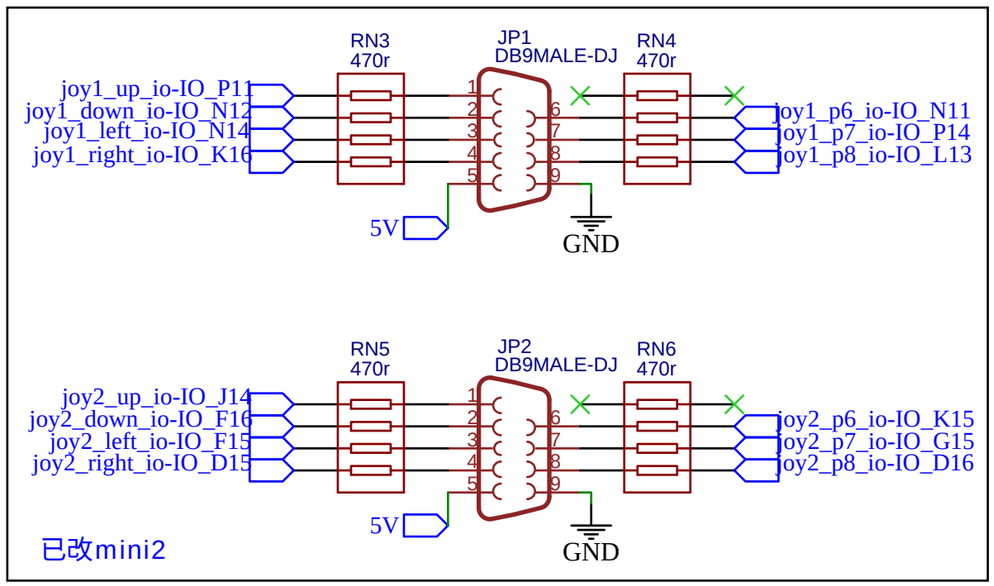


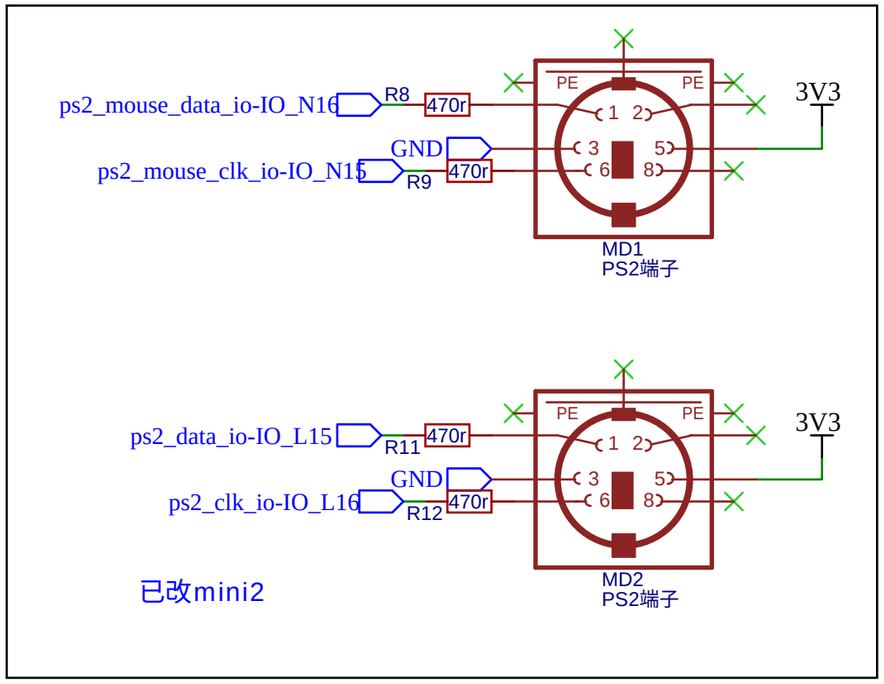




不知道如何接，之前的图都是悬空

忽略EAR功能，根本不用





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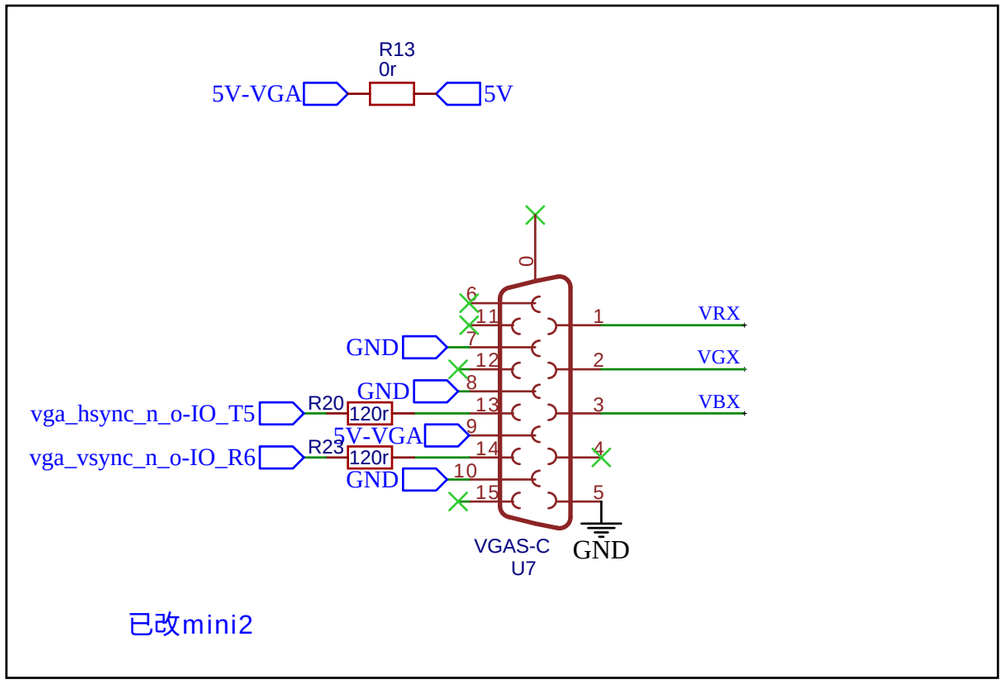

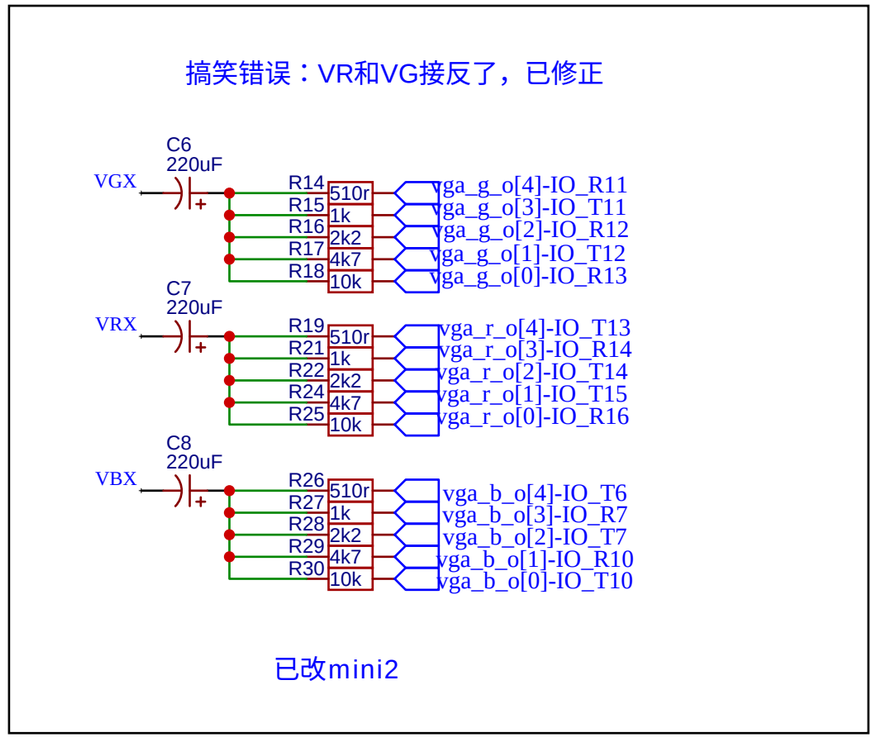

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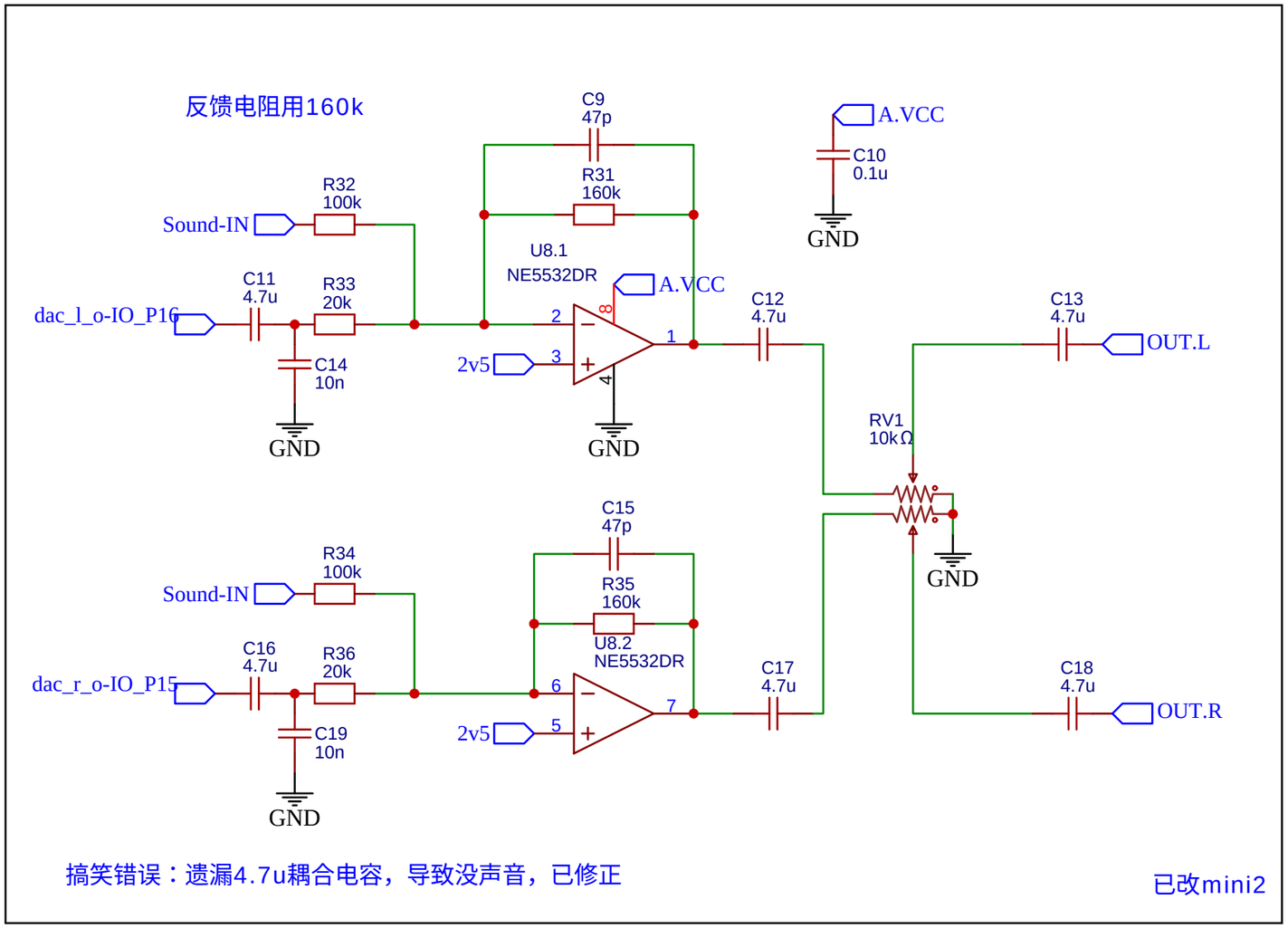
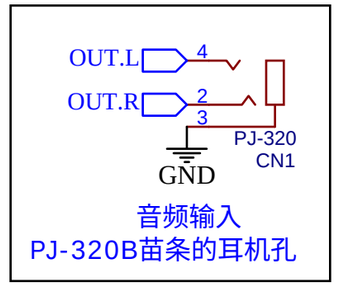
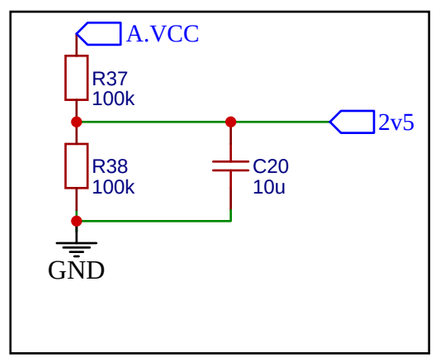
嘉立创EDA	Company: Your Company	Sheet: 1/1
	Date: 2024-03-24 Drawn By: Denjhang	







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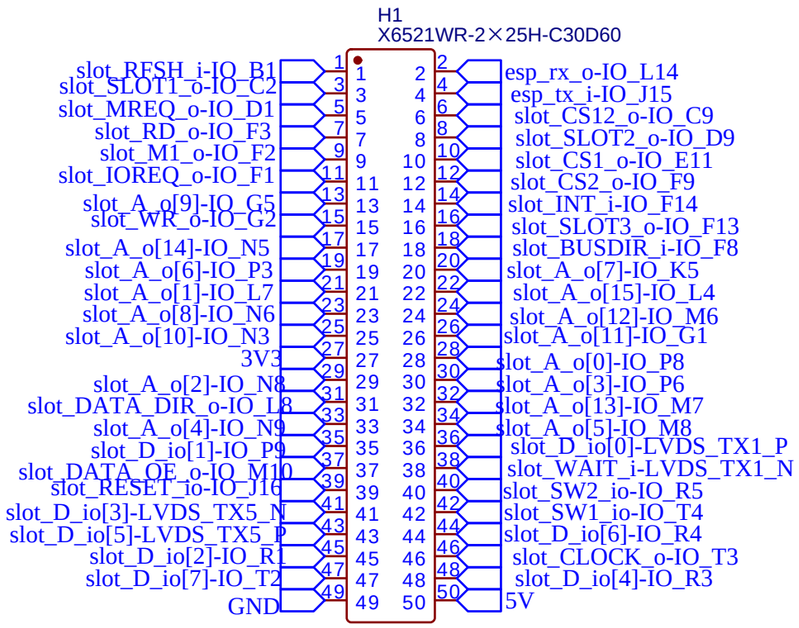
嘉立创EDA	Company: Your Company	Sheet: 1/1
	Date: 2024-03-24 Drawn By: Denjhang	



wifi模块走卡槽

兼容Mini1卡槽

已改mini2

TITLE: Sheet_1		REV: 1.0
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