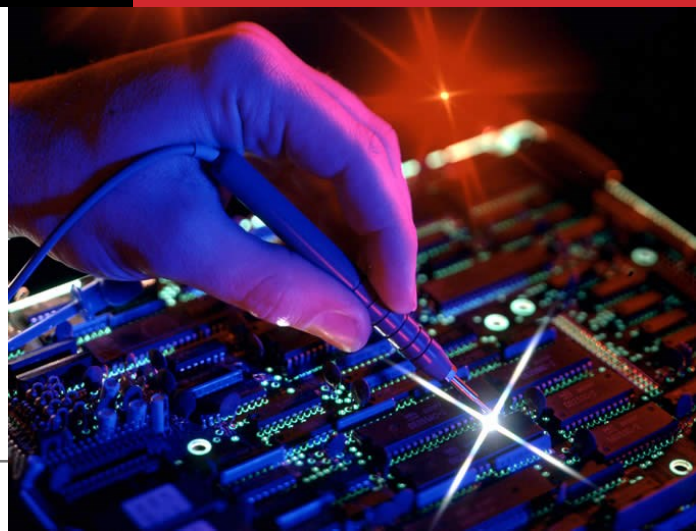
Advanced Computer Architecture

INTRODUCTION

Dennis A. N. Gookyi



CONTENTS

- Course Organization and Syllabus

INSTRUCTOR

- Instructor
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  - Research Portals:
    - https://www.researchgate.net/profile/Dennis-Gookyi
    - https://sites.google.com/view/eisedlab

INSTRUCTOR

- Instructor

Education

- Ph.D. in Information and Communication Engineering, Hanbat National University, South Korea, 2021.
- M.Eng. in Information and Communication Engineering, Hanbat National University, South Korea, 2017.
- B.Sc. in Computer Engineering, Kwame Nkrumah University of Science and Technology, Ghana, 2009.

Employment

- Research Scientist, CSIR-INSTI, Ghana, 2022 – Present.
- Researcher, Korea Electronics Technology Institute (KETI), South Korea, 2021 – 2022.
- Research and Teaching Assistant, SoC Design Lab, Hanbat National University, South Korea, 2014 – 2021.
- RTL Design Engineer, Future Systems, South Korea, 2015 – 2016.
- Teaching Assistant, Computer Engineering Department, Kwame Nkrumah University of Science and Technology, Ghana, 2013 – 2014.

LEARNING OUTCOMES

- Expected Learning Outcomes
  - Understand the basic building blocks of digital systems
  - Understand the Instruction Set Architecture of RISC-V Processor
  - Understand the inner workings of a RISC-V Processor
  - Understand the fundamentals of Designing a RISC-V Processor

PREREQUISITES AND GRADING

- Prerequisite
  - Inclination toward computer programming
  - Inclination towards Digital Systems Design
  - Engineering mindset
  - Inquisitive about the physical world
- Grading scheme: Attendance (15%), Homework (5%), Participation (5%), Project (15%), Exam (60%)
  - Homework: hybrid grading show your work in class
  - Participation: attendance, ask questions, answer questions, be active
  - Project: non-trivial implementation of something useful by applying knowledge including and beyond what's learned in class

LEARNING APPROACH

- Learning approach:
  - Type up your own code, and make it work on your device
  - Learn from sample code, assimilate then modify, integrate, or extend
  - Be ready to show your work
  - Read manuals and product specification documents

COURSE OUTLINE

- Schedule

Lecture	Topic
01	Course Overview
02	Transistors to Logic Gates
03	Combinational Logic Design
04	Memory Elements
05	Sequential Logic Design
06	Introduction to RISC-V Processor
07	RISC-V Single Cycle Implementation
08	Designing a RISC-V Single Cycle Processor from the Scratch
09	Project

TEXTBOOKS AND LINKS

- Textbook and Links
  - https://riscv.org
  - https://en.wikichip.org/wiki/WikiChip
  - https://allaboutfpga.com/product/edge-artix-7-fpga-development-board/
  - https://riscv.org/wp-content/uploads/2017/05/riscv-spec-v2.2.pdf
  - https://www.elsevier.com/__data/assets/pdf_file/0011/297533/RISC-V-Reference-Data.pdf#RISC-V%20Reference%20Data