31	27	26	25	24	20	19	15	14	12	11	7	6	0	
	funct7				rs2	]	rs1	fun	.ct3		$\operatorname{rd}$	op	code	R-type
imm[11:0]					]	rs1		.ct3	$_{\mathrm{rd}}$		op	code	I-type	
	imm[11:5] rs2		]	rs1		.ct3	imm[4:0]		op	code	S-type			
i	mm[12 10]	):5]			rs2	]	rs1	fun	.ct3	imm	[4:1 11]	op	code	B-type
	imm[31:12]										$\operatorname{rd}$	op	code	U-type
imm[20 10:1 11 19:12]										$\operatorname{rd}$	op	code	J-type	

## RV32I Base Instruction Set

	imm[31:12]	rd	0110111	LUI			
	imm[31:12]	$\operatorname{rd}$	0010111	AUIPC			
	1[20 10:1 11 19]	9:12]   rs1   000		$\operatorname{rd}$	1101111	$_{ m JAL}$	
	imm[11:0]			rd	1100111	JALR	
imm[12 10:5]	rs2	rs1	000	imm[4:1 11]	1100011	$_{ m BEQ}$	
imm[12 10:5]	rs2	rs1	001	imm[4:1 11]	1100011	BNE	
imm[12 10:5]	rs2	rs1	100	imm[4:1 11]	1100011	BLT	
imm[12 10:5]	rs2	rs1	101	imm[4:1 11]	1100011	BGE	
imm[12 10:5]	rs2	rs1	110	imm[4:1 11]	1100011	BLTU	
imm[12 10:5]	rs2	rs1	111	imm[4:1 11]	1100011	BGEU	
imm[11:0	]	rs1	000	$\operatorname{rd}$	0000011	LB	
imm[11:0	]	rs1	001	$\operatorname{rd}$	0000011	LH	
imm[11:0		rs1	010	rd	0000011	LW	
imm[11:0		rs1	100	rd	0000011	LBU	
imm[11:0	]	rs1	101	rd	0000011	LHU	
imm[11:5]	rs2	rs1	000	imm[4:0]	0100011	ceil SB	
imm[11:5]	rs2	rs1	001	imm[4:0]	0100011	SH	
imm[11:5]	rs2	rs1	010	imm[4:0]	0100011	ceil SW	
imm[11:0	]	rs1	000	$\operatorname{rd}$	0010011	ADDI	
imm[11:0	]	rs1	010	$\operatorname{rd}$	0010011	SLTI	
imm[11:0		rs1	011	rd	0010011	SLTIU	
imm[11:0	]	rs1	100	rd	0010011	XORI	
imm[11:0	]	rs1	110	rd	0010011	ORI	
imm[11:0	]	rs1	111	rd	0010011	ANDI	
0000000	shamt	rs1	001	rd	0010011	SLLI	
0000000	$\operatorname{shamt}$	rs1	101	$\operatorname{rd}$	0010011	SRLI	
0100000	$\operatorname{shamt}$	rs1	101	$\operatorname{rd}$	0010011	SRAI	
0000000	rs2	rs1	000	$\operatorname{rd}$	0110011	ADD	
0100000	rs2	rs1	000	$\operatorname{rd}$	0110011	SUB	
0000000	rs2	rs1	001	$\operatorname{rd}$	0110011	SLL	
0000000	rs2	rs1	010	rd	0110011	SLT	
0000000	rs2	rs1	011	rd	0110011	SLTU	
0000000	rs2	rs1	100	rd	0110011	XOR	
0000000	rs2	rs1	101	$\operatorname{rd}$	0110011	SRL	
0100000	rs2	rs1	101	$\operatorname{rd}$	0110011	SRA	
0000000	rs2	rs1	110	$\operatorname{rd}$	0110011	OR	
0000000	rs2	rs1	111	rd	0110011	AND	
0000 pred	l succ	00000	000	00000	0001111	FENCE	
0000 0000	0000	00000	001	00000	0001111	FENCE.I	
0000000000	000	00000	000	00000	1110011	ECALL	
0000000000	001	00000	000	00000	1110011	] EBREAK	
csr		rs1	001	rd	1110011	CSRRW	
csr		rs1	010	$\operatorname{rd}$	1110011	CSRRS	
csr		rs1	011	$\operatorname{rd}$	1110011	CSRRC	
csr		zimm	101	$\operatorname{rd}$	1110011	CSRRWI	
csr		zimm	110	$\operatorname{rd}$	1110011	CSRRSI	
csr		zimm	111	rd	1110011	CSRRCI	