Advanced Computer Architecture

2ND Semester 2024

Mid Semester Exams

Release Date

09/07/2024

Due Date

Morning Session: 18/07/2024 @ 1:00 PM (I will collect them in class)

Overview

Read the paper Reading01 (RISC-V Hardware Synthesizable Processor Design Test and Verification Using User-Friendly Desktop Application) and answer the questions.

Advanced Computer Architecture

2ND Semester 2024

Introduction

1. What are the key contributions of the paper on the functionality of the RISC-V ISA processor?
2. Explain the purpose of designing a desktop UI program for the RISC-V ISA processor.
3. How does the paper propose to use the UART protocol in the context of the RISC-V processor?
4. Describe the 32-bit single-cycle RISC-V ISA core implemented in the paper.

Related Work

1. Discuss the evolution of open-source RISC-V processors as described in the paper.
2. What improvements have been observed in the RISC-V community due to continual analysis and review of proposed architectures?
3. Compare the complexity and throughput of other open-source RISC-V processors with the one proposed in the paper.
4. How does the proposed RISC-V processor contribute to the existing body of research on RISC-V architectures?

Functionality of the Implemented RISC-V Processor Core

1. Explain the control and implementation of the 32-bit single-cycle RISC-V ISA core using Verilog HDL.
2. What are the key features of the processor designed to execute instruction data sent from the Desktop UI program?
3. Describe the internal operation monitoring of the RISC-V processor using FPGA board peripherals.
4. How does the processor handle the execution of instructions in real-time?

Advanced Computer Architecture

2ND Semester 2024

Serial Communication

1. Explain the series of schedules required to connect the user-application program to the processor.
2. How is data broken into 4-bit blocks and converted into ASCII code for transmission over UART?
3. Describe the consistency measures taken for data transmission over UART.
4. What are the steps involved in the data reception process from FPGA to the UI program?

Desktop UI Program

1. How was the desktop UI program developed and what tools were used?
2. Describe the flowchart of the execution flow of the UI program.
3. Explain the process of connecting the UI program with FPGA through UART communication.
4. What steps are involved in entering and sending instruction data using the UI program?

Hardware Resources Utilization and Experiment

1. What hardware resources were utilized in the implementation of the RISC-V processor?
2. Describe the experiment setup used to validate the RISC-V processor core.
3. How does the paper measure the utilization of hardware resources during processor operation?
4. Discuss the significance of the clock divider in the top module of the processor.

Conclusions and Future Works

1. Summarize the main conclusions drawn from the paper's research on the RISC-V processor.
2. What future works are proposed to enhance the functionality of the RISC-V processor?
3. Discuss the potential impact of the proposed future works on RISC-V processor design.
4. How does the paper suggest improving data transmission protocols in future research?