Advanced Computer Architecture

2nd Semester 2024

Course Information

Instructor

Name: Dennis Gookyi

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Website: https://sites.google.com/view/eisedlab

Class Meeting

Morning Session: Thursday 08:00 AM – 11:00 AM

Textbooks

1. David A. Patterson, John L. Hennessy: *Computer Organization and Design, The Hardware/Software Interface – RISC-V Edition*
2. Ming-Bo Lin*: Digital System Designs and Practices Using Verilog HDL and FPGAs*

Course Site

https://github.com/dennisgookyi/Advanced-Computer-Architecture

Expected Learning Outcomes

- Understand the basic building blocks of digital systems
- Understand the Instruction Set Architecture of RISC-V Processor
- Understand the inner workings of a RISC-V Processor
- Understand the fundamentals of Designing a RISC-V Processor

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Schedule

Lecture	Topic
01	Course Overview
02	Transistors to Logic Gates
03	Combinational Logic Design
04	Memory Elements
05	Sequential Logic Design
06	Introduction to RISC-V Processor
07	RISC-V Single Cycle Implementation
08	Designing a RISC-V Single Cycle Processor from the Scratch
09	Project

Useful Links

1. https://riscv.org
2. https://en.wikichip.org/wiki/WikiChip
3. https://allaboutfpga.com/product/edge-artix-7-fpga-development-board/
4. https://riscv.org/wp-content/uploads/2017/05/riscv-spec-v2.2.pdf
5. https://www.elsevier.com/__data/assets/pdf_file/0011/297533/RISC-V-Reference-Data.pdf#RISC-V%20Reference%20Data