Advanced Computer Architecture & Advanced Microprocessor System

EDGE ARTIX 7 FPGA DEVELOPMENT BOARD

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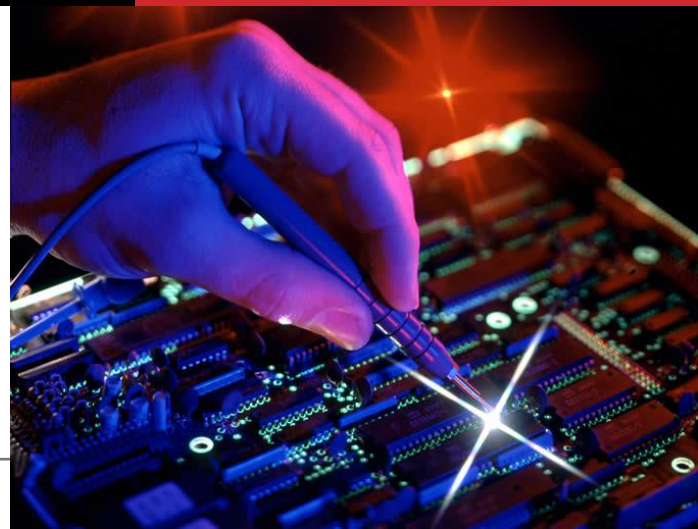

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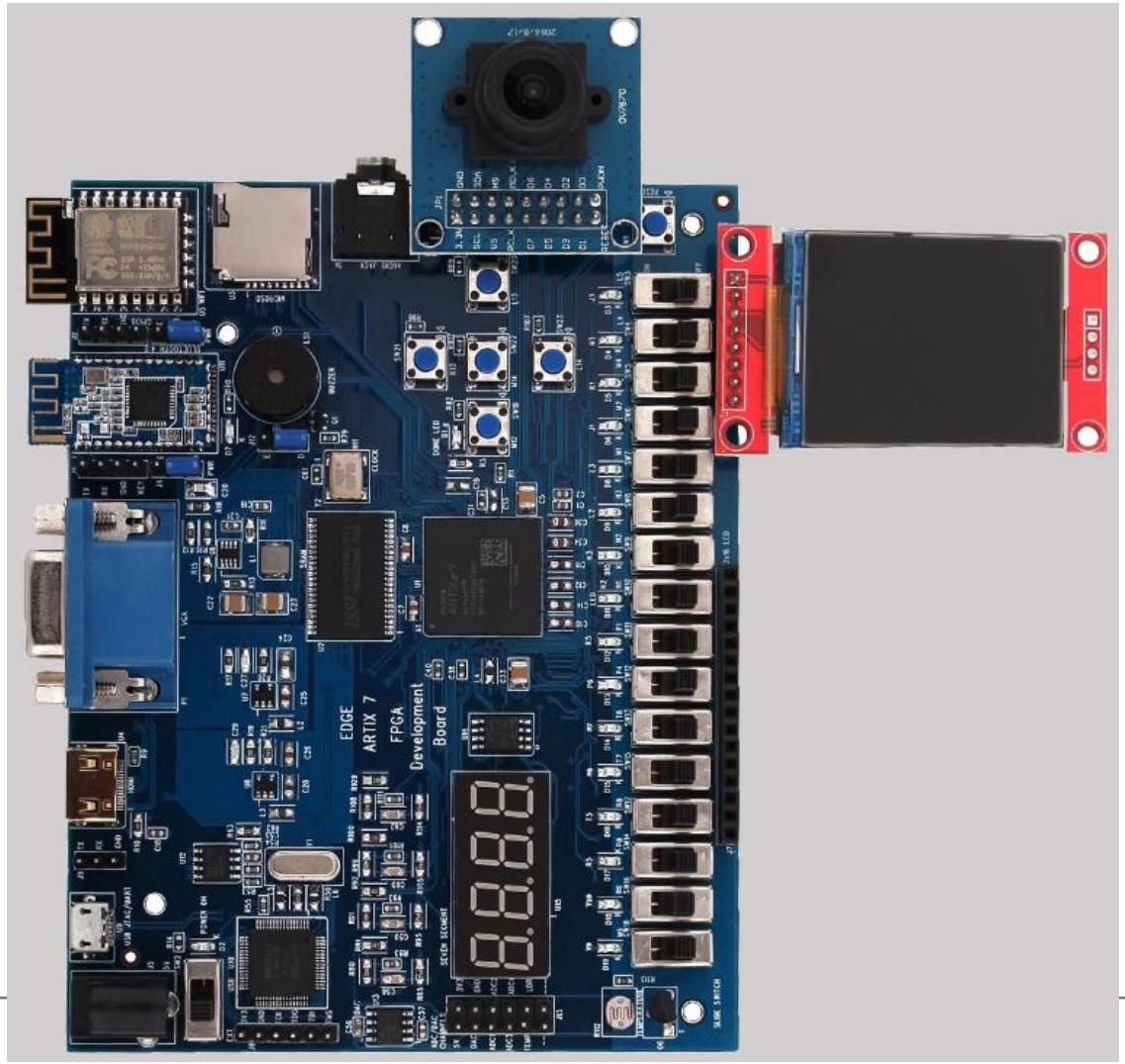
EDGE ARTIX 7 FPGA BOARD

- Artix 7 FPGA development board



EDGE ARTIX 7 FPGA BOARD

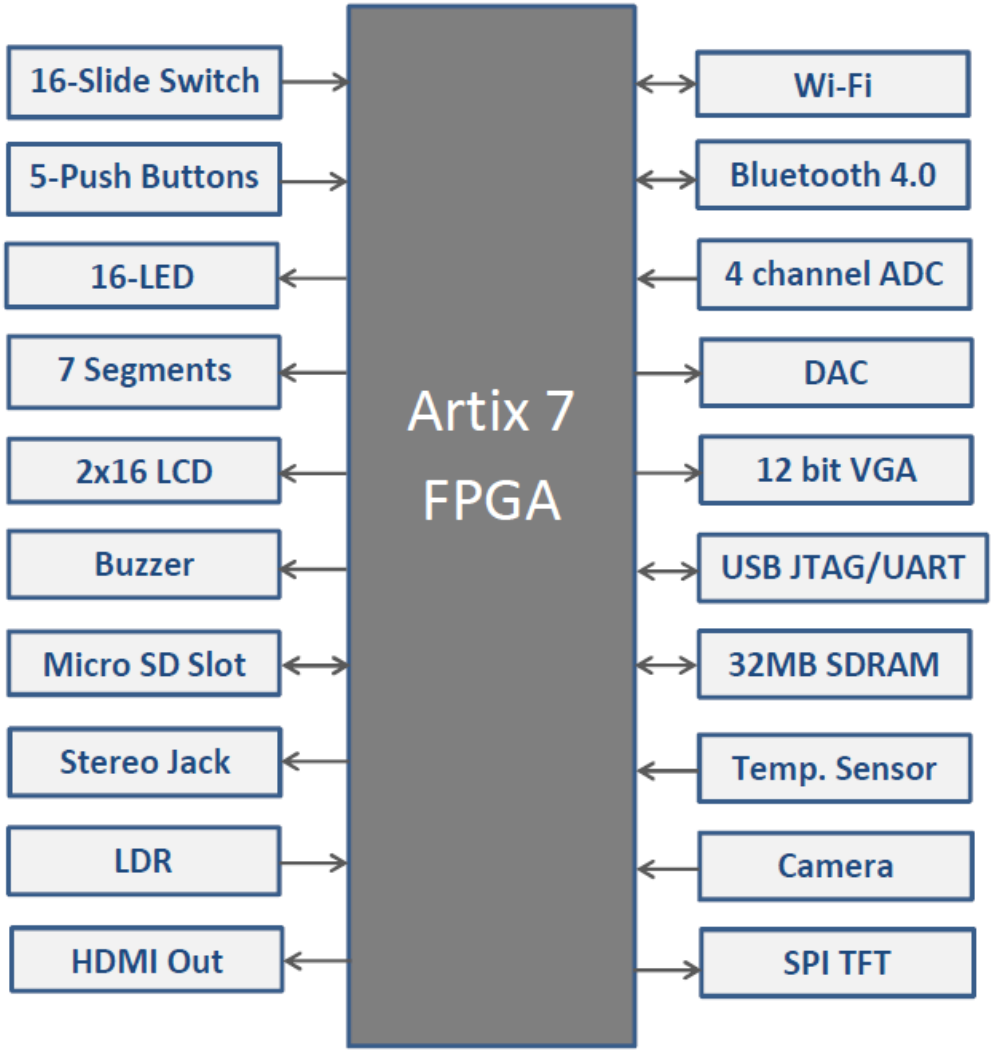
- Board Applications
  - Wireless control
  - Environment monitor
  - IoT (Internet of Things)
  - Product Prototyping
  - Image Processing
  - Video Processing
  - Audio Processing

EDGE ARTIX 7 FPGA BOARD

- Board Features
  - Xilinx XC7A35T-1FTG256 Artix 7 FPGA
  - 8MB SPI FLASH Memory
  - 32MB SDRAM
  - HDMI Out
  - Micro SD Slot
  - On-Board USB JTAG Programmer
  - USB to UART Interface
  - WIFI Interface
  - Low Power Bluetooth Interface
  - 12-bit VGA Interface
  - 8 Channel SPI ADC
  - Temperature Sensor
  - LDR Interface
  - SPI DAC
  - 2×16 LCD Display
  - 4 Digit Seven Segment Display
  - 5v Buzzer
  - CMOS Camera Interface
  - TFT Display Interface

EDGE ARTIX 7 FPGA BOARD

- Block Diagram of EDGE Artix 7 FPGA Development Board



EDGE ARTIX 7 FPGA BOARD

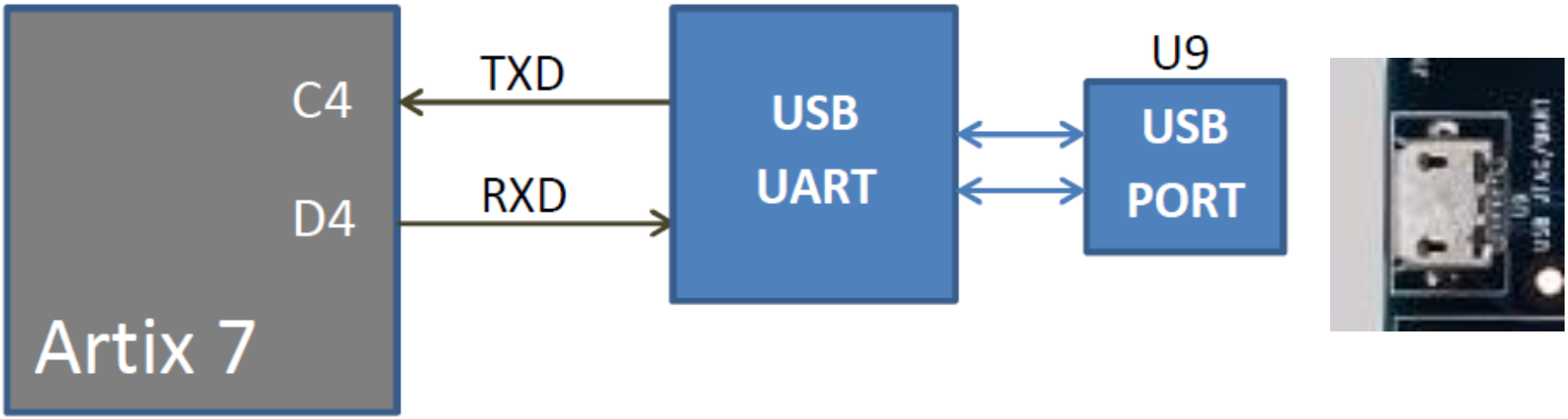
- Power Supply
  - EDGE Artix 7 development board can get 5V power from either USB JTAG Port U9 or External Power Supply connector J5
    - Switch SW2 can be used to select the source of power from USB or External Power Supply
  - Board consists of 3 Voltage regulators 3.3v, 1.8v and 1v
    - The Kit requires a 3.3v supply for FPGA I/O, SDRAM, Clock, USB, ADC, DAC, FLASH, and so on
    - The 1.8v Voltage is for FPGA Auxiliary supply and ADC
    - The 1v power supply is dedicated for FPGA Core and Block RAM voltage

EDGE ARTIX 7 FPGA BOARD

- Programming hardware
  - FPGA can be configured either from USB JTAG using Xilinx Vivado software or by on-board SPI FLASH Memory
  - FPGA configured through JTAG gets erased when the power supply is removed or by pressing the reset button SW1
  - To store the data permanently on FPGA, we have to store the configuration bit file to SPI FLASH Memory
  - It automatically reconfigures the FPGA after resetting or Power on
  - The EDGE Artix 7 FPGA Development board is fully compatible with the Xilinx Vivado design suite with on-board USB JTAG Interface

EDGE ARTIX 7 FPGA BOARD

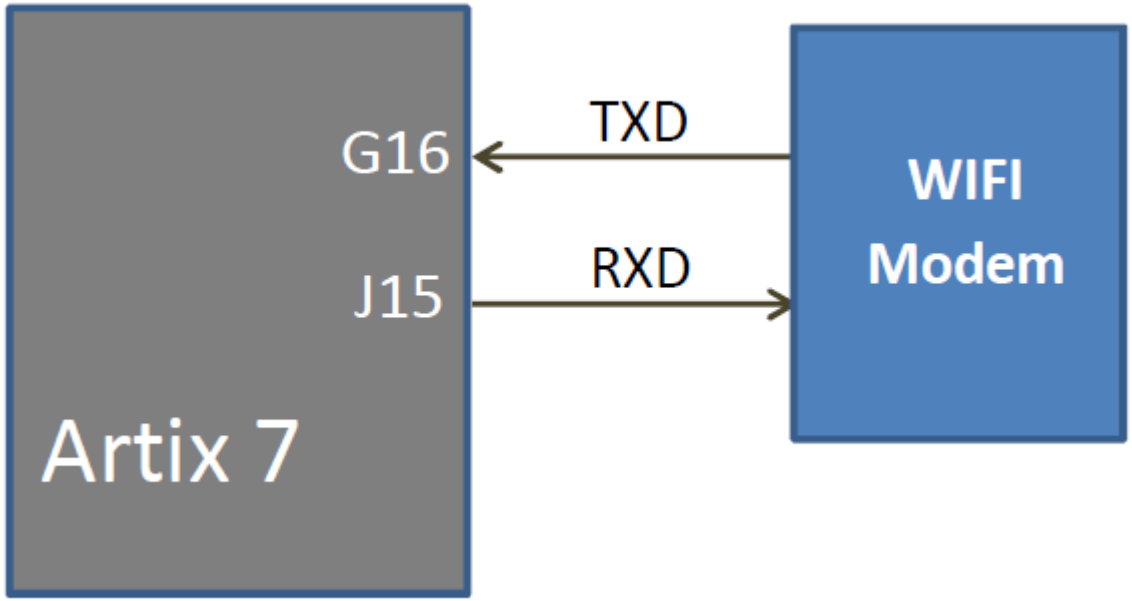
- USB UART
  - The EDGE Board includes FT2232H IC acts as USB UART Bridge to communicate board with the Windows PC COM port interface
  - The UART Transmitter and Receiver lines of the FTDI chip is directly connected to the Artix 7 FPGA I/O pins for USB UART Communication

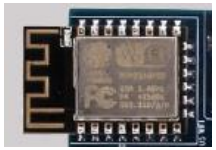



```
# USB UART
set_property -dict { PACKAGE_PIN C4 IOSTANDARD LVCMOS33 } [get_ports {usb_uart_txd}];
set_property -dict { PACKAGE_PIN D4 IOSTANDARD LVCMOS33 } [get_ports {usb_uart_rxd}];
```

EDGE ARTIX 7 FPGA BOARD

- WIFI Communication
  - The EDGE Board contains On-board ESP8266 12F WIFI Module connected with Artix 7 FPGA through serial interface
  - The range of communication for WIFI modem is 50 – 100 meter distance

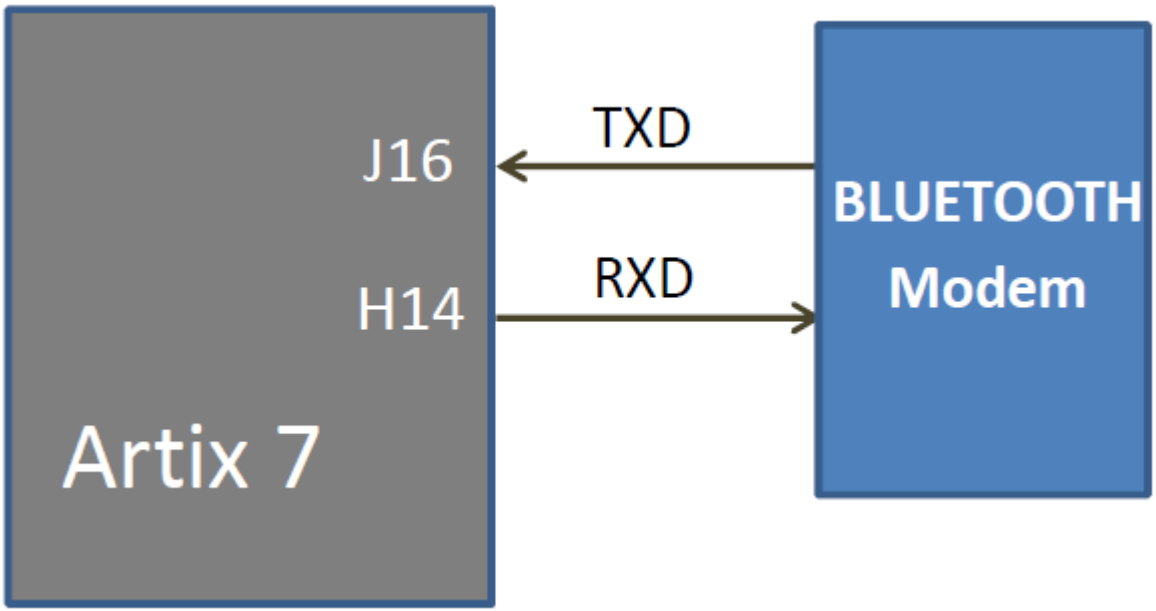




```
# WiFi
set_property -dict { PACKAGE_PIN J15 IOSTANDARD LVCMOS33 } [get_ports { wifi_txd }];
set_property -dict { PACKAGE_PIN G16 IOSTANDARD LVCMOS33 } [get_ports { wifi_rxd }];
```

EDGE ARTIX 7 FPGA BOARD

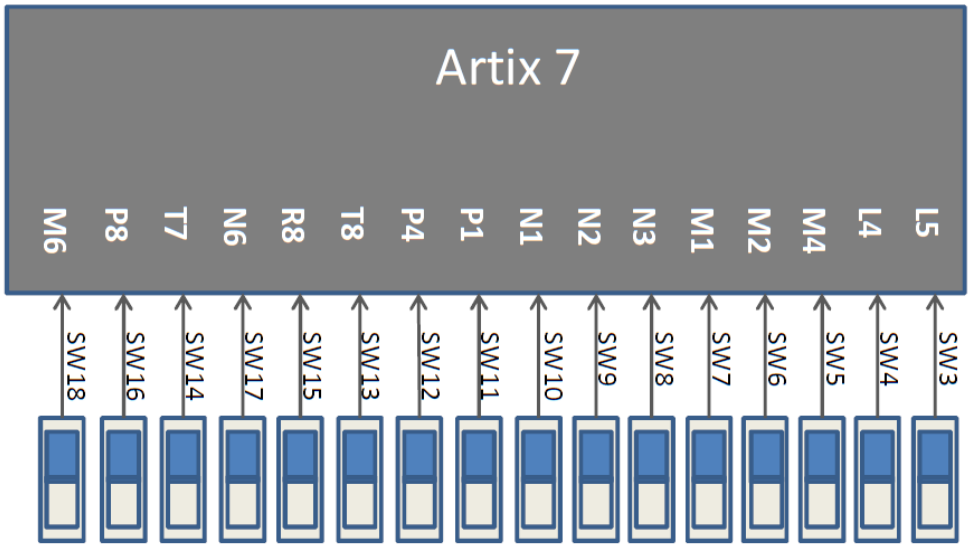
- Bluetooth Communication
  - The EDGE contains low-power Bluetooth 4.0 BLE interface on-board
  - The Bluetooth Module CC2541 is serially interfaced with FPGA with Transmit and Receive lines



```
# Bluetooth
set_property -dict { PACKAGE_PIN H14 IOSTANDARD LVCMOS33 } [get_ports { Bluetooth_txd }];
set_property -dict { PACKAGE_PIN J16 IOSTANDARD LVCMOS33 } [get_ports { Bluetooth_rxd }];
```

EDGE ARTIX 7 FPGA BOARD

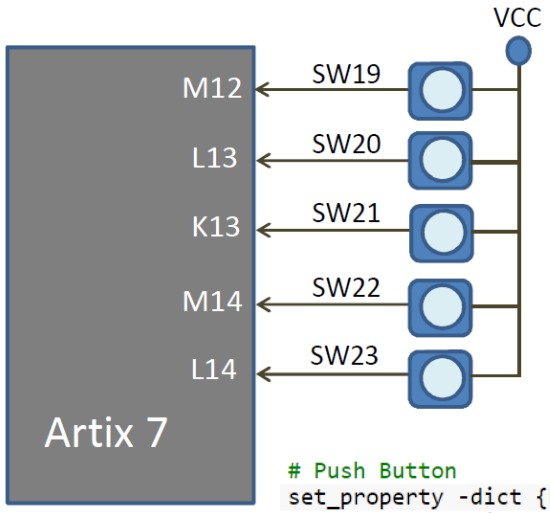
- Slide Switches
  - The EDGE board includes 16 SPDT slide switches for digital input
  - These digital inputs are connected to Artix 7 FPGA through resistors for protection against short circuit
  - Slide switch outputs constant high or constant low based on the user changing its position




```
# Switches
set_property -dict { PACKAGE_PIN L5    IOSTANDARD LVCMOS33 } [get_ports { sw[0] }];#LSB
set_property -dict { PACKAGE_PIN L4    IOSTANDARD LVCMOS33 } [get_ports { sw[1] }];
set_property -dict { PACKAGE_PIN M4    IOSTANDARD LVCMOS33 } [get_ports { sw[2] }];
set_property -dict { PACKAGE_PIN M2    IOSTANDARD LVCMOS33 } [get_ports { sw[3] }];
set_property -dict { PACKAGE_PIN M1    IOSTANDARD LVCMOS33 } [get_ports { sw[4] }];
set_property -dict { PACKAGE_PIN N3    IOSTANDARD LVCMOS33 } [get_ports { sw[5] }];
set_property -dict { PACKAGE_PIN N2    IOSTANDARD LVCMOS33 } [get_ports { sw[6] }];
set_property -dict { PACKAGE_PIN N1    IOSTANDARD LVCMOS33 } [get_ports { sw[7] }];
set_property -dict { PACKAGE_PIN P1    IOSTANDARD LVCMOS33 } [get_ports { sw[8] }];
set_property -dict { PACKAGE_PIN P4    IOSTANDARD LVCMOS33 } [get_ports { sw[9] }];
set_property -dict { PACKAGE_PIN T8    IOSTANDARD LVCMOS33 } [get_ports { sw[10] }];
set_property -dict { PACKAGE_PIN R8    IOSTANDARD LVCMOS33 } [get_ports { sw[11] }];
set_property -dict { PACKAGE_PIN N6    IOSTANDARD LVCMOS33 } [get_ports { sw[12] }];
set_property -dict { PACKAGE_PIN T7    IOSTANDARD LVCMOS33 } [get_ports { sw[13] }];
set_property -dict { PACKAGE_PIN P8    IOSTANDARD LVCMOS33 } [get_ports { sw[14] }];
set_property -dict { PACKAGE_PIN M6    IOSTANDARD LVCMOS33 } [get_ports { sw[15] }];#MSB
```

EDGE ARTIX 7 FPGA BOARD

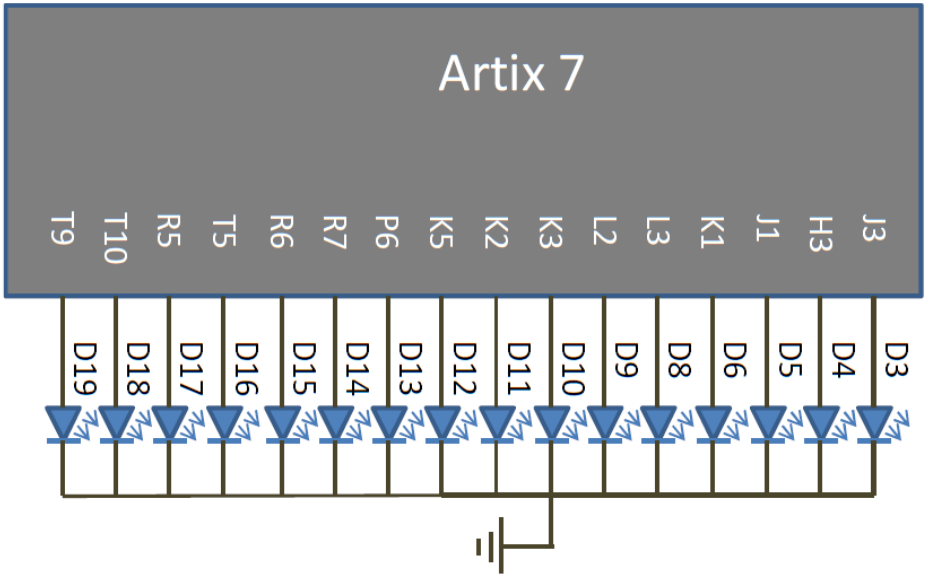
- Push Buttons
  - The Board contains 5 Push buttons for providing momentary digital inputs
  - They are connected to FPGA lines through resistors to prevent short circuit
  - By default the switch is in Active low
  - When the user pressed the push button they are driven high



```
# Push Button
set_property -dict {PACKAGE_PIN K13 IOSTANDARD LVCMOS33 PULLDOWN true} [get_ports {pb[0]}]; #Button-top
set_property -dict {PACKAGE_PIN L14 IOSTANDARD LVCMOS33 PULLDOWN true} [get_ports {pb[1]}]; #Button-bottom
set_property -dict {PACKAGE_PIN M12 IOSTANDARD LVCMOS33 PULLDOWN true} [get_ports {pb[2]}]; #Button-left
set_property -dict {PACKAGE_PIN L13 IOSTANDARD LVCMOS33 PULLDOWN true} [get_ports {pb[3]}]; #Button-right
set_property -dict {PACKAGE_PIN M14 IOSTANDARD LVCMOS33 PULLDOWN true} [get_ports {pb[4]}]; #Button-center
```

EDGE ARTIX 7 FPGA BOARD

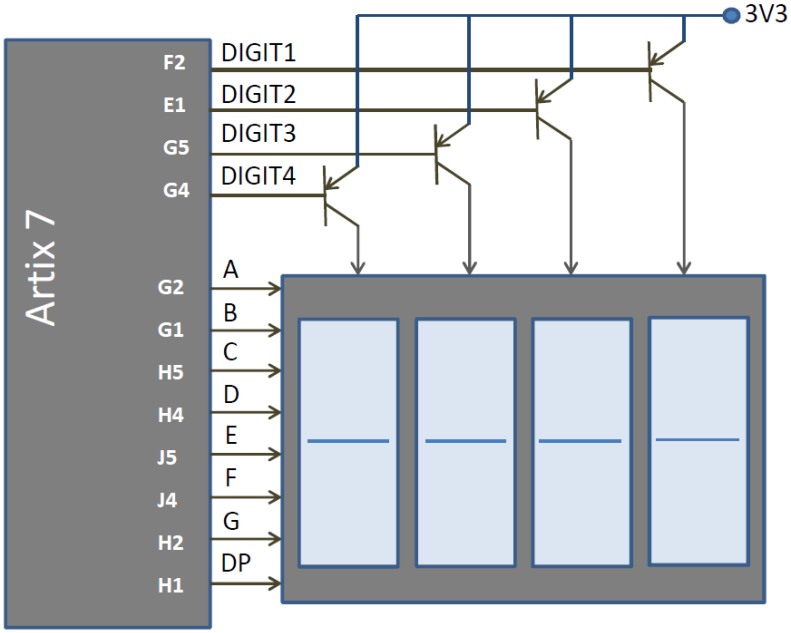
- LEDs
  - The Kit consists of 16 LEDs for displaying digital outputs
  - These LEDs are connected to FPGA through a series of resistors
  - Logic High signal turns ON LED and Logic Low signal turns OFF LED to demonstrate the digital output




```
# LEDs
set_property -dict { PACKAGE_PIN J3    IOSTANDARD LVCMOS33 } [get_ports { led[0] }];#LSB
set_property -dict { PACKAGE_PIN H3    IOSTANDARD LVCMOS33 } [get_ports { led[1] }];
set_property -dict { PACKAGE_PIN J1    IOSTANDARD LVCMOS33 } [get_ports { led[2] }];
set_property -dict { PACKAGE_PIN K1    IOSTANDARD LVCMOS33 } [get_ports { led[3] }];
set_property -dict { PACKAGE_PIN L3    IOSTANDARD LVCMOS33 } [get_ports { led[4] }];
set_property -dict { PACKAGE_PIN L2    IOSTANDARD LVCMOS33 } [get_ports { led[5] }];
set_property -dict { PACKAGE_PIN K3    IOSTANDARD LVCMOS33 } [get_ports { led[6] }];
set_property -dict { PACKAGE_PIN K2    IOSTANDARD LVCMOS33 } [get_ports { led[7] }];
set_property -dict { PACKAGE_PIN K5    IOSTANDARD LVCMOS33 } [get_ports { led[8] }];
set_property -dict { PACKAGE_PIN P6    IOSTANDARD LVCMOS33 } [get_ports { led[9] }];
set_property -dict { PACKAGE_PIN R7    IOSTANDARD LVCMOS33 } [get_ports { led[10] }];
set_property -dict { PACKAGE_PIN R6    IOSTANDARD LVCMOS33 } [get_ports { led[11] }];
set_property -dict { PACKAGE_PIN T5    IOSTANDARD LVCMOS33 } [get_ports { led[12] }];
set_property -dict { PACKAGE_PIN R5    IOSTANDARD LVCMOS33 } [get_ports { led[13] }];
set_property -dict { PACKAGE_PIN T10   IOSTANDARD LVCMOS33 } [get_ports { led[14] }];
set_property -dict { PACKAGE_PIN T9    IOSTANDARD LVCMOS33 } [get_ports { led[15] }];#MSB
```

EDGE ARTIX 7 FPGA BOARD

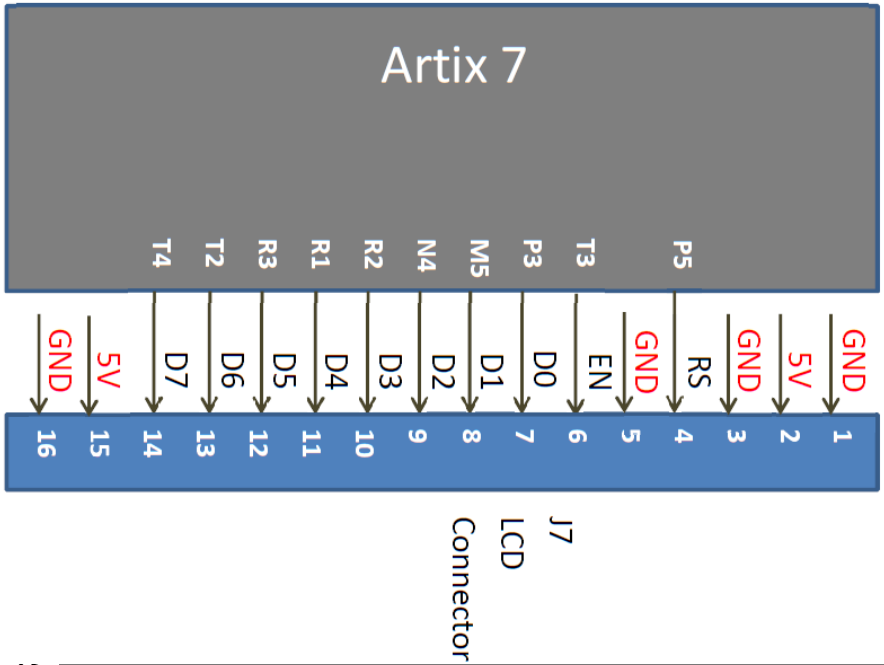
- Seven-segment Display
  - The EDGE Board consists of 4 digit 7 segment displays with common anode
  - Each of the seven segments contains LEDs that can be turned on by sending an active low signal
  - For example, to display digit 8 in the seven segments display
  - All the segments are enabled using an active low '0' signal




```
#7 segment display
set_property -dict { PACKAGE_PIN F2    IOSTANDARD LVCMOS33 } [get_ports {digit[0]}]; #LSB
set_property -dict { PACKAGE_PIN E1    IOSTANDARD LVCMOS33 } [get_ports {digit[1]}];
set_property -dict { PACKAGE_PIN G5    IOSTANDARD LVCMOS33 } [get_ports {digit[2]}];
set_property -dict { PACKAGE_PIN G4    IOSTANDARD LVCMOS33 } [get_ports {digit[3]}]; #MSB

set_property -dict { PACKAGE_PIN G2    IOSTANDARD LVCMOS33 } [get_ports {Seven_Seg[0]}];#A
set_property -dict { PACKAGE_PIN G1    IOSTANDARD LVCMOS33 } [get_ports {Seven_Seg[1]}];#B
set_property -dict { PACKAGE_PIN H5    IOSTANDARD LVCMOS33 } [get_ports {Seven_Seg[2]}];#C
set_property -dict { PACKAGE_PIN H4    IOSTANDARD LVCMOS33 } [get_ports {Seven_Seg[3]}];#D
set_property -dict { PACKAGE_PIN J5    IOSTANDARD LVCMOS33 } [get_ports {Seven_Seg[4]}];#E
set_property -dict { PACKAGE_PIN J4    IOSTANDARD LVCMOS33 } [get_ports {Seven_Seg[5]}];#F
set_property -dict { PACKAGE_PIN H2    IOSTANDARD LVCMOS33 } [get_ports {Seven_Seg[6]}];#G
set_property -dict { PACKAGE_PIN H1    IOSTANDARD LVCMOS33 } [get_ports {Seven_Seg[7]}];#DP
```

EDGE ARTIX 7 FPGA BOARD

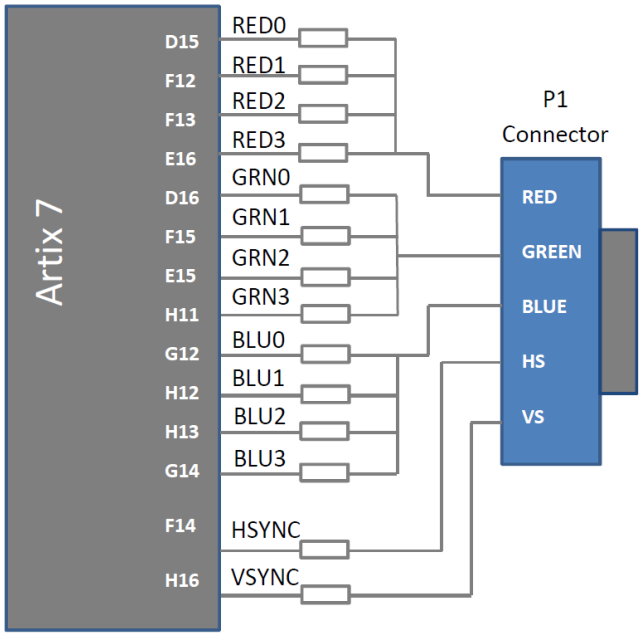
- 2x16 LCD
  - The EDGE board consists of 2x16 LCD interface at the female connector J7
  - LCD display is interfaced in the 8-bit data mode, RS pin is used to select data/command mode, and En pin is used to enable the LCD




```
# 2x16 LCD
set_property -dict { PACKAGE_PIN P3 IOSTANDARD LVCMOS33 } [get_ports {data[7]}];
set_property -dict { PACKAGE_PIN M5 IOSTANDARD LVCMOS33 } [get_ports {data[6]}];
set_property -dict { PACKAGE_PIN N4 IOSTANDARD LVCMOS33 } [get_ports {data[5]}];
set_property -dict { PACKAGE_PIN R2 IOSTANDARD LVCMOS33 } [get_ports {data[4]}];
set_property -dict { PACKAGE_PIN R1 IOSTANDARD LVCMOS33 } [get_ports {data[3]}];
set_property -dict { PACKAGE_PIN R3 IOSTANDARD LVCMOS33 } [get_ports {data[2]}];
set_property -dict { PACKAGE_PIN T2 IOSTANDARD LVCMOS33 } [get_ports {data[1]}];
set_property -dict { PACKAGE_PIN T4 IOSTANDARD LVCMOS33 } [get_ports {data[0]}];
set_property -dict { PACKAGE_PIN T3 IOSTANDARD LVCMOS33 } [get_ports {lcd_e}];
set_property -dict { PACKAGE_PIN P5 IOSTANDARD LVCMOS33 } [get_ports {lcd_rs}];
#LCD R/W pin is connected to ground by default.No need to assign LCD R/W Pin.
```

EDGE ARTIX 7 FPGA BOARD

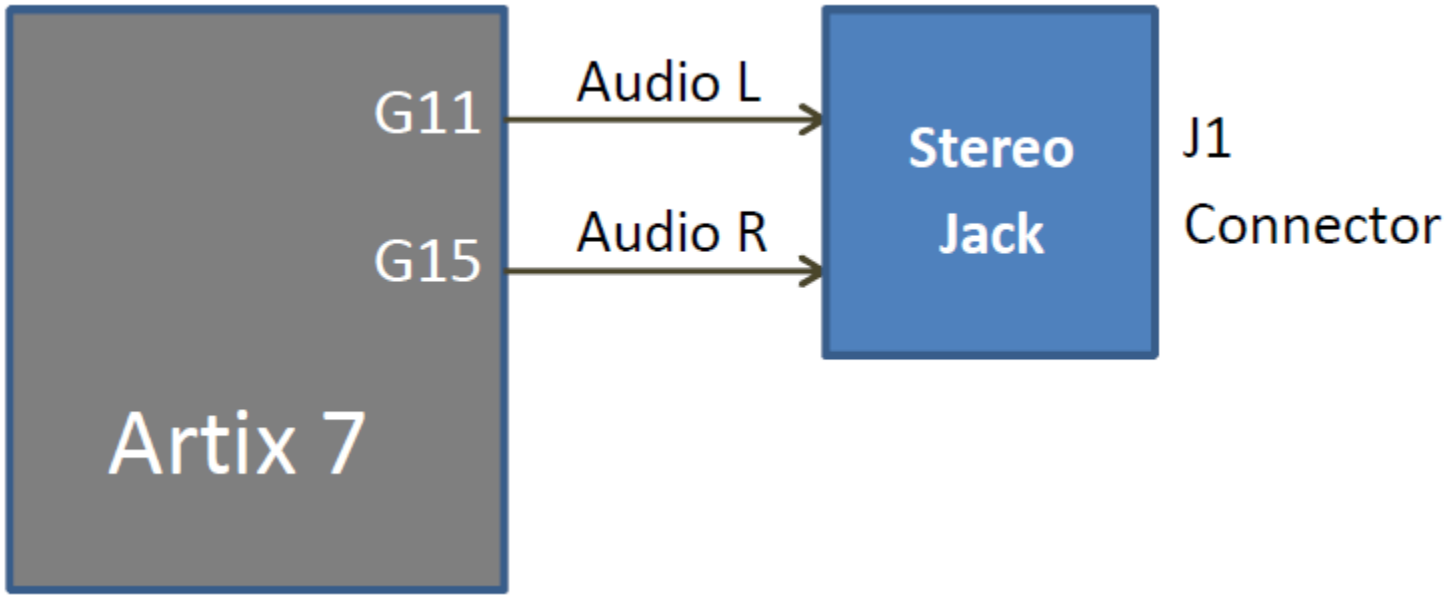
- VGA
  - The EDGE Board contains 12-bit VGA interface to generate VGA signals from FPGA and display the output in the VGA monitor
  - The 12-bit VGA output a depth of 4096 colors in the Monitor
  - Series resistors are used to construct DAC to implement VGA interface




```
# VGA 12 bit
set_property -dict { PACKAGE_PIN F14 IOSTANDARD LVCMOS33 } [get_ports {vga_hsync}];
set_property -dict { PACKAGE_PIN H16 IOSTANDARD LVCMOS33 } [get_ports {vga_vsync}];
set_property -dict { PACKAGE_PIN D15 IOSTANDARD LVCMOS33 } [get_ports {vga_r[0]}];
set_property -dict { PACKAGE_PIN F12 IOSTANDARD LVCMOS33 } [get_ports {vga_r[1]}];
set_property -dict { PACKAGE_PIN F13 IOSTANDARD LVCMOS33 } [get_ports {vga_r[2]}];
set_property -dict { PACKAGE_PIN E16 IOSTANDARD LVCMOS33 } [get_ports {vga_r[3]}];
set_property -dict { PACKAGE_PIN D16 IOSTANDARD LVCMOS33 } [get_ports {vga_g[0]}];
set_property -dict { PACKAGE_PIN F15 IOSTANDARD LVCMOS33 } [get_ports {vga_g[1]}];
set_property -dict { PACKAGE_PIN E15 IOSTANDARD LVCMOS33 } [get_ports {vga_g[2]}];
set_property -dict { PACKAGE_PIN H11 IOSTANDARD LVCMOS33 } [get_ports {vga_g[3]}];
set_property -dict { PACKAGE_PIN G12 IOSTANDARD LVCMOS33 } [get_ports {vga_b[0]}];
set_property -dict { PACKAGE_PIN H12 IOSTANDARD LVCMOS33 } [get_ports {vga_b[1]}];
set_property -dict { PACKAGE_PIN H13 IOSTANDARD LVCMOS33 } [get_ports {vga_b[2]}];
set_property -dict { PACKAGE_PIN G14 IOSTANDARD LVCMOS33 } [get_ports {vga_b[3]}];
```

EDGE ARTIX 7 FPGA BOARD

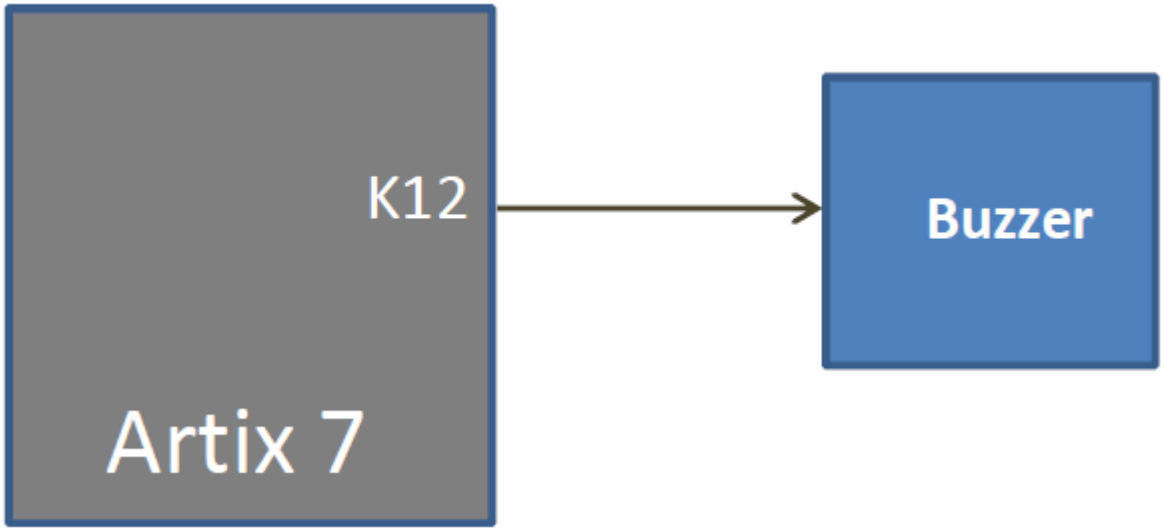
- Stereo Jack
  - Stereo Audio Jack with low pass filter is connected to the FPGA I/O lines on the EDGE Board
  - Stereo Jack provides delta-sigma audio output



```
# Audio Jack
set_property -dict { PACKAGE_PIN G11   IOSTANDARD LVCMOS33 } [get_ports { Audio_L }];
set_property -dict { PACKAGE_PIN G15   IOSTANDARD LVCMOS33 } [get_ports { Audio_R }];
```


EDGE ARTIX 7 FPGA BOARD

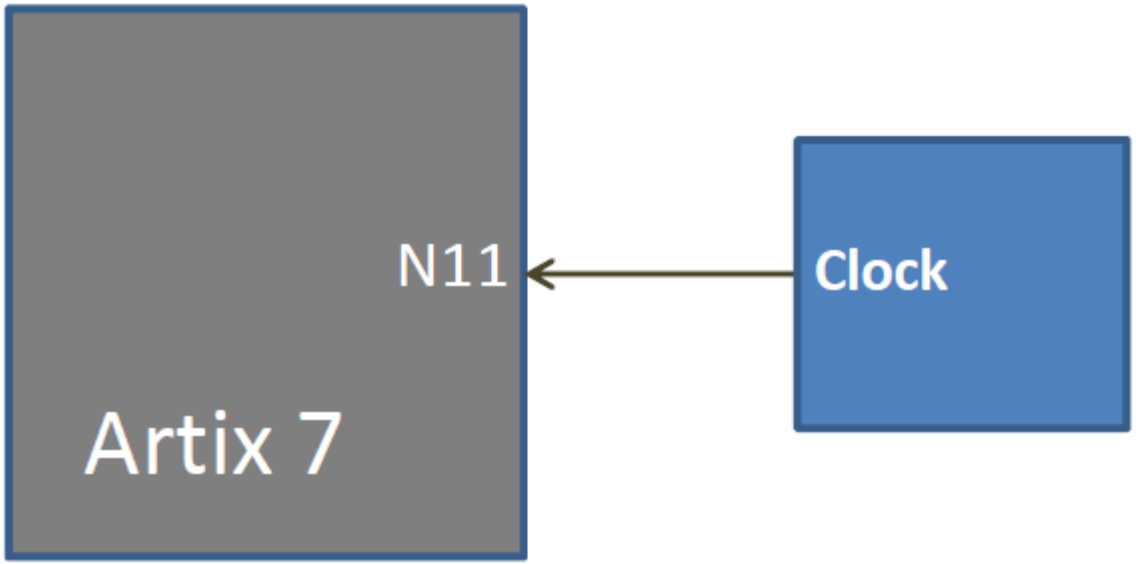
- Buzzer
  - The Edge board contains a piezo buzzer interface with FPGA through a transistor
  - 5v Buzzer is used to provide an alert tone
  - Buzzer's resonant frequency is 3.8 kHz (where you can expect its best performance)



```
# Buzzer
set_property -dict { PACKAGE_PIN K12 IOSTANDARD LVCMOS33 } [get_ports {Buzzer}];
```

EDGE ARTIX 7 FPGA BOARD

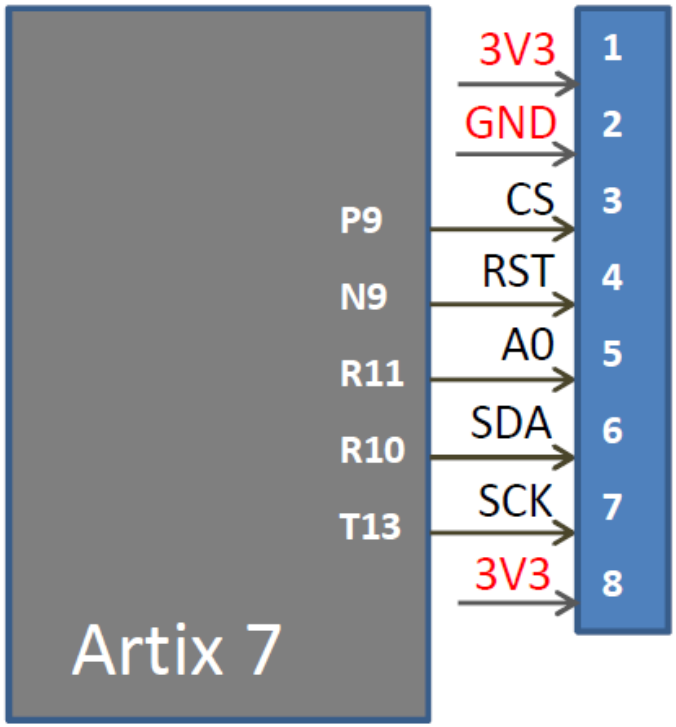
- Clock
  - The Edge board contains a 50 MHz Oscillator to provide clock input to the FPGA
  - The input clock can drive MMCMs or PLL to generate clocks of various frequencies and with known phase relationships that may be needed throughout a design




```
# Clock signal
set_property -dict { PACKAGE_PIN N11    IOSTANDARD LVCMOS33 } [get_ports { clk }];
```

EDGE ARTIX 7 FPGA BOARD

- TFT Display
  - The EDGE Board contains a TFT display interface at the J10 connector
  - TFT display communicates with FPGA through SPI protocol
  - SPI TFT is made of ST7732S SPI controller with 160x128 Display

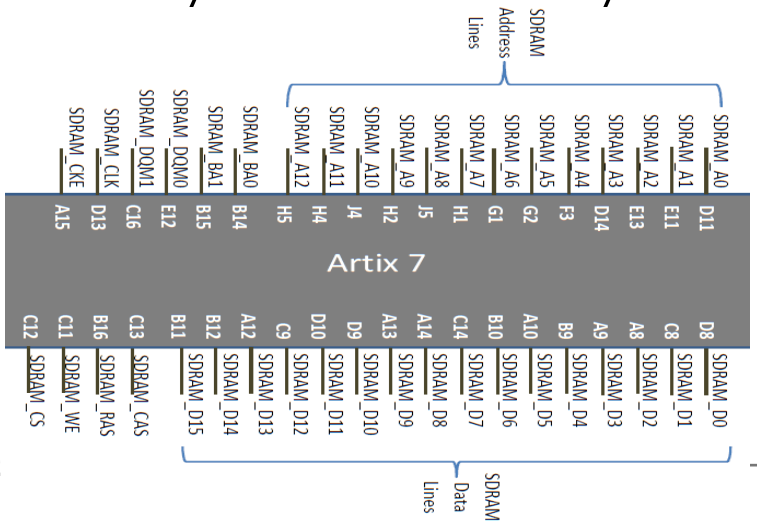


J10 Connector

```
# SPI TFT 1.8 inch
set_property -dict { PACKAGE_PIN T13 IOSTANDARD LVCMOS33 } [get_ports {tft_sck}];
set_property -dict { PACKAGE_PIN R10 IOSTANDARD LVCMOS33 } [get_ports {tft_sdi}];
set_property -dict { PACKAGE_PIN R11 IOSTANDARD LVCMOS33 } [get_ports {tft_dc}];
set_property -dict { PACKAGE_PIN N9  IOSTANDARD LVCMOS33 } [get_ports {tft_reset}];
set_property -dict { PACKAGE_PIN P9  IOSTANDARD LVCMOS33 } [get_ports {tft_cs}];
```

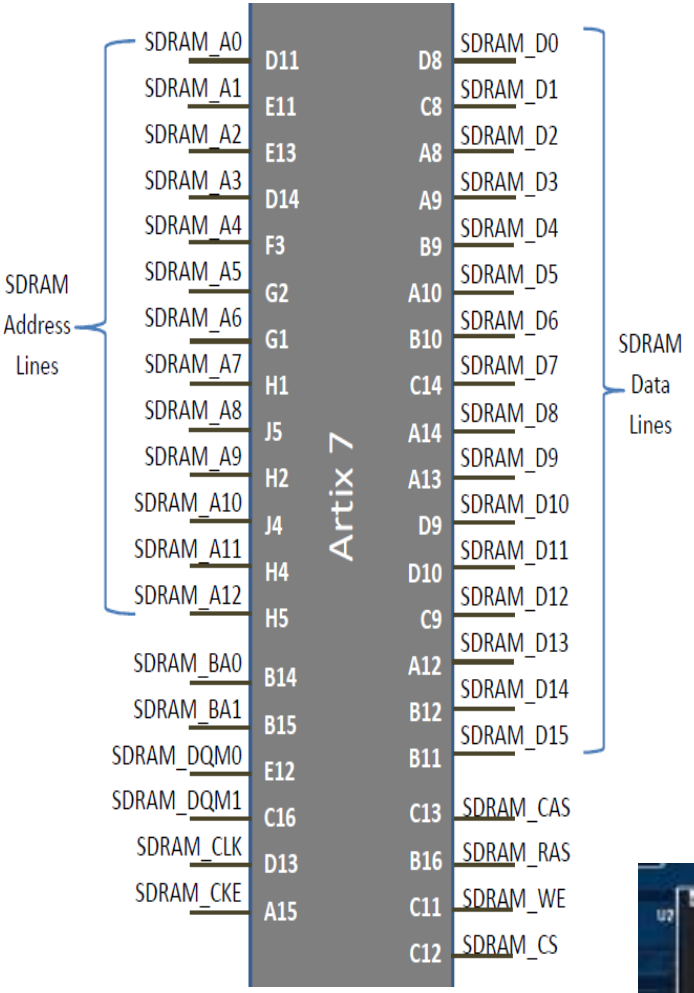
EDGE ARTIX 7 FPGA BOARD

- SDRAM
  - The EDGE Board upgraded with 32MB of SDRAM. The 32MB SDRAM is a high-speed CMOS, dynamic random-access memory containing 268,435,456 bits
  - It is internally configured as a quad-bank DRAM with a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK)
  - Each of the x16's 67,108,864-bit banks is organized as 8192 rows by 512 columns by 16 bits



EDGE ARTIX 7 FPGA BOARD

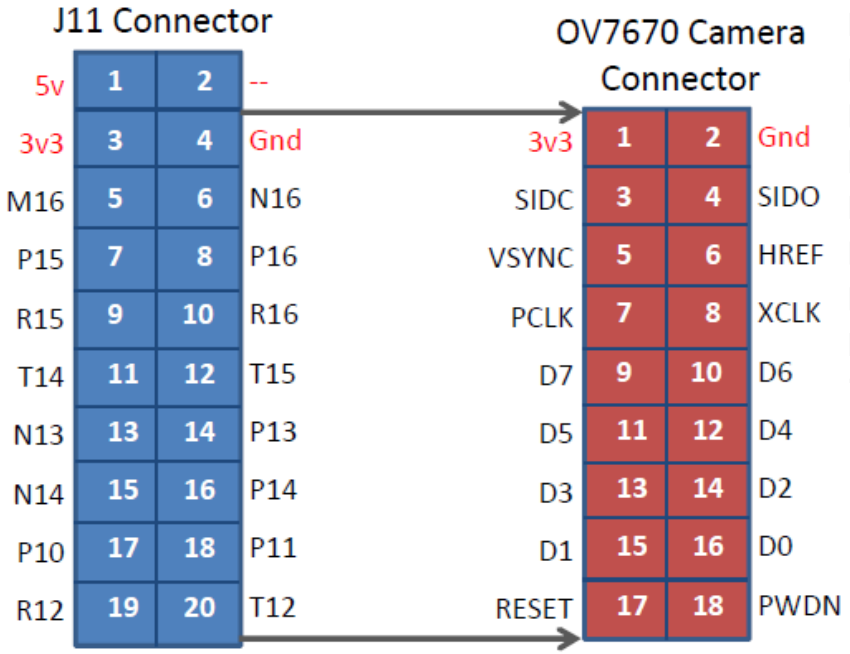
- SDRAM




```
#256Mb SDRAM (Only available with latest version of board)
set_property -dict { PACKAGE_PIN D8  IOSTANDARD LVCMOS33 } [get_ports { sdram_dq[0] }];
set_property -dict { PACKAGE_PIN C8  IOSTANDARD LVCMOS33 } [get_ports { sdram_dq[1] }];
set_property -dict { PACKAGE_PIN A8  IOSTANDARD LVCMOS33 } [get_ports { sdram_dq[2] }];
set_property -dict { PACKAGE_PIN A9  IOSTANDARD LVCMOS33 } [get_ports { sdram_dq[3] }];
set_property -dict { PACKAGE_PIN B9  IOSTANDARD LVCMOS33 } [get_ports { sdram_dq[4] }];
set_property -dict { PACKAGE_PIN A10 IOSTANDARD LVCMOS33 } [get_ports { sdram_dq[5] }];
set_property -dict { PACKAGE_PIN B10 IOSTANDARD LVCMOS33 } [get_ports { sdram_dq[6] }];
set_property -dict { PACKAGE_PIN C14 IOSTANDARD LVCMOS33 } [get_ports { sdram_dq[7] }];
set_property -dict { PACKAGE_PIN A14 IOSTANDARD LVCMOS33 } [get_ports { sdram_dq[8] }];
set_property -dict { PACKAGE_PIN A13 IOSTANDARD LVCMOS33 } [get_ports { sdram_dq[9] }];
set_property -dict { PACKAGE_PIN D9  IOSTANDARD LVCMOS33 } [get_ports { sdram_dq[10] }];
set_property -dict { PACKAGE_PIN D10 IOSTANDARD LVCMOS33 } [get_ports { sdram_dq[11] }];
set_property -dict { PACKAGE_PIN C9  IOSTANDARD LVCMOS33 } [get_ports { sdram_dq[12] }];
set_property -dict { PACKAGE_PIN A12 IOSTANDARD LVCMOS33 } [get_ports { sdram_dq[13] }];
set_property -dict { PACKAGE_PIN B12 IOSTANDARD LVCMOS33 } [get_ports { sdram_dq[14] }];
set_property -dict { PACKAGE_PIN B11 IOSTANDARD LVCMOS33 } [get_ports { sdram_dq[15] }];#MSB

set_property -dict { PACKAGE_PIN D11 IOSTANDARD LVCMOS33 } [get_ports { sdram_addr[0] }];#LSB
set_property -dict { PACKAGE_PIN E11 IOSTANDARD LVCMOS33 } [get_ports { sdram_addr[1] }];
set_property -dict { PACKAGE_PIN E13 IOSTANDARD LVCMOS33 } [get_ports { sdram_addr[2] }];
set_property -dict { PACKAGE_PIN D14 IOSTANDARD LVCMOS33 } [get_ports { sdram_addr[3] }];
set_property -dict { PACKAGE_PIN F3  IOSTANDARD LVCMOS33 } [get_ports { sdram_addr[4] }];
set_property -dict { PACKAGE_PIN G2  IOSTANDARD LVCMOS33 } [get_ports { sdram_addr[5] }];
set_property -dict { PACKAGE_PIN G1  IOSTANDARD LVCMOS33 } [get_ports { sdram_addr[6] }];
set_property -dict { PACKAGE_PIN H1  IOSTANDARD LVCMOS33 } [get_ports { sdram_addr[7] }];
set_property -dict { PACKAGE_PIN J5  IOSTANDARD LVCMOS33 } [get_ports { sdram_addr[8] }];
set_property -dict { PACKAGE_PIN H2  IOSTANDARD LVCMOS33 } [get_ports { sdram_addr[9] }];
set_property -dict { PACKAGE_PIN J4  IOSTANDARD LVCMOS33 } [get_ports { sdram_addr[10] }];
set_property -dict { PACKAGE_PIN H4  IOSTANDARD LVCMOS33 } [get_ports { sdram_addr[11] }];
set_property -dict { PACKAGE_PIN H5  IOSTANDARD LVCMOS33 } [get_ports { sdram_addr[12] }];


set_property -dict { PACKAGE_PIN B14 IOSTANDARD LVCMOS33 } [get_ports { sdram_ba[0] }];
set_property -dict { PACKAGE_PIN B15 IOSTANDARD LVCMOS33 } [get_ports { sdram_ba[1] }];

set_property -dict { PACKAGE_PIN E12 IOSTANDARD LVCMOS33 } [get_ports { sdram_dqm[0] }];
set_property -dict { PACKAGE_PIN C16 IOSTANDARD LVCMOS33 } [get_ports { sdram_dqm[1] }];

set_property -dict { PACKAGE_PIN D13 IOSTANDARD LVCMOS33 } [get_ports { sdram_clk }];
set_property -dict { PACKAGE_PIN A15 IOSTANDARD LVCMOS33 } [get_ports { sdram_cke }];
set_property -dict { PACKAGE_PIN C12 IOSTANDARD LVCMOS33 } [get_ports { sdram_cs_n }];
set_property -dict { PACKAGE_PIN C11 IOSTANDARD LVCMOS33 } [get_ports { sdram_we_n }];
set_property -dict { PACKAGE_PIN C13 IOSTANDARD LVCMOS33 } [get_ports { sdram_cas_n }];
set_property -dict { PACKAGE_PIN B16 IOSTANDARD LVCMOS33 } [get_ports { sdram_ras_n }];
```

EDGE ARTIX 7 FPGA BOARD

- 20 Pin Expansion Connector / CMOS Camera Interface
  - Expansion connector J11 provides 16 I/O lines from Artix 7 FPGA to the external interface
  - Note: To interface OV7670 CMOS Camera with EDGE Board. Leave pin1 and pin2 unconnected
  - Connect pin3 of expansion connector to pin1 of CMOS Camera




```
# CMOS Camera
set_property -dict { PACKAGE_PIN M16 IOSTANDARD LVCMOS33} [get_ports {ov7670_sioc}];
set_property -dict { PACKAGE_PIN N16 IOSTANDARD LVCMOS33} [get_ports {ov7670_siod}];
set_property -dict { PACKAGE_PIN P15 IOSTANDARD LVCMOS33} [get_ports {ov7670_vsync}];
set_property -dict { PACKAGE_PIN P16 IOSTANDARD LVCMOS33} [get_ports {ov7670_href}];
set_property -dict { PACKAGE_PIN R15 IOSTANDARD LVCMOS33} [get_ports {ov7670_pclk}];
set_property -dict { PACKAGE_PIN R16 IOSTANDARD LVCMOS33} [get_ports {ov7670_xclk}];
set_property -dict { PACKAGE_PIN T14 IOSTANDARD LVCMOS33} [get_ports {ov7670_data[7]}];
set_property -dict { PACKAGE_PIN T15 IOSTANDARD LVCMOS33} [get_ports {ov7670_data[6]}];
set_property -dict { PACKAGE_PIN N13 IOSTANDARD LVCMOS33} [get_ports {ov7670_data[5]}];
set_property -dict { PACKAGE_PIN P13 IOSTANDARD LVCMOS33} [get_ports {ov7670_data[4]}];
set_property -dict { PACKAGE_PIN N14 IOSTANDARD LVCMOS33} [get_ports {ov7670_data[3]}];
set_property -dict { PACKAGE_PIN P14 IOSTANDARD LVCMOS33} [get_ports {ov7670_data[2]}];
set_property -dict { PACKAGE_PIN P10 IOSTANDARD LVCMOS33} [get_ports {ov7670_data[1]}];
set_property -dict { PACKAGE_PIN P11 IOSTANDARD LVCMOS33} [get_ports {ov7670_data[0]}];
set_property -dict { PACKAGE_PIN R12 IOSTANDARD LVCMOS33} [get_ports {ov7670_reset}];
set_property -dict { PACKAGE_PIN T12 IOSTANDARD LVCMOS33} [get_ports {ov7670_pwdn}];
```