Abbreviations

ABI Application Binary Interface

ALU Arithmetic Logic Unit

AMAT Average Memory Access Time

API Application Programming Interface

AR Access Rights

ARN Architectural Register Number

ARSet Architectural Register Set

ASE Application-Specific Extension

ASID Address Space ID

BHR Branch History Register

BHT Branch History Table

BIA Branch Instruction Address

BL BitLine

BS Block Size

BTA Branch Target Address

BTB Branch Target Buffer

BTFNT Backwards Taken, Forwards Not-Taken

CDB Common Data Bus

CISC Complex Instruction Set Computer

CMOS Complementary Metal-Oxide-Semiconductor

CPI Cycles Per Instruction

CPU Central Processing Unit

DDR Double Data Rate

DF Data Flow

DM Data Memory

DMA Direct Memory Access

DMS Distributed Memory System

DRAM Dynamic Random Access Memory

DSP Digital Signal Processor

EPI Energy Per Instruction

EX Execute

FIFO First In First Out

FLB Finished Load Buffer

FLOPS Floating point Operations Per Second

FN Frame Number

FP Floating Point

FPGA Field Programmable Gate Array

GHR Global History Register

GPR General-purpose Register

GPU Graphic Processing Unit

HDD HardDisk Drive

HD High Definition

HDL Hardware Description Language

HLL High Level Language

HMU	Hazard Management Unit
HR	Hit Rate
HVL	Hardware Verification Language
HW	HardWare
IaaS	Infrastructure-as-a-Service
IC	Instruction Count
ID/OF	Instruction Decode/Operand Fetch
IF	Instruction Fetch
ILP	Instruction Level Parallelism
IM	Instruction Memory
I/O	Input/Output
IoT	Internet of Things
IPC	Instructions Per clock Cycle
IPS	Instructions Per Second
ISA	Instruction Set Architecture
LAR	Lock Address Register
LF	Lock flag
LFU	Least Frequently Used
LRU	Least Recently Used
lsb	least significant bit
LSB	Least Significant Byte
MC	Memory Controller
MEM	Memory

MESI Modified Exclusive Shared Invalid

MIPS Microprocessor without Interlocked Pipelined Stages

MIPS Million Instructions Per Second

MMU Memory Management Unit

MOSFET Metal-Oxide-Semiconductor Field-Effect Transistor

MPI Message Passing Interface

MR Miss Rate

msb most significant bit

MSB Most Significant Byte

NT Not Taken

NUMA Non-Uniform Memory Access

OS Operating System

PA Physical address

PC Processor Consistency

PC Program Counter

PCI Peripheral Component Interconnect

PHT Pattern History Table

PLA Programmable Logic Array

PN Page Number

PPN Physical Page Number

PPO Physical Page Offset

PSO Partial Store Ordering

PTBR Page Table Base Register

PTE Page Table Entry

RAM Random Access Memory

RAS Return Address Stack

RAT Register Alias Table

RAW Read After Write

RF Register File

RISC Reduced Instruction Set Computer

ROB Reorder buffer

ROM Read Only Memory

RRN Rename Register Number

RRSet Rename Register Set

RS Reservation Station

RTL Register transfer level

RWM Read-Write Memory

SaaS Software-as-a-Service

SIMD Single Instruction (stream), Multiple Data (streams)

SMP Symmetric MultiProcessor

SMS Shared Memory System

SNT Strongly Not Taken

SPEC Standard Performance Evaluation Corporation

SPI Stalls Per Instruction

SP Cache Memory

SP Stack Pointer

SRAM Static Random Access Memory

SSD Solid State Drive

SSE Streaming SIMD Extensions

SW SoftWare

TLB Translation Lookaside Buffer

TSO Total Store Ordering

UMA Uniform Memory Access

VA Virtual address

VHDL VHSIC Hardware Description Language

VHSIC Very High Speed Integrated Circuits

VLSI Very-Large-Scale Integration

WAR Write After Read

WAW Write After Write

WB Write-Back

WB Write Buffer

WL Word Line

WNT Weakly Not Taken

WT Write-Through