Advanced Computer Architecture & Advanced Microprocessor System

2ND Semester 2023

Course Information

Instructor

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Research Portals:

https://www.researchgate.net/profile/Dennis-Gookyi

https://scholar.google.com/citations?user=KfF-atoAAAAJ&hl=en

https://orcid.org/0000-0002-6622-0538

Class Meeting

Morning Session: Thursday 9:00 AM – 3:00 PM

Evening Session: Thursday & Friday 5:30 PM – 8:30 PM

Textbooks

1. David A. Patterson, John L. Hennessy: *Computer Organisation and Design, The Hardware/Software Interface – RISC-V Edition*

2 Ming-Bo Lin*: Digital System Designs and Practices Using Verilog HDL and FPGAs*

Course Site

https://github.com/dennisgookyi/Computer-Architecture-and-Microprocessor-System-Class

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Overview

The Advanced Computer Architecture and Advanced Microprocessor courses will be combined into a single course with the end goal of equipping students with the necessary information to design, simulate, and implement an open-sourced RISC-V-based processor on an FPGA board using commercial hardware design CAD tools and Hardware Description Languages.

Schedules (The schedule is subject to change)

Lecture	Topic
01	Introduction to FPGAs and Labs
02	Hardware Design Tools Overview and Installation
03	Combinational Logic Design
04	Sequential Logic Design
05	Hardware Description Languages and Verilog
06	CPU Execution Cycle and Introduction to RISC-V ISA
07	RISC-V Single Cycle Architecture
08	Design and Implementation of a RISC-V Single Cycle Processor Using Verilog HDL
09	RISC-V Multi Cycle Architecture
10	RISC-V Software Toolchain Ecosystem
11	System-on-Chip (SoC) Design with RISC-V Processor
12	Memory Organization and Technology

Homework

Homework will be posted on the site. Check regularly.

Projects

Projects will be posted site. Check regularly.

Useful Links

1. https://riscv.org
2. https://en.wikichip.org/wiki/WikiChip
3. https://allaboutfpga.com/product/edge-artix-7-fpga-development-board/
4. https://riscv.org/wp-content/uploads/2017/05/riscv-spec-v2.2.pdf
5. https://www.elsevier.com/__data/assets/pdf_file/0011/297533/RISC-V-Reference-Data.pdf#RISC-V%20Reference%20Data