Advanced Computer Architecture & Advanced Microprocessor System

2ND Semester 2023

LAB

Release Date

27/07/2023

Due Date

Morning Session: 03/08/2023 @ 9:00 AM

Evening Session: 03/08/2023 @ 5:30 PM

(**Note: Those outside Accra should send their answers to my email address**)

Overview

This lab will help you explore the Vivado tool which will be used for implementing our digital logic designs.

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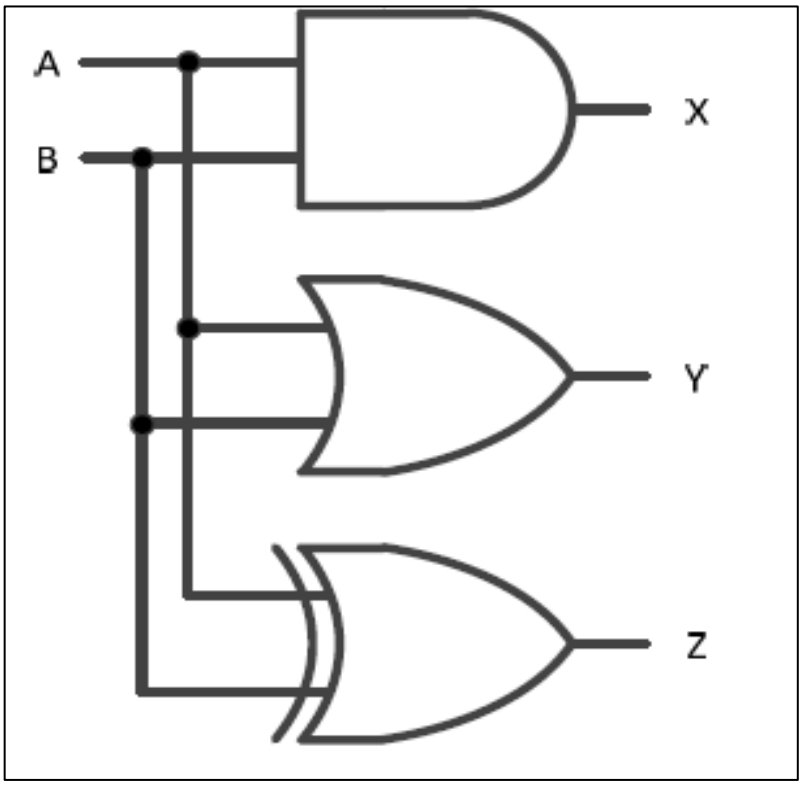
LAB Instructions (Record your results in a PPT file)

1. Install the Vivado tool on your local machines by following the Guide in Lecture L01_b (Vivado Installation User Guide)
2. Implement the digital logic below using the Vivado tool by following the steps in Lecture L01_d (Vivado-based FPGA User Guide)



A. Write the Verilog code for the digital logic
   i. Synthesize the design and record the synthesis results in a PPT file
   ii. Capture the synthesis schematic in a PPT file
B. Write the Verilog Testbench code for the digital logic
   i. Simulate the design and capture the results in a PPT file