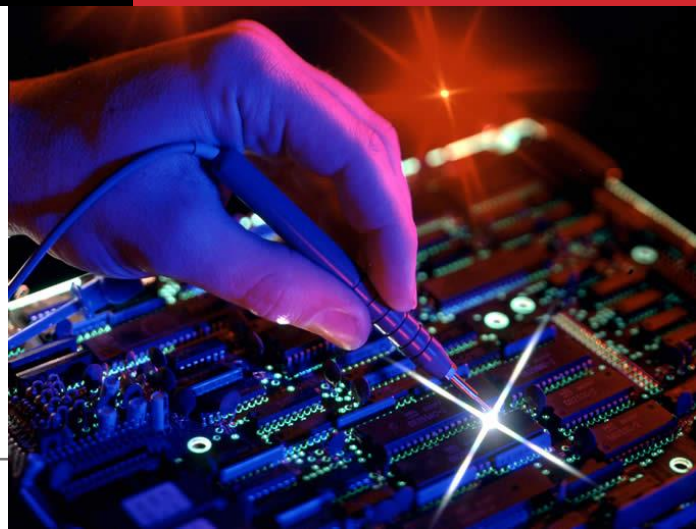
Advanced Computer Architecture & Advanced Microprocessor System

VIVADO BASED ARTIX 7 FPGA BOARD USER GUIDE

Dennis A. N. Gookyi



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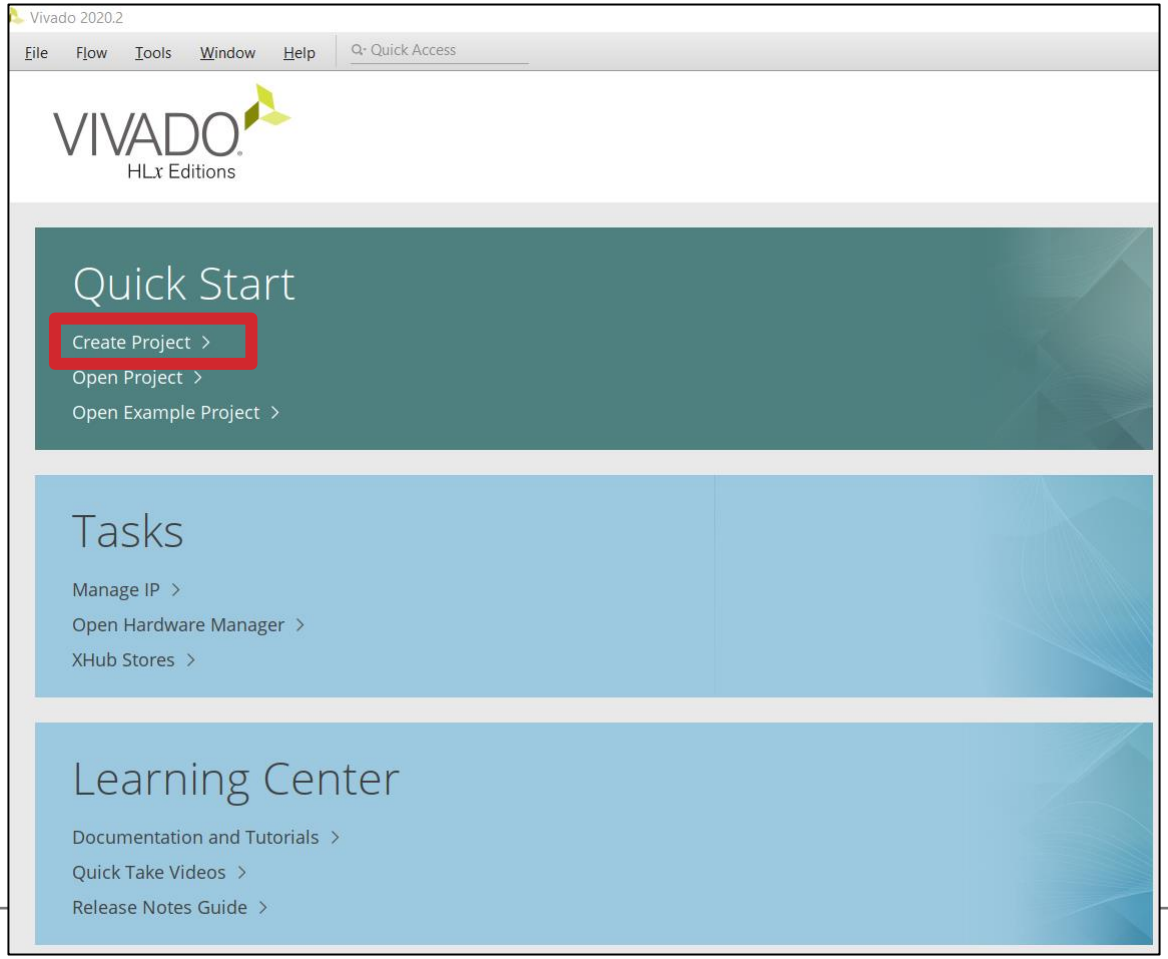
DESIGN EXAMPLE

- Verilog code and Testbench
  - Gates design
    - AND gate
    - OR gate
    - XOR gate

DESIGN EXAMPLE

- Vivado project
  - Creating an new project



DESIGN EXAMPLE

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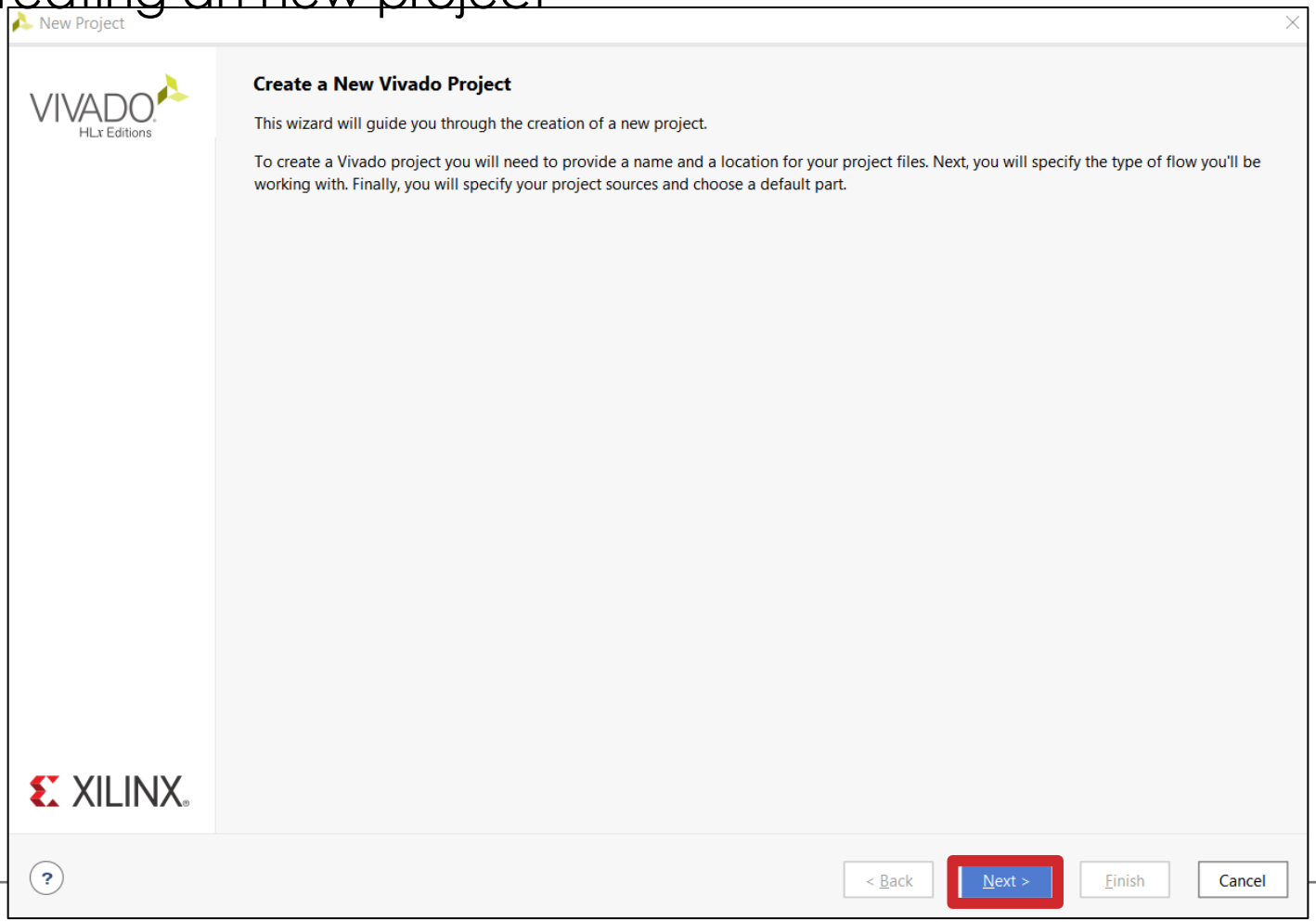
  - Creating an new project



DESIGN EXAMPLE

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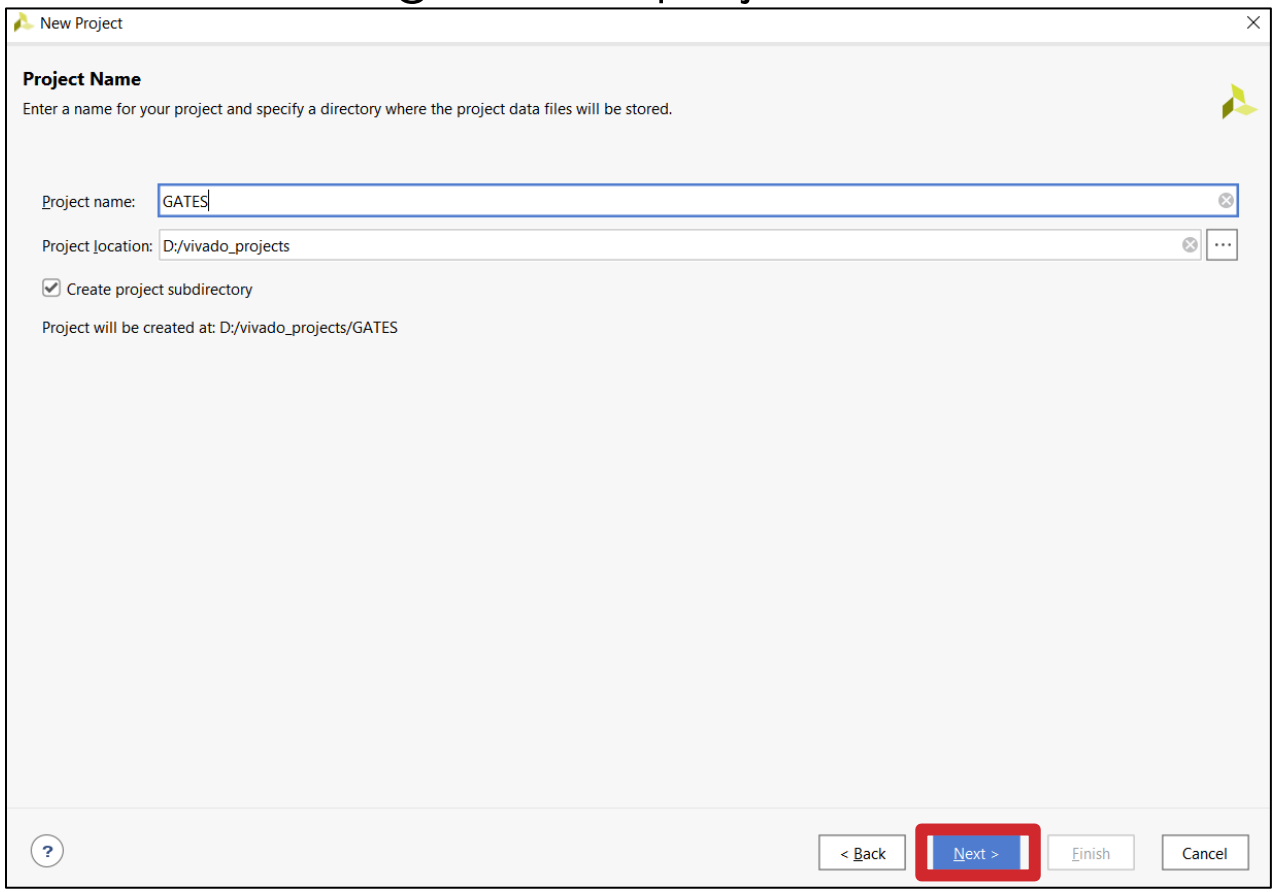
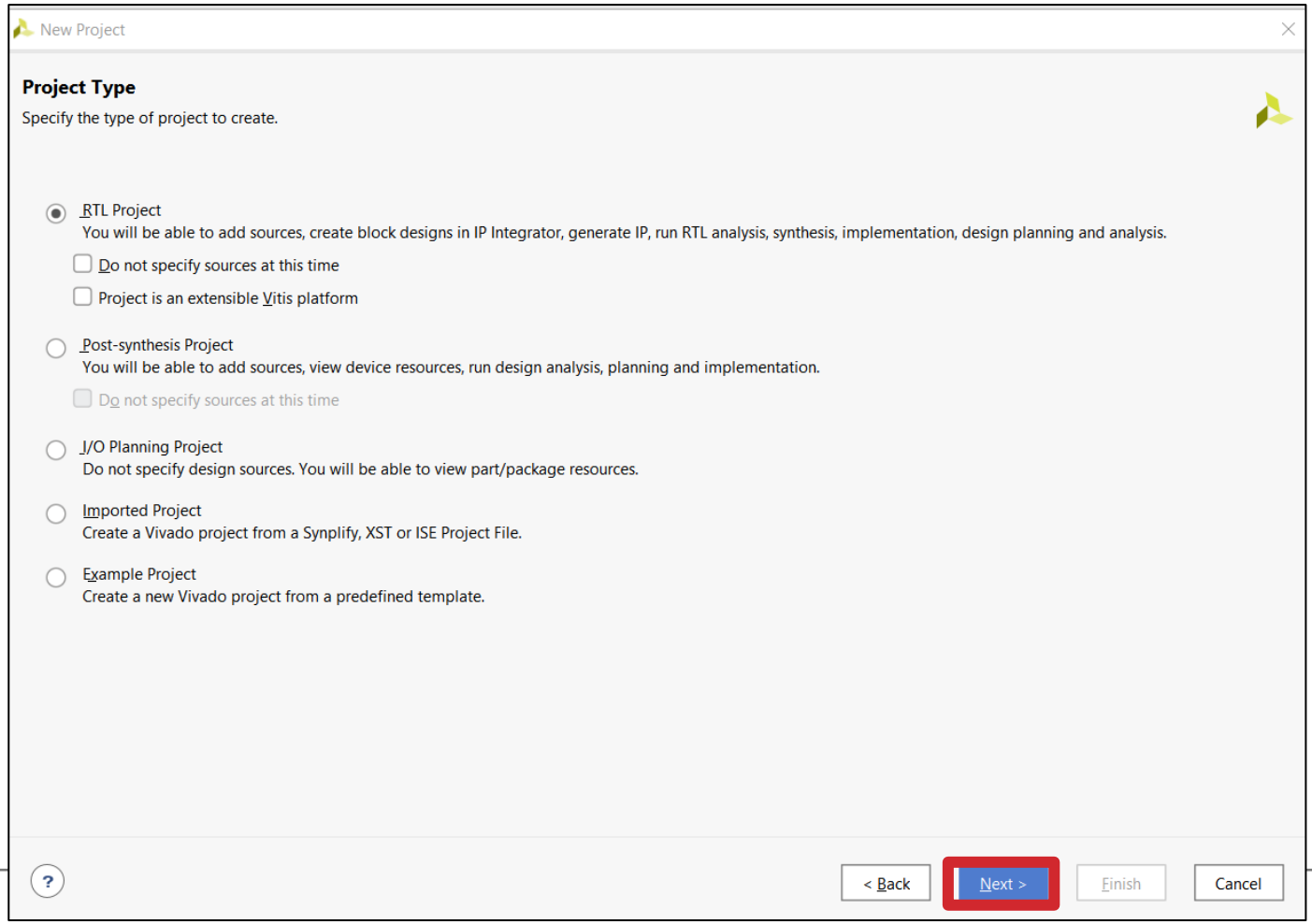


Project name
→ must start with an alphabet
→ can include "_" and numbers

Location
→location of the project
→subfolders can be created

DESIGN EXAMPLE

- Vivado project
  - Creating an new project



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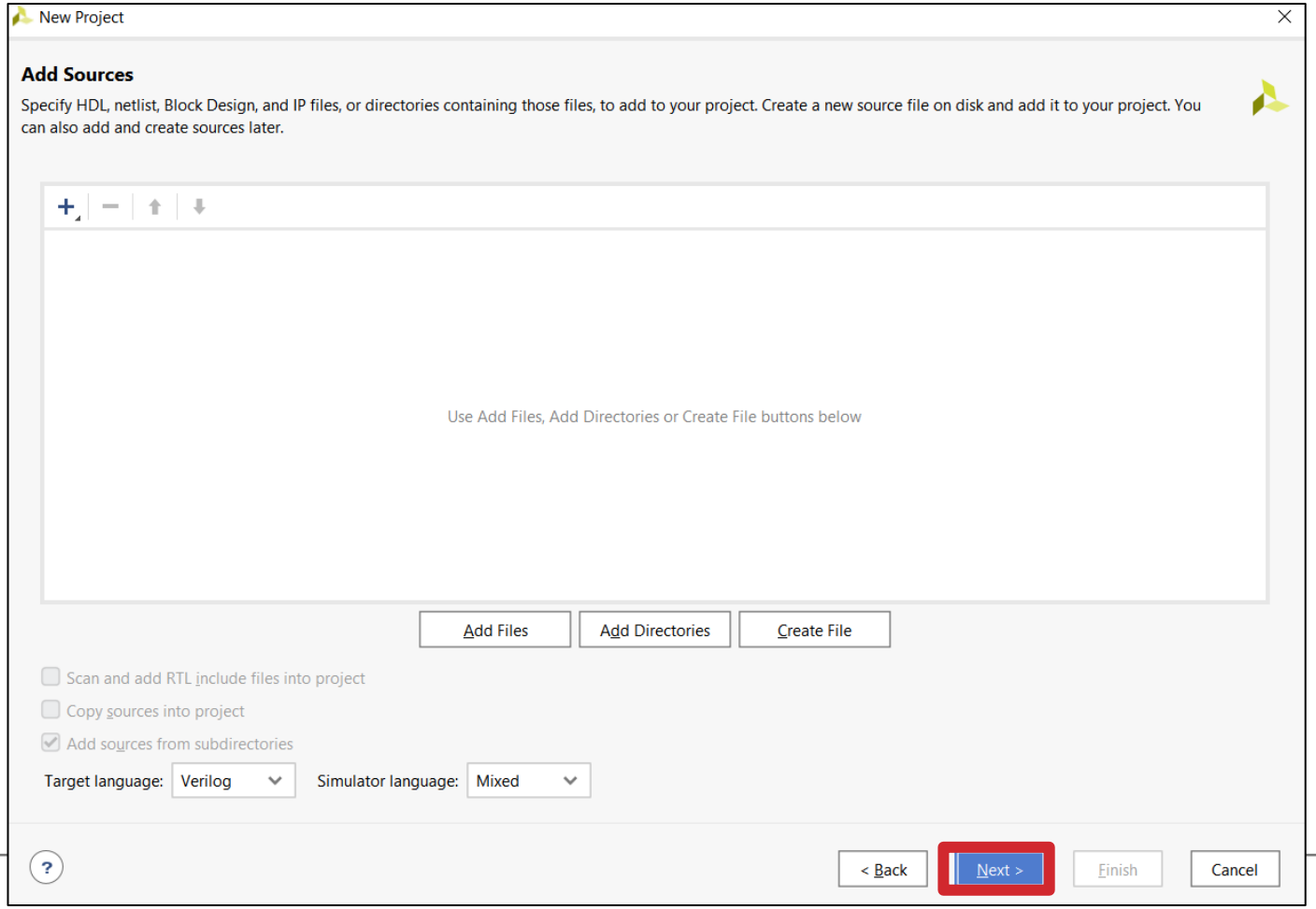

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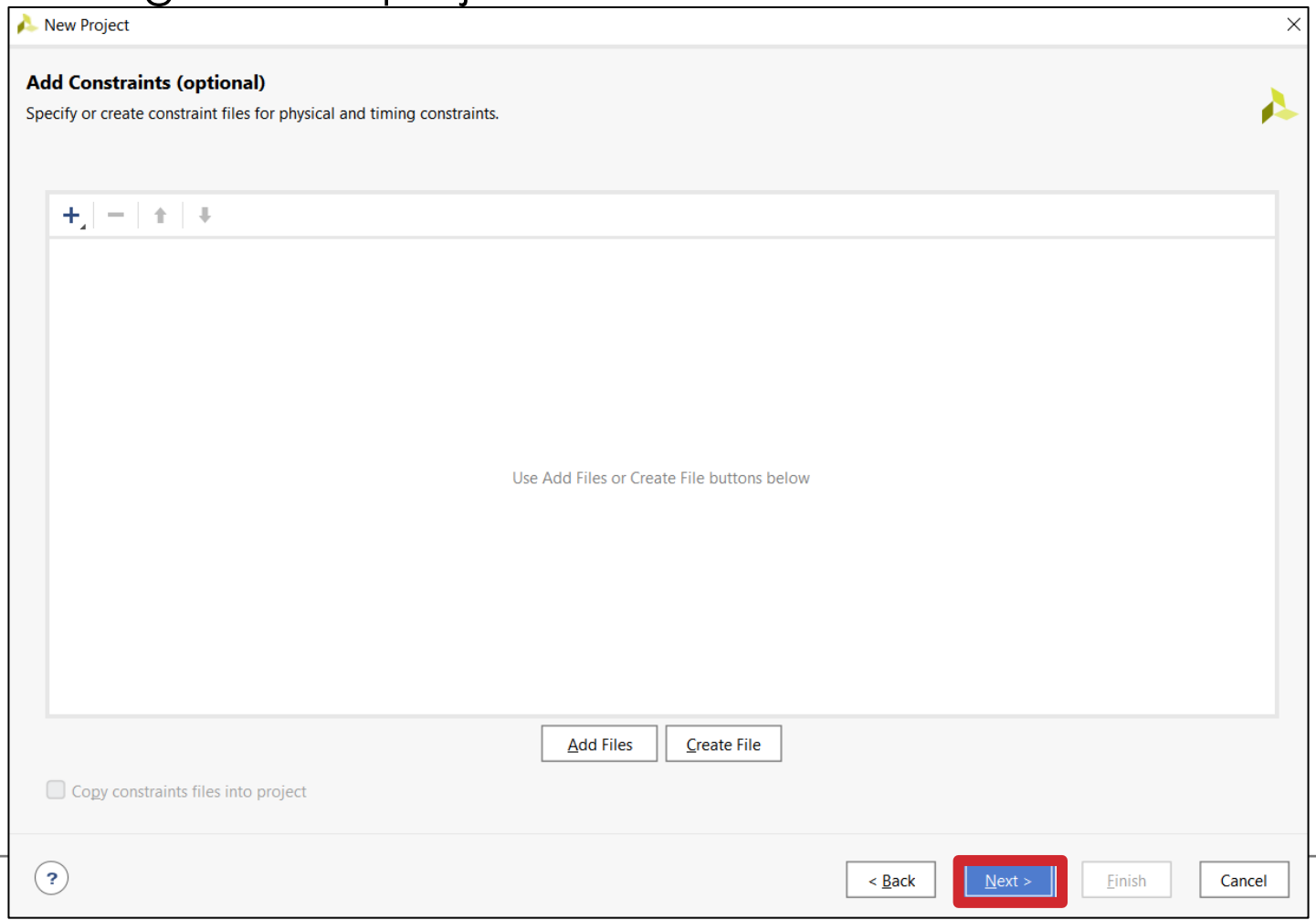
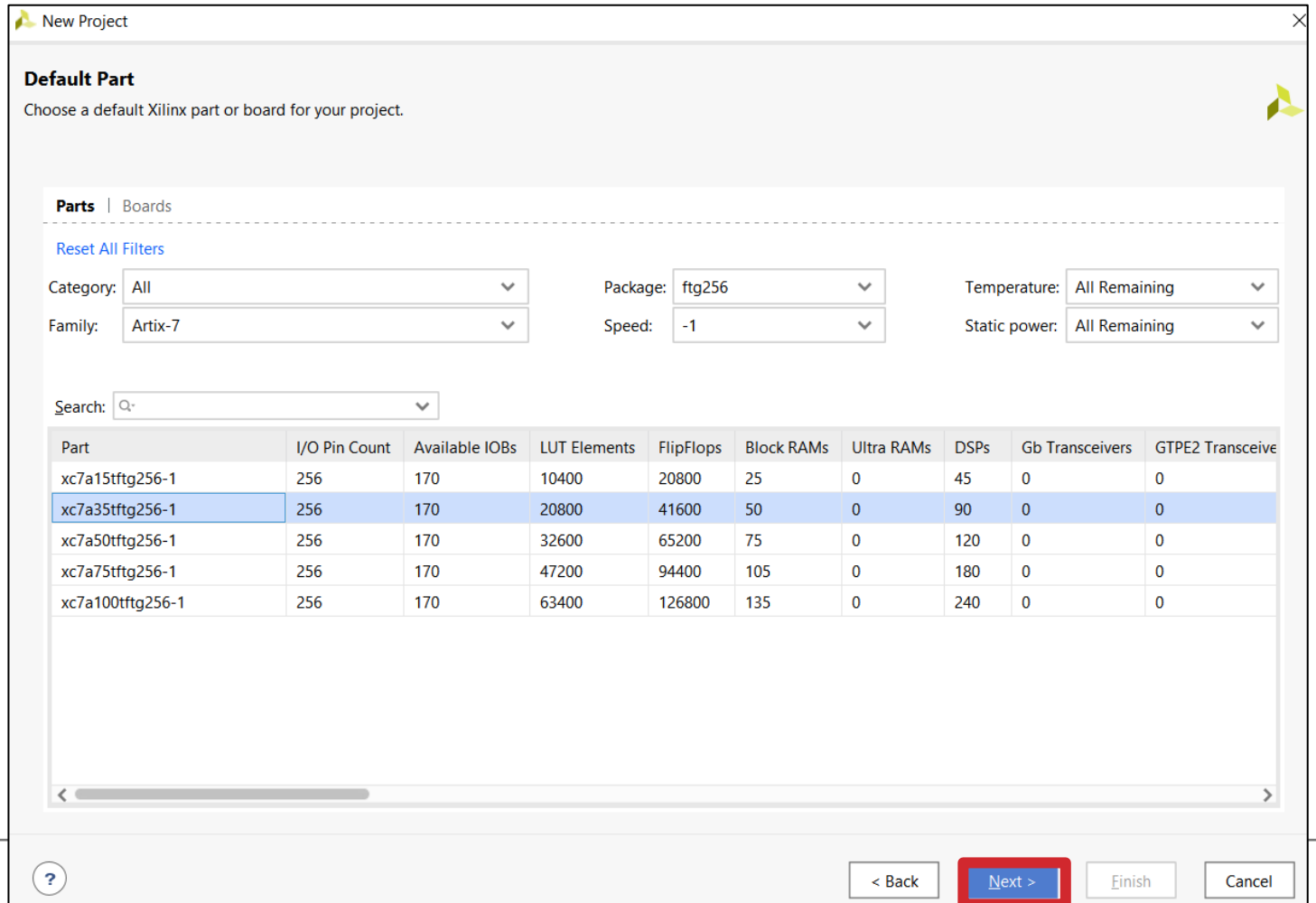


DESIGN EXAMPLE

- Vivado project
  - Creating an new project

FPGA Device: Xc7a35tftg256-1



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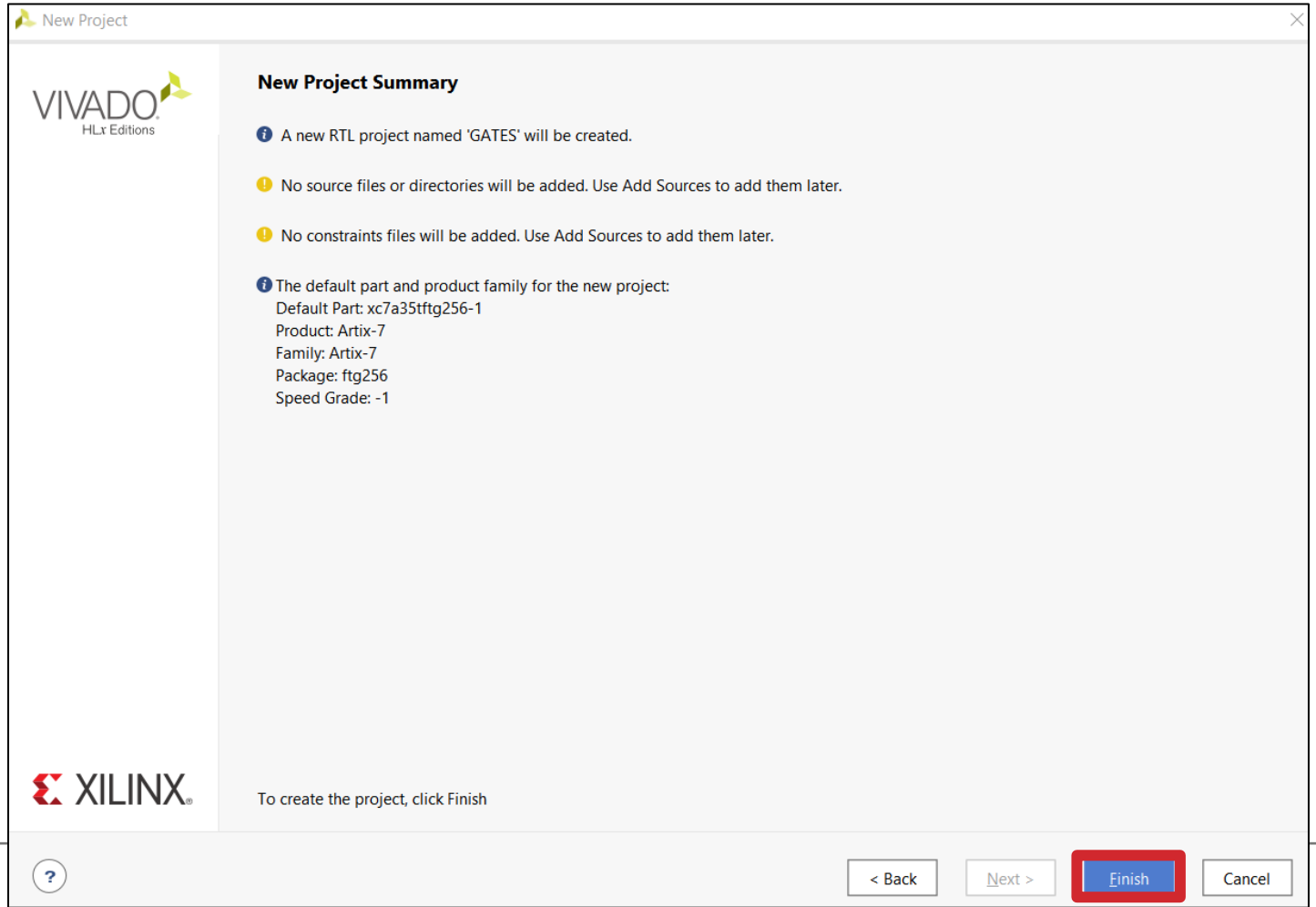

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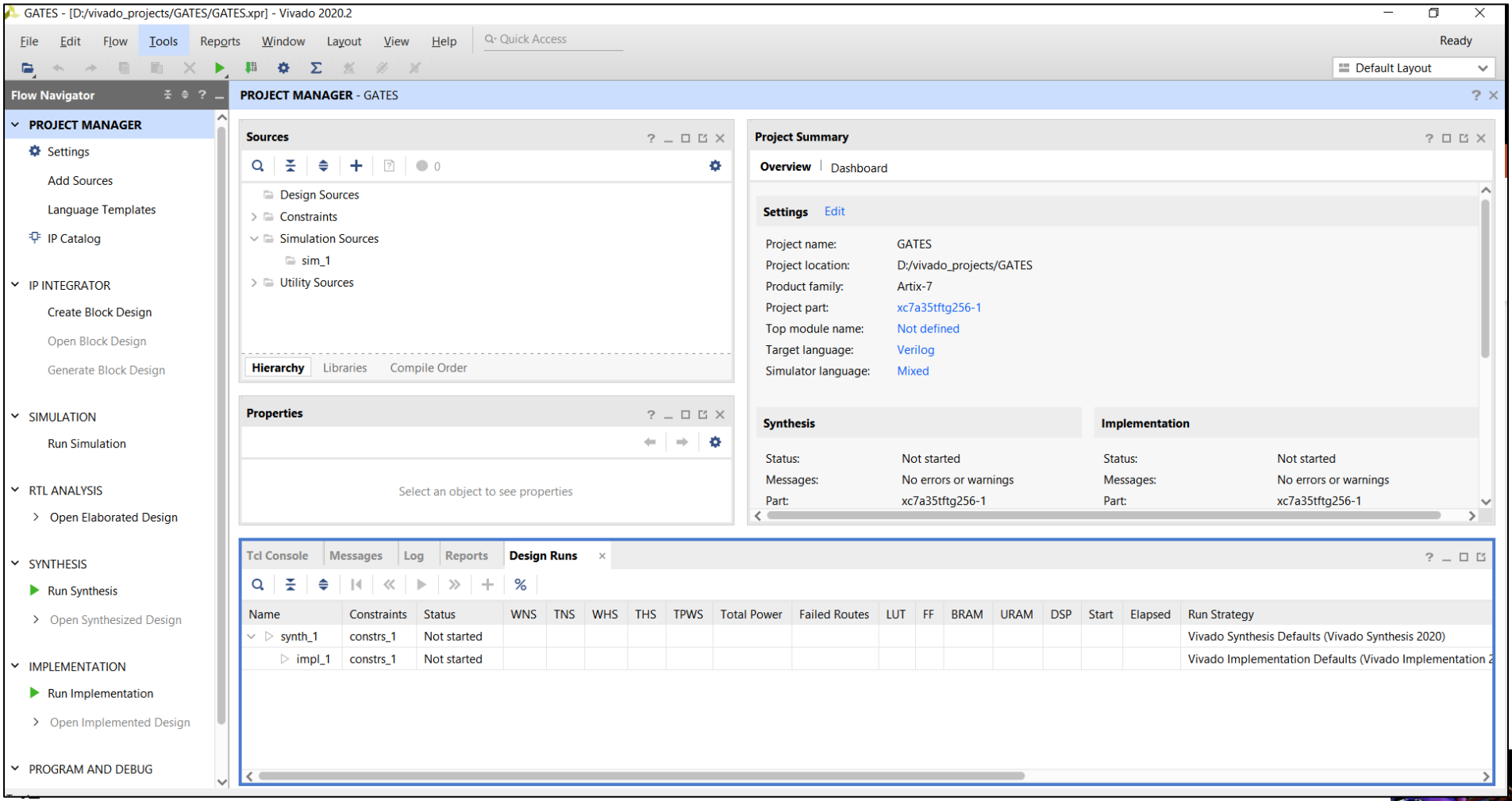

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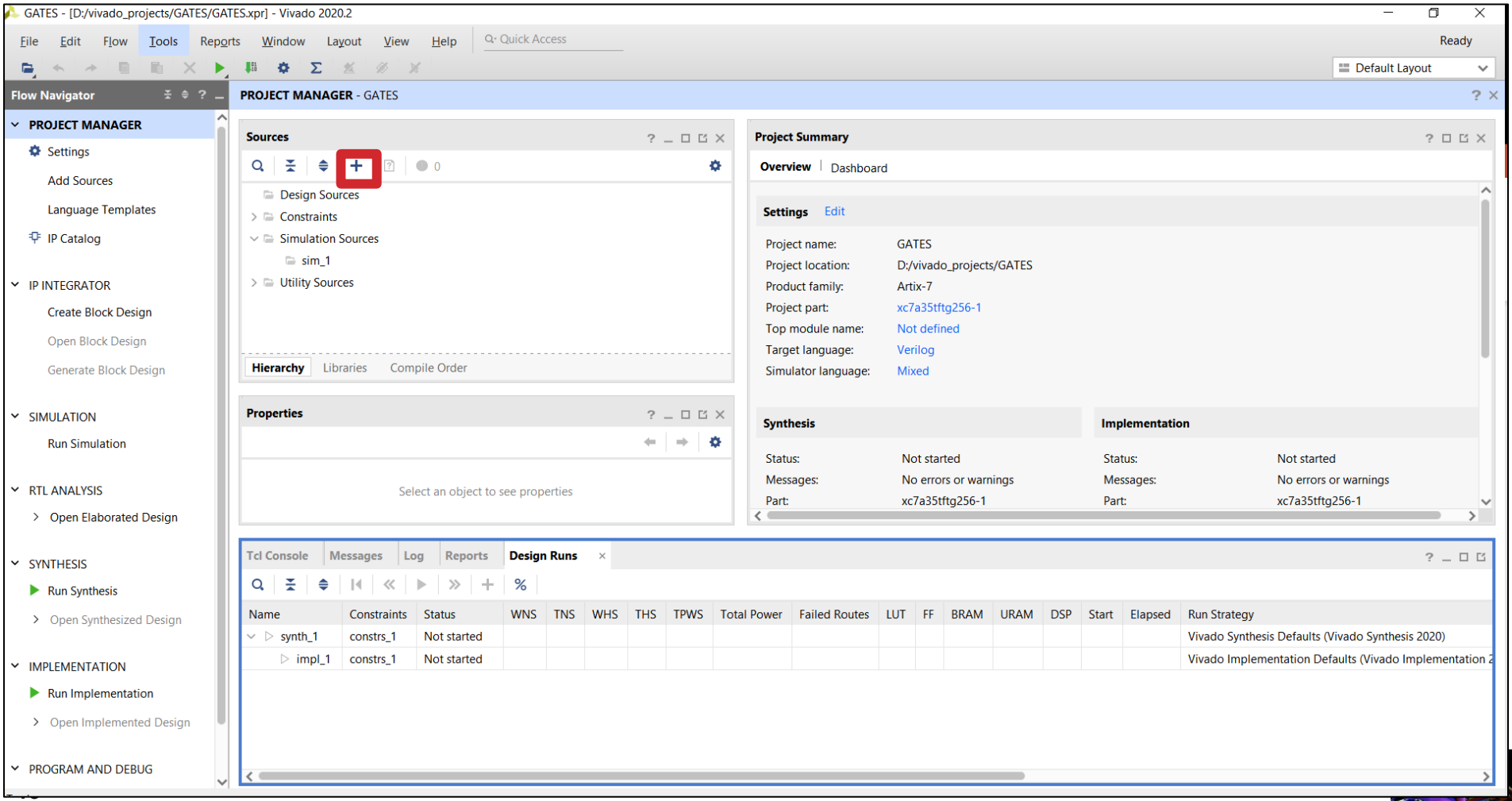

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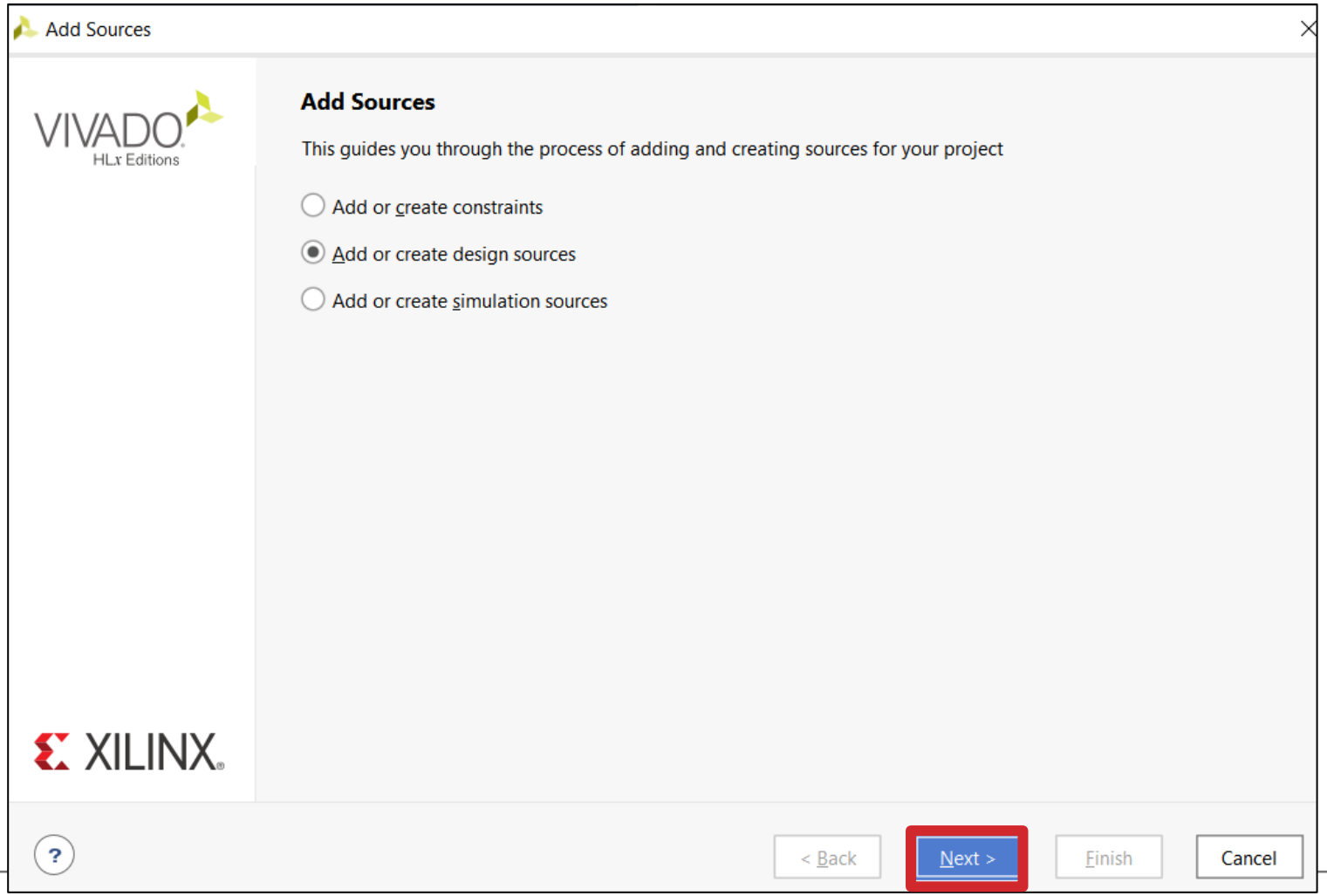

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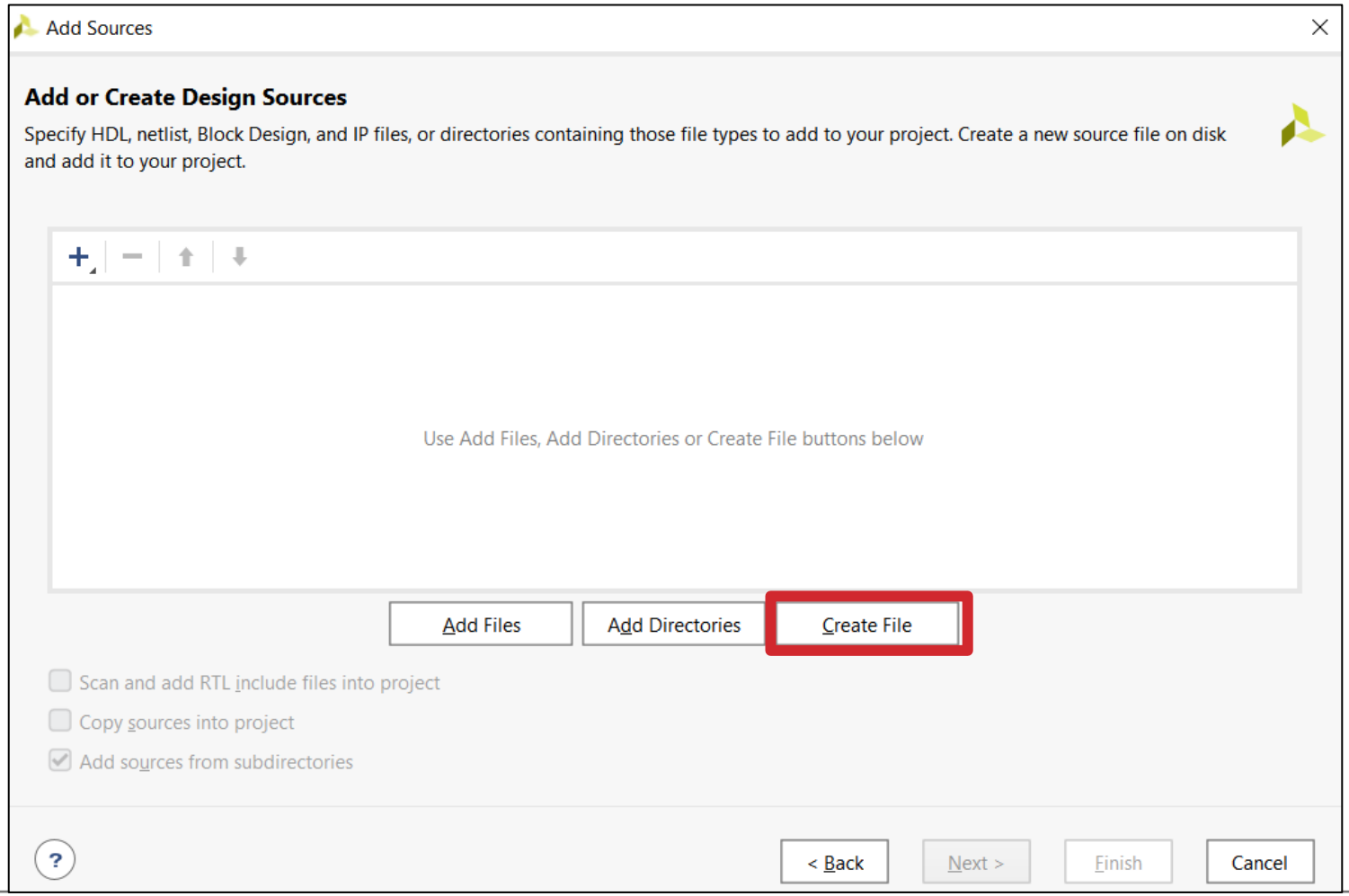

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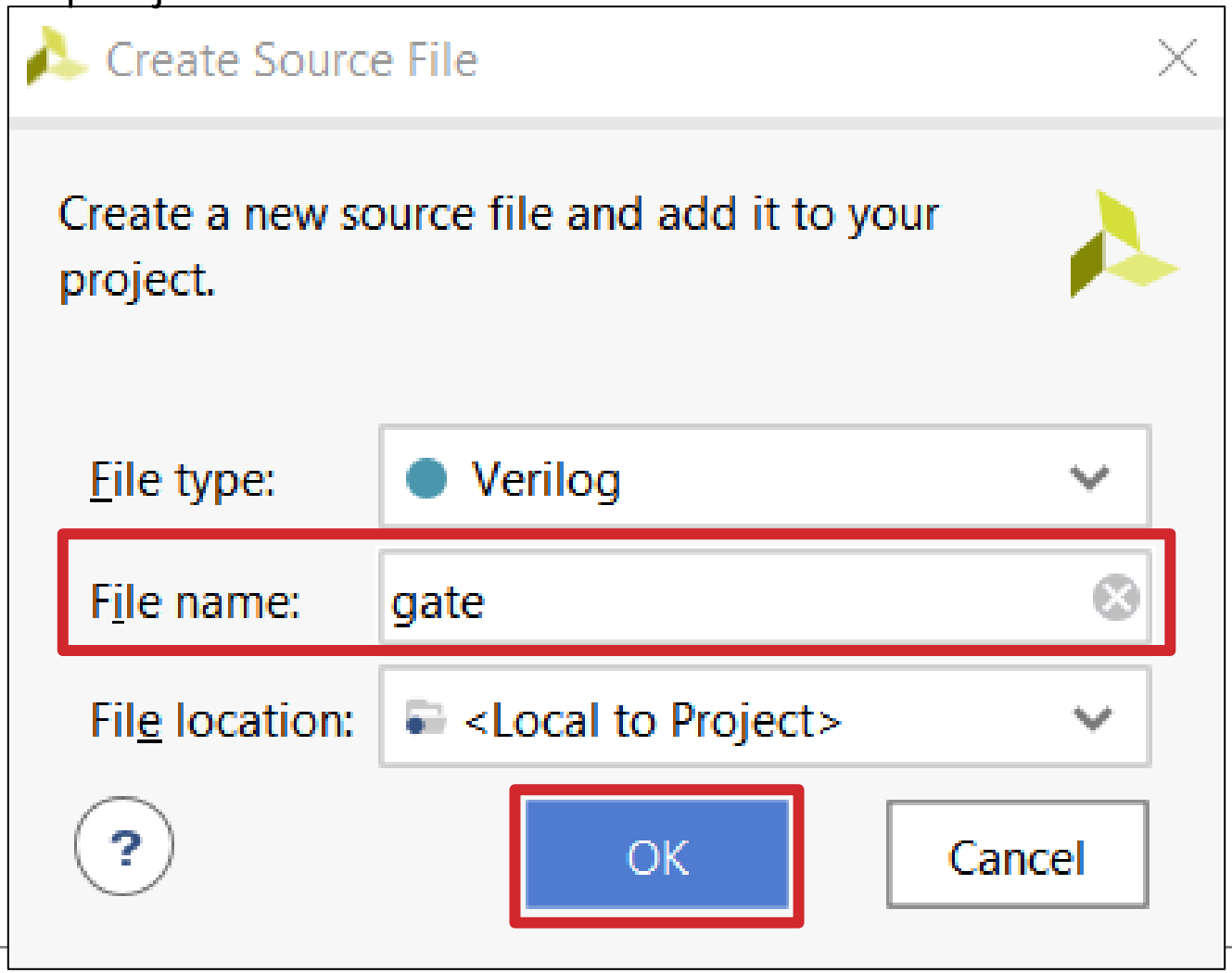

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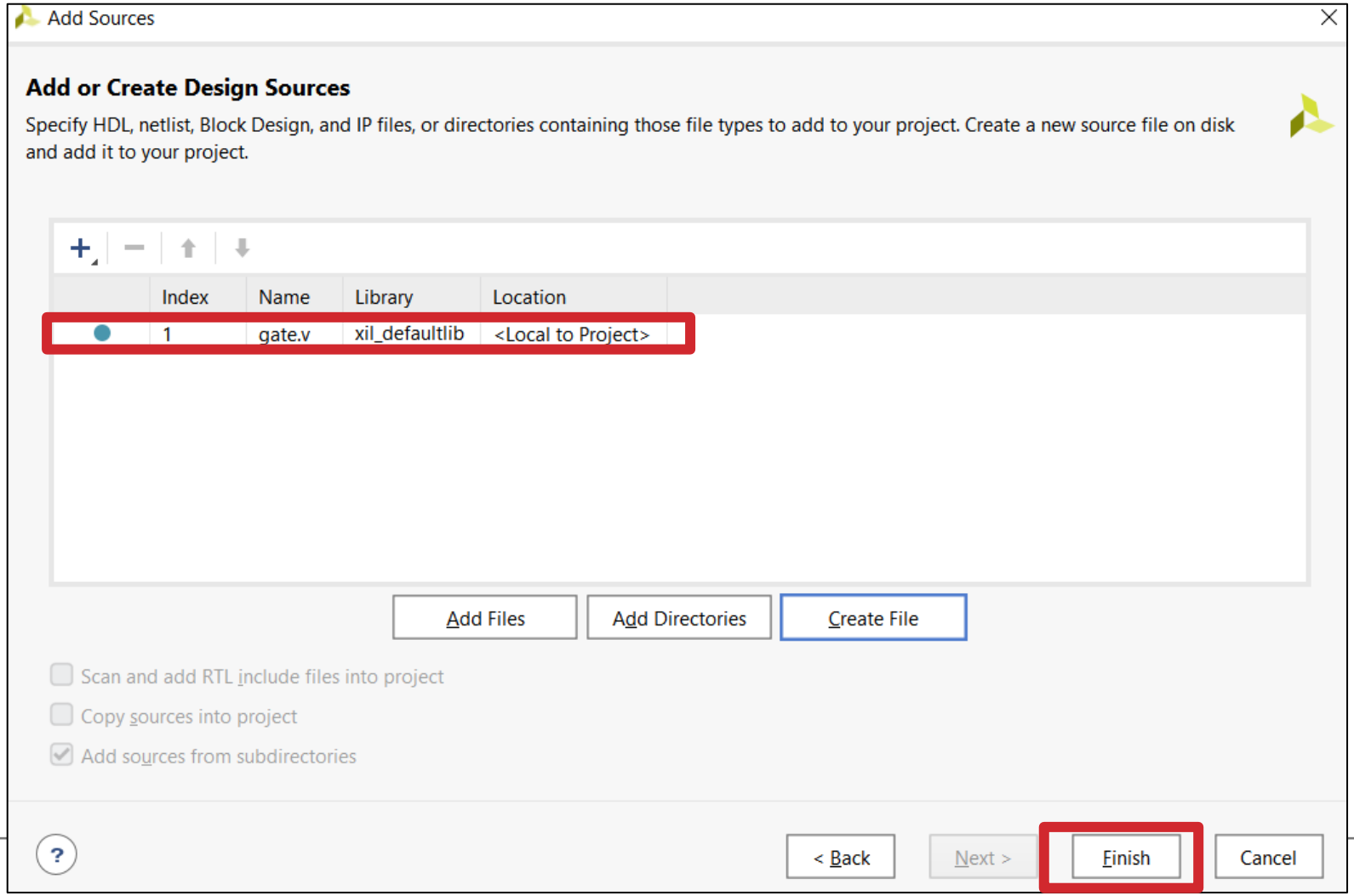

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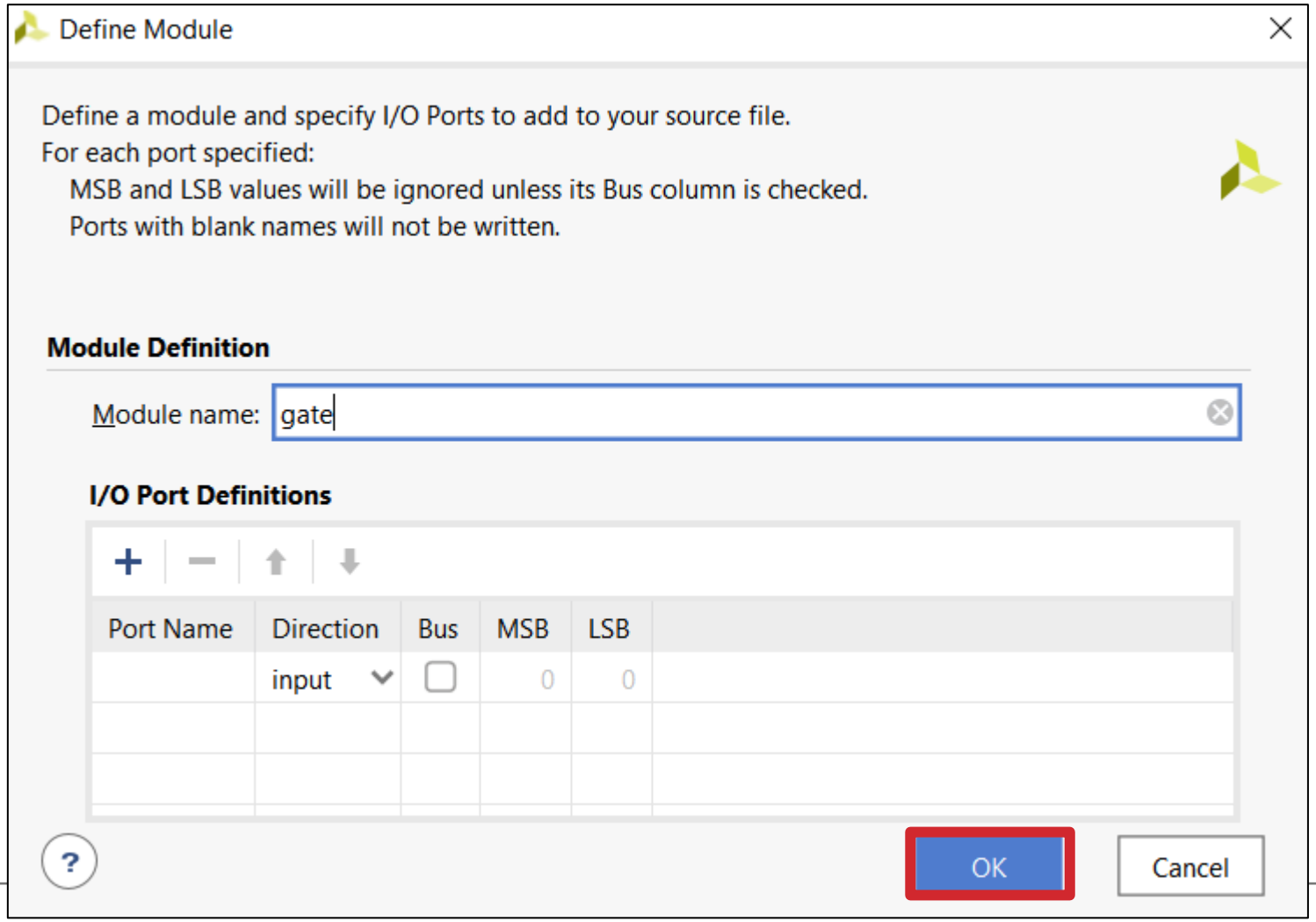

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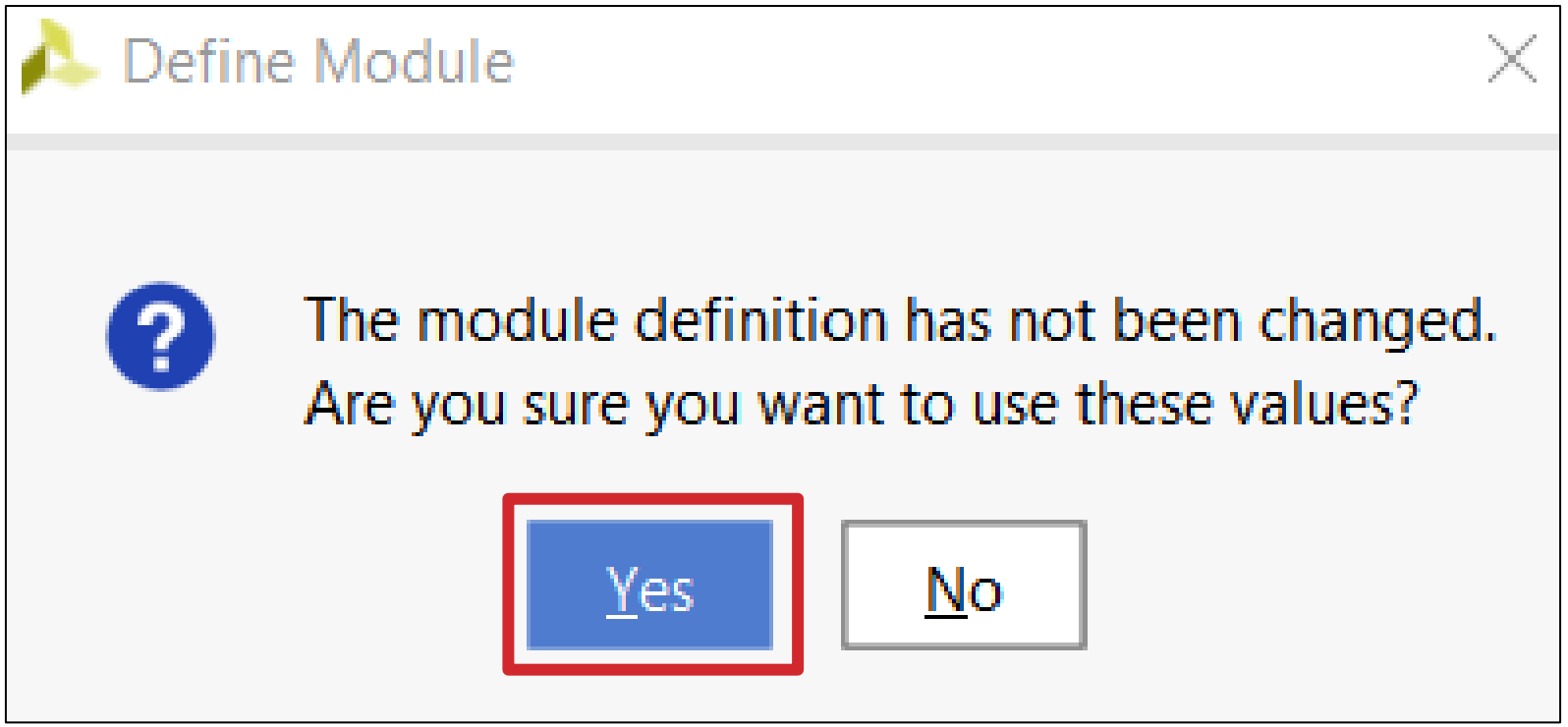

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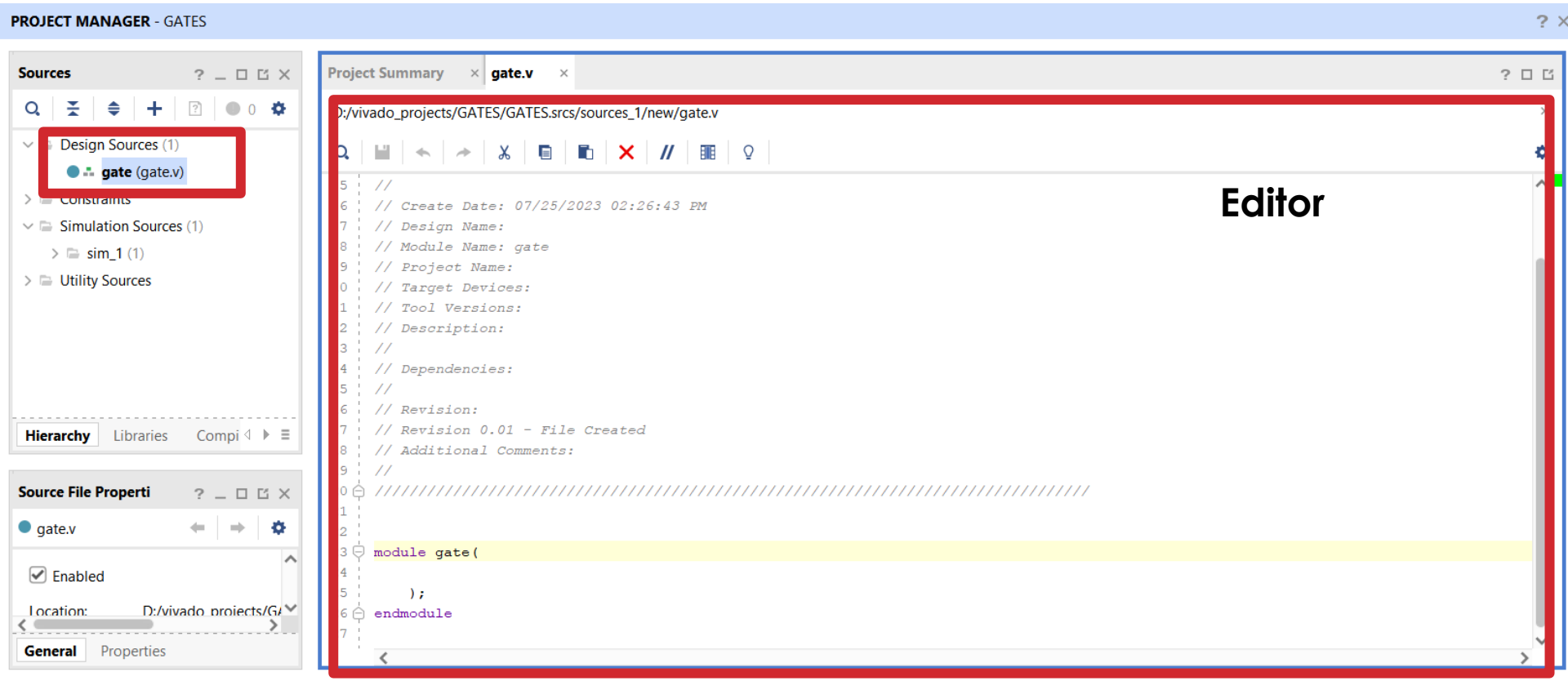
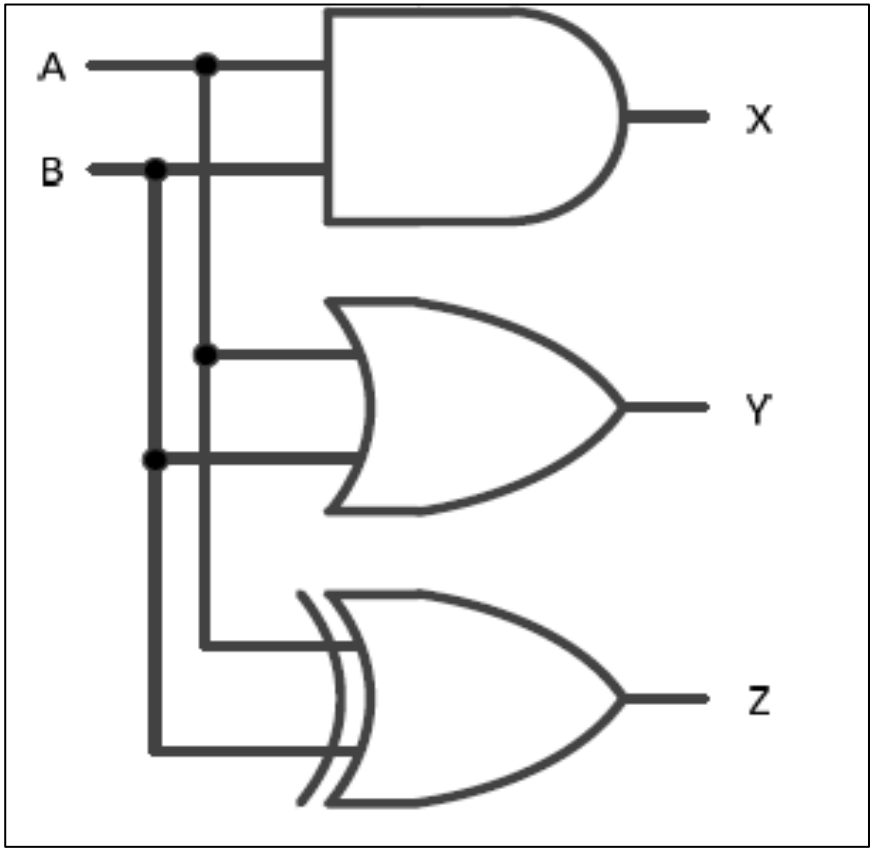


DESIGN EXAMPLE

- Vivado project
  - Verilog code and Testbench
    - **AND**-**OR**-**XOR** module



AND-OR-XOR Schematic

DESIGN EXAMPLE

- Vivado project
  - Verilog code **AND-OR-XOR** module

PROJECT MANAGER - GATES

Sources

Design Sources (1)
gate (gate.v)
Constraints
Simulation Sources (1)
sim_1 (1)
Utility Sources

Hierarchy Libraries Compi

Source File Properti

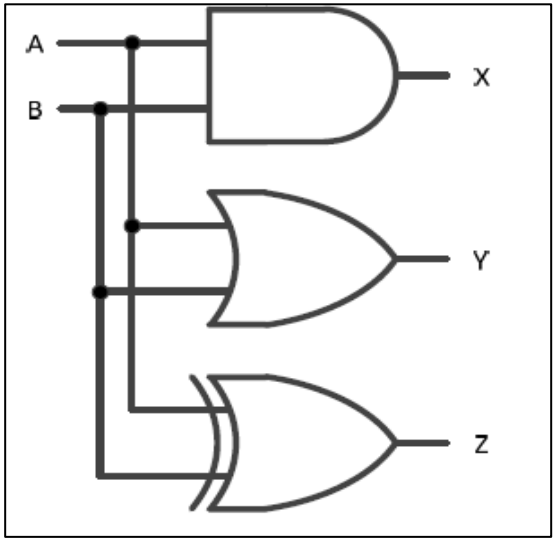
gate.v

Enabled

Project Summary | gate.v

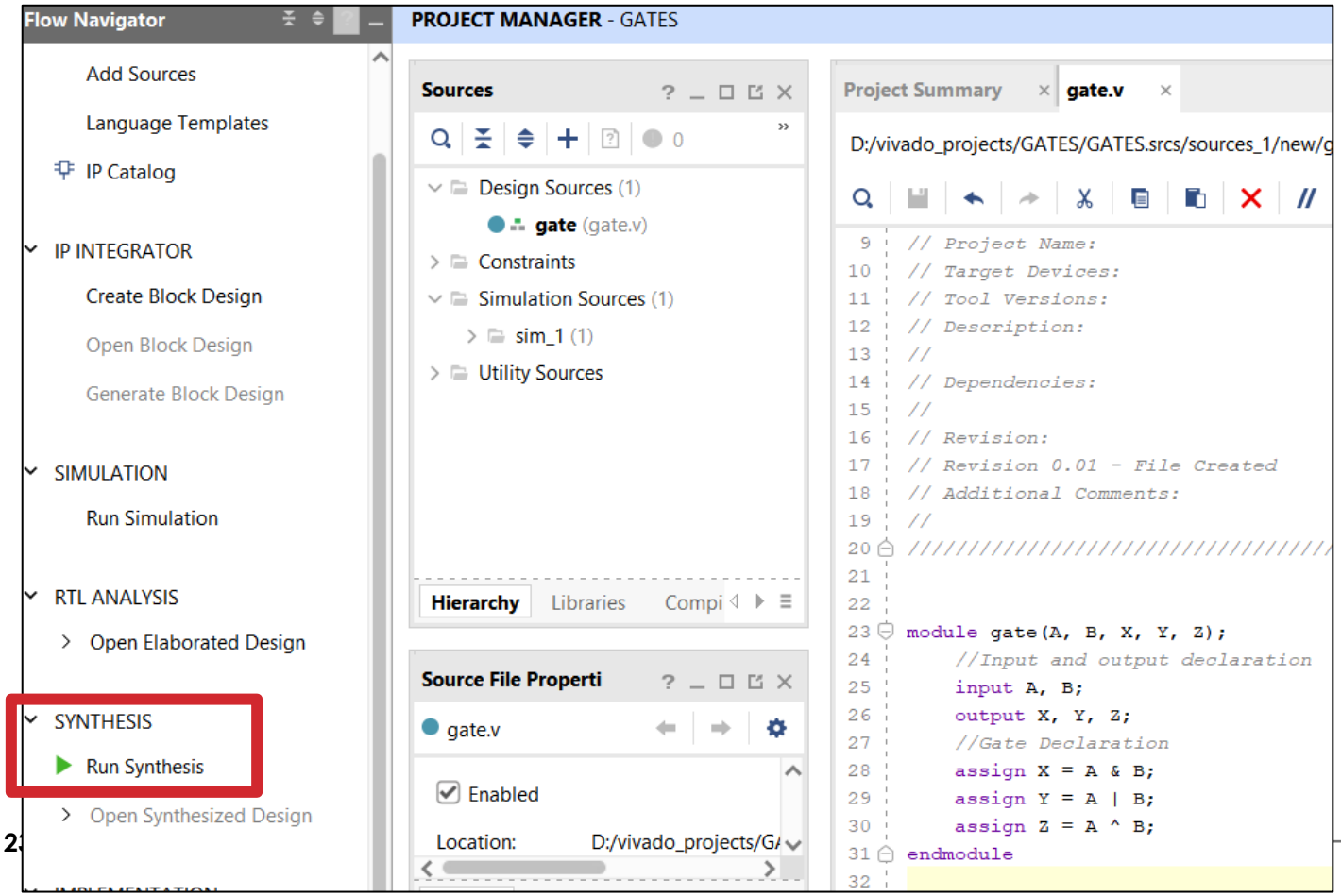
D:/vivado_projects/GATES/GATES.srcs/sources_1/new/

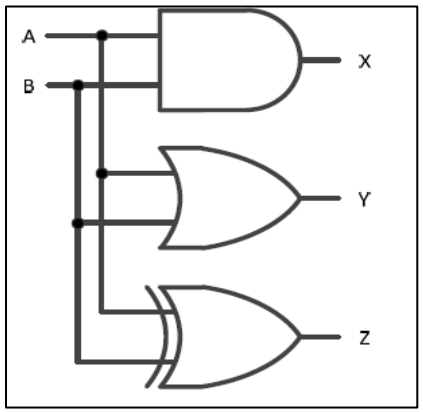
```
12  // Description:
13  //
14  // Dependencies:
15  //
16  // Revision:
17  // Revision 0.01 - File Created
18  // Additional Comments:
19  //
20  //////////////////////////////////
21
22
23  module gate(A, B, X, Y, Z);
24      //Input and output declaration
25      input A, B;
26      output X, Y, Z;
27      //Gate Declaration
28      assign X = A & B;
29      assign Y = A | B;
30      assign Z = A ^ B;
31  endmodule
```



DESIGN EXAMPLE

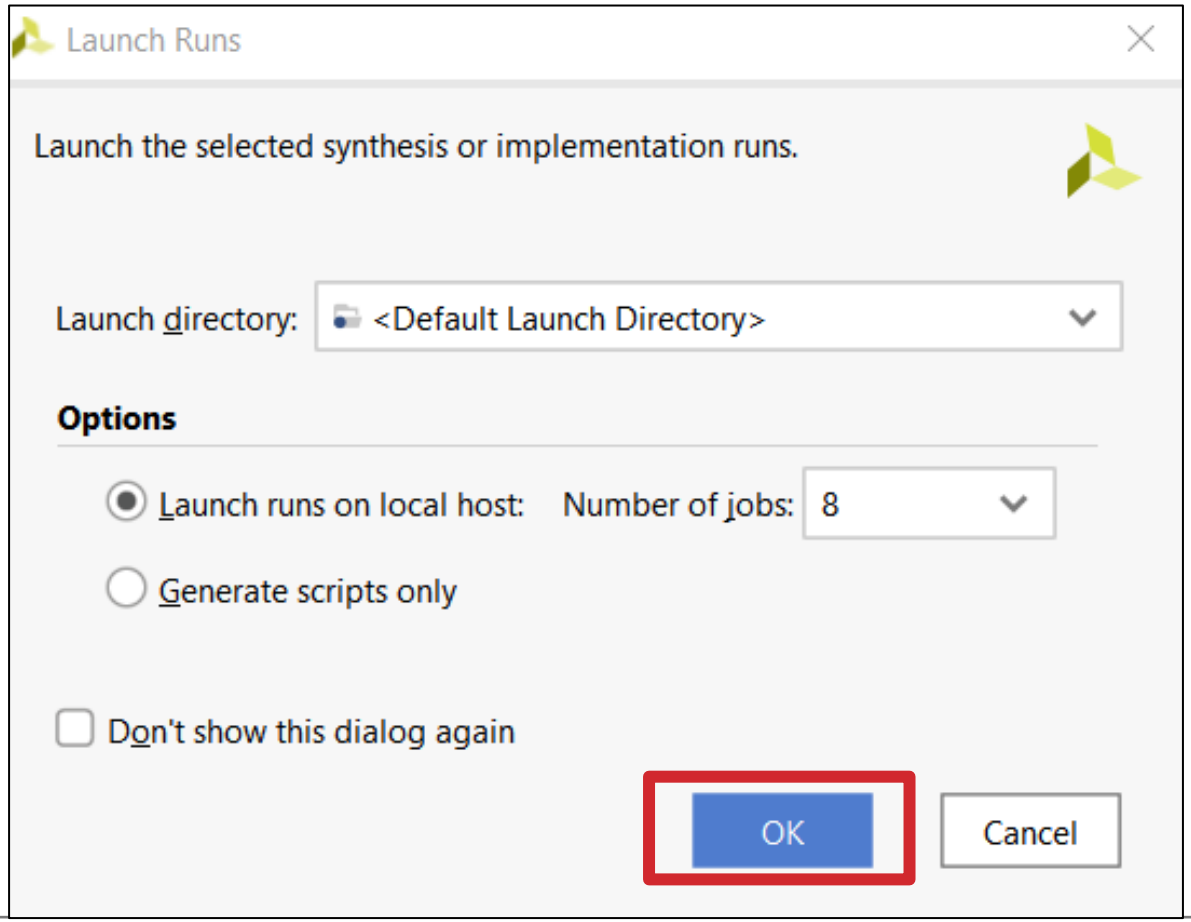
- Vivado project
  - Logic synthesis





DESIGN EXAMPLE

- Vivado project
  - Logic synthesis



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- Vivado project
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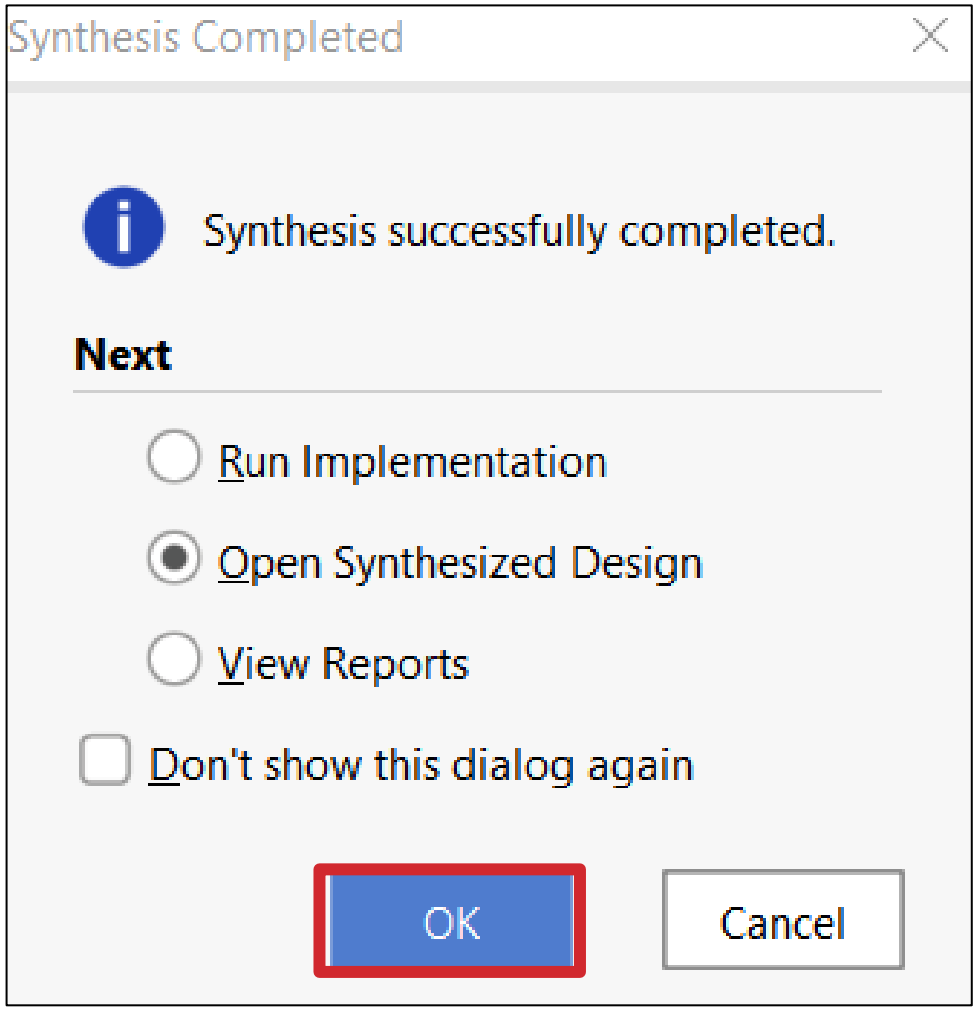
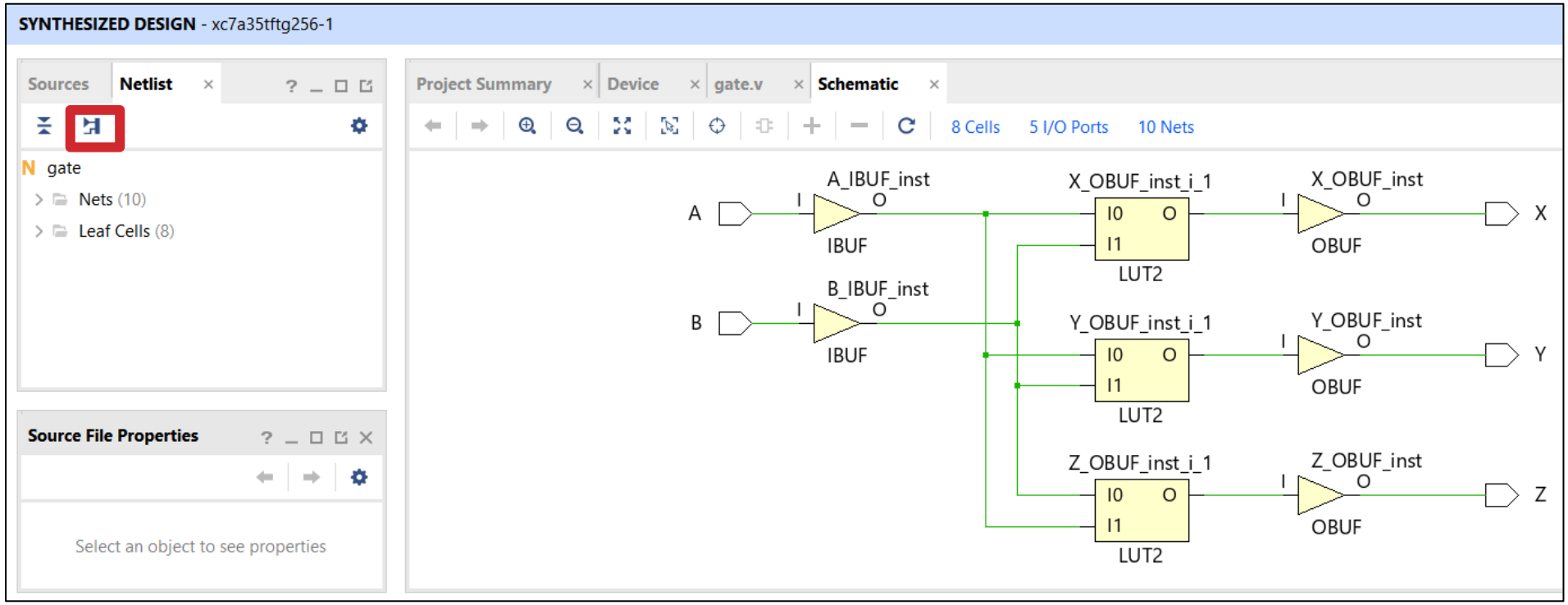


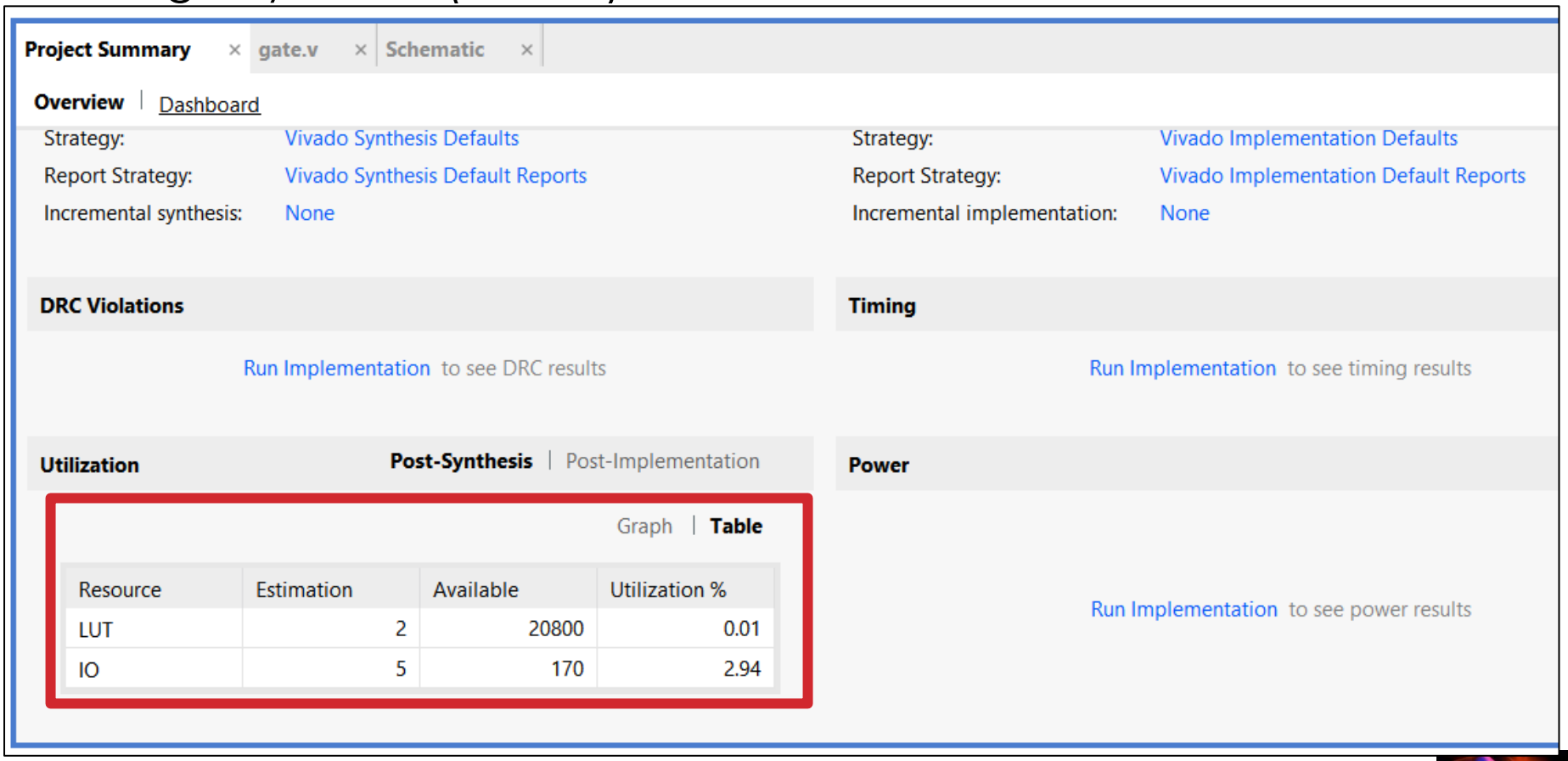
DESIGN EXAMPLE

- Vivado project
  - Logic synthesis (Schematic)



DESIGN EXAMPLE

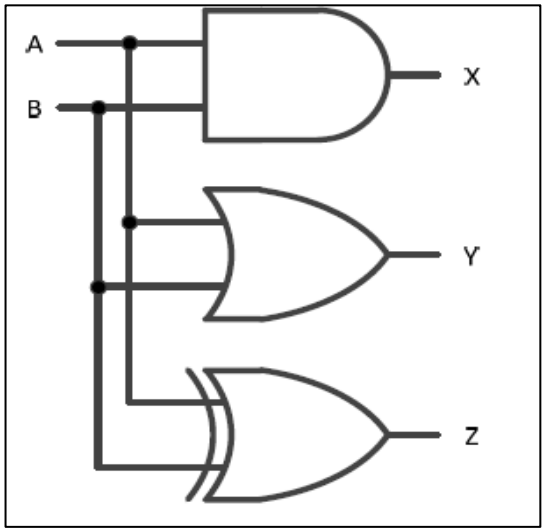
- Vivado project
  - Logic synthesis (Results)



DESIGN EXAMPLE

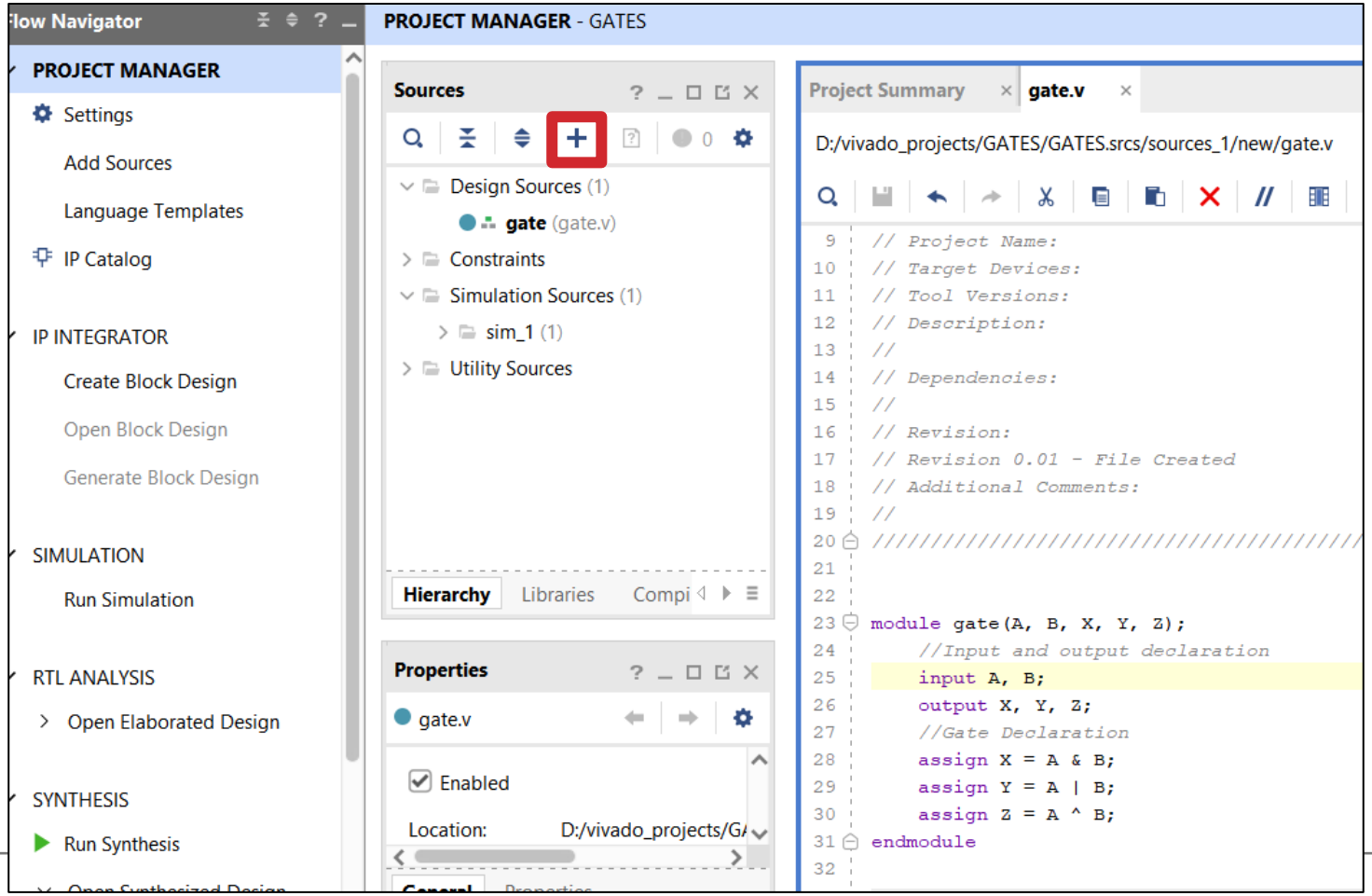
- Vivado project
  - Testbench for **AND-OR-XOR** module (Test Vectors)

A	B	X	Y	Z
0	0	0	0	0
0	1	0	1	1
1	0	0	1	1
1	1	1	1	0



DESIGN EXAMPLE

- Vivado project
  - Creating a Testbench



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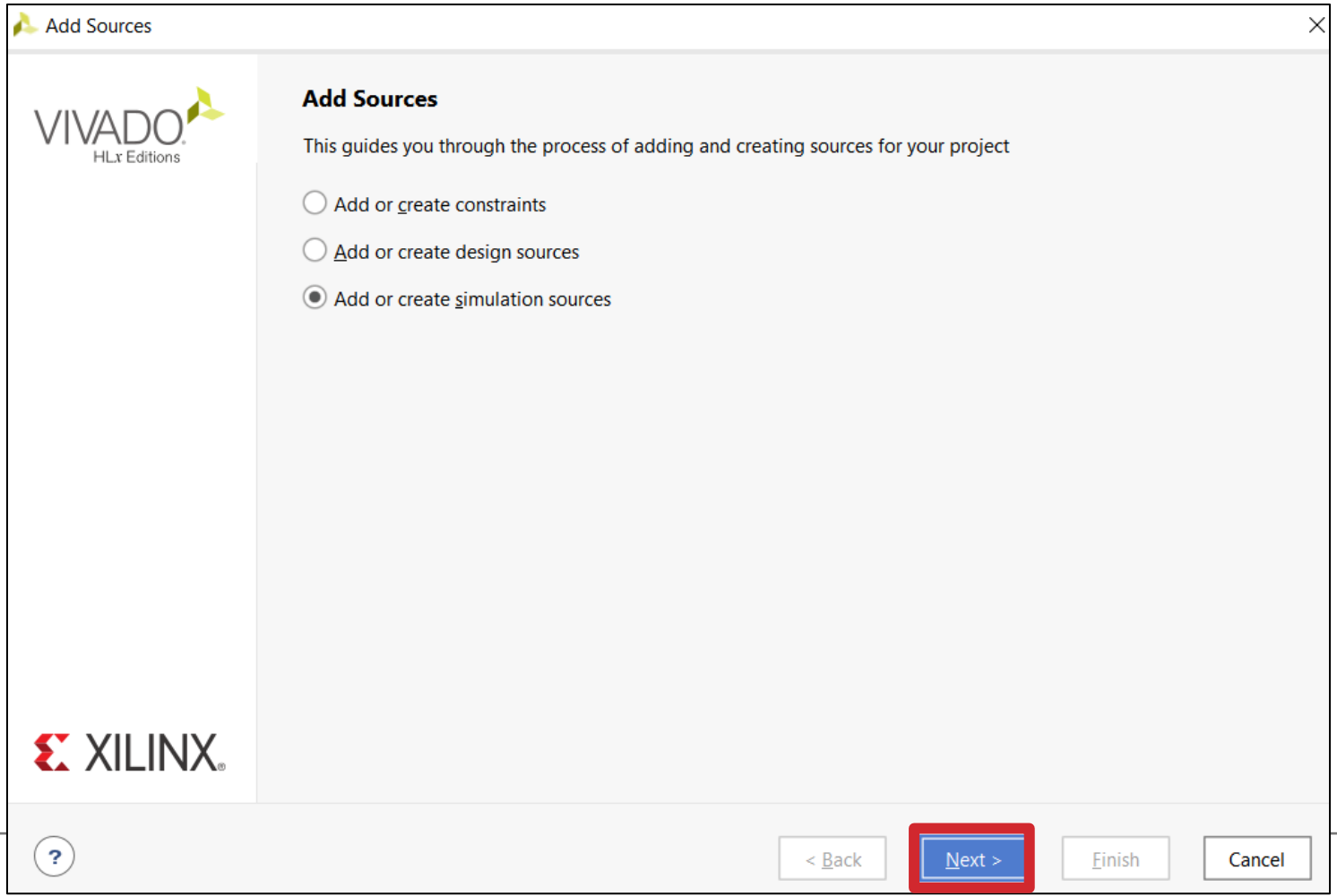

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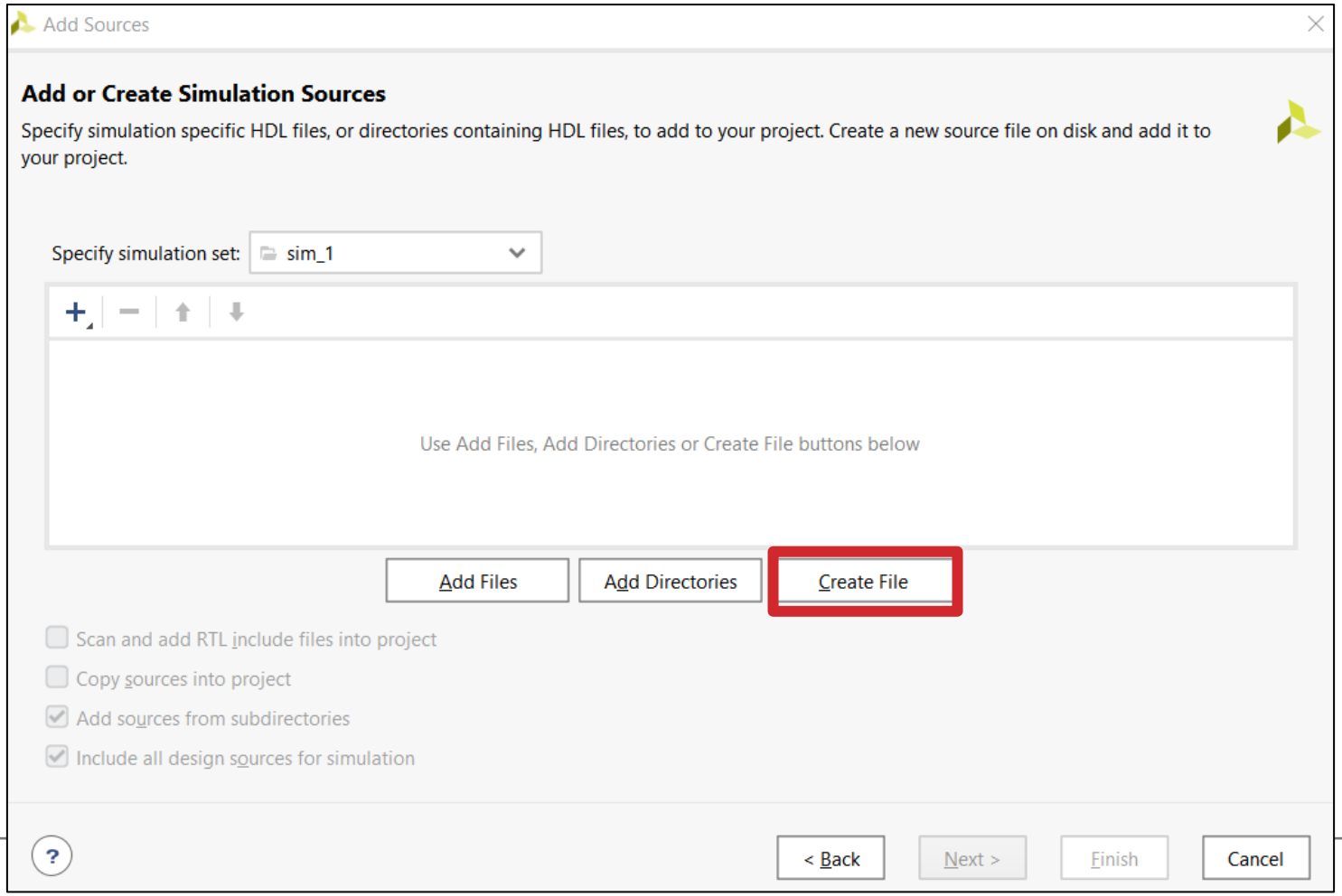

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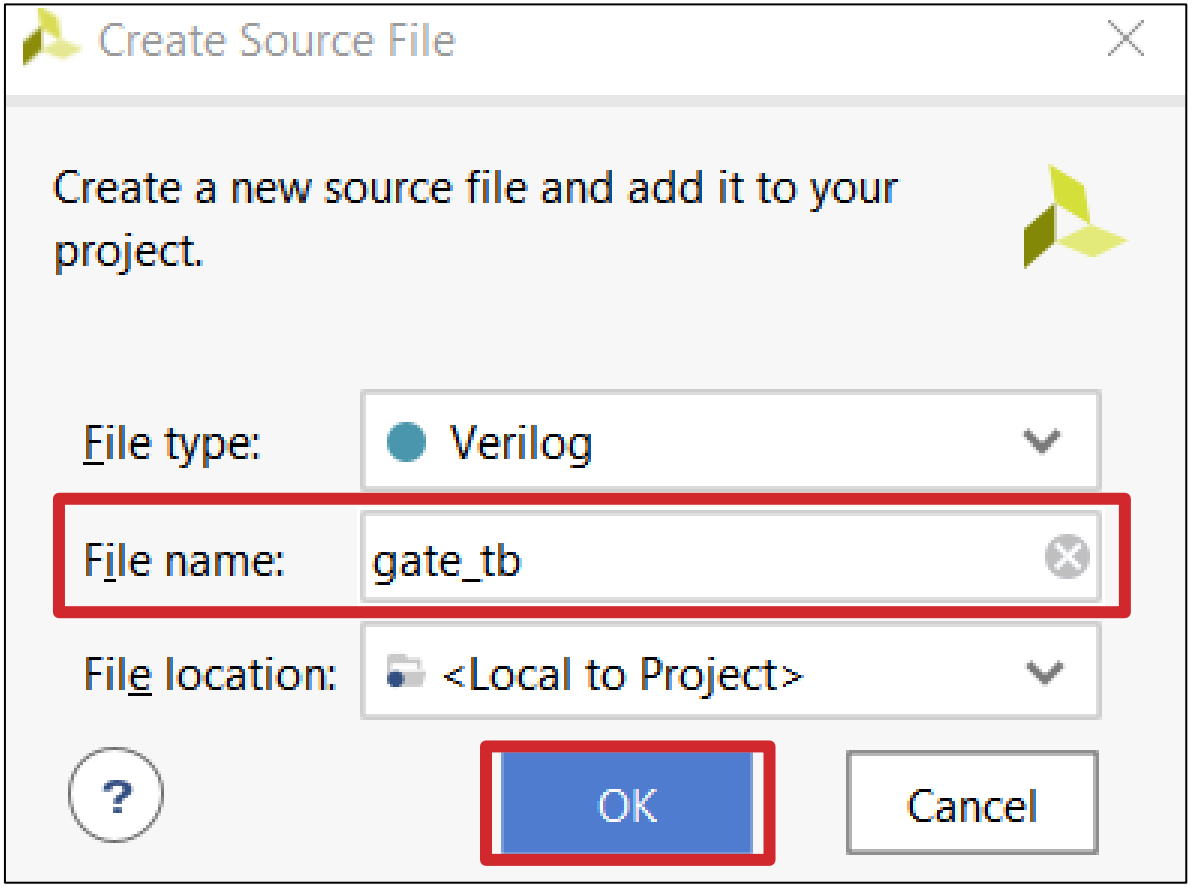

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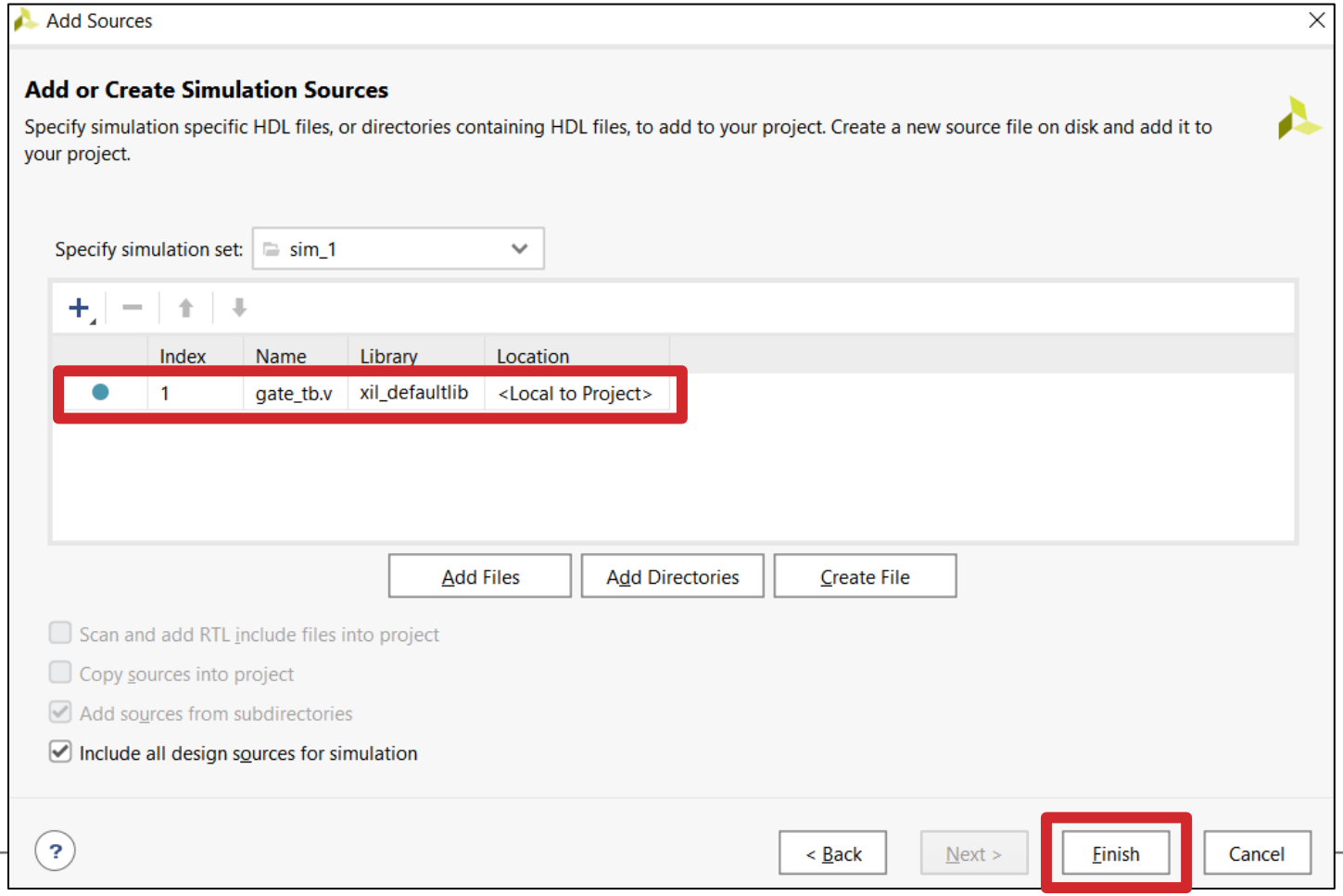

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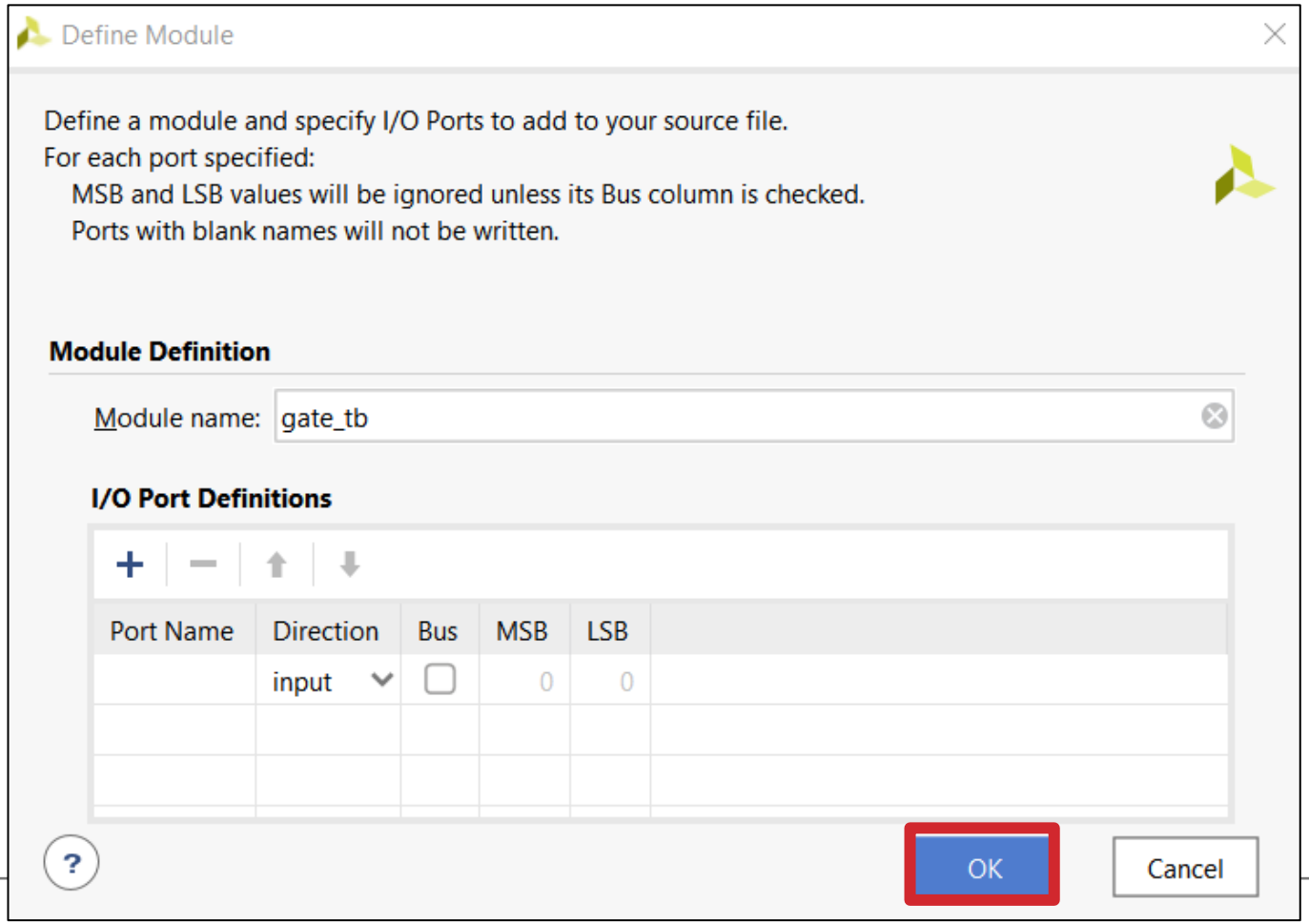

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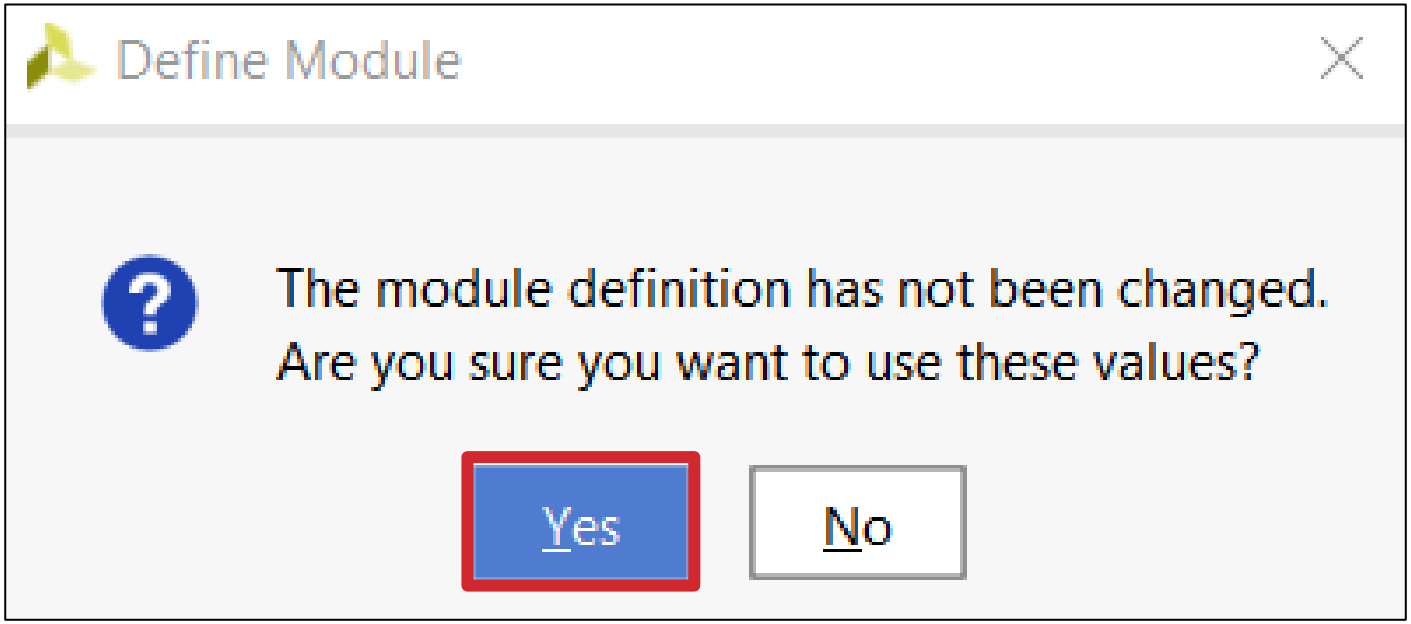

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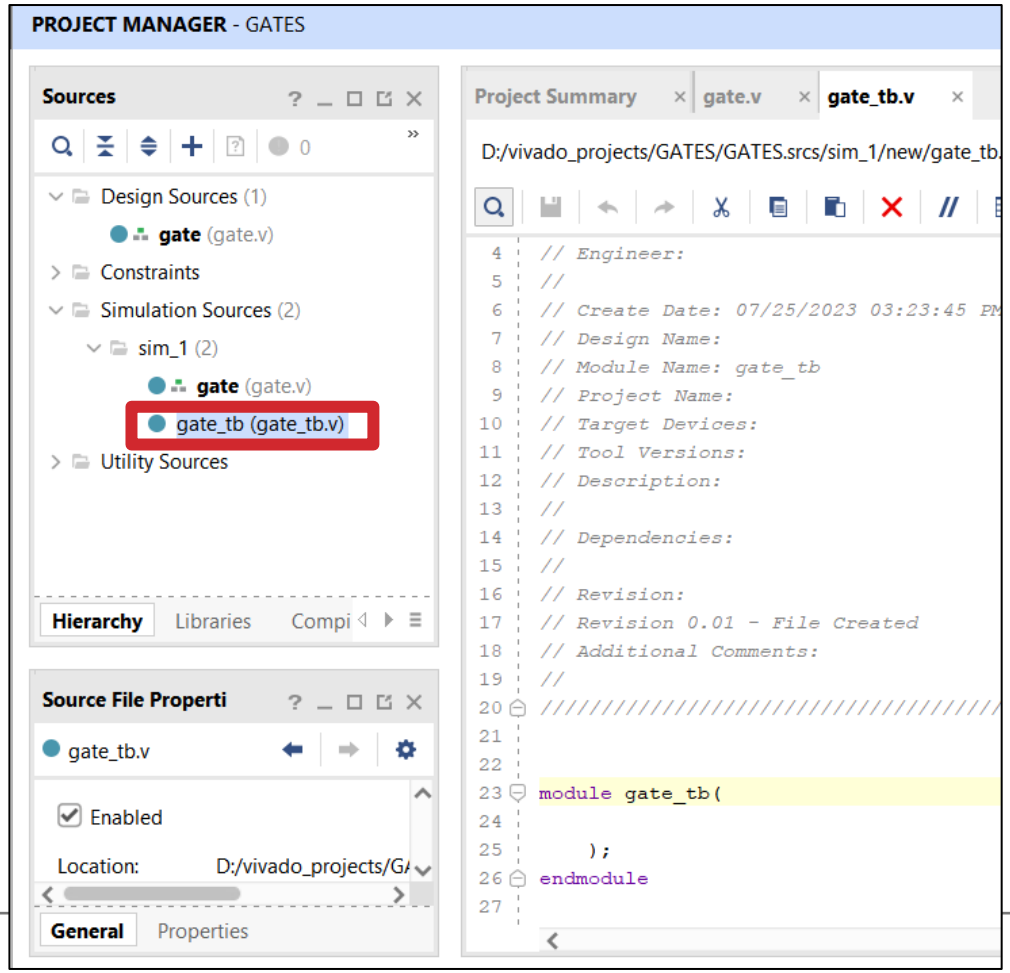

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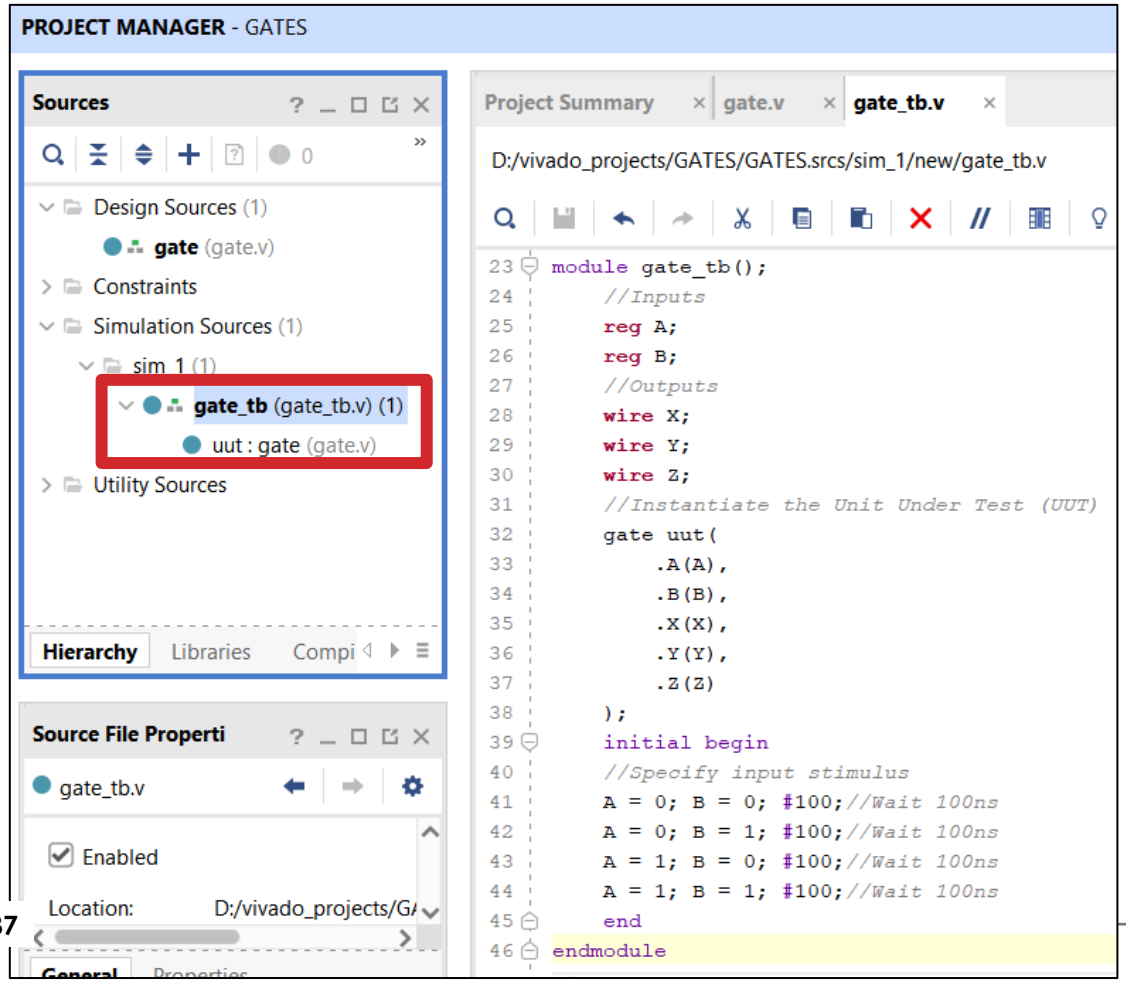
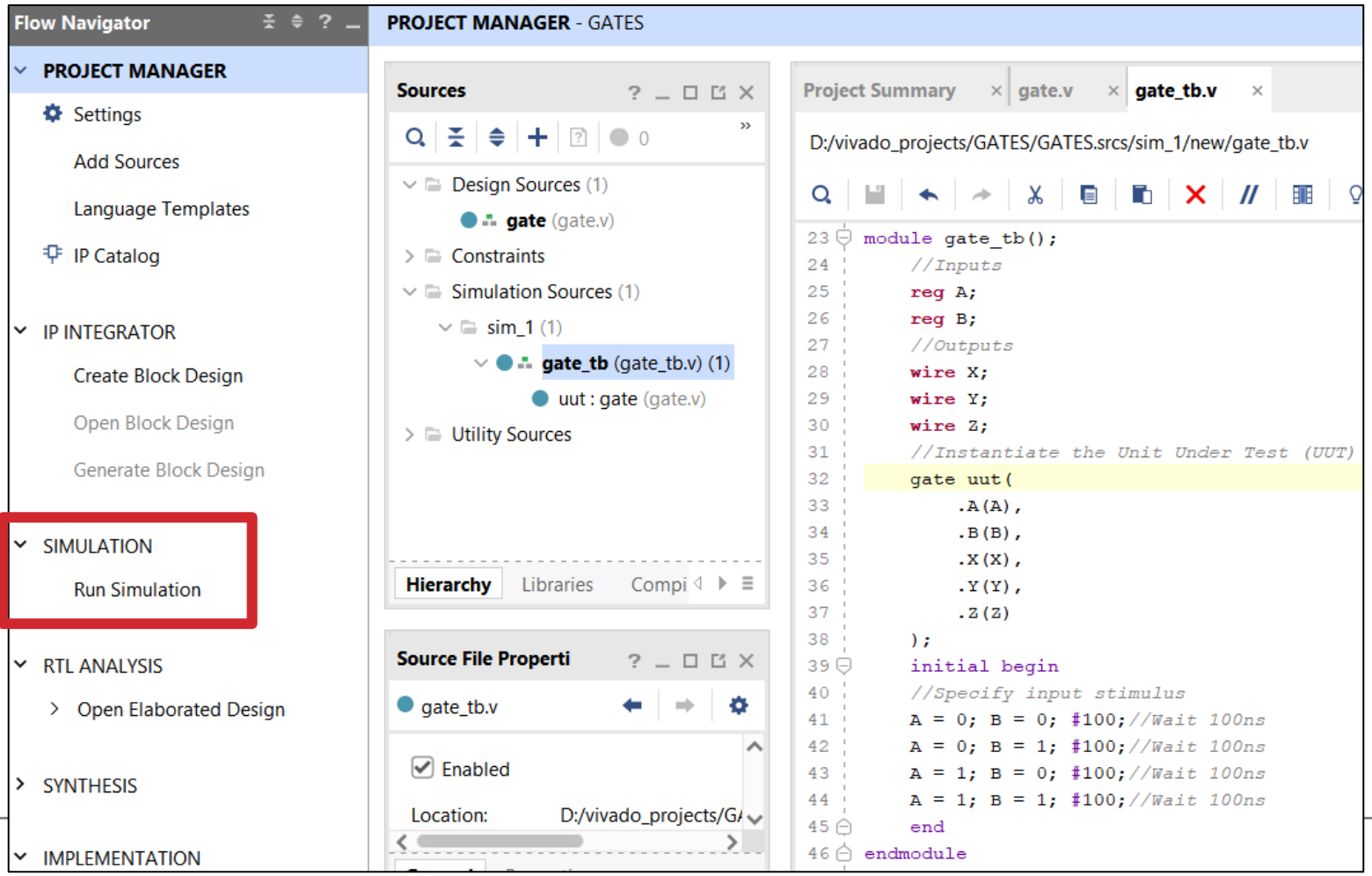


A	B	X	Y	Z
0	0	0	0	0
0	1	0	1	1
1	0	0	1	1
1	1	1	1	0

DESIGN EXAMPLE

- Vivado project
  - Running Simulation



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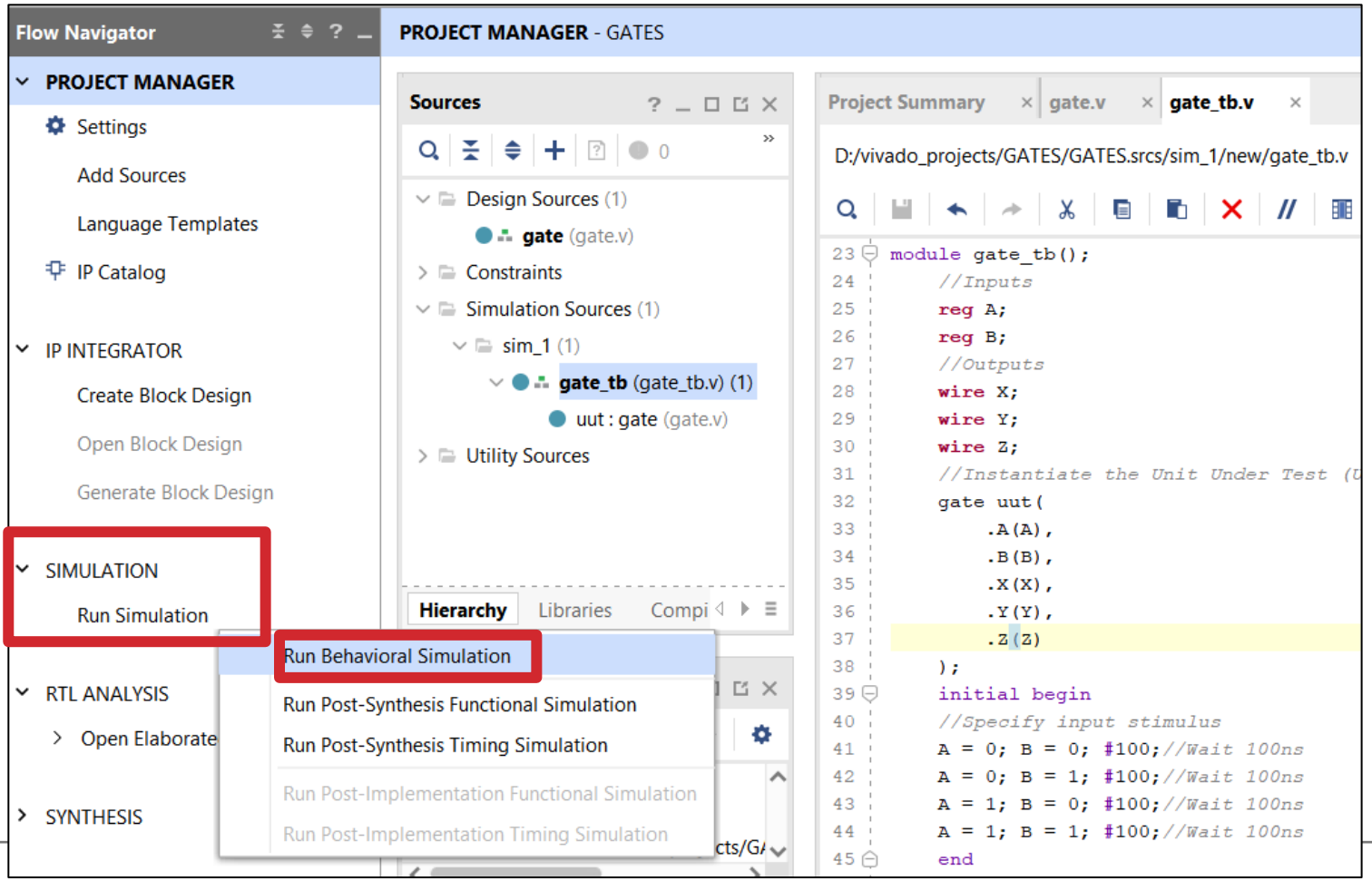
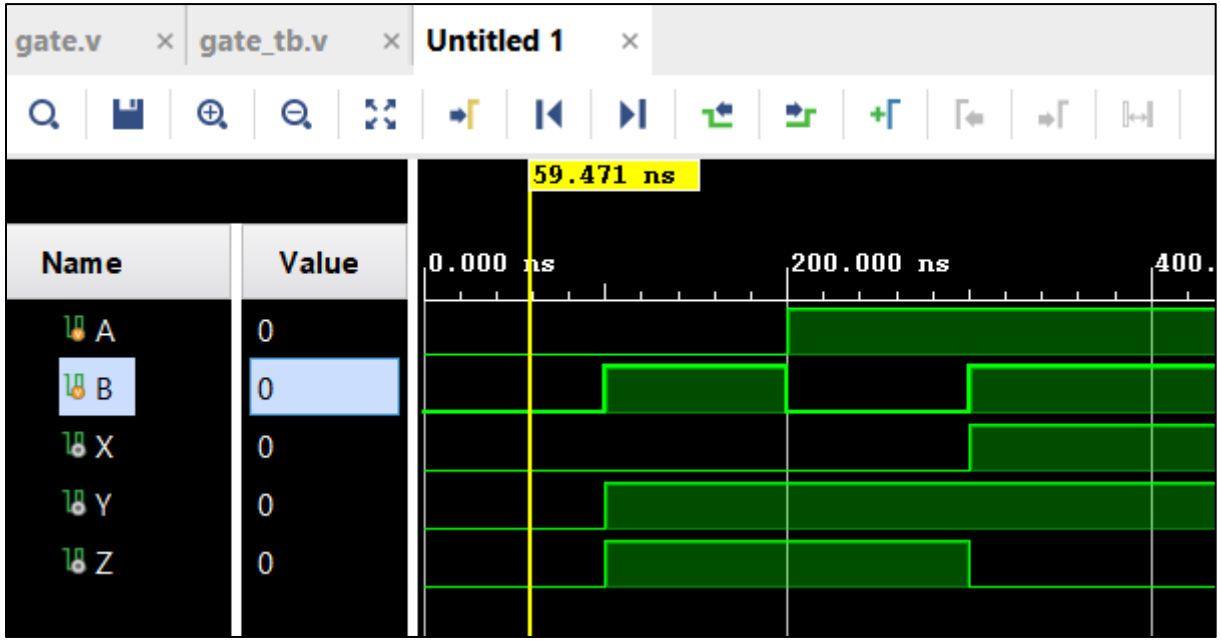


DESIGN EXAMPLE

- Vivado project
  - Running Simulation

```
//Specify input stimulus
A = 0; B = 0; #100;//Wait 100ns
A = 0; B = 1; #100;//Wait 100ns
A = 1; B = 0; #100;//Wait 100ns
A = 1; B = 1; #100;//Wait 100ns
```



A	B	X	Y	Z
0	0	0	0	0
0	1	0	1	1
1	0	0	1	1
1	1	1	1	0

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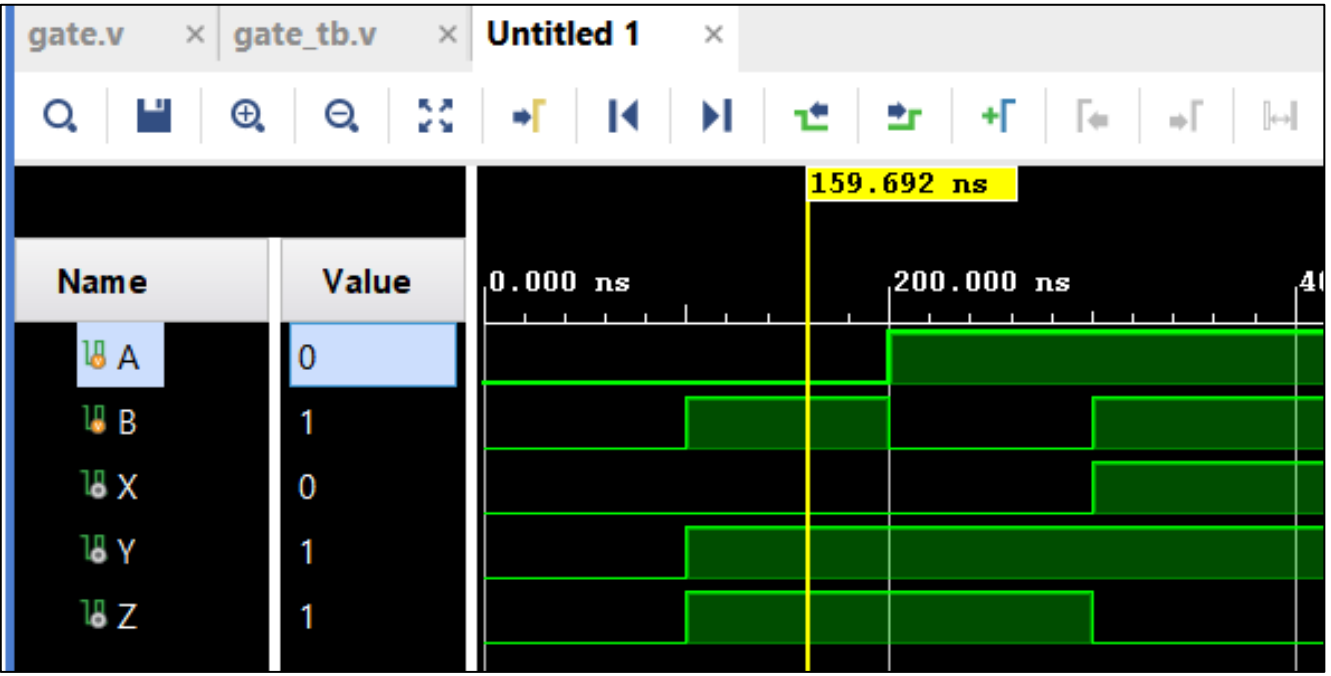

A	B	X	Y	Z
0	0	0	0	0
0	1	0	1	1
1	0	0	1	1
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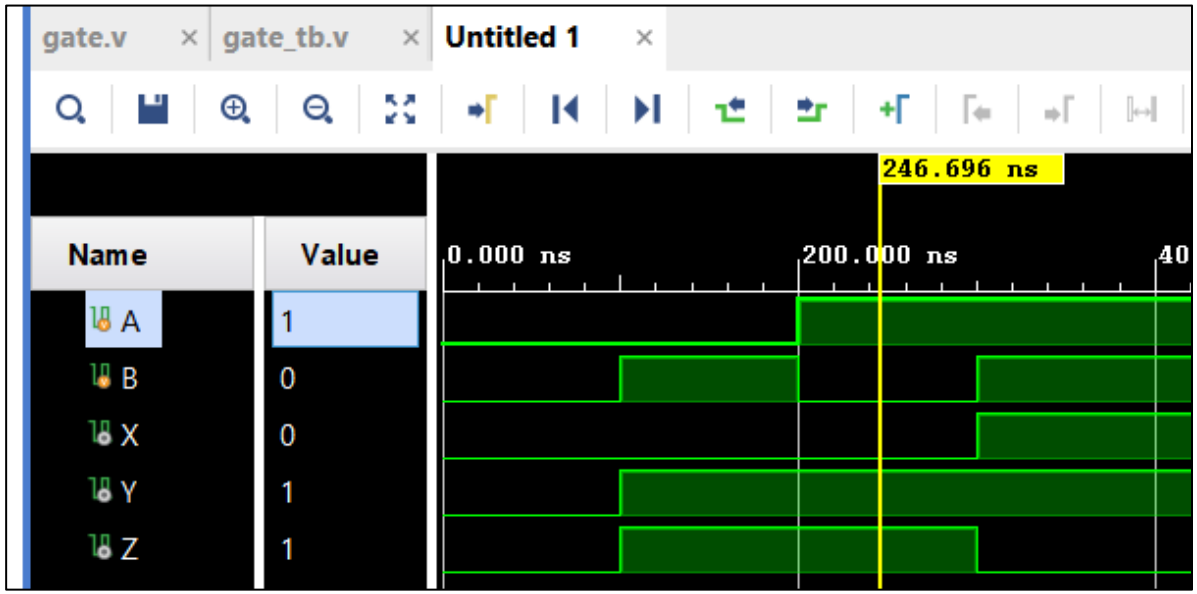

A	B	X	Y	Z
0	0	0	0	0
0	1	0	1	1
1	0	0	1	1
1	1	1	1	0

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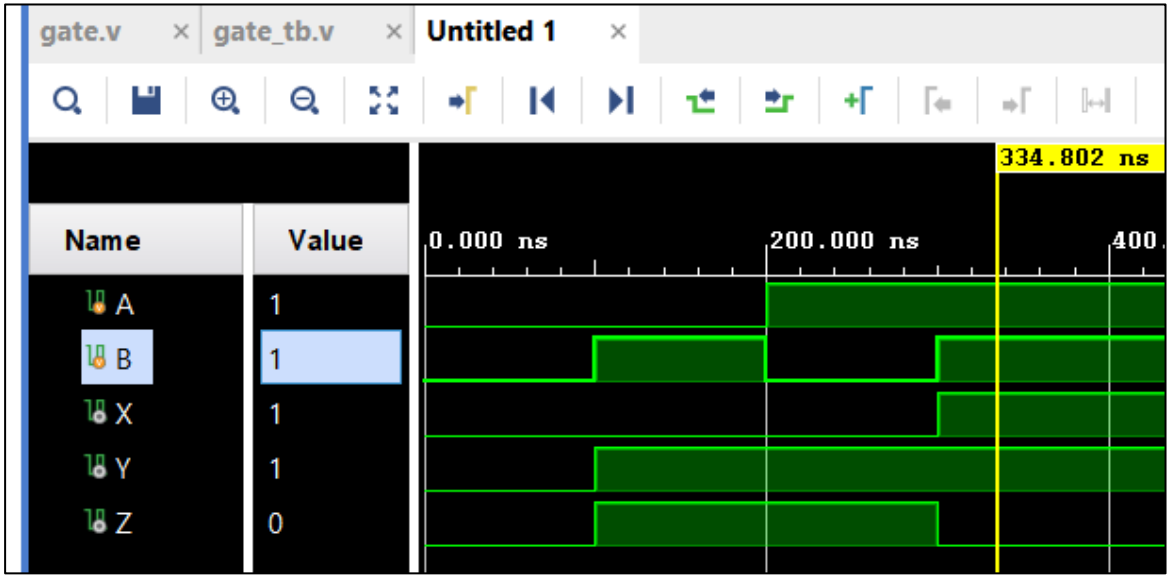
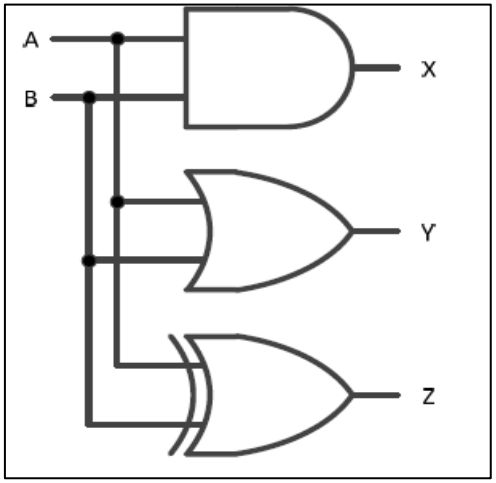
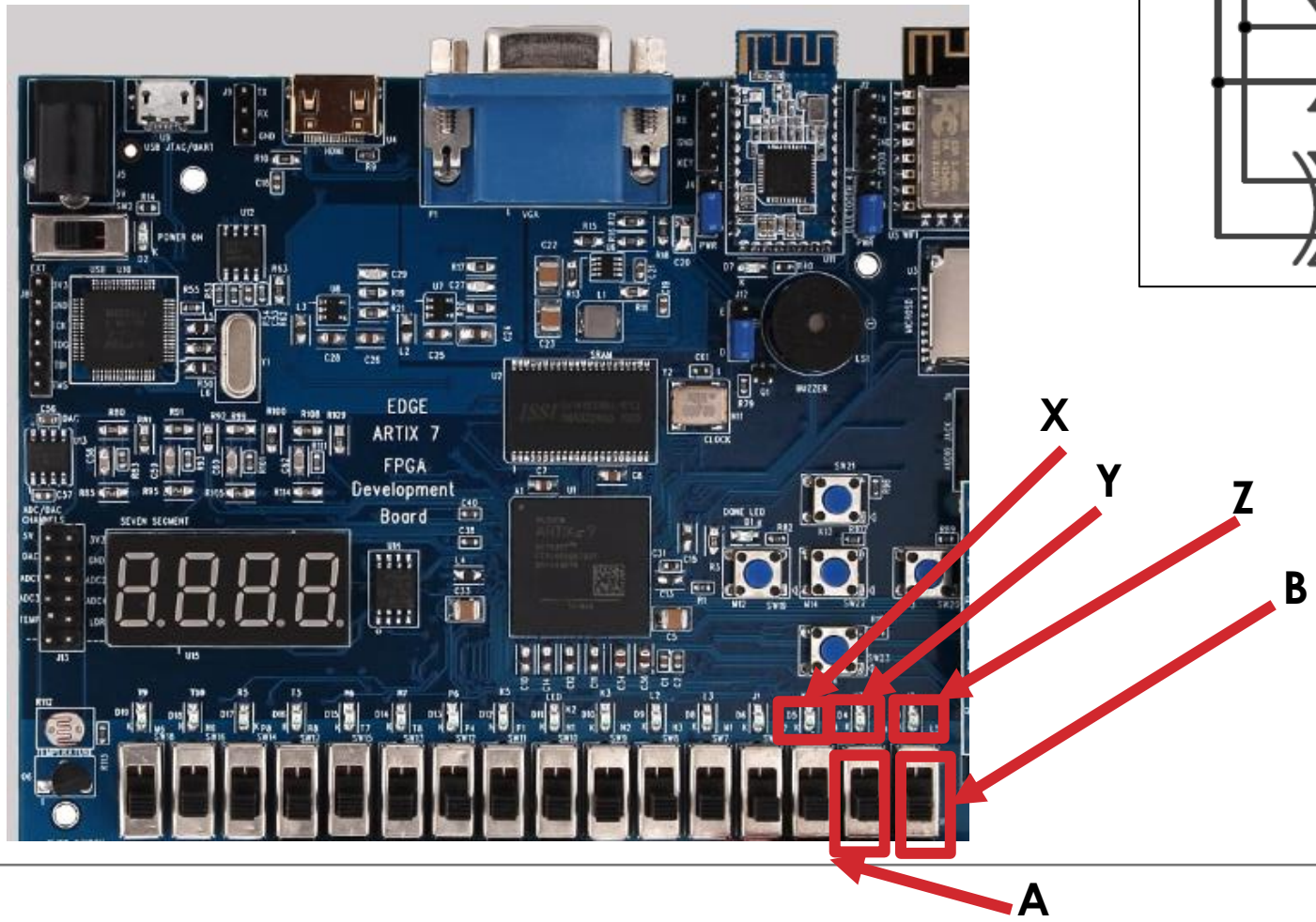


A	B	X	Y	Z
0	0	0	0	0
0	1	0	1	1
1	0	0	1	1
1	1	1	1	0

DESIGN EXAMPLE

- Vivado project
  - FPGA programming (mapping)





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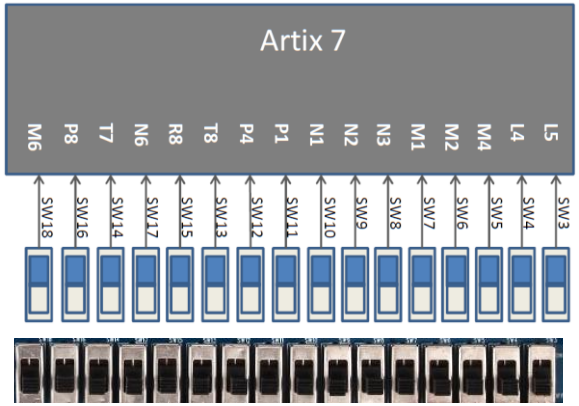
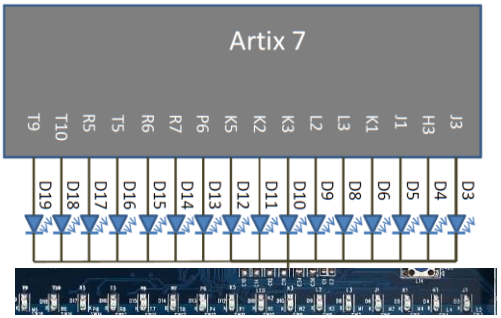



```
# Switches
set_property -dict { PACKAGE_PIN L5    IOSTANDARD LVCMOS33 } [get_ports { sw[0] }];#LSB
set_property -dict { PACKAGE_PIN L4    IOSTANDARD LVCMOS33 } [get_ports { sw[1] }];
set_property -dict { PACKAGE_PIN M4    IOSTANDARD LVCMOS33 } [get_ports { sw[2] }];
set_property -dict { PACKAGE_PIN M2    IOSTANDARD LVCMOS33 } [get_ports { sw[3] }];
set_property -dict { PACKAGE_PIN M1    IOSTANDARD LVCMOS33 } [get_ports { sw[4] }];
set_property -dict { PACKAGE_PIN N3    IOSTANDARD LVCMOS33 } [get_ports { sw[5] }];
set_property -dict { PACKAGE_PIN N2    IOSTANDARD LVCMOS33 } [get_ports { sw[6] }];
set_property -dict { PACKAGE_PIN N1    IOSTANDARD LVCMOS33 } [get_ports { sw[7] }];
set_property -dict { PACKAGE_PIN P1    IOSTANDARD LVCMOS33 } [get_ports { sw[8] }];
set_property -dict { PACKAGE_PIN P4    IOSTANDARD LVCMOS33 } [get_ports { sw[9] }];
set_property -dict { PACKAGE_PIN T8    IOSTANDARD LVCMOS33 } [get_ports { sw[10] }];
set_property -dict { PACKAGE_PIN R8    IOSTANDARD LVCMOS33 } [get_ports { sw[11] }];
set_property -dict { PACKAGE_PIN N6    IOSTANDARD LVCMOS33 } [get_ports { sw[12] }];
set_property -dict { PACKAGE_PIN T7    IOSTANDARD LVCMOS33 } [get_ports { sw[13] }];
set_property -dict { PACKAGE_PIN P8    IOSTANDARD LVCMOS33 } [get_ports { sw[14] }];
set_property -dict { PACKAGE_PIN M6    IOSTANDARD LVCMOS33 } [get_ports { sw[15] }];#MSB
```

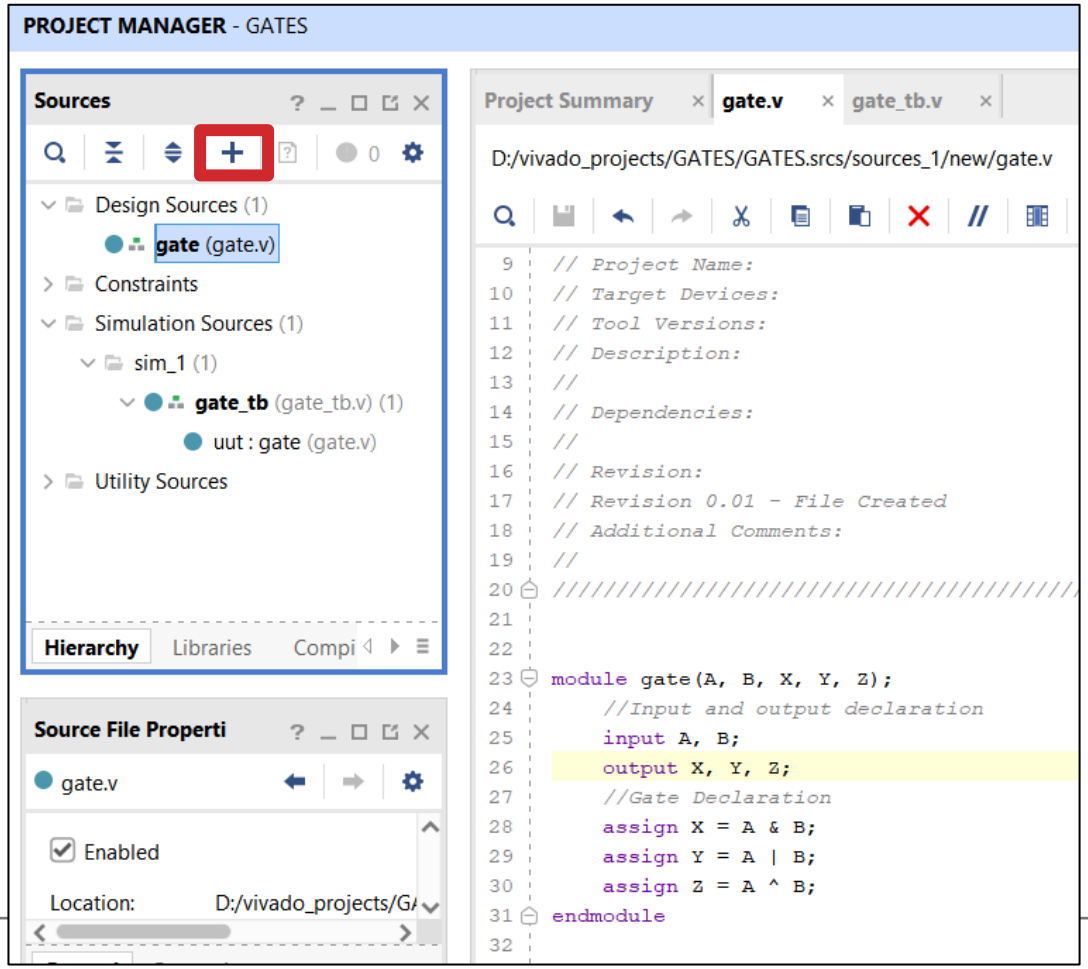



```
# LEDs
set_property -dict { PACKAGE_PIN J3    IOSTANDARD LVCMOS33 } [get_ports { led[0] }];#LSB
set_property -dict { PACKAGE_PIN H3    IOSTANDARD LVCMOS33 } [get_ports { led[1] }];
set_property -dict { PACKAGE_PIN J1    IOSTANDARD LVCMOS33 } [get_ports { led[2] }];
set_property -dict { PACKAGE_PIN K1    IOSTANDARD LVCMOS33 } [get_ports { led[3] }];
set_property -dict { PACKAGE_PIN L3    IOSTANDARD LVCMOS33 } [get_ports { led[4] }];
set_property -dict { PACKAGE_PIN L2    IOSTANDARD LVCMOS33 } [get_ports { led[5] }];
set_property -dict { PACKAGE_PIN K3    IOSTANDARD LVCMOS33 } [get_ports { led[6] }];
set_property -dict { PACKAGE_PIN K2    IOSTANDARD LVCMOS33 } [get_ports { led[7] }];
set_property -dict { PACKAGE_PIN K5    IOSTANDARD LVCMOS33 } [get_ports { led[8] }];
set_property -dict { PACKAGE_PIN P6    IOSTANDARD LVCMOS33 } [get_ports { led[9] }];
set_property -dict { PACKAGE_PIN R7    IOSTANDARD LVCMOS33 } [get_ports { led[10] }];
set_property -dict { PACKAGE_PIN R6    IOSTANDARD LVCMOS33 } [get_ports { led[11] }];
set_property -dict { PACKAGE_PIN T5    IOSTANDARD LVCMOS33 } [get_ports { led[12] }];
set_property -dict { PACKAGE_PIN R5    IOSTANDARD LVCMOS33 } [get_ports { led[13] }];
set_property -dict { PACKAGE_PIN T10   IOSTANDARD LVCMOS33 } [get_ports { led[14] }];
set_property -dict { PACKAGE_PIN T9    IOSTANDARD LVCMOS33 } [get_ports { led[15] }];#MSB
```

Port Name	Pin Number
A	L4
B	L5
X	J1
Y	H3
Z	J3

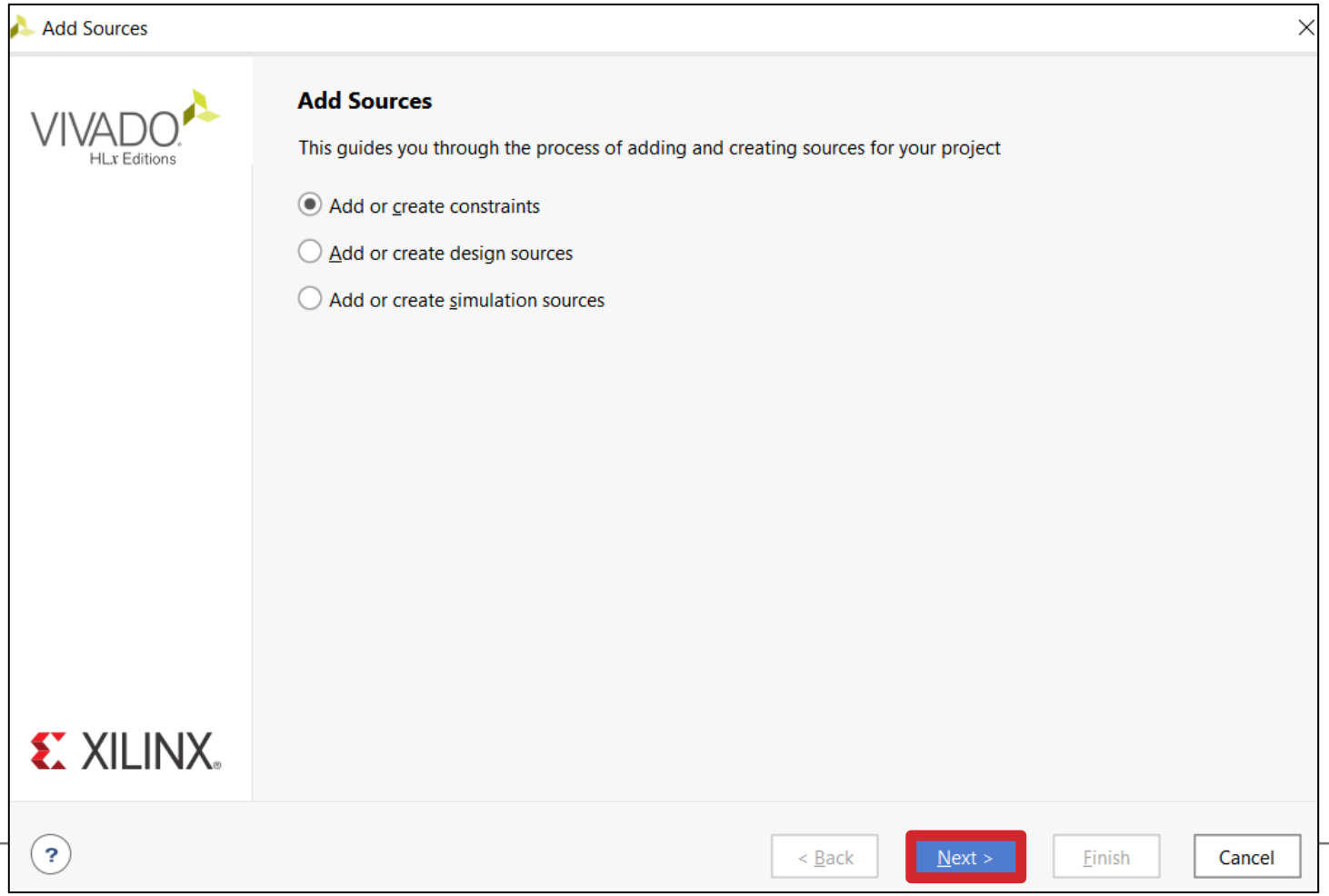
DESIGN EXAMPLE

- Vivado project
  - FPGA programming (mapping) – Create a constraint file



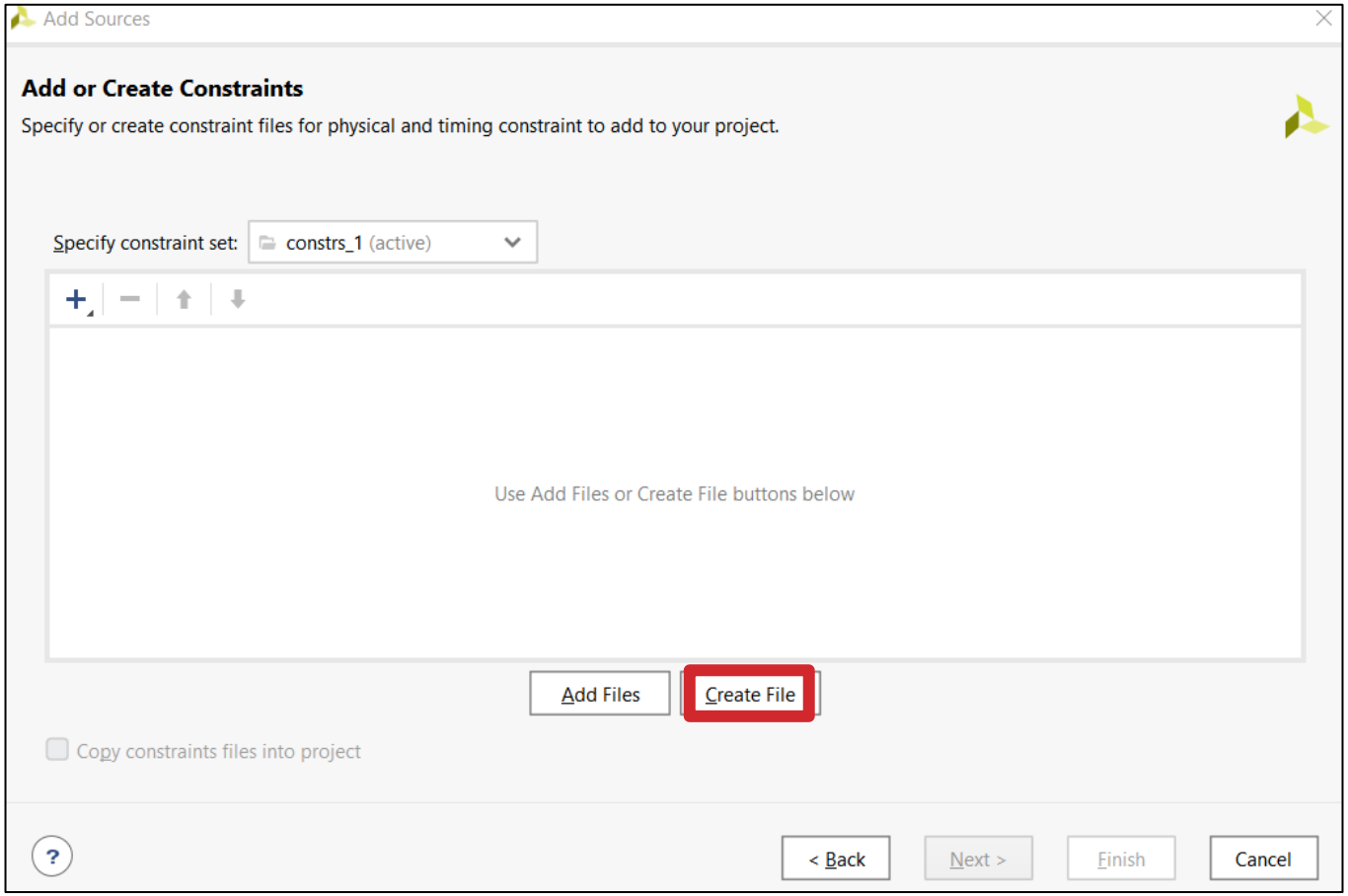
DESIGN EXAMPLE

- Vivado project
  - FPGA programming (mapping) – Create a constraint file



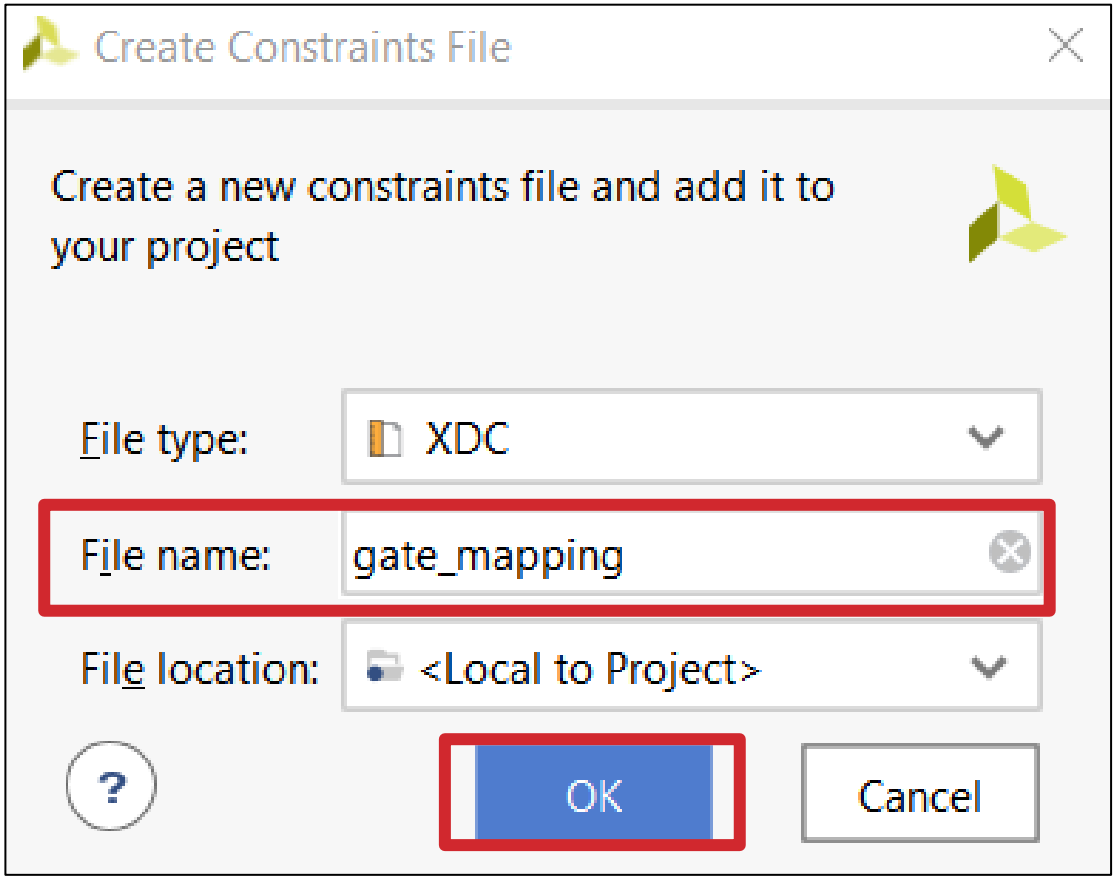
DESIGN EXAMPLE

- Vivado project
  - FPGA programming (mapping) – Create a constraint file



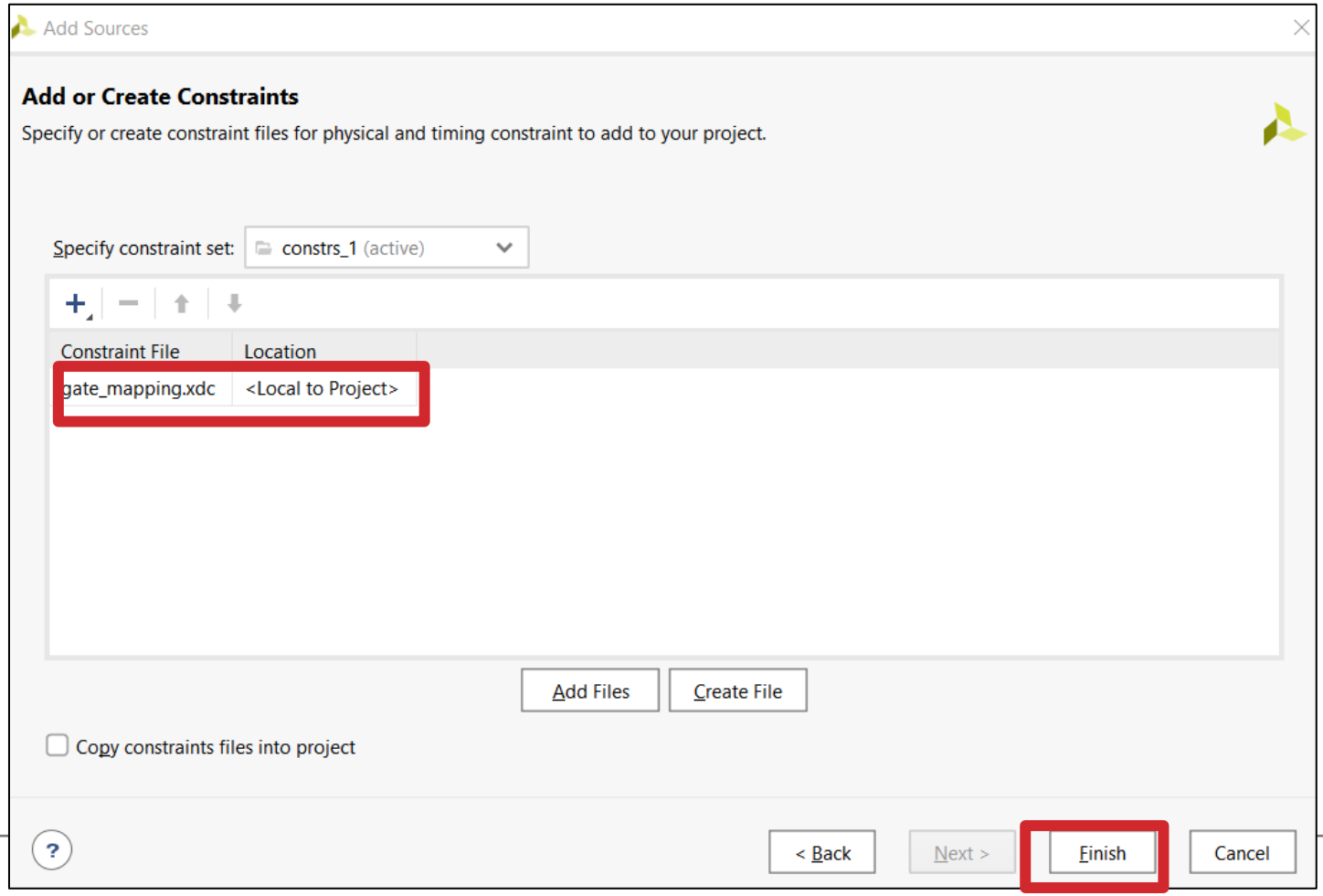
DESIGN EXAMPLE

- Vivado project
  - FPGA programming (mapping) – Create a constraint file



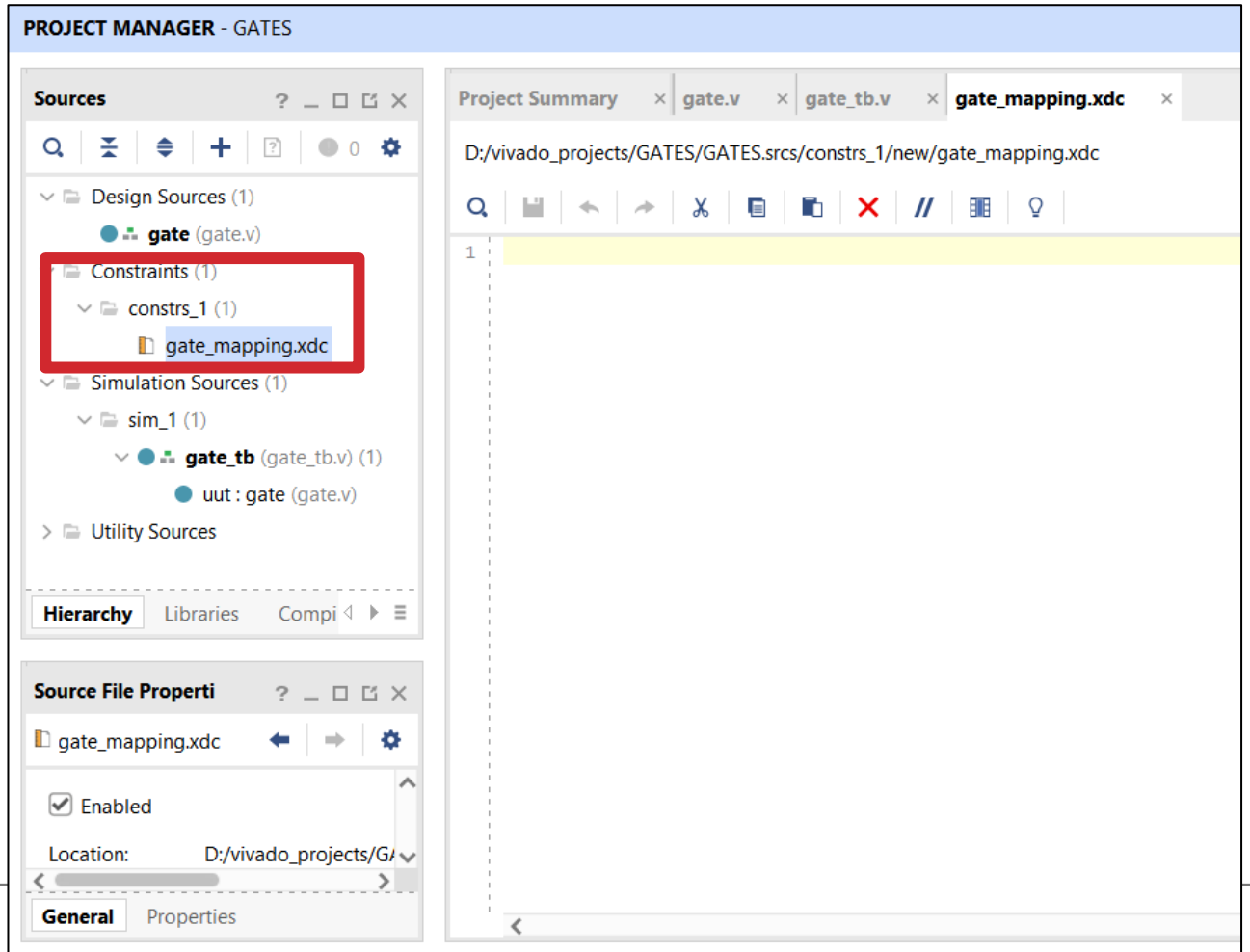
DESIGN EXAMPLE

- Vivado project
  - FPGA programming (mapping) – Create a constraint file



DESIGN EXAMPLE

- Vivado project
  - FPGA programming (mapping) – Create a constraint file



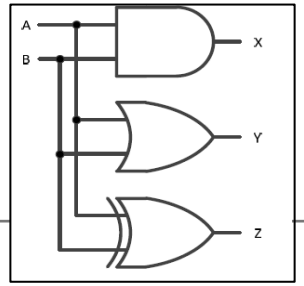
DESIGN EXAMPLE

- Vivado project
  - FPGA programming (mapping) – Create a constraint file

Project Summary | gate.v | gate_tb.v | **gate_mapping.xdc**

D:/vivado_projects/GATES/GATES.srcs/constrs_1/new/gate_mapping.xdc

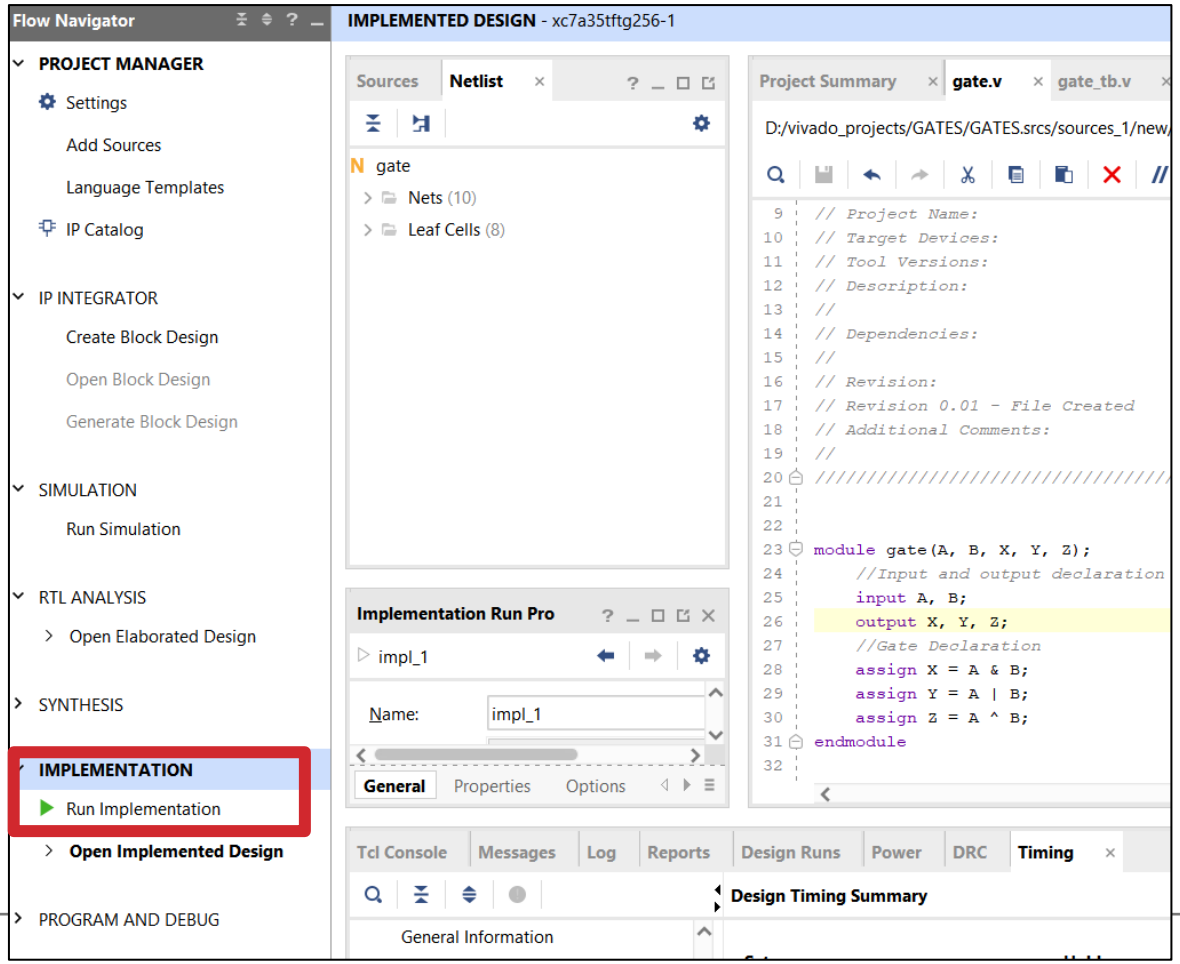
```
1  # Switches
2  set_property -dict { PACKAGE_PIN L5    IOSTANDARD LVCMOS33 } [get_ports { B }];#LSB
3  set_property -dict { PACKAGE_PIN L4    IOSTANDARD LVCMOS33 } [get_ports { A }];
4
5  # LEDs
6  set_property -dict { PACKAGE_PIN J3    IOSTANDARD LVCMOS33 } [get_ports { Z }];#LSB
7  set_property -dict { PACKAGE_PIN H3    IOSTANDARD LVCMOS33 } [get_ports { Y }];
8  set_property -dict { PACKAGE_PIN J1    IOSTANDARD LVCMOS33 } [get_ports { X }];
```



Port Name	Pin Number
A	L4
B	L5
X	J1
Y	H3
Z	J3

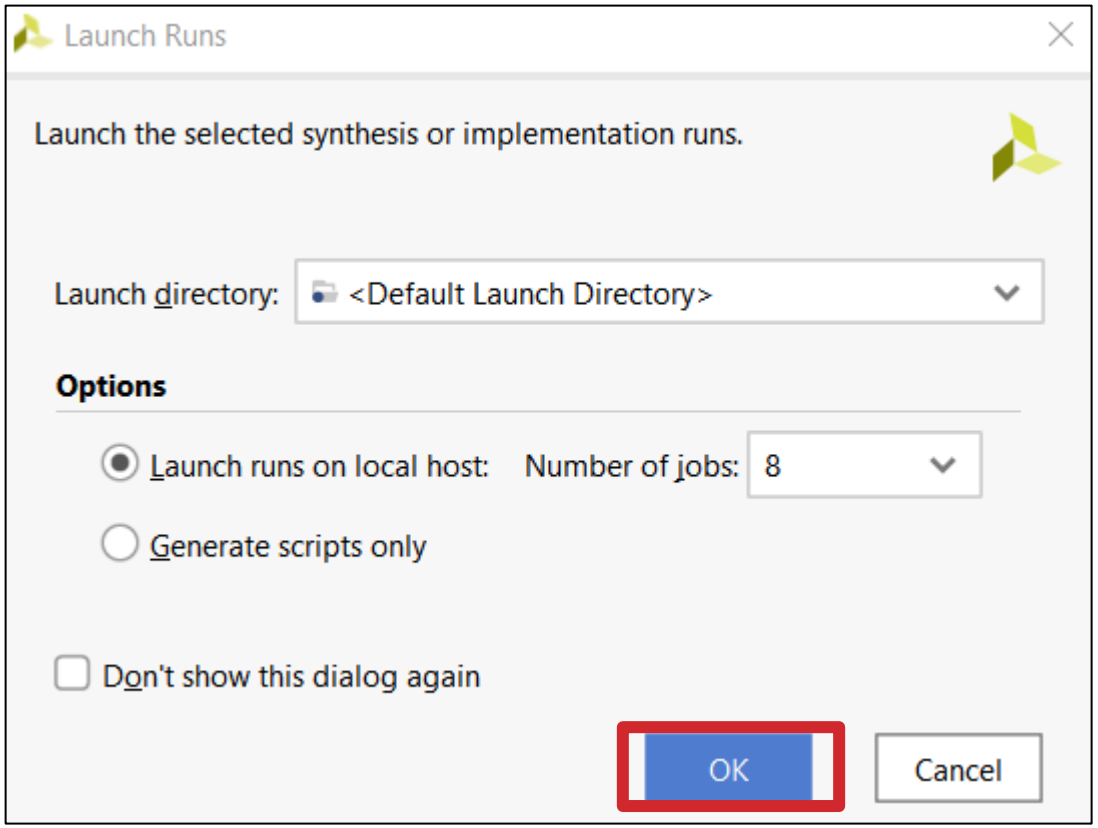
DESIGN EXAMPLE

- Vivado project
  - FPGA programming (mapping) – Implement Design



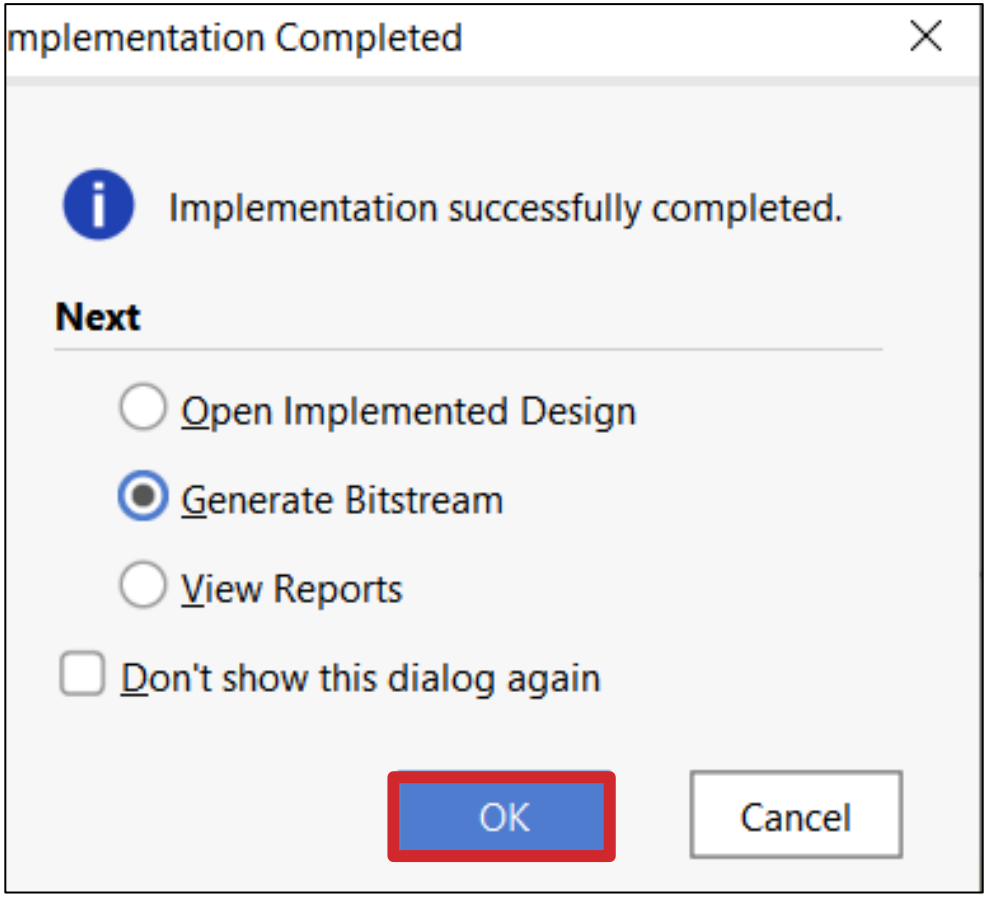
DESIGN EXAMPLE

- Vivado project
  - FPGA programming (mapping) – Implement Design



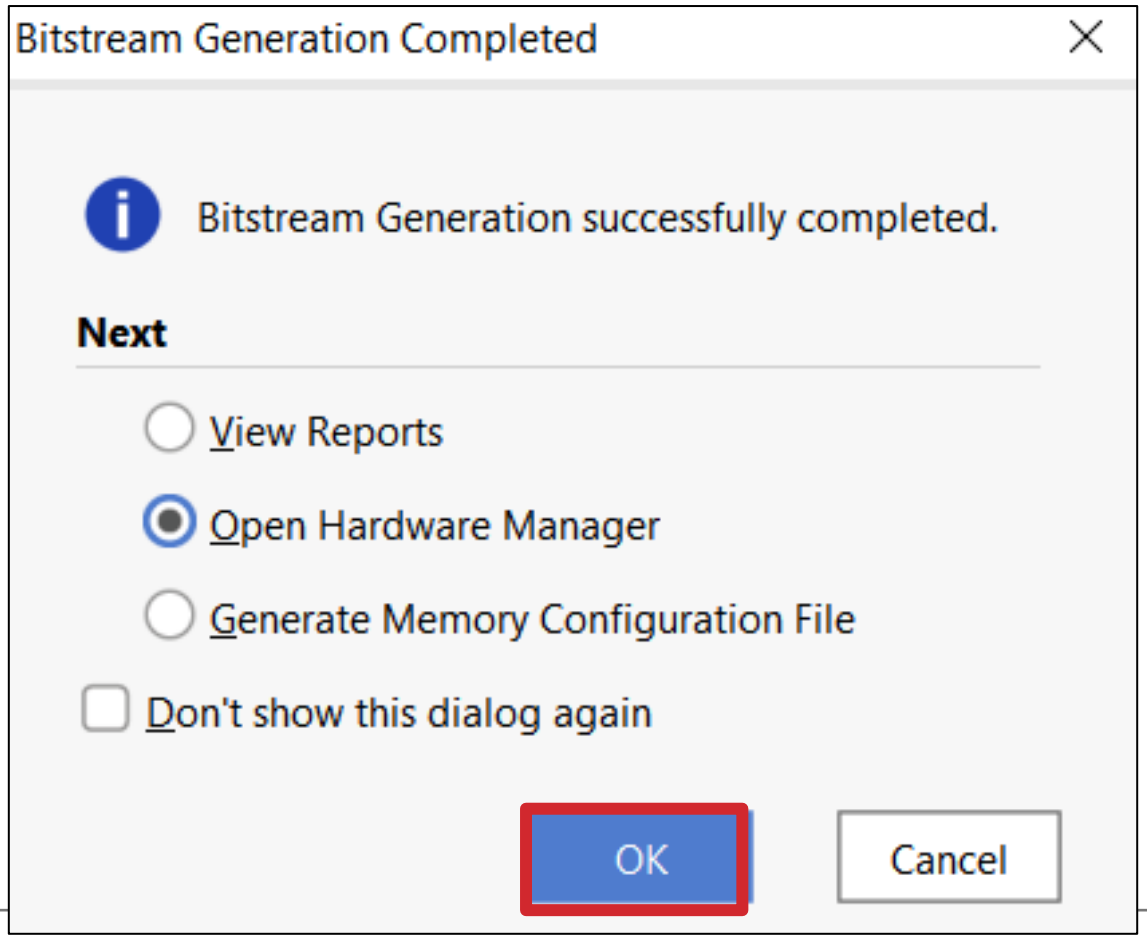
DESIGN EXAMPLE

- Vivado project
  - FPGA programming (mapping) – Generate Programming File



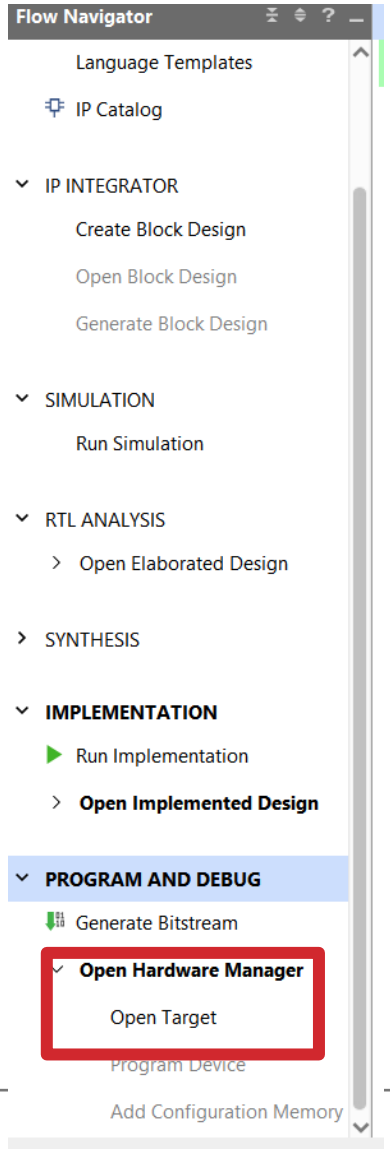
DESIGN EXAMPLE

- Vivado project
  - FPGA programming (mapping) – Generate Programming File



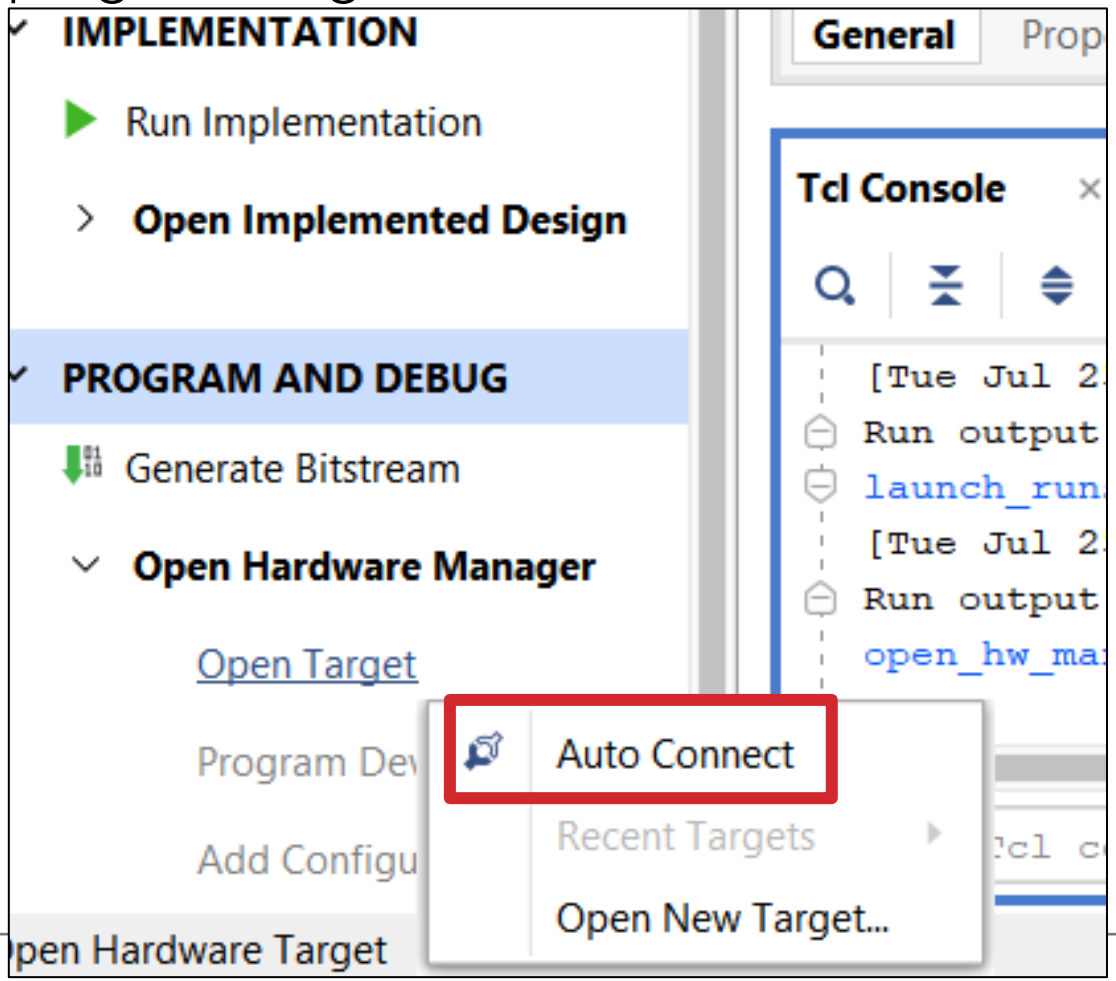
DESIGN EXAMPLE

- Vivado project
  - FPGA programming
    - Connect the FPGA board to the computer and click on Open Target



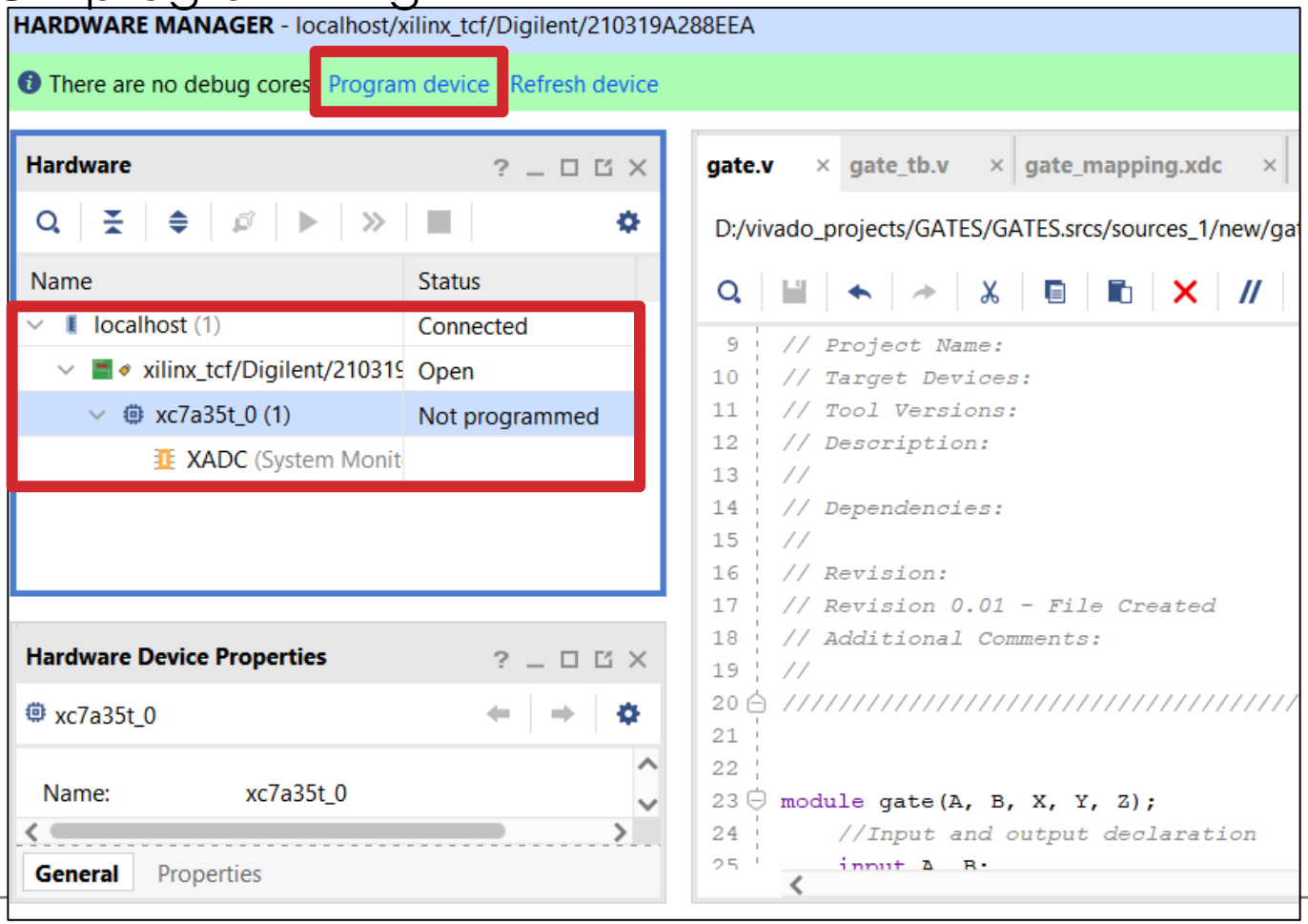
DESIGN EXAMPLE

- Vivado project
  - FPGA programming



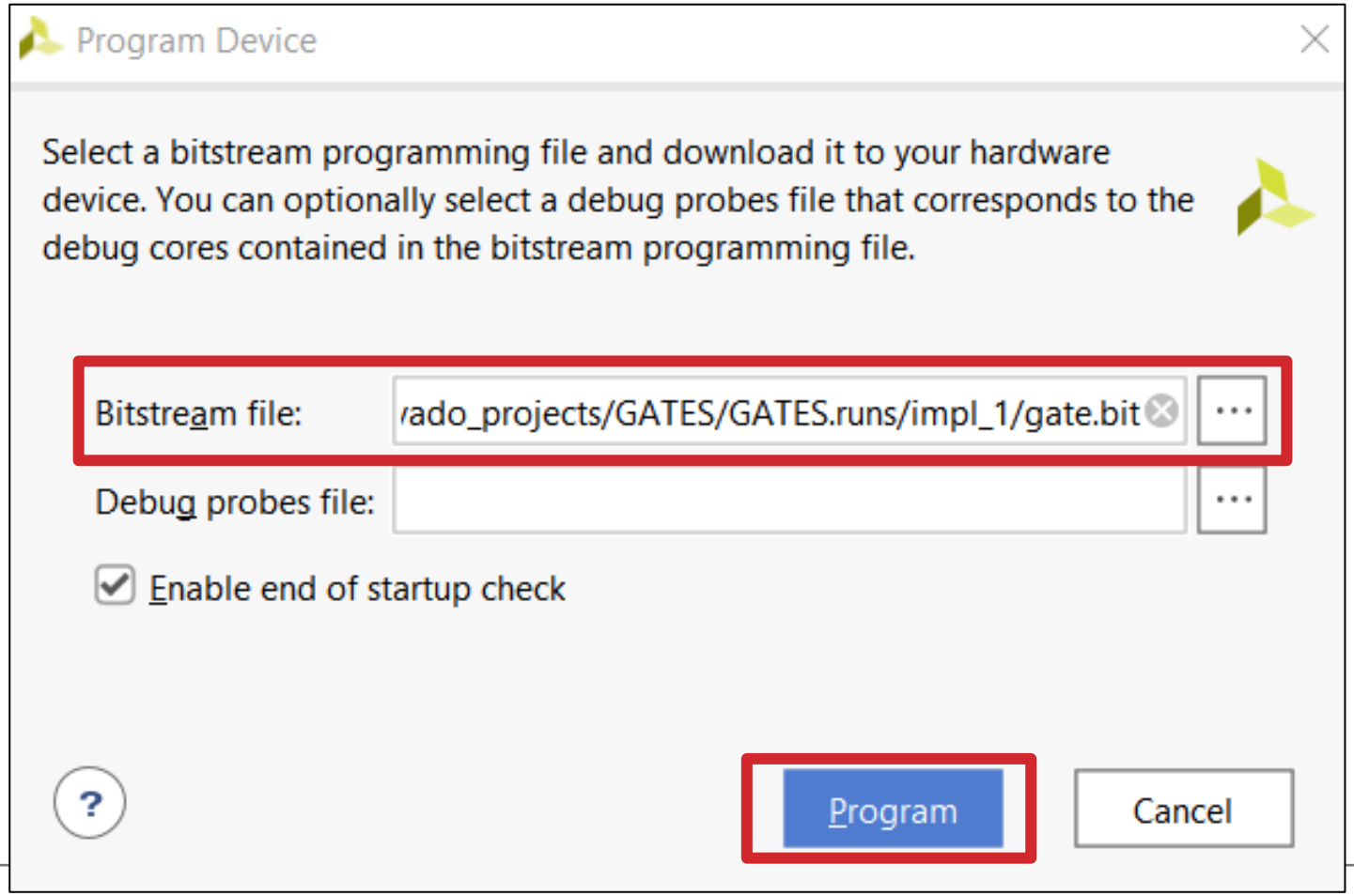
DESIGN EXAMPLE

- Vivado project
  - FPGA programming



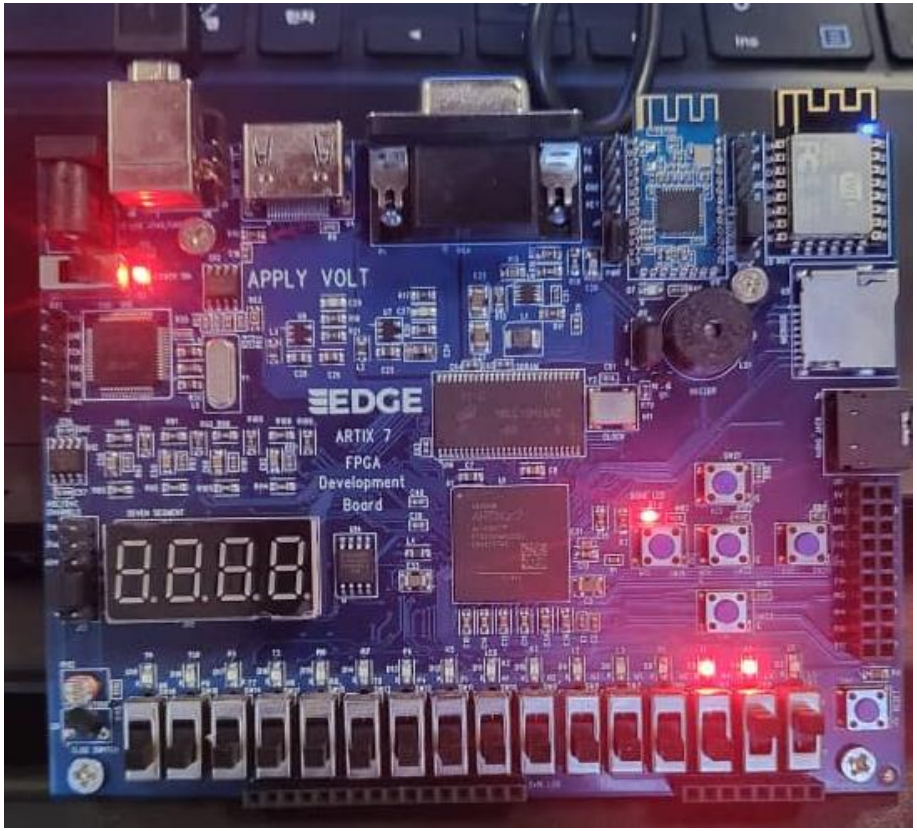
DESIGN EXAMPLE

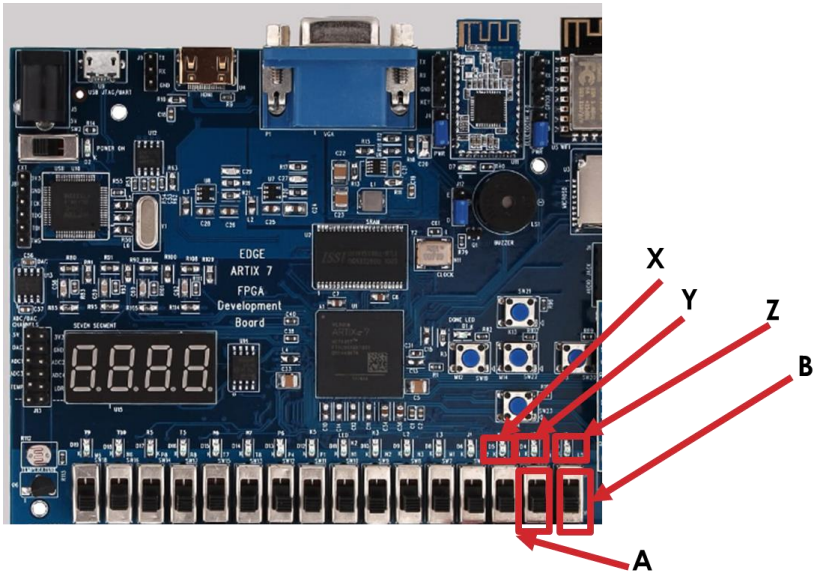
- Vivado project
  - FPGA programming



DESIGN EXAMPLE

- Vivado project
  - FPGA programming





A	B	X	Y	Z
0	0	0	0	0
0	1	0	1	1
1	0	0	1	1
1	1	1	1	0