Advanced Computer Architecture & Advanced Microprocessor System

2ND Semester 2023

Homework

Release Date

03/08/2023

Due Date

Morning Session: 10/08/2023 @ 9:00 AM

Evening Session: 10/08/2023 @ 5:30 PM

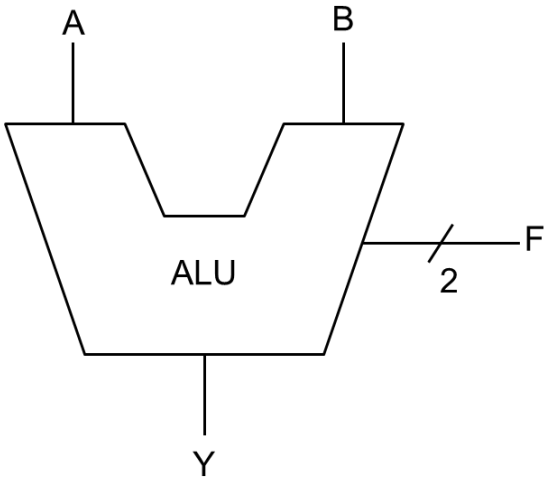
(**Note: Send solutions to your respective class reps**)

Overview

This homework is to help you revise digital logic design which is essential for this course.

1 Combinational Logic Design

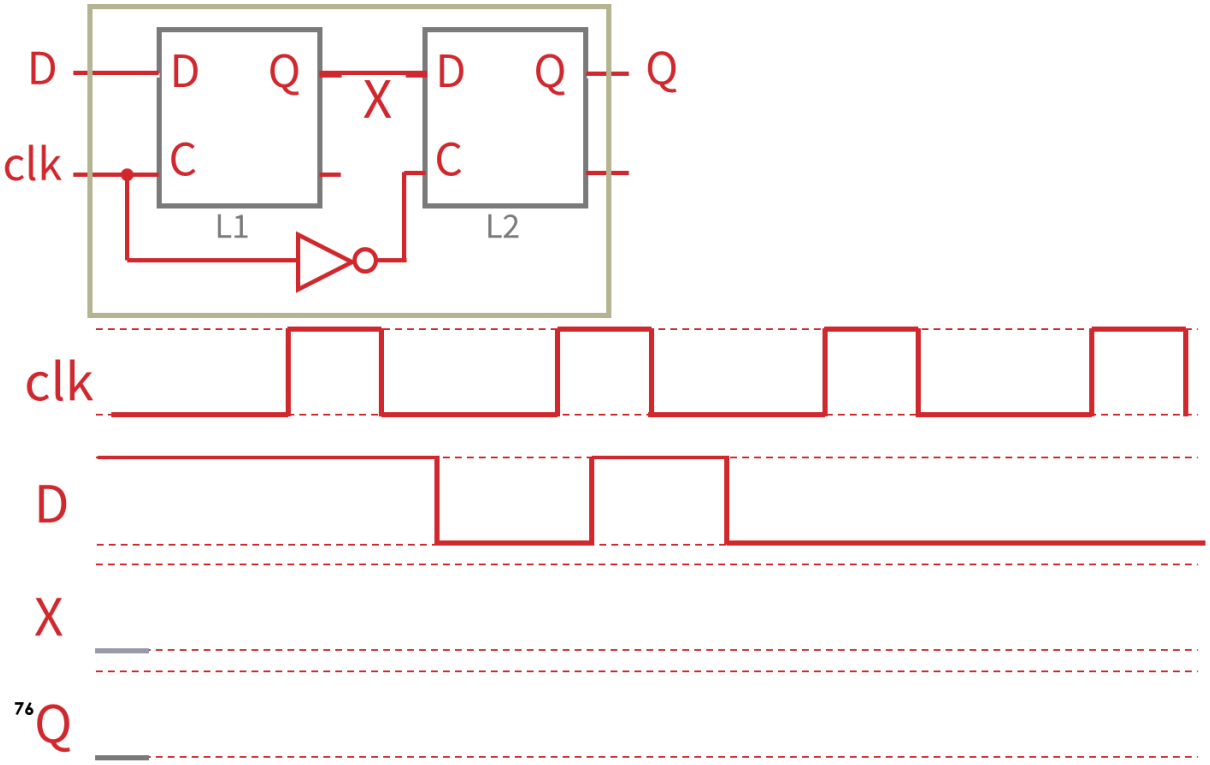
Design the logic circuit of a 2-input ALU to perform the functions in the table below. Make use of the logic gates together with multiplexers and decoders.



F[1:0]	Function
00	A AND B
01	A OR B
10	A XOR B
11	A = ~B

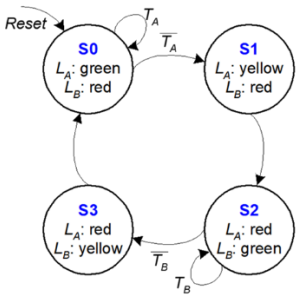
2 Memory Elements

Complete the timing diagram for signals **X** and **Q** for the D flip-flop shown below.



3 Sequential Logic Design

Draw the FSM schematic for the state and output table below using one hot encoding method for the states and outputs.



State Transition Table

Current State	Inputs		Next State
S	T_A	T_B	S'
S0	0	X	S1
S0	1	X	S0
S1	X	X	S2
S2	X	0	S3
S2	X	1	S2
S3	X	X	S0

State	Encoding
S0	0001
S1	0010
S2	0100
S3	1000

Output Table

Current State	Outputs	
	LA	LB
S0	green	red
S1	yellow	red
S2	red	green
S3	red	yellow

Output	Encoding
green	0001
yellow	0010
red	0100