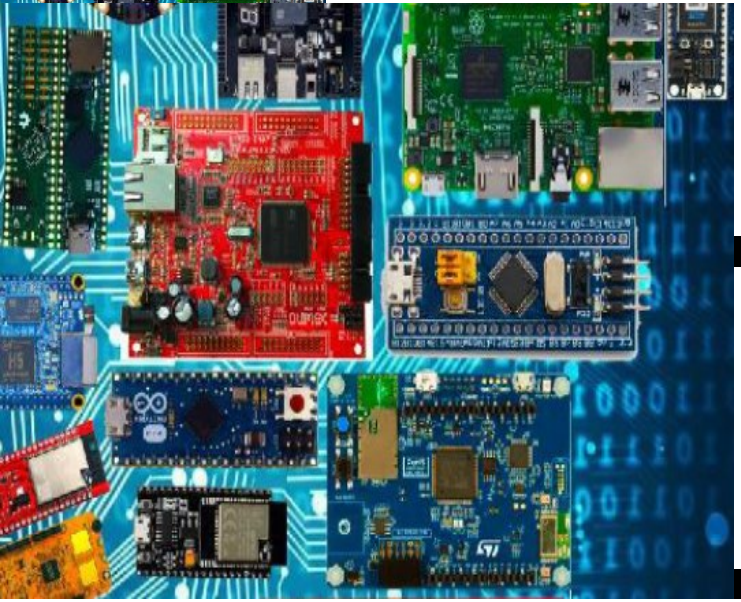


Microprocessor System & Interfacing

MEMORY ELEMENTS

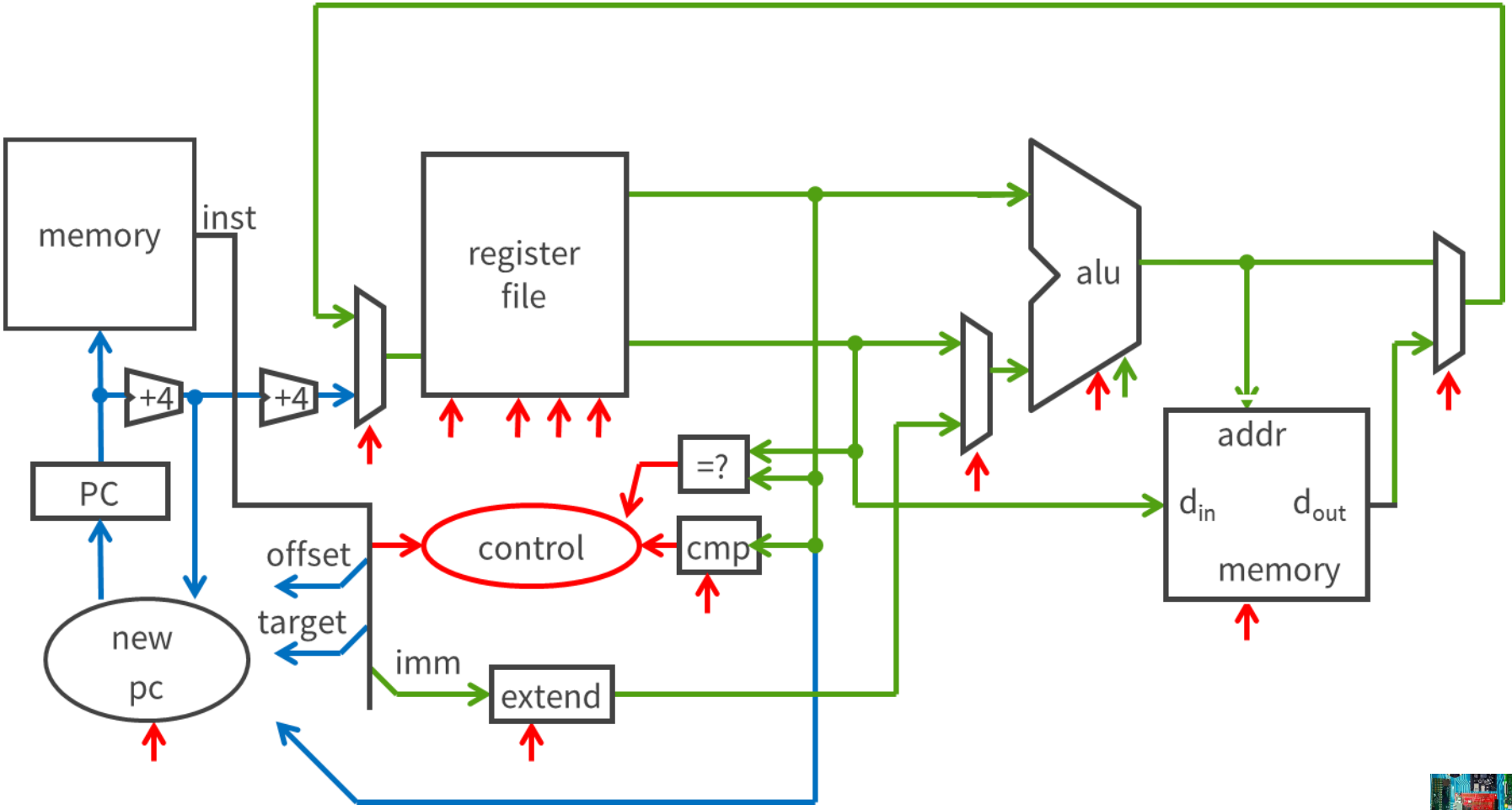
Dennis A. N. Gookyi

CONTENTS

- Memory Elements

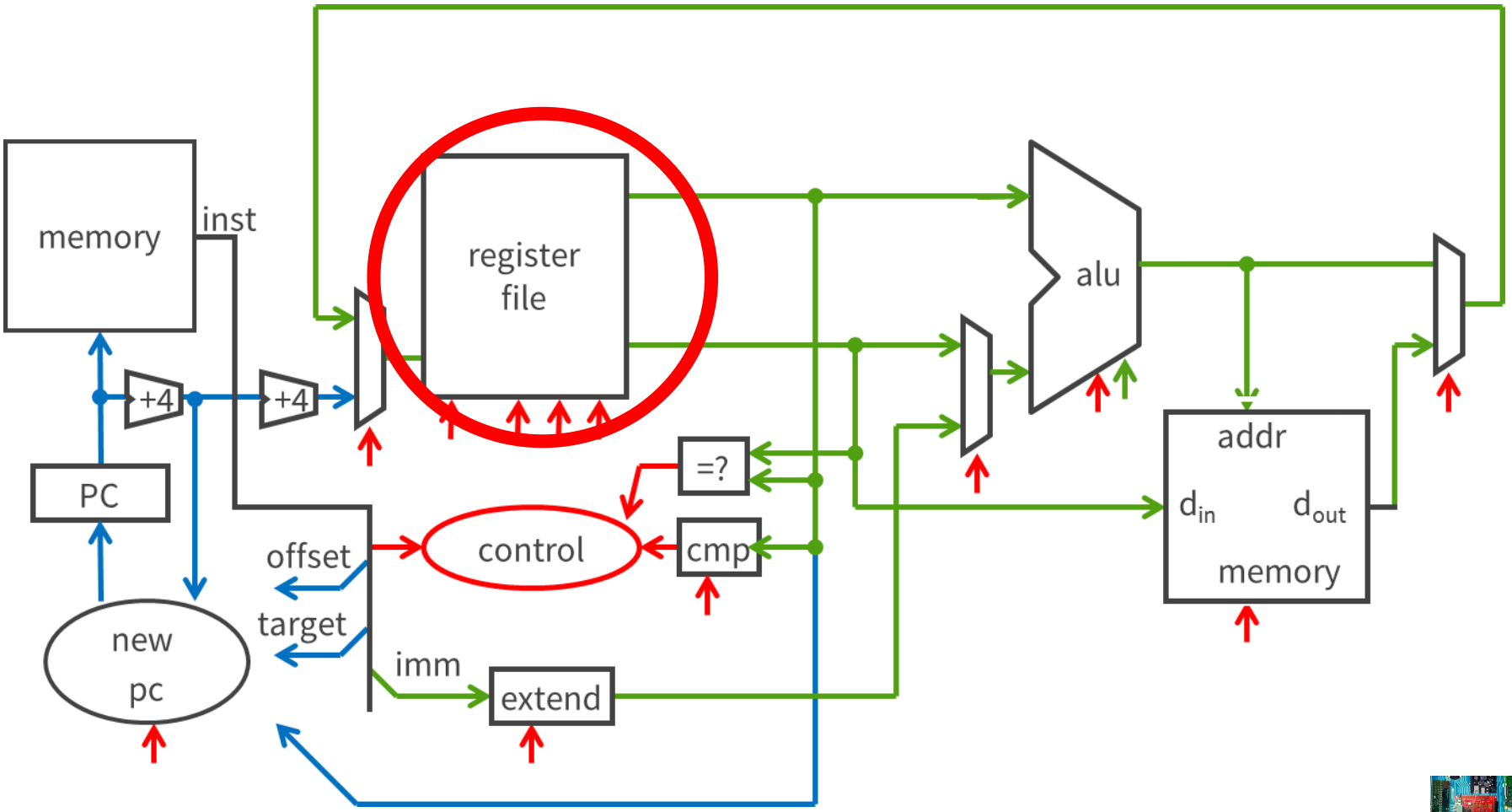
BIG PICTURE: BUILDING A PROCESSOR

- Single cycle processor



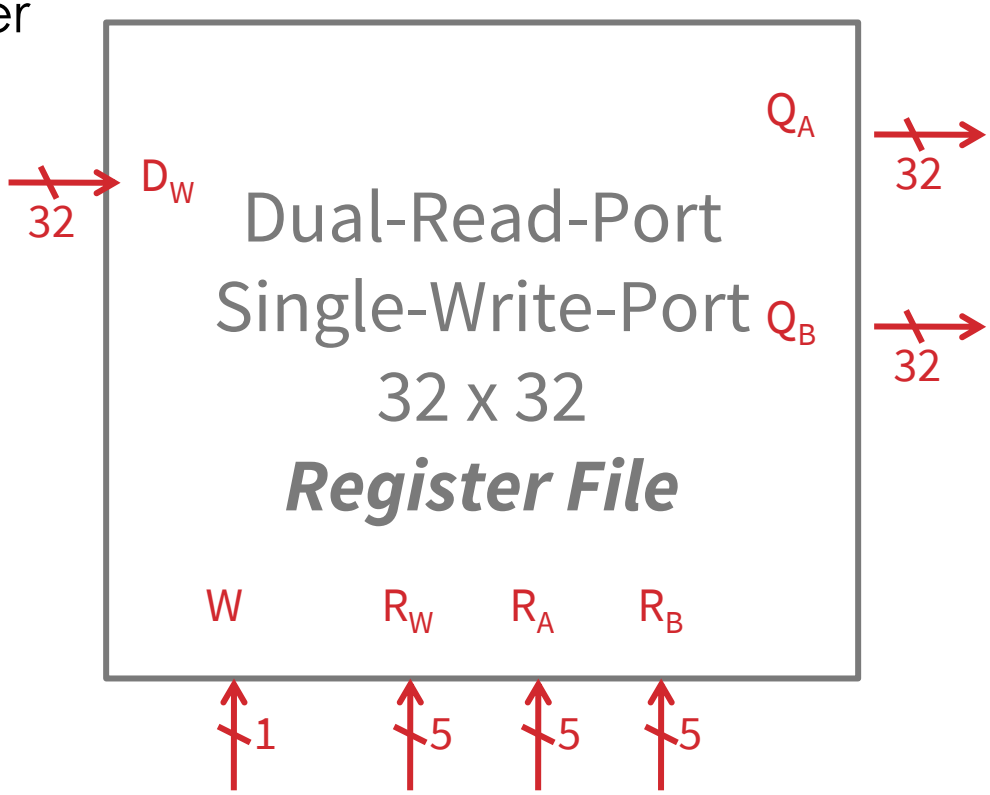
BIG PICTURE: BUILDING A PROCESSOR

- Single cycle processor



REGISTER FILE

- Register file
  - N read/write registers
  - Indexed by register number



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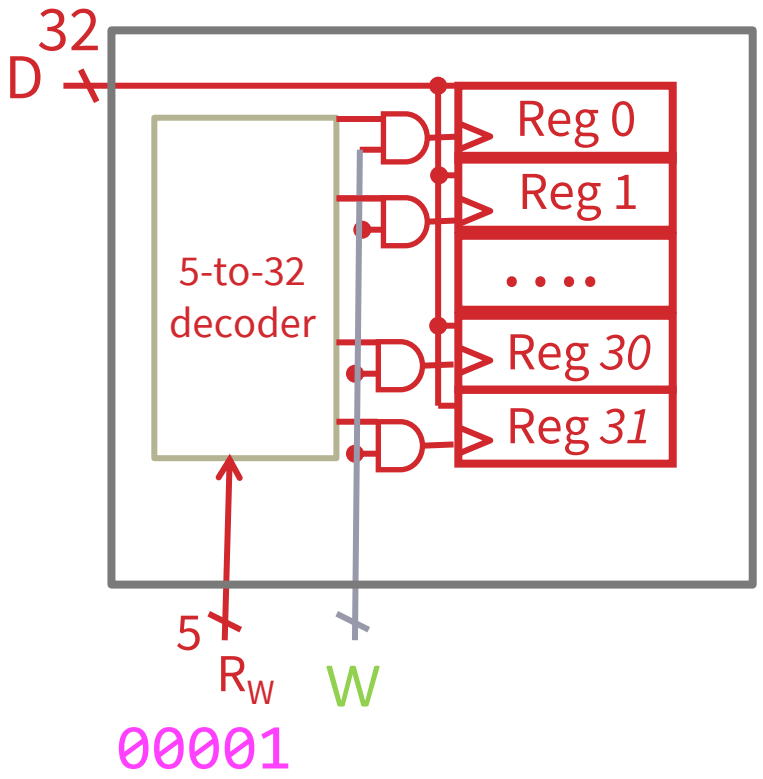


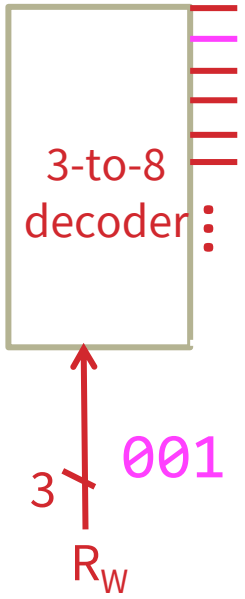

```
addi x1, x0, 10
```

- How to write one register in the register file
  - Need a decoder

REGISTER FILE

- 3-to-8 decoder truth table and circuit

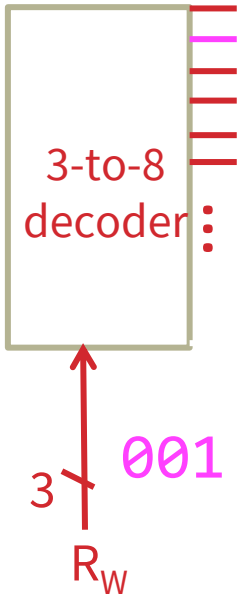
i2	i1	i0	o0	o1	o2	o3	o4	o5	o6	o7
0	0	0								
0	0	1								
0	1	0								
0	1	1								
1	0	0								
1	0	1								
1	1	0								
1	1	1								

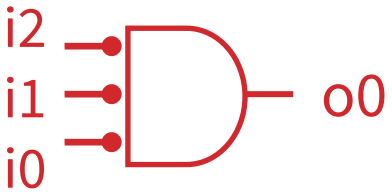


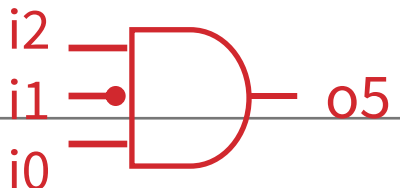
REGISTER FILE

- 3-to-8 decoder truth table and circuit

i2	i1	i0	o0	o1	o2	o3	o4	o5	o6	o7
0	0	0	1							
0	0	1		1						
0	1	0			1					
0	1	1				1				
1	0	0					1			
1	0	1						1		
1	1	0							1	
1	1	1								1







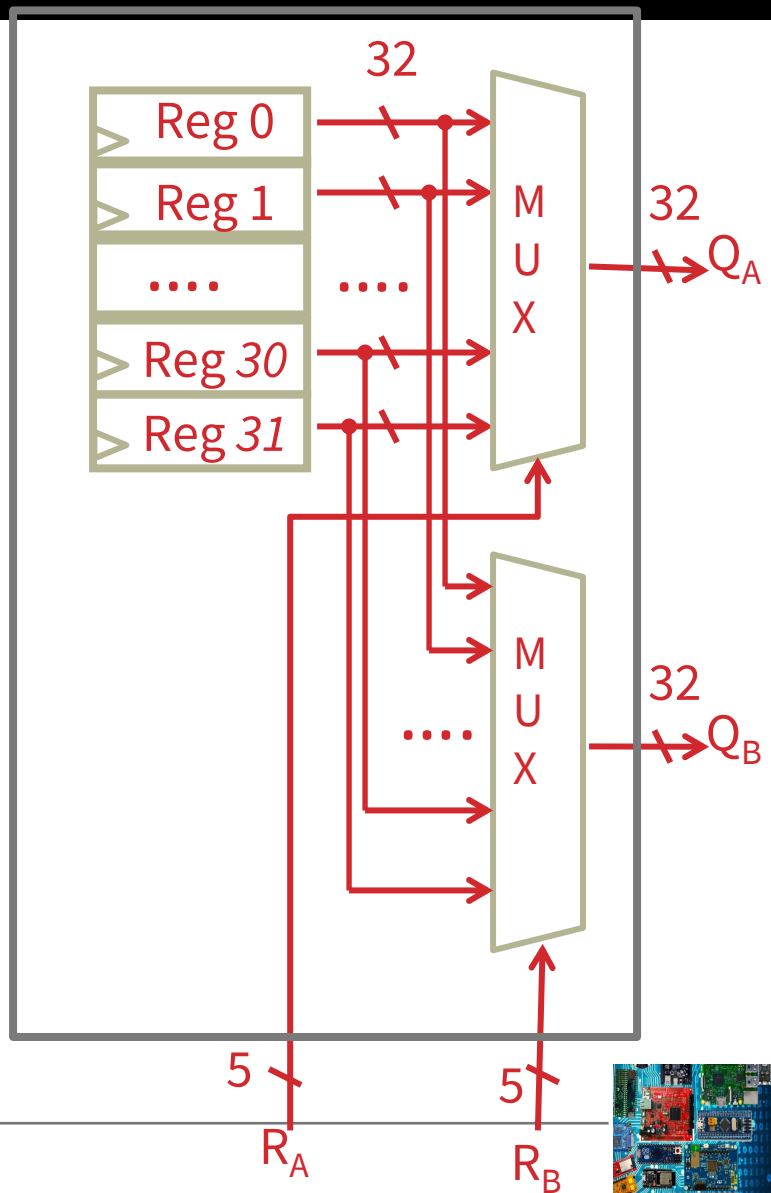
REGISTER FILE

- Register file
  - N read/write registers
  - Indexed by register number

```
add x1, x0, x5
```

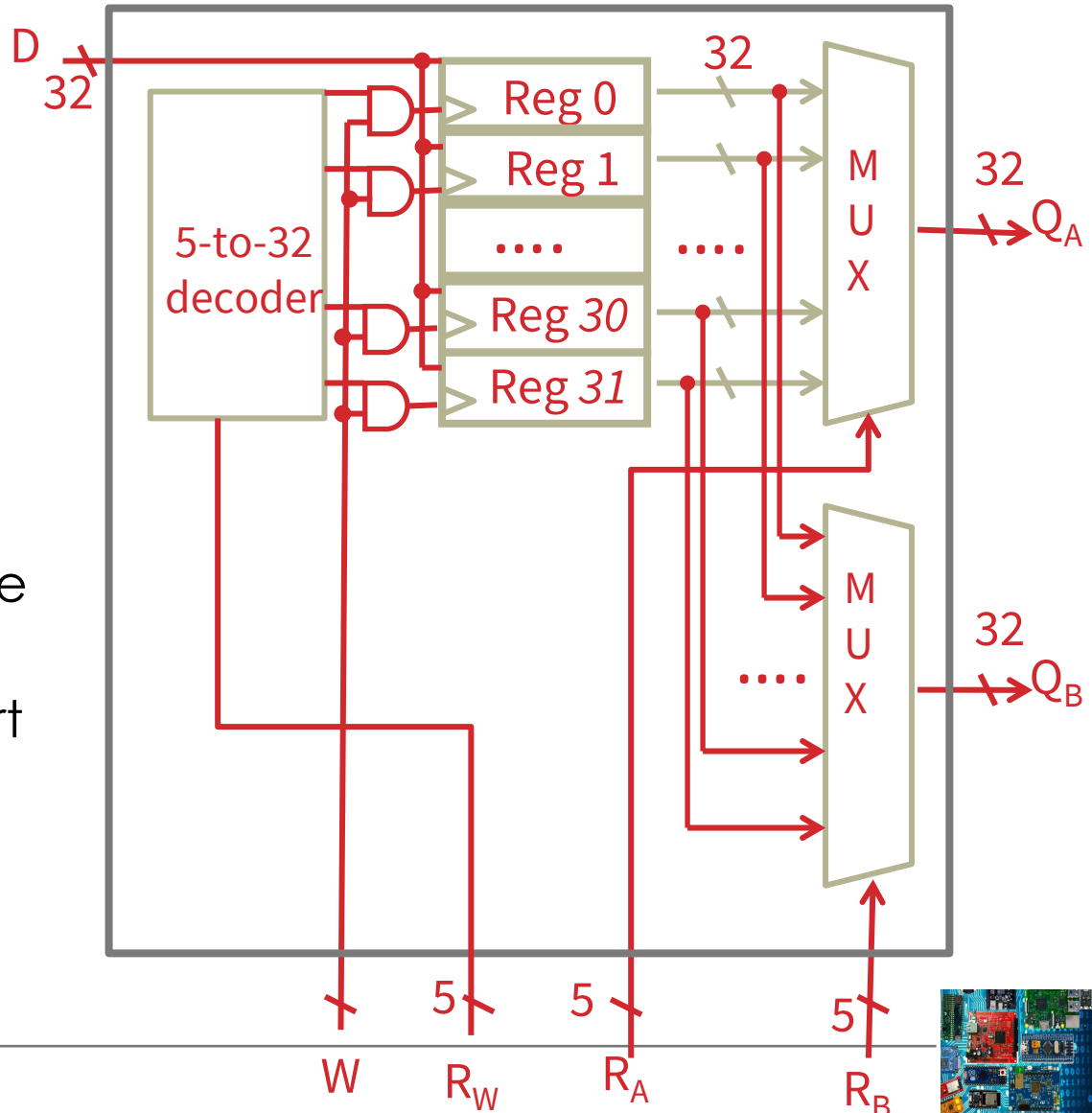
How to read from two registers?

- Need a multiplexor



REGISTER FILE

- Register file
  - N read/write registers
  - Indexed by register number
- Implementation:
  - D flip flops to store bits
  - Decoder for each write port
  - Mux for each read port



REGISTER FILE

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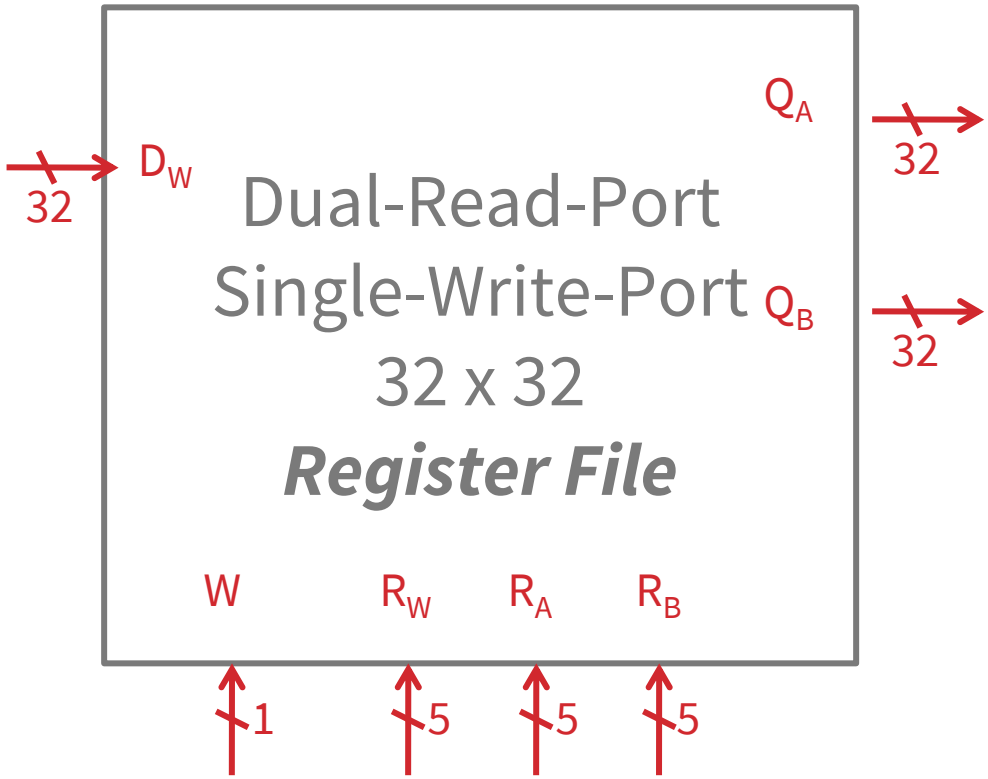


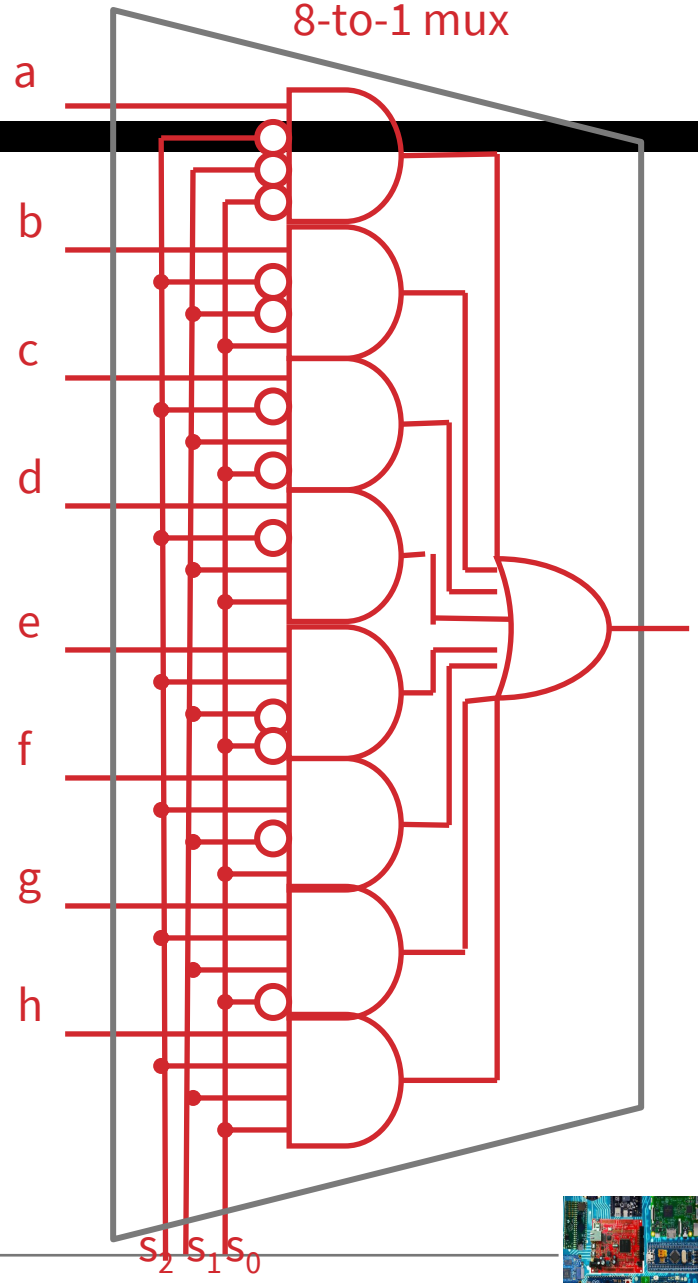
REGISTER FILE

- Register file
  - \+ Very fast (a few gate delays for both read and write)
  - \+ Adding extra ports is straightforward
  - – Doesn't scale

    e.g. 32Mb register file with 32 bit registers

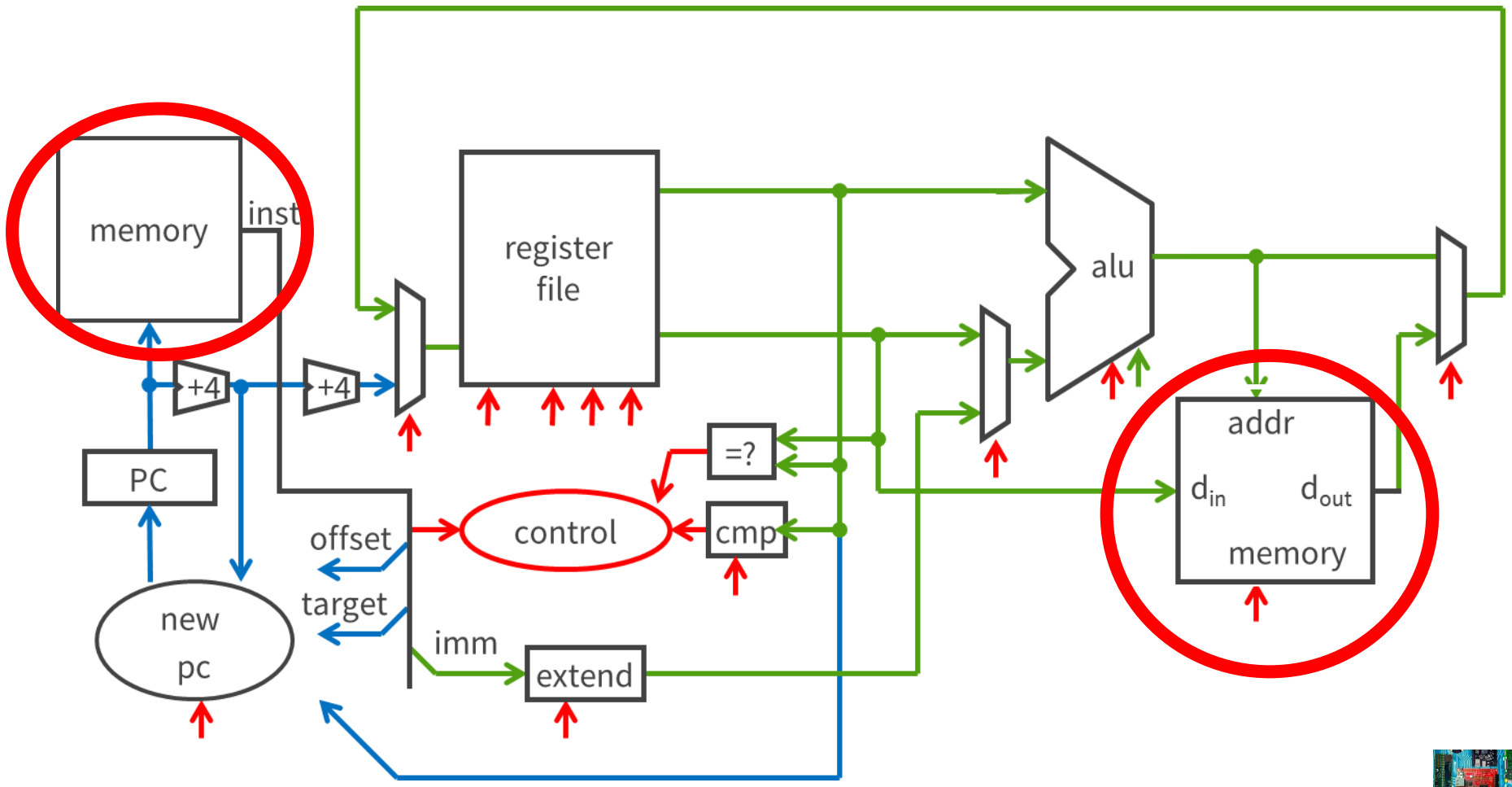
    Need 32x 1M-to-1 multiplexor and 32x 20-to-1M decoder

    How many logic gates/transistors?



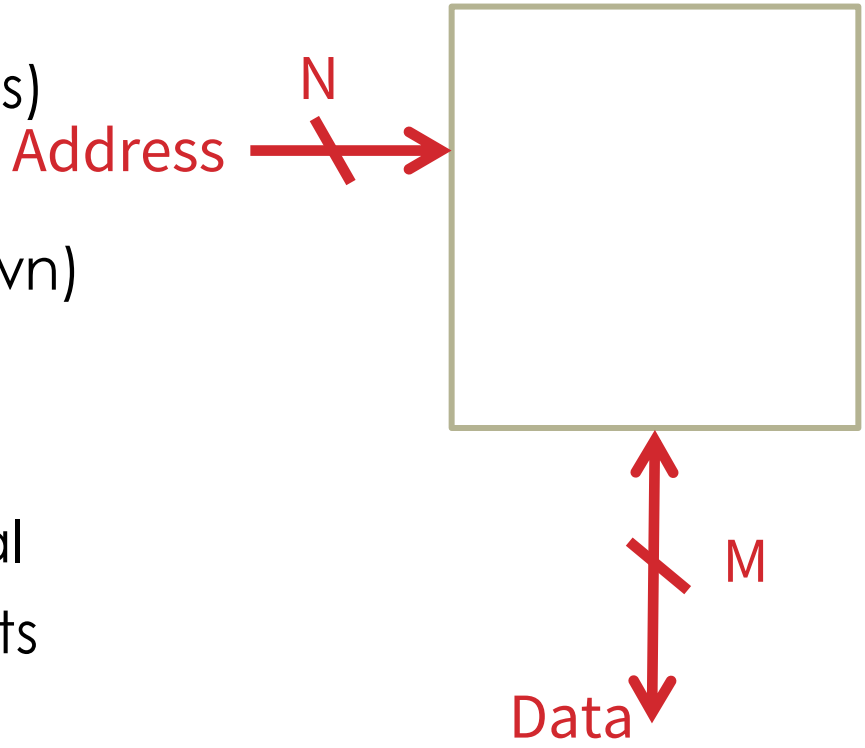
BIG PICTURE: BUILDING A PROCESSOR

- Single cycle processor



MEMORY

- Storage Cells + bus
- Inputs: Address, Data (for writes)
- Outputs: Data (for reads)
- Also need R/W signal (not shown)

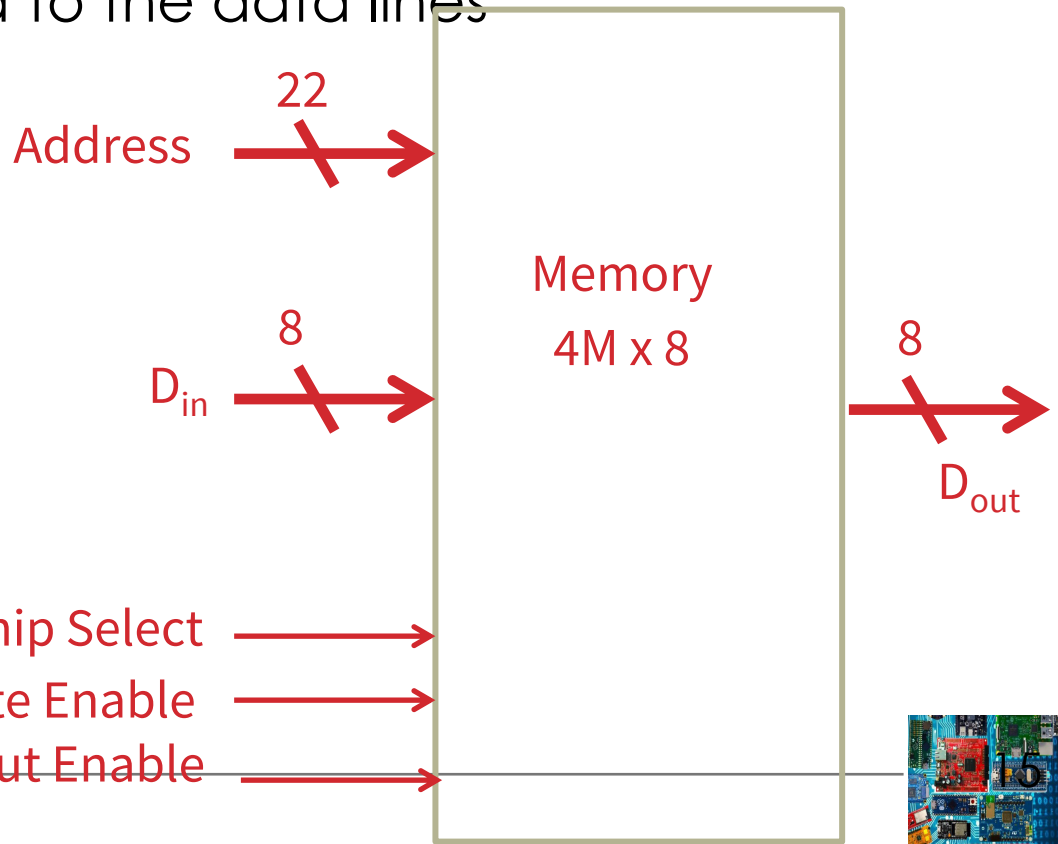


- N address bits -> 2^N words total
- M data bits -> each word M bits

- How many address bits are necessary for a 4M x 8 SRAM module?
  - 4M word lines that are each 8 bits wide

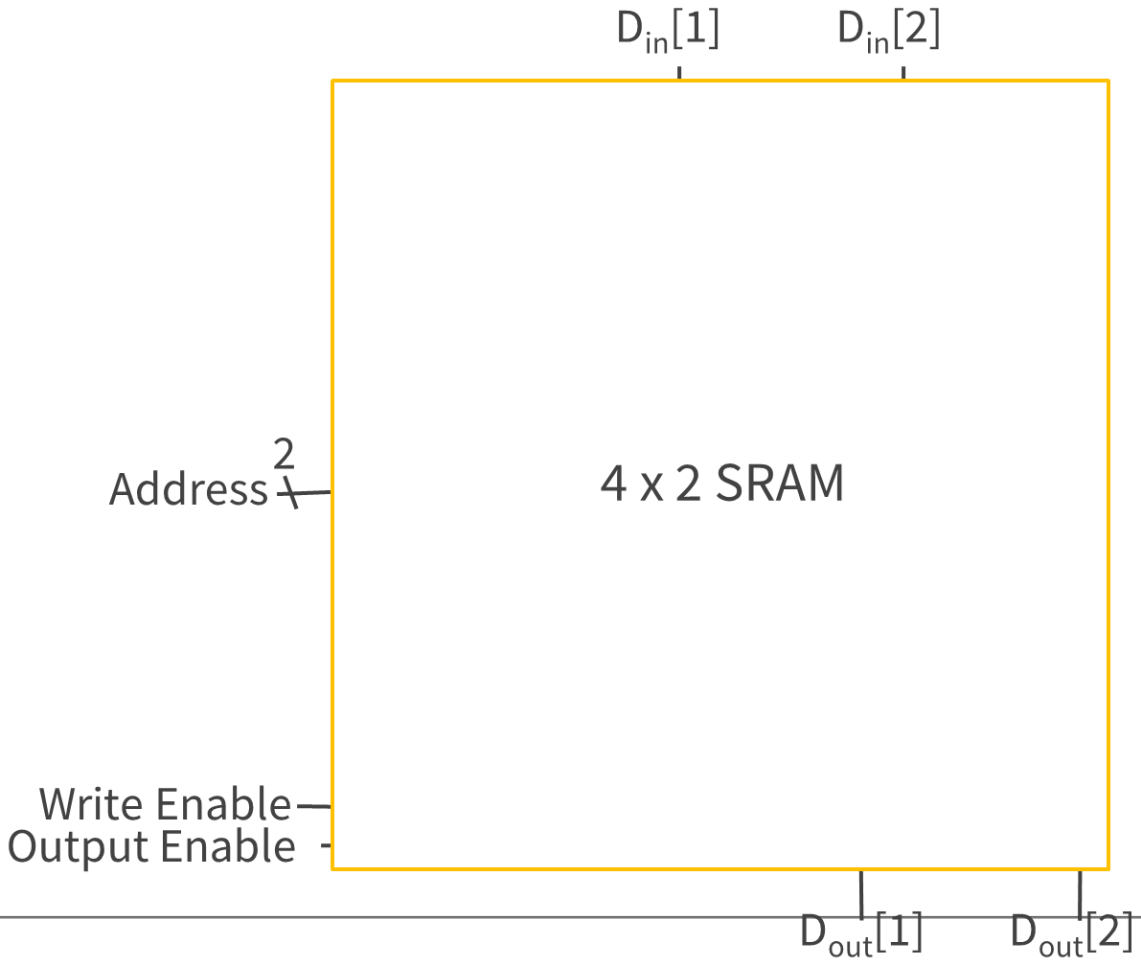
MEMORY

- Storage Cells + bus
- Decoder selects a word line
- R/W selector determines access type
- Word line is then coupled to the data lines



MEMORY

- How do we design a 4 x 2 Memory Module?
  - 4 word lines that are each 2 bits wide



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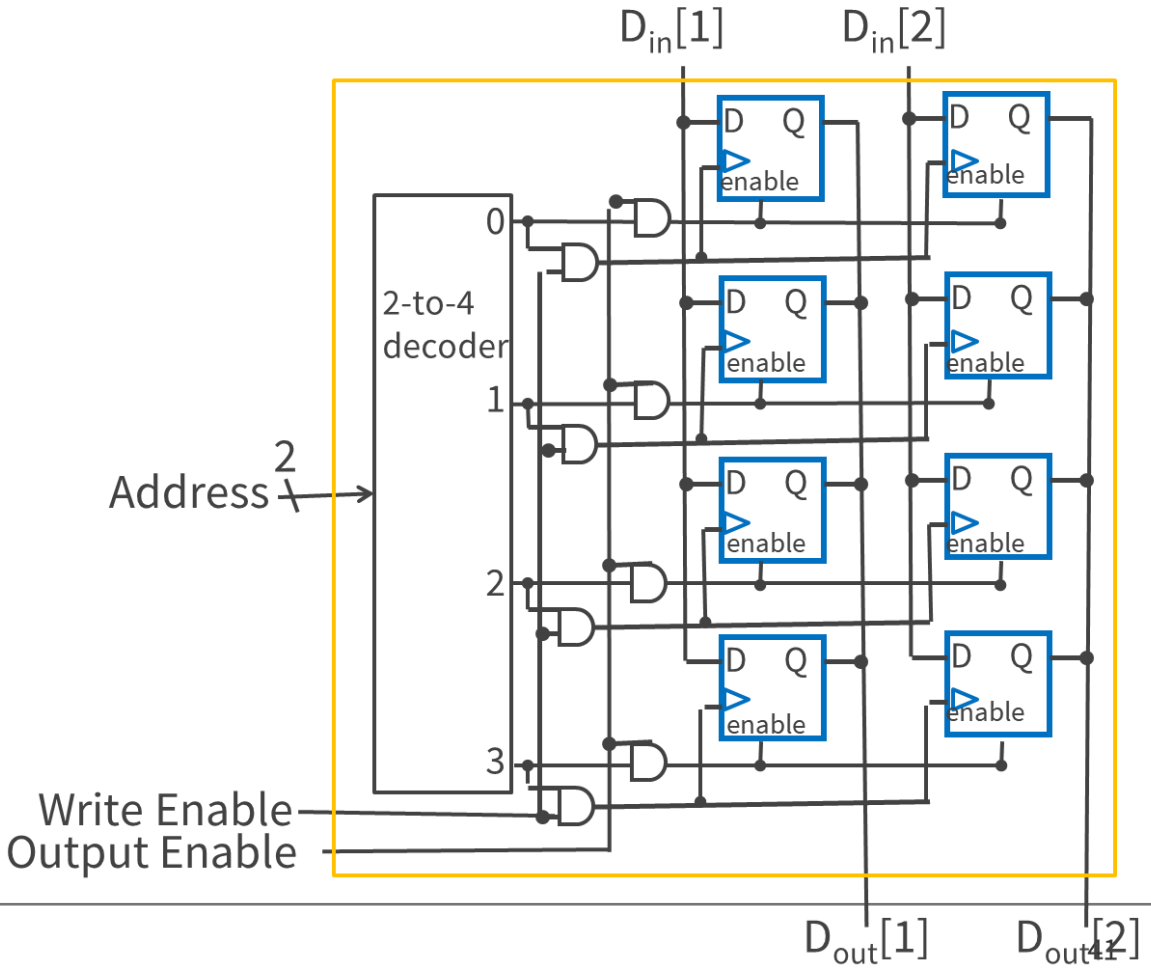

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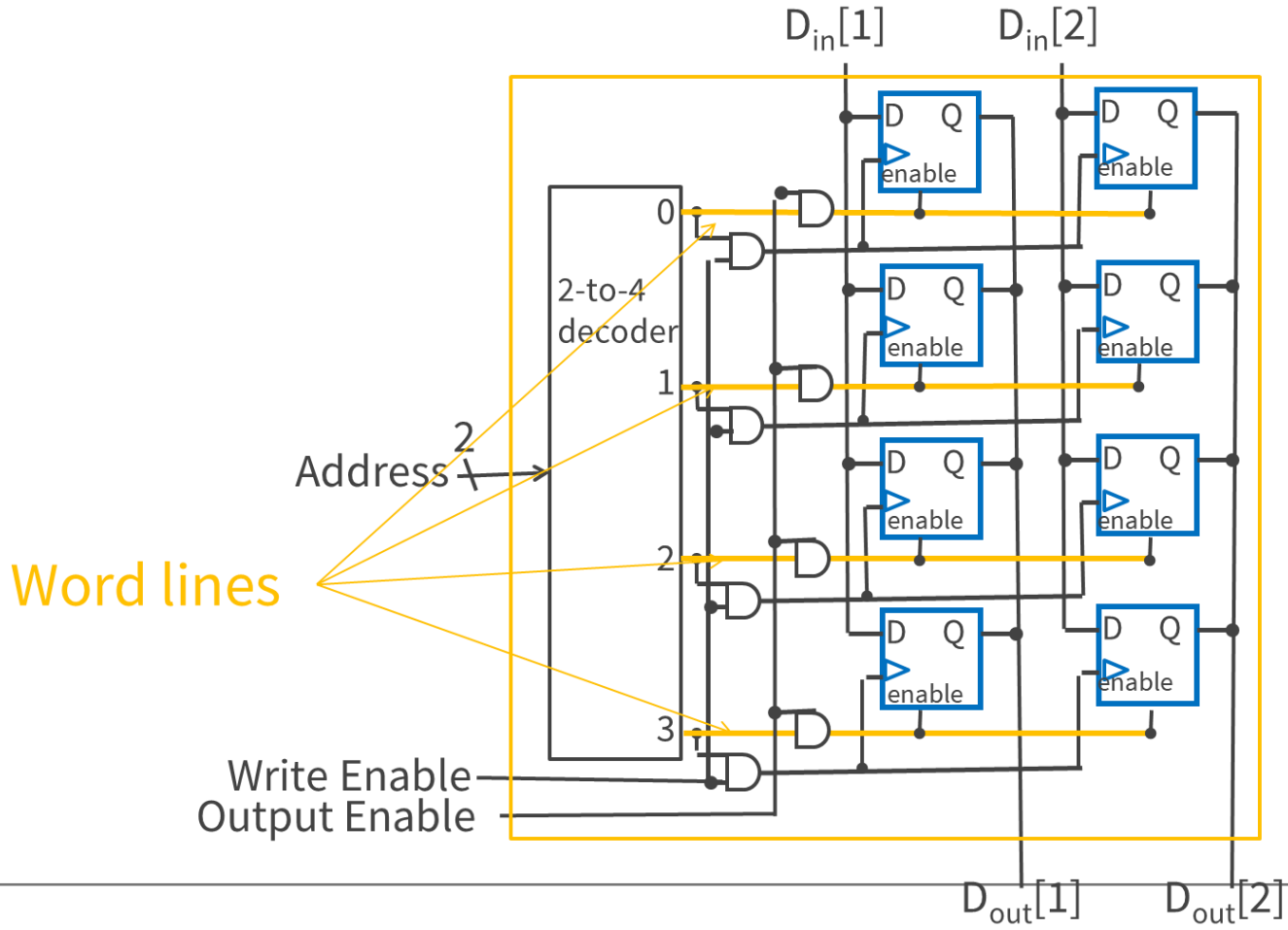

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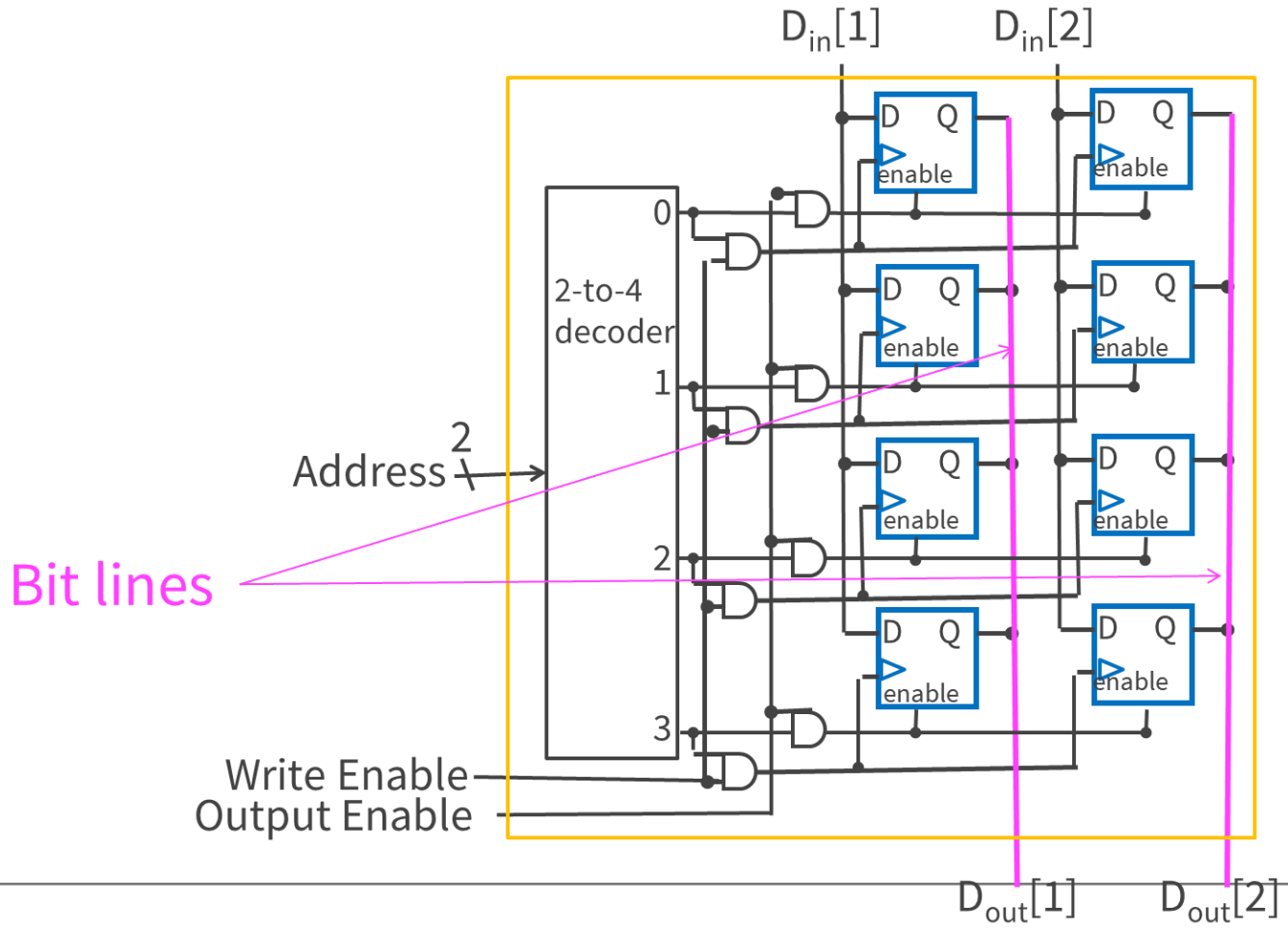

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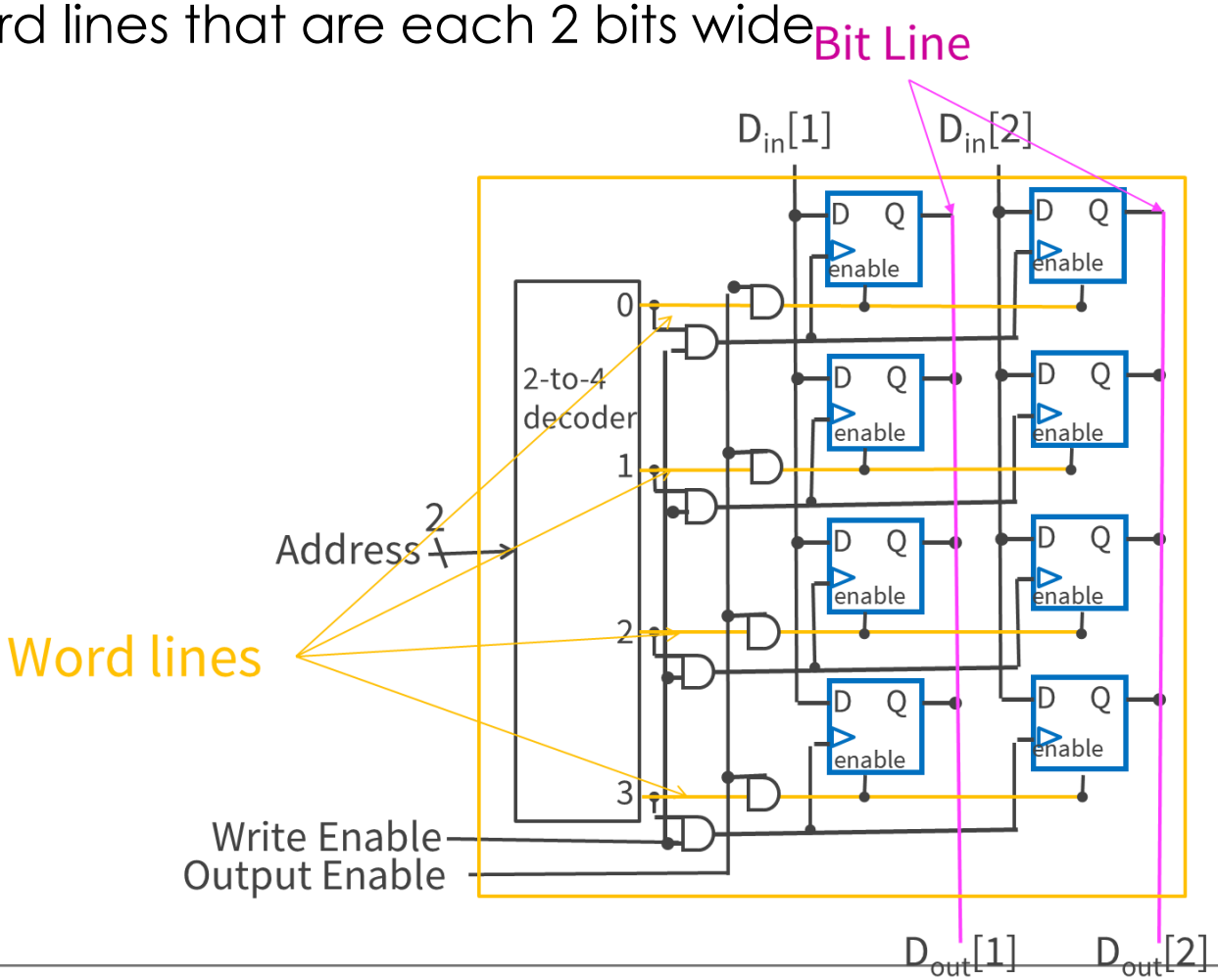
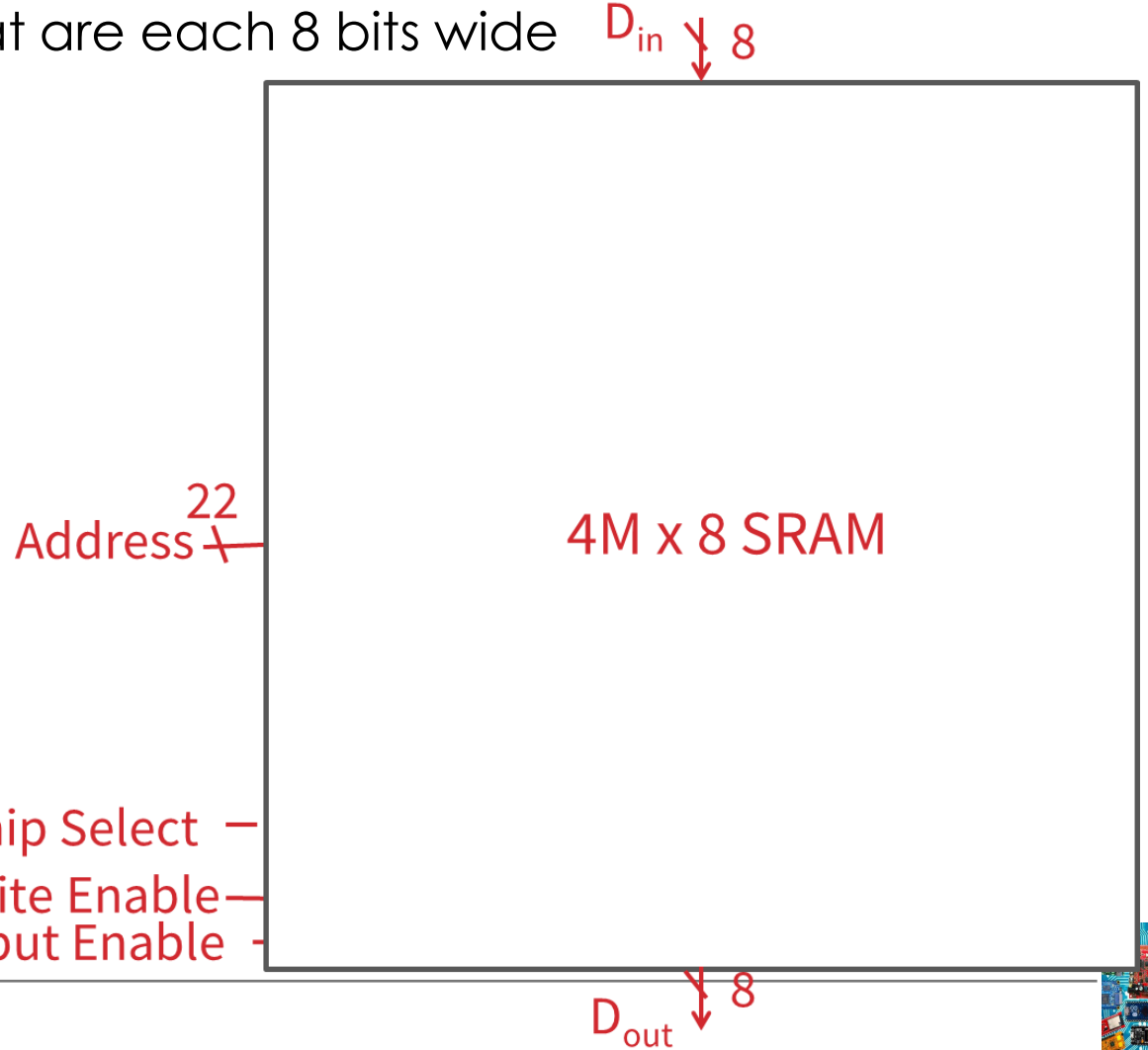


MEMORY

- How do we design a 4M x 8 Memory Module?
  - 4M word lines that are each 8 bits wide



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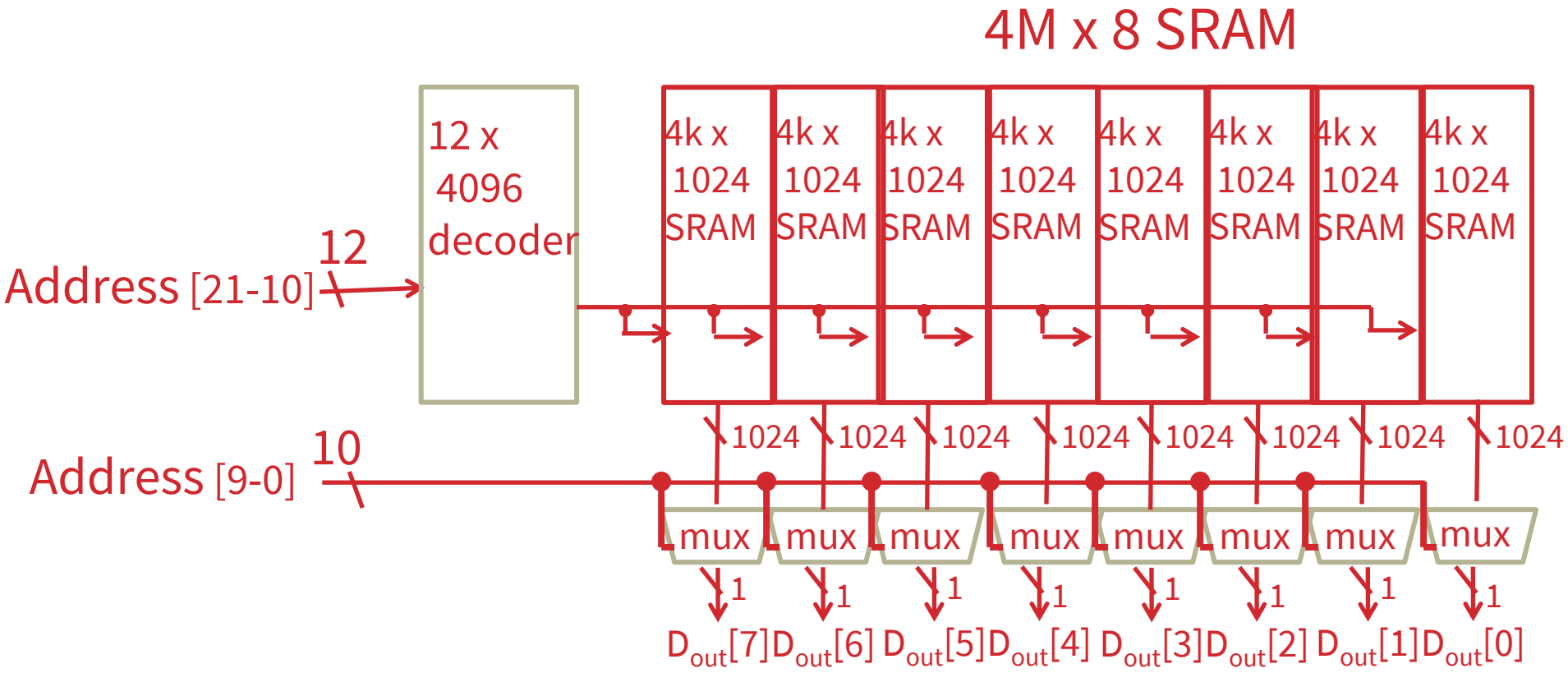

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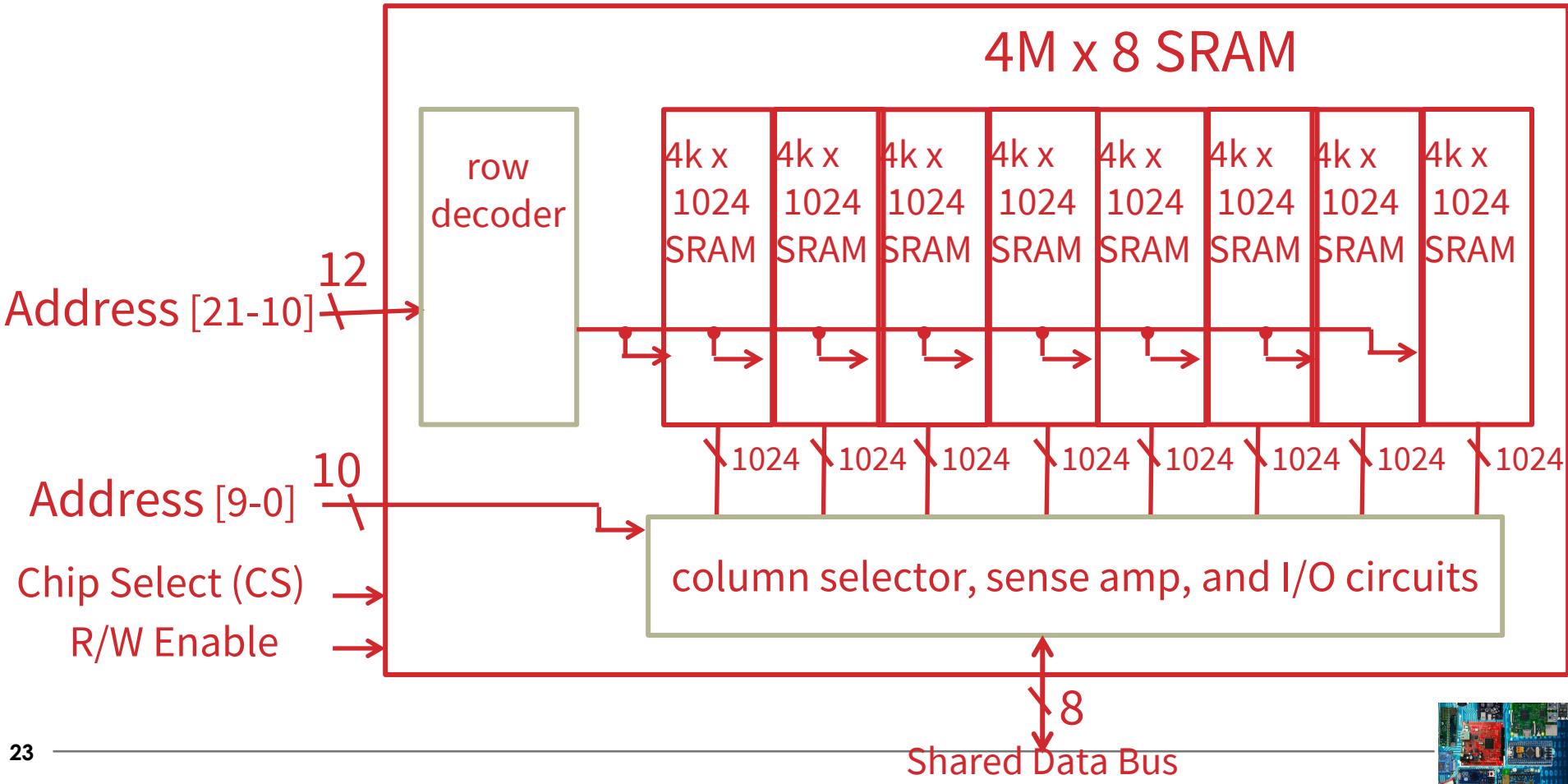

MEMORY

- Register File tradeoffs
  - + Very fast (a few gate delays for both read and write)
  - + Adding extra ports is straightforward
  - – Expensive, doesn't scale
  - – Volatile
- Volatile Memory alternatives: SRAM, DRAM, …
  - – Slower
  - + Cheaper, and scales well
  - – Volatile
- Non-Volatile Memory (NV-RAM): Flash, EEPROM, …
  - + Scales well
  - – Limited lifetime; degrades after 100000 to 1M writes