TINYML IMPLEMENTATION: MCU vs FPGA
SEMINAR SCHEDULE: FRIDAY, 2:00 PM

Week	Topic	Content	Presenter
1: Jun 16	Platform Selection: TinyML Development and Deployment with TensorFlow	1.1 Embedded Devices (TinyML Development Boards) 1.2 Machine Learning 1.3 Deep Learning 1.4 Tiny Machine Learning (TinyML) 1.5 TinyML Implementation	Fortunatus
	Platform Selection: TinyML Development and Deployment with Edge Impulse	1.6 Introduction to TensorFlow/Edge Impulse 1.7 TensorFlow/Edge Impulse Installation Guide 1.8 TinyML on TensorFlow/Edge Impulse: From Specification to Inference (Keyword Spotting Example) 1.9 Sustainability of TinyML: Assessing the Environmental Impacts of Machine Learning on Embedded Devices	Ewura
2: Jun 30	Image Data Collection	2.1 Survey of Crop Diseases in Ghana 2.2 Selecting a Crop Disease 2.3 Crop Disease Data Collection	Ewura
3: Jul 14	Dataset Preparation	3.1 Data Pre-processing Techniques 3.2 Data Augmentation Techniques 3.3 Data Labelling 3.4 Crop Disease Dataset Categorization: Training, Test, and Validation Sets	Fortunatus
4: Jul 28	Deep Learning Model Selection	4.1 Introduction to Deep Learning 4.2 Convolutional Neural Networks 4.3 Survey of Common CNNs and Their Resource Utilization 4.4 CNNs for TinyML 4.5 TinyML Model Selection/Design for Crop Disease Identification 4.6 TinyML Model Training 4.7 TinyML Model Conversion 4.8 TinyML Model Inference 4.9 TinyML Model Evaluation Metrics	Fortunatus
5: Aug 11	Deep Learning Model Optimization	5.1 Introduction to Model Optimization 5.2 Model Optimization Metrics 5.3 Model Optimization Technique: Pruning 5.4 Model Optimization Technique: Quantization 5.5 Optimized vs Unoptimized TinyML Models for Crop Disease Identification	Ewura
6: Aug 25	Deep Learning Model Parameters Generation based on Hardware Metrics	6.1 Deep Learning Software Evaluation Metrics 6.2 Constraints of Low-cost Devices 6.3 Deep Learning Hardware Evaluation Metric: Latency 6.4 Deep Learning Hardware Evaluation Metric: Memory 6.5 Deep Learning Hardware Evaluation Metric: Hardware Gate Count 6.6 Ideal TinyML Model Based on Hardware Metrics 6.7 Extracting TinyML Model Parameters	Fortunatus & Ewura
7: Sep 15	Introduction to Hardware Design Using FPGA: Digital Design	7.1 Computer System Organisation 7.2 From Switches to Logic Gates to Logic Circuits 7.3 Numbers and Arithmetic 7.4 Stateful Components 7.5 Finite State Machines 7.6 Memory 7.8 The RISC-V Processor	Dennis
8: Sep 29	Introduction to Hardware Design Using FPGA: Design Example	8.1 CAD Tools for Hardware Design Implementation 8.2 Vivado Software Installation and License Acquisition 8.3 FPGA Design Flow 8.4 User Design Example: From Specification to Simulation 8.5 User Design Example: FPGA Board Features and Components 8.6 User Design Example: FPGA Board Test	Dennis
9: Oct 13	Deep Learning Model Implementation on FPGAs	9.1 Deep Learning Hardware Primitives 9.2 Optimized Model Inference on Digital Hardware 9.3 Hardware Optimization Techniques 9.4 TinyML Model Hardware Architecture 9.5 TinyML Hardware Architecture Resource Utilization and Power Consumption	Dennis
10: Oct 27	Guest Lecture: Processing at the Edge	Processing at the Edge	Alex (FPGA Engineer @ TechPLEX Inc., Korea)
11: Nov 03	Guest Lecture: AI Acceleration at the Edge	AI Acceleration at the Edge	KETI
12: Nov/Dec	Research Paper Preparation, Writing, and Submission to a Journal/Conference	Paper Title: TinyML Implementation: MCUs vs FPGAs Journal or Conference: TBD	-