Z80 Retro! – FLEADiP Board
FPGA Logic Engine And Display Processor Board

Z80 Retro Interface

File: Z80Interface.kicad_sch

Joystick & IO Ports

File: Joystck_IO_Ports.kicad_sch

Power Supply

File: PowerSupply.kicad_sch

Mouse Config

File: Mouse-config.kicad_sch

Mouse IO

File: Mouse-io.kicad_sch

Mouse Serdes RGB & HDMI

File: Mouse-serdes.kicad_sch

Mouse VGA

File: Mouse-vga.kicad_sch

PAGE 1 : INTRODUCTION

PAGE 2 : Z80 RETRO INTERFACE

PAGE 3 : JOYSTICK & I/O PORTS

PAGE 4 : POWER SUPPLY

PAGE 5 : MOUSE FPGA CONFIGURATION

PAGE 6 : MOUSE FPGA I/O

PAGE 7 : MOUSE FPGA SERDES, RGB, & HDMI

PAGE 8 : VGA BUFFERS & CONNECTOR

MOUNTING HOLES

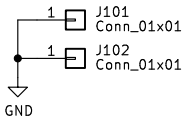
- 4 required for tooling
- 4 required for mechanical
- 1 extra if board connects directly above Z80-Retro main board

H1 MountingHole
H2 MountingHole
H3 MountingHole
H4 MountingHole

PCB STACKUP NOTE

JLC04161H-3313 stackup gives :
* Ideal trace impedance (50 & 100ohms).
* GND plane closer to signal layer routing for improved signal integrity.

PROBE GND PINS



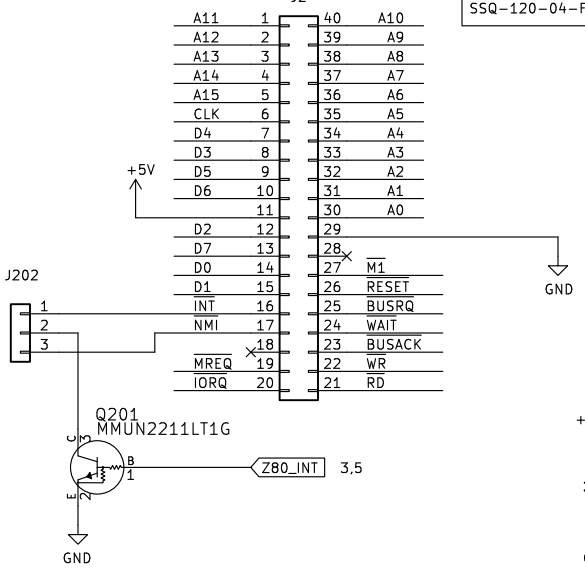
LOGO101 LOGO102

Z80 Retro! – FLEADiP Board *FPGA Logic Engine And Display Processor*		
Title: Z80 Retro! – FLEADiP Board		
Size: USLetter	Date: 2023-06-12	Rev: 0.0
KiCad E.D.A. kicad 7.0.2	Drawn: Denno Wiggle	Id: 1/8

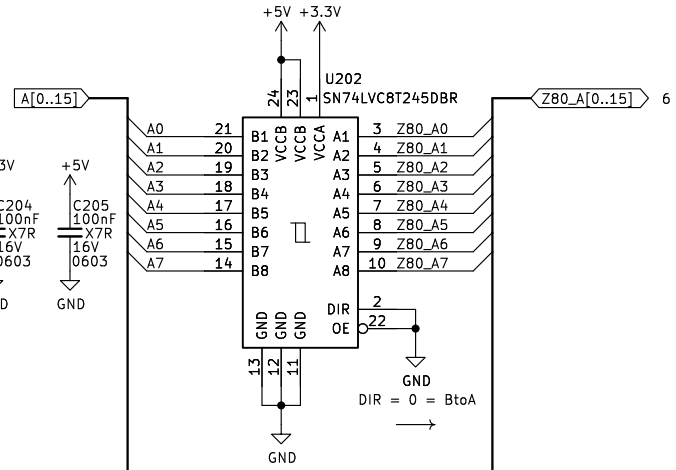
Z80 Retro! Interface

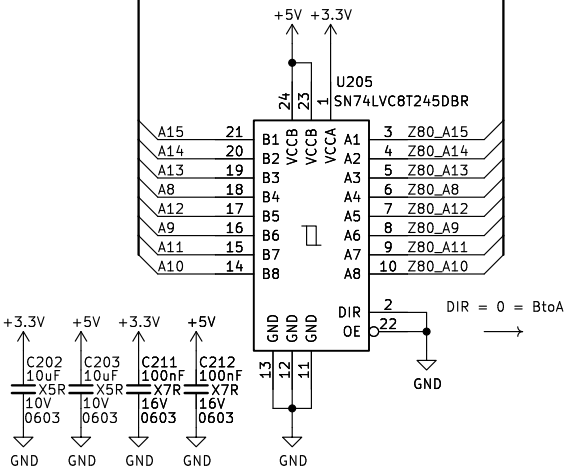
Z80 PIN HEADER

Possible Alternatives to Amazon receptacle?
SSQ-120-04-G-D
SSQ-120-04-F-D

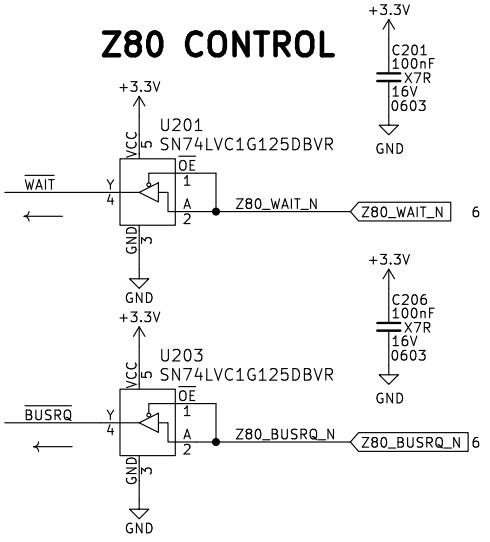


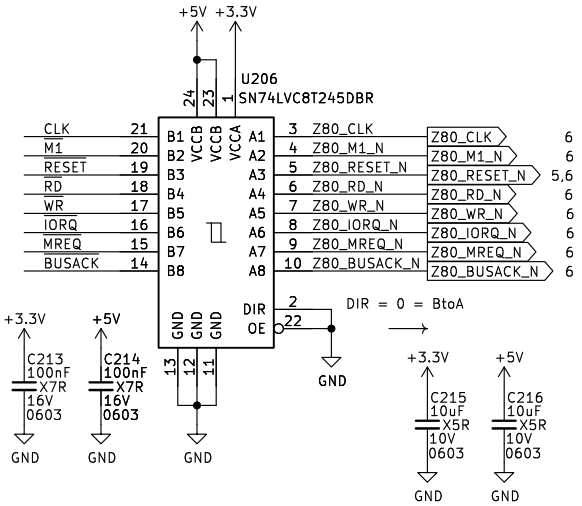
Z80 ADDRESS



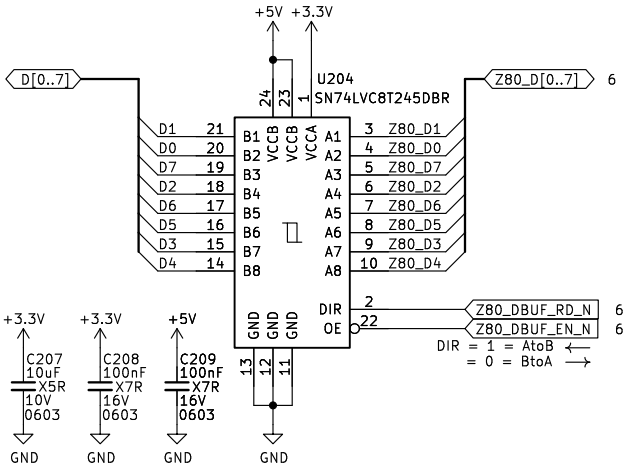


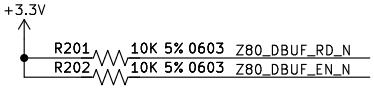
Z80 CONTROL





Z80 DATA





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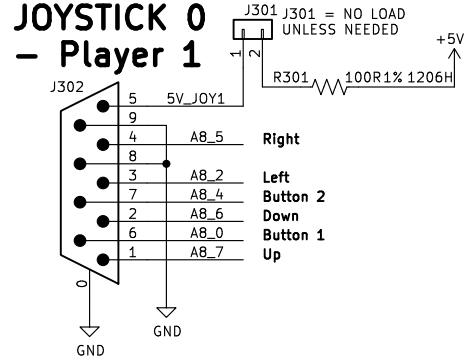
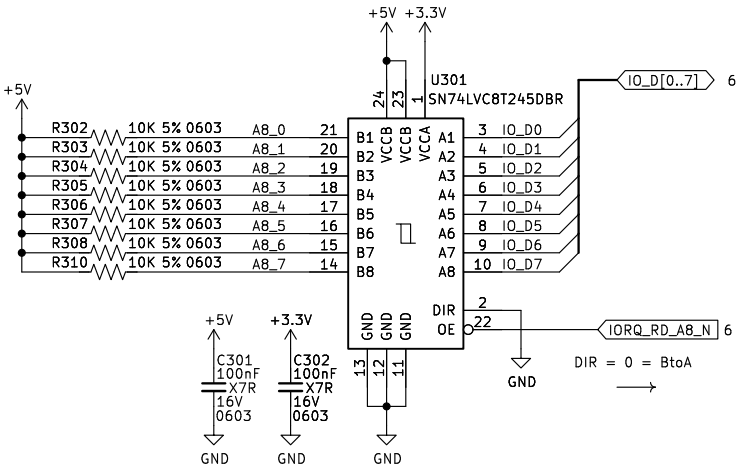
KiCad E.D.A. kicad 7.0.2	Drawn: Denno Wiggle	Id: 2/8

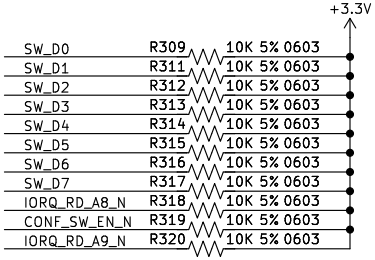
JOYSTICK & I/O PORTS

JOYSTICK 0 – Player 1



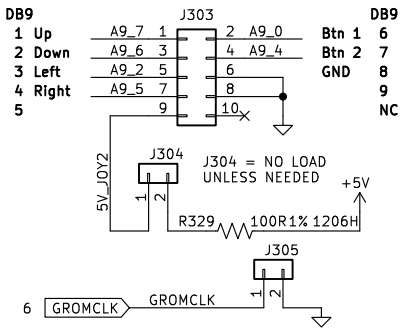
JOYSTICK0 and JOYSTICK1 btn2 and 5V are wired per MSX two button joypad.
Not for 2 button Atari compatibale joystick!



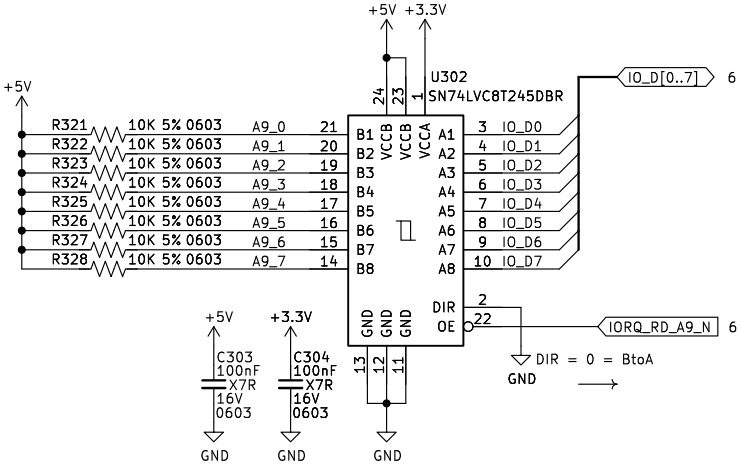


JOYSTICK 1 – Player 2

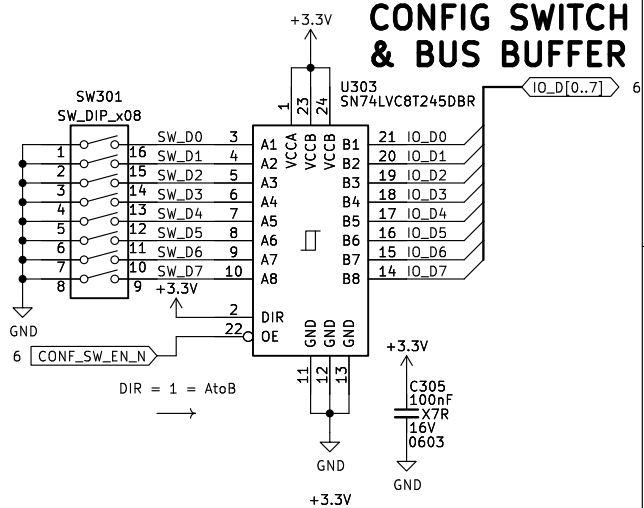
Use header to Female DB9 Cable + gender changer.
Alterate : 2x5 to Male DB9 cable with pin swap.



GROMCLK is used to check the FPGA PLL function.
Frequency should be 447,411.9Hz

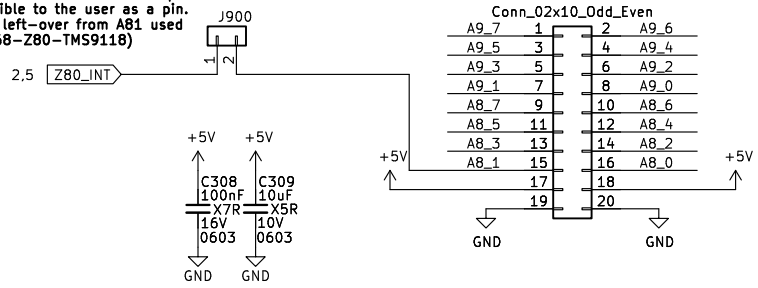


CONFIG SWITCH & BUS BUFFER

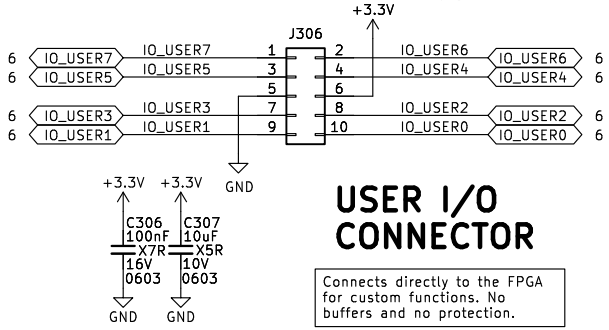


INPUT CONNECTOR

J900 has no use on FLEADiP other than to make the Z80 interrupt accessible to the user as a pin. (It's a left-over from A81 used on 2068-Z80-TMS9118)



USER I/O CONNECTOR



Connects directly to the FPGA for custom functions. No buffers and no protection.

Joystick and IO Ports		
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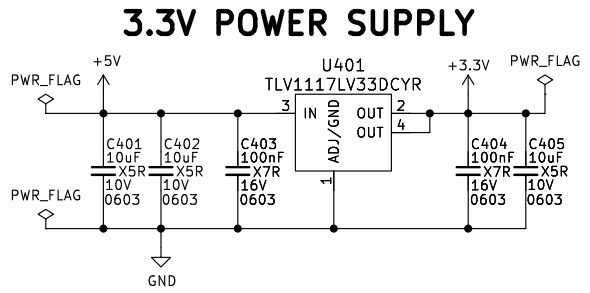
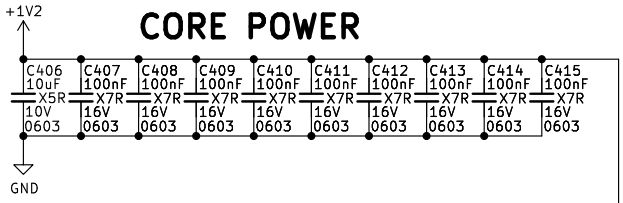
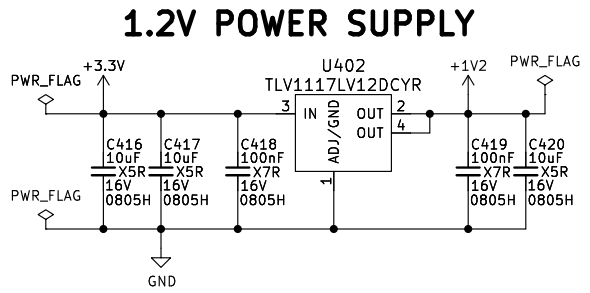
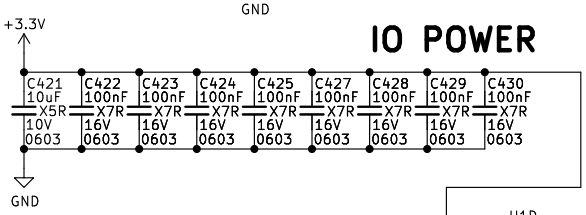
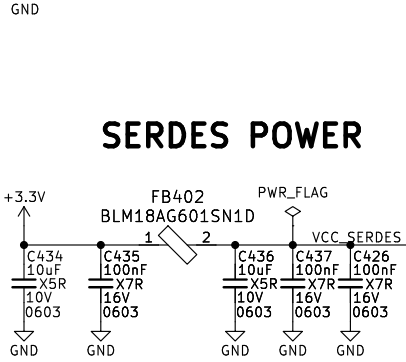
POWER SUPPLY

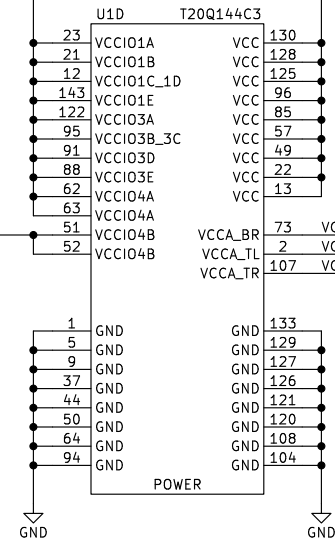


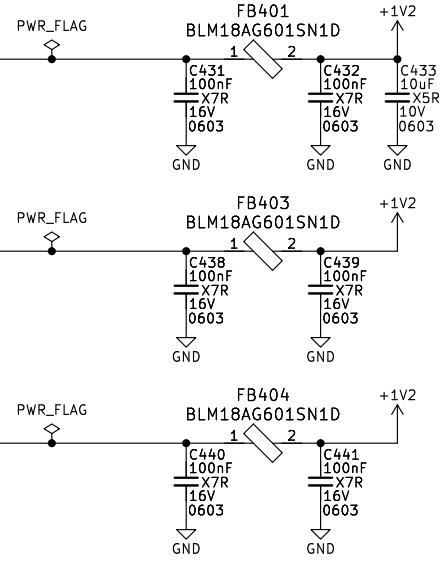








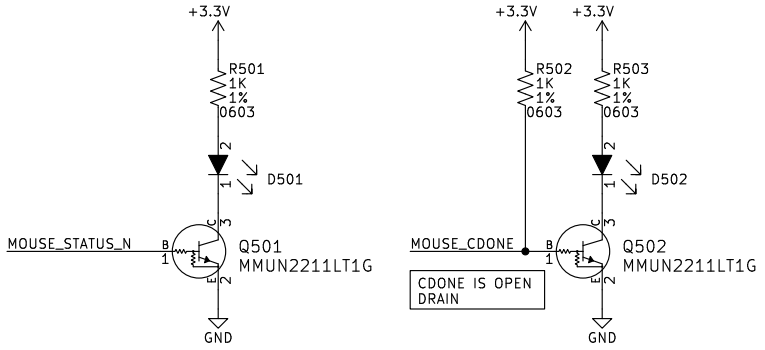




PLL POWER FILTERS

Power Supply 3.3V & 1.2V		
Title: Z80 Retro! – FLEADiP Board		
Size: USLetter	Date: 2023-06-12	Rev: 0.0
KiCad E.D.A. kicad 7.0.2	Drawn: Denno Wiggle	Id: 4/8

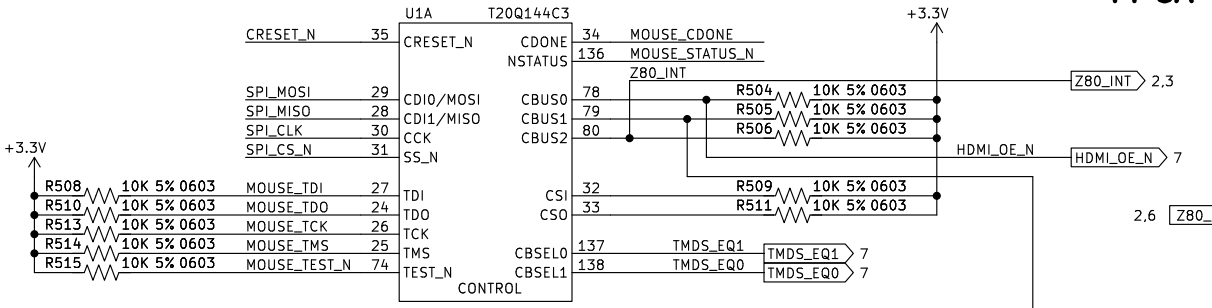
MOUSE FPGA CONFIGURATION

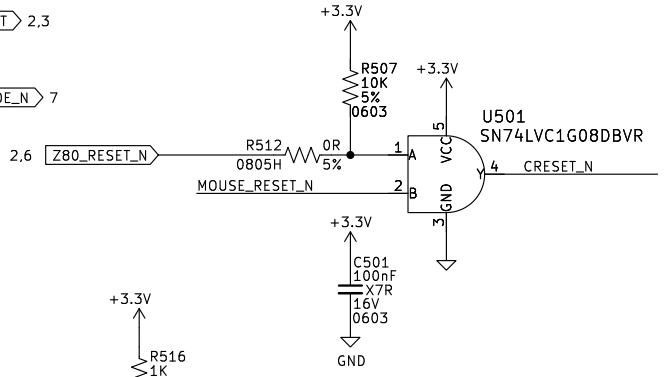


FPGA NSTATUS LED

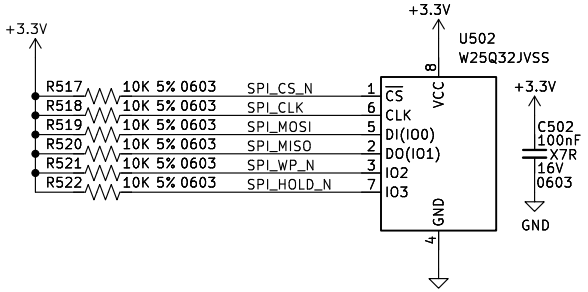
FPGA CDONE LED

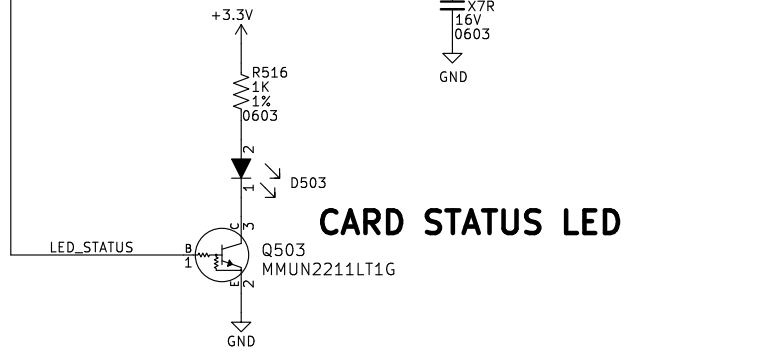
FPGA CONFIGURATION





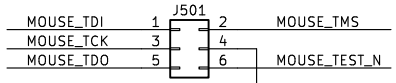
SPI FLASH





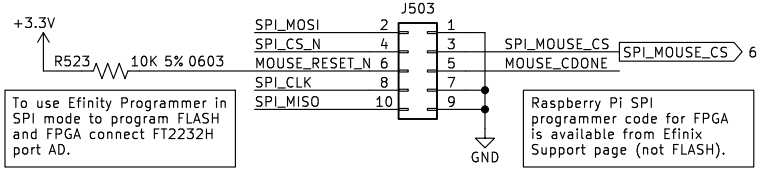
CARD STATUS LED

JTAG INTERFACE



To use Efinity Programmer and Debug tools in JTAG Mode Connect FT2232H port BD

SPI INTERFACE TO ESP PROGRAMMER BOARD



To use Efinity Programmer in SPI mode to program FLASH and FPGA connect FT2232H port AD.

Raspberry Pi SPI programmer code for FPGA is available from Efinix Support page (not FLASH).

Mouse FPGA Configuration		
Title: Z80 Retro! – FLEADiP Board		
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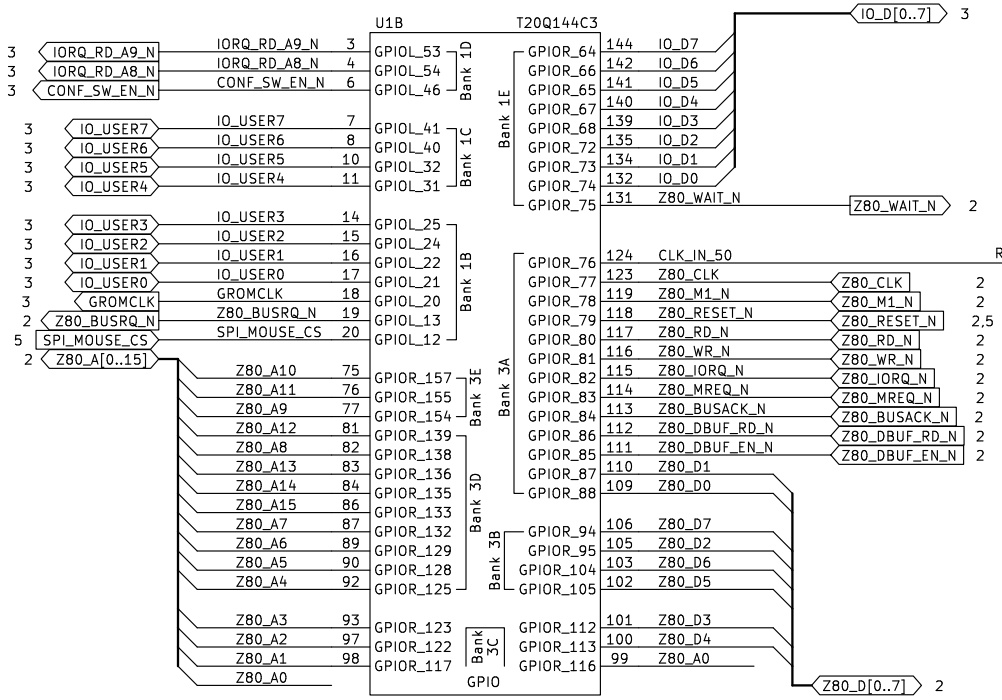
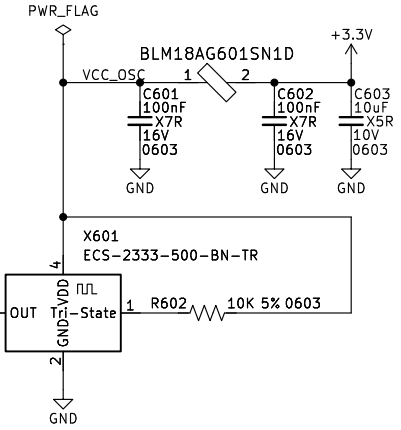
KiCad E.D.A. kicad 7.0.2	Drawn: Denno Wiggle	Id: 5/8

MOUSE FPGA I/O

GPIO PINS



50MHz OSCILLATOR



Mouse FPGA I/O Ports		
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KiCad E.D.A. kicad 7.0.2	Drawn: Denno Wiggle	Id: 6/8

MOUSE FPGA SERDES, RGB, & HDMI

LVDS TO TMDS

U701 PTN3366BSMP

+3.3V

NC 3
NC 23
NC 24
VDD 1
VDD 18

C701 100nF X7R 16V 0603
C702 10uF X5R 10V 0603
C703 100nF X7R 16V 0603
C704 10uF X5R 10V 0603

GND

5 TMDS_EQ0 → TMDS_EQ0 8 EQ0
5 TMDS_EQ1 → TMDS_EQ1 2 EQ1

R701 10K 5% 0603
R702 10K 5% 0603

HDMI_SCL_SOURCE 7 SCL_SOURCE
HDMI_SDA_SOURCE 6 SDA_SOURCE

SCL_SINK 19 SCL_SINK
SDA_SINK 20 SDA_SINK

HPD_SOURCE 5 HPD_SOURCE
HPD_SINK 21 HPD_SINK

5 HDMI_OE_N → HDMI_OE_N 17 OE_N
HDMI_DDC_EN 22 DDC_EN

R703 10K 5% 0603

EQ1	EQ0	SETTING
GND	GND	0 dB
GND	VDD	2 dB
VDD	GND	4 dB
VDD	VDD	6 dB

RGB & LVDS OUTPUTS

U1C T20Q144C3 SERDES

8 RGB_HSYNC	RGB_HSYNC	55	GPIOB_RXP00	GPIOB_TXP00	38	LVDS_S_TX2P	C705	LVDS_TX2P	32 IN_D4P
8 RGB_VSYNC	RGB_VSYNC	56	GPIOB_RXN00	GPIOB_TXN00	39	LVDS_S_TX2N	C706	LVDS_TX2N	31 IN_D4N
8 RGB_BLU[0..3]	RGB_BLU3	58	GPIOB_RXP02	GPIOB_TXP02	40	LVDS_S_TX1P	C707	LVDS_TX1P	30 IN_D3P
	RGB_BLU2	59	GPIOB_RXN02	GPIOB_TXN02	41	LVDS_S_TX1N	C708	LVDS_TX1N	29 IN_D3N
	RGB_BLU0	61	GPIOB_RXP03	GPIOB_TXP04	42	LVDS_S_TX0P	C709	LVDS_TX0P	28 IN_D2P
	RGB_BLU1	60	GPIOB_RXN03	GPIOB_TXN04	43	LVDS_S_TX0N	C710	LVDS_TX0N	27 IN_D2N
8 RGB_GRN[0..3]	RGB_GRN2	66	GPIOB_RXP07	GPIOB_TXP06	45	LVDS_S_CLKP	C711	LVDS_CLKP	26 IN_D1P
	RGB_GRN3	65	GPIOB_RXN07	GPIOB_TXN06	46	LVDS_S_CLKN	C712	LVDS_CLKN	25 IN_D1N
	RGB_GRN1	67	GPIOB_RXP10	GPIOB_TXP09	47				
	RGB_GRN0	68	GPIOB_RXN10	GPIOB_TXN09	48				
8 RGB_RED[0..3]	RGB_RED2	70	GPIOB_RXP12	GPIOB_TXP11	53	HPD_SOURCE			
	RGB_RED3	69	GPIOB_RXN12	GPIOB_TXN11	54	RGB_BLANK	R705 33R 1% 0603		
	RGB_RED1	71	GPIOB_CLKP						
	RGB_RED0	72	GPIOB_CLKN	REF_RES	36				

Bank 4A
Bank 4B

R706 12K4 1% 0603

OUT_D4P	9	TMDS_TX2P		
OUT_D4N	10	TMDS_TX2N		
OUT_D3P	11	TMDS_TX1P		
OUT_D3N	12	TMDS_TX1N		
OUT_D2P	13	TMDS_TX0P		
OUT_D2N	14	TMDS_TX0N		
OUT_D1P	15	TMDS_CLKP		
OUT_D1N	16	TMDS_CLKN		
REXT	4	R704 12K4 1% 0603		
GND	33			

LINE PROTECTION

U702 RCLAMP0524P
U703 RCLAMP0524P

TMDS_TX2P	5 IN4	OUT4 6	TMDS_TX2P		1 D2+
TMDS_TX2N	4 IN3	OUT3 7	TMDS_TX2N		3 D2−
GND	3 GND1	GND2 8	GND		4 D1+
TMDS_TX1P	2 IN2	OUT2 9	TMDS_TX1P		6 D1−
TMDS_TX1N	1 IN1	OUT1 10	TMDS_TX1N		7 D0+
TMDS_TX0P	5 IN4	OUT4 6	TMDS_TX0P		9 D0−
TMDS_TX0N	4 IN3	OUT3 7	TMDS_TX0N		10 CK+
GND	3 GND1	GND2 8	GND		12 CK−
TMDS_CLKP	2 IN2	OUT2 9	TMDS_CLKP	CEC	13 CEC
TMDS_CLKN	1 IN1	OUT1 10	TMDS_CLKN	SCL_SINK	15 SCL
				SDA_SINK	16 SDA
				HPD_SINK	14 UTILITY/HEAC+
					19 HPD/HEAC−

HDMI

J701 HDMI_A_1.4

+5V 18
D2S 2
D1S 5
D0S 8
CKS 11
GND 17
SH

PWR_FLAG
+5VD
+5V
R707 0805H DNL 5%
C713 100nF X7R 16V 0603
Z701 TVS_SMAJ5.0A
GND

SCL_SINK R708 10K 5% 0603
SDA_SINK R709 10K 5% 0603
CEC R710 2K7 5% 0805H
+5VD

On the hdmi connector void the plane underneat the TXP and TXN pins to reduce capacitance.
Ref : Layout Guideline for PTN3366

Mouse FPGA serdes, RGB, & HDMI		
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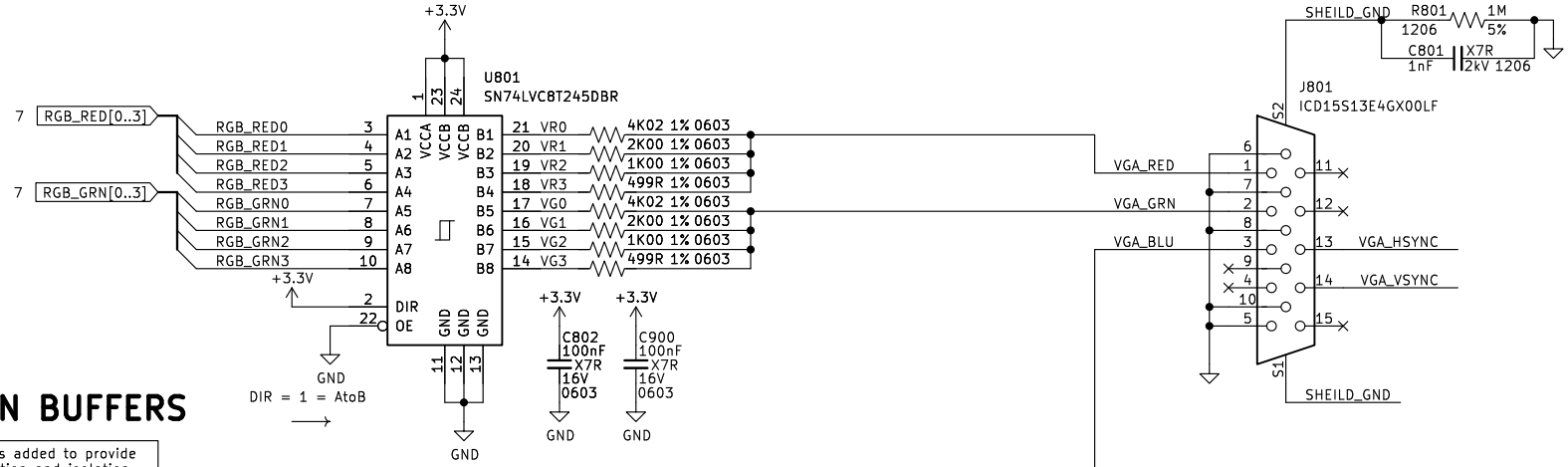
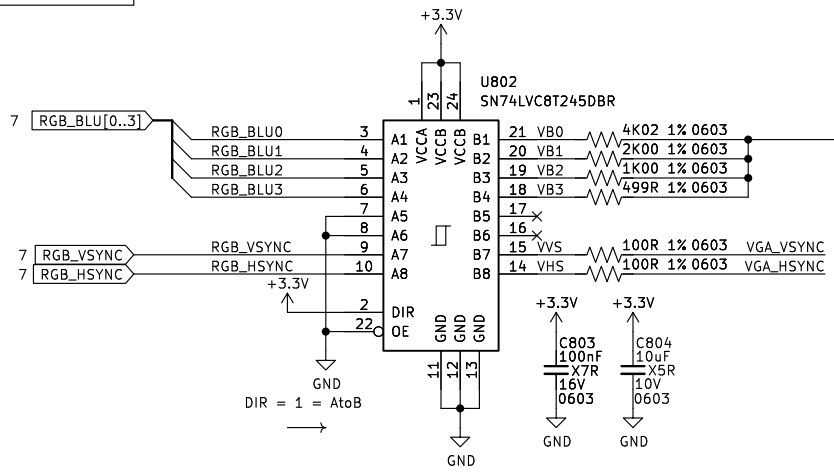
VGA BUFFERS AND CONNECTOR

VGA CONNECTOR



ISOLATION BUFFERS

Buffers added to provide protection and isolation for the Mouse FPGA



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KiCad E.D.A. kicad 7.0.2	Drawn: Denno Wiggle	Id: 8/8