

SEWER

Simple Eval With EZ80F91 on RCBUS

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PAGE 3 : CPU POWER & ZDI

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PAGE 5 : CPU ETHERNET

PAGE 6 : CPU GPIO & RTC

RcBusInterface



File: RcBusInterface.kicad_sch
CpuPowerZdi



File: ez80_PowerZdi.kicad_sch
CpuAddressData



File: ez80_AddressDataBus.kicad_sch
CpuEthernet



File: ez80_EthernetInterface.kicad_sch
CpuGpioRtc



File: ez80_Gpio.kicad_sch

LOG01



LOG02



PCB STACKUP NOTE

JLC04161H-3313 stackup gives :
* Ideal trace impedance (50 & 100ohms).
* GND plane closer to signal layer routing
for improved signal integrity.

MOUNTING/TOOLING HOLES



H1
MountingHole



H2
MountingHole



H3
MountingHole



H4
MountingHole



H5
MountingHole

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Simple Eval With EZ80F91 on RCBUS

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Size: USLetter

Date: 2024-08-16

Rev: 0

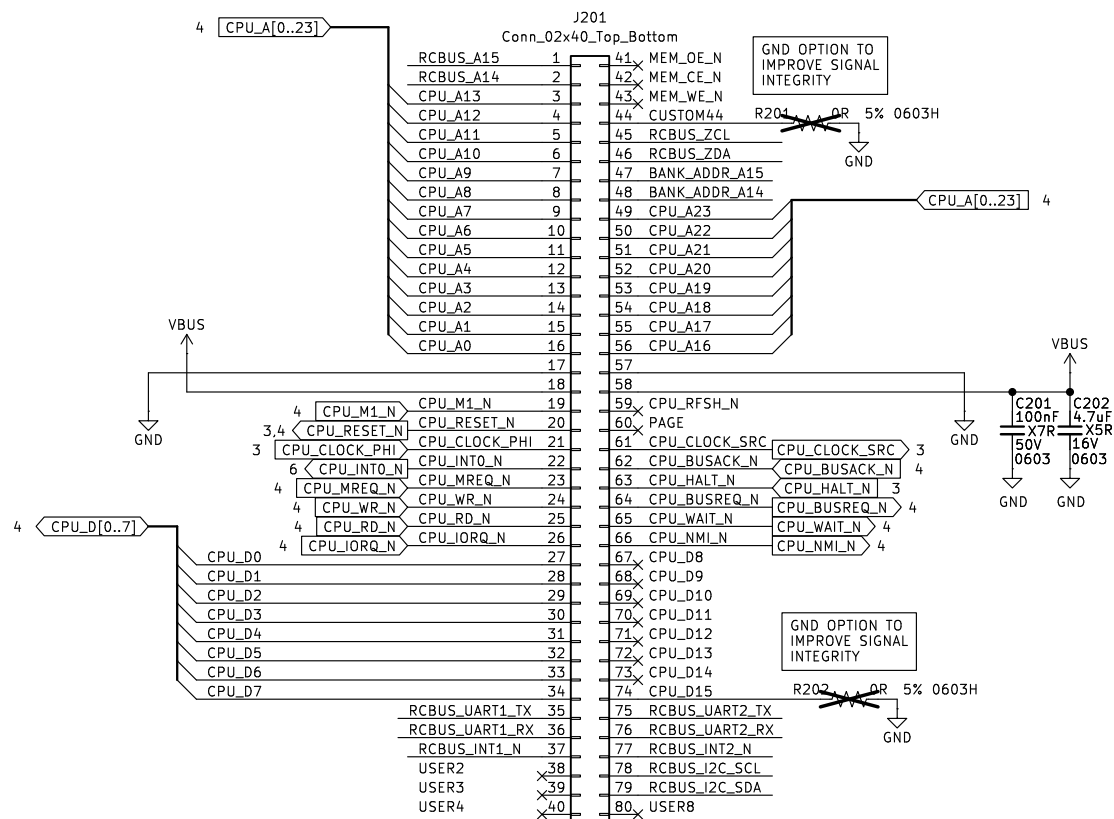
KiCad E.D.A. 8.0.4

Drawn: Denno Wiggle

Id: 1/6

RCBUS Interface

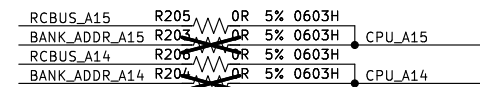
RCBUS CONNECTOR



RCBUS STUFFING OPTION FOR MEMORY BANKING

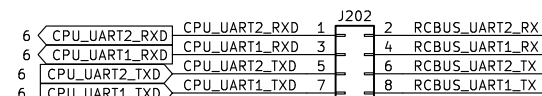
To use memory banking with a 16K granularity on PETER populate R203 & R204, remove R205 & R206, and cut RCBUS pins A16 through to A20.

To use memory banking with a 32K granularity on PETER populate R203, remove R205, and cut RCBUS pins A16 through to A20.

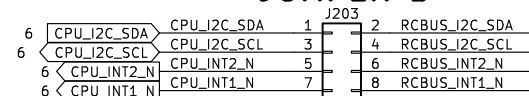


RCBUS JUMPERS

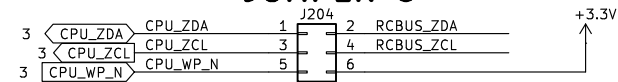
JUMPER A



JUMPER B



JUMPER C



Install Jumper between J204.5 and J204.6 to write to the internal CPU FLASH memory.

RCBUS Interface

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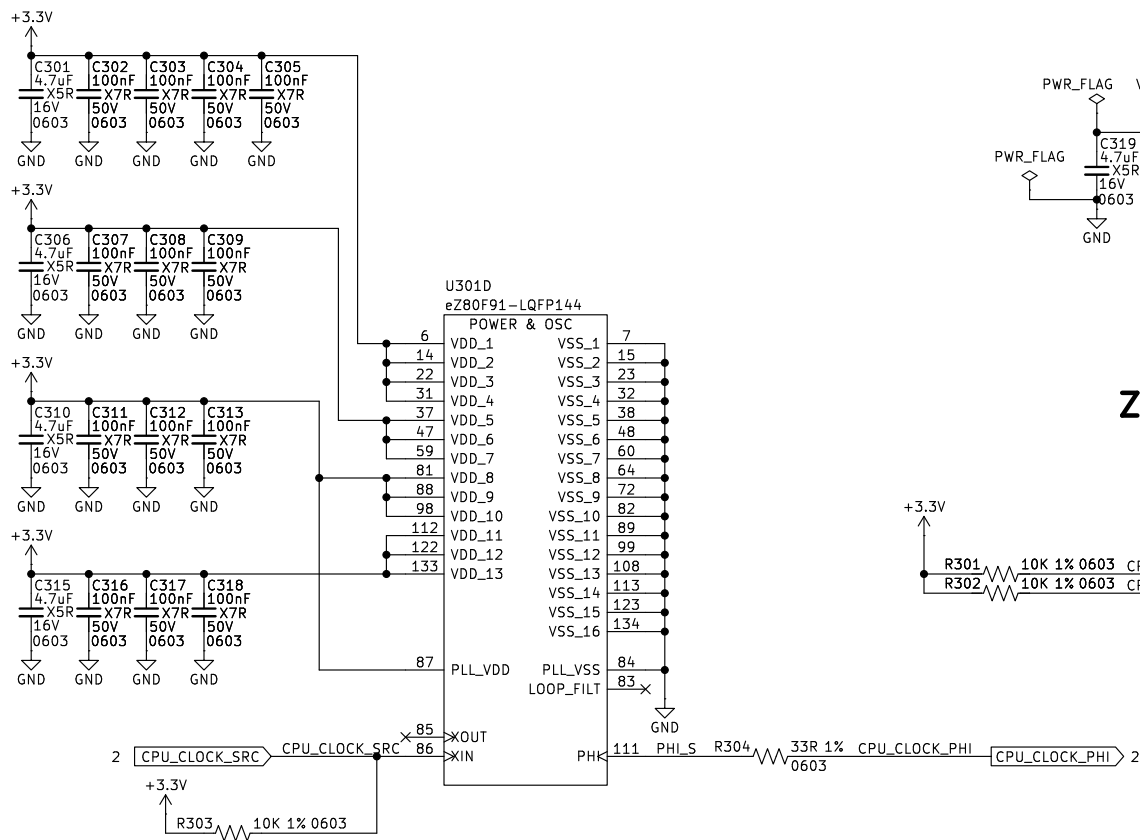
Rev: 0

KiCad E.D.A. 8.0.4

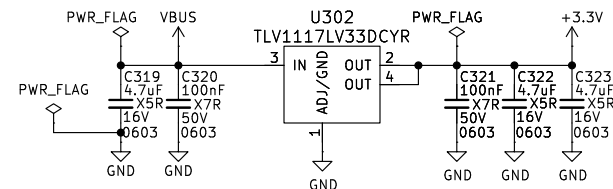
Drawn: Denno Wiggle

Id: 2/6

CPU Power & ZDI

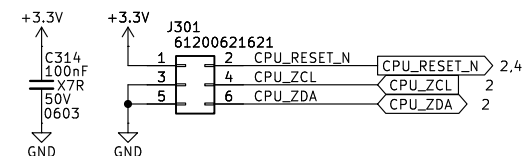
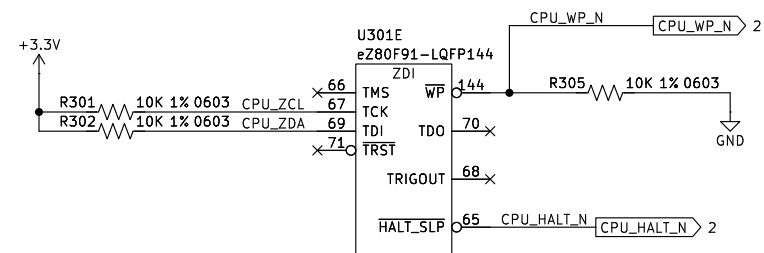


POWER SUPPLY



269-EZ80F91AZA50EK-ND

ZDI DEBUG INTERFACE



CPU Power & ZDI

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CPU Address & Data Bus



Figure 10 illustrates a multi-ported bus configuration. The top section shows a 33R 1% 0603 bus connected to four multi-ported devices: CPU_M1_N, CPU_WR_N, CPU_RD_N, and CPU_BUSACK_N. Each device has two ports, and the bus is connected to all four. Below this, a similar setup is shown for CPU_MREQ_N and CPU_IORQ_N, but with a note indicating that the bus is not connected to the MREQ_N and IORQ_N ports of the CPU_M1_N and CPU_WR_N devices.

Stuffing option for the CPU_M/IREQ_N signal to use CS timing or M/IREQ timing.
* Co-locate resistors.

CPU Address and Data Bus		
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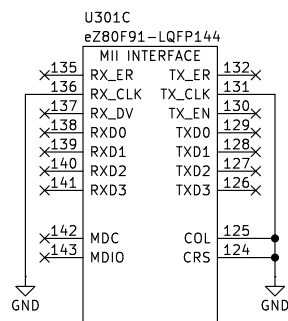
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CPU Ethernet Interface



Sheet is a placeholder for future
10/100 Ethernet implementation.

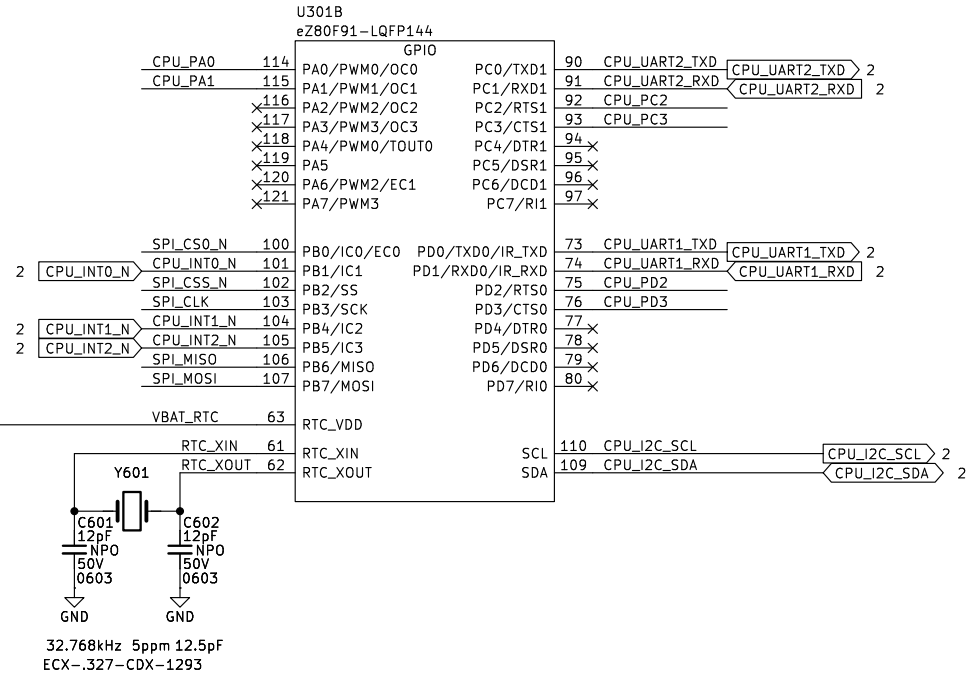
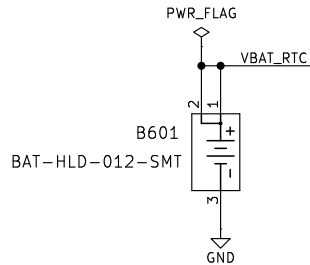
CPU Ethernet Interface

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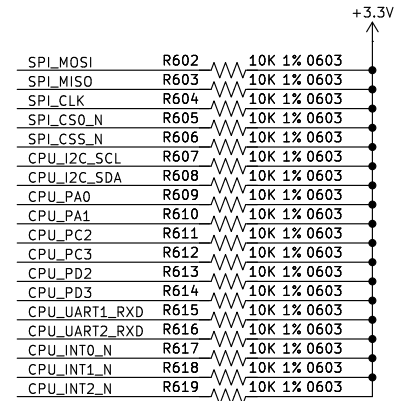
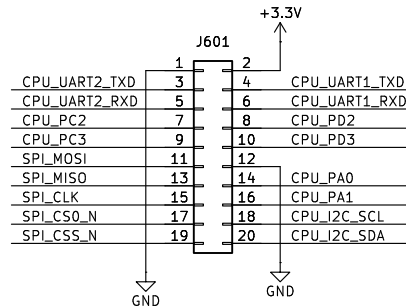
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CPU GPIO RTC

CR1225 BATTERY



TTL LEVEL CPU SIGNAL HEADER



CPU GPIO & Real Time Clock

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