PETER
Peripheral ECP5 Technology and Entertainment Resource

Power Supply

File: PowerSupply.kicad_sch

RCBUS Connectors

File: RCBUS_Connectors.kicad_sch

SRAM MEMORY

File: CpuBusSram.kicad_sch

FPGA IO

File: FPGA-io.kicad_sch

FPGA Config

File: FPGA-config.kicad_sch

RGB VGA

File: VideoRGB-port.kicad_sch

PS2 & Audio

File: PS2-Audio.kicad_sch

SNES Connectors

File: SnesConnectors.kicad_sch

UART_FT230X

File: UartPorts.kicad_sch

USER IO, SPI, I2C

File: UserIoSpiI2c.kicad_sch

ESP32-S3

File: Esp32s3-Programmer.kicad_sch

PCB STACKUP NOTE

JLC04161H-3313 stackup gives :
* Ideal trace impedance (50 & 100ohms).
* GND plane closer to signal layer routing for improved signal integrity.

MOUNTING HOLES

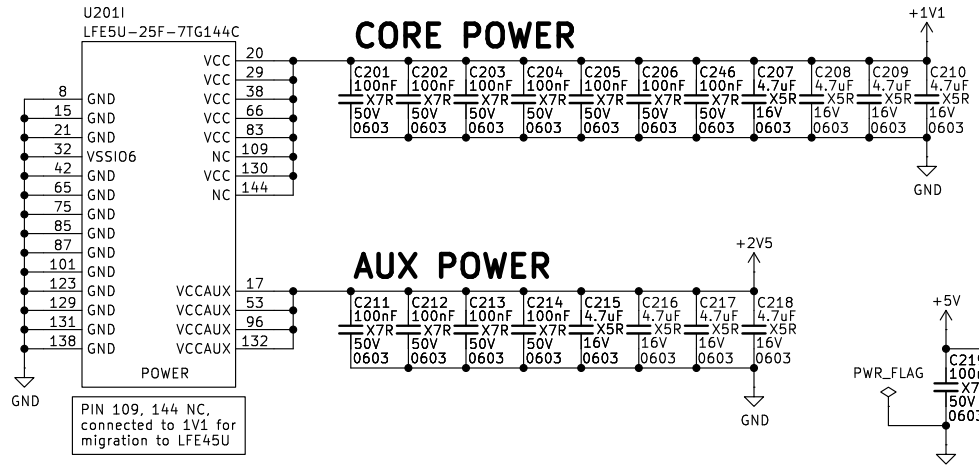
- 4 required for tooling
- 4 required for mechanical

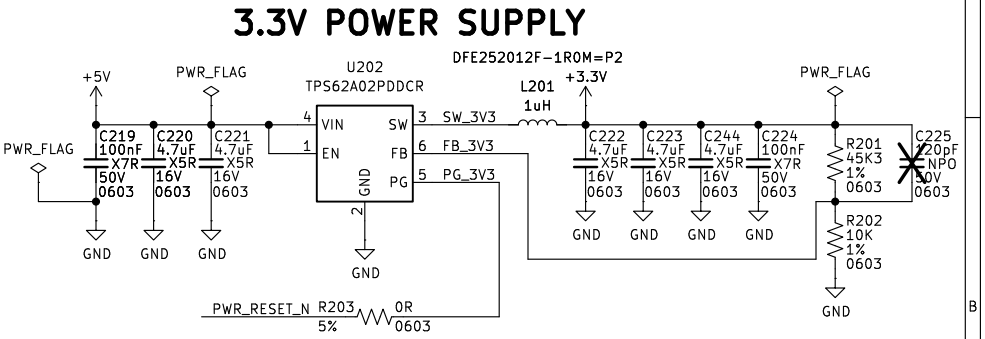
H1 MountingHole H2 MountingHole H3 MountingHole H4 MountingHole

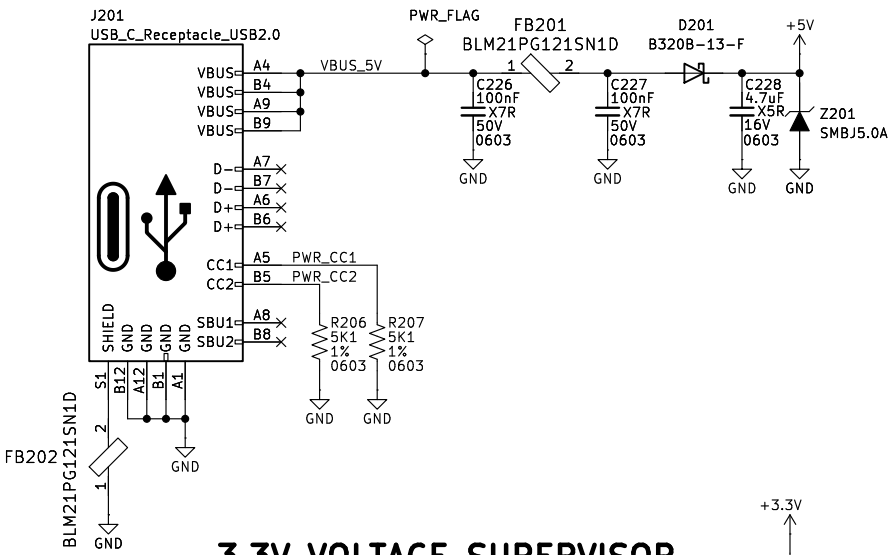
LOGO101 LOGO102

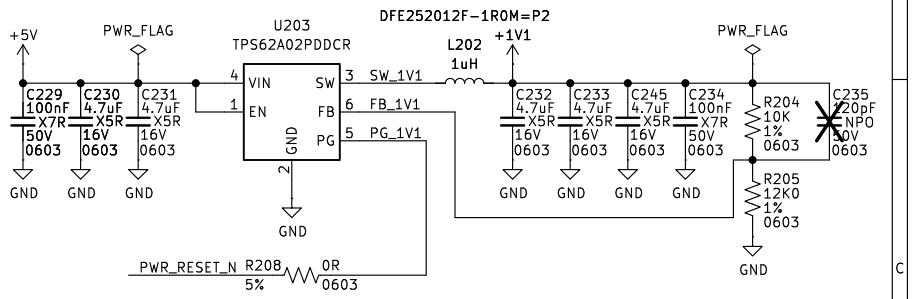
Peripheral ECP5 Technology and Entertainment Resource. Connects to CPU card/RCBUS card.		
Title: PETER		
Size: A	Date: 2024-07-29	Rev: 0.0
KiCad E.D.A. 8.0.4	Drawn: Denno Wiggle	Id: 1/12

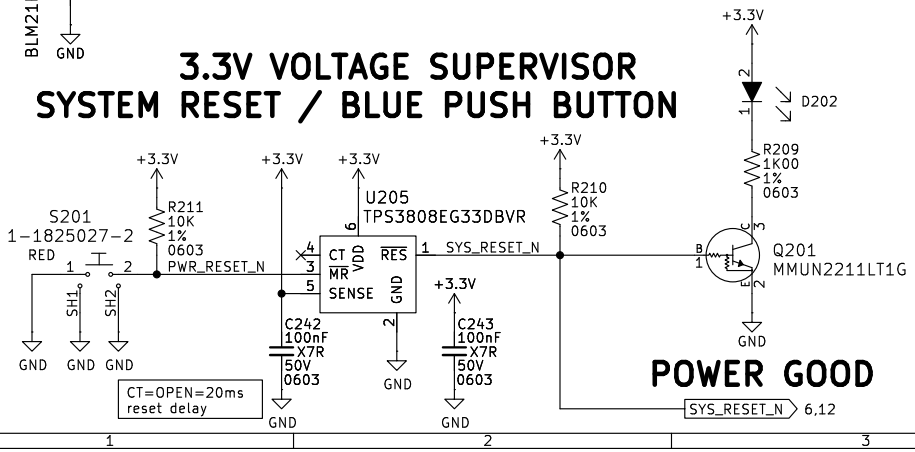
POWER SUPPLY

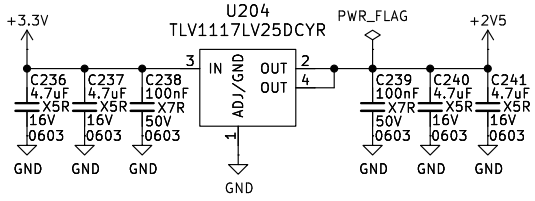










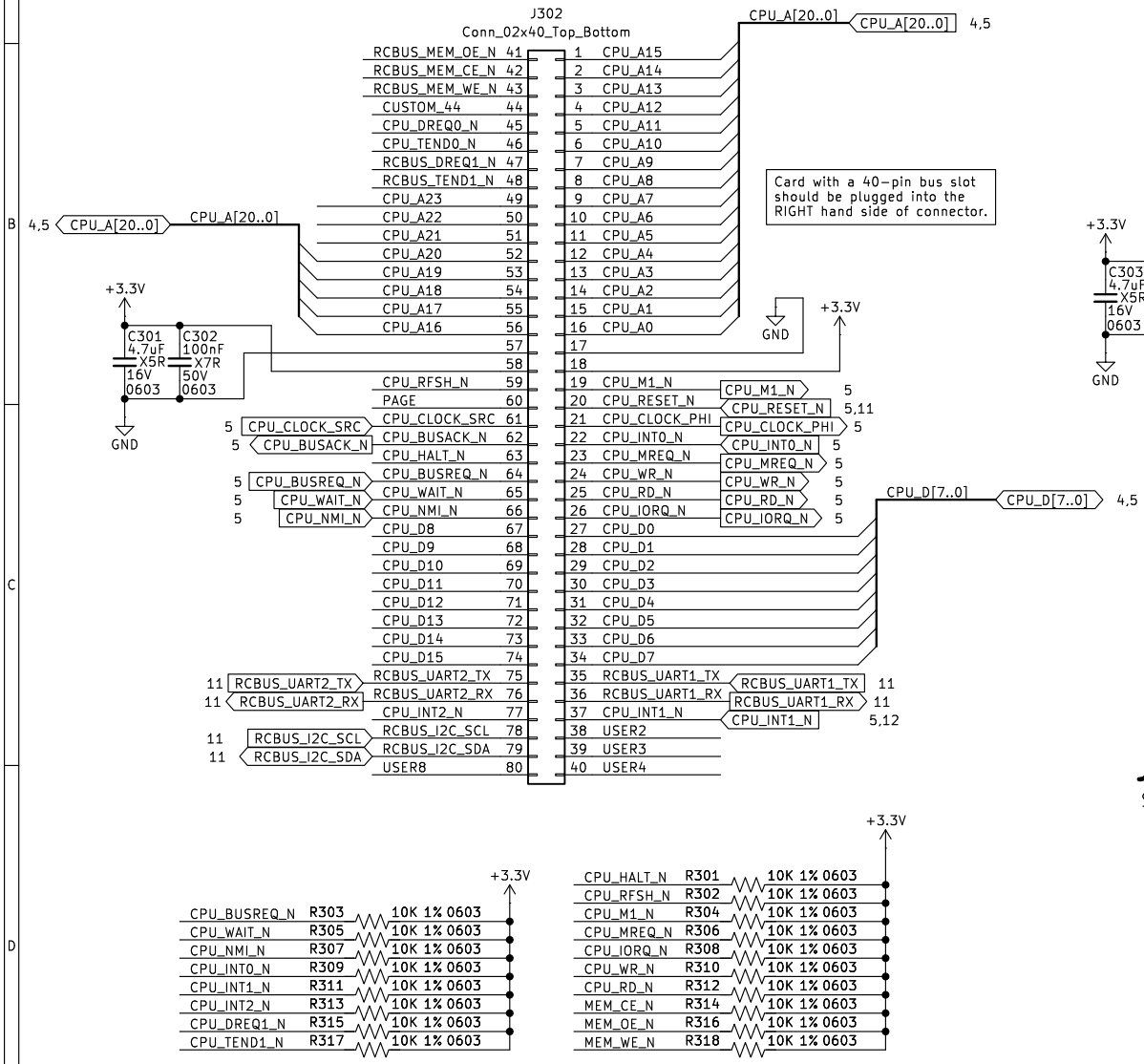


USB Power Supply 3.3V 2.5V & 1.1V.		
Title: PETER		
Size: A	Date: 2024-07-29	Rev: 0.0
KiCad E.D.A. 8.0.4	Drawn: Denno Wiggle	Id: 2/12

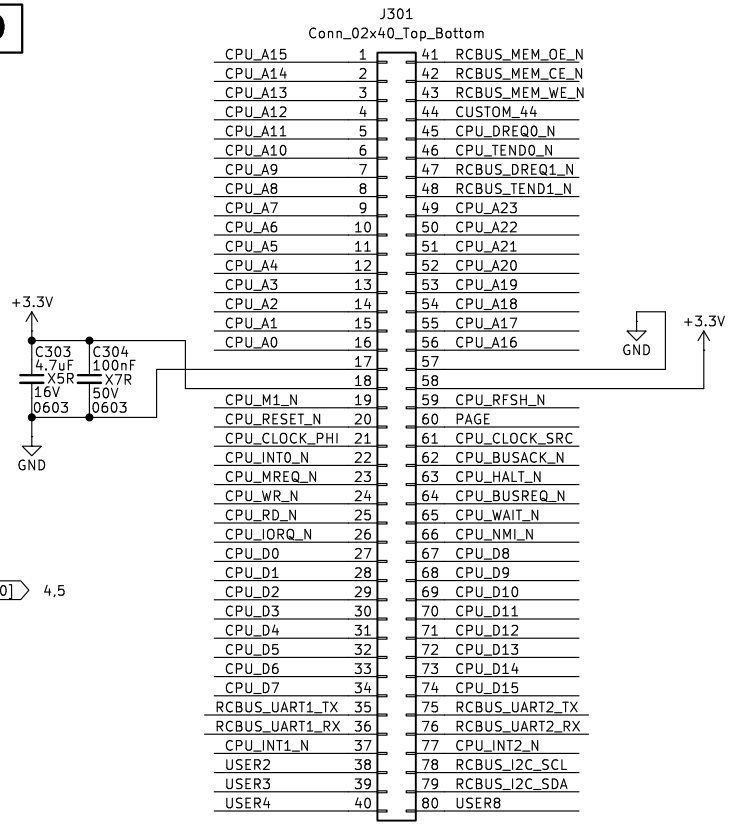
RCBUS CONNECTORS

RCBUS CARD SOCKET CONNECTOR – 3.3V ONLY
NOT 5V TOLERANT!

80–PIN BOTH SIDES **40–PIN RIGHT SIDE ON BOARD**

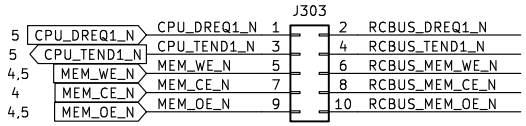


RCBUS EXPANSION PLUG CONNECTOR
NOT 5V TOLERANT!



JUMPER A RCBUS SELECTION (1 OF 2)

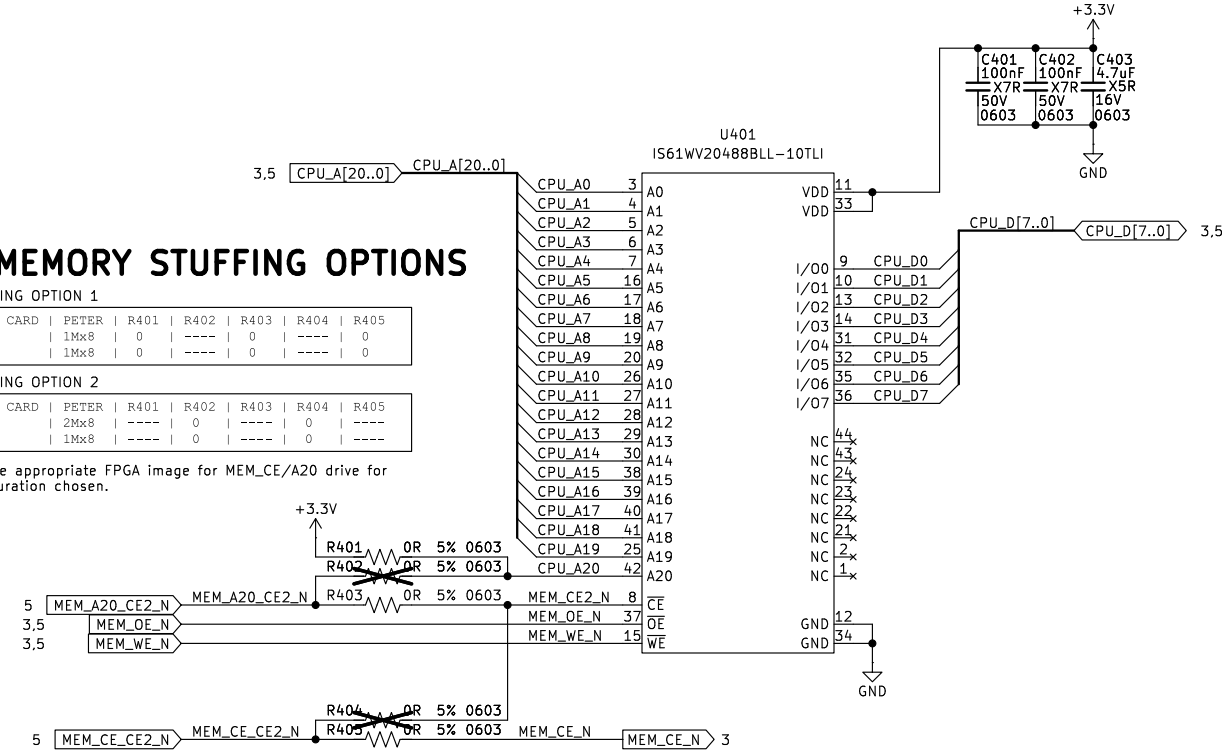
SEE P.11 FOR JUMPER B



CPU Bus Connections.		
Title: PETER		
Size: A	Date: 2024–07–29	Rev: 0.0
KiCad E.D.A. 8.0.4	Drawn: Denno Wiggle	Id: 3/12

CPU BUS SRAM MEMORY

SRAM MEMORY 2MB x 8
1MB x 8



SRAM MEMORY STUFFING OPTIONS

STUFFING OPTION 1

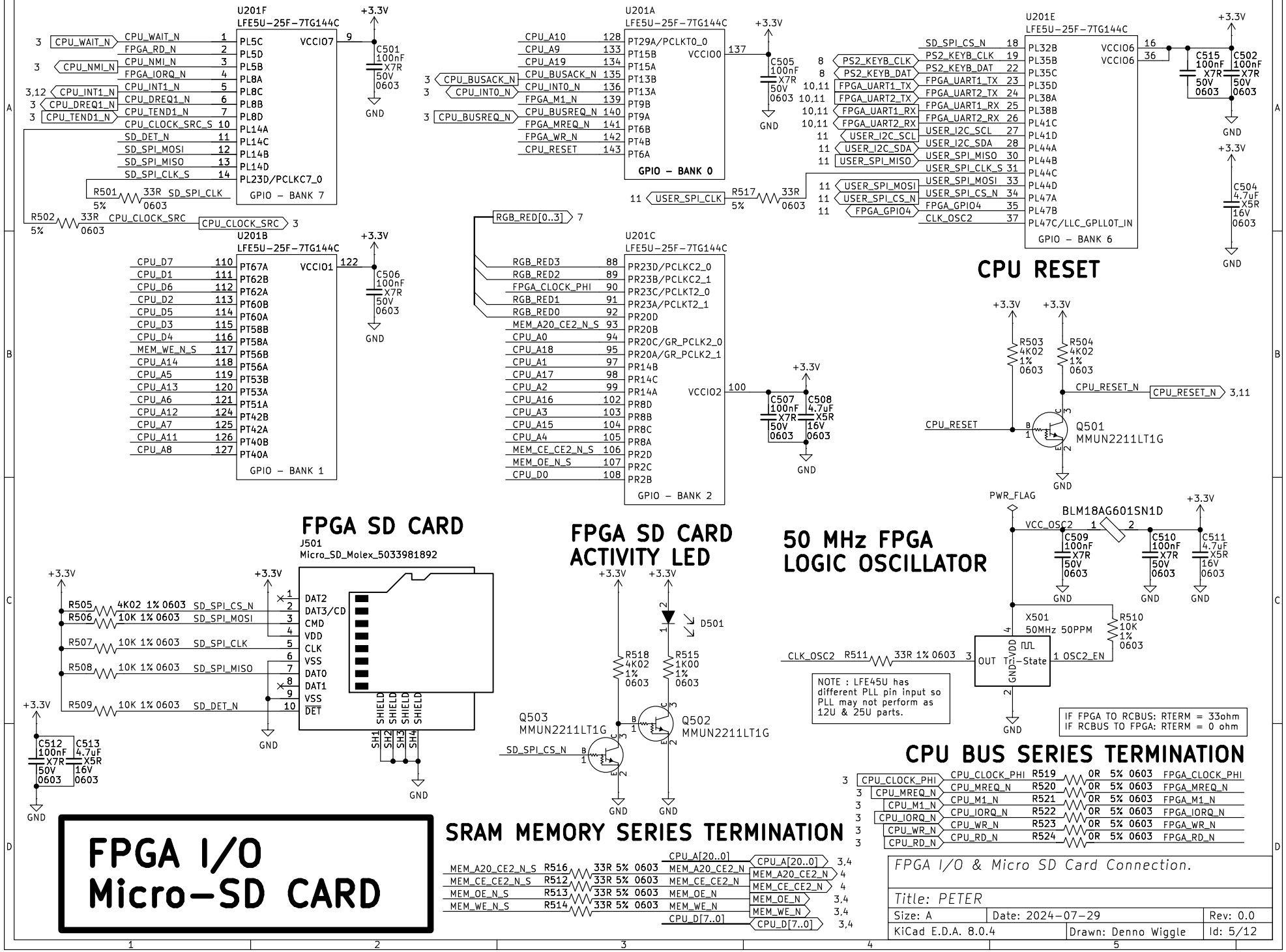
RCBUS CARD	PETER	R401	R402	R403	R404	R405
1Mx8	1Mx8	0	----	0	----	0
----	1Mx8	0	----	0	----	0

STUFFING OPTION 2

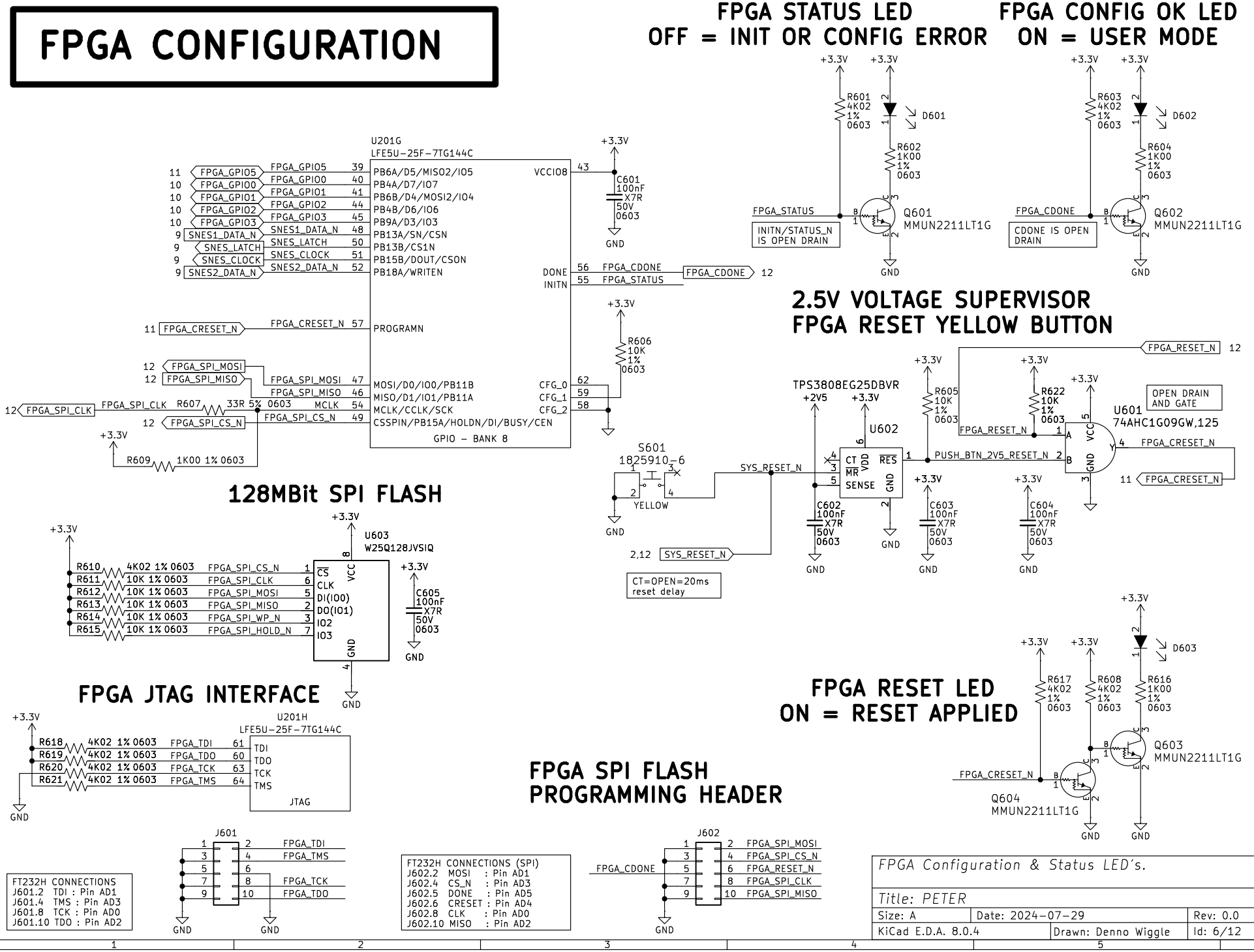
RCBUS CARD	PETER	R401	R402	R403	R404	R405
----	2Mx8	----	0	----	0	----
----	1Mx8	----	0	----	0	----

Use the appropriate FPGA image for MEM_CE/A20 drive for configuration chosen.

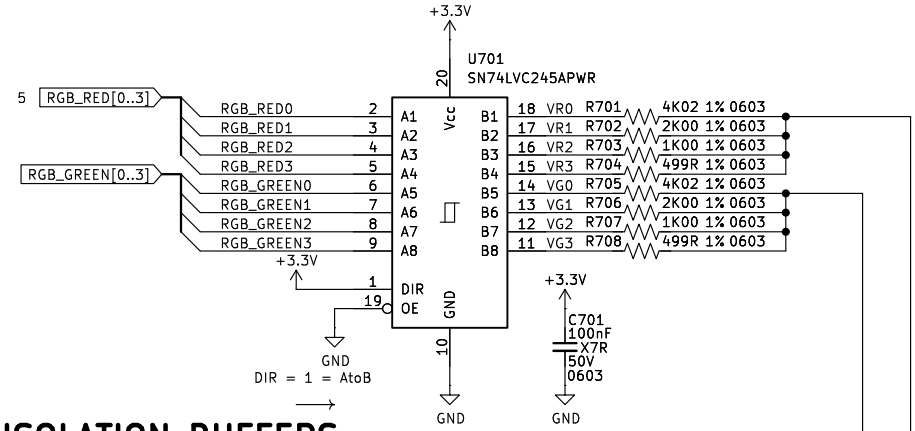
CPU Bus SRAM Memory.			
Title: PETER			
Size: A	Date: 2024-07-29		Rev: 0.0
KiCad E.D.A. 8.0.4		Drawn: Denno Wiggle	Id: 4/12


U201F
LFE5U-25F-7TG144C
PL5C VCCIO7
PL5D
PL5B
PL8A
PL8C
PL8B
PL8D
PL14A
PL14C
PL14B
PL14D
PL23D/PCLKC7_0
GPIO – BANK 7
CPU_WAIT_N
FPGA_RD_N
CPU_NMI_N
FPGA_IORQ_N
CPU_INT1_N
CPU_DREQ1_N
CPU_TEND1_N
CPU_CLOCK_SRC_S
SD_DET_N
SD_SPI_MOSI
SD_SPI_MISO
SD_SPI_CLK_S
R501 33R SD_SPI_CLK 5% 0603
R502 33R CPU_CLOCK_SRC 5% 0603
CPU_CLOCK_SRC
+3.3V
C501 100nF X7R 50V 0603
GND
U201A
LFE5U-25F-7TG144C
PT29A/PCLKT0_0
PT15B VCCIO0
PT15A
PT13B
PT13A
PT9B
PT9A
PT6B
PT4B
PT6A
GPIO – BANK 0
CPU_A10
CPU_A9
CPU_A19
CPU_BUSACK_N
CPU_INT0_N
FPGA_M1_N
CPU_BUSREQ_N
FPGA_MREQ_N
FPGA_WR_N
CPU_RESET
C505 100nF X7R 50V 0603
U201E
LFE5U-25F-7TG144C
PL32B VCCIO6
PL35B
PL35C
PL35D
PL38A
PL38B
PL41C
PL41D
PL44A
PL44B
PL44C
PL44D
PL47A
PL47B
PL47C/LLC_GPLL0T_IN
GPIO – BANK 6
SD_SPI_CS_N
PS2_KEYB_CLK
PS2_KEYB_DAT
FPGA_UART1_TX
FPGA_UART2_TX
FPGA_UART1_RX
FPGA_UART2_RX
USER_I2C_SCL
USER_I2C_SDA
USER_SPI_MISO
USER_SPI_CLK_S
USER_SPI_MOSI
USER_SPI_CS_N
FPGA_GPIO4
CLK_OSC2
C515 100nF X7R 50V 0603
C502 100nF X7R 50V 0603
C504 4.7uF X5R 16V 0603
USER_SPI_CLK
R517 33R 5% 0603
U201B
LFE5U-25F-7TG144C
PT67A VCCIO1
PT62B
PT62A
PT60B
PT60A
PT58B
PT58A
PT56B
PT56A
PT53B
PT53A
PT51A
PT42B
PT42A
PT40B
PT40A
GPIO – BANK 1
CPU_D7
CPU_D1
CPU_D6
CPU_D2
CPU_D5
CPU_D3
CPU_D4
MEM_WE_N_S
CPU_A14
CPU_A5
CPU_A13
CPU_A6
CPU_A12
CPU_A7
CPU_A11
CPU_A8
C506 100nF X7R 50V 0603
RGB_RED[0..3]
U201C
LFE5U-25F-7TG144C
PR23D/PCLKC2_0
PR23B/PCLKC2_1
PR23C/PCLKT2_0
PR23A/PCLKT2_1
PR20D
PR20B
PR20C/GR_PCLK2_0
PR20A/GR_PCLK2_1
PR14B
PR14C
PR14A VCCIO2
PR8D
PR8B
PR8C
PR8A
PR2D
PR2C
PR2B
GPIO – BANK 2
RGB_RED3
RGB_RED2
FPGA_CLOCK_PHI
RGB_RED1
RGB_RED0
MEM_A20_CE2_N_S
CPU_A0
CPU_A18
CPU_A1
CPU_A17
CPU_A2
CPU_A16
CPU_A3
CPU_A15
CPU_A4
MEM_CE_CE2_N_S
MEM_OE_N_S
CPU_D0
C507 100nF X7R 50V 0603
C508 4.7uF X5R 16V 0603
CPU RESET
R503 4K02 1% 0603
R504 4K02 1% 0603
CPU_RESET_N
Q501
MMUN2211LT1G
FPGA SD CARD
J501
Micro_SD_Molex_5033981892
DAT2
DAT3/CD
CMD
VDD
CLK
VSS
DAT0
DAT1
VSS
DET
SHIELD
R505 4K02 1% 0603 SD_SPI_CS_N
R506 10K 1% 0603 SD_SPI_MOSI
R507 10K 1% 0603 SD_SPI_CLK
R508 10K 1% 0603 SD_SPI_MISO
R509 10K 1% 0603 SD_DET_N
C512 100nF X7R 50V 0603
C513 4.7uF X5R 16V 0603
FPGA SD CARD ACTIVITY LED
D501
R518 4K02 1% 0603
R515 1K00 1% 0603
Q503
MMUN2211LT1G
Q502
MMUN2211LT1G
SD_SPI_CS_N
50 MHz FPGA LOGIC OSCILLATOR
PWR_FLAG
BLM18AG601SN1D
C509 100nF X7R 50V 0603
C510 100nF X7R 50V 0603
C511 4.7uF X5R 16V 0603
X501
50MHz 50PPM
R510 10K 1% 0603
CLK_OSC2
R511 33R 1% 0603
OUT VDD GND Tri-State
1 OSC2_EN
NOTE : LFE45U has different PLL pin input so PLL may not perform as 12U & 25U parts.
IF FPGA TO RCBUS: RTERM = 33ohm
IF RCBUS TO FPGA: RTERM = 0 ohm
CPU BUS SERIES TERMINATION
CPU_CLOCK_PHI R519 0R 5% 0603 FPGA_CLOCK_PHI
CPU_MREQ_N R520 0R 5% 0603 FPGA_MREQ_N
CPU_M1_N R521 0R 5% 0603 FPGA_M1_N
CPU_IORQ_N R522 0R 5% 0603 FPGA_IORQ_N
CPU_WR_N R523 0R 5% 0603 FPGA_WR_N
CPU_RD_N R524 0R 5% 0603 FPGA_RD_N
SRAM MEMORY SERIES TERMINATION
MEM_A20_CE2_N_S R516 33R 5% 0603
MEM_CE_CE2_N_S R512 33R 5% 0603
MEM_OE_N_S R513 33R 5% 0603
MEM_WE_N_S R514 33R 5% 0603
CPU_A[20..0]
CPU_D[7..0]
FPGA I/O
Micro-SD CARD
FPGA I/O & Micro SD Card Connection.
Title: PETER
Size: A
Date: 2024-07-29
Rev: 0.0
KiCad E.D.A. 8.0.4
Drawn: Denno Wiggle
Id: 5/12

FPGA CONFIGURATION

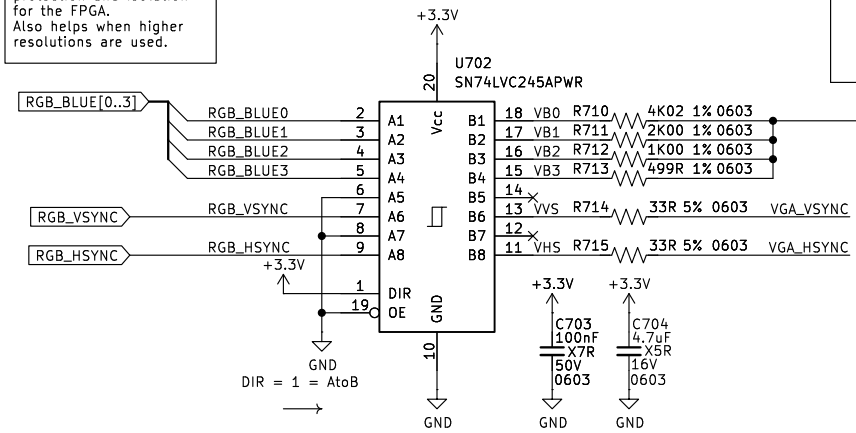


RGB BUFFERS OSCILLATOR VGA CONNECTOR

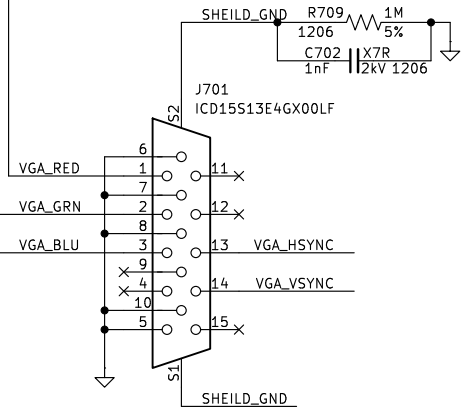


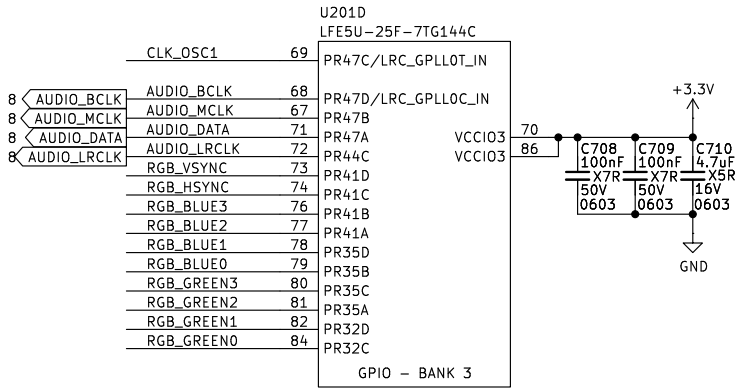
ISOLATION BUFFERS

Buffers added to provide protection and isolation for the FPGA.
Also helps when higher resolutions are used.



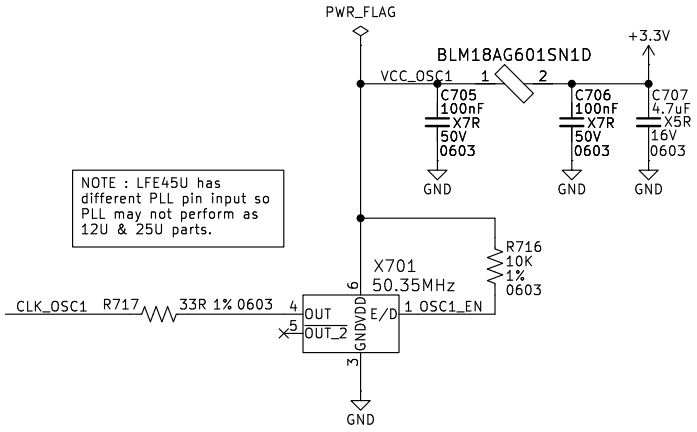
VGA CONNECTOR





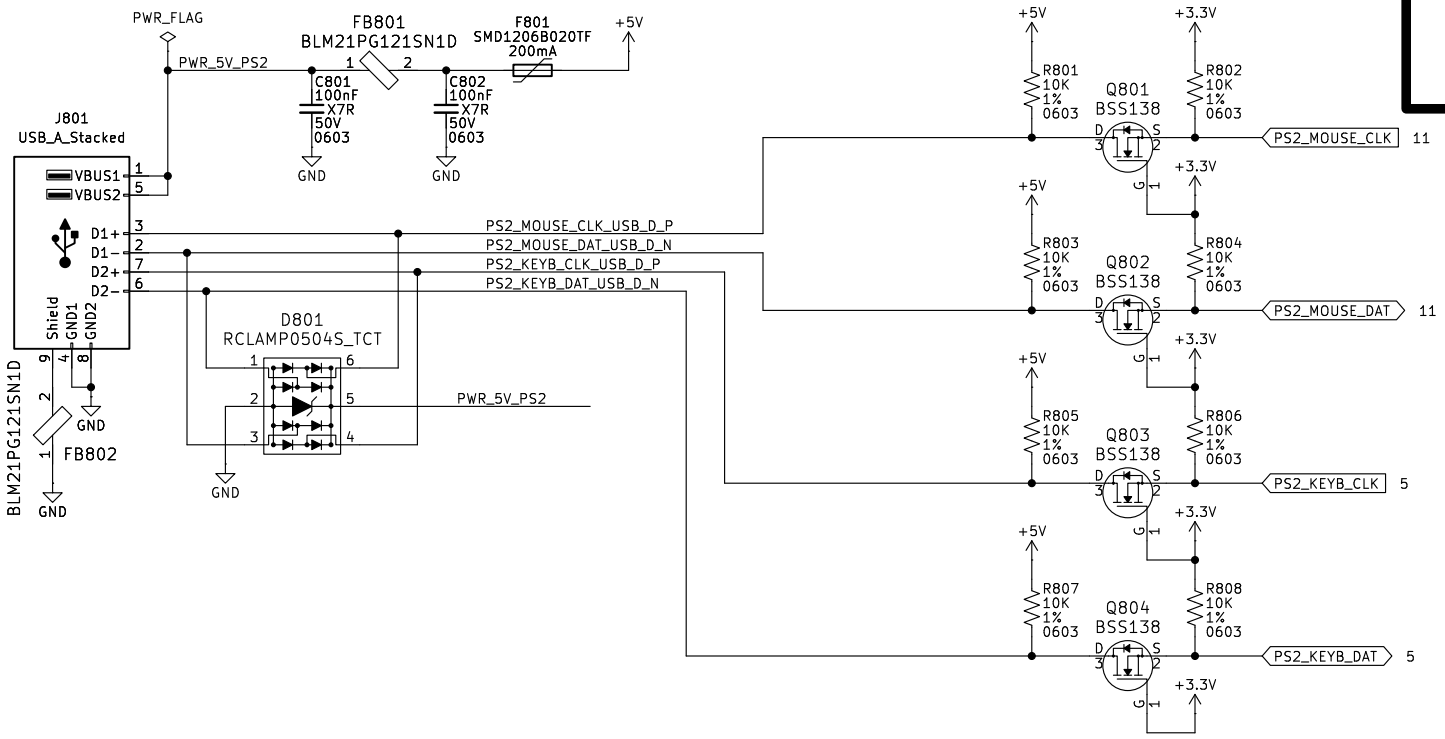
50.35MHz VGA OSCILLATOR

NOTE : LFE45U has different PLL pin input so PLL may not perform as 12U & 25U parts.

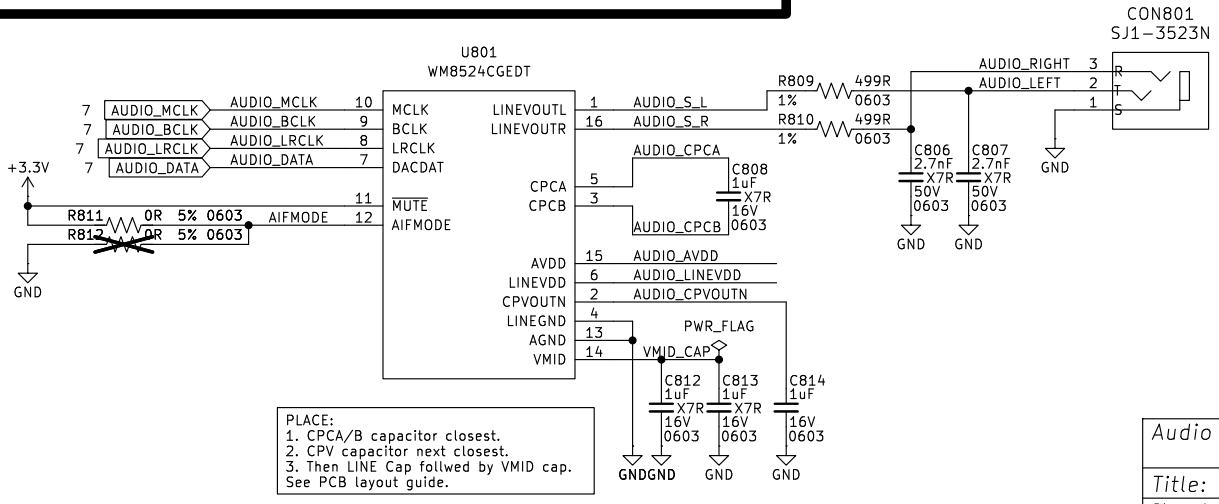


VGA Buffers and Connector. Pixel Clock Oscillator.		
Title: PETER		
Size: A	Date: 2024-07-29	Rev: 0.0
KiCad E.D.A. 8.0.4	Drawn: Denno Wiggle	Id: 7/12

PS2 MOUSE & KEYBOARD



AUDIO DAC & 3.5MM SOCKET

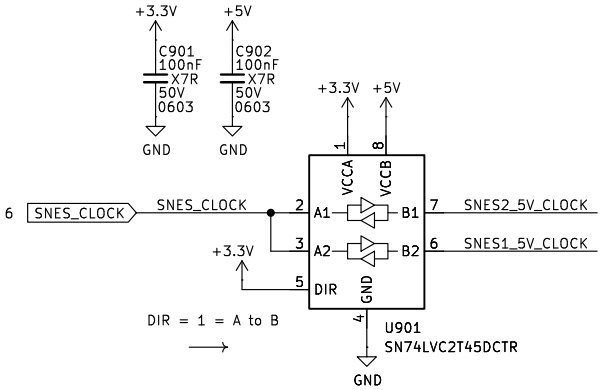


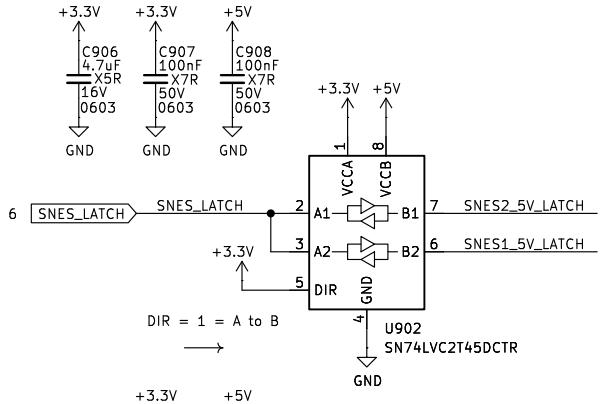
PLACE:
1. CPCA/B capacitor closest.
2. CPV capacitor next closest.
3. Then LINE Cap follwed by VMID cap.
See PCB layout guide.

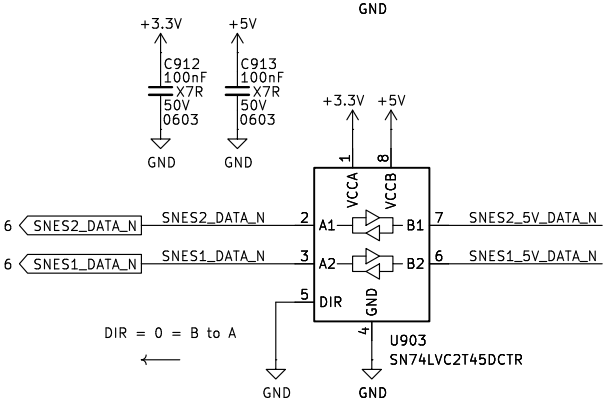
Audio DAC and PS2 Keyboard & Mouse Interface.		
Title: PETER		
Size: A	Date: 2024-07-29	Rev: 0.0
KiCad E.D.A. 8.0.4	Drawn: Denno Wiggle	Id: 8/12

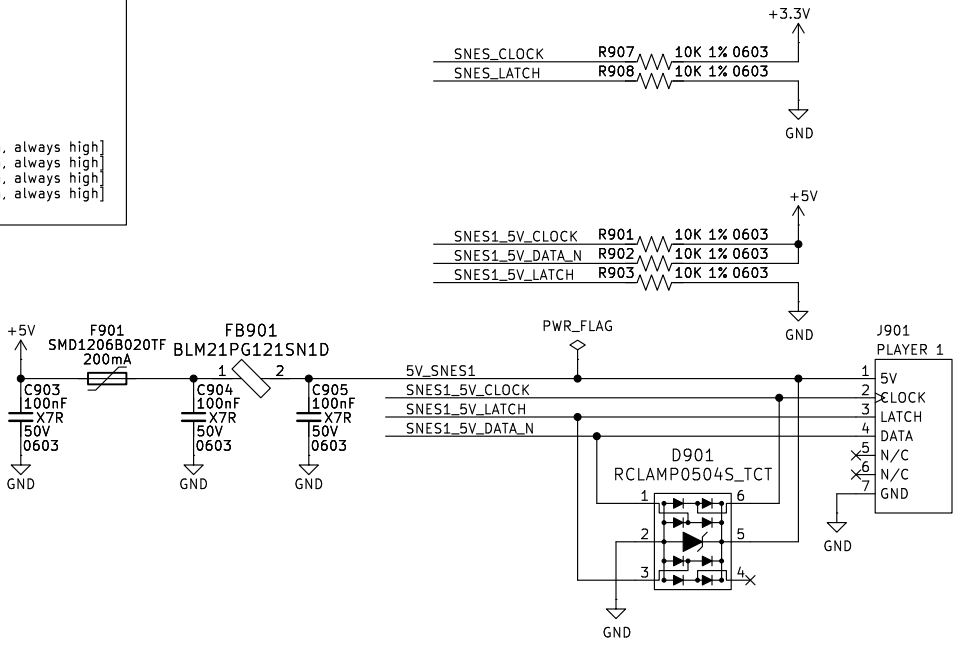
SNES CONNECTORS

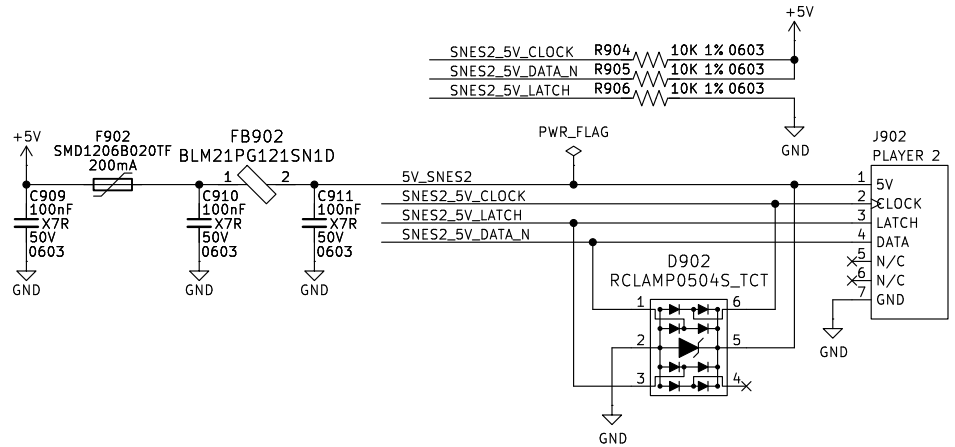
Clock pulse and corresponding button
0 B
1 Y
2 Select
3 Start
4 Up
5 Down
6 Left
7 Right
8 A
9 X
10 L
11 R
12 [no button, always high]
13 [no button, always high]
14 [no button, always high]
15 [no button, always high]



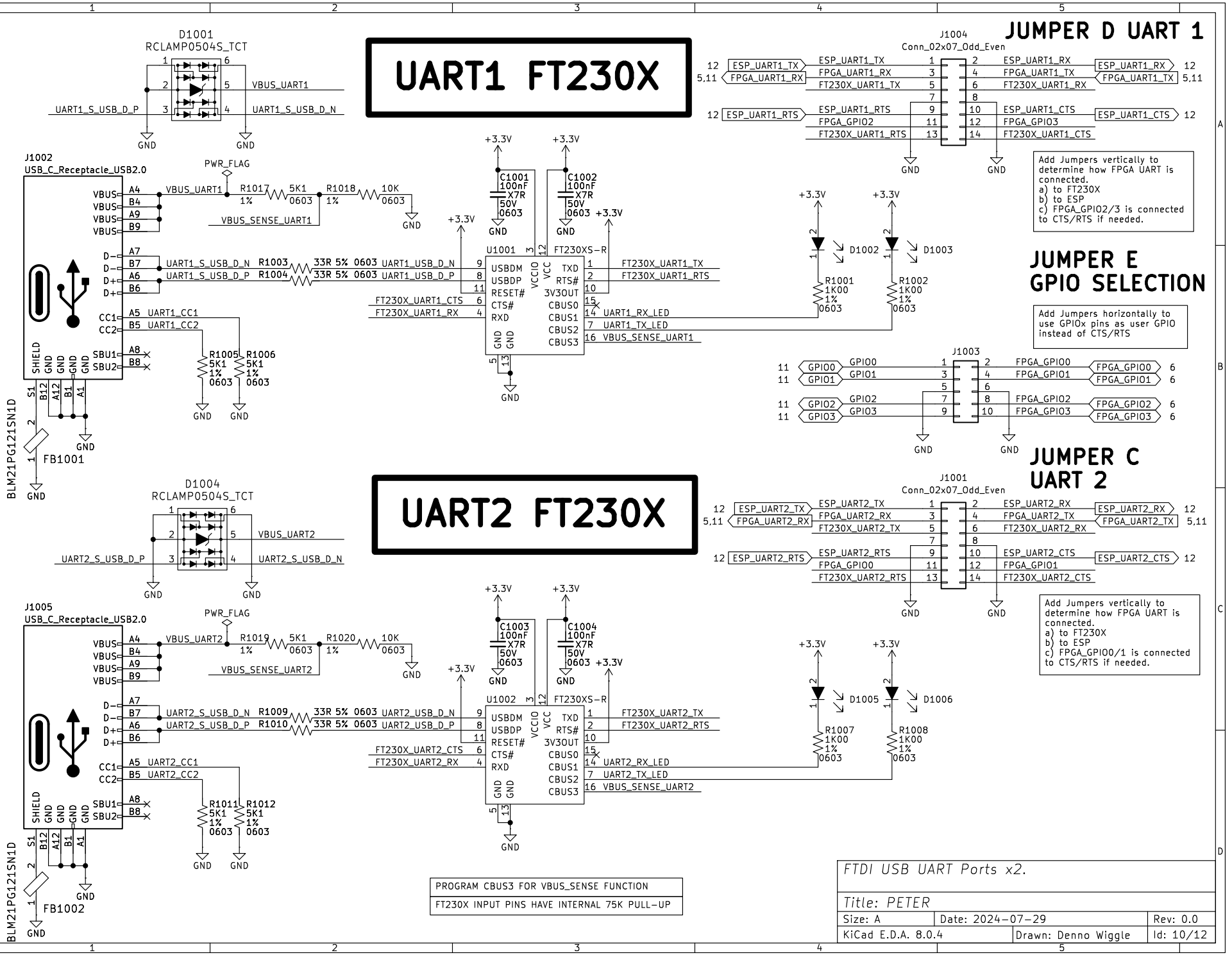






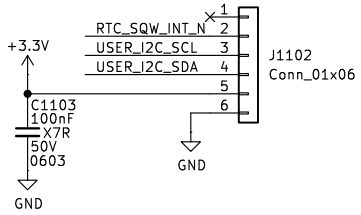


SNES Connectors x 2.		
Title: PETER		
Size: A	Date: 2024-07-29	Rev: 0.0
KiCad E.D.A. 8.0.4	Drawn: Denno Wiggle	Id: 9/12

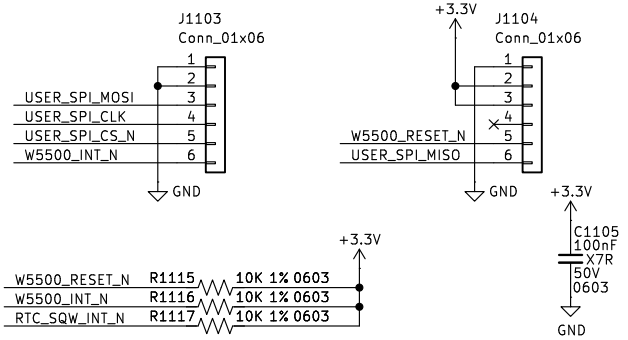

UART1 FT230X
UART2 FT230X
JUMPER D UART 1
JUMPER E GPIO SELECTION
JUMPER C UART 2
D1001 RCLAMP0504S_TCT
D1004 RCLAMP0504S_TCT
J1002 USB_C_Receptacle_USB2.0
J1005 USB_C_Receptacle_USB2.0
J1004 Conn_02x07_Odd_Even
J1003
J1001 Conn_02x07_Odd_Even
U1001 FT230XS-R
U1002 FT230XS-R
FB1001 BLM21PG121SN1D
FB1002 BLM21PG121SN1D
VBUS_UART1
VBUS_UART2
UART1_S_USB_D_P
UART1_S_USB_D_N
UART2_S_USB_D_P
UART2_S_USB_D_N
VBUS_SENSE_UART1
VBUS_SENSE_UART2
UART1_CC1
UART1_CC2
UART2_CC1
UART2_CC2
R1003 33R 5% 0603
R1004 33R 5% 0603
R1009 33R 5% 0603
R1010 33R 5% 0603
R1001 1K00 1% 0603
R1002 1K00 1% 0603
R1007 1K00 1% 0603
R1008 1K00 1% 0603
R1005 5K1 1% 0603
R1006 5K1 1% 0603
R1011 5K1 1% 0603
R1012 5K1 1% 0603
R1017 5K1 1% 0603
R1018 10K 0603
R1019 5K1 1% 0603
R1020 10K 0603
C1001 100nF X7R 50V 0603
C1002 100nF X7R 50V 0603
C1003 100nF X7R 50V 0603
C1004 100nF X7R 50V 0603
D1002
D1003
D1005
D1006
PWR_FLAG
+3.3V
GND
ESP_UART1_TX
ESP_UART1_RX
ESP_UART1_RTS
ESP_UART1_CTS
FPGA_UART1_TX
FPGA_UART1_RX
FPGA_UART1_RTS
FPGA_UART1_CTS
FT230X_UART1_TX
FT230X_UART1_RX
FT230X_UART1_RTS
FT230X_UART1_CTS
ESP_UART2_TX
ESP_UART2_RX
ESP_UART2_RTS
ESP_UART2_CTS
FPGA_UART2_TX
FPGA_UART2_RX
FPGA_UART2_RTS
FPGA_UART2_CTS
FT230X_UART2_TX
FT230X_UART2_RX
FT230X_UART2_RTS
FT230X_UART2_CTS
UART1_RX_LED
UART1_TX_LED
UART2_RX_LED
UART2_TX_LED
GPIO0
GPIO1
GPIO2
GPIO3
FPGA_GPIO0
FPGA_GPIO1
FPGA_GPIO2
FPGA_GPIO3
Add Jumpers vertically to determine how FPGA UART is connected.
a) to FT230X
b) to ESP
c) FPGA_GPIO2/3 is connected to CTS/RTS if needed.
Add Jumpers horizontally to use GPIOx pins as user GPIO instead of CTS/RTS
Add Jumpers vertically to determine how FPGA UART is connected.
a) to FT230X
b) to ESP
c) FPGA_GPIO0/1 is connected to CTS/RTS if needed.
PROGRAM CBUS3 FOR VBUS_SENSE FUNCTION
FT230X INPUT PINS HAVE INTERNAL 75K PULL-UP
FTDI USB UART Ports x2.
Title: PETER
Size: A
Date: 2024-07-29
Rev: 0.0
KiCad E.D.A. 8.0.4
Drawn: Denno Wiggle
Id: 10/12

USER IO, SPI, I2C

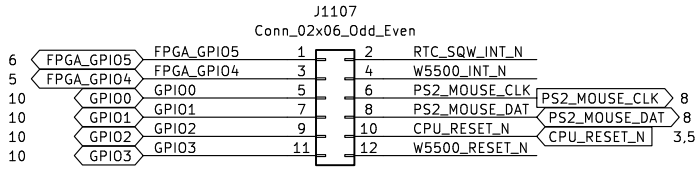
DS3132 RTC + AT24C32 MODULE



WIZMON W5500 ETHERNET MODULE



JUMPER F
FPGA I/O BOARD DEVICE SIGNAL SELECTION

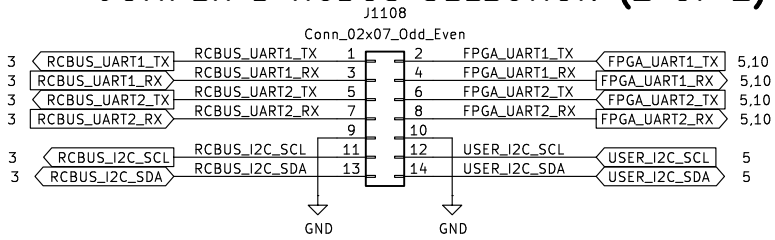


Add Jumpers to connect GPIO Pins on left side of connector to specific use signals if needed.

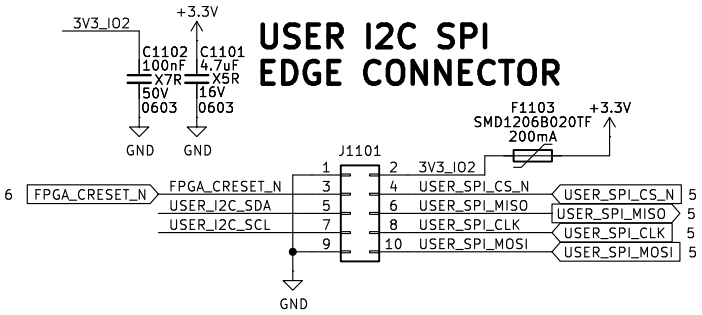
GPIO0–3 can be used for CTS/RTS instead. See FT230X page.

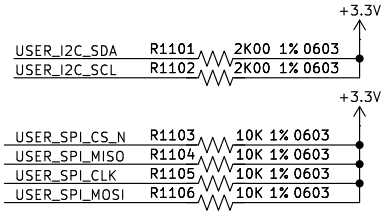
If using W5500 module add a vertical jumper between CPU_RESET_N & W5500_RESET_N or a horizontal jumper to GPIO3.

JUMPER B RCBUS SELECTION (2 OF 2)

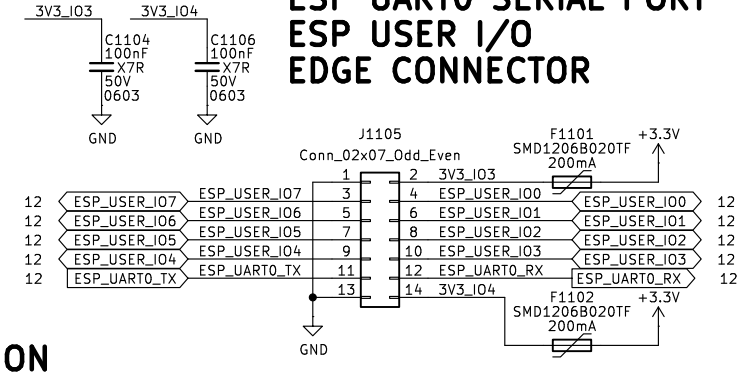


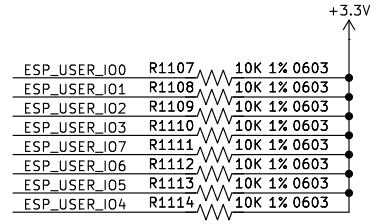
USER I2C SPI EDGE CONNECTOR





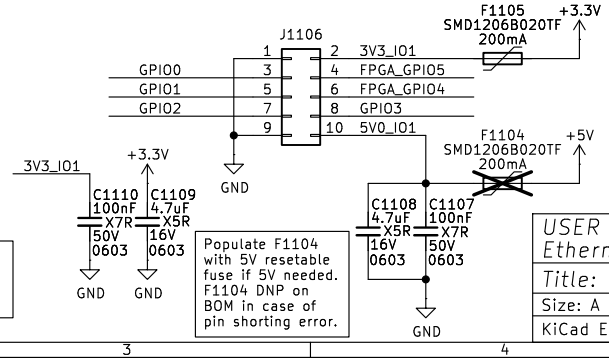
ESP UART0 SERIAL PORT
ESP USER I/O
EDGE CONNECTOR



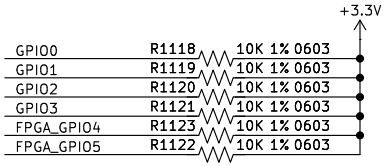


Do not populate ESP_USER_IO4 to 6 resistor if using ESP32 with Octal Flash (1.8V).

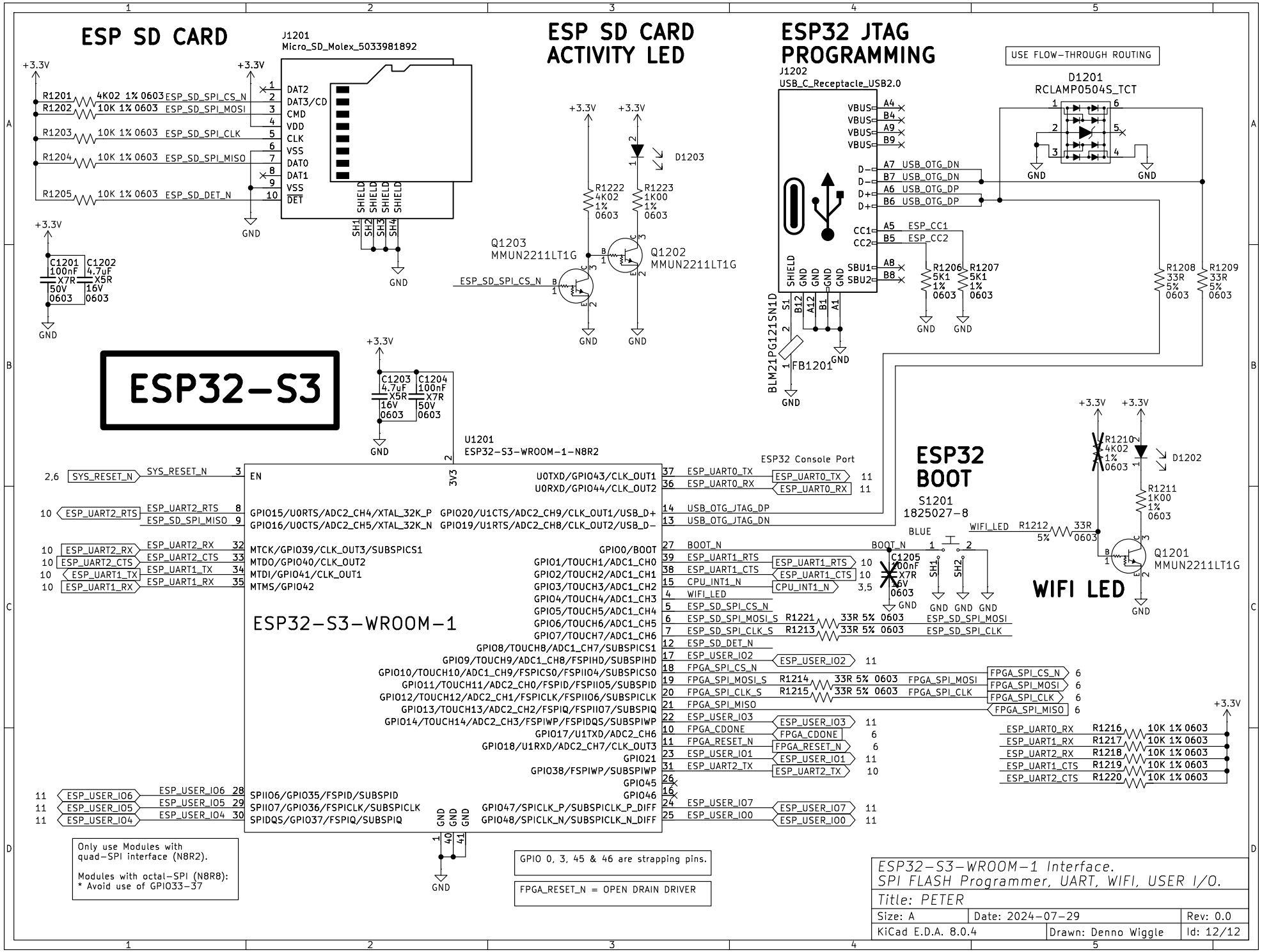
USER GPIO
EDGE CONNECTOR



Populate F1104 with 5V resetable fuse if 5V needed. F1104 DNP on BOM in case of pin shorting error.



USER I/O, SPI, I2C, DS3231 RTC & W5500 Ethernet Modules.RCBUS Jumper Selection.		
Title: PETER		
Size: A	Date: 2024-07-29	Rev: 0.0
KiCad E.D.A. 8.0.4	Drawn: Denno Wiggle	Id: 11/12


ESP SD CARD
J1201
Micro_SD_Molex_5033981892
R1201 4K02 1% 0603 ESP_SD_SPI_CS_N
R1202 10K 1% 0603 ESP_SD_SPI_MOSI
R1203 10K 1% 0603 ESP_SD_SPI_CLK
R1204 10K 1% 0603 ESP_SD_SPI_MISO
R1205 10K 1% 0603 ESP_SD_DET_N
DAT2
DAT3/CD
CMD
VDD
CLK
VSS
DAT0
DAT1
VSS
DET
SHIELD
+3.3V
GND
C1201 100nF X7R 50V 0603
C1202 4.7uF X5R 16V 0603
ESP SD CARD ACTIVITY LED
D1203
R1222 4K02 1% 0603
R1223 1K00 1% 0603
Q1203 MMUN2211LT1G
Q1202 MMUN2211LT1G
ESP_SD_SPI_CS_N
ESP32 JTAG PROGRAMMING
USE FLOW-THROUGH ROUTING
J1202
USB_C_Receptacle_USB2.0
D1201
RCLAMP0504S_TCT
VBUS
A7 USB_OTG_DN
B7 USB_OTG_DN
A6 USB_OTG_DP
B6 USB_OTG_DP
A5 ESP_CC1
B5 ESP_CC2
R1206 5K1 1% 0603
R1207 5K1 1% 0603
R1208 33R 5% 0603
R1209 33R 5% 0603
BLM21PG121SN1D
FB1201
ESP32-S3
C1203 4.7uF X5R 16V 0603
C1204 100nF X7R 50V 0603
U1201
ESP32-S3-WROOM-1-N8R2
ESP32-S3-WROOM-1
EN
3V3
GPIO15/U0RTS/ADC2_CH4/XTAL_32K_P
GPIO16/U0CTS/ADC2_CH5/XTAL_32K_N
MTCK/GPIO39/CLK_OUT3/SUBSPICS1
MTDO/GPIO40/CLK_OUT2
MTDI/GPIO41/CLK_OUT1
MTMS/GPIO42
U0TXD/GPIO43/CLK_OUT1
U0RXD/GPIO44/CLK_OUT2
GPIO20/U1CTS/ADC2_CH9/CLK_OUT1/USB_D+
GPIO19/U1RTS/ADC2_CH8/CLK_OUT2/USB_D-
GPIO0/BOOT
GPIO1/TOUCH1/ADC1_CH0
GPIO2/TOUCH2/ADC1_CH1
GPIO3/TOUCH3/ADC1_CH2
GPIO4/TOUCH4/ADC1_CH3
GPIO5/TOUCH5/ADC1_CH4
GPIO6/TOUCH6/ADC1_CH5
GPIO7/TOUCH7/ADC1_CH6
GPIO8/TOUCH8/ADC1_CH7/SUBSPICS1
GPIO9/TOUCH9/ADC1_CH8/FSPIHD/SUBSPIHD
GPIO10/TOUCH10/ADC1_CH9/FSPICS0/FSPII04/SUBSPICS0
GPIO11/TOUCH11/ADC2_CH0/FSPID/FSPII05/SUBSPID
GPIO12/TOUCH12/ADC2_CH1/FSPICLK/FSPII06/SUBSPICLK
GPIO13/TOUCH13/ADC2_CH2/FSPIQ/FSPII07/SUBSPIQ
GPIO14/TOUCH14/ADC2_CH3/FSPIWP/FSPIDQS/SUBSPIWP
GPIO17/U1TXD/ADC2_CH6
GPIO18/U1RXD/ADC2_CH7/CLK_OUT3
GPIO21
GPIO38/FSPIWP/SUBSPIWP
GPIO45
GPIO46
GPIO47/SPICLK_P/SUBSPICLK_P_DIFF
GPIO48/SPICLK_N/SUBSPICLK_N_DIFF
SPII06/GPIO35/FSPID/SUBSPID
SPII07/GPIO36/FSPICLK/SUBSPICLK
SPIDQS/GPIO37/FSPIQ/SUBSPIQ
SYS_RESET_N
ESP_UART2_RTS
ESP_SD_SPI_MISO
ESP_UART2_RX
ESP_UART2_CTS
ESP_UART1_TX
ESP_UART1_RX
ESP_USER_IO6
ESP_USER_IO5
ESP_USER_IO4
ESP32 Console Port
ESP_UART0_TX
ESP_UART0_RX
USB_OTG_JTAG_DP
USB_OTG_JTAG_DN
BOOT_N
ESP_UART1_RTS
ESP_UART1_CTS
CPU_INT1_N
WIFI_LED
ESP_SD_SPI_CS_N
ESP_SD_SPI_MOSI_S
ESP_SD_SPI_CLK_S
ESP_SD_DET_N
ESP_USER_IO2
FPGA_SPI_CS_N
FPGA_SPI_MOSI_S
FPGA_SPI_CLK_S
FPGA_SPI_MISO
ESP_USER_IO3
FPGA_CDONE
FPGA_RESET_N
ESP_USER_IO1
ESP_UART2_TX
ESP_USER_IO7
ESP_USER_IO0
R1221 33R 5% 0603
R1213 33R 5% 0603
R1214 33R 5% 0603
R1215 33R 5% 0603
FPGA_SPI_MOSI
FPGA_SPI_CLK
ESP32 BOOT
S1201
1825027-8
BLUE
C1205 100nF X7R 16V 0603
SH1
SH2
WIFI LED
R1210 4K02 1% 0603
D1202
R1211 1K00 1% 0603
R1212 33R 5% 0603
Q1201 MMUN2211LT1G
R1216 10K 1% 0603
R1217 10K 1% 0603
R1218 10K 1% 0603
R1219 10K 1% 0603
R1220 10K 1% 0603
Only use Modules with quad-SPI interface (N8R2).
Modules with octal-SPI (N8R8):
* Avoid use of GPIO33-37
GPIO 0, 3, 45 & 46 are strapping pins.
FPGA_RESET_N = OPEN DRAIN DRIVER
ESP32-S3-WROOM-1 Interface.
SPI FLASH Programmer, UART, WIFI, USER I/O.
Title: PETER
Size: A
Date: 2024-07-29
Rev: 0.0
KiCad E.D.A. 8.0.4
Drawn: Denno Wiggle
Id: 12/12