SEWER Simple Eval With EZ80F91 on RCBUS

PAGE 1: INTRODUCTION

RcBusInterface

File: RcBusInterface.kicad sch CpuPowerZdi

File: ez80_PowerZdi.kicad_sch CpuAddressData

File: ez80_AddressDataBus.kicad_sch CpuEthernet

File: ez80_EthernetInterface.kicad_sch CpuGpioRtc

File: ez80_Gpio.kicad_sch

PAGE 2: RCBUS INTERFACE

PAGE 3: CPU POWER & ZDI

PAGE 4: CPU ADDRESS & DATA BUS

PAGE 5 : CPU ETHERNET

PAGE 6: CPU GPIO & RTC

LOG02

PCB STACKUP NOTE



JLC04161H-3313 stackup gives : * Ideal trace impedance (50 & 100ohms). * GND plane closer to signal layer routing for improved signal integrity.

MOUNTING/TOOLING HOLES











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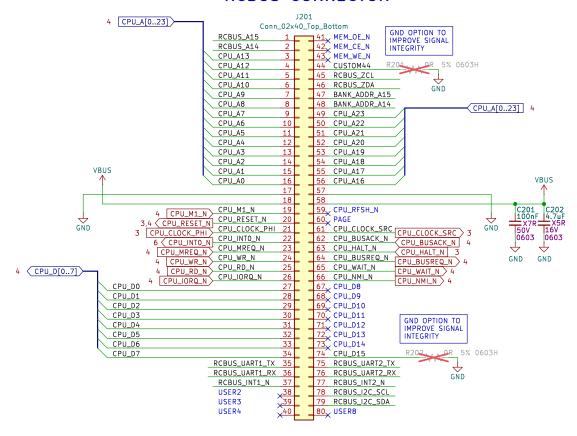
Simple Eval With EZ80F91 on RCBUS

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RCBUS Interface

RCBUS CONNECTOR



RCBUS STUFFING OPTION FOR MEMORY BANKING

To use memory banking with a 16K granularity on PETER populate R203 & R204, remove R205 & R206, and cut RCBUS pins A16 through to A20.

To use memory banking with a 32K granularity on PETER populate R203, remove R205, and cut RCBUS pins A16 through to A20.

RCBUS_A15	R205	5% 0603H	
BANK_ADDR_A15	R203 VVVOR	5% 0603H	CPU_A15
RCBUS_A14	R206 AAA OR	5% 0603H	
BANK_ADDR_A14	R204 VVOR	5% 0603H	CPU_A14

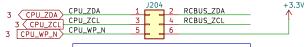
RCBUS JUMPERS JUMPER A

				J202		
6 .	CPU_UART2_RXD	CPU_UART2_RXD	1		_ 2_	RCBUS_UART2_RX
٠ -	CPU_UART1_RXD	CPU_UART1_RXD	3		4	RCBUS_UART1_RX
٠ ٥	CPU_UART1_RXD	CPU_UART2_TXD	5		6	RCBUS_UART2_TX
6	CPU_UARTZ_IXD	CPU_UART1_TXD	7		8	RCBUS_UART1_TX
0	CPU_UARI1_IXD					

JUMPER B

			J203		
6 CPU I2C SDA	CPU_I2C_SDA	1	5205	1 2	RCBUS_I2C_SDA
6 CDIL 12C SCI	CPU_I2C_SCL	3		4	RCBUS_I2C_SCL
C COULINITA N	CPU_INT2_N	5		6	RCBUS_INT2_N
CPU_INT2_N	CPU_INT1_N	7	Γ -	8	RCBUS_INT1_N
D C CPU INTT N			P =	-	

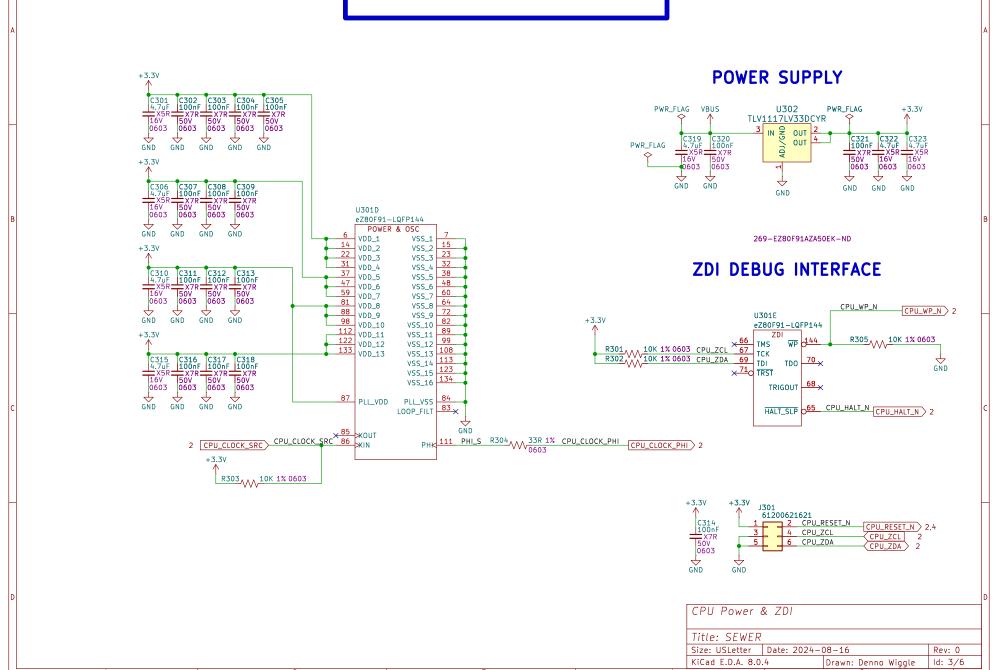
JUMPER C



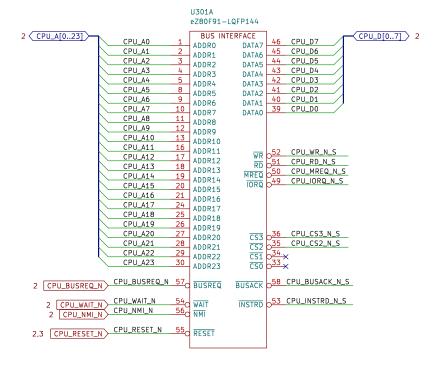
Install Jumper between J204.5 and J204.6 to write to the internal CPU FLASH memory.

RCBUS Interi	ace		
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CPU Power & ZDI



CPU Address & Data Bus



INPUT SIGNAL PULL-UPS

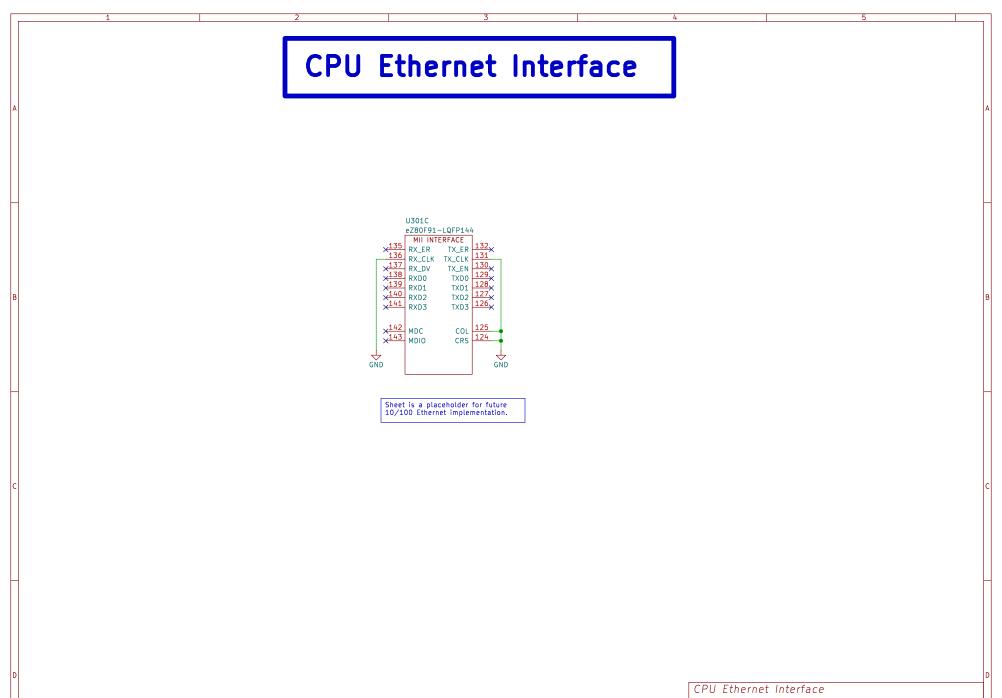
		+3.3V
		1
CPU_RESET_N	R410 A A A 10K 1% 0603	5
CPU_BUSREQ_N	R411 VVV 10K 1% 0603	i I
CPU_WAIT_N	R412 VVV 10K 1% 0603	i i
CPU_NMI_N	R413 VVV 10K 1% 0603	Ĭ
CPU_MREQ_N_S	R417 VVV 10K 1% 0603	Ĭ
CPU_IORQ_N_S	R418 VVV 10K 1% 0603	5

Rev: 0

ld: 4/6

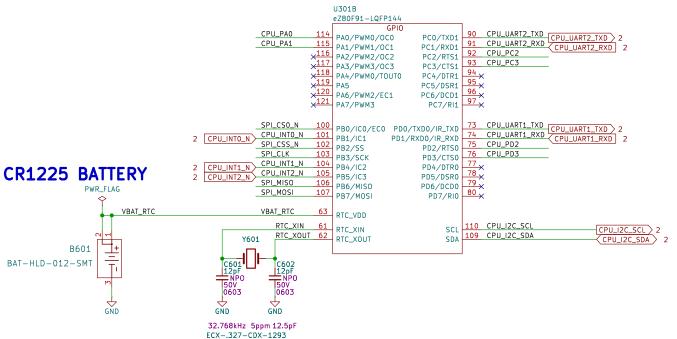
SERIES TERMINATORS

CPU_INSTRD_N_S R401	
CPU_MREQ_N_S R405 33R 1% 0603 CPU_MREQ_N CPU_CS3_N_S R406 33R 1% 0603 CPU_MREQ_N 2	
CPU_IORQ_N_S R407 33R 1% 0603 CPU_IORQ_N CPU_IORQ_N 2 CPU_IORQ_N 3 CPU	
Stuffing option for the CPU_M/IOREQ_N signal Title: SEWER	
to use CS timing or M/IOREQ timing. * Co-locate resistors. Size: USLetter Date: 2024-08-16	
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CPU GPIO RTC



TTL LEVEL CPU SIGNAL HEADER

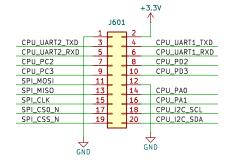
+3.3V

16V 0603

GND

C604 C605 100nF 100nF

50V 50V 0603 0603



		<u> </u>
SPI_MOSI	R602	AAA 10K 1% 0603
SPI_MISO	R603	VVV10K 1% 0603
SPI_CLK	R604	VVV 10K 1% 0603
SPI_CSO_N	R605	VVV10K 1% 0603
SPI_CSS_N	R606	VVV10K 1% 0603
CPU_I2C_SCL	R607	VVV10K 1% 0603
CPU_I2C_SDA	R608	VVV 10K 1% 0603
CPU_PA0	R609	VVV10K 1% 0603
CPU_PA1	R610	VVV10K 1% 0603
CPU_PC2	R611	VVV10K 1% 0603
CPU_PC3	R612	VVV10K 1% 0603
CPU_PD2	R613	VVV10K 1% 0603
CPU_PD3	R614	VVV10K 1% 0603
CPU_UART1_RXD	R615	VVV10K 1% 0603
CPU_UART2_RXD	R616	VVV10K 1% 0603
CPU_INTO_N	R617	VVV10K 1% 0603
CPU_INT1_N	R618	VVV10K 1% 0603
CPU_INT2_N	R619	10K 1% 0603
		-

+3.3V

CPU GPIO &	Real Time	Clock				
T.U. 651/55						
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