# SEWER Simple Eval With EZ80F91 on RCBUS

PAGE 1: INTRODUCTION

RcBusInterface

PAGE 2: RCBUS INTERFACE

File: RcBusInterface.kicad\_sch CpuPowerZdi

PAGE 3: CPU POWER & ZDI

File: ez80\_PowerZdi.kicad\_sch CpuAddressData

PAGE 4: CPU ADDRESS & DATA BUS

File: ez80\_AddressDataBus.kicad\_sch

puEthernet

PAGE 5: CPU ETHERNET

File: ez80\_EthernetInterface.kicad\_sch CpuGpioRtc

PAGE 6: CPU GPIO & RTC

File: ez80\_Gpio.kicad\_sch

1.0G01

10602

#### PCB STACKUP NOTE



JLC04161H-3313 stackup gives : \* Ideal trace impedance (50 & 1000hms). \* GND plane closer to signal layer routing for improved signal integrity.

#### MOUNTING/TOOLING HOLES

H1 H2 MountingHole H2 H3 MountingHole H4 MountingHole MountingHole MountingHole

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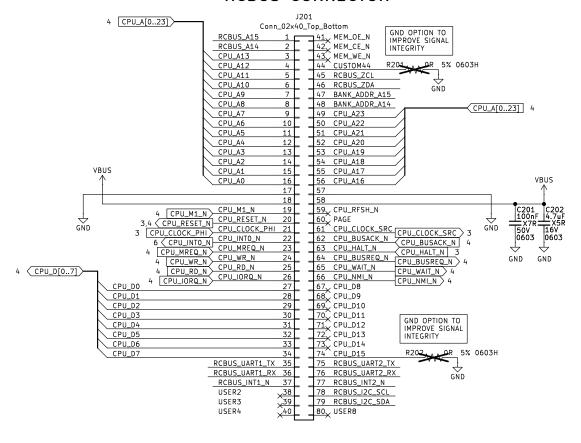
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3

### **RCBUS** Interface

#### RCBUS CONNECTOR



## RCBUS STUFFING OPTION FOR MEMORY BANKING

To use memory banking with a 16K granularity on PETER populate R203 & R204, remove R205 & R206, and cut RCBUS pins A16 through to A20.

To use memory banking with a 32K granularity on PETER populate R203, remove R205, and cut RCBUS pins A16 through to A20.

RCBUS_A15	R205 <sub>AAA</sub> OR		
BANK_ADDR_A15	R203 VVVOR	5% 0603H	CPU_A15
RCBUS_A14		5% 0603H	
BANK_ADDR_A14	R204 VV OR	5% 0603H	CPU_A14

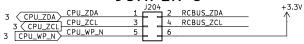
## RCBUS JUMPERS JUMPER A

				1202		
6.	CPU_UART2_RXD	CPU_UART2_RXD	1 [		2	RCBUS_UART2_RX
٠ ٠	CPU_UARTZ_RXD	CPU_UART1_RXD	3 [		4	RCBUS_UART1_RX
٠ ٥	CPU_UARTI_RXU	CPU_UART2_TXD	5		6	RCBUS_UART2_TX
0	CPU_UARTZ_IXD	CPU UART1 TXD	7		8	RCBUS UART1 TX
6	CPU_UARI1_IXD >		$\rightarrow$	_	_	

#### JUMPER B

		1	203		
6 CPILIZC SDA	CPU_I2C_SDA	1 É		2	RCBUS_I2C_SDA
6 CPU_IZC_SDA	CPU_I2C_SCL	3		4	RCBUS_I2C_SCL
6 CPU_IZC_SCL	CPU_INT2_N	5	. 1	6	RCBUS_INT2_N
6 CPU_INT2_N	CPU_INT1_N	7	1	8	RCBUS_INT1_N
b ( CPU_INII_N			, 7		

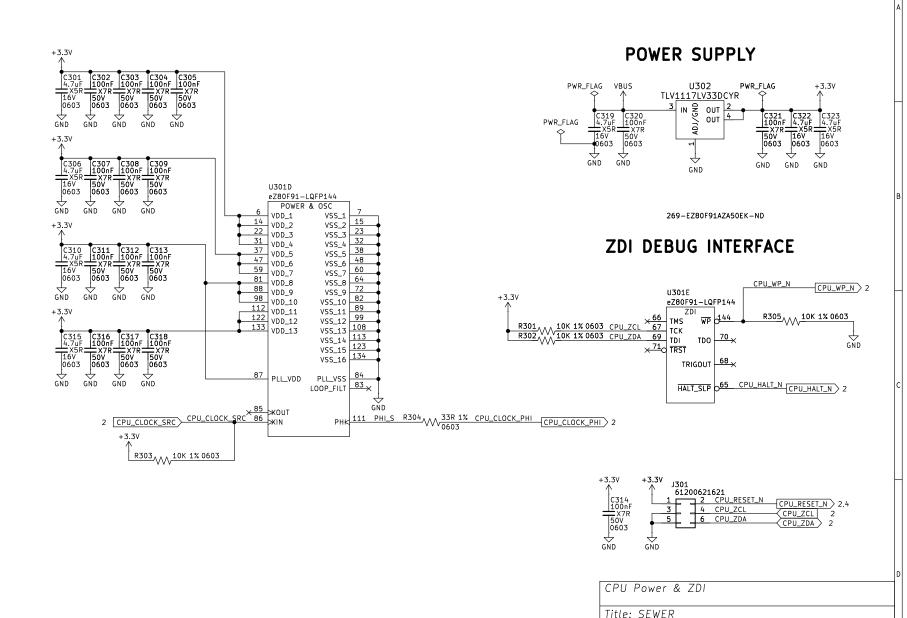
#### JUMPER C



Install Jumper between J204.5 and J204.6 to write to the internal CPU FLASH memory.

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Size: USLetter	Date: 2024-0	08-16	Rev: 0		
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### CPU Power & ZDI



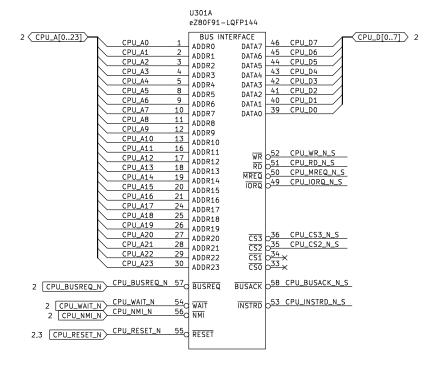
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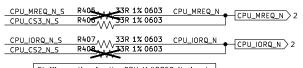


## INPUT SIGNAL PULL-UPS

	+3.3
	<b>1</b>
CPU_RESET_N	R410 A A A 10K 1% 0603
CPU_BUSREQ_N	R411 VVV 10K 1% 0603
CPU_WAIT_N	R412 VVV 10K 1% 0603
CPU_NMI_N	R413 VVV 10K 1% 0603
CPU_MREQ_N_S	R417 VVV 10K 1% 0603
CPU_IORQ_N_S	R418 VVV 10K 1% 0603

#### **SERIES TERMINATORS**

CPU_INSTRD_N_S CPU_WR_N_S CPU_RD_N_S	R401 33R 1% 0603 R402 33R 1% 0603 R403 33R 1% 0603 R404 33R 1% 0603	CPU_M1_N CPU_WR_N CPU_RD_N	CPU_M1_N
CPU_BUSACK_N_S	R404 VV 33R 1% 0603	CPU_BUSACK_N	CPU_BUSACK_N 2

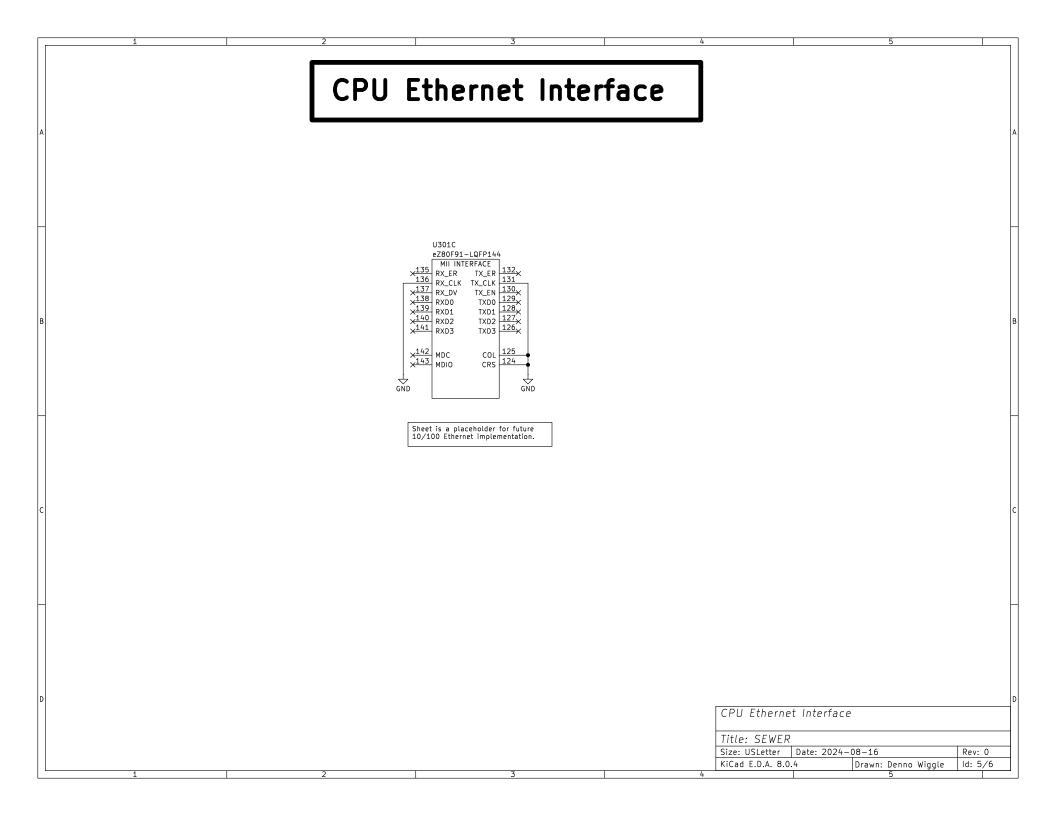


Stuffing option for the CPU\_M/IOREQ\_N signal to use CS timing or M/IOREQ timing.
\* Co-locate resistors.

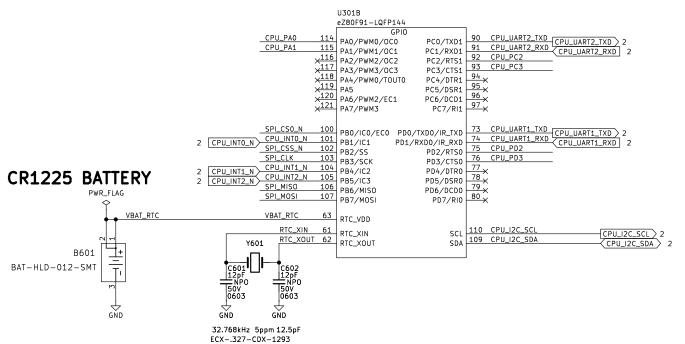
CPU Address and Data Bus

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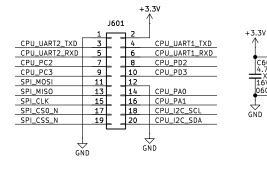
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# CPU GPIO RTC



#### TTL LEVEL CPU SIGNAL HEADER



		†
SPI_MOSI	R602	10K 1% 0603 \
SPI_MISO	R603	VVV10K 1% 0603
SPI_CLK	R604	VVV10K 1% 0603
SPI_CSO_N	R605	VVV10K 1% 0603
SPI_CSS_N	R606	VVV10K 1% 0603
CPU_I2C_SCL	R607	VVV10K 1% 0603
CPU_I2C_SDA	R608	VVV10K 1% 0603
CPU_PA0	R609	VVV10K 1% 0603
CPU_PA1	R610	VVV10K 1% 0603
CPU_PC2	R611	VVV10K 1% 0603
CPU_PC3	R612	VVV10K 1% 0603
CPU_PD2	R613	VVV10K 1% 0603
CPU_PD3	R614	VVV10K 1% 0603
CPU_UART1_RXD	R615	VVV10K 1% 0603
CPU_UART2_RXD	R616	VVV10K 1% 0603
CPU_INTO_N	R617	VVV10K 1% 0603
CPU_INT1_N	R618	VVV10K 1% 0603
CPU_INT2_N	R619	VVV10K 1% 0603
		- v v v

+3.3V

	CPU GPIO &	Real Time	Clock	
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2