## INPUT SIGNAL SERIES TERMINATORS Z8S180 20 MHZ CPU **PULL-UPS** 33R 1% 0603H CPU\_IORQ\_N 33R 1% 0603H CPU\_MREQ\_N CPU\_MREQ\_N\_S R2 CPU\_CLOCK\_SRC R3 33R 1% 0603H CPU\_M1\_N R4 R5 CPU\_M1\_N\_S CPU\_RESET\_N 33R 1% 0603H CPU\_WR\_N -\(\sqrt{\frac{10K}{10K}}\frac{1\chi}{10K}\frac{1\chi}{10K}\frac{10K}{10K}\frac{1 CPU\_WR\_N\_S R6 CPU\_BUSREQ\_N R7 33R 1% 0603H CPU\_RD\_N R8 VVV33R 1% 0603H CPU\_NU\_N R10 AAA 33R 1% 0603H CPU\_CLOCK\_PHI R9 CPU\_RD\_N\_S CPU\_WAIT\_N -\(\sqrt{\frac{10K}{10K}}\frac{1\chi}{0603H}\) R10 VVV33R 1% 0603H CPU\_BUSACK\_N R12 VV33R 1% 0603H CPU\_BUSACK\_N COLUMN TEND1 N CPU\_PHI\_S CPU\_NMI\_N Z8S18020FSG R13 CPU\_INTO\_N R15 VVV10K 1% 0005 CPU\_INT1\_N R17 W 10K 1% 0603H CPU\_INT2\_N D5 40 CPU\_D5 CPU\_IORQ\_N\_S ĪORQ CPU\_DREQ1\_N CPU\_MREQ\_N\_S 66 MREQ 39 CPU\_D4 DΔ CPU E 67 38 CPU\_D3 D3 37 CPU\_D2 +3.3V CPU\_M1\_N\_S 68 M1 D2 CPU\_WR\_N\_S 69 36 CPU\_D1 RCBUS JUMPERS $\overline{\mathsf{WR}}$ D1 CPU\_RD\_N\_S 70 35 CPU\_D0 $\overline{RD}$ DΛ CPU\_PHI\_S 71 +3.37 PHI GND 72 <sub>GND</sub> 33 CPU\_A19 RCBUS\_UART1\_TX A19 73 RCBUS\_UART2\_TX 3 GND VDD 74 XTAL 75 NC 76 EXTA CPU\_A18 RCBUS\_UART1\_RX 5 C2 100nF 4.7uF 100nF X5R X7R 16V 50V 0603H 0603H A18 GŇD RCBUS\_UART2\_RX 7 NC CPU\_CLOCK\_SRC CPU\_A17 RCBUS\_INT2\_N EXTAL A17 CPU\_WAIT\_N 77 CPU\_A16 28 RCBUS\_INT1\_N WAIT A16 78 BUSACK A15 27 CPU\_A15 CPU\_BUSACK\_N\_S A14 26 CPU\_A14 RCBUS CONNECTOR CPU\_BUSREQ\_N 79 RCBUS\_DREQO\_N BUSREQ A13 25 CPU\_A13 CPU\_RESET\_N RCBUS\_TENDO\_N 3 RESET RCBUS\_DREQ1\_N RCBUS\_TEND1\_N Conn\_02x40\_Top\_Bottom 41 MEM\_OE\_N 42 MEM\_CE\_N 43 MEM\_WE\_N 44 CUSTOM 44 45 RCBUS\_DEGO\_N CPU\_A15 C3 4.7uF X5R X5R X7R 16V 0603H CPU\_A14 CPU\_A13 CPU A5 CPU A6 CPU A7 CPU A8 CPU A9 CPU A10 CPU A10 CPU\_A12 CPU\_A11 46 RCBUS\_TENDO\_N 47 RCBUS\_DREQ1\_N CPU\_A10 CPU\_A9 GŇD TTL LEVEL CPU 48 RCBUS\_TEND1\_N CPU\_A8 8 GND CPU\_A7 9 49 CPU\_A23 SIGNAL HEADER 50 CPU\_A22 51 CPU\_A21 52 CPU\_A20 53 CPU\_A19 CPU\_A6 10 L CPU\_A5 11 PWR\_FLAG +3.30 CPU\_A4 PWR\_FLAG J3 CPU\_A3 13 CPU\_A2 14 \_54 CPU\_A18 55 <u>CPU\_A17</u> CPU\_A1 +3.3٧ 15 ZORO CPU CKS CPU\_A0 16 56 CPU\_A16 CPU\_TXS 17 CPU\_CKA1 57 **Z8S180 ON RCBUS ONLY** 18 9 [ \_\_58 CPU\_M1\_N 59 CPU\_RFSH\_N CPU\_TXA1 19 11 60 PAGE 61 CPU\_CLOCK\_SRC CPU\_RESET\_N 20 CPU TXA0 13 CPU\_CLOCK\_PHI 21 CPU\_DCDO\_N 15 CPU\_INTO\_N 22 62 CPU\_BUSACK\_N CPU RTSO N 17 CPU\_MREQ\_N 23 63 CPU\_HALT\_N 64 CPU\_BUSREQ\_N 19 CPU\_WR\_N 24 CPU\_RD\_N 25 65 CPU\_WAIT\_N GND 66 CPU\_NMI\_N CPU\_IORQ\_N 26 PCB STACKUP NOTE 67 CPU\_D8 68 CPU\_D9 69 CPU\_D10 LOG02 CPU\_D0 27 CPU\_D1 28



CPU\_D2

CPU D3

CPU\_D4

CPU\_D5

CPU\_D6

CPU\_D7

IISFR2

USER3 USER4

RCBUS\_UART1\_TX 35 RCBUS\_UART1\_RX 36

RCBUS\_INT1\_N

29

30

31

32

33

34

37

<sub>~</sub>38 [

70 CPU\_D11

71 CPU\_D12 72 CPU\_D13

73× CPU\_D14

78 12C\_SCL 79 12C\_SDA

\_\_\_\_74\(\hat{C}\) CPU\_D15

75 RCBUS\_UART2\_TX

76 RCBUS\_UART2\_RX 77 RCBUS\_INT2\_N

JLC04161H-7628 (STD) stackup gives : 50ohm trace impedance for 13mil trace.

## MOUNTING/TOOLING HOLES

OH1
MountingHole
MountingHole
MountingHole
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MountingHole

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Z8S180 On	On RCBUS Only			
Title: ZORO				
Size: USLetter	Date: 2024-07-24		Rev: 0	
KiCad E.D.A. 8.0.4		Drawn: Denno Wiggle	ld: 1/1	

R32

R33 CPU\_CTSO\_N R34 VVV10K 1% U0U3...
R35 VVV10K 1% U0U3...

CPII RXA0

CPU\_RXA1

CPU RXS

+3.37

10K 1% 0603H

√10K 1% 0603H

10K 1% 0603H

√10K 1% 0603H

CPU TXA0

4 CPU\_TXA1

6 CPU\_RXA0

8 CPU\_RXA1

10 CPU\_INT2\_N

12 CPU\_INT1\_N

4 CPU\_CKA1

+3.3٧

+3.3V

<u> 6</u>

8

10

12

20

GND

10K 1% 0603H

10K 1% 0603H

CPU RXS

CPU CKAO

CPU\_RXA1

14 CPU\_RXA0 16 CPU\_E

18 CPU\_CTSO\_N

CPU\_DREQ1\_N

C5 C6 4.7uF 100nF

0603H 0603H

GND

+3.30

8 CPU\_TEND1\_N

6

-\(\sqrt{\frac{10K}{10K}}\frac{1% 0603H}{20K}\frac{1}{2}\(\sqrt{\frac{1}{2}}\)