SEWER
Simple Eval With EZ80F91 on RCBUS

PAGE 1 : INTRODUCTION

RcBusInterface

File: RcBusInterface.kicad_sch

PAGE 2 : RCBUS INTERFACE

CpuPowerZdi

File: ez80_PowerZdi.kicad_sch

PAGE 3 : CPU POWER & ZDI

CpuAddressData

File: ez80_AddressDataBus.kicad_sch

PAGE 4 : CPU ADDRESS & DATA BUS

CpuEthernet

File: ez80_EthernetInterface.kicad_sch

PAGE 5 : CPU ETHERNET

CpuGpioRtc

File: ez80_Gpio.kicad_sch

PAGE 6 : CPU GPIO & RTC

LOGO1 LOGO2

PCB STACKUP NOTE

JLC04161H-3313 stackup gives :
* Ideal trace impedance (50 & 100ohms).
* GND plane closer to signal layer routing for improved signal integrity.

MOUNTING/TOOLING HOLES

H1 MountingHole H2 MountingHole H3 MountingHole H4 MountingHole H5 MountingHole

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Title: SEWER		
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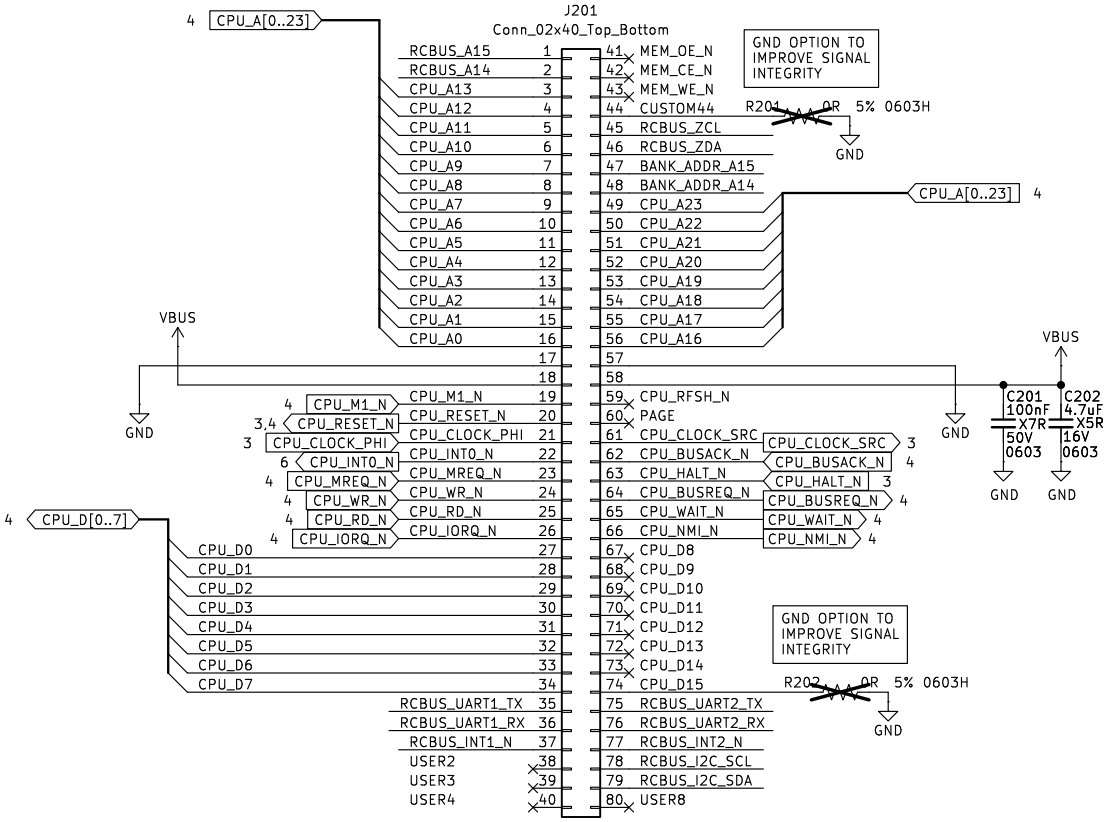
RCBUS Interface

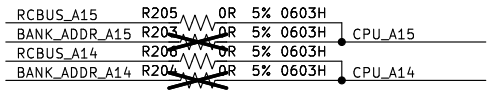
RCBUS CONNECTOR



RCBUS STUFFING OPTION FOR MEMORY BANKING

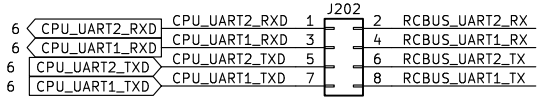
To use memory banking with a 16K granularity on PETER populate R203 & R204, remove R205 & R206, and cut RCBUS pins A16 through to A20.

To use memory banking with a 32K granularity on PETER populate R203, remove R205, and cut RCBUS pins A16 through to A20.

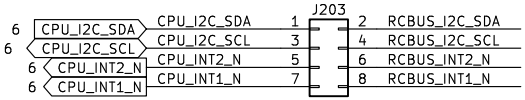


RCBUS JUMPERS

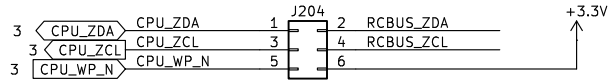
JUMPER A



JUMPER B



JUMPER C



Install Jumper between J204.5 and J204.6 to write to the internal CPU FLASH memory.

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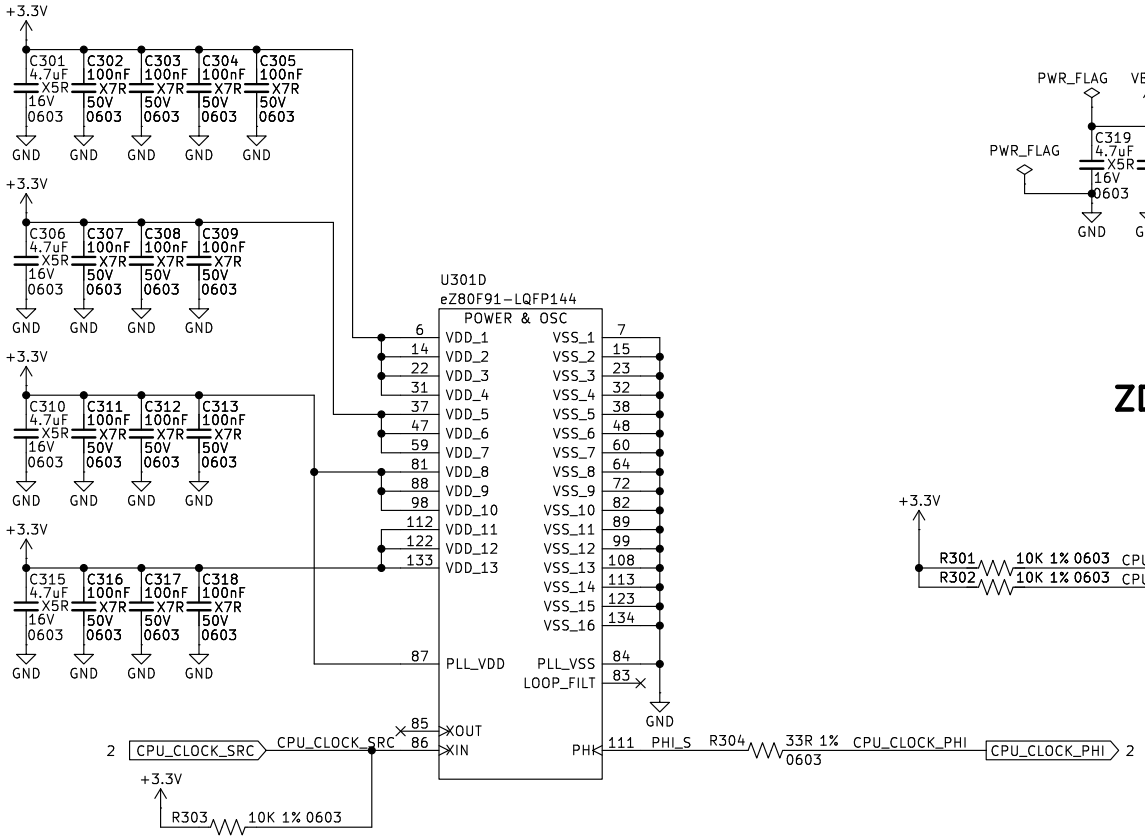
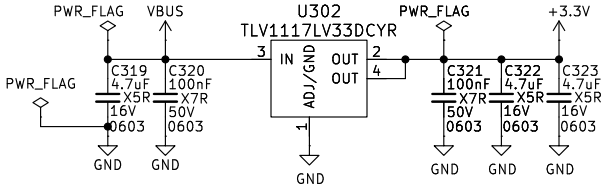
CPU Power & ZDI

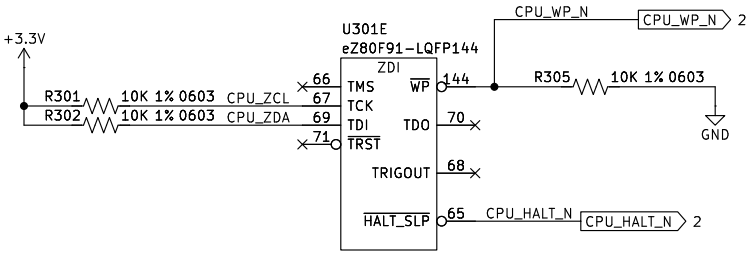


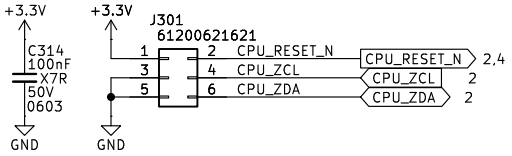
POWER SUPPLY



269-EZ80F91AZA50EK-ND

ZDI DEBUG INTERFACE





CPU Power & ZDI		
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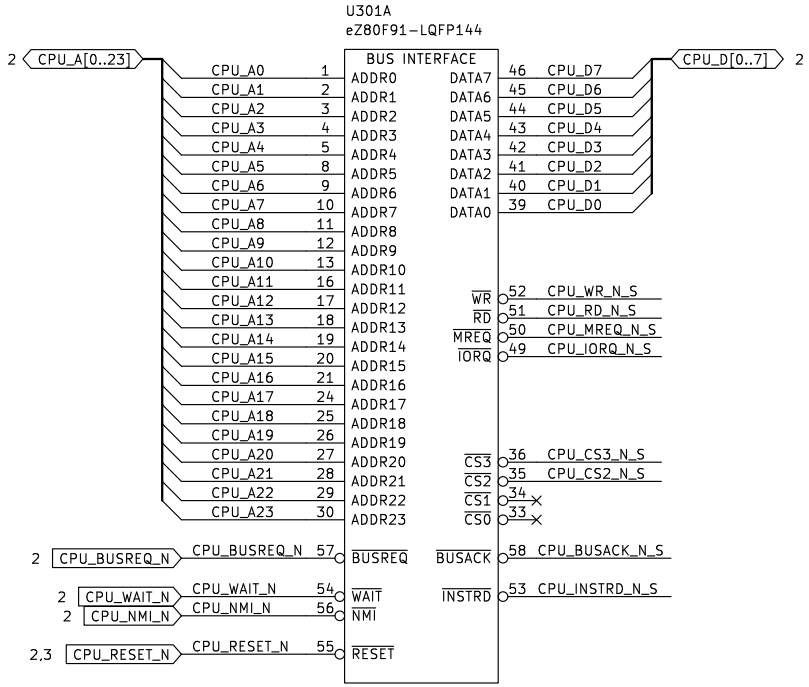
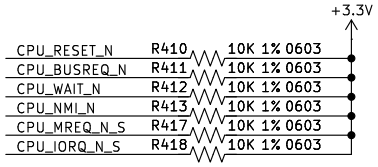
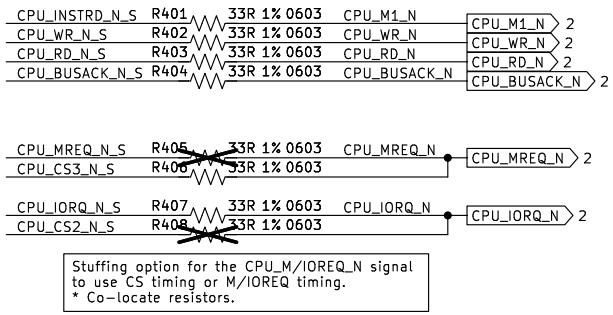
CPU Address & Data Bus



INPUT SIGNAL PULL-UPS



SERIES TERMINATORS



Stuffing option for the CPU_M/IOREQ_N signal
to use CS timing or M/IOREQ timing.
* Co-locate resistors.

CPU Address and Data Bus		
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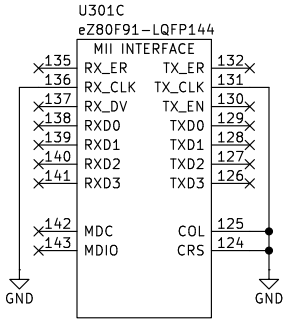
CPU Ethernet Interface



Sheet is a placeholder for future 10/100 Ethernet implementation.

CPU Ethernet Interface		
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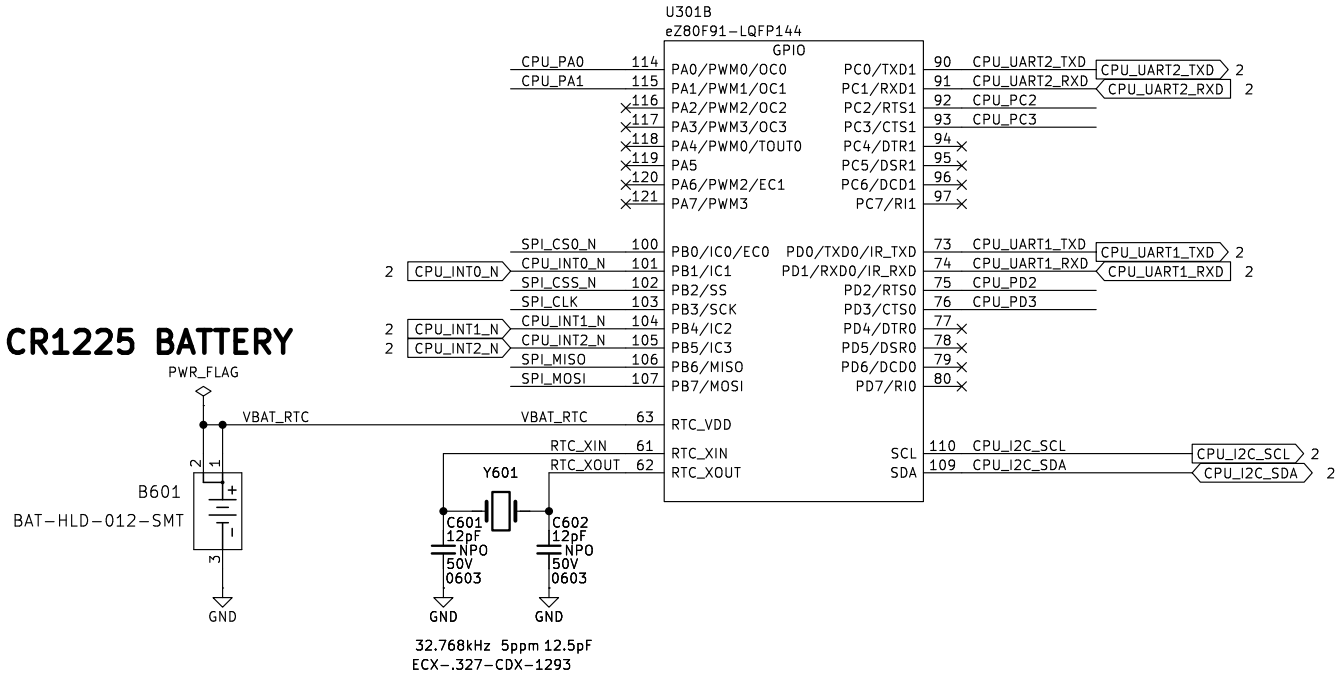
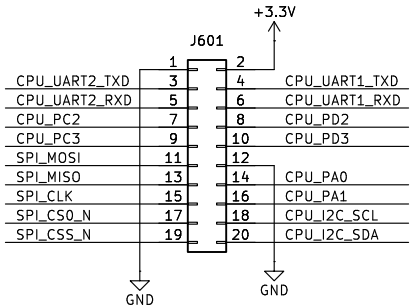
CPU GPIO RTC

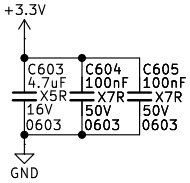


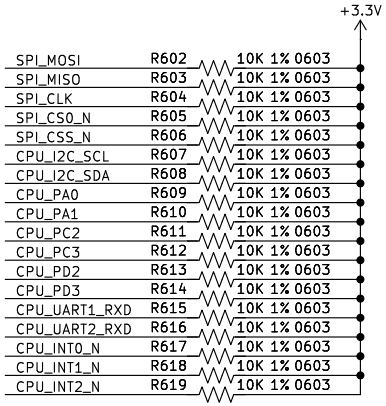
CR1225 BATTERY

32.768kHz 5ppm 12.5pF
ECX-.327-CDX-1293

TTL LEVEL CPU SIGNAL HEADER







CPU GPIO & Real Time Clock		
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