Family Name .....

Given Name .....

Student No. .....

Signature .....

# THE UNIVERSITY OF NEW SOUTH WALES

## School of Electrical Engineering & Telecommunications

## FINAL EXAMINATION

## SUMMER 2016 - 2017

## ELEC1111
## Electric Circuits

| | |
|---|---|
| **TIME ALLOWED:** | **3 hours** |
| **TOTAL MARKS:** | **100** |
| **TOTAL NUMBER OF QUESTIONS:** | **5** |

**THIS EXAM CONTRIBUTES 60% TO THE TOTAL COURSE ASSESSMENT**

Reading Time: 5 minutes.

This paper contains 6 pages.

Candidates must **ATTEMPT ALL** questions.

Answer each question in a **separate answer booklet**.

Marks for each question are indicated beside the question.

This paper **MAY NOT** be retained by the candidate.

Print your name, student ID and question number on the front page of each answer book.

Authorised examination materials:

Candidates should use their own UNSW-approved electronic calculators.

This is a closed book examination.

Assumptions made in answering the questions should be stated explicitly.

All answers must be written in ink. Except where they are expressly required, pencils **may only be used** for drawing, sketching or graphical work.

## QUESTION 1 [20 marks]

(i) Calculate the equivalent impedance of the circuit of Figure 1 as seen by :

a. **(4 marks)** a *dc* voltage source

b. **(6 marks)** an *ac* voltage source with a frequency of $\omega$ = 1 rad/sec

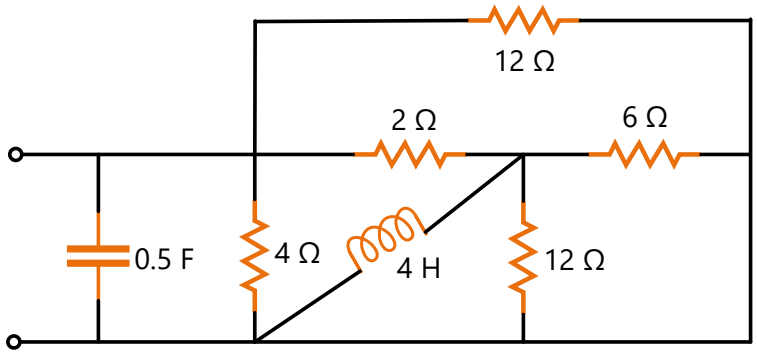


*Figure 1*

(ii) **(6 marks)** Find the Thevenin equivalent of the circuit in Figure 2.

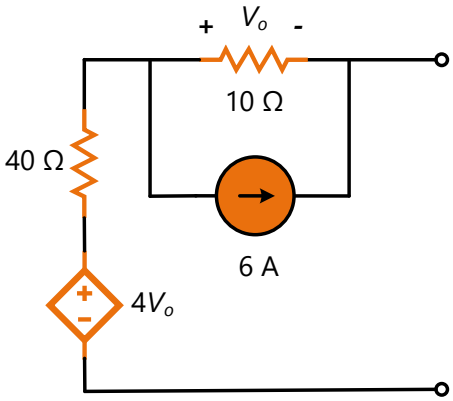


*Figure 2*

**(iii)** **(4 marks)** Calculate the power of the three sources in the circuit of Figure 3. Clearly explain if a source supplies or absorbs power.

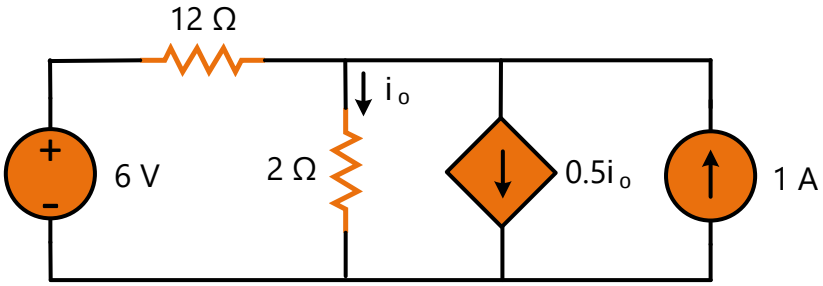


*Figure 3*

## QUESTION 2 [20 marks]

(i) **(6 marks)** Find the voltage across the 1 Ω resistor and the power dissipated in the 3 Ω resistor of the circuit in Figure 4.

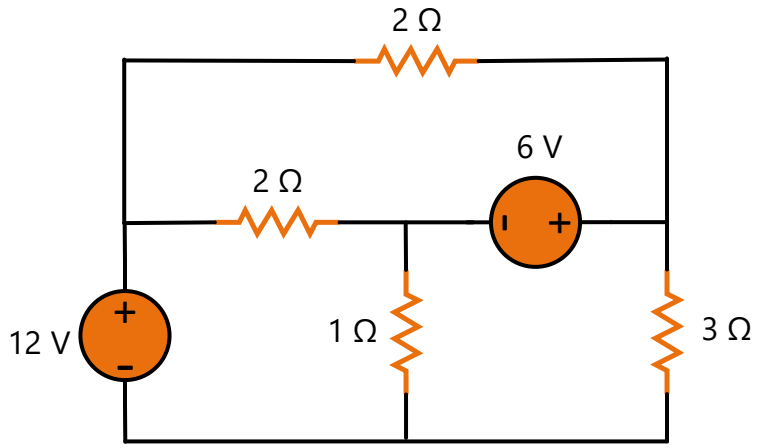


*Figure 4*

(ii) **(5 marks)** Find the voltage of node x ($V_x$) in the circuit of Figure 5.

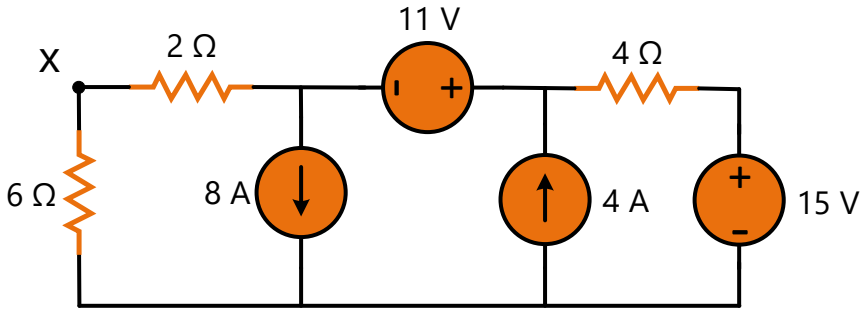


*Figure 5*

(iii) **(9 marks)** Find the current $i_o(t)$ in the circuit of Figure 6.

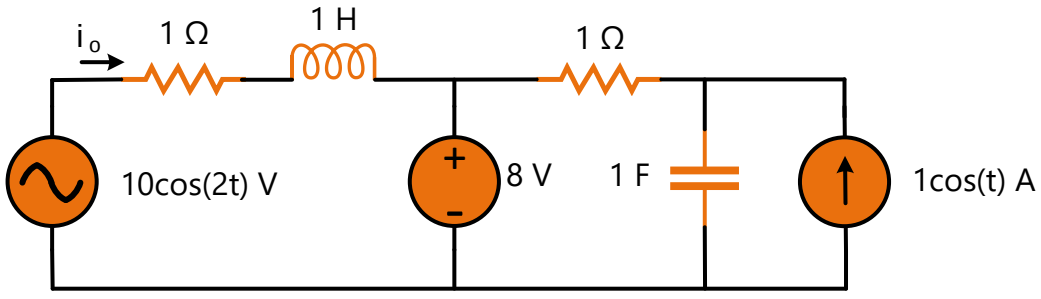


*Figure 6*

## QUESTION 3 [20 marks]

(i) **(8 marks)** In the circuit of Figure 7, the switch has been in the open position for a long time and closes at t = 0. Showing all working, derive an expression for the voltage of the capacitor $v_c(t)$ for t>0.

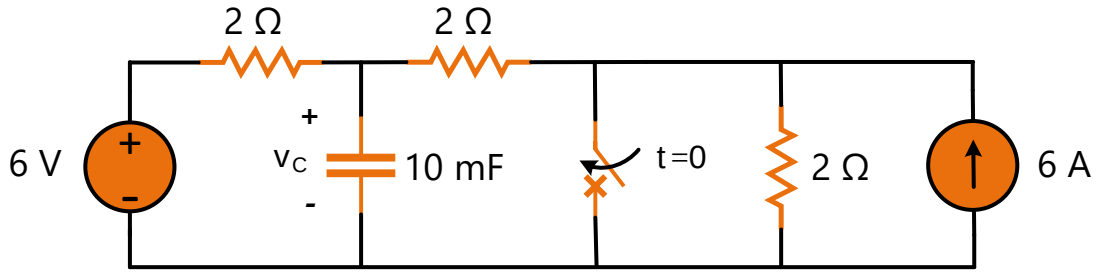


*Figure 7*

(ii) **(8 marks)** In the circuit of Figure 8, the switch has been in the closed position for a long time. The switch opens at t=0 and closes again at t=1sec. Showing all working, derive an expression for the current through the inductor $i_L(t)$ for t>0.

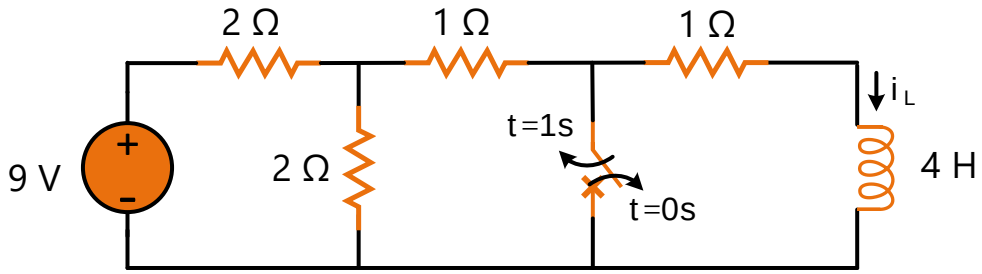


*Figure 8*

(iii) **(4 marks)** Find the element and the value of the element that must be connected parallel to nodes a-b of the circuit shown in Figure 9 so that the impedance $Z_{eq}$, seen from an ac voltage source with a frequency $\omega$ = 10 rad/sec is purely resistive.

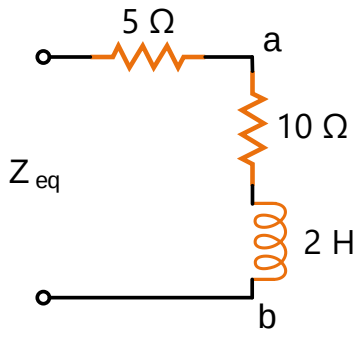


*Figure 9*

## QUESTION 4 [20 marks]

(i) **(5 marks)** Find $\mathbf{V_o}$ in the circuit of Figure 10 and draw phasors $\mathbf{V_o}$, $\mathbf{V_1}$, and $\mathbf{V_2}$ in the same phasor diagram.

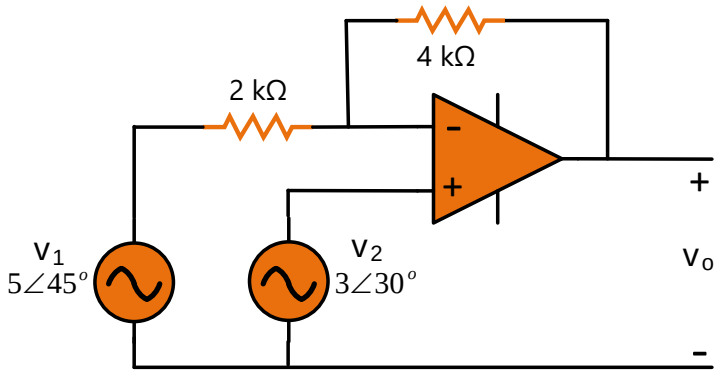


*Figure 10*

(ii) **(7 marks)** Consider the circuit of Figure 11. Find the current $\boldsymbol{I_o}$ and the voltages of the resistor $\boldsymbol{V_R}$, the capacitor $\boldsymbol{V_C}$ and the inductor $\boldsymbol{V_L}$. Plot them in the same phasor diagram, clearly indicating each phasor.

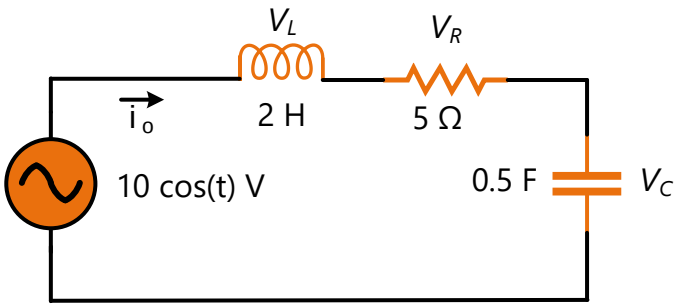


*Figure 11*

(iii) **(8 marks)** Two loads are connected in parallel and are supplied by a 230 $V_{rms}$, 50 Hz voltage source. **Load 1** consumes 10 kVA of power at a power factor of 0.8 leading (capacitive) while **load 2** consumes 5 kW at a power factor of 0.9 lagging (inductive). Calculate:

a. The total complex power of the two loads.
b. The total apparent power.
c. The combined power factor of the two loads, and
d. The rms value of the current supplied by the source.

## QUESTION 5 [20 marks]

(i) **(5 marks)** Design an operational amplifier circuit where $v_o(t) = -15\ v_s(t)$. Explain analytically your design process.

(ii) **(7 marks)** For the circuit shown in Figure 12, calculate the output voltage $\mathbf{V_o}$.

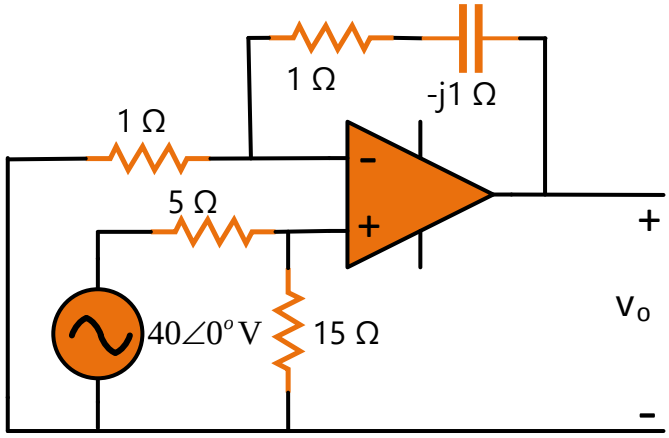


*Figure 12*

(iii) **(8 marks)** Consider the following logical diagram

a. Derive a logical expression for Z.
b. Write the truth table of the circuit.
c. Explain, also showing the required connections ad circuits, how a NAND Gate can be used to configure i) a NOT gate, ii) an AND gate and iii) an OR gate.

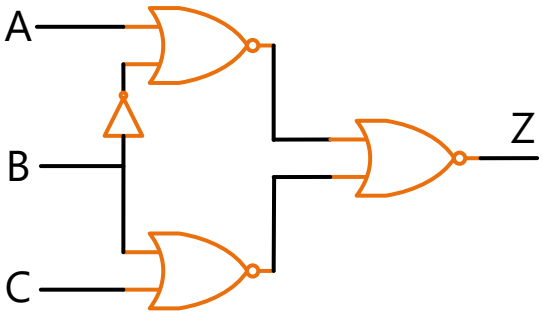


*Figure 13*

**END OF PAPER**