Name.....

Student Number.....

Signature.....

THE UNIVERSITY OF NEW SOUTH WALES

School of Electrical Engineering & Telecommunications

FINAL EXAMINATION

Session 2, 2016

ELEC1111
Electrical and Telecommunications Engineering

TIME ALLOWED:	**3 hours**
TOTAL MARKS:	**100**
TOTAL NUMBER OF QUESTIONS:	**5**

THIS EXAM CONTRIBUTES 60% TO THE TOTAL COURSE ASSESSMENT

Reading Time: 10 minutes.

This paper contains 5 pages.

Candidates must **ATTEMPT ALL** questions.

Answer each question in a **separate answer book**.

Marks for each question are indicated beside the question.

This paper may **NOT** be retained by the candidate.

Print your name, student ID and question number on the front page of each answer book.

Authorised examination materials:

Candidates should use their own UNSW-approved electronic calculators.

This is a closed book examination.

Assumptions made in answering the questions should be stated explicitly.

All answers must be written in ink. Except where they are expressly required, pencils **may only be used** for drawing, sketching or graphical work.

QUESTION 1 [25 marks]

(a) Consider the circuit shown in Figure 1 with $R_L=2\Omega$.

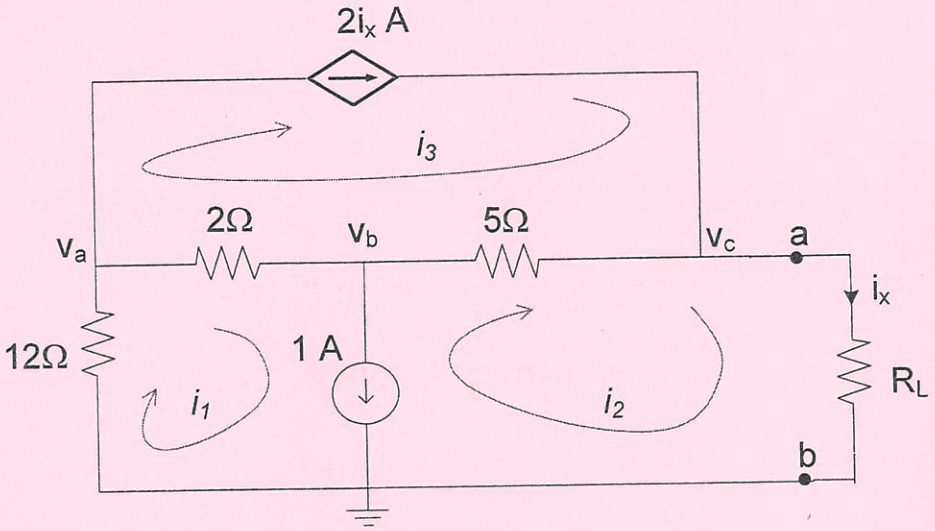


Figure 1

i) Write down three node equations for the node voltages v_a, v_b and v_c. **[4 marks]**
ii) Find the values of v_a, v_b and v_c. **[2 marks]**
iii) Write down three equations for the mesh currents i_1, i_2 and i_3. **[4 marks]**
iv) Find the values of i_1, i_2 and i_3. **[2 marks]**
v) Find the power supplied or absorbed by each element of the circuit and show that power is conserved in this circuit. **[2 marks]**

(b) For the circuit in Figure 1, find the resistance of the resistor R_L such that the power dissipating on it is maximized. Calculate the maximum power. *Hint*: *This can be answered by finding the Thevenin equivalent of the circuit to the left of terminals a-b.* **[2 marks]**

(c) Using superposition principle, find the voltage V_o in the circuit in Figure 2. **[6 marks]**

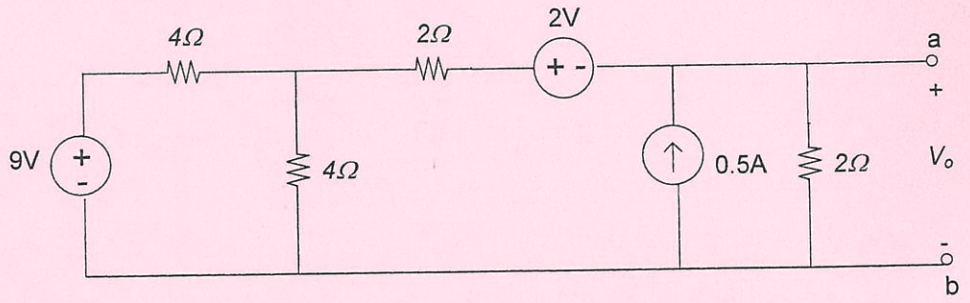
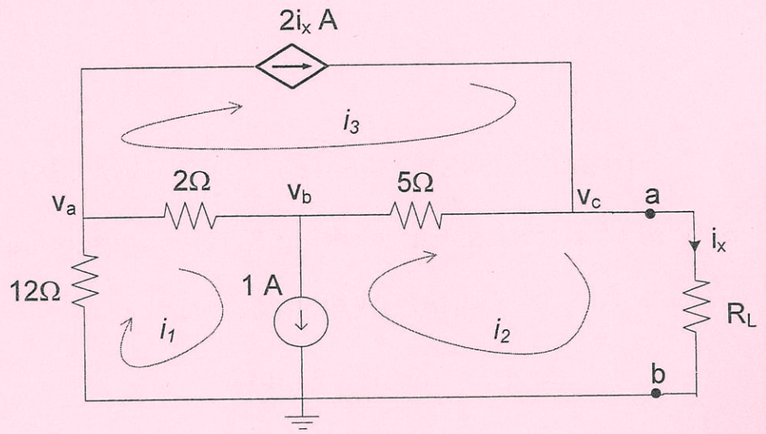


Figure 2

(d) For the circuit in Figure 2, determine the values for the Thevenin equivalent of the circuit to the left of the terminal pair *a-b*. **[3 marks]**

QUESTION 1 [25 marks]

(a) Consider the circuit shown in Figure 1 with R_L=2Ω.



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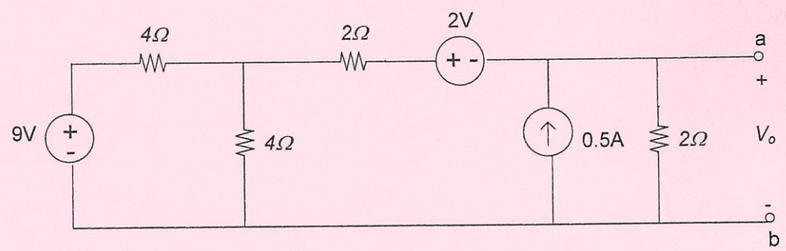

Figure 2

(d) For the circuit in Figure 2, determine the values for the Thevenin equivalent of the circuit to the left of the terminal pair *a-b*. **[3 marks]**

QUESTION 2 [15 marks]

Consider the circuit shown in Figure 3. Assume that the switch has been opened for a long time and is closed at $t = 0$. The switch then remains closed for 1 second and opens again.

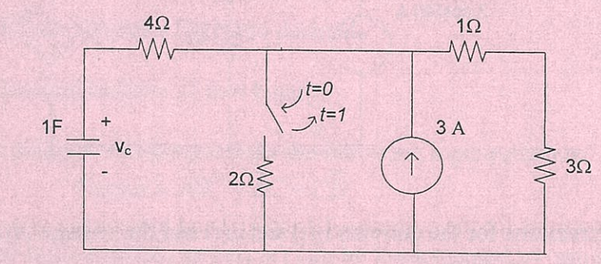

Figure 3

Determine:

(a) The initial value of the voltage across capacitor, i.e. $v_c(0^+)$ **[2 marks]**
(b) An expression for the voltage $v_c(t)$ when $0 \le t \le 1$. **[5 marks]**
(c) An expression for the voltage $v_c(t)$ when $t \ge 1$. **[4 marks]**
(d) The steady state voltage when $t > 1$, i.e. $v_c(+\infty)$. **[2 marks]**
(e) The energy stored in the capacitor at time t = 5 seconds. **[2 marks]**

QUESTION 3 [25 marks]

(a) Consider the circuit shown in Figure 4 where L = 0.1H, $C = 2\text{x}10^3 \mu$F, R = 6Ω and the angular frequency is ω=100rad/s.

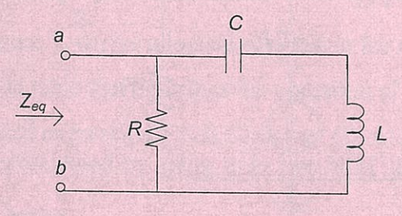

Figure 4

i. Write down an expression for the impedance Z_{eq} between terminals *a-b* in terms of R, C, L and ω. **[4 marks]**
ii. Calculate Z_{eq}. **[2 marks]**
iii. A voltage source $v_s(t)=240\sin(100t)$ V is supplied to the terminals *a-b* of the circuit. Find an expression for the current supplied by the source in time domain. **[2 marks]**
iv. Find the phase difference between the voltage $v_s(t)$ and current in part (iii). Is the voltage leading or lagging compared to the current? **[2 marks]**
v. In order to make the circuit have a unity power factor, a capacitor C_x is connected in parallel with the resistor. Find the capacitance of C_x. **[2 marks]**

(b) Consider the circuit in Figure 5.

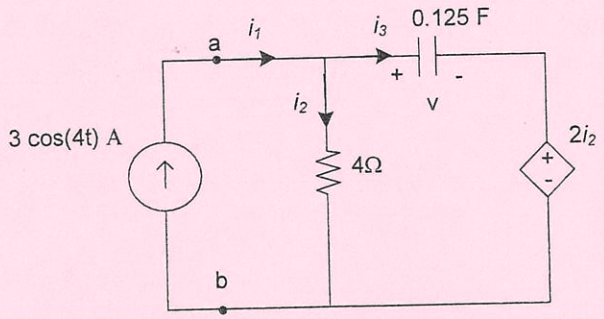

Figure 5

i) Find expressions for the currents $i_2(t)$ and $i_3(t)$ and the voltage v(t). **[7 marks]**

ii) Sketch a phasor diagram showing all currents and voltages in the circuit. **[3 marks]**

iii) Calculate the power factor of the circuit to the right of the terminal pair *a-b*. **[3 marks]**

QUESTION 4 [15 marks]

Consider the circuit in Figure 6 with $v_1=v_2=1V$; $R_1=R_2=20k\Omega$; $R_3=R_4=10k\Omega$ and $R_5=100k\Omega$.

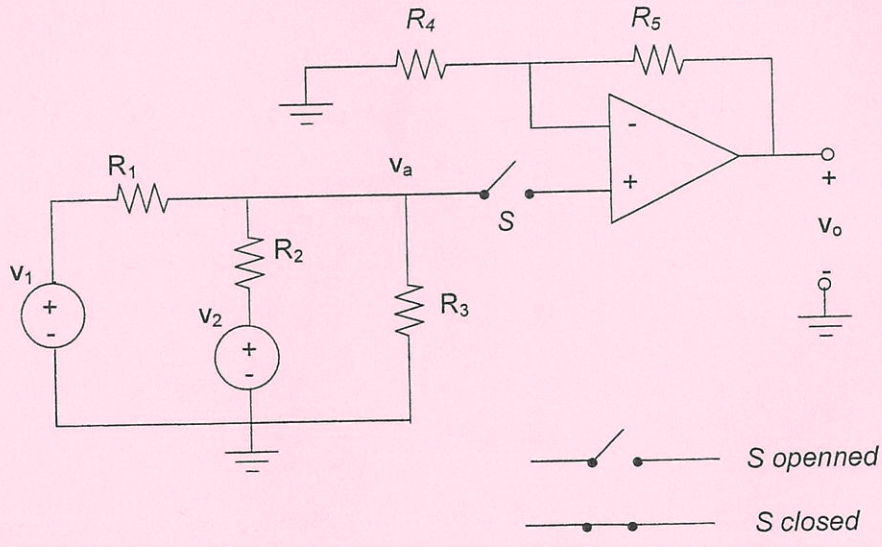

Figure 6

a. When the switch S is opened, find the voltage v_a. **[5 marks]**

b. When the switch S is closed:

i. Determine the ratio v_o/v_a. **[5 marks]**

ii. Find the output voltage v_o. **[2 marks]**

iii. Justify that the circuit is a non-inverting amplifier circuit based on your answer in part (i). **[3 marks]**

QUESTION 5 [20 Marks]

(a) Convert the binary number *11001* into decimal. **[2 marks]**

(b) Convert the decimal number *35* into binary. **[2 marks]**

(c) Draw a logic diagram which represents the following logic equation:

$$Output = \overline{A}BC + \overline{B}C + C\overline{D}$$ **[4 marks]**

(d) Show that the logic equation in part (c) can be implemented by using only NAND gates and sketch the logic diagram of the equation using only NAND gates. **[2 marks]**

(e) Consider the logic diagram shown in Fig. 7.

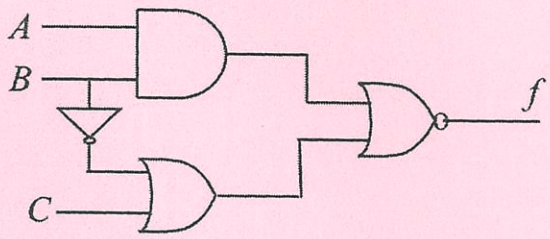

Figure 7

i. Directly from Figure 7, derive a logical expression for f(A,B,C). **[5 marks]**

ii. Write down a truth table that describes the operation of this diagram. **[3 marks]**

iii. Simplify the logical expression f(A,B,C) in part (i) as much as possible and show that it can be implemented by using only two NOT gates and one 3-input AND gate. **[2 marks]**

END OF PAPER