Family Name .....

Given Name .....

Student No. .....

Signature .....

THE UNIVERSITY OF NEW SOUTH WALES

School of Electrical Engineering & Telecommunications

FINAL EXAMINATION

Session 1, 2016

ELEC1111
Electrical and Telecommunications Engineering

TIME ALLOWED: **3 hours**
TOTAL MARKS: **100**
TOTAL NUMBER OF QUESTIONS: **5**

THIS EXAM CONTRIBUTES 60% TO THE TOTAL COURSE ASSESSMENT

Reading Time: 10 minutes.

This paper contains 7 pages.

Candidates must **ATTEMPT ALL** questions.

Answer each question in a **separate answer book**.

Marks for each question are indicated beside the question.

This paper **MAY** be retained by the candidate.

Print your name, student ID and question number on the front page of each answer book.

Authorised examination materials:

Candidates should use their own UNSW-approved electronic calculators.

This is a closed book examination.

Assumptions made in answering the questions should be stated explicitly.

All answers must be written in ink. Except where they are expressly required, pencils **may only be used** for drawing, sketching or graphical work.

QUESTION 1 [20 marks]

(a) **(10 marks)** Consider the circuit in Figure 1.

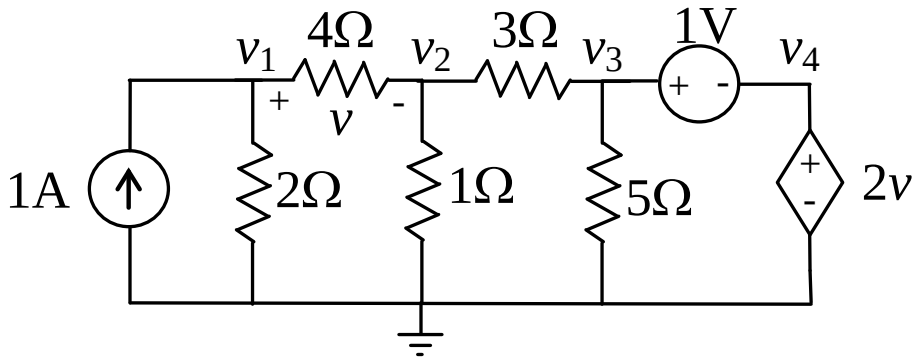

Figure 1

i) Showing all working, identify all the nodes in the circuit, analyse the circuit to write down the node equations. (6 marks)

ii) Showing all working, solve the node equations. (4 marks)

(b) **(10 marks)** Consider the circuit shown in Figure 2.

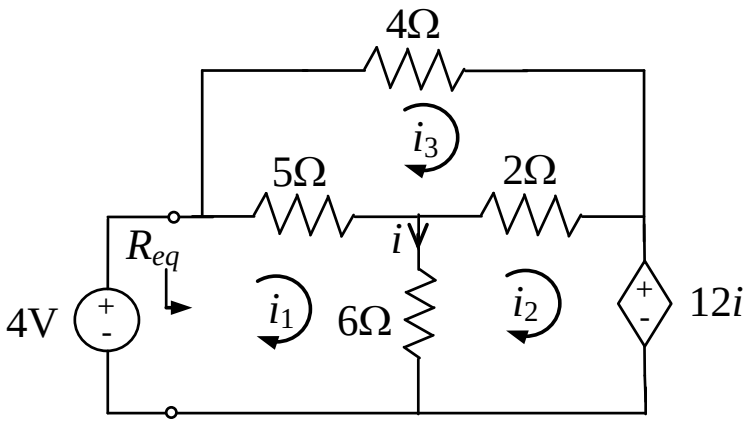

Figure 2

i) Showing all working, write down the mesh equations and find the mesh currents i_1, i_2, and i_3. (8 marks)

ii) Showing all working, find the equivalent resistance R_{eq} seen by the 4V independent voltage source. (2 marks)

QUESTION 2 [20 marks]

Consider the circuit shown in Fig. 3, and assume that the switch has been closed for a long time and is opened at $t = 0$.

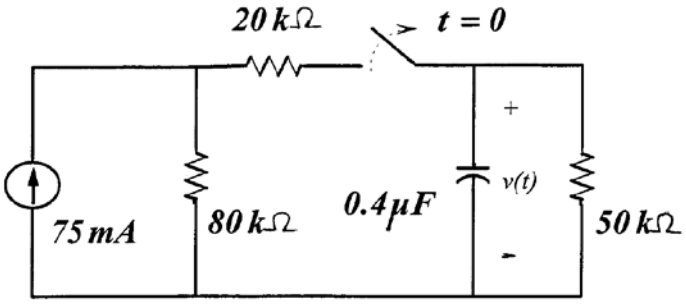

Figure 3

Determine:

(a) **(4 marks)** The Thévenin equivalent for the part of the circuit to the left of the capacitor.
(b) **(4 marks)** The initial value of the voltage $v(t)$.
(c) **(2 marks)** The time constant for $t > 0$.
(d) **(4 marks)** An expression for the voltage $v(t)$ after the switch has been opened.
(e) **(3 marks)** An expression for the discharging current $i(t)$ after the switch has been opened.
(f) **(3 marks)** The initial energy stored in the capacitor.

QUESTION 3 [20 marks]

(a) **(10 marks)** Consider the circuit in Fig. 4.

i) Find all voltages and currents in the circuit.

ii) Sketch all voltages and currents on a phasor diagram.

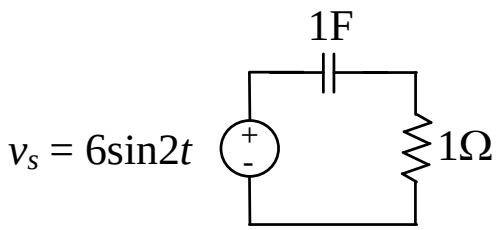

Figure 4

(b) **(6 marks)** Consider the circuit in Fig. 5. Find $v(t)$ using phasors.

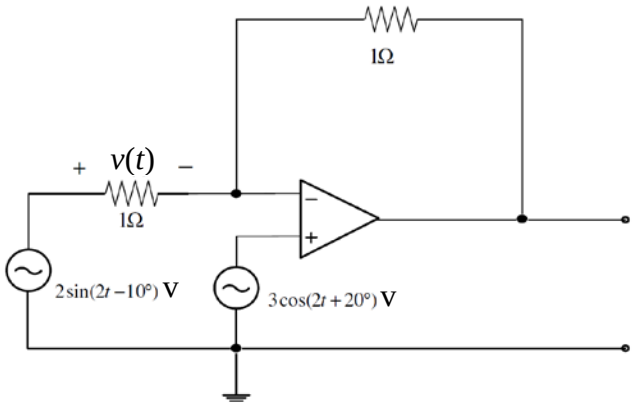

Figure 5

(c) **(4 marks)** Consider the circuit shown in Fig. 6, where L = 27 mH, C = 22 μF and R = 6Ω. Find the angular frequency ω for which the impedance Z_{eq} between terminals a-b is purely resistive.

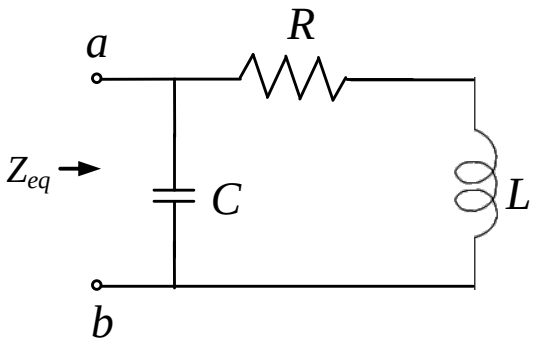

Figure 6

QUESTION 4 [20 marks]

(a) **(7 marks)** Consider the circuit below in Figure 7, where switch S_1 has been closed for a long time and switch S_2 has been open for a long time. At $t = 0$, switch S_1 opens and switch S_2 closes. ***Derive*** an expression for the inductor current $i_L(t)$ for $t > 0$.

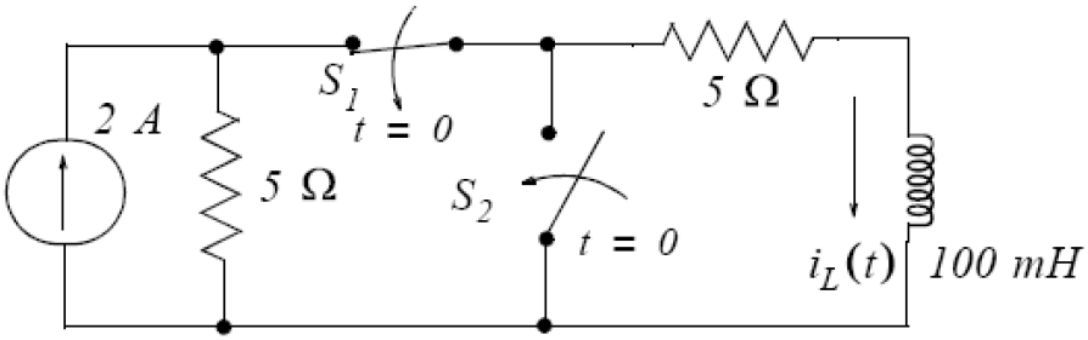

Figure 7

(b) **(7 marks)** Sketch, showing all necessary details, a diagram of a circuit containing an op-amp that is capable of realizing the function $v_{out}(t) = 5v_{in}(t)$, where is the $v_{in}(t)$ input voltage and is $v_{out}(t)$ the output voltage. Explain why negative feedback is desirable.

(c) **(6 marks)** For the circuit shown in Figure 8, determine the values for the Norton equivalent of the circuit to the left of the terminal pair *a-b*.

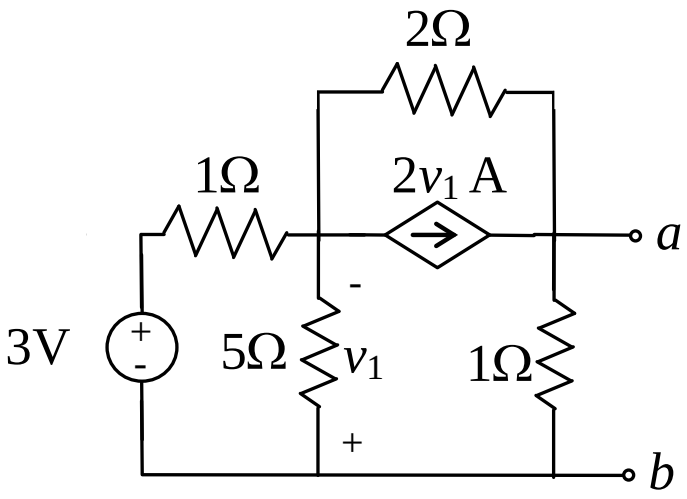

Figure 8

QUESTION 5 [20 Marks]

Consider the circuit in Fig. 9.

(a) **(5 marks)** Determine the voltage V and current I.

(b) **(5 marks)** Determine the power absorbed or supplied by each of the three current sources. For each element, you should specify whether the power is absorbed or supplied.

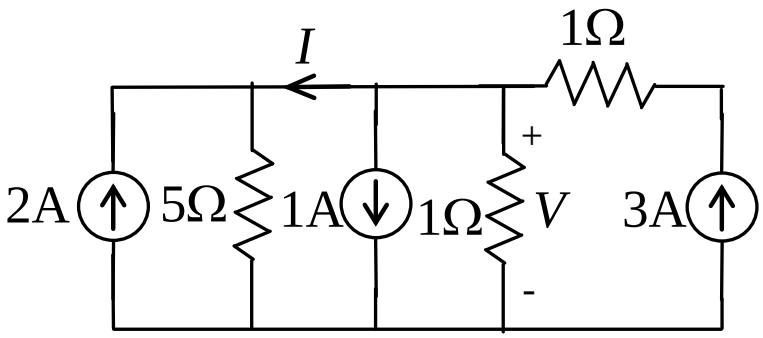

Figure 9

Consider the logic diagram shown in Fig. 10.

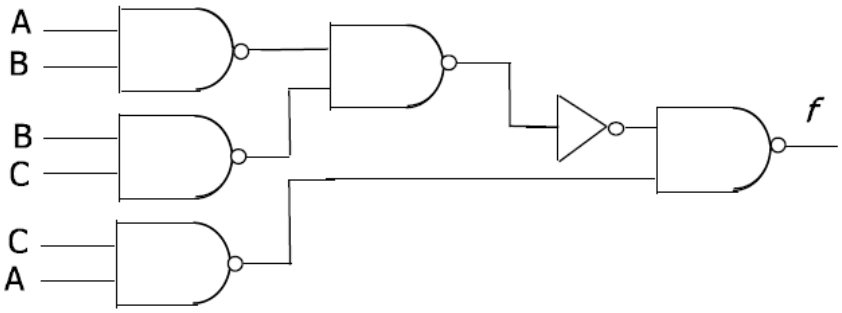

Figure 10

(c) **(4 marks)** Directly from Fig. 9, derive the logical expression f(A,B,C), and simplify it as much as possible, explaining which theorems have been used at each step of your working.

(d) **(3 marks)** Construct the logical truth table relating f to inputs A, B and C.

(e) **(3 marks)** Using part (a) and/or part (b), show that f can be realised using exactly three 2-input AND gates and two 2-input OR gates, and sketch the logic diagram.

END OF PAPER