Family Name .....

Given Name .....

Student No. .....

Signature .....

THE UNIVERSITY OF NEW SOUTH WALES

School of Electrical Engineering & Telecommunications

FINAL EXAMINATION

Session 2, 2015

ELEC1111
Electrical and Telecommunications Engineering

TIME ALLOWED:	**3 hours**
TOTAL MARKS:	**100**
TOTAL NUMBER OF QUESTIONS:	**5**

THIS EXAM CONTRIBUTES 60% TO THE TOTAL COURSE ASSESSMENT

Reading Time: 10 minutes.

This paper contains 7 pages.

Candidates must **ATTEMPT ALL** questions.

Answer each question in a **separate answer book**.

Marks for each question are indicated beside the question.

This paper **MAY NOT** be retained by the candidate.

Print your name, student ID and question number on the front page of each answer book.

Authorised examination materials:

Candidates should use their own UNSW-approved electronic calculators.

This is a closed book examination.

Assumptions made in answering the questions should be stated explicitly.

All answers must be written in ink. Except where they are expressly required, pencils **may only be used** for drawing, sketching or graphical work.

QUESTION 1 [20 marks]

(i) **[6 marks]** Find the equivalent capacitance at terminals *a*-*b* of the circuit in Figure 1. All capacitances are in μF.

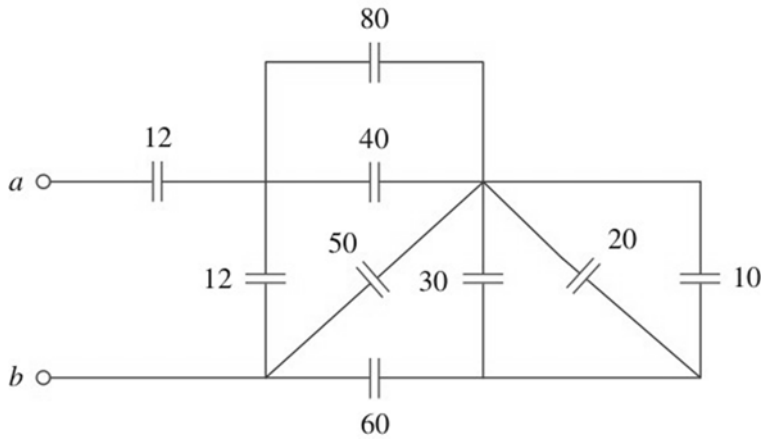

Figure 1

(ii) **[7 marks]** For the circuit shown in Figure 2:

a. Find the indicated currents I_1, I_2 and I_3.

b. Find the voltage V_{ab}.

c. Find the total power dissipated by the resistors.

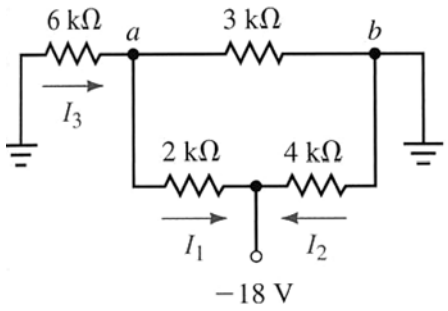

Figure 2

(iii) **[7 marks]** For the circuit shown in Figure 3, use nodal analysis to find the nodal voltages V_a and V_b.

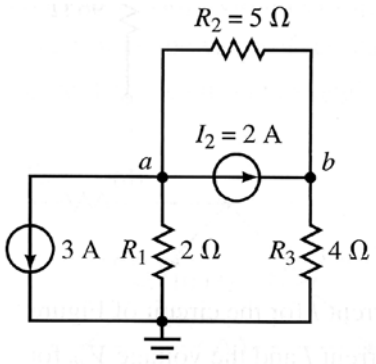

Figure 3

QUESTION 2 [20 marks]

(i) **[6 marks]** For the circuit shown in Figure 4, use mesh analysis to calculate the current I_1.

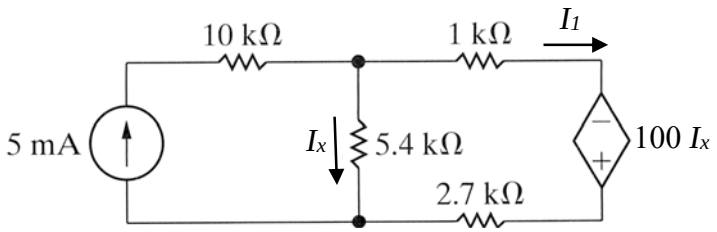

Figure 4

(ii) **[8 marks]** For the circuit shown in Figure 5 use the principle of superposition to find the voltage v_x .

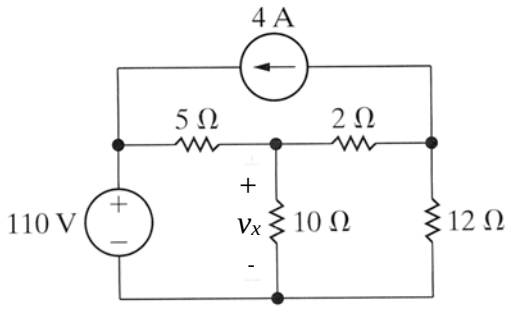

Figure 5

(iii) **[6 marks]** Find and draw the Thevenin equivalent circuit with respect to the terminals A-B for the circuit in Figure 6.

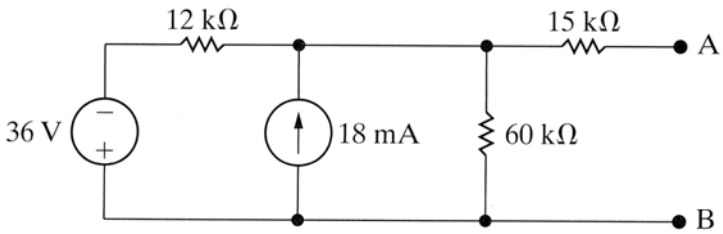

Figure 6

QUESTION 3 [20 marks]

(i) **[4 marks]** For the circuit shown in Figure 7:

a. Determine the current I_C after the circuit has reached steady state.

b. Determine the capacitor voltages V_{C1}, V_{C2} and V_{C3} after the circuit has reached steady state.

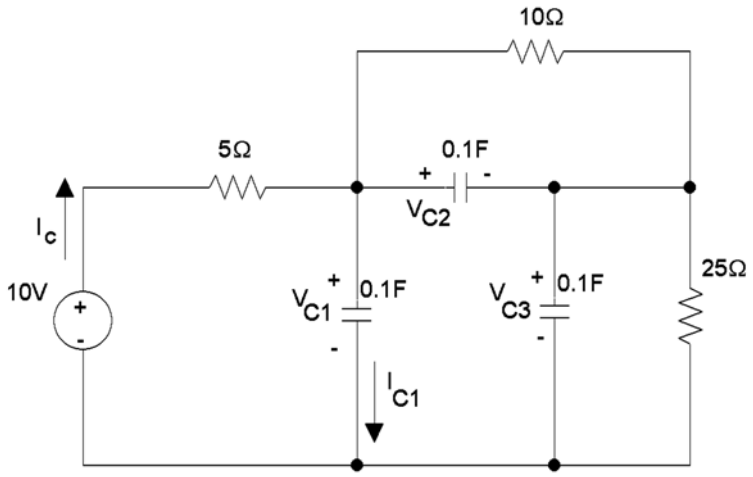

Figure 7

(ii) **[6 marks]** Refer to the circuit shown in Figure 8. The switch has been closed for a long time before opening at time $t=0$. Calculate the values $i_R(0^+)$, $i_L(0^+)$ and $i_C(0^+)$, immediately after the switch opens. Calculate the values $i_R(\infty)$, $i_L(\infty)$ and $i_C(\infty)$, after the switch has been open for a long time.

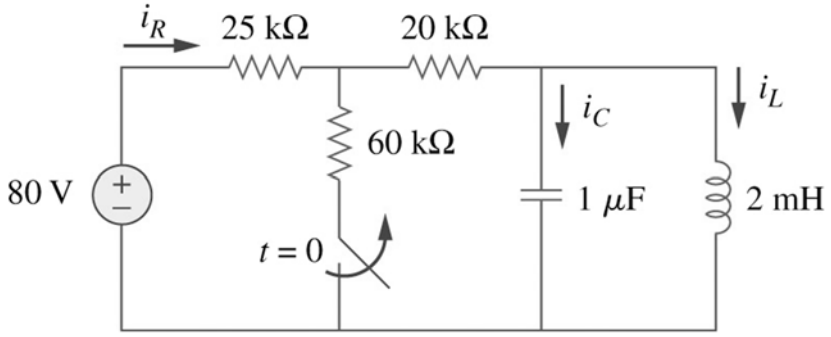

Figure 8

QUESTION 3 CONTINUES ON NEXT PAGE

(iii) **[10 marks]** In the circuit shown in Figure 9, switch S_1 is closed at $t=0$ and switch S_2 is closed at $t=4$. Find the current $i(t)$ for $t>0$.

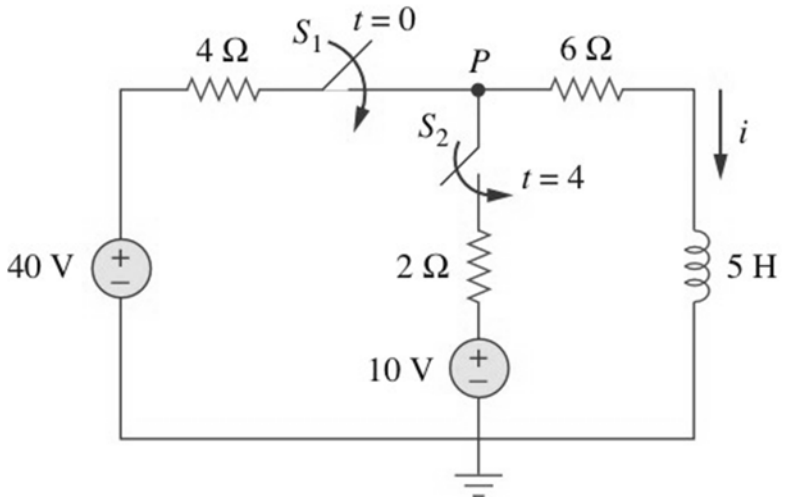

Figure 9

QUESTION 4 [20 marks]

(i) **[10 marks]** Determine v_0 in the circuit shown in Figure 10:

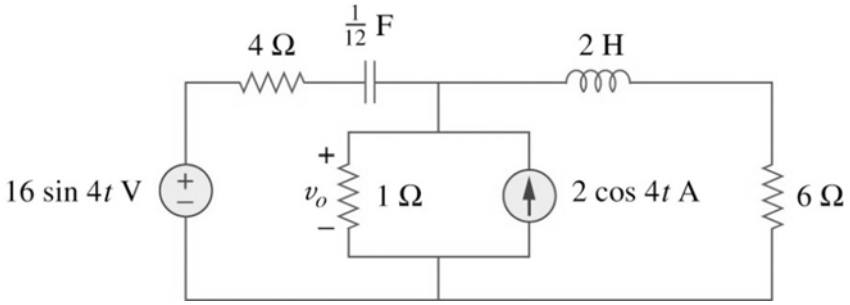

Figure 10

(ii) **[5 marks]** Find the input admittance, $\mathbf{Y}_{in}$, of the circuit shown in Figure 11 at $\omega = 100\text{rad/s}$. Express answer in polar form.

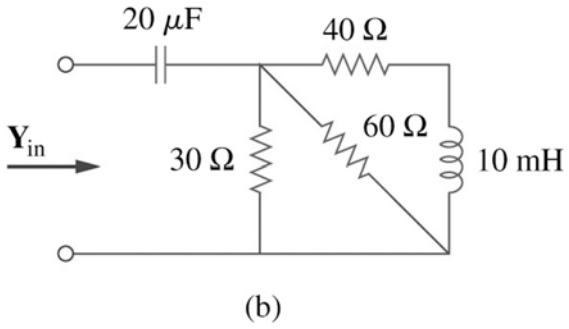

Figure 11

(iii) **[5 marks]** For Figure 12, $i_1 = 100\sin(50t + 100°)$ A and $i_T = 50\sin(50t - 40°)$ A. Determine phasors $\mathbf{I}_1$, $\mathbf{I}_2$ and $\mathbf{I}_T$ and draw the phasor diagram showing $\mathbf{I}_1$, $\mathbf{I}_2$ and $\mathbf{I}_T$.

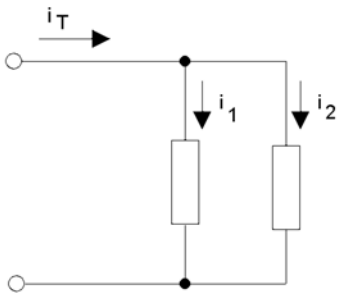

Figure 12

QUESTION 5 [20 marks]

(i) **[8 marks]** Calculate the voltage v_0 after the op amp circuit of Figure 13 has reached steady state.

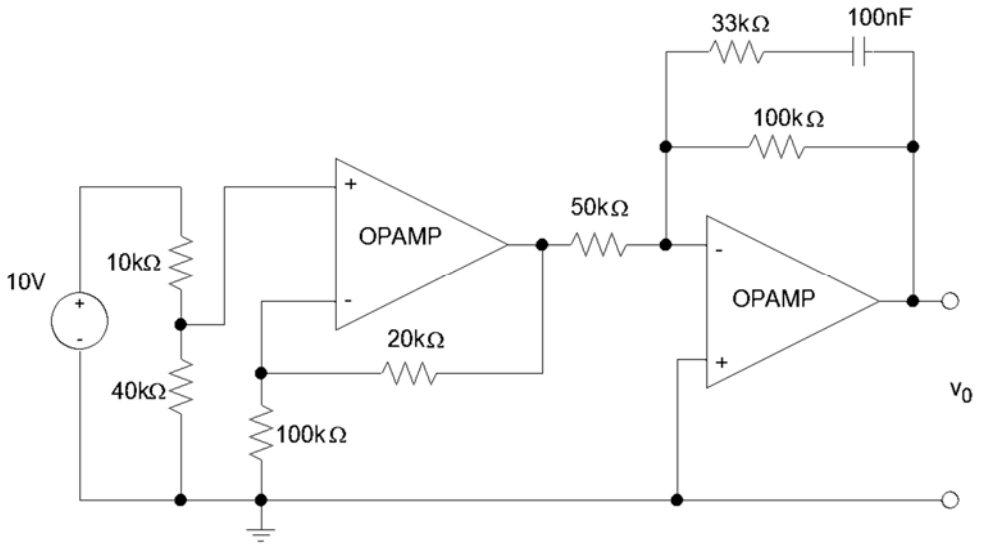

Figure 13

(ii) **[6 marks]** Draw the logic diagram which represents the function of this logic equation:

$$Output = \overline{A}.B.D + B.\overline{C} + \overline{D}$$

(iii) **[6 marks]** For the logic circuit shown in Figure 14, draw up a truth table that describes the operation of this circuit.

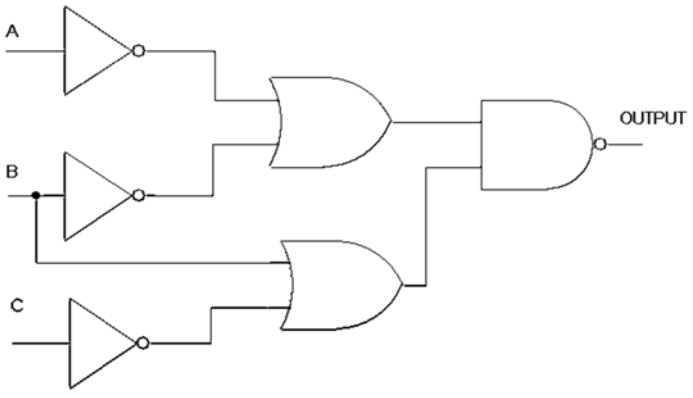

Figure 14

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