The University of New South Wales

School of Electrical Engineering and Telecommunications

ELEC2141: Digital Circuit Design

Final Examination

Session 1, 2009

- Time allowed: 3 hours.
- This paper contains this page and SIX (6) Questions on 6 other pages.
- Total marks available: 100.
- All questions are of equal value. Part marks are as indicated.
- **Answer 5 questions only.**
- Answer EACH question in a SEPARATE book.
- The exam paper may be retained by the candidate.
- Authorized examination materials: University approved calculators.
- Any assumptions found to be necessary in answering the questions should be stated explicitly.
- All answers must be written in ink. Except where they are expressly required, pencils may be used only for drawing, sketching or graphical work.

Question 1. (20 marks)

i) Consider the Boolean function:

$$F(A,B,C,D) = (A+B)(A+C+D) + (\bar{A}+B)(B+C+\bar{D})A$$

a) Find the truth table representation for *F*. **[3 marks]**

b) Express the function *F* as a Sum-of-Minterms (you may use the "little *m*" short-cut notation). **[1 mark]**

c) Express the function *F* as a Product-of-Maxterms (you may use the "big *M*" short-cut notation). **[1 mark]**

d) Use a Karnaugh map to find minimal Sum-of-Products expression for *F*. **[1 mark]**

e) Use a Karnaugh map to find minimal Product-of-Sums expression for *F*. **[2 marks]**

f) Find the gate-input cost (inverters included) of the function *F*, assuming the implementation follows the given expression for *F* exactly. **[2 marks]**

ii)

a) Using Boolean algebra, prove the identity: **[3 marks]**

$$X + Y = X \oplus Y + XY$$

b) Therefore, or otherwise, find an expression for the function

$$G(A,B,C) = A\bar{B} + AB\bar{C} + \bar{A}B$$

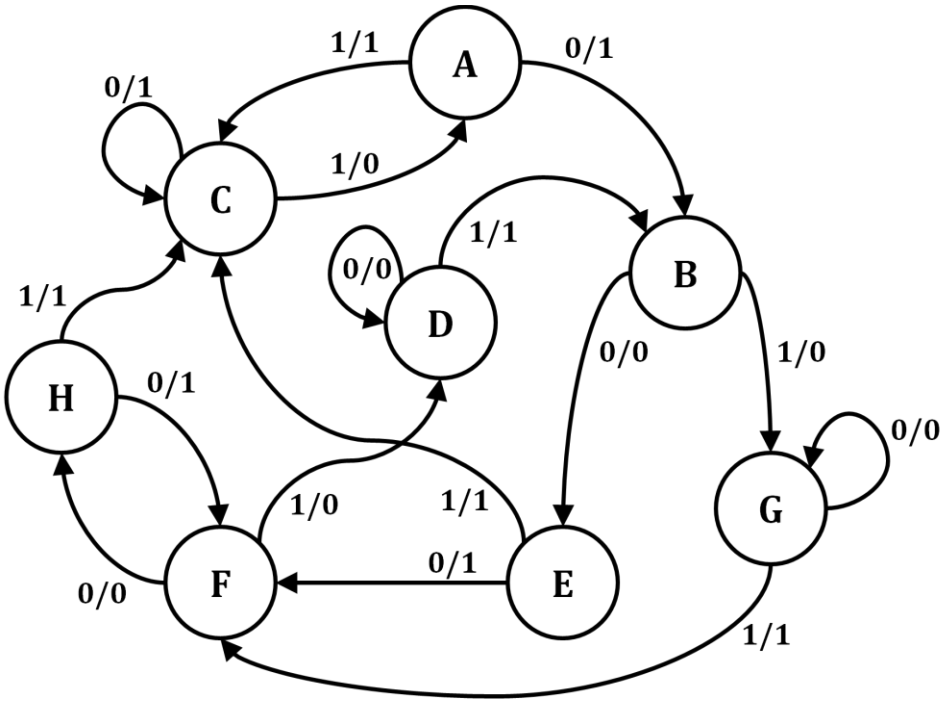
which uses only XOR and AND gates. **[4 marks]**

c) Draw the logic diagram (circuit) for the expression found in part (b). Assume the signals *A*, *B*, and *C* are available, as well as the power rails (V_{DD} and GND). You may only use 2-input XOR and 2-input AND gates. **[3 marks]**

Please turn over - Question 2 on next page.

Question 2. (20 marks)

Consider the following Mealy state machine, with one input *X* and one output *Z*, defined by the state diagram:



i) Write the state transition table for the Mealy machine. **[3 marks]**

ii) Minimize the number of states and derive the reduced state transition table (Hint: this can be done using four states). **[5 marks]**

iii) Convert the reduced Mealy machine to an equivalent Moore machine. Describe the Moore machine using a state transition table. **[5 marks]**

The Moore machine is to be implemented using D flip-flops and additional logic.

iv) Choose and list binary code assignments for the states. **[1 mark]**

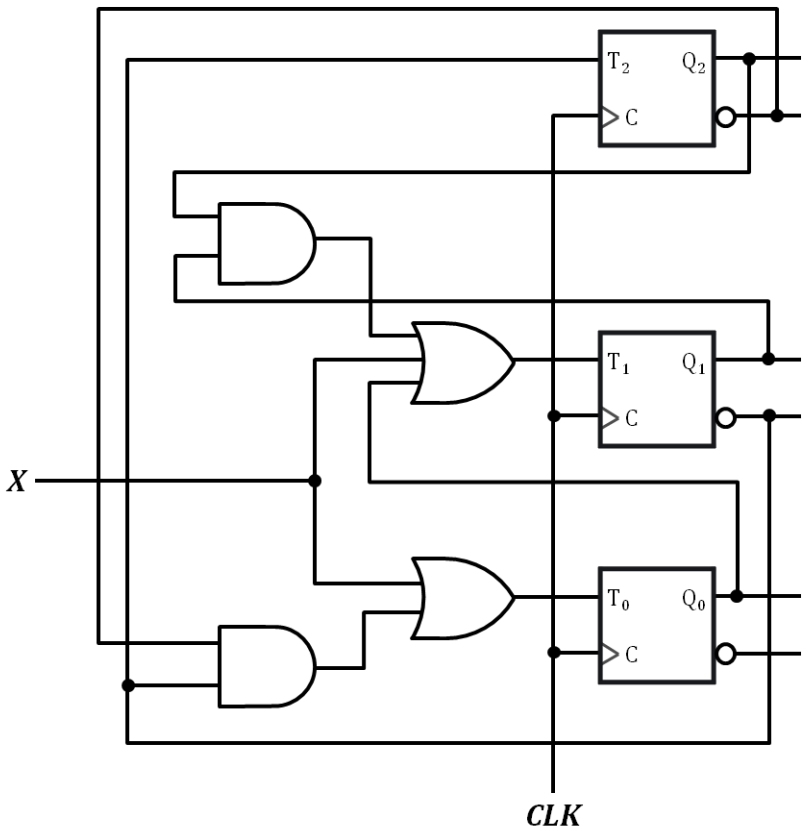
v) Derive the flip-flop and output equations. **[3 marks]**

vi) Draw the logic diagram that implements the machine. **[3 marks]**

Please turn over - Question 3 on next page.

Question 3. (20 marks)

Consider the following T flip-flop based synchronous sequential circuit, with one input *X*:



i) Write the three flip-flop equations. **[3 marks]**

ii) Derive the state transition table. **[10 marks]**

iii) With the states labeled as:

State	$Q_2Q_1Q_0$	State	$Q_2Q_1Q_0$
S	000	A	100
T	001	W	101
E	010	-	110
R	011	!	111

draw the state diagram (note that the last two characters are the actual state names).
[4 marks]

iv) With initial state S, and input sequence 01010001 on *X*, find the sequence of (labeled) states traversed. **[3 marks]**

Please turn over - Question 4 on next page.

Question 4. (20 marks)

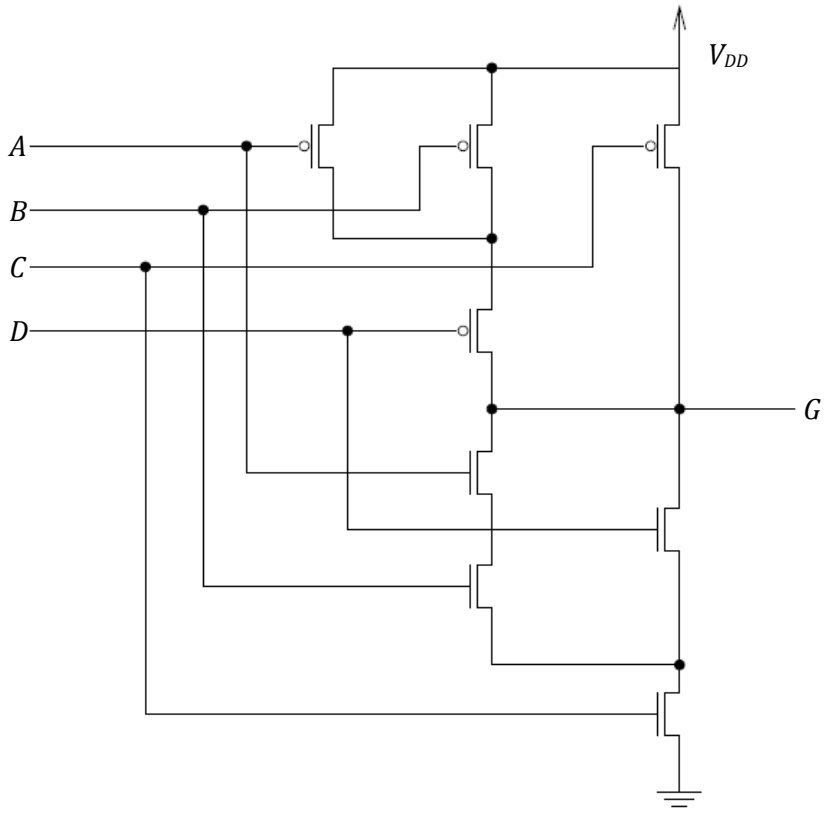
i) Convert the decimal number 27.40625 to binary. **[5 marks]**

ii) Consider the function:

$$F = X + \bar{X}\bar{Y} + \bar{Y}\bar{Z}$$

Construct a CMOS complex gate which gives the same truth table as that of the Boolean function *F*. Hint: simplification of the function is allowed. **[8 marks]**

iii) Find the truth table for the following CMOS circuit: **[7 marks]**



Question 5. (20 marks)

i) Given a D flip-flop and any number of logic gates, construct a JK flip-flop (draw the logic diagram). **[6 marks]**

ii) Consider the following Verilog program:

```
module fbc (CLK, RESET, EN, Q, CO);
      input CLK, RESET, EN;
      output [3:0] Q;
      output CO;

      reg [3:0] Q;

      assign CO = Q[3] & Q[2] & Q[1] & Q[0];

      always @(posedge RESET) begin
            Q <= 4'b0000;
      end

      always @(posedge CLK) begin
            if (EN) Q <= Q + 1;
      end
endmodule
```

a) Draw the block symbol that represents the module. **[3 marks]**

b) In one sentence, describe the overall function of this module. **[2 marks]**

c) Give a brief description for each of the inputs and outputs, and how they are being used. **[5 marks]**

d) By cascading two block symbols together, the function of this module can be expanded to double the amount of outputs. With the aid of a block diagram, show how you would connect two such modules to form correct expanded functionality. **[4 marks]**

Please turn over - Question 6 on next page.

Question 6. (20 marks)

i) A negative edge-triggered D flip-flop with asynchronous set and reset signals is to be implemented in Verilog. The flip-flop should sample the input *D* at every falling edge of the *CLK* signal, store the value and output it on *Q* until the following falling edge of the clock. The flip-flop also has asynchronous *S* (set) and *R* (reset) input signals, whose operation is not dependent on the clock. On a rising edge (and only then) of the Set signal, the flip-flop output should be set to $Q = 1$. Similarly, on a rising edge (and only then) of the Reset signal, the flip-flop output should be reset to $Q = 0$.

The following Verilog code defines the interface for the desired flip-flop:

```
module dff_async_sr (CLK, S, R, D, Q);
      input CLK, S, R, D;
      output Q;

      reg Q;

      // Your code goes here.

endmodule
```

Write the missing statements that will implement the flip-flop as per the requirements. **[8 marks]**

ii) For the following operation, where the numbers are interpreted as <u>unsigned</u> values:

$$0110\ 1010 + 0010\ 1100$$

a) Derive the 8-bit result. **[2 marks]**

b) Determine the value of the N, Z, C, V flags. **[2 marks]**

c) Using the flags, or otherwise, determine whether an overflow occurred. **[2 marks]**

iii) For the following operation, where the numbers are interpreted as <u>signed</u> values:

$$1001\ 0001 - 0010\ 0100$$

a) Derive the 8-bit result. **[2 marks]**

b) Determine the value of the N, Z, C, V flags. **[2 marks]**

c) Using the flags, or otherwise, determine whether an overflow occurred. **[2 marks]**

End of paper.