Assignment marking guidelines

Assignment II has one design problem. The problem will be marked out of 100.

The marking breakdown is as follows:

1. State diagram: (30 marks)
   - Any assumptions made must be explicitly stated.
   - You may concisely re-write the specification including your design assumptions if needed.
   - Clearly draw the state diagram.
   - Clearly describe in words what each state stands for.
   - Draw the state table.
   - Apply state minimization (all steps must be shown).

2. Implementation (40 marks)
   - State assignment and re-draw the state table.
   - Obtain excitation equations (flip-flop input equations) for all flip-flops used (D, T and JK). Clearly show all tables and K-maps used. In the case of K-maps, indicate which essential prime implicates or prime implicates are used.
   - Draw the logic diagram or schematics for each implementation.
   - Indicate the GIC for each of the implementation and make a comment on the best implementation.

3. Verification: (15 marks)
   - Draw the schematics of your D implementation in Xilinx ISE.
   - Write a test bench (Verilog test file) – you need to attach screenshots of the file.
   - The test bench should be developed such that each state is visited at least once.
   - Include the simulation result from Xilinx (attach screenshots of the file).
   - It has to clearly show the waveforms for the inputs, states, and output.

4. Verilog HDL (15 marks)
   - Write clearly (must be legible) the Verilog HDL (behavioural) of the design based on the state diagram. (you may use this in (3) for verification instead of schematics).
   - Write clearly (must be legible) the Verilog HDL (structural) of the design for DFF implementation.