*The University of New South Wales*

**ELEC2141: Digital Circuit Design**

**Tutorial Week 9 – Arithmetic Circuits**

1. **(3-51)** Obtain the 1s and 2s complements of the following unsigned binary numbers:

    a. 1001 1100
    b. 1001 1101
    c. 1010 1000
    d. 0000 0000
    e. 1000 0000

2. Consider the number 0xF2. Write down the decimal value of this number when represented as an:

    a. 8-bit unsigned number.
    b. 8-bit sign-magnitude number.
    c. 8-bit 1s complement.
    d. 8-bit 2s complement.

3. **(3-52)** Perform the indicated subtraction with the following unsigned binary numbers by taking the 2's complement of the subtrahend:

    a. 11010 - 10001
    b. 11110 - 1110
    c. 111 1110 – 111 1110
    d. 101 001 - 101

4. For the following 8-bit binary additions, determine the result, all status flags (N, Z, C, V), and whether an overflow occurred for both signed and unsigned numbers.

    a. 1100 1000 + 0011 1000
    b. 1000 0000 + 1000 0000
    c. 1010 1010 + 1100 1110
    d. 1010 1010 + 1110 0010

5. **(3-54)** Perform the following arithmetic operations in binary using signed 2s complement representation for negative numbers.

    a. (+36) + (-24)
    b. (-35) - (-24)

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Where referenced, questions are taken from the textbook:

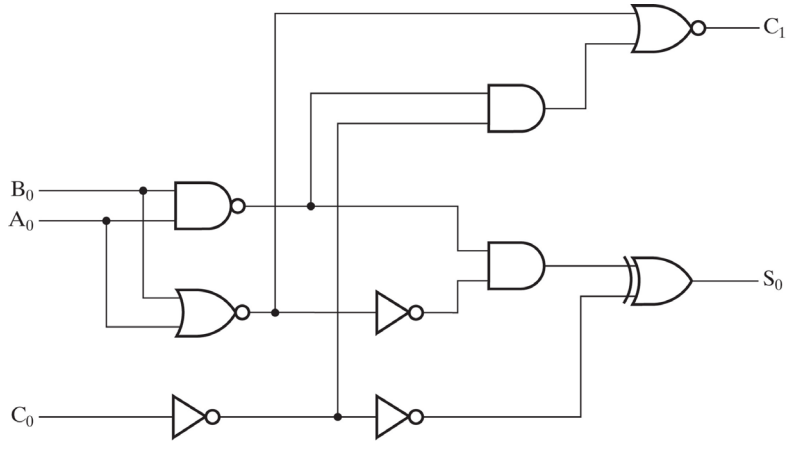
*M. Mano, C. R. Kime and T. Martin, Logic and Computer Design Fundamentals, 5th Edition (Global Edition), Pearson, 2016*

6. **(3-55)** The following binary numbers have a sign in the leftmost position and, if negative, are in 2s complement form. Perform the indicated arithmetic operations, determine the value of the status flags (N, Z, C, V) and verify the answer in decimal. Indicate whether overflow occurs for each computation.

    a. 110 001 + 011 101
    b. 011 0111 + 010 1111
    c. 0000 0111 - 1111 0100
    d. 011 0111 - 010 1111

7. **(3-59)** Design a combinational circuit that compares two 4-bit unsigned numbers *A* and *B* to see whether *B* is greater than *A*. The circuit has one output *X*, so that $X = 1$ if $A < B$ and $X = 0$ if $A \geq B$.

8. **(3-50 & 3-69)** The logic diagram of the first stage of a 4-bit adder is shown below. Verify that the circuit implements a full adder. Write a structural Verilog description for the circuit. Compile and simulate your description. Apply all eight input combinations to check the description.




9. Design a circuit that generates the 9's complement of a BCD digit. Note that the 9's complement of a BCD number *d* is 9-*d*.

10. Derive a scheme for performing subtraction using BCD operands. Show a block diagram for the subtractor circuit.

    Hint: Subtraction can be performed easily if the operands are in 10's complement form. Here the sign bit is 0 for a positive number and 9 for a negative number.