The University of New South Wales

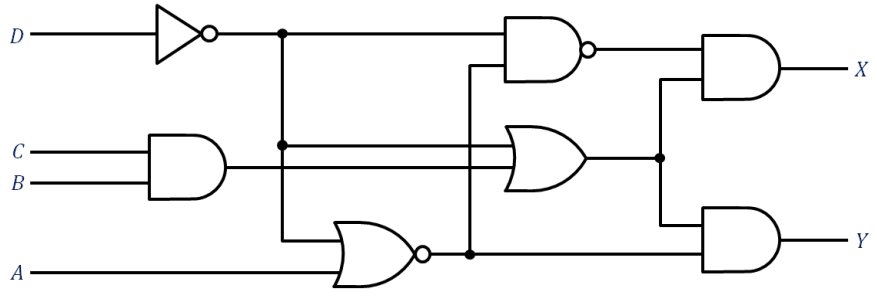
ELEC2141: Digital Circuit Design

Tutorial Week 8 – Verilog HDL

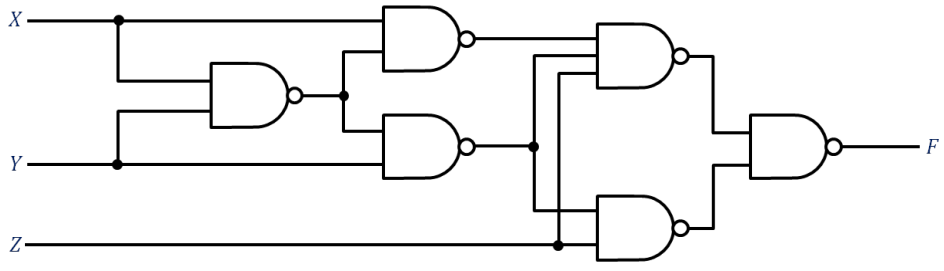
1. Rewrite the Verilog description given below (from lectures) for the 2-to-4-line decoder using vector notation for inputs, outputs and wires.

```
// 2-to-4-Line Decoder with Enable: Structural Verilog Description

module decoder_2_to_4_st_v(EN, A0, A1, D0, D1, D2, D3);
   input EN, A0, A1;
   output D0, D1, D2, D3;

   wire A0_n, A1_n, N0, N1, N2, N3;

   not gn0(A0_n, A0);
   not gn1(A1_n, A1);

   and ga3(N0, A0_n, A1_n);
   and ga4(N1, A0, A1_n);
   and ga5(N2, A0_n, A1);
   and ga6(N3, A0, A1);
   and ga7(D0, N0, EN);
   and ga8(D1, N1, EN);
   and ga9(D2, N2, EN);
   and ga10(D3, N3, EN);

endmodule
```

2. Write a structural Verilog description of the circuit given below.



3. Write a structural Verilog description of the circuit given below. Replace *X*, *Y*, and *Z* with `input [2:0] X`.



4. Find a logic diagram that corresponds to the Verilog structural description in the figure below. Note that complemented inputs are not available.

```
// Combinational Circuit 1: Structural Verilog Description

module comb_ckt_1(x1, x2, x3, x4, f);
   input x1, x2, x3, x4;
   output f;

   wire n1, n2, n3, n4, n5, n6;

   not gn0(n1, x1);
   not gn1(n4, n3);

   and ga2(n2, x2, n1);
   and ga3(n3, x2, x3);
   and ga4(n5, x3, x4);
   and ga5(n6, x1, n4);

   or go6(f, n2, n5, n6);

endmodule
```

5. Find a logic diagram representing minimum two-level logic needed to implement the Verilog dataflow description below. Note that complemented inputs are available.

```
// Combinational Circuit 2: Dataflow Verilog Description

module comb_ckt_2(a, b, c, d, a_n, b_n, c_n, d_n, f, g);
   input a, b, c, d, a_n, b_n, c_n, d_n;
   output f, g;

   assign f = b & (a | (a_n & c)) | (b_n & c & d_n);
   assign g = b & (c | (a_n & c_n) | (c_n & d_n));

endmodule
```

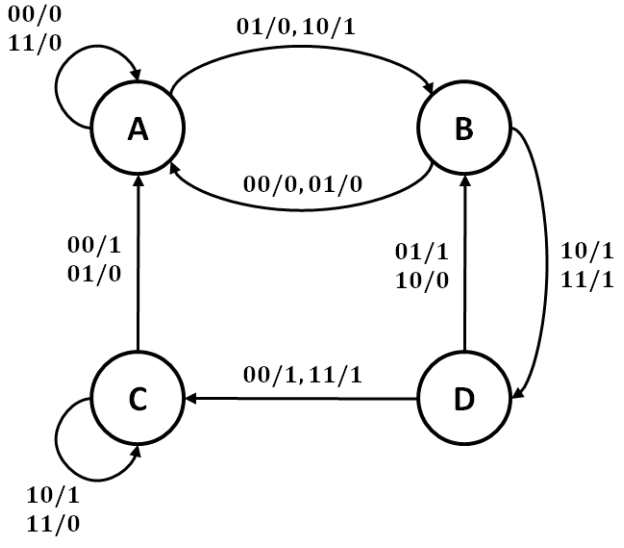
6. Write a dataflow description for the four-input priority encoder, presented in lectures, using the binary decision dataflow concept.

7. Write a Verilog description for a JK negative edge-triggered flip-flop with clock *CLK* and synchronous set (*S*) and reset (*R*) inputs.

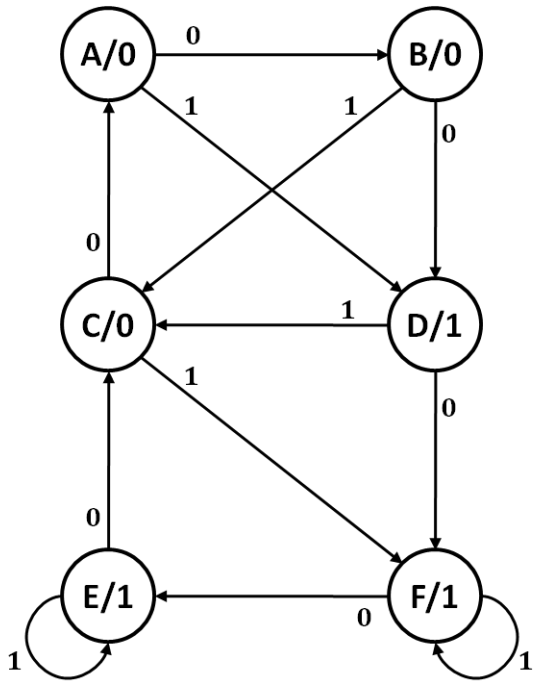
8. Write a Verilog description for a 4-to-1-line multiplexer by using a process containing a case statement.

9. Repeat question 8 by using a Verilog process containing if-else statements.

10. Write a Verilog description for the circuit specified by the following state diagram.



11. Write a Verilog description for the circuit specified by the following state diagram.


A/0
B/0
C/0
D/1
E/1
F/1
0
1
1
0
0
1
1
0
0
0
1
1