The University of New South Wales

ELEC2141: Digital Circuit Design

Tutorial Week 4 – Combinational Logic Circuits Analysis

1. **(2-27)** Prove that the dual of the exclusive-OR is also its complement.
2. **(2-28)** Implement the following Boolean function with exclusive-OR and AND gates, using a minimum number of gate inputs:

$$F(A, B, C, D) = AB\bar{C}D + A\overline{D} + \bar{A}D$$

3.
   a. Implement the function $H = \bar{X}Y + XZ$ using two three-state buffers and an inverter.
   b. Construct an exclusive-OR gate by interconnecting two three-state buffers and two inverters.
4.
   a. Connect the outputs of three 3-state buffers together, and add additional logic to implement the function

$$F = \bar{A}BC + ABD + A\bar{B}\overline{D}$$

   Assume that C, D, and $\overline{D}$ are data inputs to the buffers and A and B pass through logic that generates the enable inputs.
   b. Is your design in part (a) free of three-state output conflicts? If not, change the design to be free of such conflicts.
5. **(3-4)** A simple well-known game, tic-tac-toe, is played on a three-by-three grid of squares by two players. The players alternate turns. Each player chooses a square and places a mark in a square (One player uses X and the other O). The first player with three marks in a row, in a column, or on a diagonal wins the game. A logic circuit is to be designed for an electronic tic-tac-toe that indicates the presence of a winning pattern. The circuit output W is a 1 if a winning pattern is present and a 0 if a winning pattern is not present. For each of the nine squares, there are two signals, X_i and O_i. Two copies of the circuit are used, one for Xs and one for Os. *Hint*: form a condensed truth table for $W(X_1, X_2, \ldots, X_9)$.
   a. Design the X circuit for the following pattern of signals for the squares:

$$X_1\ X_2\ X_3$$
$$X_4\ X_5\ X_6$$
$$X_7\ X_8\ X_9$$

   b. Minimize the W output for the X circuit as much as possible, using Boolean algebra.
6. **(3-9)** Design a combinational circuit that accepts a 4-bit number and generates a 3-bit binary number output that approximates the square root of the number. For example, if the square root is 3.5 or larger, give a result of 4. If the square root is < 3.5 and ≥ 2.5, give a result of 3.

Where referenced, questions are taken from the textbook:

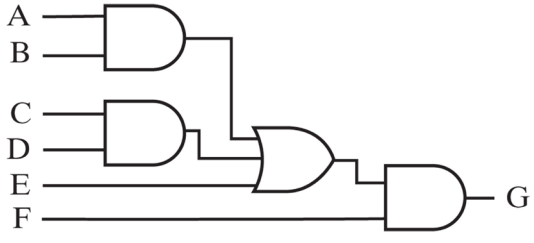
M. Mano, C. R. Kime and T. Martin, Logic and Computer Design Fundamentals, 5th Edition (Global Edition), Pearson, 2016

7. **(3-13)** Design a circuit to implement the following pair of Boolean equations:

$$F_0 = Z(XY + \bar{X}\bar{Y}) + \bar{Z}(X\bar{Y} + \bar{X}Y)$$
$$F_1 = \bar{W}(X\bar{Y} + \bar{X}Y) + W(XY + \bar{X}\bar{Y})$$

To simplify drawing the schematic, the circuit is to use a hierarchy based on the factoring shown in the equation. Three instances (copies) of a single hierarchical circuit component made up of two AND gates, an OR gate, and an inverter are to be used. Draw the logic diagram for the hierarchical component and for the overall circuit diagram using a symbol for the hierarchical component.

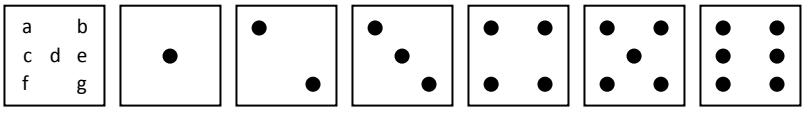
8. **(3-16)** Perform technology mapping to NAND gates for the circuit shown below. Use gate types selected from: Inverter, 2-input NAND, 3-input NAND and 4-input NAND.



9. **(3-17)** Repeat Question 4 using NOR gate types selected from: Inverter, 2-input NOR, 3-input NOR and 4-input NOR.

10. **(3-30)** Design a 5-to-32-line decoder using a 3-to-8-line decoder, a 2-to-4-line decoder, and 32 2-input AND gates.

11. **(3-32)** An electronic game uses an array of seven LEDs (light-emitting diodes) to display the results of a random roll of a die. A decoder is to be designed to illuminate the appropriate diodes for the display of each of the six die values. The desired display patterns are shown in the figure below.



   a. Use a 3-to-8-line decoder and OR gates to map the 3-bit combinations on inputs X_2, X_1, and X_0 for values 1 through 6 to the outputs a through g. Input combinations 000 and 111 are don't-cares.

   b. Note that for the six die sides, only certain combinations of dots occur. For example, dot pattern $A = \{d\}$ and dot pattern $B = \{a, g\}$ can be used for representing input values 1, 2 and 3 as $\{A\}$, $\{B\}$, and $\{A, B\}$. Define four dot patterns A, B, C, and D, and compare its gate-input cost to that of the 3-to-8 decoder and OR gates in part a.

12. **(3-35)** Design a 4-input priority encoder with inputs and outputs as the priority encoder presented in lectures, but with the truth table representing the case in which input D_0 has the highest priority and input D_3 the lowest priority.

13. **(3-38)** Design an 8-to-1-line multiplexer using a 3-to-8-line decoder, eight 2-input AND gates and an 8-input OR gate.

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M. Mano, C. R. Kime and T. Martin, Logic and Computer Design Fundamentals, 5th Edition (Global Edition), Pearson, 2016

14. **(3-44)** A combinational circuit is defined by the following three Boolean functions:

$$F_1 = \bar{X}Y\bar{Z} + \bar{X}\bar{Y}Z + X\bar{Y}\bar{Z}$$
$$F_2 = \bar{X}\bar{Y}\bar{Z} + YZ$$
$$F_3 = YZ + XY$$
$$F_4 = \bar{X}Y + XY\bar{Z}$$

Design the circuit with a decoder and external OR gates.

15. **(3-45)** The rear lights of a car are to be controlled by digital logic. There is a single lamp in each of the rear lights.

The inputs are:

LT	left turn switch - causes blinking of left side lamp
RT	right turn switch - causes blinking of right side lamp
EM	emergency flasher switch - causes blinking of both lamps
BR	brake applied switch - causes both lamps to be on
BL	blinking signal with 1 Hz frequency

The outputs are:

LR	power control for left rear lamp
RR	power control for right rear lamp

a. Write the equations for LR and RR. Assume that BR overrides EM and that LT and RT override BR.

b. Implement each function LR(BL, BR, EM, LT) and RR(BL, BR, EM, RT) with a 4-to-16-line decoder and external OR gates.

16. **(3-46)** Implement the following Boolean function with an 8-to-1-line multiplexer and a single inverter with variable *D* as its input:

$$F(A, B, C, D) = \Sigma m(0, 2, 3, 5, 6, 9, 10, 13)$$

17. **(3-47)** Implement the Boolean function

$$F(A, B, C, D) = \Sigma m(1, 3, 4, 11, 12, 13, 14, 15)$$

with a 4-to-1-line multiplexer and external gates. Connect inputs *A* and *B* to the selection lines. The input requirements for the four data lines will be a function of the variables *C* and *D*. The values of these variables are obtained by expressing *F* as a function of *C* and *D* for each of the four cases when *AB* = 00, 01, 10, and 11. These functions must be implemented with external gates.