Q1

$F = A\bar{B}(C+D) + (\bar{A}+B)AC + \bar{B}C(A+\bar{D}) + CD(\overline{A+B})$

a) literals = 16

complements = 4

terms = 8

GIC = 16 + 4 + 8 = 28

b)

$f(A,B,C,D) = A\bar{B}C + A\bar{B}D + ABC + \bar{A}\bar{B}C + \bar{B}C\bar{D} + \bar{A}\bar{B}CD$

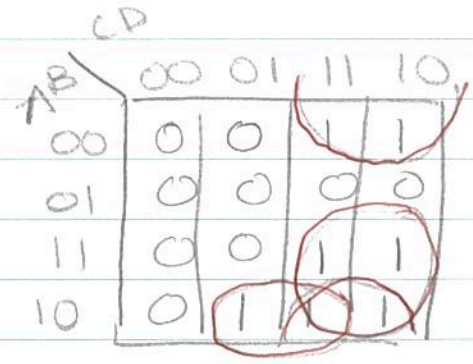
A	B	C	D	f
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	1
1	1	1	1	1

c) $f = \Sigma m(2,3,9,10,11,14,15)$

d) $f = \Pi M(0,1,4,5,6,7,8,12,13)$

Q1

e)

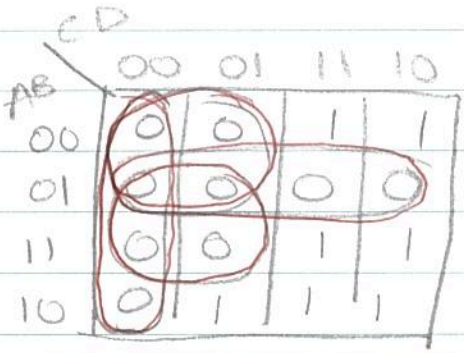


$f = A\bar{B}D + AC + \bar{B}C$

Essential PIs same as PIs

$\Rightarrow A\bar{B}D,\ AC,\ \bar{B}C$

f)



$F = (C+D)(A+\bar{B})(A+C)(\bar{B}+C)$

g) $F = A\bar{B}D + AC + \bar{B}C$

literals = 7

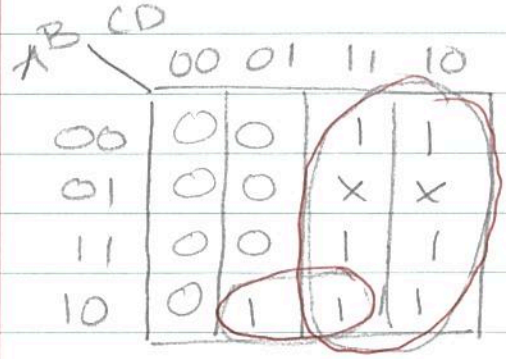
complements = 1

terms = 3

GIC = 7 + 1 + 3 = 11

reduction = 28 − 11 = 17

h) $\Sigma d(6,7)$



$F = C + A\bar{B}D$

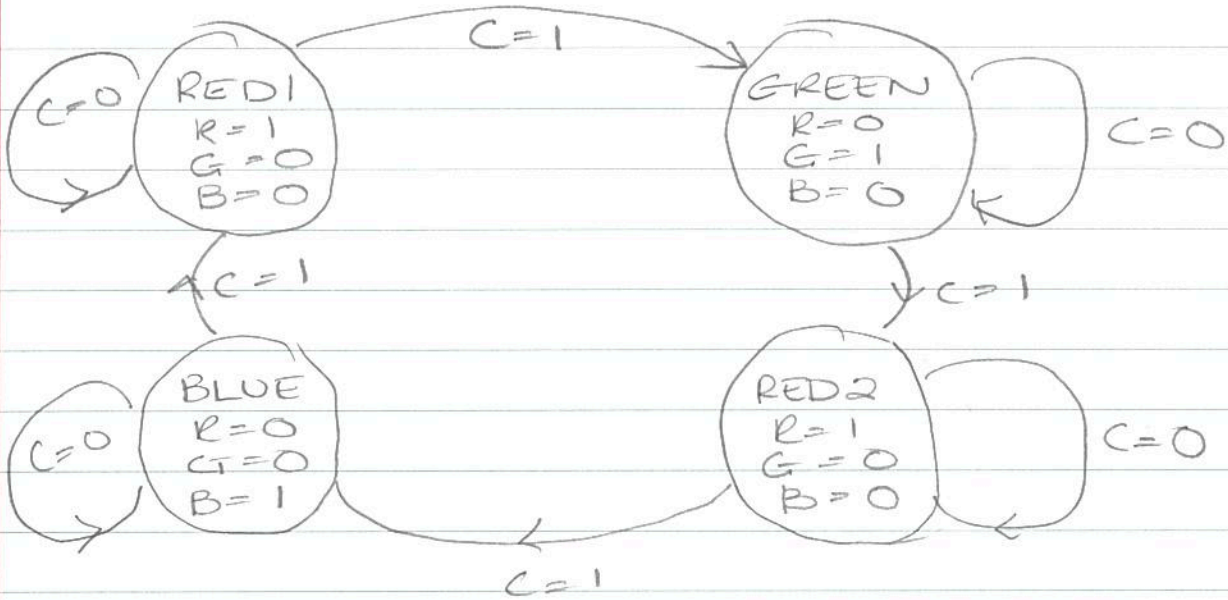
Q2(i)

Input = change (C)

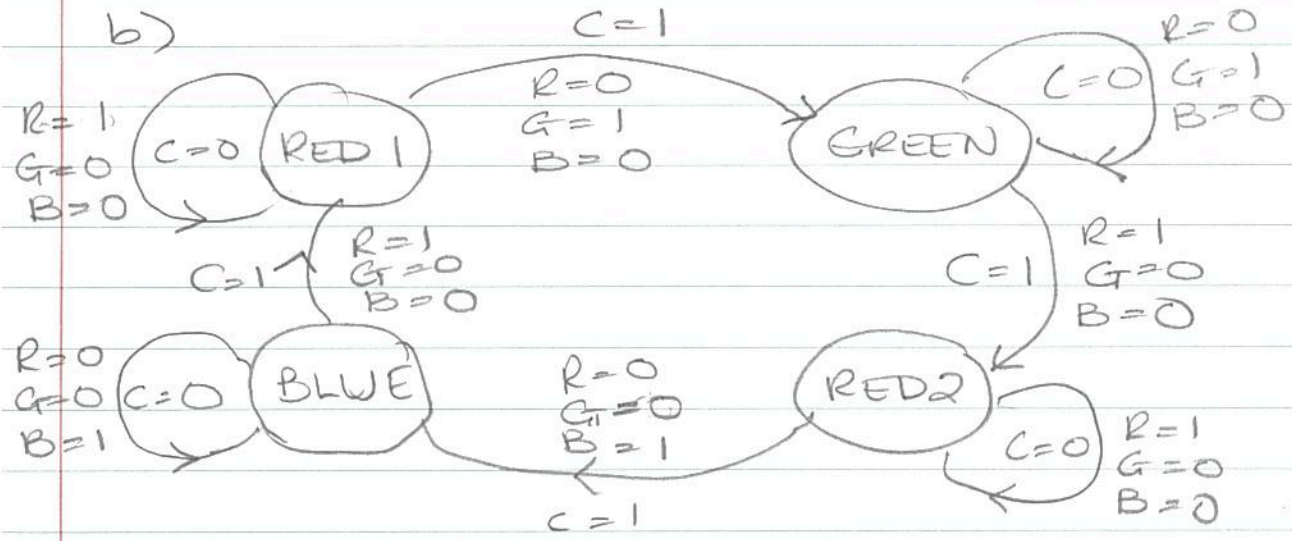
outputs = Red(R) ; Green(G) ; Blue(B)

4 states : Red1, Green, Red2, Blue

a)



b)



c)

4 states ⇒ 2 flipflops X & Y

State assignment

RED1 = 00

GREEN = 01

RED2 = 10

BLUE = 11

OR ALTERNATIVE (PAGE 7)

This can be skipped

(I)

Present State	Next state C=0	Next state C=1	Output/RGB C=0	Output/RGB C=1
RED1	RED1	GREEN	100	010
GREEN	GREEN	RED2	010	100
RED2	RED2	BLUE	100	001
BLUE	BLUE	RED1	001	100

(II)

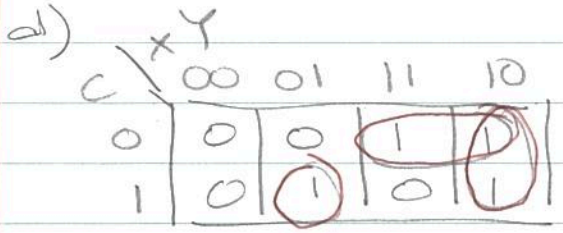
Present State XY	Next state C=0 XY	Next state C=1 XY	Output/RGB C=0 RGB	Output/RGB C=1 RGB
00	00	01	100	010
01	01	10	010	100
10	10	11	100	001
11	11	00	001	100

OR — could be in part (d)

(III)

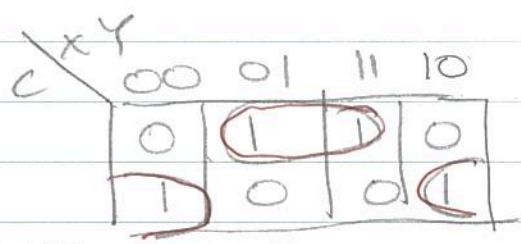
Input C	Present state XY	Next state XY	Output RGB
0	00	00	100
1	00	01	010
0	01	01	010
1	01	10	100
0	10	10	100
1	10	11	001
0	11	11	001
1	11	00	100

d)



$X(t+1) = D_X$

$= X\bar{C} + X\bar{Y} + \bar{X}YC$



$Y(t+1) = D_Y$

$= Y\bar{C} + \bar{Y}C = Y \oplus C$

C \ XY	00	01	11	10
0	1	0	0	1
1	0	1	1	0

$R = \overline{Y}C + Y\overline{C}$

$= Y \oplus C$

C \ XY	00	01	11	10
0	0	1	0	0
1	1	0	0	0

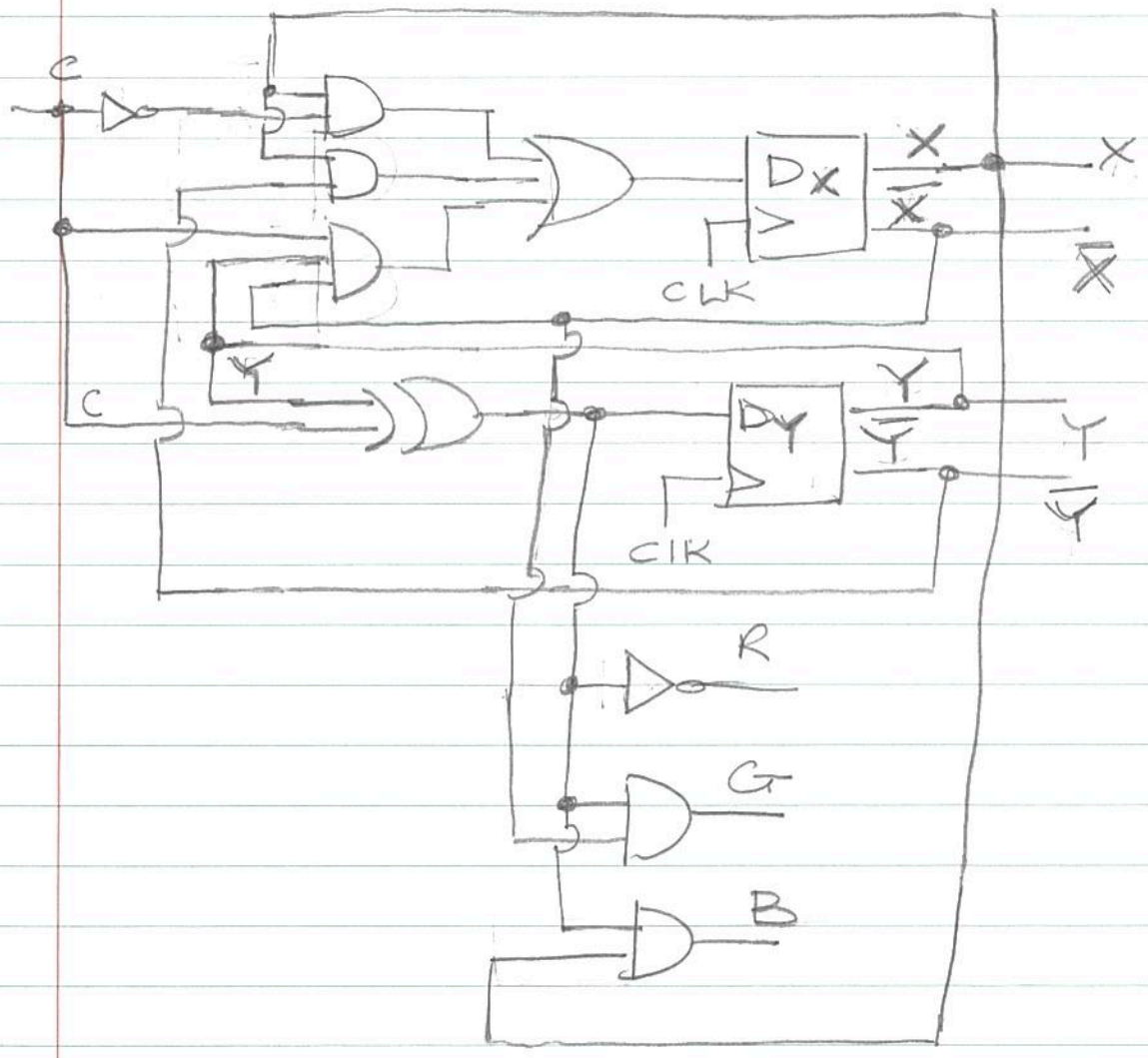
$G = \overline{X}Y\overline{C} + \overline{X}\overline{Y}C$

$= \overline{X}(Y\overline{C} + \overline{Y}C) = \overline{X}(Y \oplus C)$

C \ XY	00	01	11	10
0	0	0	1	0
1	0	0	0	1

$B = XY\overline{C} + X\overline{Y}C$

$= X(Y\overline{C} + \overline{Y}C) = X(Y \oplus C)$



e)

```
module mealy_RGRB(C, clk)
    input C, clk;
    output R, G, B;
    wire a, b;
    reg X, Y;

    assign a = Y^C;
    assign b = (X & ~C) | (X & ~Y) | (~X & Y & C);
    assign R = ~a;
    assign G = ~X & a;
    assign B = X & a;

    Dff D1(X, b, clk);
    Dff D2(Y, a, clk);
endmodule

module Dff(Q, DO, clk)
    input DO, clk;
    output reg Q;
    always @(posedge clk)
        Q <= DO;
endmodule
```

ALTERNATIVE SOLUTION

c) Using one hot coding

RED1 = 1000
GREEN = 0100 ⇒ Uses 4 flip-flops
RED2 = 0010 WXYZ
BLUE = 0001

d)

Present state	Next state		Output	
	C=0	C=1	C=0	C=1
WXYZ	WXYZ	WXYZ	RGB	RGB
1000	1000	0100	100	010
0100	0100	0010	010	100
0010	0010	0001	100	001
0001	0001	1000	001	100

$W(t+1) = W\bar{C} + ZC$
$X(t+1) = X\bar{C} + WC$
$Y(t+1) = Y\bar{C} + XC$
$Z(t+1) = Z\bar{C} + YC$

$R = W\bar{C} + Y\bar{C} + XC + ZC$
$G = X\bar{C} + WC$
$B = Z\bar{C} + YC$

- Circuit diagram of above

e) Code for above

2(ii)

597.892_{10}

2	597	
	298	1
	149	0
	74	1
	37	0
	18	1
	9	0
	4	1
	2	0
	1	0

$597_{10} = 1001010101_2$

$0.892 \times 2 = 1.784$	1
$0.784 \times 2 = 1.568$	1
$0.568 \times 2 = 1.136$	1
$0.136 \times 2 = 0.272$	0
$0.272 \times 2 = 0.544$	0
$0.544 \times 2 = 1.088$	1
$0.088 \times 2 = 0.176$	0

$0.892_{10} = 0.111001$

→ $597.892_{10} = 1001010101.111001_2$

3(i)

a) 1 1 1 0 1 1 1 1 (−33)
+ 1 0 1 1 1 0 0 0 (−72)
1 | 1 0 0 1 0 1 1 1 (−105)

0 1 1 1 0 1 0 1 (117)
− 1 1 0 1 0 1 1 0 — (−42)

As subtraction need to take 2's comp of 11010110

2's comp of 11010110 = 00101010

⇒ 0 1 1 1 0 1 0 1
0 0 1 0 1 0 1 0
0 | 1 0 0 1 1 1 1 1

b)

N	Z	C	V
1	0	1	0

N	Z	C	V
0	0	0	1

c)

$C_{in}(MSB) = 1$

$C_{out}(MSB) = 1$

$\Rightarrow V = C_{in} \oplus C_{out} = 0$

$C_{in}(MSB) = 1$

$C_{out}(MSB) = 0$

$\Rightarrow V = C_{in} \oplus C_{out} = 1$

3(11)

a) It is a 4 bit shift register that moves bits from left to right (clk)

b) inputs: the clock & 1 input bit (in)
outputs: 4 outputs from the 4 flipflops used in register (out1 – 4)

At the positive edge of the clock (clk) the input bit (in) in fed to the left most flipflop.

⇒ out1 = in

and output of the left most flip flop is fed to the next one & so on

⇒ out2 = out1
out3 = out2
out4 = out3

3(iii)

$F(A,B,C) = AB + AC + BC$

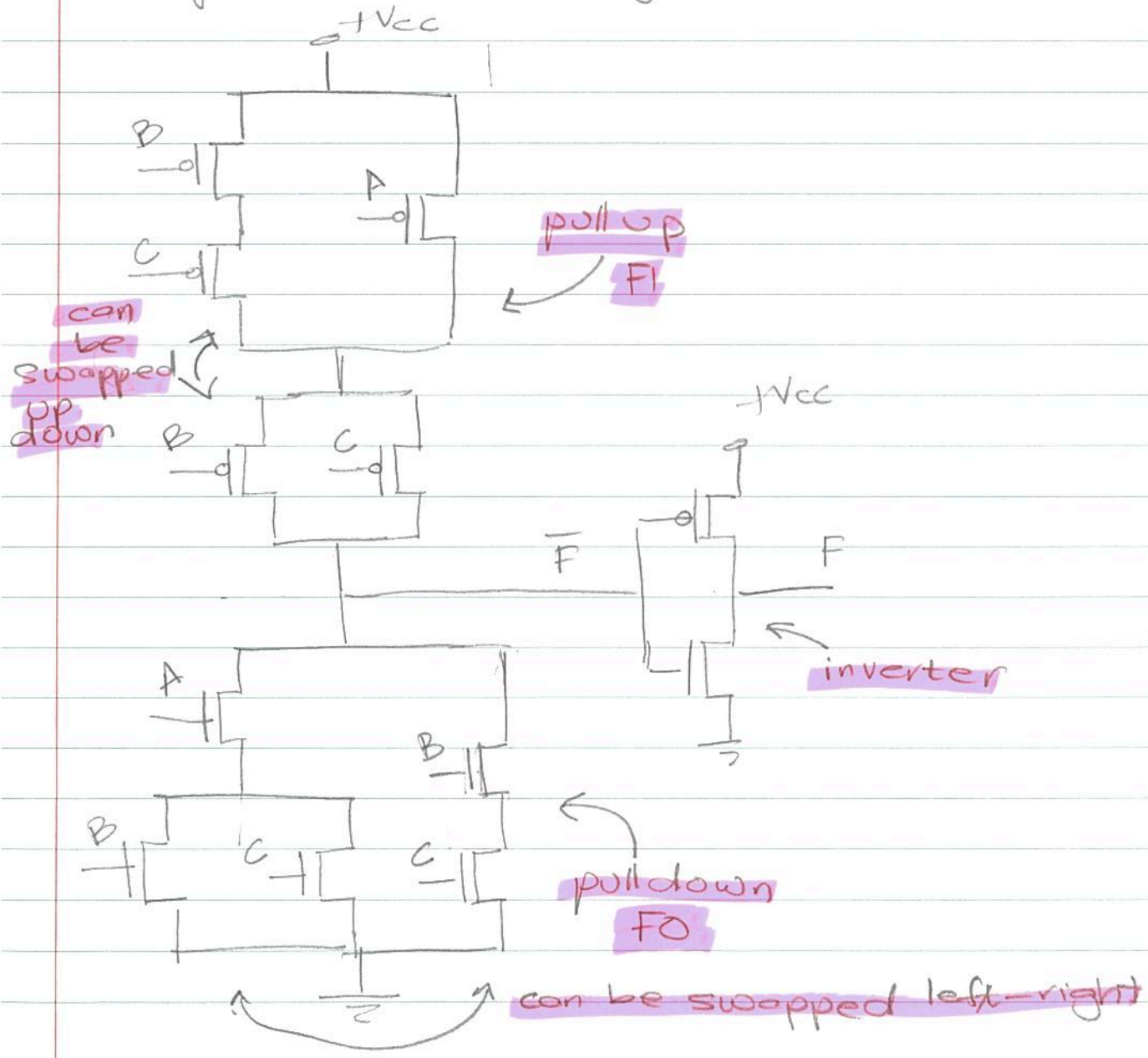
$= A(B+C) + BC$

CMOS implementation will require complement of each variable, ie. inverters with 2 transistors each = 6 transistors plus implementation cost

$\overline{F} = \overline{A(B+C)+BC} = [\overline{A(B+C)}]\,\overline{BC}$

$= [\bar{A} + \overline{(B+C)}]\,\overline{BC} = (\bar{A} + \bar{B}\bar{C})(\bar{B}+\bar{C})$

Implementation of $\overline{F}$ will not require complements so will use less transistors - just 2 extra to get F at end

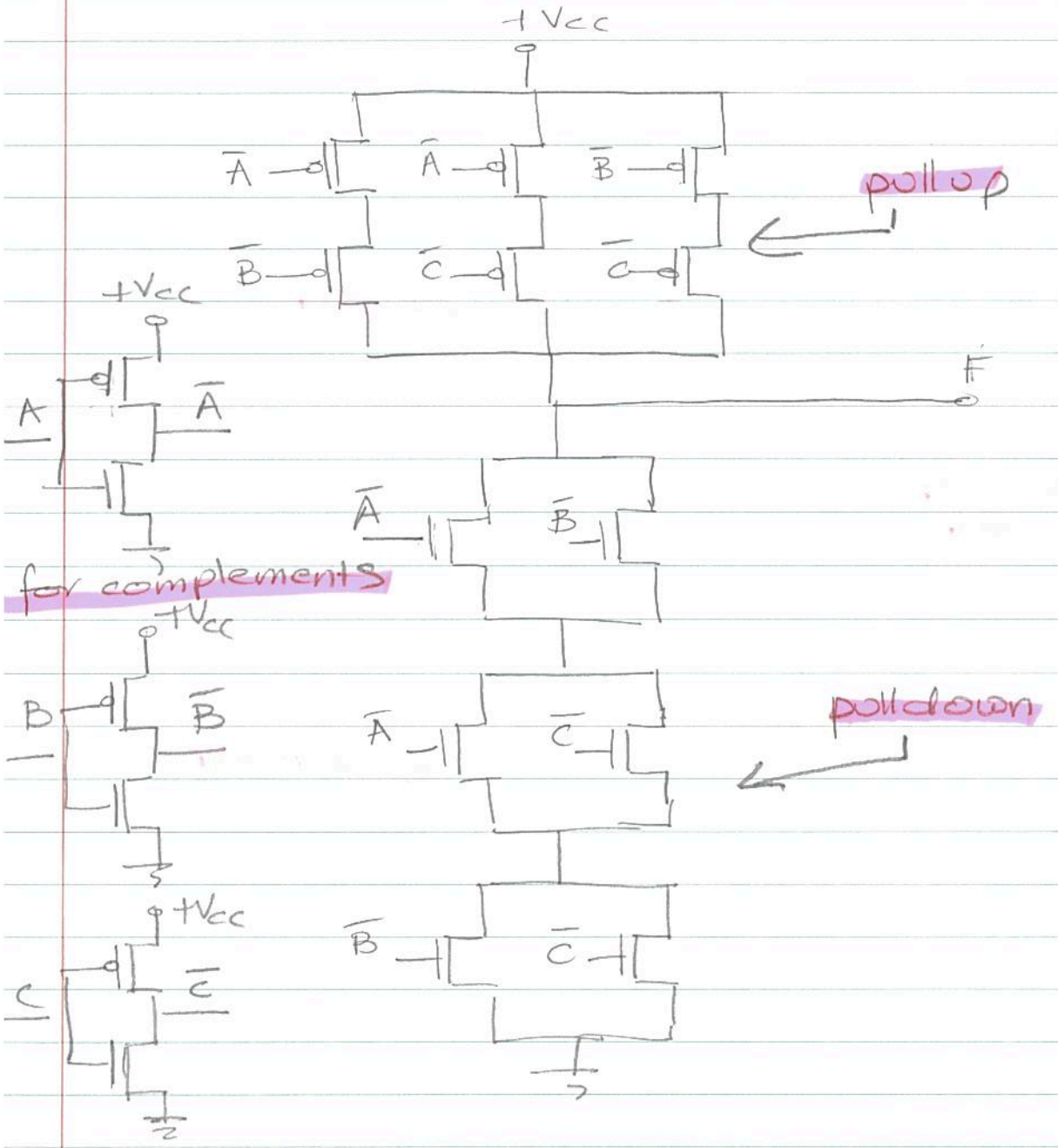


3(iii) – Alternative

$F(A,B,C) = AB + AC + BC$

$\overline{F} = \overline{AB + AC + BC} = (\overline{AB})(\overline{AC})(\overline{BC})$

$= (\overline{A} + \overline{B})(\overline{A} + \overline{C})(\overline{B} + \overline{C})$



This uses 12 transistors + 6 transistors to get complemented = 18 total

B(iii) — Alternative

$F(A,B,C) = A(B+C)+BC$ *

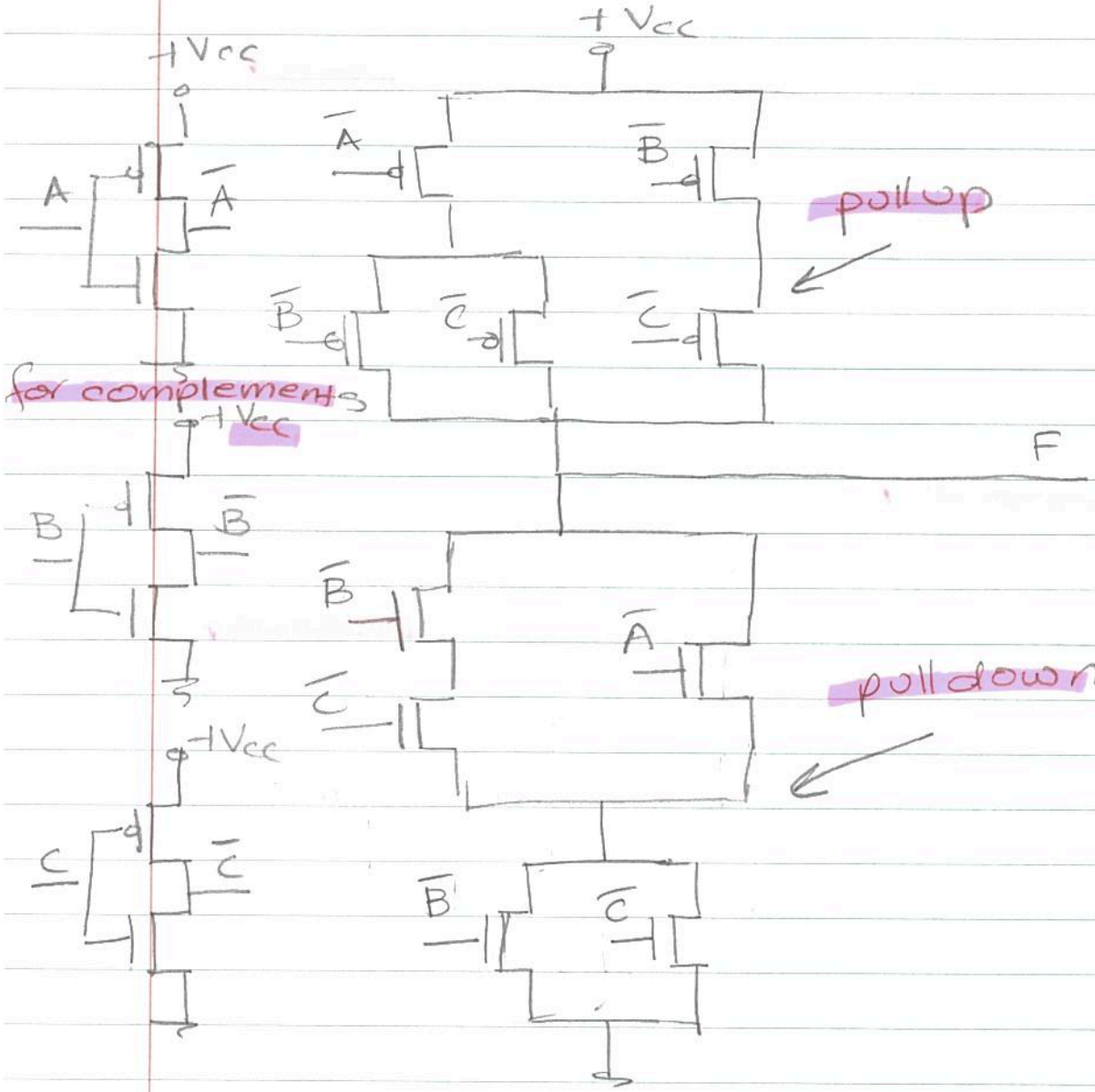
OR

$AB + C(A+B)$

OR

$AC + B(A+C)$

$$\overline{F} = \overline{A(B+C)+BC} = \left[\overline{A(B+C)}\right]\overline{BC}$$
$$= \left[\bar{A} + \overline{(B+C)}\right](\bar{B}+\bar{C})$$
$$= (\bar{A} + \bar{B}\bar{C})(\bar{B}+\bar{C})$$



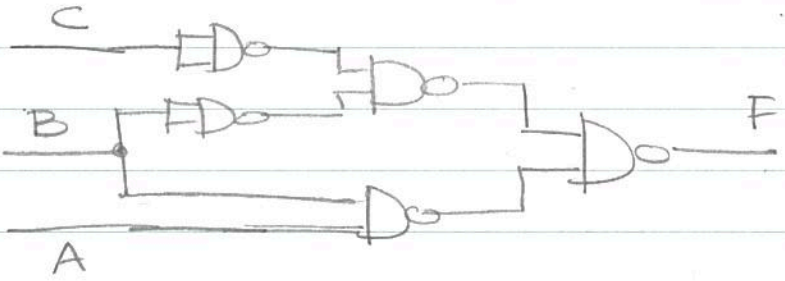
This uses 10 transistors + 6 transistors to get complements = 16 transistors

4(i)

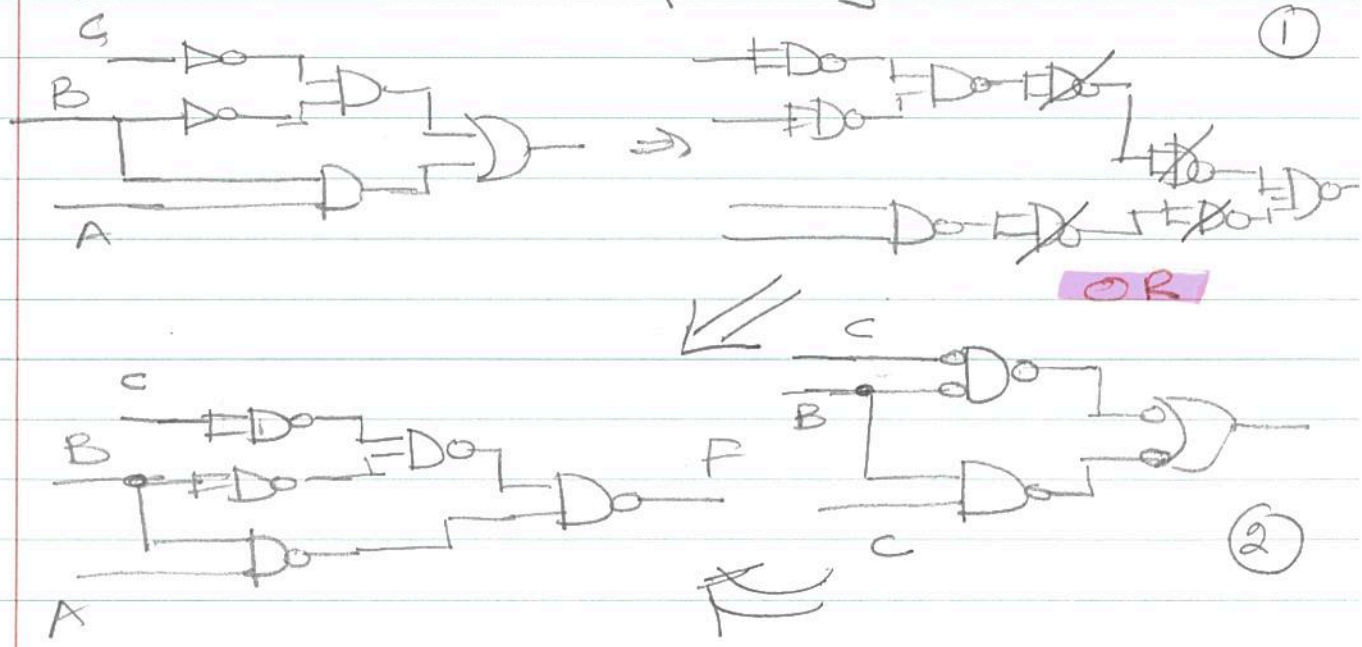
$F(A,B,C) = \overline{B}\overline{C} + AB$

a) $F = \overline{\overline{B}\overline{C} + AB} = \overline{(\overline{B}\overline{C})(\overline{AB})}$

↳ Applying DeMorgan's law



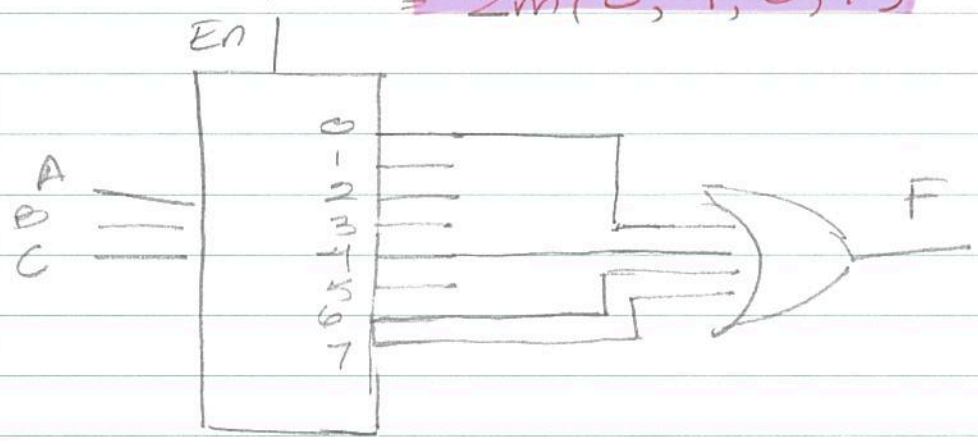
OR Graphically



b) $F(A,B,C) = \overline{B}\overline{C} + AB = (A+\overline{A})\overline{B}\overline{C} + (C+\overline{C})AB$

$= \overline{A}\overline{B}\overline{C} + A\overline{B}\overline{C} + AB\overline{C} + ABC$

$= \Sigma m(0,4,6,7)$

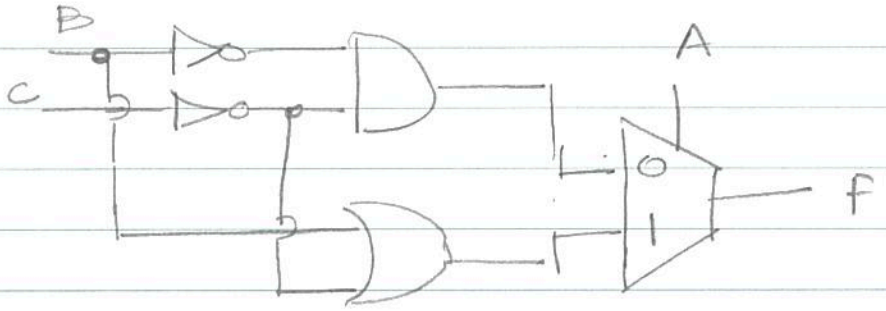


4(i)

c)

A	B	C	F
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

A	F
0	$\bar{B}\bar{C}$
1	$B+\bar{C}$



Can implement any of these three

OR

C	A	B	F
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

$A+\bar{B}$ | AB

OR

B	A	C	F
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

$\bar{C}$ | A

C	F
0	$A+\bar{B}$
1	AB

circuit as per above with C on enable

B	F
0	$\bar{C}$
1	A

circuit as per above with B on enable

4(ii)

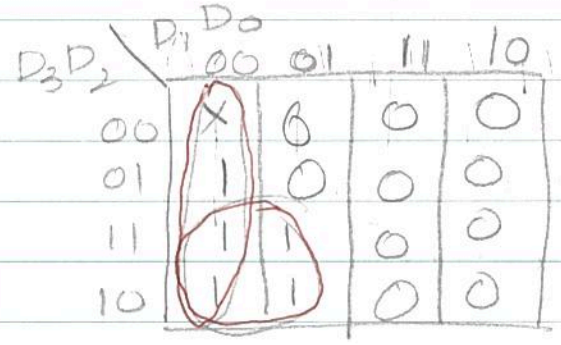
$D_1 > D_3 > D_0 > D_2$

a)

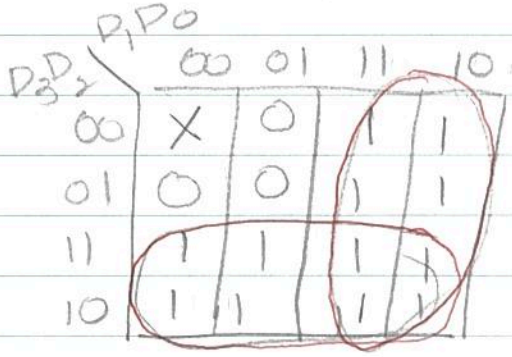
D_3	D_2	D_1	D_0	A_1	A_0	V
0	0	0	0	x	x	0
0	x	0	1	0	0	1
x	x	1	x	0	1	1
0	1	0	0	1	0	1
1	x	0	x	1	1	1

b)

$$V = \overline{\overline{D_3}\,\overline{D_2}\,\overline{D_1}\,\overline{D_0}} = D_3 + D_2 + D_1 + D_0$$



$$A_1 = \overline{D_1}\,\overline{D_0} + D_3\overline{D_1} = \overline{D_1}(\overline{D_0} + D_3)$$



$$A_0 = D_1 + D_3$$

4(iii)

a)

$D_X = X_1(t+1) = w(X + Y)$

$D_Y = Y(t+1) = w(\overline{X} + \overline{Y})$

$z = X\overline{Y}$

State assignment table:

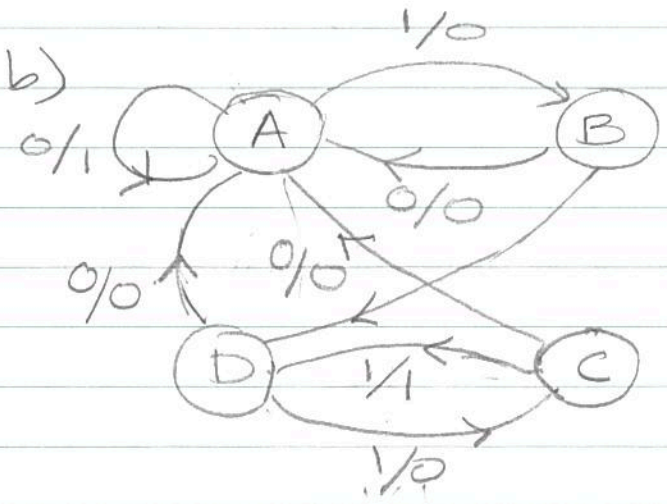
Present state	Next state $w=0$	Next state $w=1$	Output
XY	XY	XY	z
00	00	01	0
01	00	11	0
10	00	11	1
11	00	10	0

OR

State table:

Present state	Next state $w=0$	Next state $w=1$	Output
			z
A	A	B	0
B	A	D	0
C	A	D	1
D	A	C	0

b)



for $z=1$ w needs to be a 0 followed by 1's

9(iii)

a) ALTERNATIVE

Input	Present state	Next state	Output
w	XY	XY	Z
0	00	00	0
1	00	01	0
0	01	00	0
1	01	11	0
0	10	00	1
1	10	11	1
0	11	00	0
1	11	10	0