The University of New South Wales

ELEC2141: Digital Circuit Design

Tutorial Week 10 – Digital IC Logic Families

1.

$$\text{fan-out} = \text{minimum of}\left(\frac{I_{OH}}{I_{IH}}, \frac{I_{OL}}{I_{IL}}\right)$$

$$= \text{minimum of}\left(\frac{1mA}{0.05mA}, \frac{20mA}{2mA}\right)$$

$$= \text{minimum of}\,(20, 10) = 10$$

$$\text{power dissipation} = V_{CC} \cdot \left(\frac{I_{CCH} + I_{CCL}}{2}\right)/4$$

$$= 5V \cdot \left(\frac{10+20}{2}\right) \cdot \frac{1}{4}$$

$$= 5 \cdot 15 \cdot \frac{1}{4} = \frac{75}{4} = 18.75mW$$

$$\text{propagation delay} = \text{maximum of}\,(t_{PLH} \text{ or } t_{PHL})$$

$$= \text{maximum of}\,(3ns, 3ns) = 3ns$$

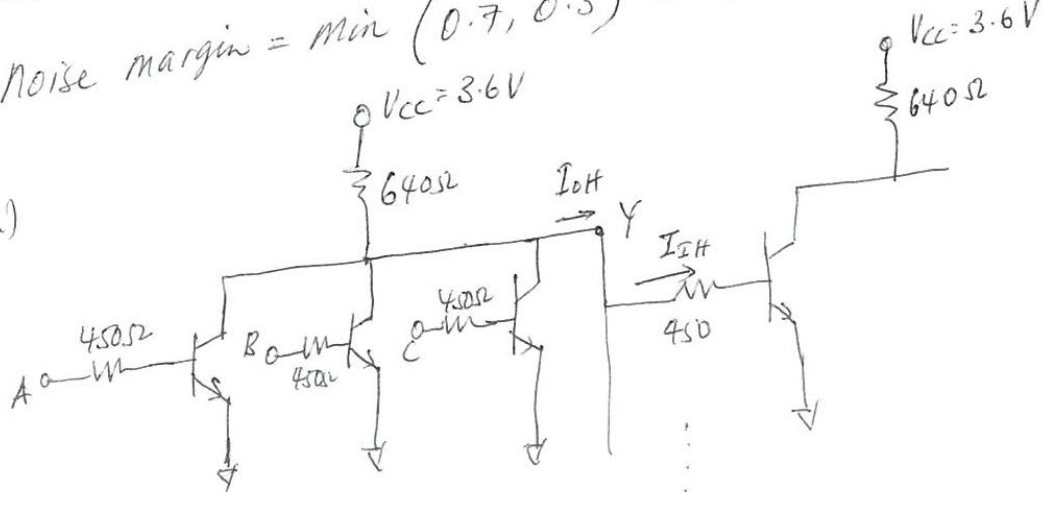
$$\text{High state noise margin} = V_{OH} - V_{IH} = 2.7V - 2V = 0.7V$$

$$\text{Low state noise margin} = V_{IL} - V_{OL} = 0.8 - 0.5 = 0.3V$$

$$\text{noise margin} = \text{Min}\,(0.7, 0.3) = 0.3V$$

2.

(a)



For high output, all inputs (A, B, C) ~~are to~~ should be low and all the transistors are off. Hence, I_{OH} flows through only 640Ω from the supply $V_{cc} = 3.6V$.

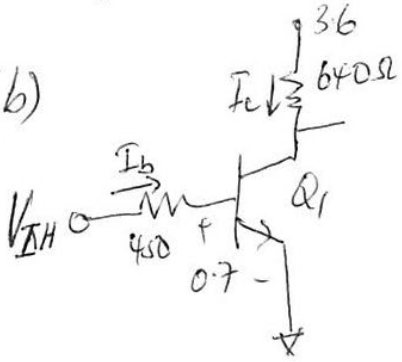
$$3.6V = 640\, I_{OH} + 450\, \frac{I_{OH}}{5} + 0.7$$

$$= (640 + 90)\, I_{OH} = 2.9$$

$$I_{OH} = \frac{2.9}{730} = \underline{3.9mA}$$

$$V_{OH} = Y = 3.6 - 640(3.9) = \underline{1.06V}$$

(b)



When Q goes into saturation $V_{CE} \approx 0.2$

$$\therefore I_c = \frac{3.6 - 0.2}{640} A = 5.31mA$$

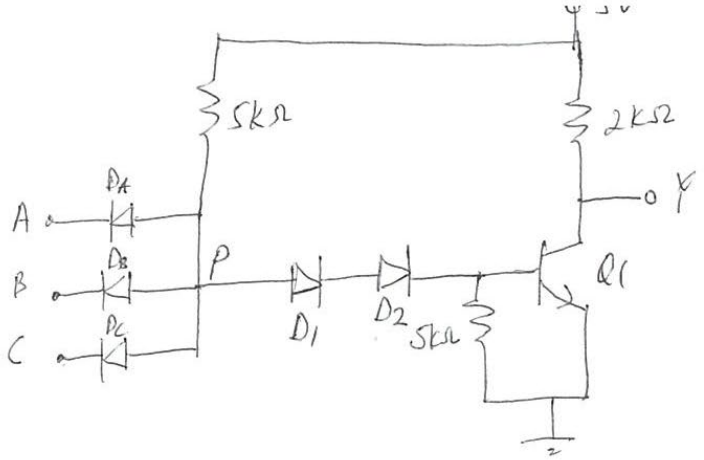
$$I_b = I_c/20 = 0.26mA$$

$$V_{IH} = 450 \times I_b + 0.7 = 0.82V$$

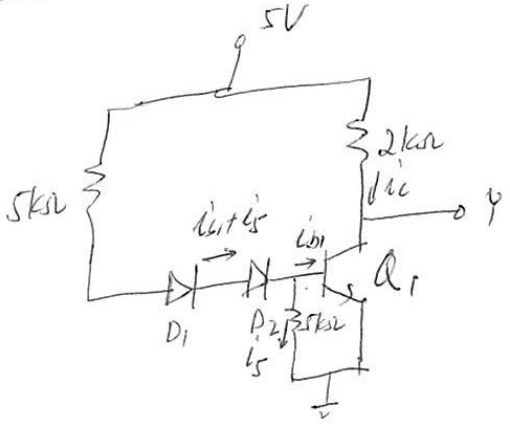
(C) $V_{OH} - V_{IH}$ = noise margin

noise margin = $1.06 - 0.82 = 0.24V$

3.



When A, B, and C are high, diode D_A, D_B and D_C will be reversed biased and the above circuit can be represented as



$$5V - 5(i_{b1} + i_5') - 0.7 - 0.7 - 0.7 = 0$$

$$5 - 5(i_{b1} + i_5') = 2.1$$

$$i_{b1} + i_5' = \frac{5 - 2.1}{5} = 0.58mA$$

$$i_5' = \frac{0.7}{5} = 0.14mA$$

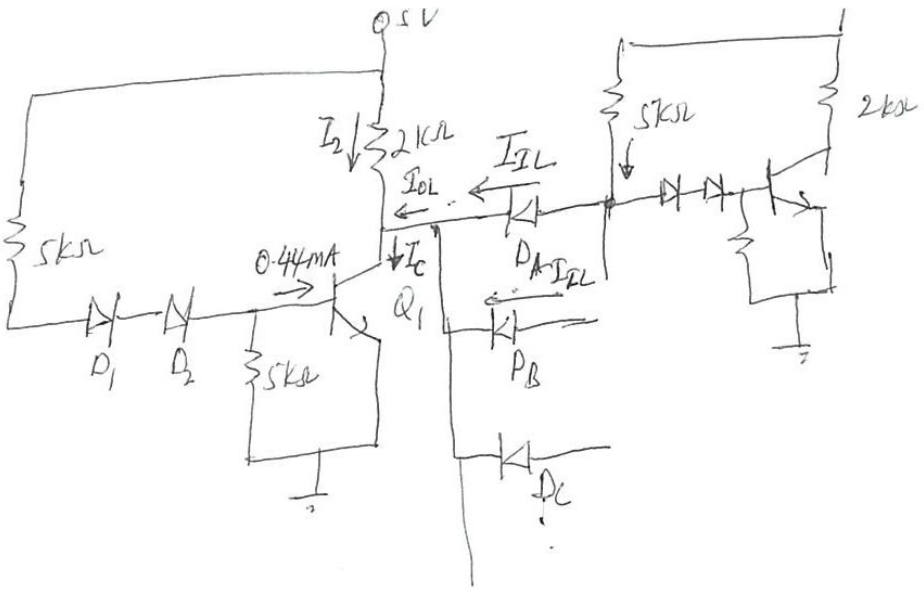
$$\therefore \quad i_{b1} = 0.58 - 0.14 = 0.44mA$$

For $h_{fe} = 20$, $I_{CS} = 20(0.44) = 8.8mA$

$$I_{CS} = \frac{5 - 0.2}{2} = 2.4mA < 8.8mA$$

$\therefore Q_1$ is in saturation

4.



$I_C = 0.44 \times 20 = 8.8\,mA$

(a) $I_2 = \dfrac{5-0.2}{2} = 2.4\,mA$

$I_{OL} = 8.8\,mA - 2.4\,mA = 6.4\,mA$

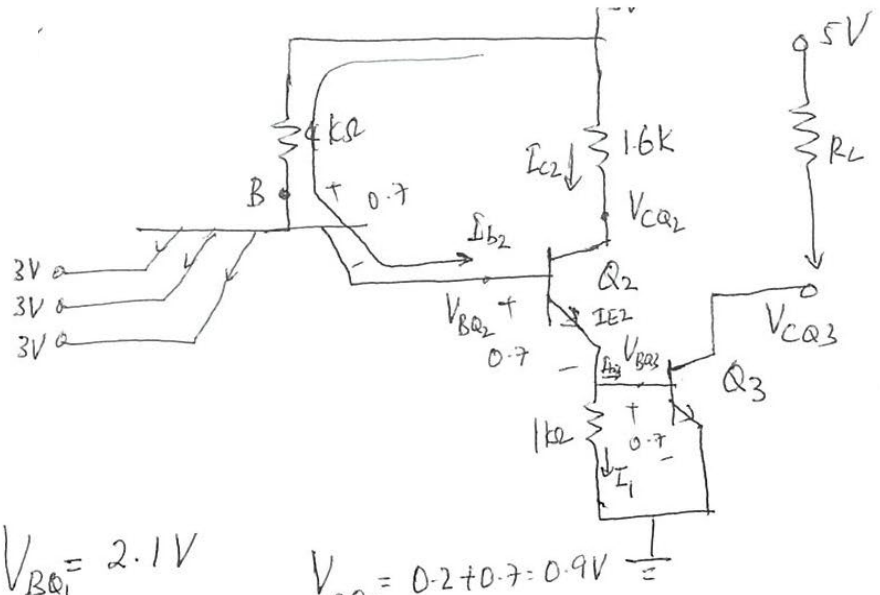
(b) $I_S = \dfrac{5-0.9}{5} = 0.82\,mA = I_{IL}$

(c) $2.4 + 0.82N$

(d) $N = \dfrac{I_{OL}}{I_{IL}} = \dfrac{6.4\,mA}{0.82\,mA} = 7.8$

(e) $N = 7$

5.



(a)

$V_{BQ_1} = 2.1V$ $\quad V_{CQ_2} = 0.2 + 0.7 = 0.9V$

$V_{BQ_2} = 1.4V$ $\quad V_{CQ_3} = 0.2V$

$V_{BQ_3} = 0.7V$ $\quad V_{EQ_2} = V_{BQ3} = 0.7V$

(b) $$I_{b2} = \frac{5 - 2.1}{4} = 0.725mA$$

$$I_{C2} = \frac{5 - 0.9}{1.6} = 2.5625mA$$

(c) $$h_{fe} = \frac{2.5625}{0.725} = 3.53$$

(C) $$I_{b3} = I_{E2} - I_1 = (I_{b2} + I_{C2}) - I_1$$

$$= [(0.725 + 2.5625) - 0.7]$$

$$= 2.5875$$

(d) $$I_{C3} = 2.5875 \times 6.18 = 16mA$$

(e) $$R_L = \frac{5 - 0.2}{16} = 300\Omega$$

6.

(a) When C is low and A is low

Q_7 is off
Q_6 is off
Q_2 is off
Q_3 is off
Q_5 is ON
Q_4 is ON
Y is high

(b) When C is low and A is high

Q_7 is off
Q_6 is off
Q_2 is ON
Q_3 is ON
Q_4 is OFF
Q_5 is off

Q_7 is on
Q_8 is on
Q_2 is ON
Q_3 is off
Q_4 is off
Y is high impendence

7.

By analyzing the PDN, the function is:

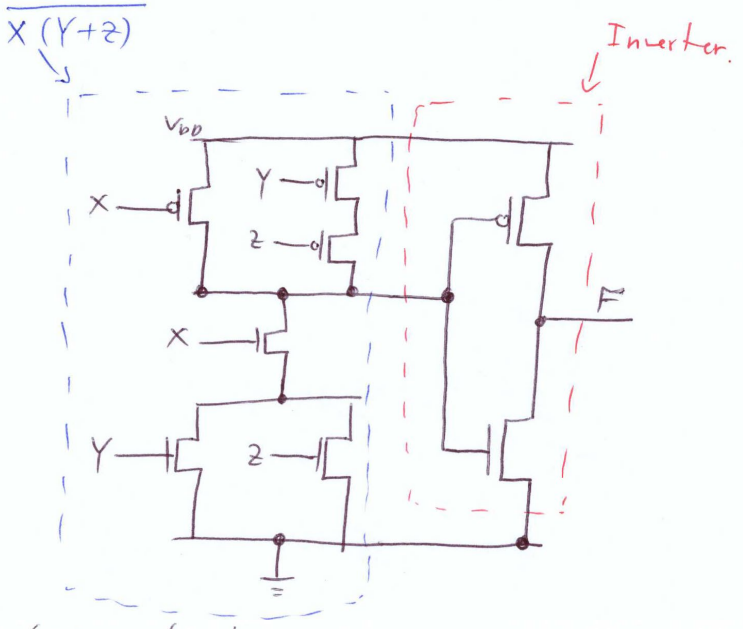
$$Z = \overline{AB + C + D}$$

$$= (\bar{A} + \bar{B})\,\bar{C}\,\bar{D}$$

8.

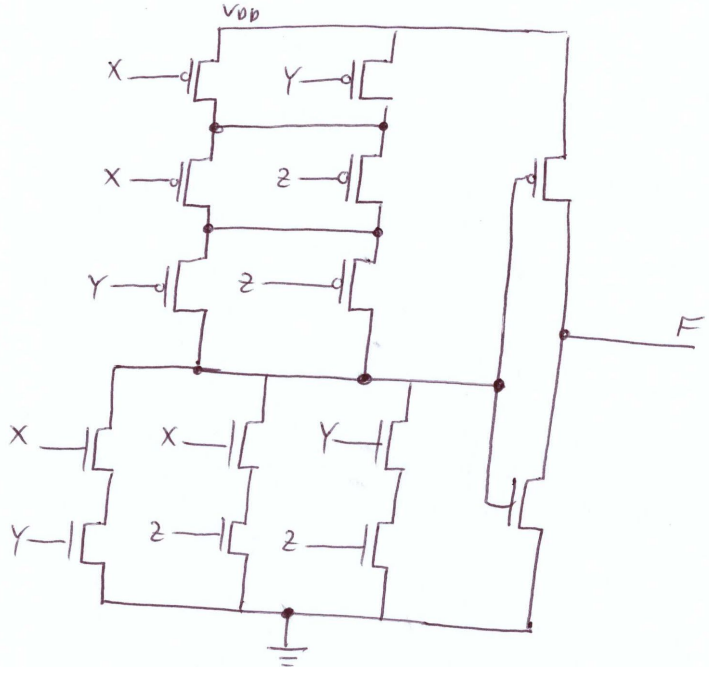
a. To minimize the number of transistors used, factorize the function:

$$F = X(Y+Z)$$

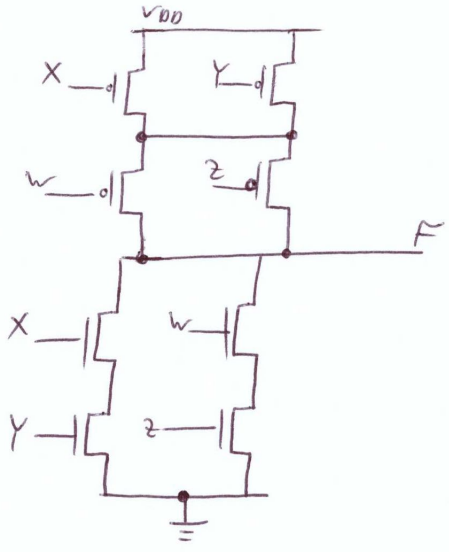


b. (This function may be minimized further)

$$F = XY + XZ + YZ$$

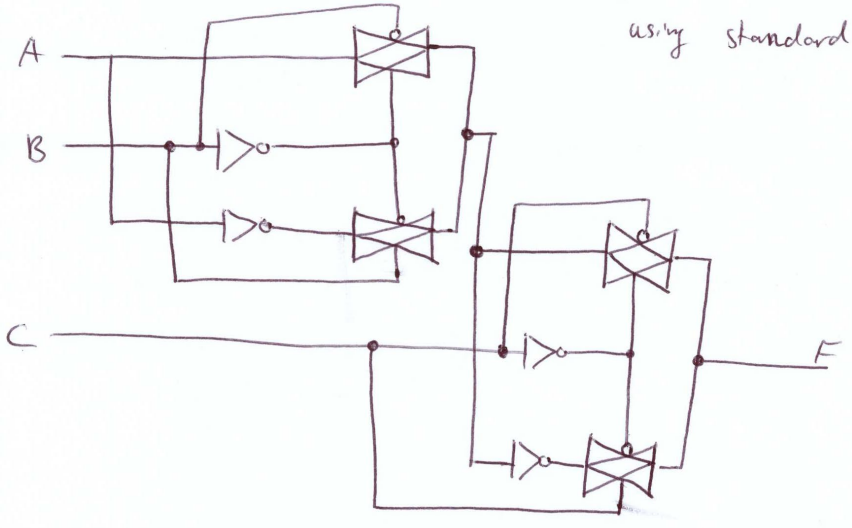


c. $F = \overline{XY + WZ}$



d. Using transmission gates:

(where the inverters are implemented using standard CMOS design).

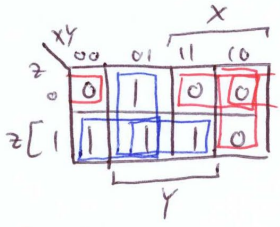


9. a.

$$F = YZ + \bar{X}Z + \bar{X}Y\bar{Z}$$

Implementing this directly requires 20 transistors.

Using a k-map, try to find minimal expression for both F and $\bar{F}$ to check which one gives the least transistors.



$F = \bar{X}Z + YZ + \bar{X}Y$ (16)

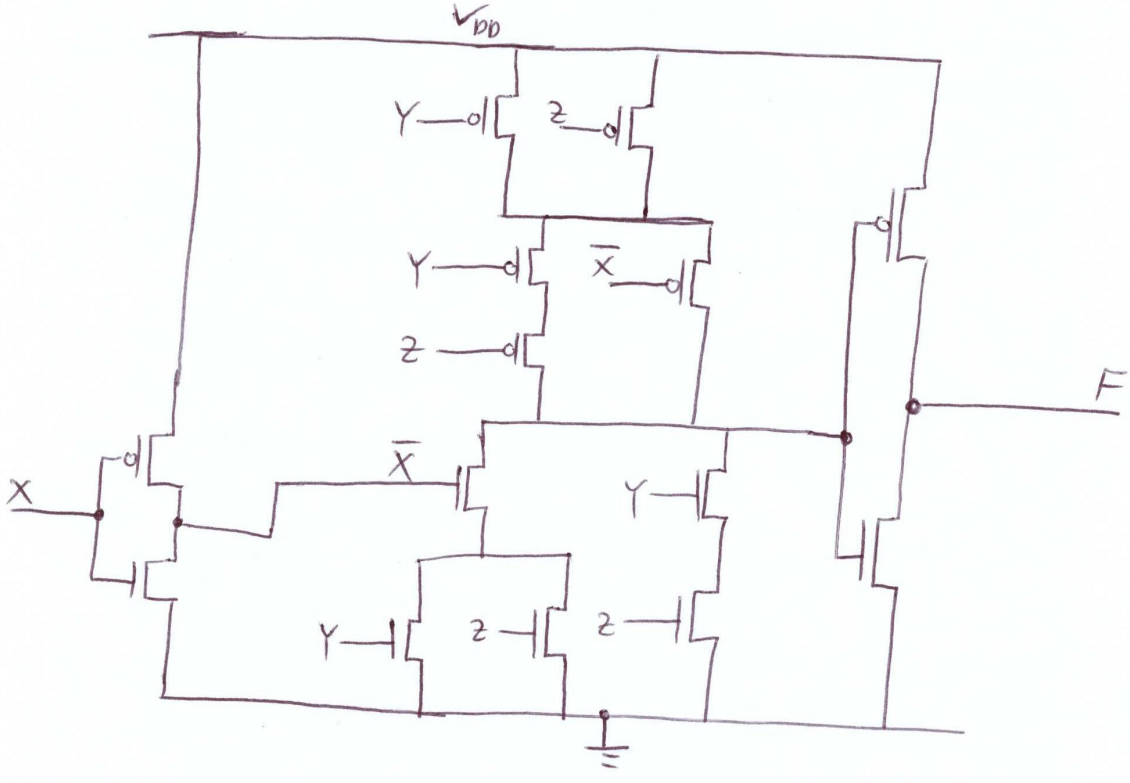
$= \bar{X}(Y+Z) + YZ$ (14)

$\bar{F} = X\bar{Y} + X\bar{Z} + \bar{Y}\bar{Z}$ (16)

$= X(\bar{Y} + \bar{Z}) + \bar{Y}\bar{Z}$ (14)

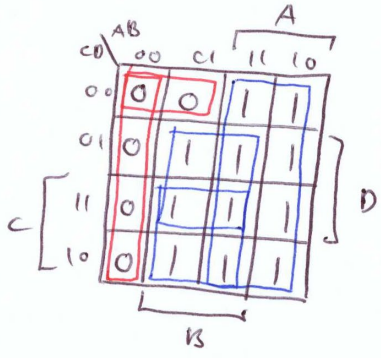
Can implement either one

Implement: $\bar{F} = \bar{X}(Y+Z) + YZ$



b. Use K-map to simplify the function:

$F = A\bar{D} + A\bar{B} + BD + BC$ (22 transistors)



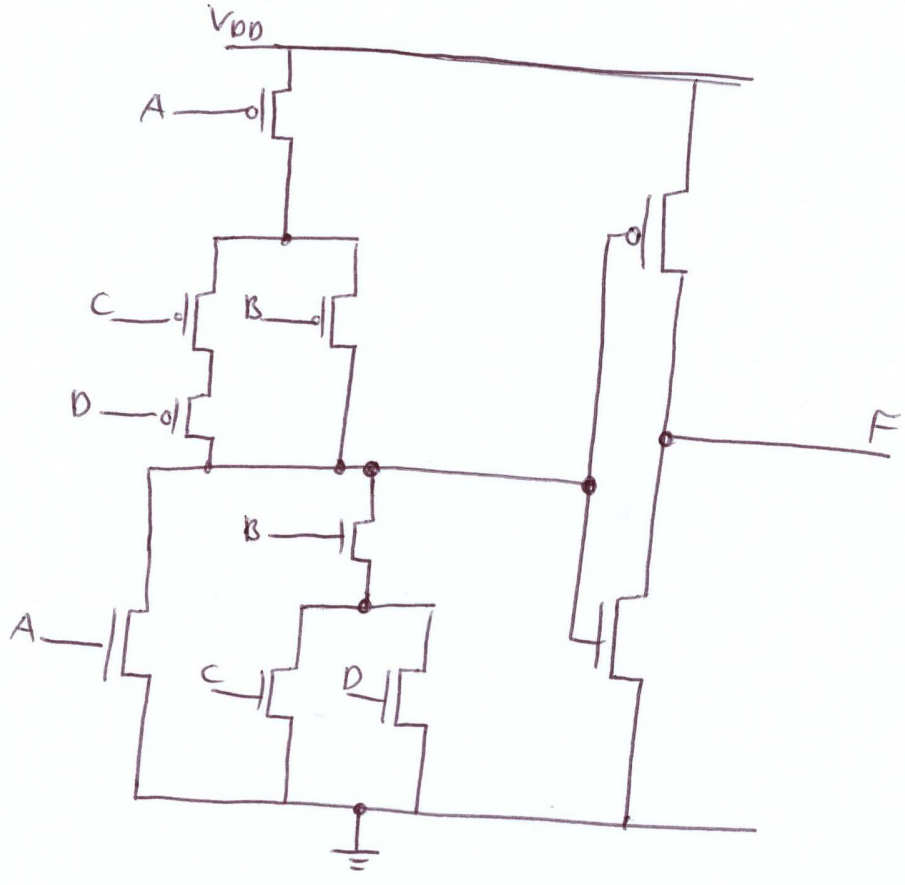
$F = A + BC + BD$ (12)

$= A + B(C + D)$ (10)

$\bar{F} = \bar{A}\bar{B} + \bar{A}\bar{C}\bar{D}$ (18)

$= \bar{A}(\bar{B} + \bar{C}\bar{D})$ (16)

So implement $F = A + B(C + D)$



10.

a. Try to minimize number of transistors:

$$F = (A+\bar{C})(\bar{A}+C)(B+\bar{D})(\bar{B}+D) \qquad (26)$$

$$= (AC + \bar{A}\bar{C})(BD + \bar{B}\bar{D}) \qquad (26)$$

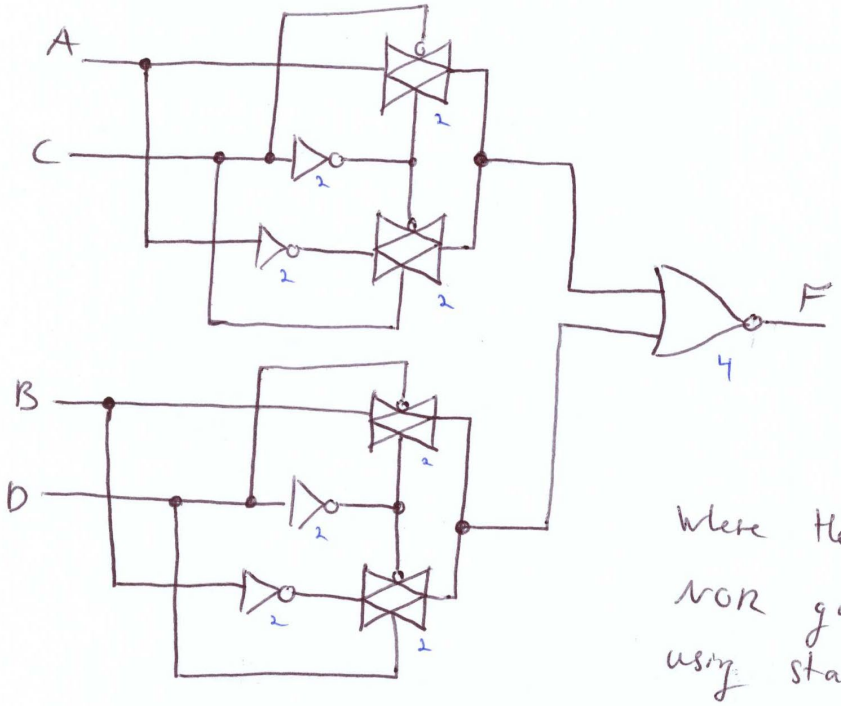
$$= \overline{(A \oplus C)}\ \overline{(B \oplus D)} \qquad (22)$$

using TG's.

$$= \overline{(A \oplus C) + (B \oplus D)} \qquad (20)$$

using TG's

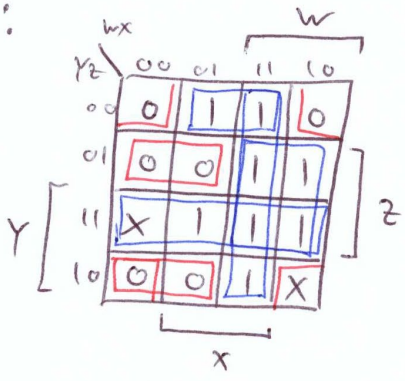
So implement: $F = \overline{(A \oplus C) + (B \oplus D)}$



(20)

Where the inverters and the NOR gate are implemented using standard CMOS.

b. Find an expression for F:



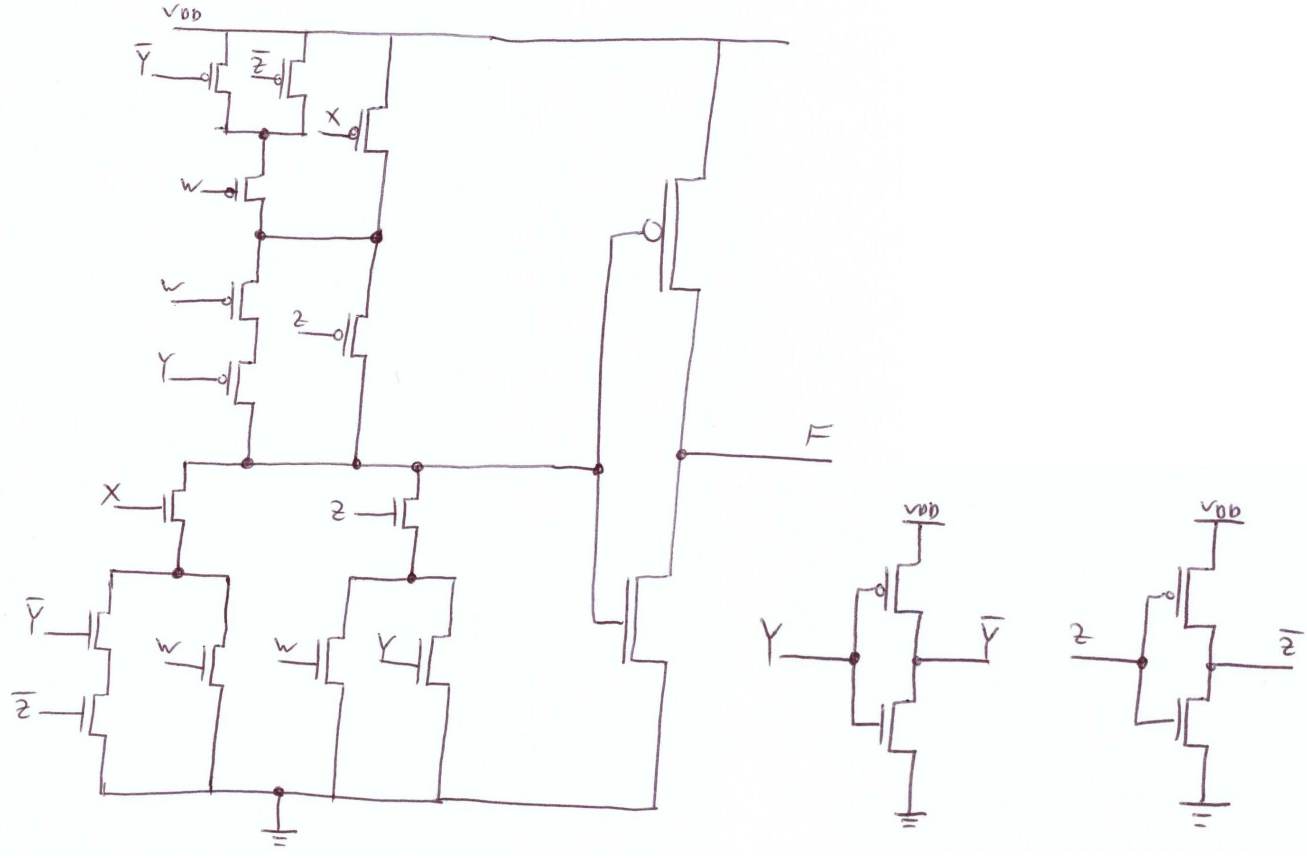
$$F = wx + wz + yz + x\bar{y}\bar{z} \quad (24)$$

$$= x(w + \bar{y}\bar{z}) + z(w + y) \quad (20)$$

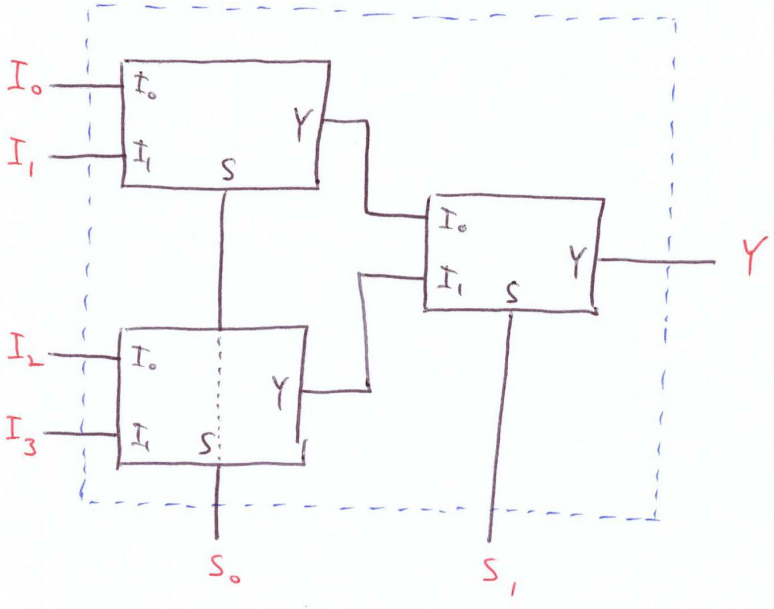
$$\bar{F} = \bar{x}\bar{z} + \bar{w}y\bar{z} + \bar{w}\bar{y}z \quad (24)$$

$$= \bar{x}\bar{z} + \bar{w}(y\bar{z} + \bar{y}z) \quad (22)$$

Implement: $F = x(w + \bar{y}\bar{z}) + z(w + y)$



11. A 4-to-1-Line Multiplexer can be implemented by cascading three 2-to-1 MUX in the following manner:



Each of the 2-to-1 MUX can be implemented using inverters and transmission gates: