ELEC2141
DIGITAL CIRCUIT DESIGN

Never Stand Still | Faculty of Engineering | School of Electrical Engineering and Telecommunications

ELEC2141 Laboratory Manual

2020

Student Name:

Student ID:

ELEC2141 Laboratory Manual

This laboratory manual contains all the information you need to complete your laboratory and gain lab marks, which go towards your assessment. It is hoped that you will find this manual informative, easy to read and of great use when completing the labs. Much information has been provided to assist you with the activities and to explain the phenomena which you will observe along the way. It is therefore imperative that you spend some time before your laboratory session to read up on what is required so as to make most of the time available in the lab. Lab demonstrators will be available to assist you with your work, however, it is normally expected that students will be able to complete the labs just by following the handbook and making sure they understand the information provided. It is expected that each lab exercise will take one lab session to complete. When you have completed the lab up to a checkpoint, you should add your name to the marking sheet so that the lab demonstrators can come and mark your work when they are ready. Be prepared to answer any additional questions which may be based on the material you have read prior to the lab. If you do not understand something, please ask. While working, it would be a good idea to save your work and keep a copy of it in case the demonstrators do not have the time to mark you in the class time allocated, or you need to refer to it in a later lab. Other necessary resources such as datasheets have been placed in appendices at the end of this manual as well as on the course webpage. Make sure that you refer to them while working.

Outcomes

The laboratory exercises are designed to enhance your ability in:

- Extracting and interpreting information from datasheets.
- Constructing combinational logic circuits with multiple inputs.
- Constructing circuits using sequential logic.
- Analysing and constructing Synchronous State Machines.
- Using an Integrated Development Environment (IDE) to program, simulate and implement circuits using FPGA hardware.
- Describing digital circuits using a hardware description language and implementing them on FPGA hardware

Overview

- Lab 1a – Introduction to digital circuits.
- Lab 1b – Introduction to Xilinx ISE and Digilent Nexys.
- Lab 2 – Comprehensive Guide to FPGA Programming.
- Lab 3 – Combinational circuit design problem
- Lab 4 – Flip-Flop Basics.
- Lab 5 – Sequential circuit Basics
- Lab 6 – Counters and 7-Segment Display
- Lab 7 – Electronic Handball Game
- Appendix A – Digilent Nexys 3 Board Reference Manual.
- Appendix B – Digilent Nexys 3 Board Schematic.
- Appendix C – 7400 Series Datasheets.

Discrete ICs Used in This Lab

- 7400 (SN74HC00) Quad 2-Input Positive-NAND Gates.
- 7414 (SN74HC14) Hex Schmitt-Trigger Inverters.
- 7474 (SN74HC74) Dual D-Type Positive-Edge-Triggered Flip-Flops.
- 7486 (SN74HC86) Quad 2-Input Exclusive-OR Gates.
- 7493(SN74LS93) four bit binary counter.
- 7447(SN74LS47) BCD-7 segment display decoder/driver

Laboratory Regulations

1. All laboratory users must undergo induction and agree to comply with laboratory rules, plus they should read any required safety manuals.

2. **No bare feet or exposed, open footwear (e.g. sandals) are permitted.**

3. Food and drink are not to be consumed at any time in laboratories.

4. Under no circumstance is the 240v 50Hz mains power to be used for any purpose other than that approved by the School. Only authorised personnel are allowed to alter power connections (50v above) or connect any equipment to mains power.

5. Tampering with or removal of laboratory equipment is strictly forbidden.

6. Data network connections should not be altered. Personal equipment may not be connected to the School data network without first seeking permission.

7. Personal mobile phones are not to be operated at any time within a laboratory.

8. Students are expected to conduct themselves in a reserved manner at all times. All noise is to be kept to a minimum.

9. **All bags should be stored under benches.**

10. Students should clean and tidy their workstations when they have finished and return all leads before leaving the laboratory.

11. Faulty equipment should be reported to laboratory staff who may not otherwise be aware of the problem.

2141 Laboratory Rules and FAQ

Are we working in pairs?

- Yes, choose a partner in the first lab session, and choose a bench. Stay with this partner and bench for the remainder of the semester.

What to bring to the lab:

- Closed shoes, you won't be allowed to enter the lab in thongs, sandals, etc.
- Your breadboard.
- The ELEC2141 component pack, collected from the workshop (G15).
- A printed and **bound** copy of the ELEC2141 lab manual, one per student.

What should I do before the lab?

- The ELEC2141 labs are demanding, **it is very important to read through the lab and complete the pre-lab quiz on Moodle before each session. Students will not be allowed to start the lab unless they have answered all the questions in the pre-lab quiz. Students will have unlimited attempts to complete the pre-lab quiz.**
  Going further than this, you can actually complete the work at home if you download the Xilinx package, and build your breadboard circuits before. There is a mark for finishing your work on time.
- Ask questions on the Moodle forum if you have any, demonstrators will respond to your questions there.
- Locate and read the datasheets for any ICs used in the lab.

You are encouraged to keep a backup of your files. If you use a USB-drive, please remember to take it with you at the end of the lab. Label your USB-drive with your name and student number, or place a file on the USB-drive so it can be returned to you in case you leave it behind.

- Plagiarism of any form is strictly forbidden. Although healthy student discussion of the laboratory material is highly encouraged**, any blatant copying of work will result in a zero mark for the entire laboratory component.**
- Support files for labs that require them will be uploaded on Moodle.

Marking Guideline

- **3 marks** for your lab work, the same mark will be given to you and your partner.
    - Demonstrate it works to us, and works as it should for up to **3 marks.**
    - If you are assessed the week after the lab is due, this will be capped at **2 marks**.

- **2 marks** based on your response to questions, individually assessed.
    - Demonstrators will ask you each 2 questions, and will assign up to **1 mark** per question based on the quality of your response. Demonstrators need to limit the amount of time they allow you when answering questions.

What are the rules at marking time?

- There is a lab schedule that we will adhere to; Lab 1a and 1b will start in Week 3, Lab 2 in Week 4 and so on.
- You may place your group's names and bench number down on the marking sheet up until the last 15 minutes of the lab session; the sheet will be closed off at 15 minutes to the hour.
- If you run out of time and are not marked, you may place your group's details down on the sheet within the **first 15 minutes** of next week's lab. This is known as the grace period and only applies to the previous week's labwork.
- To recap, if you want to be marked for lab **n** you should write your details on the marking sheet:
    - In the week lab **n** is scheduled, at least before the last 15 minutes of the lab session.
    - In the week following lab **n**, in the first 15 minutes of the lab.
- Once a demonstrator arrives at your bench to mark you, it's marking time. Requests for demonstrators to "come back later" won't be entertained.

Using VMWare in the Labs

In the labs, we will be using Xilinx 13.1, a legacy software that is unstable when run on Windows 10. Therefore, Windows 7 will need to be run via virtual machine to use Xilinx 13.1 in the labs. Please be aware that any files saved on newer versions versions of Xilinx will not be comptible with Xilinx 13.1.

1. Launch **VMWave Workstation 15 Player** from Desktop or Start Menu.
2. Launch **Windows 7 x64 - Xilinx 13.1** from the VMWare window.
3. Select **Remind me later** when prompted on software updates.
4. Wait for Windows 7 to boot before proceeding with the steps in labs requiring Xilinx 13.1.

When using USBs:

1. Select **Connect to a virtual machine** on the pop up window.
2. Select **Windows 7 x64 - Xilinx 13.1**.

It is recommended that you work from USBs as the files left on the virtual machine may not be there the next time you use the computer. You may also use online cloud storage or email to back up your lab files.

Due to the unstable nature of Xilinx 13.1 on Windows 10, students are encouraged to turn up to other lab sessions and use any unoccupied benches to work on lab tasks. Please let the lab demonstrators know if you would like a Digilent Nexys 3 Board to work with in the lab.

Lab 1a – Introduction to Digital Circuits

In this laboratory, you will be introduced to

- Breadboard
- Generating inputs for digital circuits using binary counter
- Displaying digital outputs from digital circuits on the oscilloscope
- Digital IC circuits, datasheets for the IC circuits, constructing basic logic circuit and experimentally verifying their operation.
- Measuring propagation delays in digital logic gates

Introducing Your Breadboard

Your breadboard is essentially a set of wires which have been arranged into a pattern to allow easy solder-less prototyping of circuits. By slotting devices and wires into the holes, you can make connections between terminals. The breadboard is internally connected as follows:

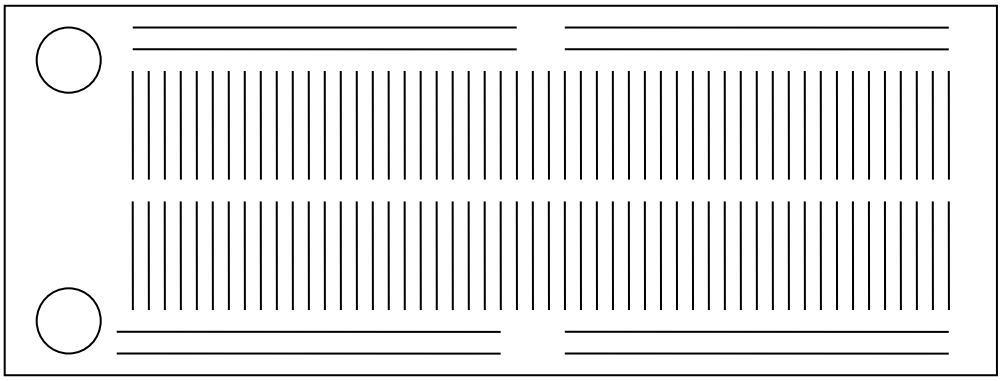


Figure 1.1: Schematic illustration of internal connection of breadboard

We normally prefer that you hold the board as shown in the above orientation. The two circles represent banana sockets or binding posts which are used to supply power to the board. The eight horizontal strips are called *buses*. Wires and components are simply put into the respective holes to make the appropriate connections and can be removed and replaced as many times as you like. Integrated circuits (*ICs* or *chips*) are placed across the break that runs through the centre – so they straddle the gap that runs across the middle of the board.

Preparing Your Breadboard

If you have just purchased a new breadboard, there are a few things which you might have to do to get it ready for use. If your breadboard was supplied with banana sockets or binding posts, these should be securely fitted to the board first. Then, these should be connected by a short piece of wire to the buses on your breadboard. You may also choose to prepare some more short pieces of wire to complete your buses. Usually the positive rail (normally coloured red) is at the top and the negative rail (normally coloured black) is at the bottom. Your board should look like this when it is prepared.

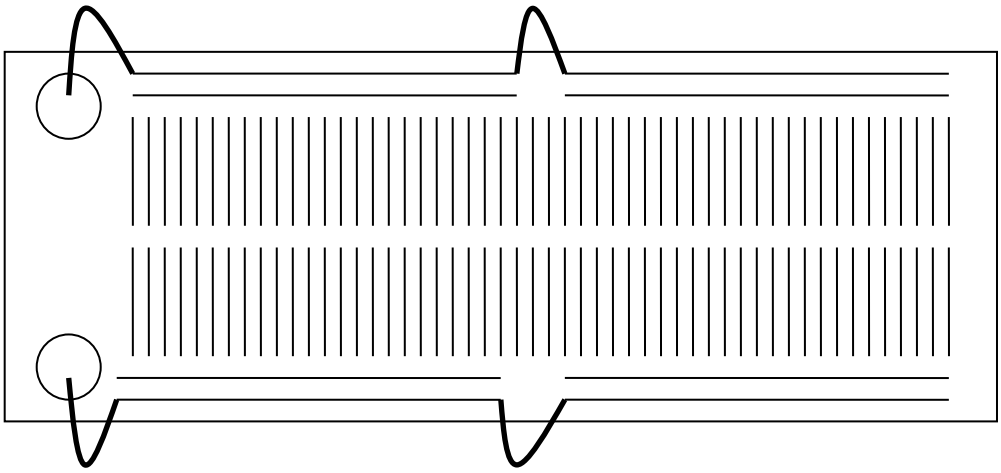


Figure 1.2: Connecting positive (VCC) and negative (GND) rails on the breadboard

General Construction Hints

When building circuits on breadboards, please make sure you do the following:

- **Colour code your wires.** Use standard colours – red for **Vcc**, black for **GND**, blue for inputs, yellow for outputs and green between chips. It will make troubleshooting a lot easier.
- **Keep wires as short as possible** so that they stay close to the breadboard. This makes storing your circuit easier as well as the wires are less likely to be pulled off in transport.
- **Be careful when stripping wires** – avoid stripping too much off the end of the wire as this will leave exposed wire that could be a source of short circuits later on. Try not to press too hard on the tool when stripping or the wire may snap when you insert it into your breadboard.

- **Think ahead** and try to construct the circuit in a smaller area of board. This may make it easier for you to troubleshoot and maintain your design as you won't have wires going everywhere.
- **Take care when handling integrated circuits** – most integrated circuits are static sensitive and can be damaged by static charges accumulated by your body from your clothing and from walking around. Before handling integrated circuits, touch a large piece of grounded metal such as a computer chassis and avoid handling the pins of the IC. Furthermore, the pins on the IC are fragile, it is recommended you store them with care and leave them plugged into your breadboard while in transit.

What are Integrated Circuits (Ics)?

Integrated Circuits (*ICs*), commonly known as *chips* or *microchips*, are electronic devices that contain a miniaturised circuit etched onto the surface of a thin substrate of semiconductor material, such as Silicon. It allows for complex circuits to be built into small packages, reducing their size, as well as enabling faster operation and lower power consumption.

The basic mechanism of a digital circuit lies in the ability to turn an output on and off. Since the invention of the transistor, this can be done using solely transistors and other discrete passive elements. However, building these circuits for fundamental logic operations is repetitive, tedious and inefficient. The diagram below shows one possible implementation of a 2-input inverted AND gate:

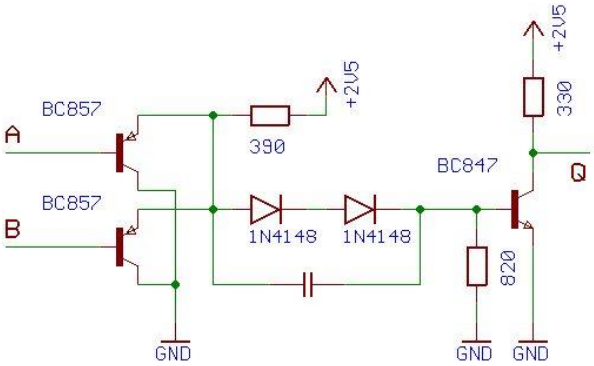


Figure 1.3: Transistor level implementation of 2-input inverted AND gate

A few of these gates would have occupied an area of around the size of a business card if constructed using individual discrete components. However, hundreds of these circuits can be manufactured into an IC which is the size of a coin. This fact alone allows great reductions in the size of finished circuits.

Figure 1.4: IC chip and a coin

7400 Series

The cost of the production overheads to manufacture just a single gate in its own package is quite high. Therefore, it is not feasible to manufacture packages containing individual gates, but rather IC packages with several gates of the same type in them. The *7400 digital logic series* of ICs features such a collection of commonly used logical functions and some special purpose devices. These ICs are readily available from hobbyist electronics supply stores such as Jaycar or Farnell.

Each member of the 7400 series is identified by a part number beginning with the digits 74, followed by the type number. For example, *7400* is type 0 of the 7400 series and it is a Quad 2-input NAND gate; *7427* is type 27 of the series and it is a Triple 3-input NOR gate, and *74118* is type 118 of the series and it is a Hex Set/Reset Latch.

Each type may be made up of multiple gates of the same type. For example, a Quad 2-input NAND gate has four distinct 2-input NAND gates available while a Hex Inverter has six inverter gates available.

A single type of IC may also come in a different speed or power consumption level. This is indicated by the letters between the family prefix, 74, and the part

number. For example, *74LS00* indicates a low power Schottky version of 7400 while *74HC00* indicates a high speed CMOS variant.

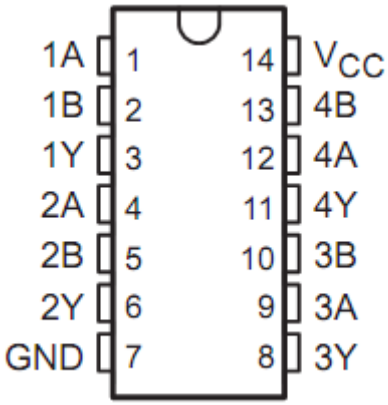
The following table shows a list of just a few of the most commonly used types of ICs in the 7400 series:

PART NUMBER	FUNCTION
7400	2-input NAND Gates
7402	2-input NOR Gates
7404	Inverter
7408	2-input AND Gates
7432	2-input OR Gates
7474	D-Flip-Flop
7486	2-input XOR Gates
74157	1-bit 2-1 Multiplexer
74192	Decade Counter
74193	Binary Counter

Table 1.1: List of few typically used ICs

Packaging

The following diagram shows the pin-out of the 7400 Quad 2-Input NAND IC:



FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

Figure 1.5: Pin configuration for 7400 Quad 2-Input NAND and its functional table

The truth table may not be in a format that you are normally accustomed to, using logic 0s and 1s – this is because it is written in terms of voltage levels. *H* stands for a High level voltage (typically 5v) which is equivalent to logic 1,

whereas *L* stands for Low level voltage (typically 0v) which is equivalent to logic 0. An *X* symbol stands for *don't-care* which can be either a 0 or a 1.

The pinout diagram above indicates the following:

- **Notch (or sometimes a dimple)** – This helps you orient the IC and locate Pin 1.

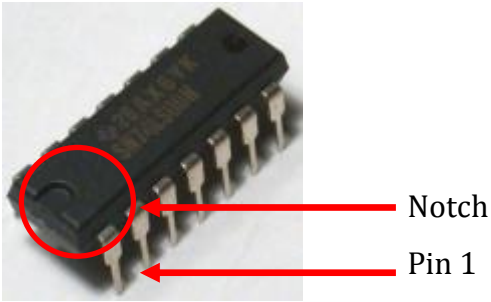


Figure 1.6: Picture of IC showing the Notch and pins

- **Vcc** – This is the positive power supply rail (typically 5v).
- **GND** – This is the negative power supply rail (typically 0v).
- **Pin Labels** – This indicates the inputs and outputs of the logic gates – the number indicates which pins belong to which logic gate and the letters represent the input and outputs as shown in the truth table.

The diagram below graphically represents how the gates within the IC are connected to the pins.

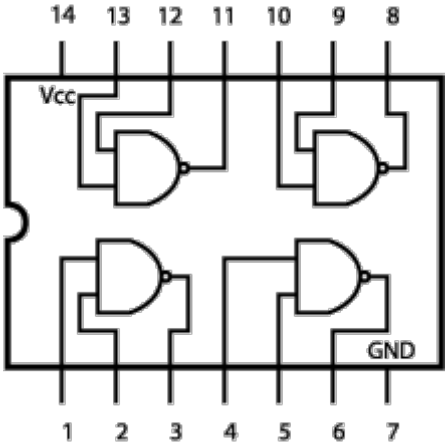
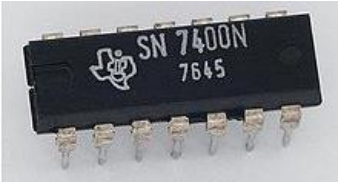
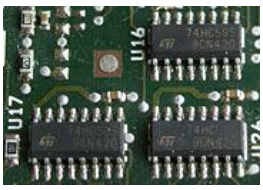


Figure 1.7: Gates connection to the 7400IC's pins

Each type of 7400 series IC may have different number of pins – a 7400 has 14 pins while a 7476 has 16 pins. However, the ICs from this series all come in standard packages such as the *Dual Inline-Package* (*DIP*) or *Small Outline*

Package (*SOP*) as shown below. This allows for easy prototyping on breadboards and populating onto printed circuit boards.





Dual-Inline Package (DIP) *Small Outline Package (SOP)*

Figure 1.8: DIP and SOP Packages

There are other types of standard IC packages such as Quad Flat Package, Quad Flat No-lead, Grid Array, Ball Grid Array and Low Insertion Force Socket. The package type is usually chosen by the manufacturer based on circuit requirements, size, cost of production and ease of population.

Datasheets

A *datasheet* is a document summarising the performance and other characteristics of a component (e.g. an electronic component), a sub-system (e.g. a power supply) or software in sufficient detail to be used by a design engineer to design the component into a system. Typically, a datasheet is created by the component manufacturer and begins with an introductory page describing the rest of the document. This is followed by listings of specific components, with further information on the connectivity of the devices and their nominal performance parameters and operational conditions. In cases where there is relevant source code to include, it is usually attached near the end of the document as an appendix or separated into another file.

An example of information which a datasheet may provide includes packaging, pin layout, functionality, speed, power dissipation and operating conditions. See the sample datasheets provided in Appendix C.

Basic Logic Gates

It can be shown that any logic function can be implemented using NAND gates only. A NAND gate is simply an AND gate with its output inverted. In this lab, we will implement AND gate, XOR gate, and three input NAND gate using two-input NAND gates, and verify their operations.

Producing Inputs to Digital Logic Using Binary Counter

Digital logic is often thought to be a binary state – either a *1* or a *0*, a *high* or a *low*. The inputs to a digital circuit, however, are usually analog voltages which are continuously variable. Commonly, a 1 is represented by a high voltage (e.g. close to **Vcc** – the supply voltage) and a 0 as a low voltage (e.g. close to **GND** – the ground rail voltage). In order to produce some input to our IC, we have to alter the voltages going to the inputs of the IC. Although slide switches and bush-button switches can be used as a typical ways of generating digital input signals, we will look at the use of binary counter as digital input signal generator in this laboratory exercise.

Binary Counters

Later in the course, you will learn how to design counters. For now we only need to know what they do and how to configure them for proper operation. Figure 1.10 shows a schematic diagram and connections for 7493 IC as a four-bit counter. The counter is driven by either a push-button pulser or a clock. The digital outputs of the counter are $Q_A, Q_B, Q_C,$ and $Q_D$with Q_A and Q_D being the least and most significant bits, respectively. At the arrival of each pulse or clock, the counter increments by one until all digital outputs are HIGH (15) and then reset back to the state where all the digital outputs are LOW (0). This pattern repeats with continuous application of pulse or clock. Table 1.2 shows the digital output pattern of the counter as it counts from 0 to 15. As can be seen from the table, the counter can be used to generate all input combinations required for testing combinational circuits with upto four inputs.

Note that the connection of Q_A to ClkB and either R1 and R2 be low is required so that a four bit binary counter is achieved. The counter can be reset to zero at anytime by applying HIGH to both R1 and R2 at the same time.

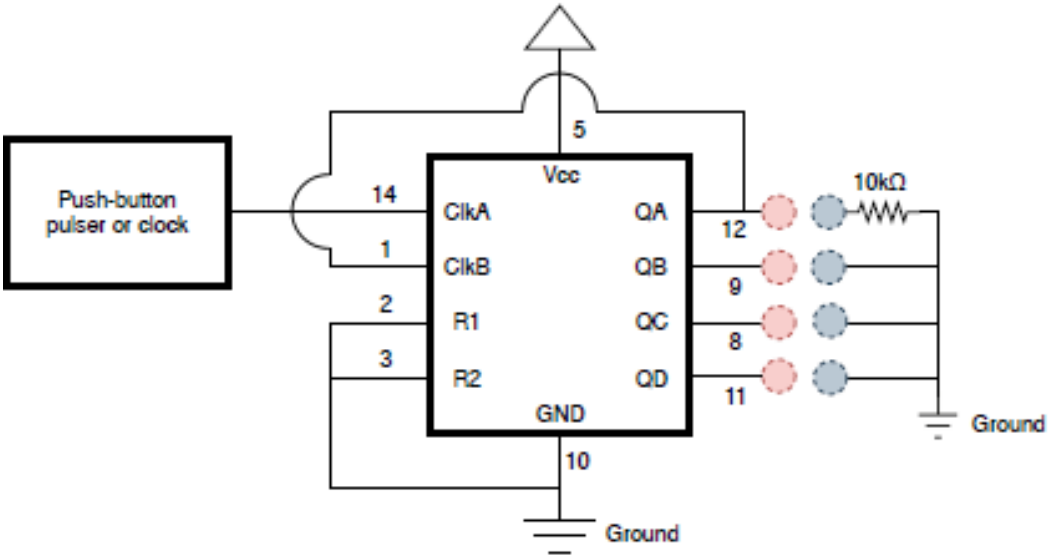


Figure 1.9: SN74LS93 wired up as binary counter with oscilloscope probe. Connect the positive probe of the oscilloscope to the output of the counter and negative/ground probe to the Ground.

	Q_D	Q_C	Q_B	Q_A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

Table 1.2: Digital input patterns that can be generated by a four bit counter

You may also note from Table 1.2 that at a given clock frequency QA varies twice as frequent as QB, four-times as frequent as QC, and eight-times as frequent as QD.

Displaying Output from Digital Logic

The output of the IC is a voltage – either high or low. But how can we visualise this so we know what is happening? You could measure the voltage with a voltmeter or plot the output on an oscilloscope or we can show the output on a *Light Emitting Diode* (*LED*). In this lab, we will be using an oscilloscope to display digital output waveforms from the counter and digital logic circuits.

Laboratory Procedure

1. Construct a four bit binary counter on your breadboard using SN74LS93 IC as shown in Figure 1.9. Make sure that i) Q_A (Pin 12) and Clk B (Pin 1) are connected; (ii)Pin2 (R1) and Pin3(R2) are set to LOW by connecting them to GND (pin 10); GND is connected to the negative rail of your bread board.;(iii) Connect pin 5 to the positive rail of your breadboard ; (iv) connect pin 14(ClkA) to TTL/CMOS output port of the signal generator; (v) Connect your breadboard to the bench-top power supply by using the supplied leads in the laboratory. Use the fixed 5v output on the right-hand side of the power supply.
2. In order to reduce noise and interference on the power supply as well as ensure a stable voltage level, large capacitors, in the order of 10μF – 100μF are often placed across the power supply rails as illustrated below. This is a common practice in all forms of electronics and one which students are encouraged to follow. Therefore, connect the supplied 100μF capacitor as shown in Figure 1.10 Make sure you place the capacitor in the right orientation with respect to its polarity!

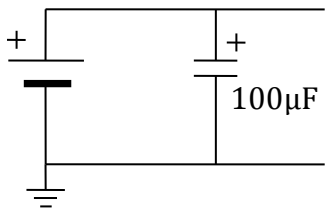


Figure 1.10: Connecting 100μF across the positive and negative rails.

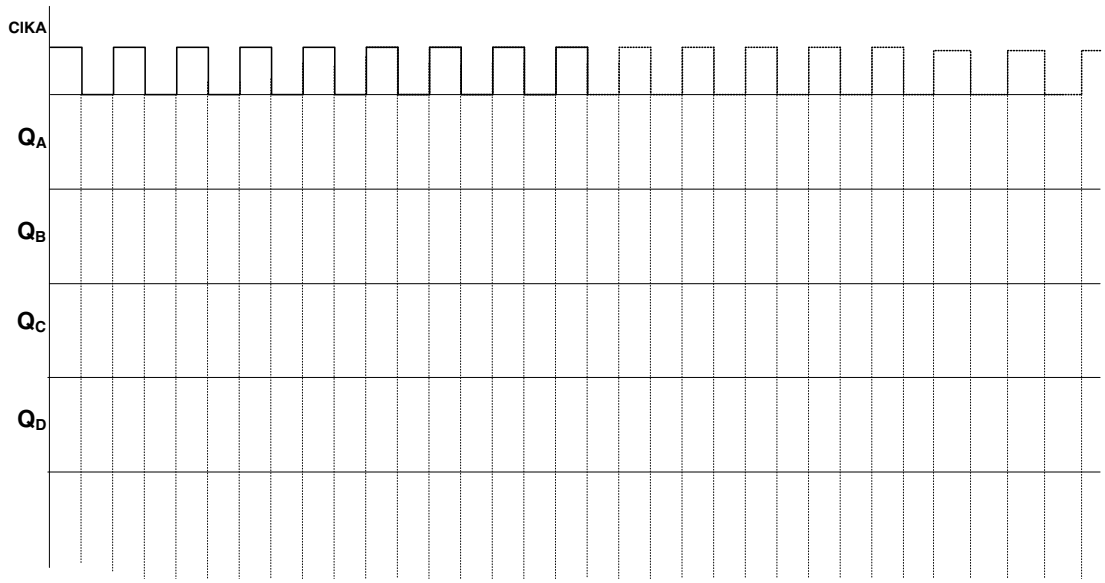


Figure 1.11: Waveform recording chart for procedure 4-7

3. Switch on the power supply.
4. Display the clock signal from the signal generator (on CHANNEL 1) and the Q_A output from the binary counter (on CHANNEL 2) at the same time on the oscilloscope. Plot the signals displayed on the oscilloscope. You may use Figure 1.11 to record the displayed signals. What is the frequency relationship between the two signals?
5. Display the Q_A output from the binary counter (on CHANNEL 2) and the Q_B output from the binary counter (on CHANNEL 1) at the same time. Plot the signals displayed on the oscilloscope and establish the frequency relationship between them. (use Figure 1.11 for the plot)
6. Repeat step 5 for Q_A and Q_C. (use Figure 1.11 for the plot)
7. Repeat step 5 for Q_A and Q_D. (use Figure 1.11 for the plot)
8. If the constructed four bit counter is working properly, keep it as you will need to show to the demonstrator later on and for the next procedures.
9. Construct the following logic function with four inputs (A, B, C, D) using the NAND gates available in SN74HC00 IC. Make sure that pin 7 and pin 14 of SN74HC00 are connected to GND and VCC, respectively.

$$y = AB + CD$$

10. Verify the correct operation of the logic function constructed in step 9. For the verification, use the binary counter outputs (Q_A, Q_B, Q_C, Q_D) as inputs to the logic circuit and display Q_A (on CHANNEL 1) and y (on CHANNEL 2)

on the oscilloscope. Record the resulting waveforms in Figure 1.12.

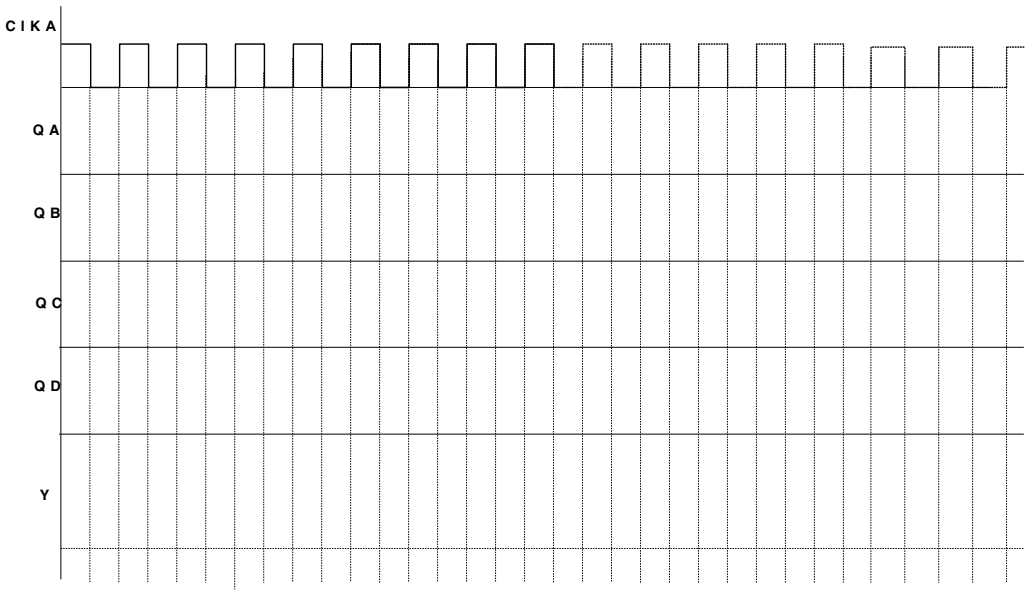


Figure 1.12: Waveform recording chart for procedure 10

11. *(If you do not have time, you may skip this procedure) Connect the six inverters inside SN74HC14 IC in cascade. Apply a clock signal at a frequency of 1MHz to the input of the first inverter. Display the clock signal (on CHANNEL 1) and the output signal from the sixth inverter (on CHANNEL 2) on the oscilloscope at the same time. The two signals are similar except that one is the delayed version of the other. Change the time division scale to the lowest possible and measure the delays at upswing and down swing of the signals. Divide the measured delays by six to obtain the upward and downward propagation delays in each inverter.

Checkpoint 1a	*Assessor*	*Marks (5)*	*Date*

— CONTINUE TO LAB 1B —

Lab 1b – Introduction to Xilinx ISE and Digilent Nexys 3

Important Note: Please read Page 6 before commencing this lab task in the labs.

In this lab, we will be introduced to

- the Digilent Nexys 3 development board equipped with a Xilinx Spartan-6 FPGA. The term *FPGA* stands for *Field Programmable Gate Array*. FPGAs are programmable ICs which incorporate a large number of logic blocks and interconnects which can be electronically switched (programmed) so as to wire up the logical blocks together in a certain way in order to perform the function of a circuit normally involving many logic gates and flip-flops. We can thus produce any circuit that is a combinational or sequential function solely with an FPGA. There are many types of FPGAs in the market, each differ in electrical and physical characteristics such as speed, capacity and power consumption. The Digilent Nexys 3 development board offers numerous I/O interfaces integrated onboard, which makes it ideal for an introductory course such as this one.
- how to download a program to the FPGA
- how you can create the schematics of your digital circuit design (combinational circuit for now) using Xilink ISE.
- how you can simulate the operation of your digital circuit design using Xilink ISE.
- designing combinational circuits using logic gates from a minimized boolean function, and functional blocks such as multiplexer and decoder

Downloading a Program to the FPGA

Downloading a program to the FPGA is very similar in principle to installing and running an application on a computer. However, instead of an application, we will take a pre-compiled design, load it and run it on the development board.

Begin by locating **Labfiles\lab2\directio.bit** from Moodle page of the course. Copy this file into your personal USB-drive. Also ensure that you have a Digilent Nexys 3 board plugged to your computer before continuing. On your Digilent Nexys 3 board, locate the power switch (next to Adept USB port)

and toggle the switch to the on position. The LEDs should light up indicating that the board is ready for use.

Start **Adept** from the **Start** menu by selecting:

Start → All Programs → Digilent → Adept → Adept

You should see the following screen:

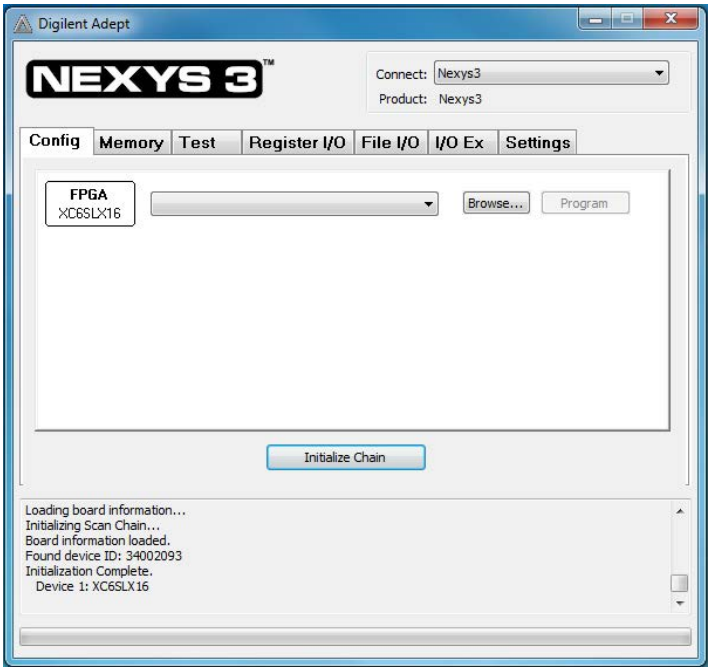


Figure 2.1: Digilent Adept window

Click **Browse…** to the right of the FPGA chip and locate **directio.bit**.

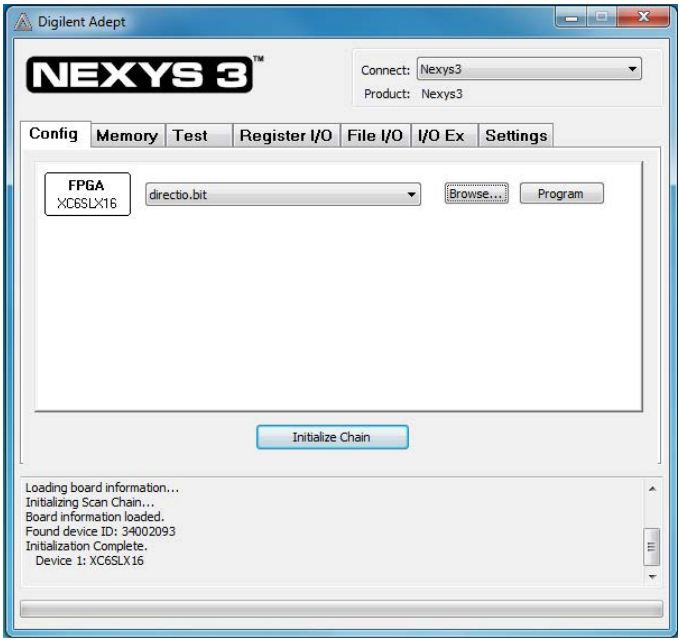


Figure 2.2: Digilent Adept window with a bit file selected

Click on the **Program** button. This will start transferring the bit-file onto the board. During this process, be careful not to disturb the board.

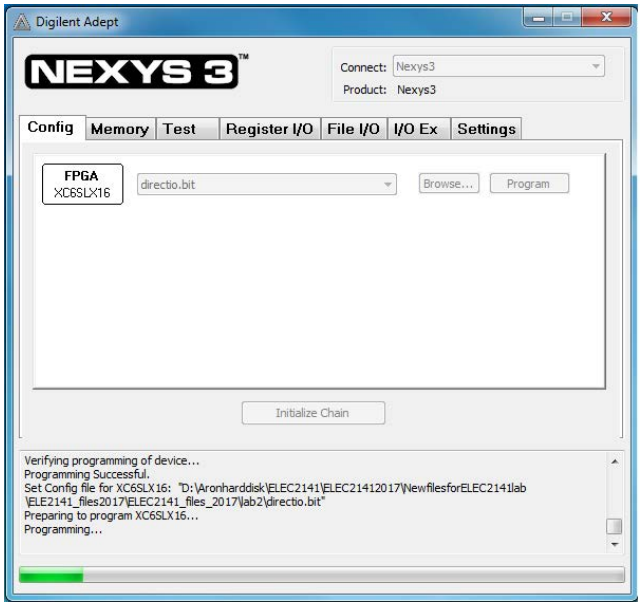


Figure 2.3: Digilent Adept window programming the bit file onto the FPGA

Once this is complete you will see **Programming Successful** in the status box.

Your board is now loaded with a program that does the following:

- The switches turn on the corresponding LEDs (e.g. **SW0** turns on **LED0**).
- The push-buttons turn on the 7-segment displays. (e.g. **BTNL** turns on the leftmost 7-segment display, showing an '8' figure).

Test that all of the switches and buttons work by toggling them on and off. If your board does not behave as expected, ask a demonstrator for help.

Downloading another Program to the FPGA – Your Turn

Turn all eight switches to the off position. This time, copy the eleccool.bit (**Labfiles\lab2\eleccool.bit**) file from Moodle to your personal USB-drive and download it onto the FPGA in a similar way to the previous example.

Question: What do you see on the 7-segment display?

Drawing a Schematic in Xilinx

The Adept utility is only used to download compiled logic designs onto the FPGA. In order to create and build new designs, we need to use Xilinx ISE. In this lab, we will design and implement a combinational circuit with the following specification:

Design Specification

A small company is owned by four peoples (Mr. W. Mr. X, Mrs. Y, Mr. Z) and has a total of 10 shares of stock. Each share entitles its owner one vote at a stockholder's meeting. A motion is passed at the stockholder's meeting if it receives a majority vote (that is five or more votes). The 10 shares of stock are distributed among the owners as follow:

Mr. W has one share

Mr.X has two shares

Mrs.Y has three shares

Mr. Z has four shares

Each owner has a switch at the stockholder's meeting to cast their vote on a motion. When a motion is passed, a lamp is switched on.

In implementing and testing the combinational circuit that has the specifications as presented above, we use SW0, SW1, SW2, and SW3 on the Digilent Nexy board as input switches for Mr W, Mr.X, Mrs.Y, and Mr.Z, respectively, in the stockholder's meeting and LED0 as the lamp (output) that indicates if the motion is passed.

Before we start creating this project on Xilinx, programming it on the FPGA and finally testing it, let us translate the specification into a truth table and obtain a Boolean function .

	W	X	Y	Z	Total vote	Motion passed (P)
0	0	0	0	0	0	0
1	0	0	0	1	4	0
2	0	0	1	0	3	0
3	0	0	1	1	7	1
4	0	1	0	0	2	0
5	0	1	0	1	6	1
6	0	1	1	0	5	1
7	0	1	1	1	9	1
8	1	0	0	0	1	0
9	1	0	0	1	5	1
10	1	0	1	0	4	0
11	1	0	1	1	8	1
12	1	1	0	0	3	0
13	1	1	0	1	7	1
14	1	1	1	0	6	1
15	1	1	1	1	10	1

Table 2.1: Truth table for the design specification

The Boolean function can be written as the sum of minterms

$$P = \sum m(3,5,6,7,9,11,13,14,15)$$

The above Boolean function can be realized

a) **Using logic gates**: for this the Boolean function will have to be minimized. K-map can be used for this purpose. A four variable K-map is drawn for P

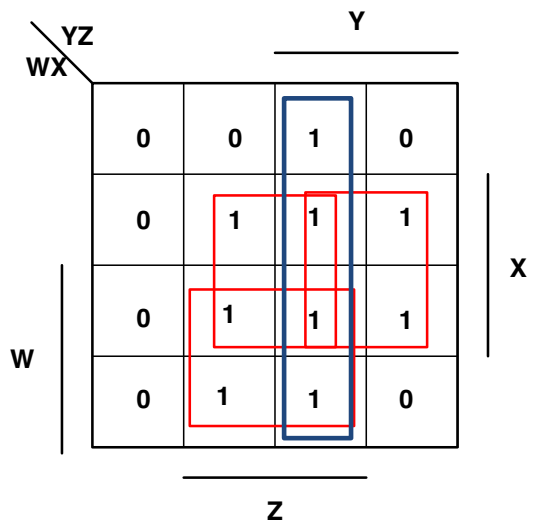


Figure 2.4: K-map for P

$$P = WZ + YX + ZX + YZ$$

Further minimization can be achieved by factorization.

$$P = Z(W + Y) + X(Y + Z)$$

Now, we can implement the minimized Boolean function using AND and OR logic gates as follows:

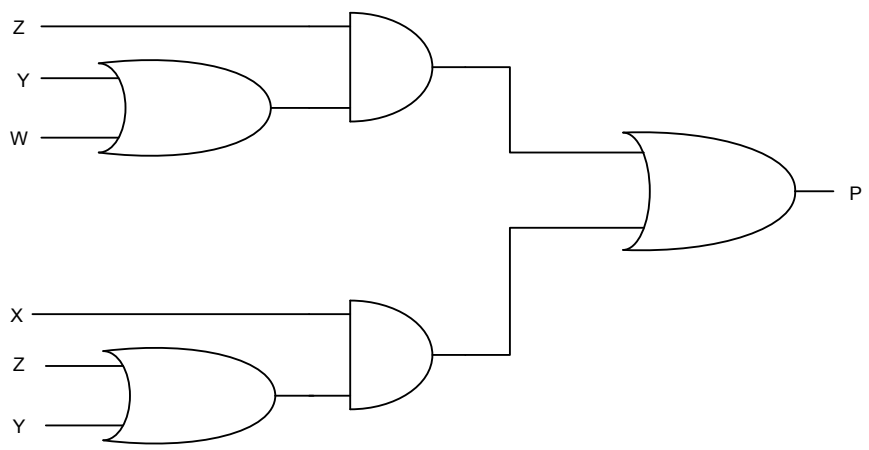


Figure 2.5: Realization using AND and OR logic gates

b) **Using multiplexer**: Since we have four inputs, we will have to use 8-to-1 multiplexer with three select lines. When a Boolean function is implemented using multiplexer, we do not need to minimize the function. However, we need to choose which inputs to be applied to the select lines. From the truth table provided in Table 2.1, it will make sense to choose W,X,Y as select lines and apply either 0, 1, Z or $\overline{Z}$ to each of the eight input

line to realize the Boolean function. This can be seen from the re-plotted truth table in Table 2.2.

	Select lines				Output	Inputs
	S_2	S_1	S_o			
	W	X	Y	Z	P	
0	0	0	0	0	0	$M_o = 0$
1	0	0	0	1	0	
2	0	0	1	0	0	$M_1=Z$
3	0	0	1	1	1	
4	0	1	0	0	0	$M_2=Z$
5	0	1	0	1	1	
6	0	1	1	0	1	$M_3 = 1$
7	0	1	1	1	1	
8	1	0	0	0	0	$M_4 = Z$
9	1	0	0	1	1	
10	1	0	1	0	0	$M_5=Z$
11	1	0	1	1	1	
12	1	1	0	0	0	$M_6=Z$
13	1	1	0	1	1	
14	1	1	1	0	1	$M_7 = 1$
15	1	1	1	1	1	

Table 2.2: Modified truth table for multiplexer realization

The realization of the truth table using the 8-to-1 multiplexer is shown in Figure 2.6 below

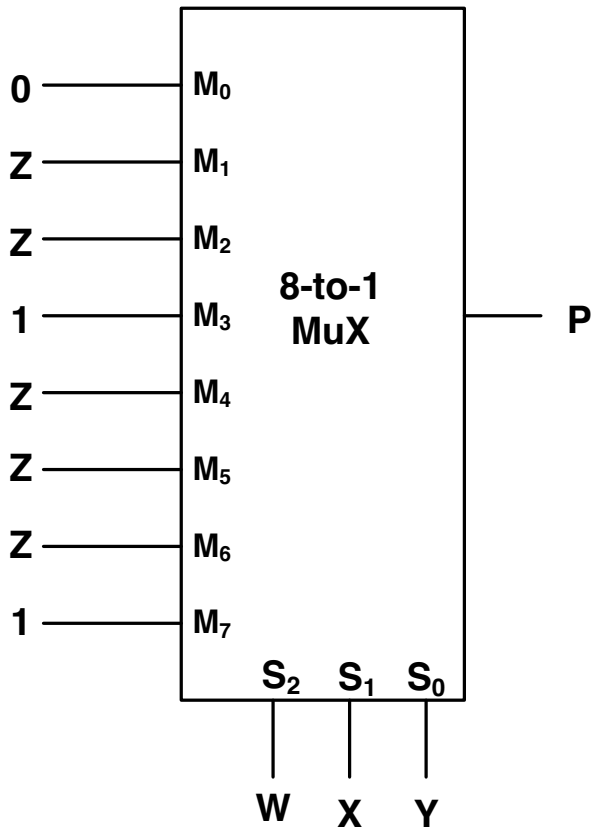


Figure 2.6: Realization using multiplexer

c) **Using decoder and multiple input OR gates**: Each output of the decoder represents a minterm of the inputs. Since the Boolean function has four inputs, we need to use 4-to-16 decoder for the realization and each of the minterms in the Boolean function can then be ORed together. Since the Boolean function has nine minterms, an OR gate with nine inputs can be employed. The figure below shows the realization of the Boolean function using a 4-to-16 decoder and a nine input OR gate.

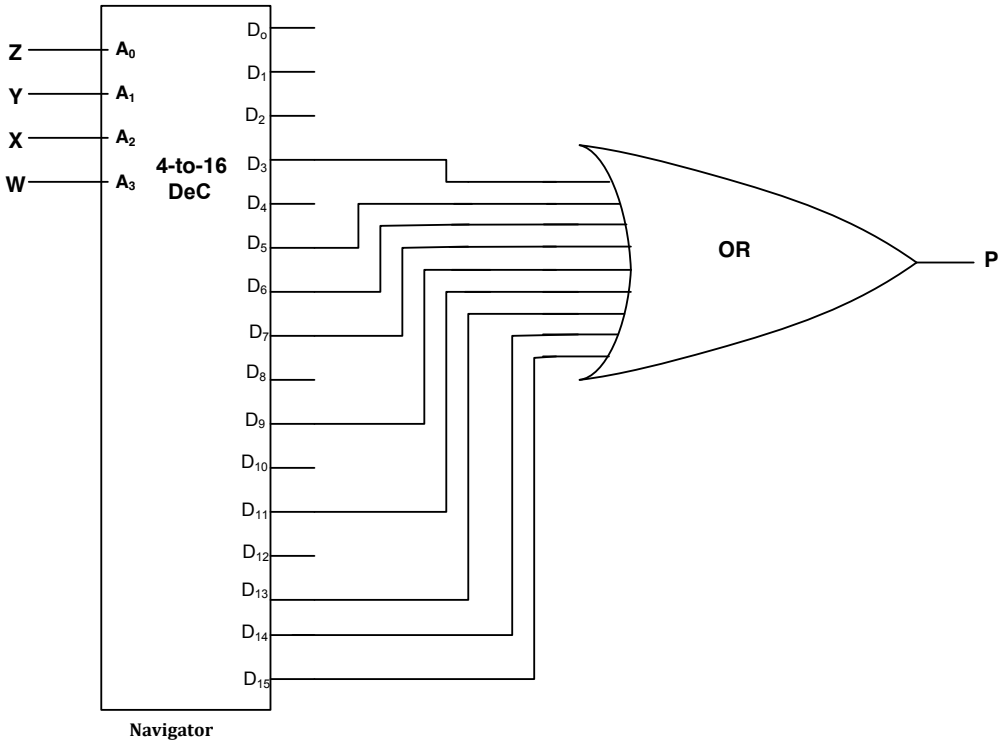


Figure 2.7: Realization using decoder and nine input OR gate

We are going to implement the realization in Figure 2.5 with **SW0 (Z), SW1 (Y), SW2 (X), and SW3(W)** as inputs and **LED0** as the output.

Start Xilinx ISE from the start menu by selecting 64-bit Project Navigator

Start → All Programs → Xilinx ISE Design Suite 13.1 → ISE Design Tools → Project

Now we need to create a new project. To do so:

1. Select **New Project from File → New Project**; the **New Project Wizard** appears.
2. Enter in **Project Location**. The **Working Directory** field will be filled out for you automatically. Please avoid creating projects under **My Documents** on the lab computers as the files may be deleted on the next system start-up . Optionally enter a description for your project.
3. Type **Votecircuit1** in the **Project Name** field.
4. For this project, choose **Schematic** as the **Top-Level Source Type** list.

5. Click **Next** to move to the device properties page.
6. Fill in the properties in the table as shown below:
    - Product Category: **All**
    - Family: **Spartan6**
    - Device: **XC6SLX16**
    - Package: **CSG324**
    - Speed Grade: **-3**
    - Top-Level Source Type: **Schematic**
    - Synthesis Tool: **XST (VHDL/Verilog)**
    - Simulator: **ISim (VHDL/Verilog)**
    - Preferred Language: **Verilog**
    - Leave all other boxes at default settings.

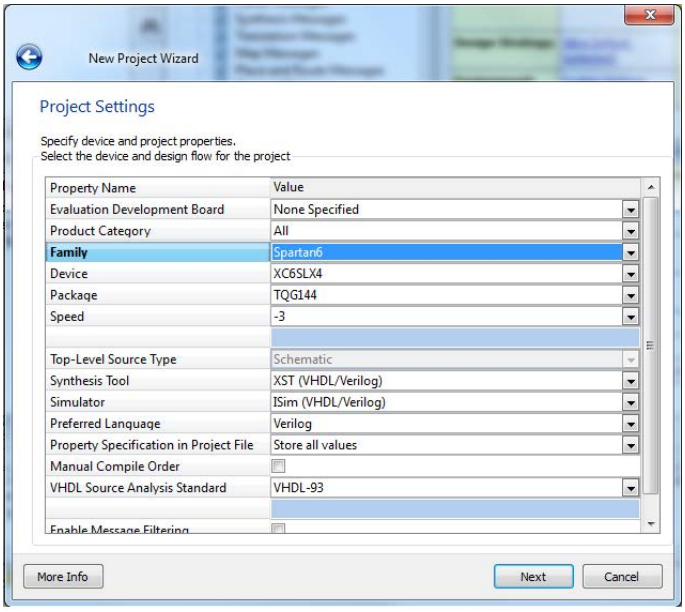


Figure 2.8: New project wizard window for device properties

7. Click **Finish**.

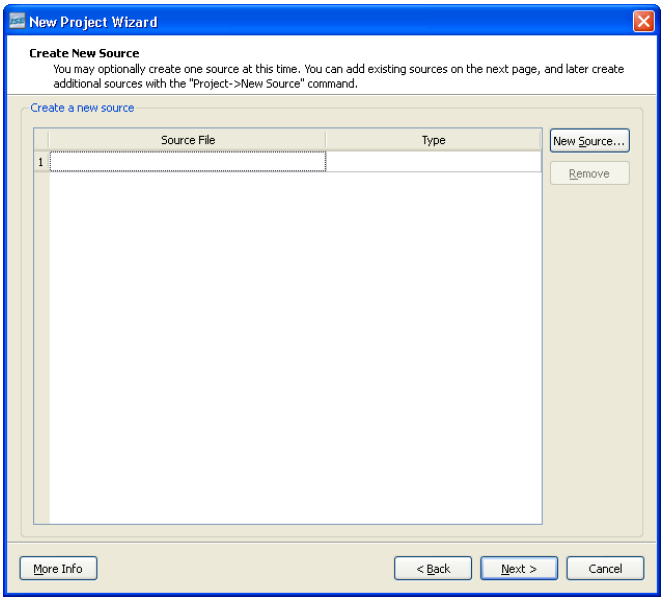


Figure 2.9: New Project Wizard window for Create New Source

To create a blank top-level schematic:.

8. **Right click** on xc6slx16-3csg324 under the Hierarchy tab at top left hand side of the screen. Select **New Source**
9. Select **Schematic** as the source type.
10. Type in the file name **Voteciruit1** (same as the project name).
11. Verify that the **Add to project** checkbox is selected.
12. Click **Next** and then click **Finish**

On the upper left-hand side of the screen, locate the **Sources** screen by clicking on the **Design** tab. Double-click on **Votecircuit1 (Votecircuit1.sch)** to open the schematic. If it is already open, you will find it in the files tab bar just above the **Console** area at the bottom of the screen. You can just click the tab to open the file.

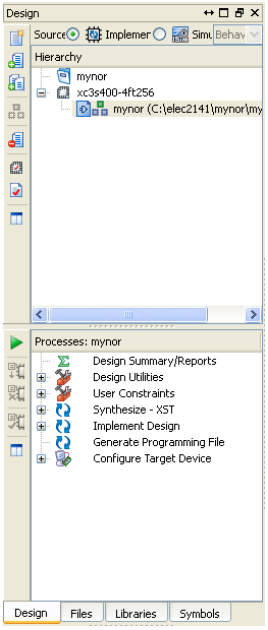


Figure 2.10: Design tab

To insert a symbol, we need to switch to the **Symbols** tab. Click on the tab to switch the view.

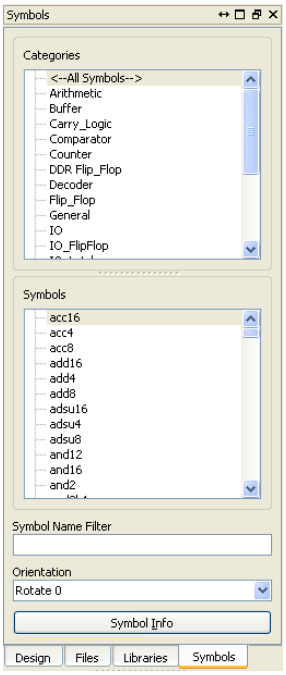


Figure 2.11: Symbols tab

Select **logic** under **categories** window and double click on **and2** under **Symbols**. Move your pointer to the right into the schematic design area. You should see that the mouse cursor is now a cross, with a **AND** symbol next to it.

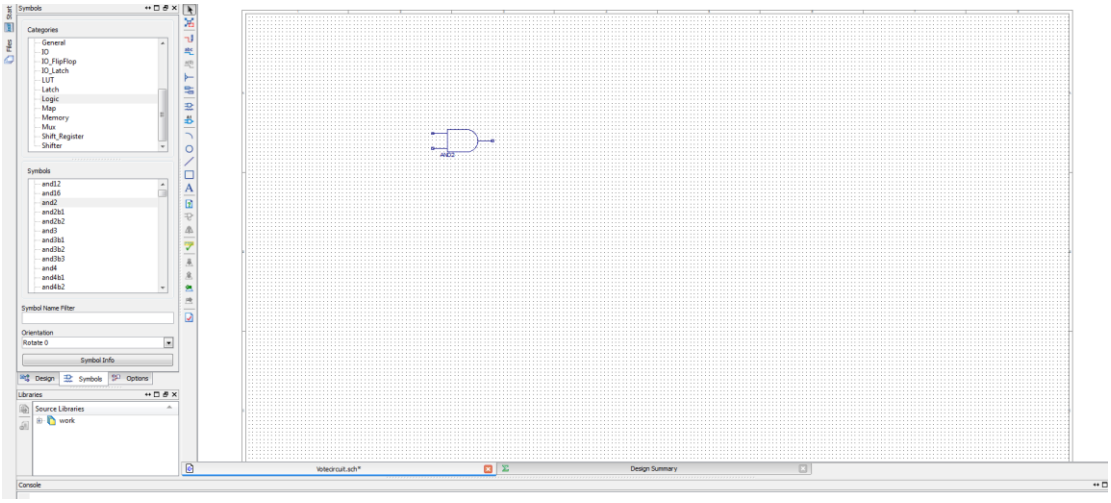


Figure 2.12: AND symbol

Clicking on the screen inside the design area will place the **AND** gate onto the schematic. The symbol might be very small. Place your mouse cursor on the centre of the circuit and press **F8** to zoom-in until it is large enough to view comfortably.

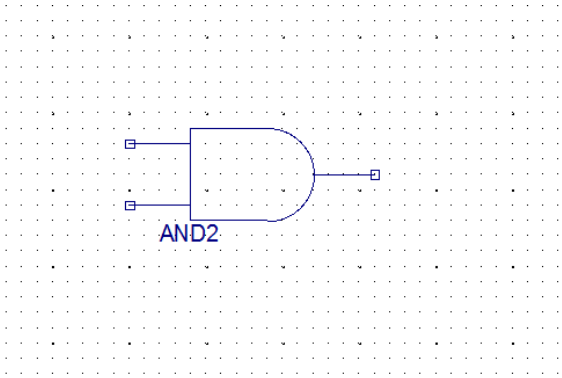


Figure 2.13: AND symbol zoomed in

Click on **and2** under symbol again to place another **AND** gate on the schematic. Right click to stop placing the symbols on the schematics.

To place two input **OR** gates, select **logic** under **catagories** and click on **or2** under the **symbols** and place **three OR gates** on the schematics. Right click to stop placing the **or2** symbol.

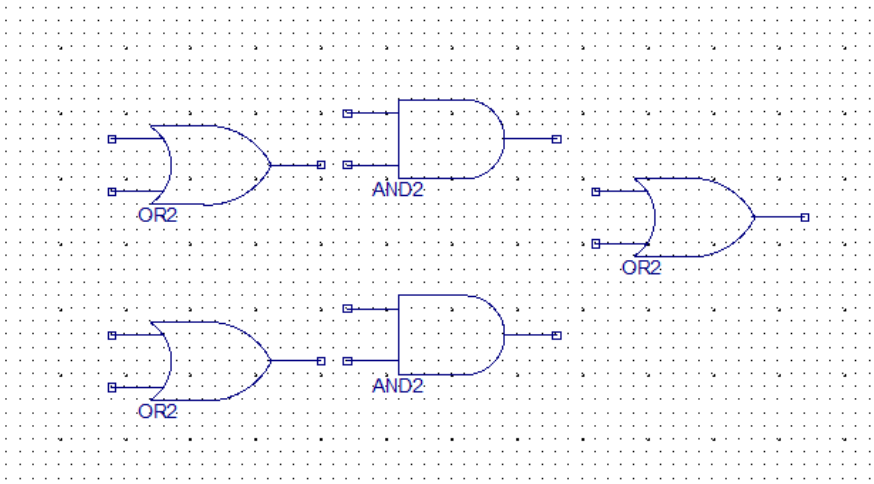


Figure 2.14: Two AND symbols and three OR symbols

To draw wires to create electrical interconnection between the gates, press **Ctrl-W** or click on the pencil with a red line icon on the left-hand side toolbar – the mouse cursor will change to a cross. Click on the square at the end of one of the inputs. Move your cursor toward the left to extend the wire, click once and press **Esc** to end.

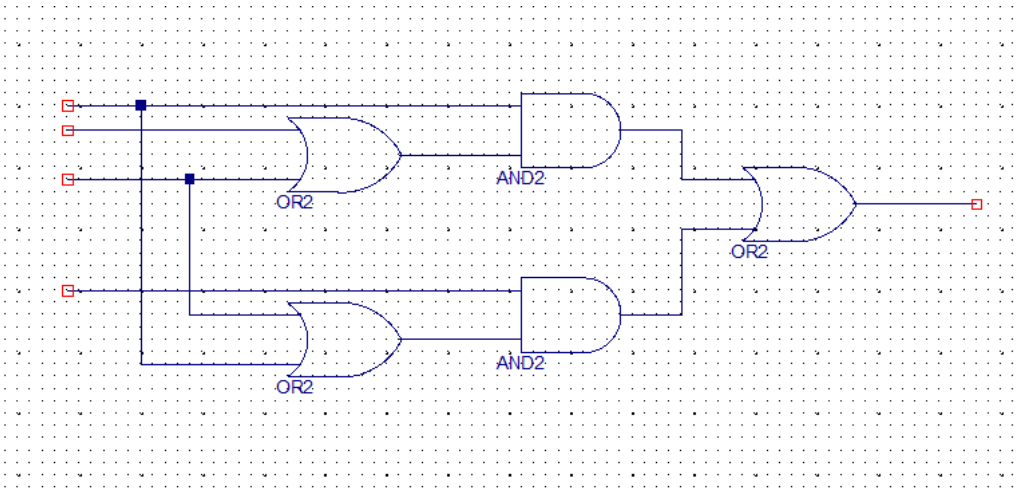


Figure 2.15: Gate interconnection through wires

Now, press **Ctrl-G** or click on button to add I/O markers. Click on the squares at the end of the inputs and the output of the combinational circuit. The numbers on the newly added I/O markers are random and you may get different labels. Press **Esc** to stop adding more I/O markers.

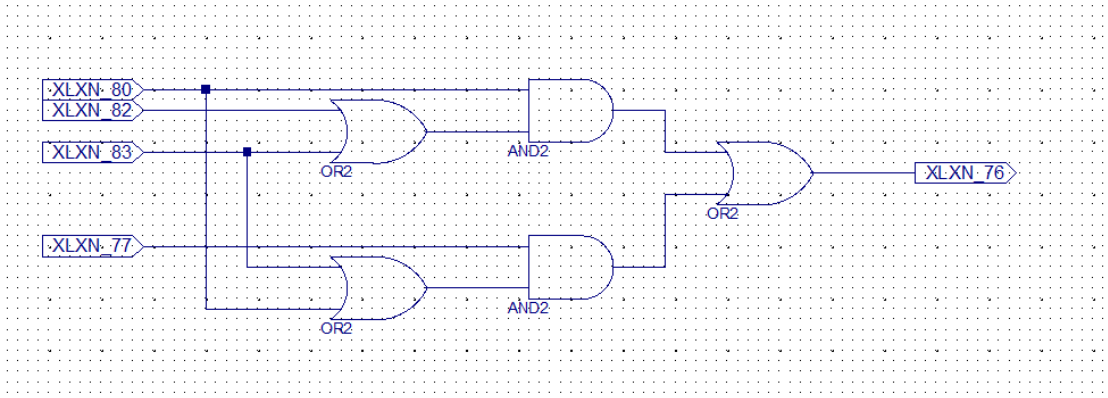


Figure 2.16: I/O markers added to the input and output terminals

Right-click on an I/O marker, for example **XLXN_80** as on the above schematic. Select **Rename Port...** from the menu.

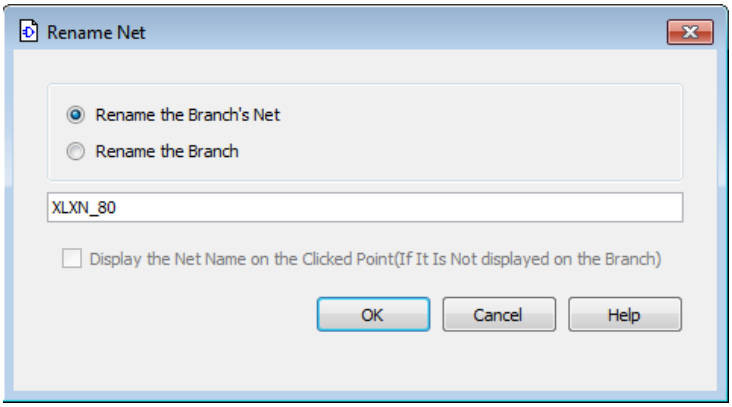


Figure 2.17: Rename Net window

Rename the Branch's Net to **Z.** Click **OK.**

Similarly, change the other inputs to **W, Y, X** and the output to **P**.

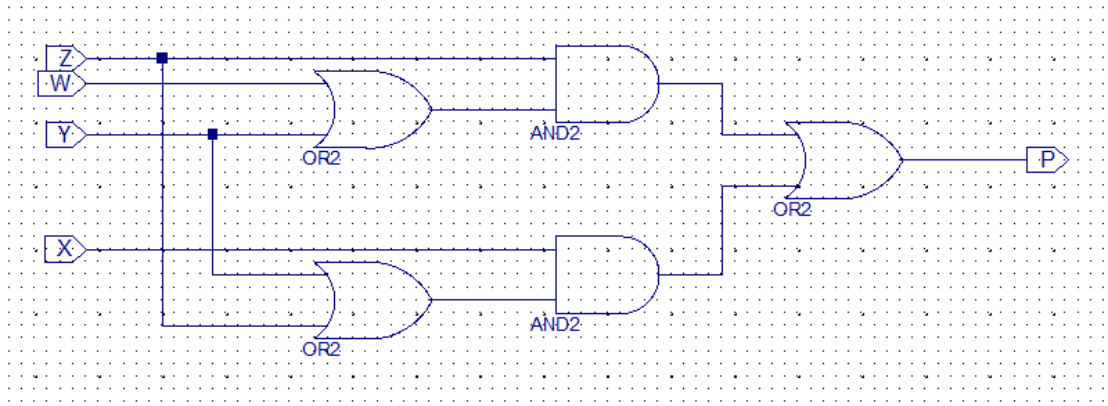


Figure 2.18: Input and output terminals after renaming

The instructions thus far illustrate the basics of using schematic design such as inserting symbols, connecting wires and adding I/O markers. **Save** and **Close** the project.

Drawing a Schematic in Xilinx – Your Turn

Start a new project named **Votecircuit2**, with the top-level schematic of the same name. Draw the schematics in Figure 2.6 in Xilinx: Select **Mux** under **catagories** and **m8_1e** under **symbols** to place 8-to-1 multiplexer. Also use **general** under **catagories** to select and place **Vcc** and **GND** symbols.

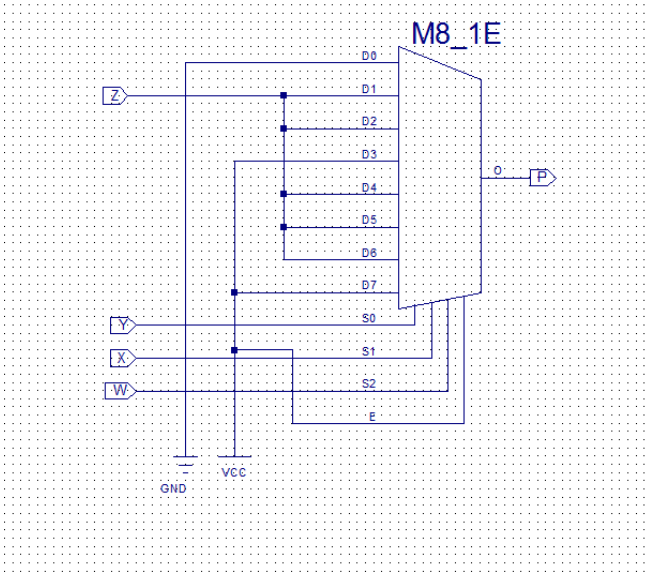


Figure 2.19: Schematic drawing of Figure 2.6

Save this work to show the schematic later to a demonstrator.

Start a new project named **Votecircuit3**, with the top-level schematic of the same name. Draw the schematic in Figure 2.7 in Xilinx: It should look like in the figure below

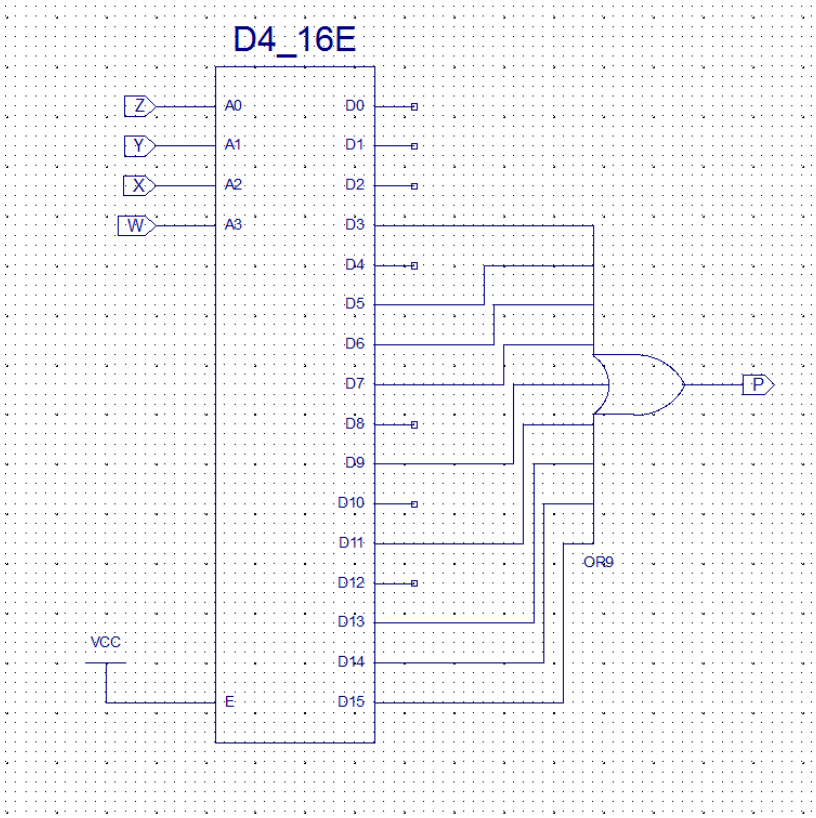


Figure 2.20: Schematic of Figure 2.7

Save this work to show the schematic to a demonstrator later

Simulation in Xilinx

Open **Votecircuit1** project We would like to simulate the circuit in order to verify its correct operation. For this purpose we need to create a test bench. Select **Project → New Source** and create a new **Verilog Test Fixture.** Name it **Votecircuit1_tbw**. Click **Next** and select **Votecircuit1** to associate it with the schematic. Click on **Next** and then **Finish**. An editor will open, presenting a Verilog Test Fixture with some code already filled in. For the moment, we will only cover the basics of writing code in Verilog. You will learn more detailed Verilog programming later in the course.

Verilog is a *Hardware Description Language* which can be used to build implementations of digital logic circuits, as well as simulate them. We will be writing a test bench (also known as a test fixture in Xilinx ISE) which allows us to specify a set of signals to be input to the *Unit Under Test* (*UUT* – otherwise known as the circuit that you are testing, that is, the one you have associated your test

fixture with when you created it). We can specify values to be given to certain input ports of our design, and specify delays between signal changes in order to simulate and observe the result of our circuit.

Coding in Verilog is quite similar to programming in C. For the moment, we will introduce you to a few key concepts which will allow you to write simple Verilog test benches on your own.

Firstly, numbers are specified in Verilog in the format `n'Bxxxx` where *n* represents the number of bits in the value, *B* represents the base and *xxxx* represents the number in the specified base. For example – 8 bits of 1 could be notated as 8'b11111111. Likewise, binary 1100 could be written as 4'b1100.

Secondly, assignments can be made to inputs similar to C. For example, to assign 11111111 to **A**, you simply write `A = 8'b11111111;` (to be accurate, this is only valid inside a *procedural block*, as you will learn later in the course).

Thirdly, to specify a delay, use `#xxxx;` where *xxxx* represents the number of time steps to delay for. The default time step is 1ns (configured in the `` `timescale 1ns/1ps `` line). You will not need to change this. If a 500ns delay is required, simply put `#500;` on a line of its own, and the simulator will delay for 500ns when it reaches that line.

For your **Votecircuit1** test bench, we want to have signals scheduled as provided in table 2.3.

Note that *1'b* in front of a number indicates that the number is specified in binary; likewise, *4'h* in front of a number indicates that the number is in hexadecimal. This is a programmers' notation, which will need to be converted to the Verilog notation stated earlier by specifying the number of bits explicitly – i.e. 0b00010000 will become 8'b00010000 and 0xA5 will become 8'hA5.

In order to produce the above test pattern, we must code this into our test bench. First of all, notice that under the `// Inputs` line, the inputs to our circuits are defined as `reg Z;reg X;reg Y; reg W;` This means that our inputs are **Z,X,Y,** and **W** respectively, and each of them is a bit.

Time (ns)	W	X	Y	Z
0 – 100	1'b0	1'b0	1'b0	1'b0
100 - 200	1'b0	1'b0	1'b0	1'b1
200 - 300	1'b0	1'b0	1'b1	1'b1
300 – 400	1'b0	1'b0	1'b1	1'b0
400 - 500	1'b0	1'b1	1'b1	1'b0
500 - 600	1'b0	1'b1	1'b1	1'b1
600-700	1'b0	1'b1	1'b0	1'b1
700-800	1'b0	1'b1	1'b0	1'b0
800-900	1'b1	1'b1	1'b0	1'b0
900-1000	1'b1	1'b1	1'b0	1'b1
1000-1100	1'b1	1'b1	1'b1	1'b1
1100-1200	1'b1	1'b1	1'b1	1'b0
1200-1300	1'b1	1'b0	1'b1	1'b0
1300-1400	1'b1	1'b0	1'b1	1'b1
1400-1500	1'b1	1'b0	1'b0	1'b1
1500-1600	1'b1	1'b0	1'b0	1'b0

Table 2.3: Test bench signals

For most of the test benches you will be writing, you will not need to concern yourself too much with the code that's been provided. The code that is provided simply does the tedious work of declaring your inputs, outputs and unit under test – what you are really concerned with is the section labelled **Initialize Inputs**. It is under this section which all of the real simulating work is done.

Begin by commenting out the lines `` `ifdef auto_init `` and `` `endif `` by adding `//` in front of them. Before `// `endif`, add `end` on a line of its own. Now we can begin adding our signals to our test bench. Locate the line that says `Z=0;Y=0;X=0;W=0;` We want our signals to be 1 bit of zeroes, so change them to `Z=1'b0;Y=1'b0;X=1'b0;W=1'b0;` This condition is held for 100ns, so after the fourth lines, and on its own line, put `#100;`

Now, we repeat the same idea again, this time assigning appropriate values to **W,X,Y,** and **Z** and setting up another delay. This time, add `Z = 1'b1;` and `#100;` There is no need to assign new values to **W,X, and Y** as it stays constant throughout this time. Similarly, continue by entering the appropriate lines for the other conditions.

After this, your Verilog test fixture should look like the following (lines in bold indicate lines which were changed):

```
// Verilog test fixture created from schematic //C:
\experiment\Votecircuit1\Votecircuit1.sch - module
Votecircuit_Votecircuit_sch_tb();
// Inputs
   reg  Z;
   reg  X;
   reg  Y;
   reg W;
// Output
   wire P;
// Bidirs
// Instantiate the UUT
Votecircuit UUT (
           .Z(Z),
           .X(X),
           .Y(Y),
           .W(W),
           .P(P)
);
// Initialize Inputs
//    `ifdef auto_init
        initial begin
           Z  =  1'b0;
           Y  =  1'b0;
           X  =  1'b0;
           W = 1'b0;
           #100;
           Z = 1'b1;
           #100;
           Y = 1'b1;
           #100;
           Z = 1'b0;
           #100;
           X = 1'b1;
           #100;
           Z = 1'b1;
           #100;
           Y = 1'b0;
           #100;
           Z = 1'b0;
```

```
            #100;
            W = 1'b1;
            #100;
            Z = 1'b1;
            #100;
            Y = 1'b1;
            #100;
            Z = 1'b0;
            #100;
            X = 1'b0;
            #100;
            Z = 1'b1;
            #100;
            Y = 1'b0;
            #100;
            Z = 1'b0;
            end
            `endif
    //
endmodule
```

Figure 2.21: Verilog test fixture for Votecircuit1

Save your test fixture, and close the file. Now we are ready to begin simulating. Make sure that you are in the **Design** tab on the left-hand side, and choose the radio button for **Sources** to be **Simulation** (this is near the top).

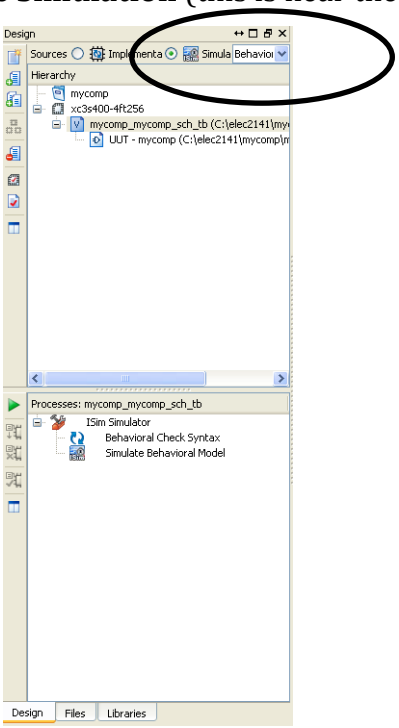


Figure 2.22: Design tab for simulation

Click on the test bench file (**Votecircuit1_Votecircuit1_sch_tb**) once to select it and then go to the **Processes** pane just below, right-click **Simulate Behavioral**

Model and choose **Process Properties**. Make sure the **Simulation Run Time** is set to **1600ns** (or any desired value in future simulations). Click **OK**.

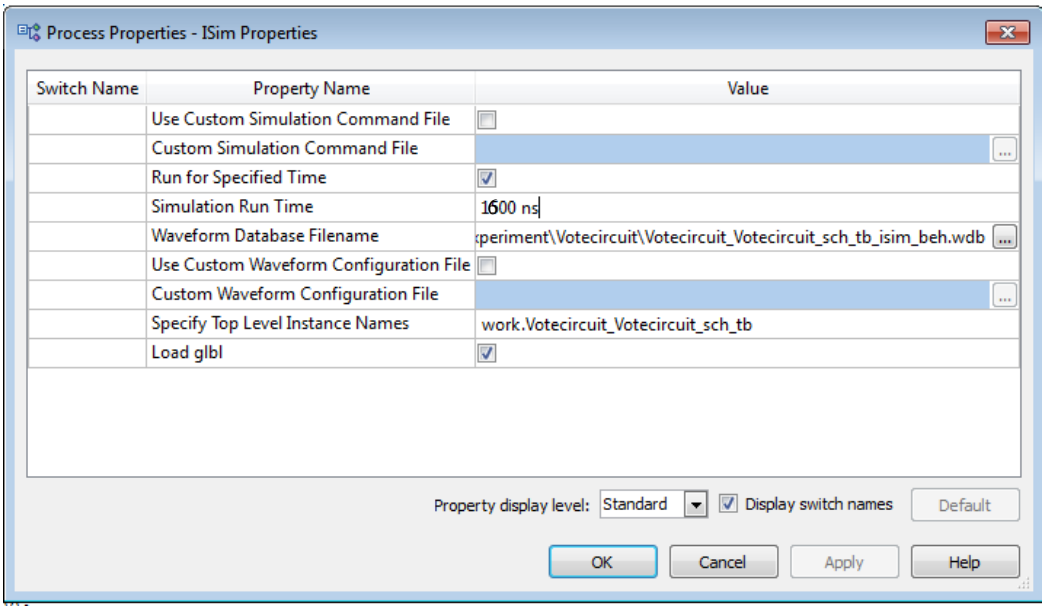


Figure 2.23: Process Properties window for 1600ns simulation time

Now, we need to verify that our simulation file is valid – that is, its syntax is correct. To do so, double-click on **Behavioural Check Syntax** in the **Processes** pane. If the file is okay, you will get a green tick next to the line; if it is not, you will get a red cross. If you do get a red cross, double-click on your test bench file and inspect it carefully, correct any errors and save it. The red cross will change into an orange question mark to indicate that you must re-run the process. Once you have a green tick, you may proceed to double-click on **Simulate Behavioral Model** which will bring up **ISim Simulator.** After a while, the simulation result will be displayed. By default, you will only see a limited view of the simulation as the time scale is zoomed in. Right-click in the black area and select **To Full View** to see all of your simulation. Your result should be similar to the image below. Note that the order of the signals displayed may be different.

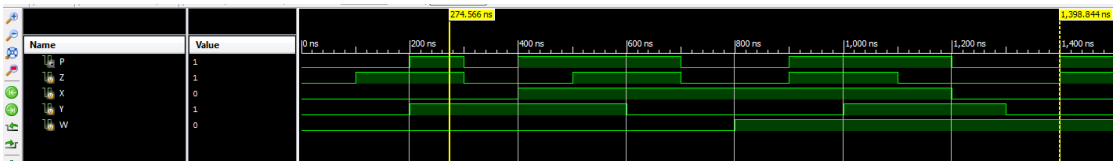


Figure 2.24: ISim Simulator window after full view

From the result, you can see that **P** has the same value as the truth table 2.1 for all input combinations, which verifies the correct operation of the designed combinational circuit. Remember to close the simulation when you are done. You

can always re-run the simulation by selecting **Sources** for **Simulation**, selecting the appropriate test bench file and double-clicking on **Simulate Behavioural Model**.

Note that the Verilog text fixture for Votecircuit1 can be rewritten in a more efficient way as below.

```
// Verilog test fixture created from schematic
//C:\experiment\Votecircuit1\Votecircuit1.sch -
module Votecircuit_Votecircuit_sch_tb();
// Inputs
   reg Z;
   reg X;
   reg Y;
   reg W;
// Output
   wire P;
// Bidirs
// Instantiate the UUT
   Votecircuit UUT (
          .Z(Z),
          .X(X),
          .Y(Y),
          .W(W),
          .P(P)
   );
// Initialize Inputs
//`ifdef auto_init
       initial begin
          Z = 1'b0;
          Y = 1'b0;
          X = 1'b0;
          W = 1'b0;
       forever begin
          #100;
          {W,X,Y,Z} = {W,X,Y,Z} + 1;
         end
      end
//    `endif
endmodule
```

Figure 2.25: More efficient Verilog text fixture

Simulation in Xilinx – Your Turn

Open the **Votecircuit2** project, add Verilog test fixture, modify the code and simulate the circuit.

Once you have verified that **Votecircuit2** is working properly, open **Votecircuit3** project, add Verilog test fixture, modify the code and simulate the circuit.

Show your simulation results of both projects to the demonstrator for a checkpoint.

Checkpoint 1b	*Assessor*	*Marks (5)*	*Date*

— END —

Lab 2 – Comprehensive Guide to FPGA Programming

In the previous lab, step-by-step instructions were provided to introduce you to schematic design and simulation of digital circuits in Xilinx. In this lab, we will give you an insight into the internal processes that Xilinx ISE uses to produce implementations for the FPGA. Combinational circuits designed and simulated in the previous labs will be implemented on the FPGA on Diligent Nexys 3 board and tested.

Compiling a project for downloading to the FPGA

During this lab, we will explore the complete process of digital logic design from scratch – from a bunch of gates, to compiling a design file ready to be programmed onto the FPGA.

For this project, we will interface the four switches on the board, namely **SW0**, **SW1**, **SW2**, and **SW3**, with the four inputs of the digital circuit, whose schematic shown in Figure 2.18, and the **LED0** on the board with the output **P**. The project is split into two stages: developing the design on the computer and downloading the design to the board.

The first stage requires the use of Xilinx ISE, so load the program on the computer.

The next step is to open the **Votecircuit1** project you created in lab 2. When this project was created, we have chosen our FPGA device which the project will be implemented from. There are hundreds of FPGA models in the market, and a design compiled for one type may not work directly on another device without modification. Xilinx simplifies this problem by applying device specific constraints and optimisation appropriate for the FPGA we are targeting.

The Xilinx FPGA is categorised in terms of its family, its device type, its packaging and its speed grade. FPGAs from different families differ in overall performance and cost. The one used in this lab, a *Spartan 6*, is a low cost FPGA. Another family,

called *Virtex*, is designed for higher performance and is generally more expensive than the Spartan6 equivalent.

Different device types within the same family usually have a different number of logical blocks which are used to implement logic cells, optimised multiplication, memory and I/O pins. The *XC6SLX16* used in the lab has about 1,600,000 gates with a capacity of 14,579 logic cells – large enough for a medium size design.

The physical package affects the number of I/O pins the device has and thus the amount of devices that are able to connect to it. The *CS324* package that the *XC6SLX16* comes in has provision for 232 I/O pins. The speed grade indicates the maximum switching rate of the device. The lower the speed grade, the faster the device can operate, and therefore, the faster the implemented circuit can be used. This is of importance when implementing circuits which run at high clock speeds. As an example, a grade -6 device has a shorter switching time compared to a grade -4 device. For more details about the FPGA we are using, refer to its datasheet available on the Xilinx website.

You may also recall that when the project is created, we chose schematic as the top-level design. The top-level design specifies how the logic gates themselves are to be connected together to create the final project. It can be either a schematic (drawing) or a Hardware Description Language file (coding). The principle is that the same design can be ported to a different hardware by only changing the mapping of the nets in the design to the pins on the device (by using a constraints file) without redesigning the underlying functionality of the project. It is easier to conceptualise how each subsystem interacts with each other using a schematic than it is using a HDL file, which is why we elect to use top-level schematic. Xilinx automatically recognises a schematic with the same name as the project to be the top-level design when creating a new project.

The top-level schematic is indicated by the three-squares icon next to the module.

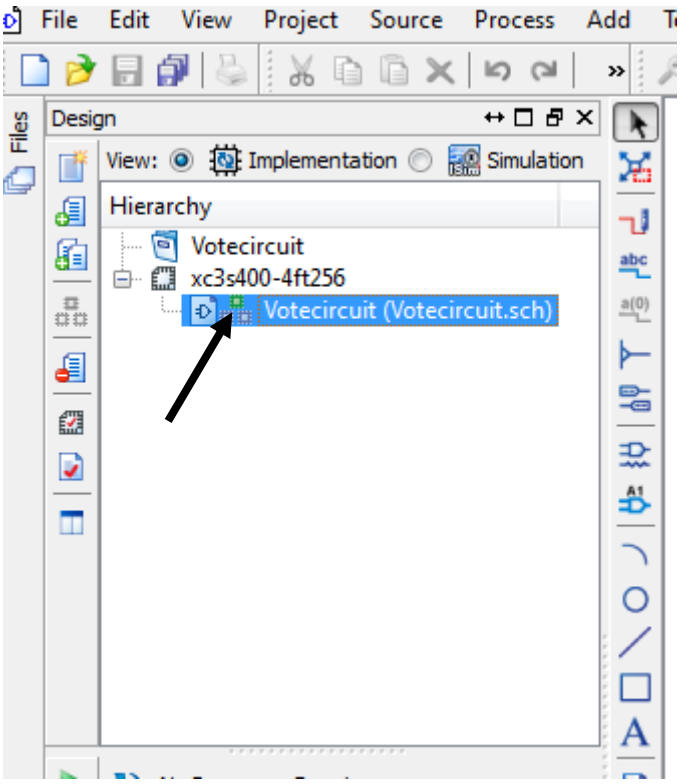


Figure 3.1: Top-level schematic indicated by three squares icon

The next step is to modify the schematics to create I/0 markers with **SW0, SW1, SW2, and SW3** for inputs and connect these makers with **Z, Y, X, and W**, respectively. In order to do that, first place four buffers (use catagories buffer and select buf from symbol), connect I/O markers at input side of each of the buffers, and rename the I/O markers to **SW0, SW1, SW2 and SW3** as shown in the figure below. To change I/O marker name, right click on the marker and select Rename port, and edit the name on the rename net window

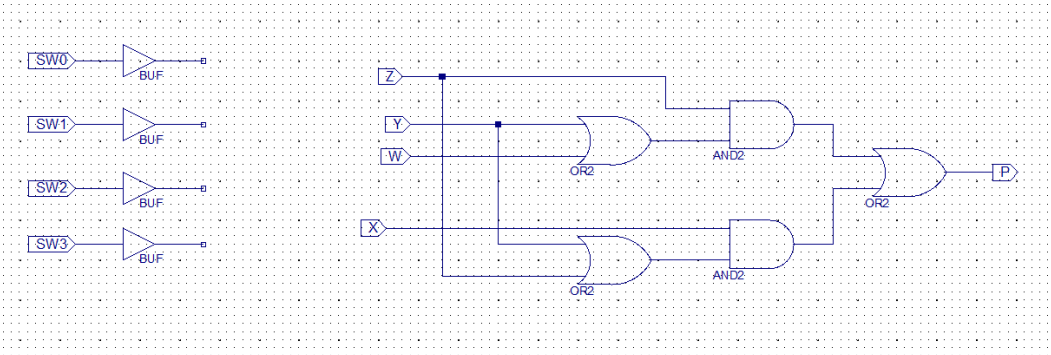


Figure 3.2: I/0 markers with **SW0, SW1, SW2, and SW3**

Next, change the input markers W,X,Y,and Z into just net names by clicking on the markers once and pressing delete button. Place I/O markers at the output

sides of the buffers, and rename the markers as Z (connected SW0), Y(connected to SW1), X(connected to SW2), and W(connected to SW3). Change the markers into just net names by clicking on the markers and pressing delete button. You should see the figure below after those steps.

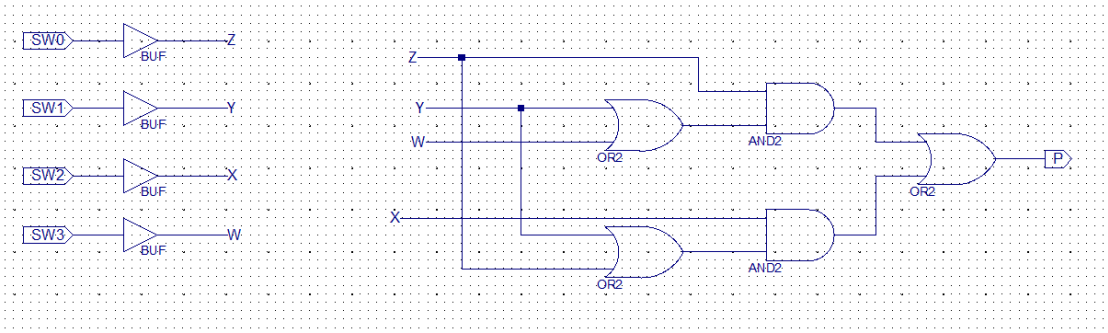


Figure 3.3: Connecting **SW0,SW1,SW2, and SW3** markers with inputs

Similarly, we need to modify the schematics by further connecting the output P from the digital circuit to output marker with LED0. Place one more buffer symbol on the schematic, add I/0 marker at the output of the buffer, rename the port as LED0, change P marker into just a branch net name, add I/O marker at the input of the buffer, and rename the marker as P and convert it into just a branch name. The schematic will look like as follows

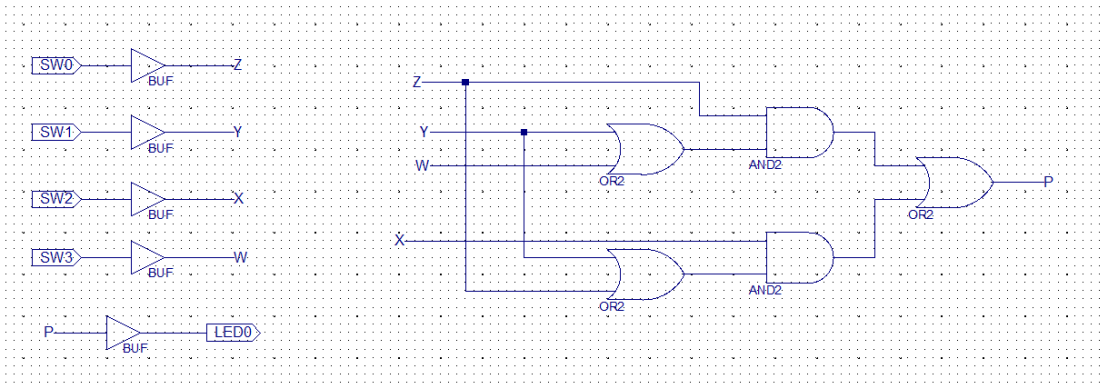


Figure 3.4: Connecting the output to I/O marker LED0

The final step is to prepare the design for testing on the FPGA. You now need to specify which marker corresponds to which physical pin on the FPGA. Pins on FPGA are grouped into *banks*. Each bank is denoted by a letter, and each pin in a bank is numbered from 1 to 16. For example L15 refers to pin 15 of bank L. Some pins may be **Vcc** or **GND**, some may be clock input only, some may be bidirectional and so on. Refer to the manual given in Appendix A for a comprehensive description of all the pins.

We need to create a *constraints file* to tell Xilinx where we want the nets connected to. To do this, click on new source and select "Implementation Constraints File". Name it as **Votecircuit1** and click **Next and then finish**.

Next, locate where the I/Os are connected. We are going to map the 4 switches and 1 LED using the pin location table from Appendix A:

Net Name	**Pin**
SW0	T10
SW1	T9
SW2	V9
SW3	M8
LED0	U16

Table 3.1: Pin locations for I/Os

In the constraints editor type the following that corresponds to the above pin mapping:

```
NET "LED0"  LOC = "U16";


NET  "SW0"    LOC  =  "T10";
NET "SW1"    LOC = "T9";
NET "SW2"    LOC = "V9";
NET "SW3"    LOC = "M8";
```

Figure 3.5: Constraints file

Then, save the UCF file.

Design Synthesis

Synthesising the design means expressing all the schematics and any other modules used into *netlist files*. Netlist files provide information on the design of the modules (and their instances) and their relation (how they are connected together).

To synthesise the design, select **Votecircuit1** in the **Sources** view, and make sure that **Sources** for **Implementation** is selected (and not **Simulation**). Next in the **Processes** pane, double-click on **Synthesize – XST.** The icon to the left of this line should start animating. After a minute or two, you should get a green tick on the left if you had followed the steps correctly. If you do not get a green tick, check the **Console** tab at the bottom of your screen to see what warnings and/or errors appear and try to correct them before trying again. Contact your lab demonstrator if unsuccessful.

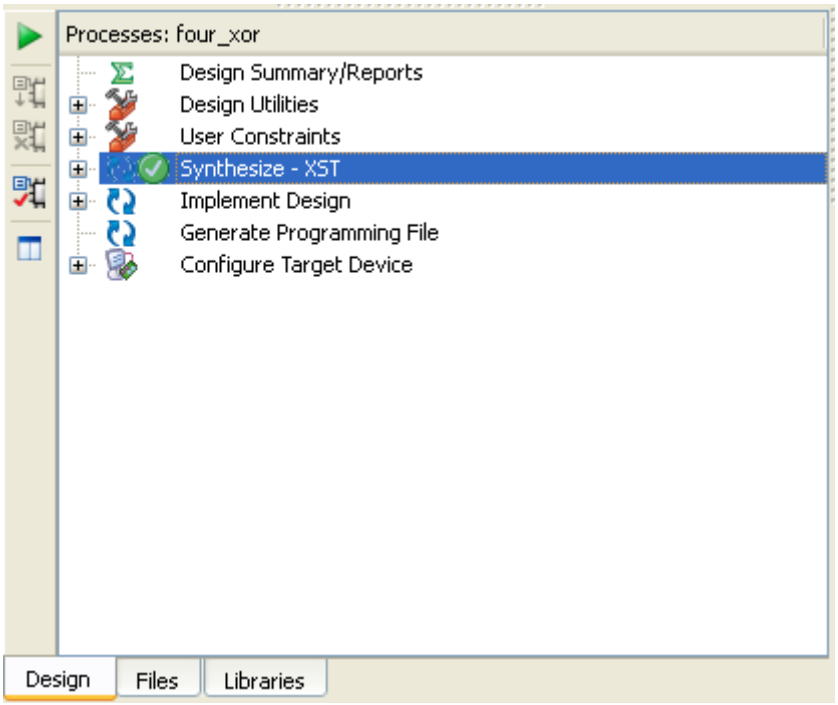


Figure 3.6: Synthesize -XST

Design Implementation

There are three steps in the implementation stage: *translate*, *map* and *place & route*.

The **Translate** process merges all of the netlist files and design constraints to produce a Xilinx native generic database, which describes the logical design reduced to Xilinx primitives. The **Map** process maps the logic defined during translation into FPGA elements, such as logical blocks and I/O buffers. The output design is a native circuit description file that physically represents the design mapped to the components in the Xilinx FPGA. The **Place & Route** process then produces an arrangement for the components within the FPGA and describes how each of the components are interconnected via common connection lines and how the pins are connected to the components.

To implement the design, make sure **Votecircuit1** is still selected in the **Sources** view, and we have chosen **Sources** for **Implementation**. Next in the **Processes** view double-click on **Implement Design.** If the icon turns into a red cross or orange question mark, then you can expand this item to see which of the processes failed. If you have a problem, check the warnings and errors in the **Console** tab at the bottom of your screen to get a hint to what the problem might be. Contact your lab demonstrator if you still do not get a tick.

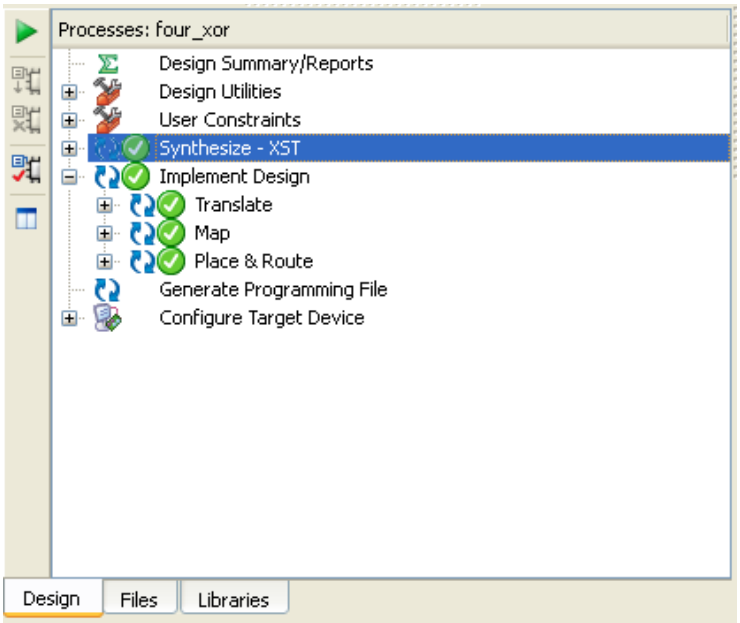


Figure 3.7: Implement design

Programming File Generation

The **Generate Programming File** process produces a *bitstream file* for Xilinx device configuration. After the design is completely routed, you must configure the device so it can execute the desired function.

First set the FPGA start-up clock which is specific to this board. Right-click on **Generate Programming File** under **Processes** view. Choose **Process Properties**, and then click on **Startup Options** in the left-hand pane and select **JTAG Clock** on the right for **FPGA Start-Up Clock**. Click **OK.**

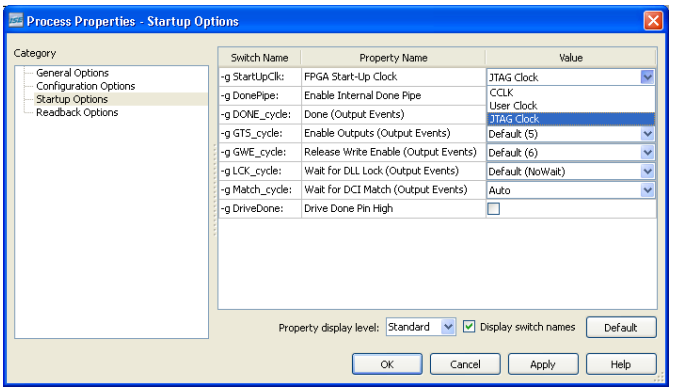


Figure 3.8: Process properties window

You are now ready to compile your first bit-file. Double-click **Generate Programming File** and wait until the **Console** view at the bottom of the screen shows the completion message:

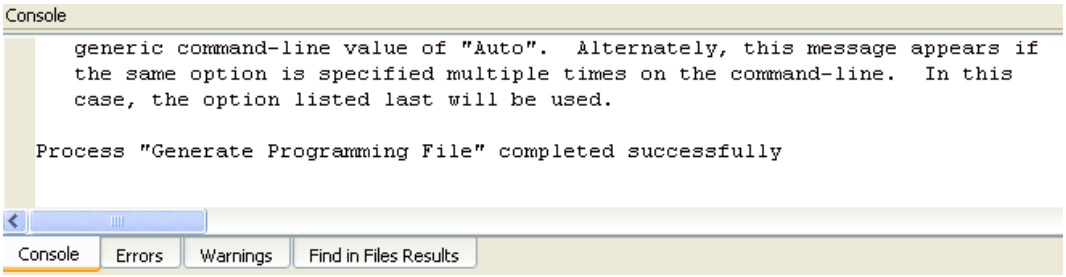


Figure 3.9: Console showing successful programming file

The generated bit file, **Votecircuit1.bit,** will be located in the same folder as the project. Download your design to the FPGA using the Adept utility (in a similar way to the method used at the beginning of Lab 2). Verify the operation of the digital circuit by using the switches and the LED. You may fill the table below and compare it with Table 2.1

	SW3(W)	SW2(X)	SW1(Y)	SW0(Z)	LED0(P)
0	0	0	0	0	
1	0	0	0	1	
2	0	0	1	0	
3	0	0	1	1	
4	0	1	0	0	
5	0	1	0	1	
6	0	1	1	0	
7	0	1	1	1	
8	1	0	0	0	
9	1	0	0	1	
10	1	0	1	0	
11	1	0	1	1	
12	1	1	0	0	
13	1	1	0	1	
14	1	1	1	0	
15	1	1	1	1	

Table 3.2: Verification table for **Votecircuit1**

Similarly, implement and test your design **Votecircuit2** from lab 2 on the FPGA. For the implementation, use the same switches and LED as previous. Verify that the operation of this design and its similar functionality with **Votecircuits1** by filling up the table below

	SW3(W)	SW2(X)	SW1(Y)	SW0(Z)	LED0(P)
0	0	0	0	0	
1	0	0	0	1	
2	0	0	1	0	
3	0	0	1	1	
4	0	1	0	0	
5	0	1	0	1	
6	0	1	1	0	
7	0	1	1	1	
8	1	0	0	0	
9	1	0	0	1	
10	1	0	1	0	
11	1	0	1	1	
12	1	1	0	0	
13	1	1	0	1	
14	1	1	1	0	
15	1	1	1	1	

Table 3.3: Verification table for **Votecircuit2**

Implement and test your design **Votecircuit3** from lab 2 on the FPGA in the similar manner as you did for Votecircuit1 and Votecircuit2. For the implementation, use the same switches and LED as previous. Verify that the operation of this design and its similar functionality with **Votecircuit1 and Votecircuit2** by filling up the table below. Show the working implementations to your demonstrator.

	SW3(W)	SW2(X)	SW1(Y)	SW0(Z)	LED0(P)
0	0	0	0	0	
1	0	0	0	1	
2	0	0	1	0	
3	0	0	1	1	
4	0	1	0	0	
5	0	1	0	1	
6	0	1	1	0	
7	0	1	1	1	
8	1	0	0	0	
9	1	0	0	1	
10	1	0	1	0	
11	1	0	1	1	
12	1	1	0	0	
13	1	1	0	1	
14	1	1	1	0	
15	1	1	1	1	

Table 3.4: Verification table for **Votecircuit3**

Checkpoint 2	*Assessor*	*Marks (5)*	*Date*

— END —

Lab 3 – Combinational Circuit Design Project.

In this lab, you will

- be introduced to 7-segment display units and push-button switches on the development board and
- design, simulate, implement on the FPGA and test a more advanced version of a combination circuit whose design specifications were presented in Lab 2. The statement of the design specification is presented again here for convenience

Design specification

A small company is owned by four peoples (Mr. W. Mr. X, Mrs. Y, Mr. Z) and has a total of 10 shares of stock. Each share entitles its owner one vote at a stockholder's meeting. A motion is passed at the stockholder's meeting if it receives a majority vote (that is five or more votes). The 10 shares of stock are distributed among the owners as follow:

Mr. W has one share

Mr.X has two shares

Mrs.Y has three shares

Mr. Z has four shares

Each owner has a switch at the stockholder's meeting to cast their vote on a motion. When a motion is passed, a lamp is to be switched on.

The digital circuit that will be designed and implemented in this lab should have additional functionality. It will display the number of total votes on one of the four seven segment displays available on DIGILENT Nexys board. If the total number of votes is 0, the seven segment display should be blank. If the total number of votes is anywhere from 1 to 9, display that digit. If the total number of votes is 10, display 0 because we have only one digit to work with in this lab.

In implementing and testing the combinational circuit, you will use **SW0, SW1, SW2, and SW3** on the Digilent Nexy board as input switches for Mr W, Mr.X, Mrs.Y, and Mr.Z, respectively, in the stockholder's meeting, **LED0** as the lamp (output) that indicates if the motion is passed, and a 7-segment unit to display

the total number of votes (You can choose one of the four display units and the other display units should remain blank).

This is a design project and as such you may have your own particular design choice. It is important to remember that you will have to justify to the lab demonstrator why you make the particular design choice.

Before you embark on the design work, it will be worthwhile having some experience working with the 7-segment display units and push-button switches on the development board.

7-Segment Display Unit

The development board has four 7-segment display units. Each display unit has seven LED elements, each of which can be individually turned on or off to produce simplified representations of the Hindu-Arabic numerals. The LED elements of a 7-segment display unit are referred to by the letters A to G, where the optional DP decimal point is used for the display of non-integer numbers.

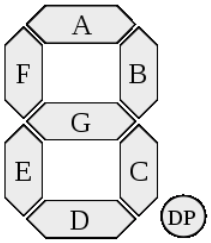


Figure 4.1: 7 segment display unit

Each 7-segment display unit requires 8 signals to control its display pattern. This means 32 control signals are needed if each segment in the four display units is to be independently controlled. However, the development board provides only 8 control signals for the display units. In addition to these 8 control signals, it also provides four select lines, one for each 7-segment display unit (**SEGA0, SEGA1, SEGA2, and SEGA3**). The 8 control signals (**SEGDA, SEGDB, SEGDC,SEGDD,SEGDE,SEGDF, SEGDG and SEGDP**) are applied to all the display units at any given time, but only controls those display units which are selected. Create a new project called **segment** and name the top-level schematic **segment** as well**.** Draw 12 **BUF** (buffers) on the schematic. Connect the 8 switches to the 8 segments beginning with **SEGD*x*** via a buffer. Also connect the push-buttons to

the four **SEGA*x*** via a buffer. Your schematic should look like the one shown below. Note that D,U,R, and L in PBD, PBU, PBR, PBL are to represent the Down, Up, Left and Right push button switches on the Nexys board.

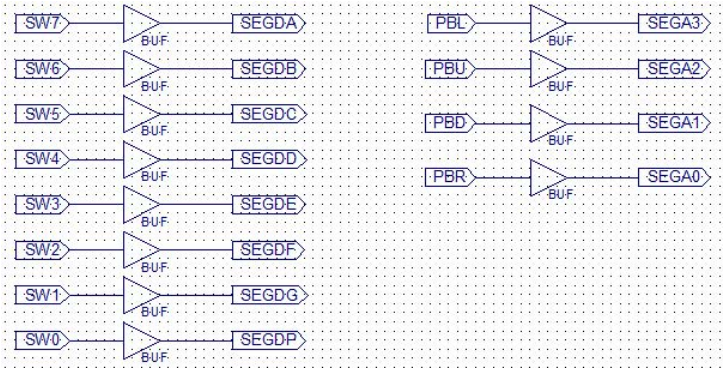


Figure 4.2: Schematic for project segment

You will have to make a new UCF file for this project. We haven't provided the mappings here, however, you can find it in Appendix A. Produce an appropriate UCF file, save it, generate a programming file and download it to the FPGA. Change all the switches to 0 (down). Do the LEDs light up?

All 7-segment displays should be displaying the same pattern. Now press and hold **PBD** (**SEGA1 = 1**), what happens to the four 7-segment displays? Note down your observations as you will use this behaviour to display multiple digits. A 7-segment display can display the digits 0 to 9 numerically by turning some of the segments on and off. Experiment with different combinations and fill in the table below to show how each of the 10 digits can be formed.

Digit	SEGDA	SEGDB	SEGDC	SEGDD	SEGDE	SEGDF	SEGDG
0							
1							
2							
3							
4							
5							
6							
7							
8							
9							

Design Procedure

1) Convert the specification (at the beginning of this lab) into a truth table. The combinational circuit has four inputs and eight outputs (seven for controlling the LED elements of the display unit, and one to control LED0).
2) Obtain the Boolean functions for each of the output and realize the functions using either logic gates or multiplexers or decoders and or gates.
3) Create a new project on Xilinx ISE with schematic as top level
4) Add a new schematic source and prepare the schematic of your design.
5) Simulate your schematics design and verify its correct operation against your truth table.
6) Implement the design onto the FPGA and test the correct operation of your design
7) Demonstrate the operational circuit to the lab demonstrator

Checkpoint 3	*Assessor*	*Marks (5)*	*Date*

Lab 4 – Flip-Flop Basics

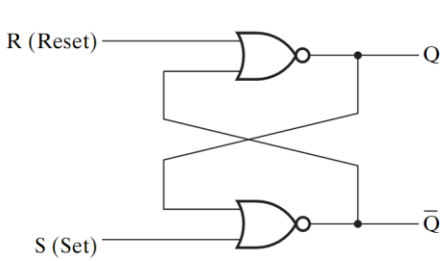
A *storage element* is a circuit which can maintain a binary state indefinitely (while the circuit is powered). This is essentially memory, allowing us to store a single bit. There are many ways to do this, including using a capacitor to store charge, like DRAM in modern computers, or using feedback logic circuit. They differ in terms of layout density, speed, power-consumption and complexity. In this lab, we will focus on the feedback logic circuit type of storage element.

The binary information stored in these elements at any given time defines the state of the circuit at that time, which can be changed by an input signal. The most basic storage elements are latches, from which flip-flops are usually constructed.

For the rest of this lab, we will adopt the **/X** notation as an alternative to the overbar notation, to denote a variable negation.

SR-Latch

The simplest storage element is a *latch*. A latch has the ability to hold an input state. An *SR-Latch* is a circuit with two cross-coupled NAND gates or two cross-coupled NOR gates. It has two useful states: the *Set* and *Reset* states. The two outputs of the latch are normally complements of each other. However, when both inputs are 1 (in an SR-Latch built with NOR gates) or 0 (in an SR-Latch built with NAND gates), an undefined state with both identical outputs may occur.

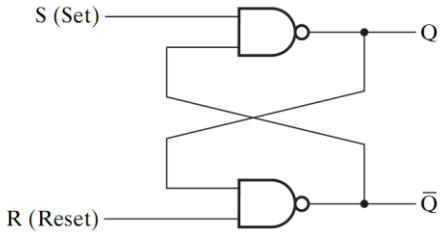


(a) Logic diagram

S	R	Q	$\overline{Q}$	
1	0	1	0	Set state
0	0	1	0	
0	1	0	1	Reset state
0	0	0	1	
1	1	0	0	Undefined

(b) Function table

Figure 5.1: SR latch using NOR gates



(a) Logic diagram

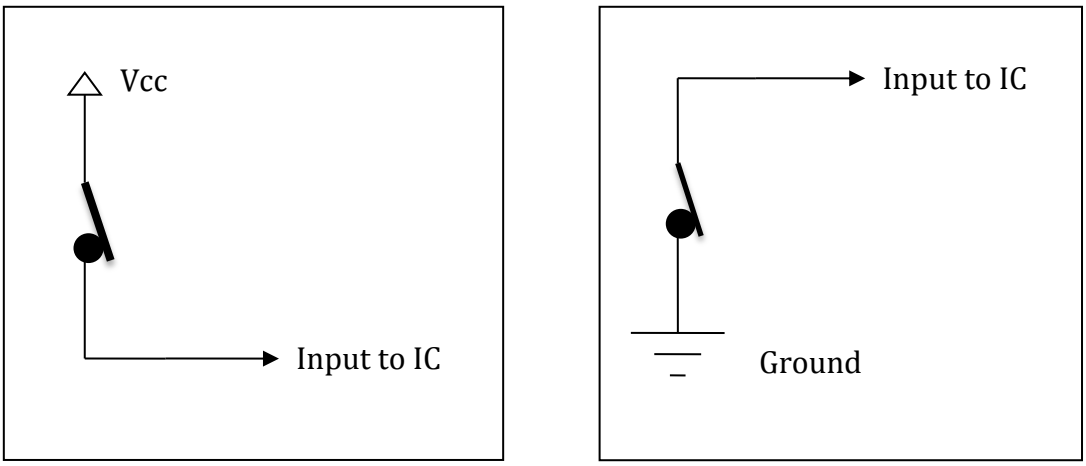
S	R	Q	$\overline{Q}$	
0	1	1	0	Set state
1	1	1	0	
1	0	0	1	Reset state
1	1	0	1	
0	0	1	1	Undefined

(b) Function table

Figure 5.2: SR latch using NAND gates

In testing the circuits in this lab and next, you will use slide switches as inputs and LEDs as outputs. The use and operation of slide switches and LEDs as an inputs and outputs, respectively, are described hereafter before you begin building and testing circuits

Slide switches can be in one of two states: an open circuit or a closed circuit. In Figure 5.3 (a) and (b), both switches are in closed circuit state. A digital input voltage of 1 or HIGH is provided by Figure 5.3(a) while the arrangement in Figure 5.3(b) provides a digital input of 0 or LOW. What would happen if the switches in both figures are opened? - the value of the input to a digital circuit becomes unknown since the pins will be floating – that is, unconnected. **You cannot automatically assume that the input to a digital circuit is 0 when it is unconnected!** As they are high-impedance inputs – stray voltages from inside the IC itself, or from adjacent inputs can cause unpredictable behaviour of inputs which are left unconnected. Whenever building circuits with ICs, tie all the unused inputs to an appropriate logic level to avoid problems while not interfering with the operation of your circuit.



(a) (b)

Figure 5.3: Digital input of (a) HIGH and (b) LOW

Instead of the arrangements in the above figures, switches are connected as in Figure 5.4 as an input for digital circuits. When the switch is in an open state, a digital input of "0" or "LOW" is obtained. When the switch is closed, a digital input of "1" or "HIGH" is generated.

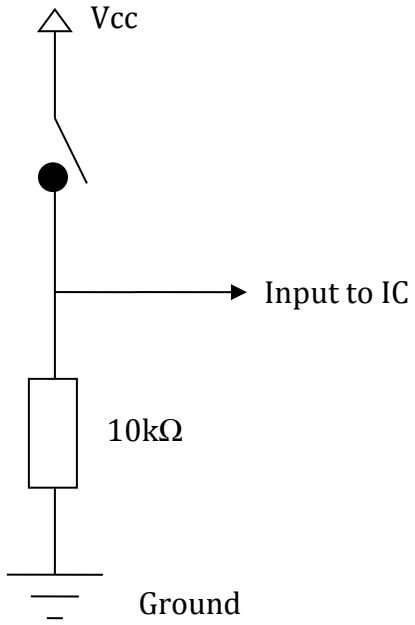


Figure 5.4: Configuration of a switch as a digital input.

The resistor is there to limit the current flow when the switch is closed, otherwise we would have a short circuit! Make sure you can explain why this circuit avoids the issues with the above designs!

You have been provided four slide *DIP switches* which you can use as inputs. The schematic representation and physical view of the four slide DIP switch is shown in Figure 5.5. It is essentially a block of four individual switches combined into a single unit as you can see in the diagram below.

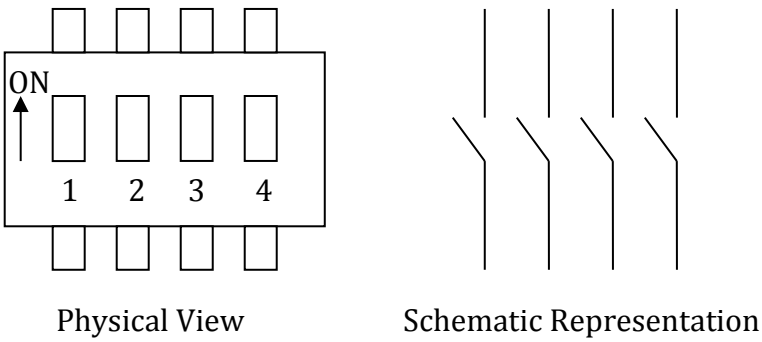


Figure 5.5: Top view and schematic representation of a four slide switch

LED is a special form of diode that produces light when current flows through it. Normally, LEDs have about 2v forward voltage drop and 20mA nominal current to produce their rated output. If more voltage is applied, a larger current flows and it will cause thermal runaway and damage the LED. This means that we cannot just connect the LED to the output, but rather we will have to put the LED in series with a resistor that limits the current flow and prevents damage.
The output is thus constructed as shown below:

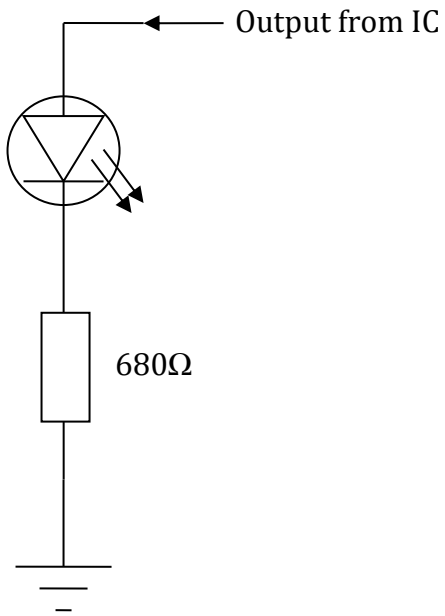


Figure 5.6: Connection of LED for displaying output

The LED has two terminals. The longer leg of your LED is the positive (*anode*) terminal, the shorter leg is the negative (*cathode*) terminal. If you have cut the legs of your LED, you can identify the polarity by looking for a flat surface around the base of the LED. The flat surface is adjacent to the negative terminal. You may trim the legs of your LED carefully so they sit flush to the surface of your breadboard.

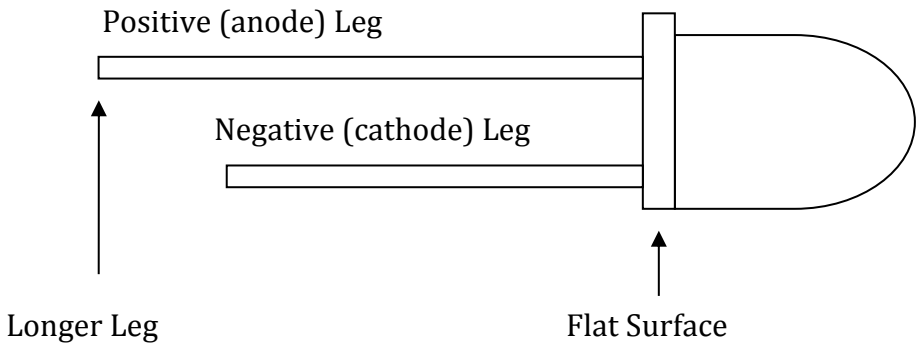


Figure 5.7: Physical layout of LED

Exercise: Operation of NAND SR-Latch

The following is the logic diagram for a SR-Latch built with NAND gates:

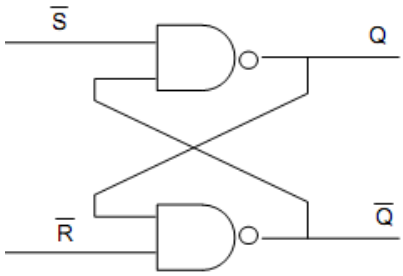
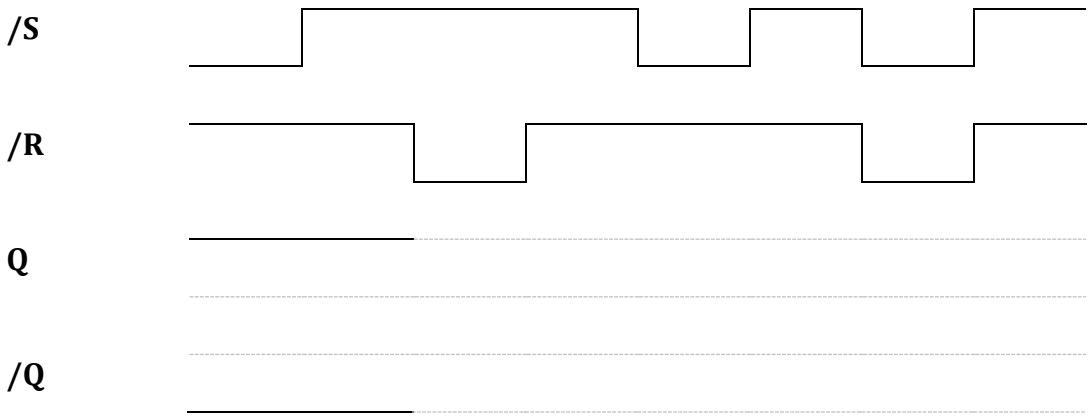


Figure 5.8: SR-Latch with NAND gates

Build this circuit on your breadboard. Connect the inputs to switches and the outputs to LEDs. Fill in the following truth table by testing out different input combinations and recording the values of **Q** and **/Q**.

/S	**/R**	**Q**	**/Q**
0	0		
0	1		
1	0		
1	1		

Verify the truth table using the given circuit by reading the outputs for the waveform below:



Exercise: Operation of SR-Latch with Control

The following is the circuit for *SR-Latch with Control* using four NAND gates:

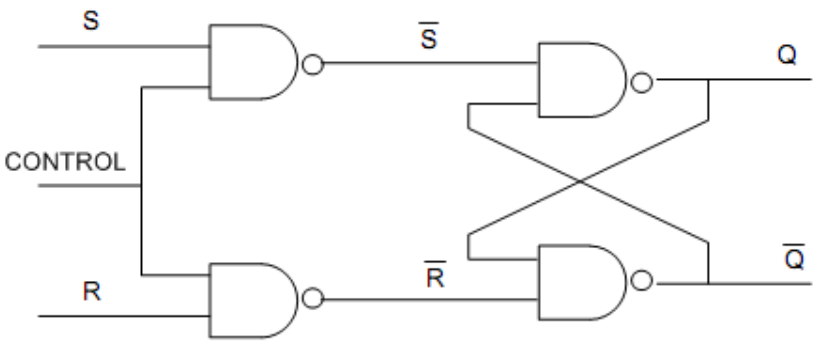


Figure 5.9: SR latch with Control

Begin by answering the following questions:

- If the **CONTROL** signal is 0, what are the values of **/S** and **/R**?

- If the **CONTROL** signal is 0, are the values of **/S** and **/R** dependent on **S** and **R** respectively?

Construct the circuit and verify its operation.

For the remainder of the lab, the following symbol will be used to denote a SR-Latch with Control:

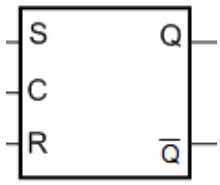


Figure 5.10: Symbolic representation for SR-latch with Control

Exercise: Operation of a D-Latch

The following is the circuit of a *D-Latch* using a SR-Latch with Control and a single inverter:

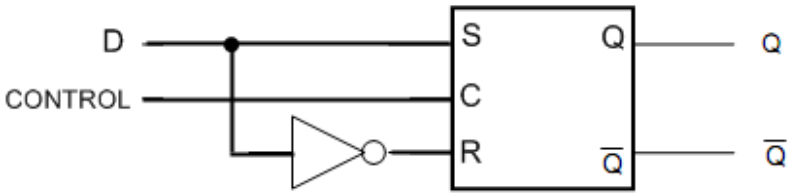
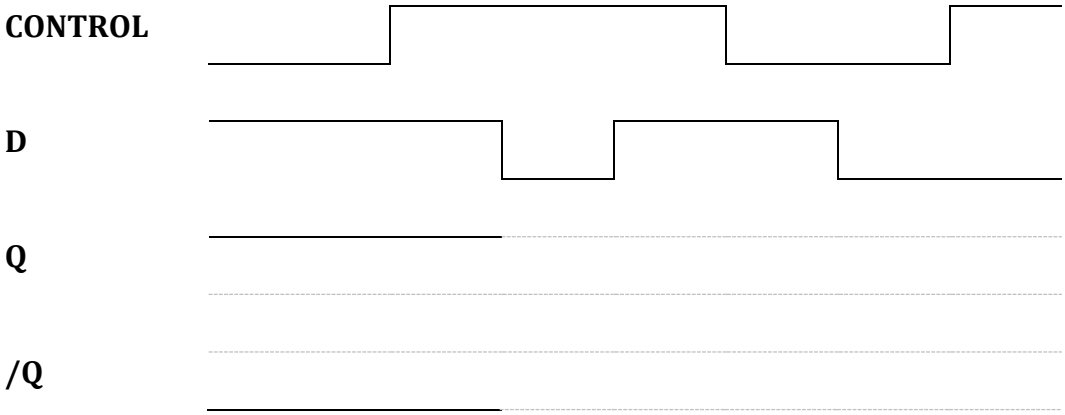


Figure 5.11: D-Latch constructed from SR-latch with Control

Construct the circuit and complete the following waveform diagram:



What is the benefit of using a D-Latch over SR-Latch?

For the remainder of the lab, the following symbol will be used to denote a D-Latch:

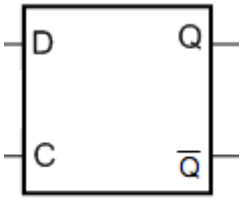


Figure 5.12: Symbolic representation of D-Latch

Flip-Flop

The output of a *flip-flop* can only change on the rising or falling edge of the control signal. This change in control signal is called a *trigger* and it enables, or triggers, the flip-flop. Triggering is achieved by having a D-Latch connected back-to-back with an SR-Latch with complementary control lines. The idea is to use the first D-Latch to capture the input at the moment the control signal switches state and use the second SR-Latch to hold this state while the control signal switches back. Essentially, this triggering only allows the state to change when the control signal changes.

Exercise: Operation of a D-Flip-Flop

The following is the circuit of a D-Flip-Flop constructed using a D-Latch, an SR-Latch with Control and a single inverter:

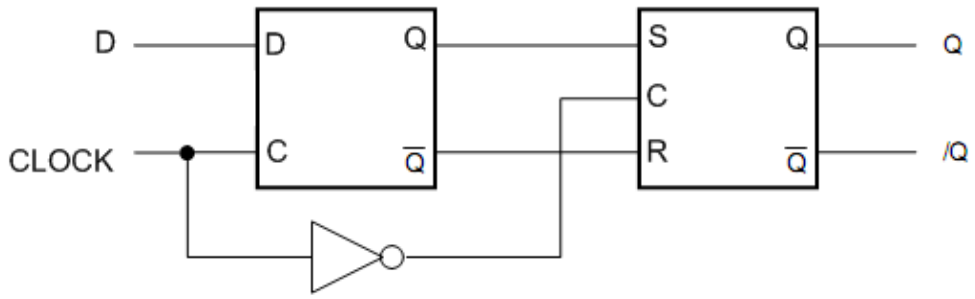
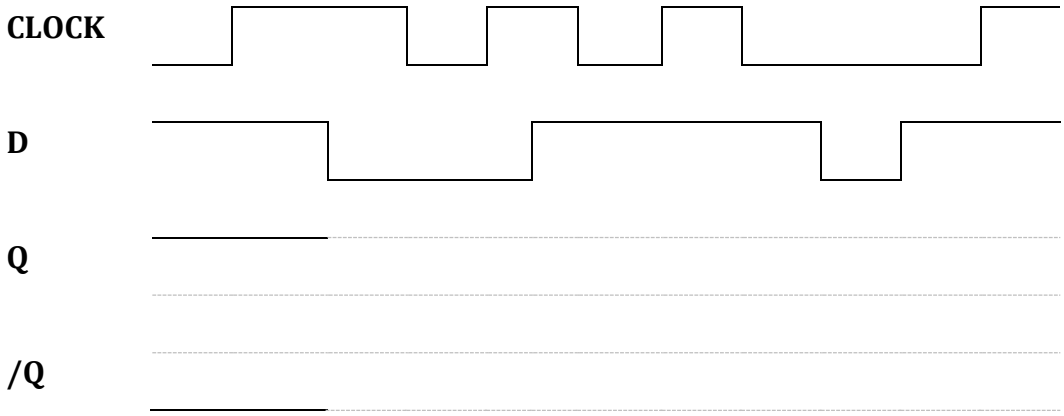
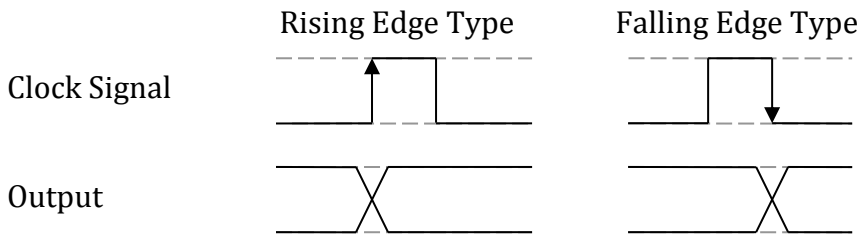


Figure 5.13: D-Flip flop

Fill in the following diagram showing the outputs that appear as a result of the inputs shown:



Flip-flops can change their state on either the *rising-edge* (or positive-edge) or the *falling-edge* (or negative-edge) of the clock input, as illustrated below:



Construct the above circuit by combining two D-latches built with NAND gates.

Is the constructed D-flip-flop positive-edge triggered or negative-edge triggered?

How would you modify the circuit to obtain the other triggering type?

How many NAND gates would you need to construct a D-flip-flop if everything was to be constructed with NAND gates only?

Demonstrate your circuit to your lab demonstrator.

Checkpoint 4	*Assessor*	*Marks (5)*	*Date*

— END —

Lab 5 – State machine basics

In this lab, you will

- build a sequential circuit on a breadboard using D-flip flops.
- be introduced to debouncing circuit and their use in a single pulse generator push-button switch
- experimentally derive the state diagram and state table of the sequential circuit.
- minimize the implementation and verify its equivalent operation.

The following sequential circuit has one input, X, one output Y, and consists of two D flip-flops for four possible states defined by A and B.

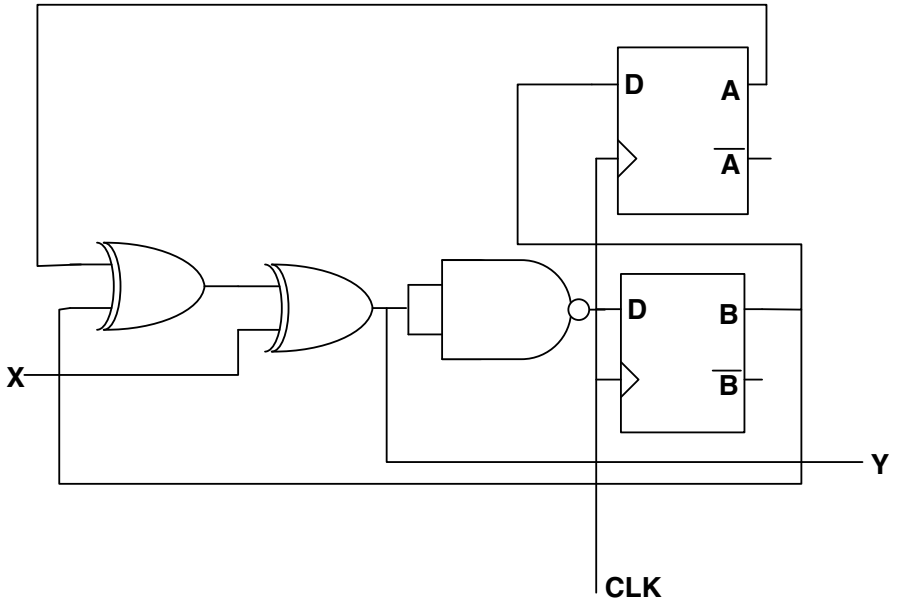


Figure 6.1: Sequential circuit with an input, an output and two DFFs

To understand the operation of this sequential circuit, we need to obtain the flip-flop and output equations, from which the state transition table and diagram of the circuit can be derived.

The Flip-flop input equations: $D_A = B$

$$D_B = \overline{A \oplus B \oplus X}$$

Output equation $Y = \overline{D_B}$

For D flip-flop, the next state is the same as the D flip-flop input, and hence we have

$$A(t+1) = D_A$$

$$B(t+1) = D_B$$

State transition table:

Present state	**Next state**		**Output**	
	X =0	**X =1**	**X = 0**	**X = 1**
AB	**AB**	**AB**		
00	**01**	**00**	**0**	**1**
01	**10**	**11**	**1**	**0**
11	**11**	**10**	**0**	**1**
10	**00**	**01**	**1**	**0**

Table 6.1: State transition table for the sequential circuit in Figure 6.1

State diagram:

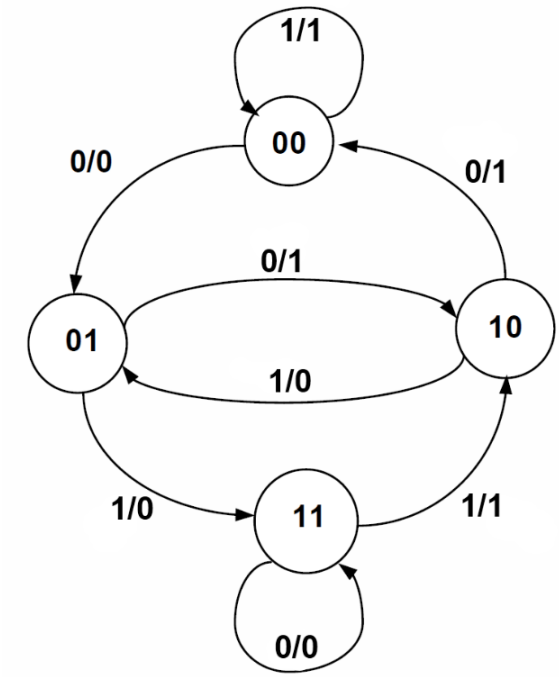


Figure 6.2: State diagram for the sequential circuit in Figure 6.1.

Can you predict what the sequential circuit does from the state diagram?

Implementing the above sequential circuit using ICs

The sequential circuit will be constructed using one 7474 Dual D-flip-flop ICs, a 7486 Quad XOR Gate IC, and a 7400 Quad NAND gate. The D-flip-flop comes with active-low *preset* and *clear* pins, which will be used to initialise the state of the register.

Referring to the datasheets for the 7474, 7486, and 7400 (given in the Appendix C), build the sequential circuit shown in Figure 6.1 on your breadboard. In order to observe the states of the D-flip flops and the output of the circuit, you need to connect LEDs at **A, B and Y** nodes (in Figure 6.1) of the circuit. The input at **X,** and the **PRESET** pins of the D-flip flops are set using slide switches.

In the implementation, we will use a push-button switch (a pulser) as a pulse generator to act as a clock to drive the sequential circuit. You have been provided with a push-button switch inside your laboratory kit. The schematic representation of the push-button switch is shown below

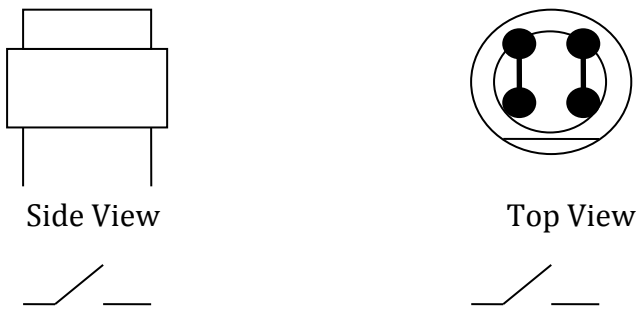


Figure 6.3: Schematic illustration of a push-button switch

Take notice that the push-button switch is not round all the way around its base. There is a flattened side; this flattened side must run parallel to the buses on your breadboard, otherwise the switch will not work! Use a resistor in combination with the push-button switch in a similar manner as the slide switches are used in the previous lab (refer to Figure 5.4).

When push button switches are used as a pulser, it is important to make sure that a single pulse is generated whenever the button is pressed and released. The common problem with push-button switch is that the contacts inside the switch

bounce off one another, causing multiple pulses to be generated every time the button is pushed. The following diagram illustrates the situation:

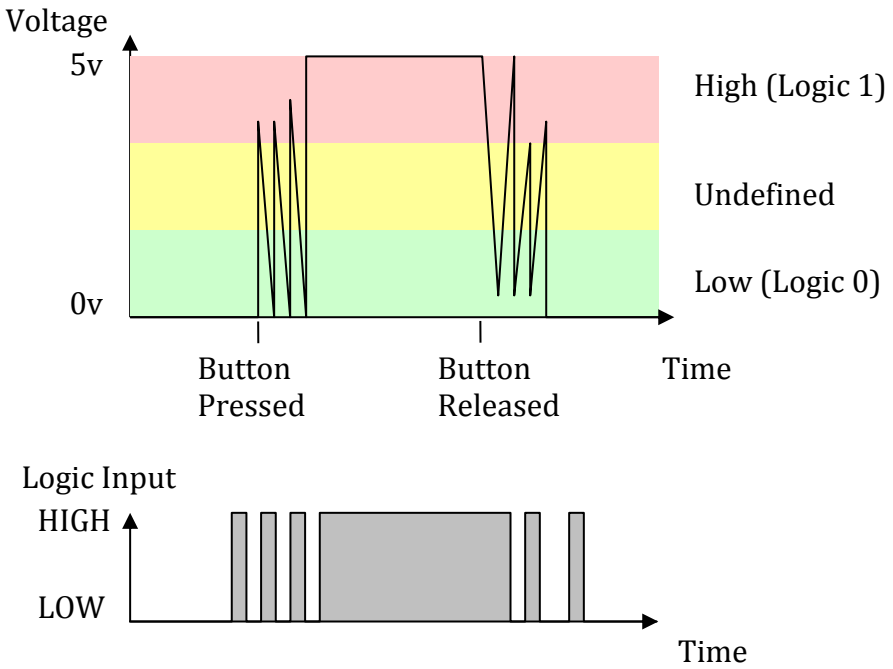


Figure 6.4: Waveform illustrating the problem with a push-button switch

A *debounce circuit* is used to eliminate the extra pulses due to the bouncing of the contacts in the push-button switch. The circuit below shows such a debounce circuit. This circuit comprises of a resistor-capacitor based (RC) *filter* and a *Schmitt trigger* buffer. The buffer is required to isolate the filter circuit from the inputs to the gates. If the buffer is not present, the filter capacitance adds with the input capacitance of all the gates. This capacitance is too large to charge/discharge and as a result the clock does not work.

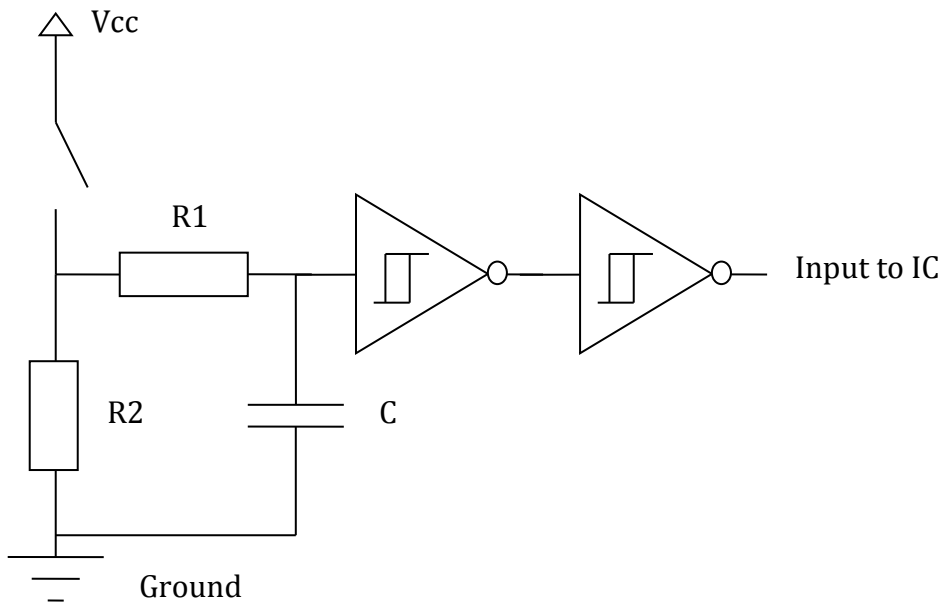


Figure 6.5: A push button switch with a denouncing circuit

RC Filter

The RC filter works by introducing a delay. The delay is achieved through the charge/discharge time of the capacitor. While charging/discharging, the input voltage level does not swing past the logic voltage threshold on the short pulses produced by the bouncing of contacts.

Schmitt Trigger

The Schmitt Trigger is a type of circuit that asserts its output high when its input exceeds a particular threshold value. The output will be asserted low only when a second, lower threshold level is reached. Schmitt triggers employ hysteresis in order to accommodate several transition conditions. The operation of the Schmitt trigger is best described with the diagram below which shows the input vs. output for a non-inverting Schmitt trigger. The arrows indicate the transition direction.

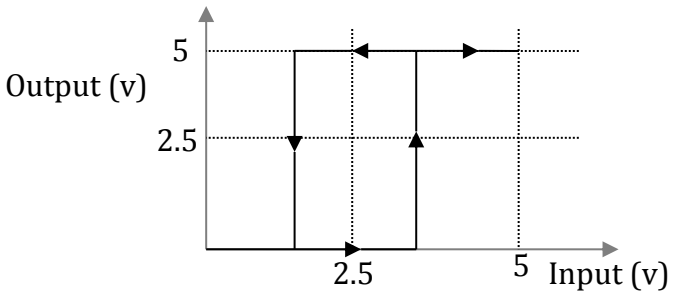


Figure 6.6: Hysteresis characteristics of Schmitt triggers

Schmitt triggers are commonly used in debouncing circuits because the hysteresis prevents transitional changes unless the lower or upper thresholds are reached. Thus, the effects of switching noise are greatly reduced. The symbol for the Schmitt trigger is given below. Schmitt triggers come in both non-inverting (left) and inverting (right) types.

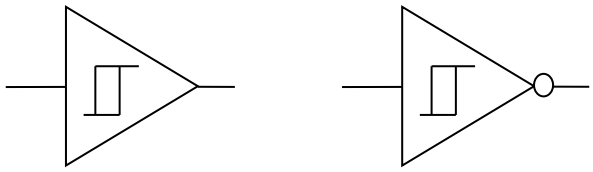


Figure 6.7: Schmitt trigger types (a) non-inverting (left), (b) inverting (right)

Exercise: Debounce Circuit

Construct the debounce circuit in Figure 6.5 for your push-button switch. Use R1 = 680Ω, R2 = 10kΩ and C = 1μF (notice that R2 is, in fact, already connected as your switch's pull-down resistor). Also use 7414 IC (Data sheet given in Appendix C), which has six inverting Schmitt triggers. What is the charge time of this circuit? Can you suggest a method to determine the minimum charge time required to absorb the bouncing effect of the switch? What might happen if we made the charge time very long? What about if we made it very short?

Verifying the sequential circuit as implemented on the breadboard

Collect all the **PRESET** lines from each of your flip-flop and wire them to the output of one of the slide-switches. Also, connect the input **X** to another slide-switch. Likewise, collect all the **CLOCK** lines from each of your flip-flops and

connect them to the push-button. Last, collect all the **CLEAR** lines and connect them to **Vcc**.

Make sure the **CLOCK** push-button is not pressed (i.e. the **CLOCK** signal is LOW). Initialise the circuit by applying the active-low **PRESET** signal: set the **PRESET** switch to LOW and then back to HIGH. Leave the switch in the HIGH position. What is the present state of the sequential circuit?

First switch the input to LOW position. Now toggle the **CLOCK** by pressing and releasing the push-button. A toggle on this button applies a clock signal to the flip-flop. What state does the sequential circuit transit to and what is the output of the circuit? Record the next state and output into Table 6.2 provided below.

Keep toggling the clock by pressing and releasing the push-button switch until you return to the initial state.

Present state	**Next state**		**Output (Y)**	
	X =0	**X =1**	**X = 0**	**X = 1**
AB	**AB**	**AB**		
00				
01				
11				
10				

Table 6.2: Experimental state transition table

Now switch the input to HIGH position and toggle the clock. Record the next state and output into Table 6.2. If the state does not change, switch the input to LOW position and toggle the clock and record the next state and output into Table 6.2

Repeat the above procedure until you fill the table.

Once the table is filled, compare it with the state transition table presented in Table 6.1. Is the comparison as you expect?

Starting from state 11, obtain the output sequence for the input sequence given Table 6.3.

Input sequence	**Output sequence**
0101000010	

Table 6.3: Output sequence

Demonstrate it to a lab demonstrator after you have verified your design.

Is the implementation optimal? Can it be minimized? If so, draw the minimized circuit and verify its equivalence to the sequential circuit shown in Figure 6.1.

Checkpoint 5	*Assessor*	*Marks (5)*	*Date*

— END —

Lab 6 – Counters and 7-Segment Display

Assumed Knowledge

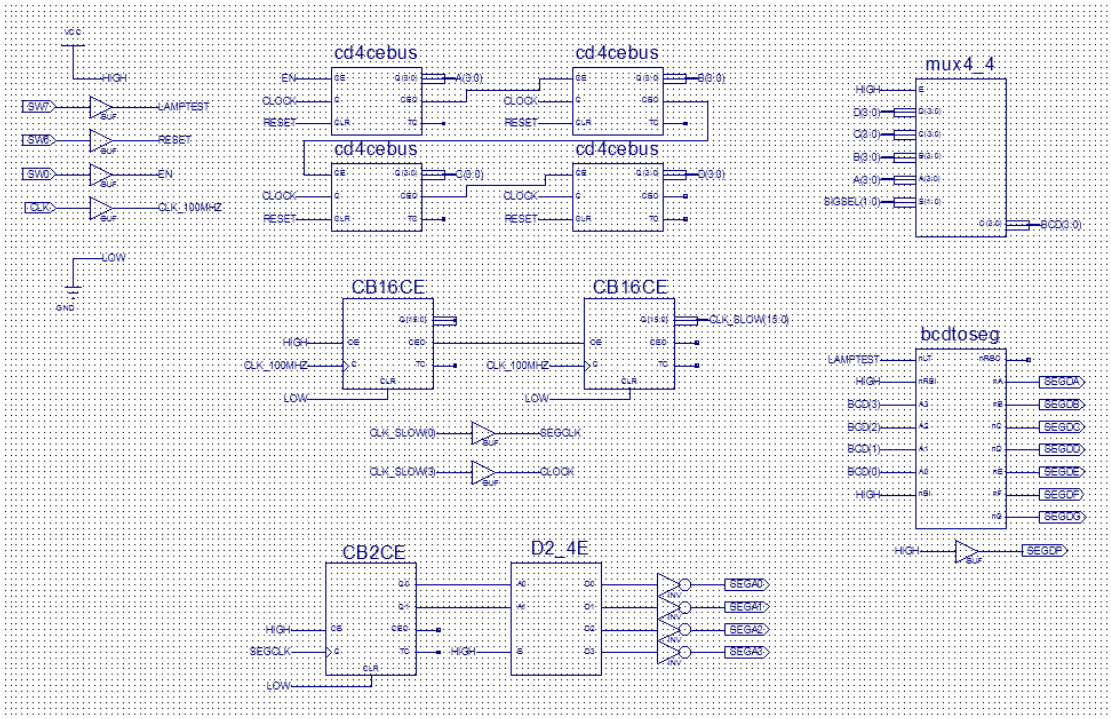
- You are able to create a project in Xilinx ISE.
- You are able to draw schematics in Xilinx ISE.
- You are able to simulate a design in Xilinx ISE.
- You know how to synthesise and implement a design in Xilinx ISE.
- You know how to assign nets to the pins of the Nexys 3 board in Xilinx ISE.
- You know how to download a design onto the Nexys 3 board via Digilent Adept.

In this lab, you will build a timer that counts at around 1Hz up to 10,000 seconds. This exercise introduces you to internal clocking, including how to derive a slower clock signal from a faster one using what is known as a *prescaler*.

The timer will require a 4-digit BCD counter. Making a 4-digit BCD counter requires the following logic devices:

- Four 4-bit BCD counters, one for each digit.
- A 4x4 multiplexer for displaying one digit at a time.
- A BCD to 7-segment decoder to display digits in human readable form.
- A clock signal for controlling the multiplexers (i.e. which digit is shown).
- A clock signal for the counter itself.

The final design for this exercise will look something like this:



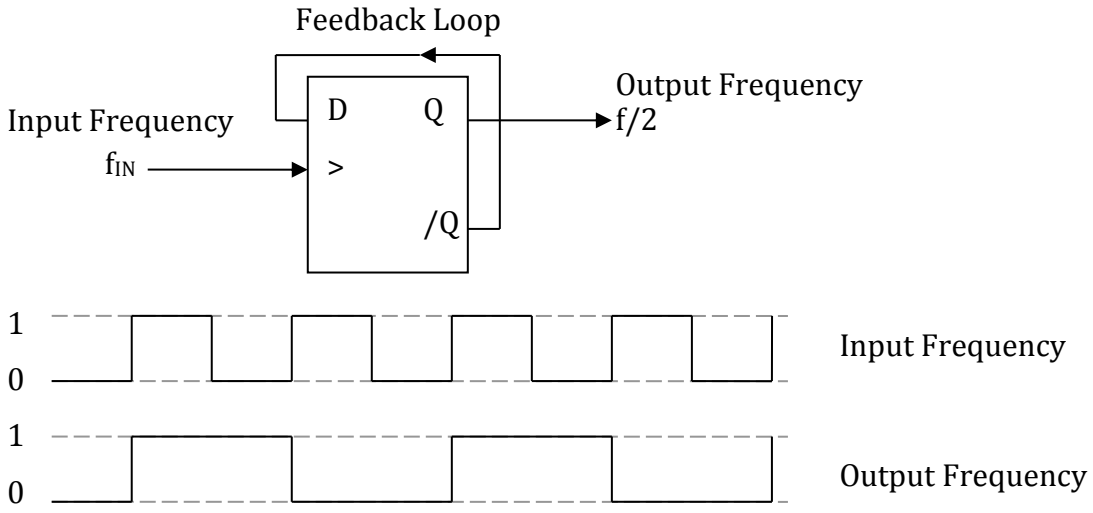
We will now design this in a section-by-section manner.

Before we embark into the design, brief introduction to counters is presented below

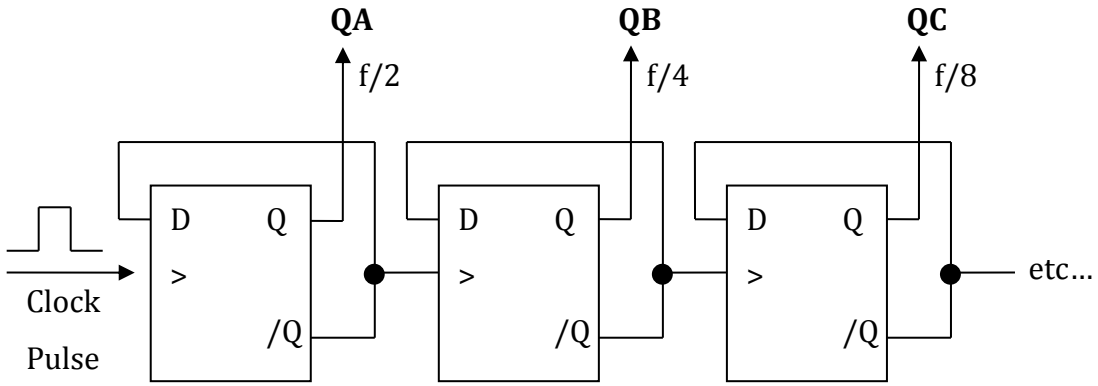
Binary Counter

A *counter* is a digital circuit which stores the number of times the clock signal has been toggled. There are many types of counters: binary, decade, modulo-n, Johnson, and so on. They each differ in their output sequences, but are all fundamentally similar.

The most basic counter is a 1-bit counter. It is essentially a D-flip-flop connected as a Toggle flip-flop. Because the D-flip-flop triggers once per clock cycle, the output toggles at half the frequency of the clock signal (make sure you understand why!). It should also be noted that regardless of the duty cycle of the clock signal, the duty cycle of the output clock will be 50% provided the input clock frequency is constant.



If we represent a 1-bit counter as a divide-by-2 block, we can cascade the blocks together by using the output of a previous stage to clock the next stage. In this way, we can make a divide-by-4 or divide-by-8 and so forth counter.



The count held by this counter is read in the reverse order from the order in which the flip-flops are triggered. Thus, output **QC** is the high order bit of the count (most significant bit, or MSB), while output **QA** is the low order bit (least significant bit, or LSB). The count held by the counter is then read as **CBA**, and runs from 000 (decimal 0) to 111 (decimal 7). This is a *3-bit binary counter* or *modulo-8 counter*.

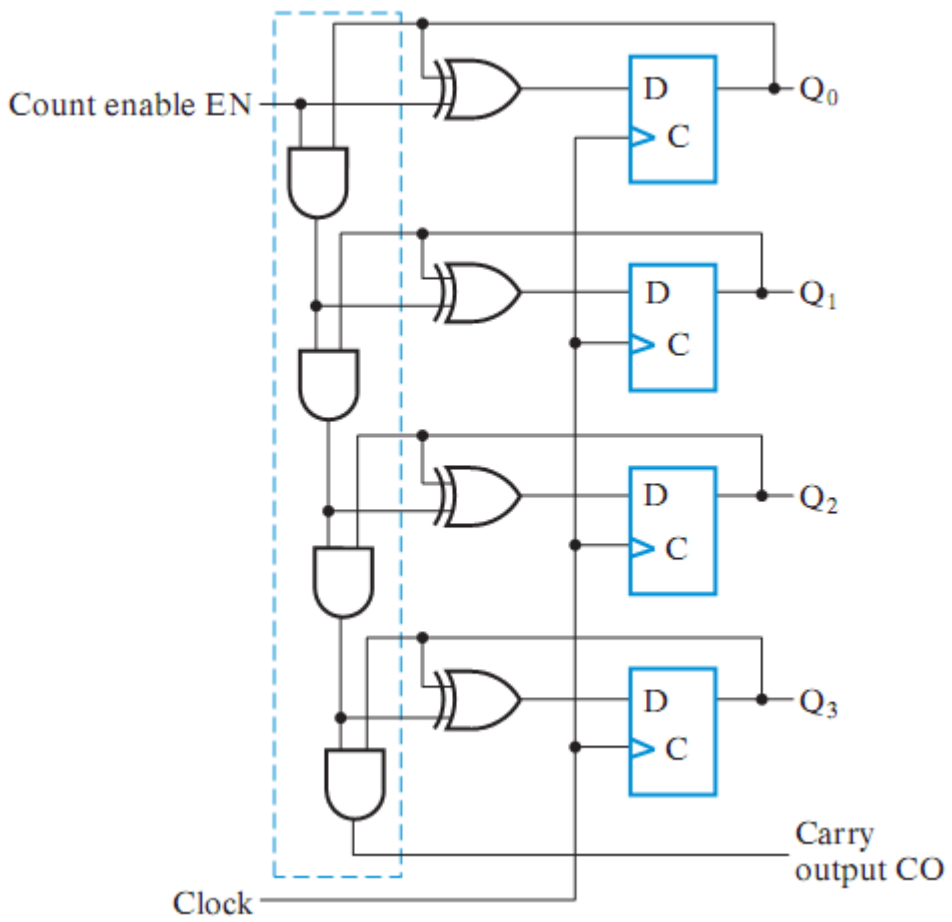
Cascading 1-bit counters up in such a fashion creates a *ripple counter*. One problem with the ripple counter is that the output does not change coherently. For example, when changing from 011 (decimal 3) to 100 (decimal 4), the

counter first changes the LSB, and at this moment the output becomes 010 (decimal 2) before the second stage D-flip-flop sees a new input and toggles to become 000 (decimal 0) and finally the third flip-flop will then see a new input and cause the output to flip over to 100 (decimal 4).

This causes no problem if the output is only to be read by human eyes – the ripple effect is too fast for us to perceive. However, if the count is to be used by other digital circuits (such as a multiplexer or demultiplexer), the ripple effect can cause unexpected circuit operation.

In order to prevent this, we need to be able to cause all of the flip-flops to change state at the same moment. This is known as a *synchronous counter*.

The diagram below shows an implementation of a 4-bit synchronous counter.



Xilinx provides an implementation of the 4-bit synchronous counter as a module named **CB4CE**.

Binary-Coded Decimal (BCD) Counter

Binary counters are the simplest device which can be used to count clock pulses. However, there is no simple way of displaying the count value in decimal format. Because of this fact, the *binary-coded decimal* (*BCD*) counter is commonly used instead. BCD is an encoding for decimal numbers in which each digit is represented by its own 4-bit binary sequence. By utilising BCD, the manipulation of numerical data for the display can be greatly simplified by treating each digit as a separate 4-bit BCD counter. By connecting the output of these BCD counters directly to a 7-segment LED display decoder, the values are shown in decimal.

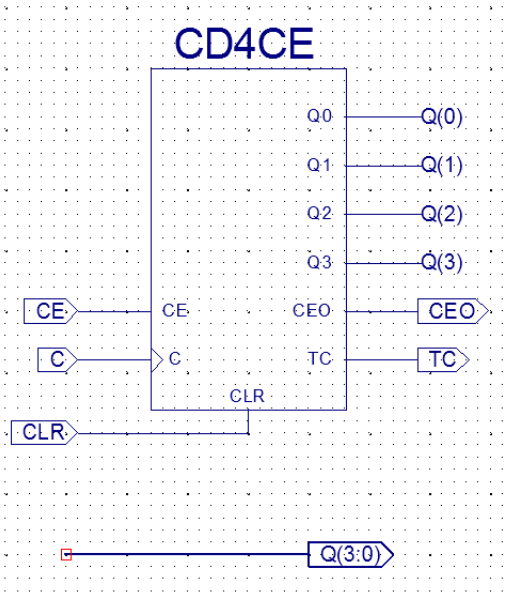
Implementation of a BCD counter is similar to a synchronous counter, except that the input to the D-flip-flop is a logic function of the current outputs. Xilinx has already provided an implementation of the 4-bit synchronous BCD counter as a module named **CD4CE**.

Design

Start a new project named **segmux** and create a blank top-level schematic of the same name. There are 4 digits to be displayed, and each digit has 4 bits. Hence we need four 4-bit BCD counters and a 4x4 multiplexer. For ease of connection we are going to use bus notation for the data line.

First, we must prepare the 4-bit BCD counter. The symbol provided by Xilinx does not use bus notation, so we will need to modify it. Add a new schematic named **cd4cebus.** Insert an instance of **CD4CE**. Connect wires to **Q0**, **Q1**, **Q2** and **Q3** such that the lines are extended outward. Name the wires **Q(0)** to **Q(3)** respectively by adding an I/O marker, then renaming it, clicking on the I/O marker and then pressing the **Delete** key. This tells Xilinx that these signals are part of a bus. Next, draw a wire somewhere underneath **Q0**, name it **Q(3:0)** and connect an I/O marker at the other end. Notice the line becomes thicker,

indicating Xilinx recognises that **Q** is a bus. Attach I/O markers to all the remaining pins and label them with the names as in the diagram below.



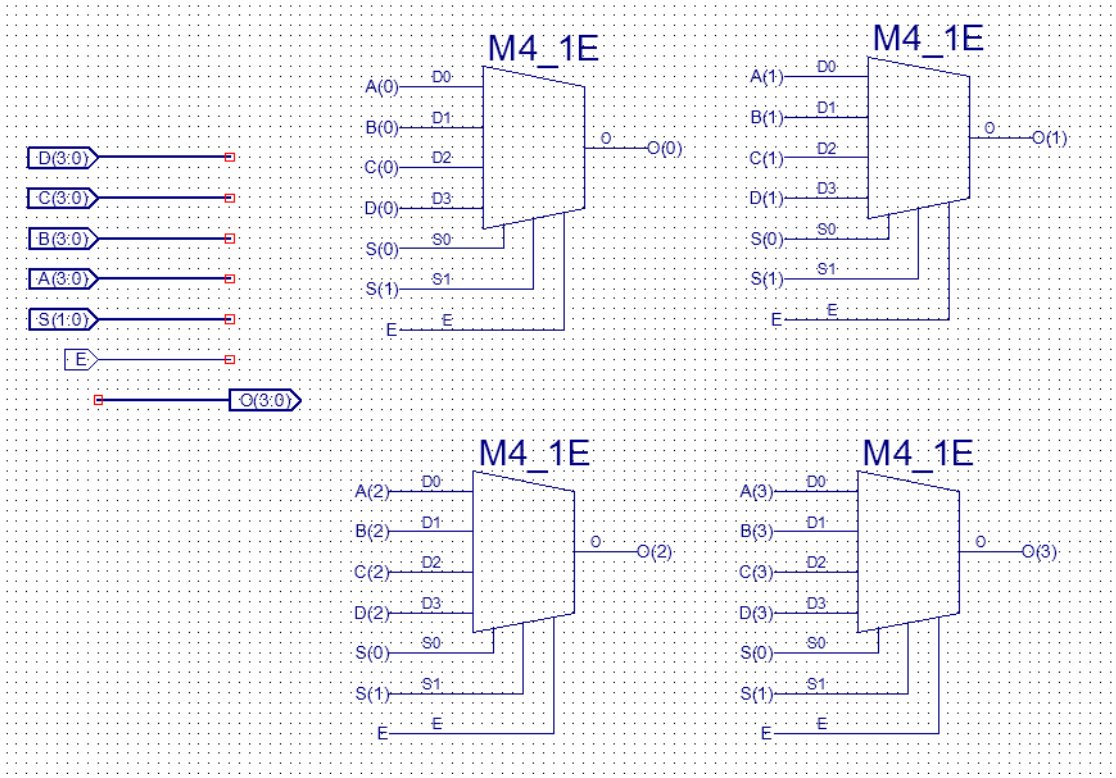
Save the schematic and use it to create a symbol.

Tools → Symbol Wizard

OR

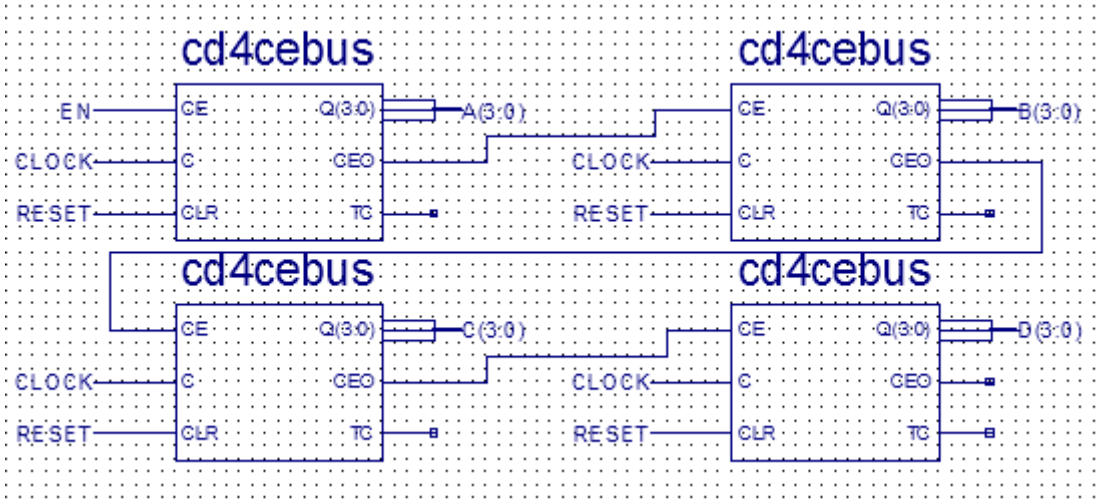
Processes Pane → Design Utilities → Create Schematic Symbol

The next step is to create the multiplexer. Again, Xilinx does not provide us with a 4x4 multiplexer, so we can instead make our own using 4x1 multiplexers. Essentially each multiplexer selects a bit from one of the four digits, and all four multiplexers can share the same selector bits because they are selecting the same digit. Add a new schematic named **mux4_4** and insert four **M4_1E** 4x1 multiplexers. Label the nets and I/O markers as in the following diagram:



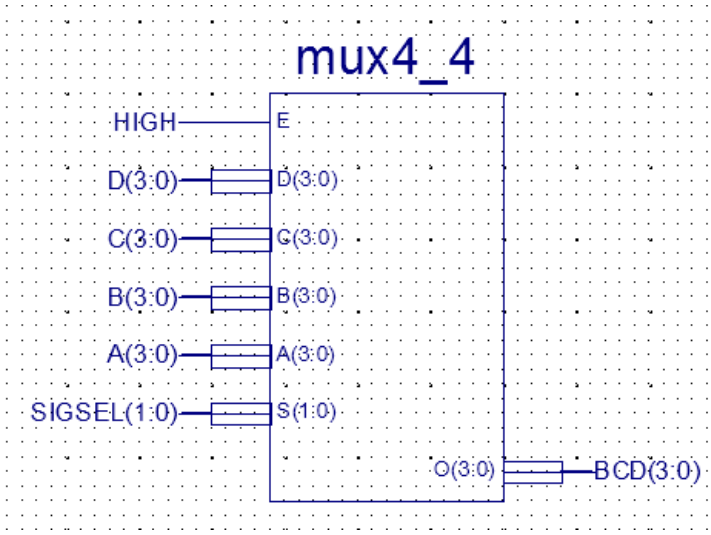
You will notice that **E**, **S(0)**, and **S(1)** are common to multiple **M4_1E**s. You will be warned that **There is already a net named xxxx. Do you want to merge them?** Select **Yes**. Save the schematic and create a symbol for it as well. We do not need to make a decoder as the one provided by Xilinx is sufficient for our purposes.

Open the top-level **segmux** schematic. We will now prepare the synchronous BCD counter. Insert four **cd4cebus** symbols and arrange them in a 2x2 layout. The **CLR** pin of each counter will be connected to a net named **RESET**, while the clock pin **C** will be connected to the counter clock named **CLOCK.** Chain the counters together by connecting **CEO** of the previous stage to **CE** of the next stage. This signal is generated on the negative edge when the counter rolls over from 9 to 0. Connect **EN** to **CE** of the first stage. **A(3:0)** will be the right-most digit while **D(3:0)** will be the left-most digit.



To rename the buses, right-click the I/O marker you have added, select **Rename Bus…** and then under **New Base Name of Bus**, type **A** (for example **A(3:0)**) and click **OK**. Select the I/O marker, and press the **Delete** key to remove the I/O symbol, leaving only its name. Repeat for all the other buses.

Next we insert the multiplexer **mux4_4**. **SEGSEL(1:0)** will be used to select which digit is to be displayed. The Enable signal (pin **E**) of the multiplexer will be connected to a net named **HIGH**, which we will later connect to a constant logic 1. **BCD(3:0)** will be the input of the BCD to 7-segment decoder.



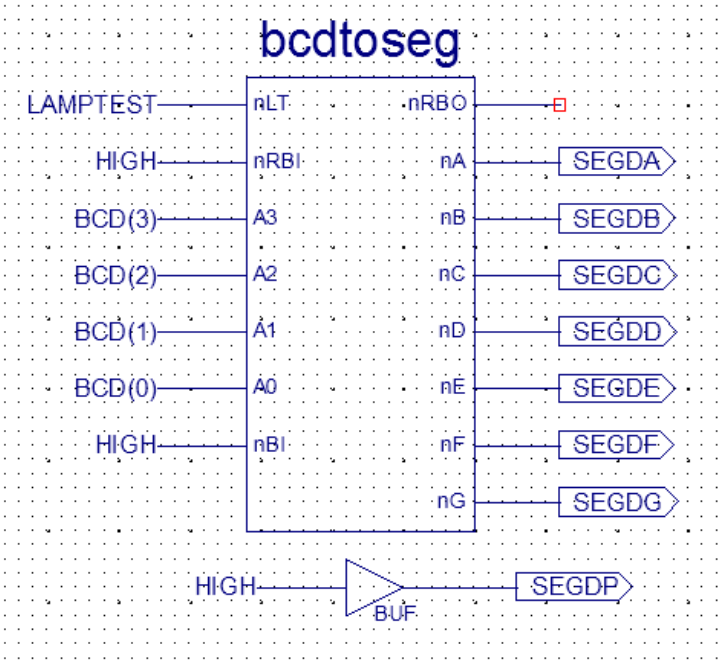
In order to add the buses **A(3:0)** to **D(3:0)**, we must merge them to the existing nets. You can do this by selecting the I/O marker, select **Rename Port** under the

right-click menu, choose to **Rename the Branch** and put in the full name of the branch – e.g. **A(3:0)**. Click **OK** and then use the **Delete** key to leave only its name.

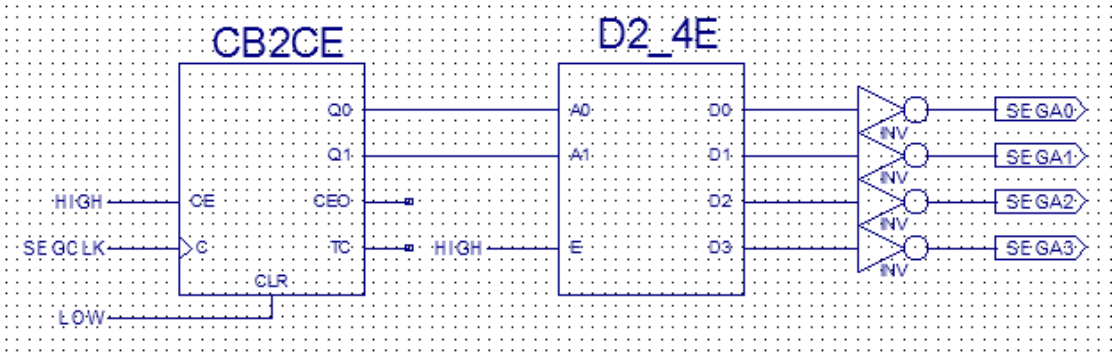
Next we connect the multiplexer output to the BCD decoder, which is simply 7474 IC. A module, written in Verilog, has been supplied to mimic such a chip. Copy the module file, which can be found from the Moodle page of the course at **lab7\bcdtoseg.v** to your personal USB-drive and **Add this Source** and create a new symbol for this.

As this is the last stage of the logic, we would like to have some means of debugging the circuit if the output is not displaying the patterns that we expect. In order to do this, we've added a function to the circuit that tests the display. **LAMPTEST** is a push-button connected to a decoder that tests the illumination of the display. If only one display is illuminated, then we know that there is a problem with the multiplexer. If all displays are illuminated, but the number is not changing, we know there is a problem with the BCD counter.

SEGDP is turned off by connecting it to logic 1. **RBO** is not used and is left unconnected. The remaining outputs are connected to segment data lines **SEGD*x***. **RBI** and **BI** are not used, and so they are connected to logic 1. The decoder inputs are connected to the multiplexer outputs via the **BCD** bus. This is shown in the diagram below.



So far we have the logic to display one digit at a time, but we need a way to automatically periodically rotate which digit we are displaying. To do this, we are going to use a 2-bit counter, which rotates the illumination of each display. Insert a **CB2CE**, a 2-bit binary counter, and a **D2_4E**, a 2-bit decoder, and connect them as shown.



Make sure you right-click on the wire connecting between **Q0** and **A0** and choose **Rename the Selected Net...** and rename it to **SIGSEL(0)**. Likewise, name the wire connecting **Q1** to **A1** as **SIGSEL(1)**.

The net called **LOW** serves as logic 0. We will connect this later. A logic 0 connection to **CLR** of **CB2CE** means the counter will never be reset manually. A **HIGH** to **CE** of **CB2CE** means the counter will always count. **SEGCLK**, a clock

signal which will be generated later, is the rate at which the displays will be cycled through. Note that the frequency of **SEGCLK** is dependent on how long we want each display to be illuminated for, and how frequent we need to refresh each display such that our eyes are tricked into seeing a solid display. In the Nexys3 reference manual (Appendix A), it is indicated that this clock frequency should be around 1 KHz. This clock signal will be supplied by the prescaler to be built later, which uses the high frequency clock signal supplied by the Nexys3 board.

The counter outputs are connected to the decoder. The purpose of the decoder is to select one output at a time. For example, if the input is 2, then **D2** is set to 1 while the other outputs are set to 0. Because the **SEGA*x*** pins are active low (i.e. we turn the display on by setting logic 0), we need to connect inverters between the outputs of the decoder and **SEGA*x***. A **HIGH** signal connected to the Enable pin **E** of the decoder keeps the decoder running permanently.

The final block to be added is the clock prescaler. A prescaler is an electronic counting circuit used to reduce a high frequency electrical signal to a lower frequency by integer division. A prescaler is essentially a counter-divider – a BCD counter can be used as a divide-by-2 or divide-by-5 counter, while a binary counter can only be used as a divide-by-2.

A 100 MHz clock is supplied to the FPGA by the clock generator on the development board. We will need two new clock signals at frequencies of around 1 KHz and 1 Hz. Considering we are only going to use a binary counter, how many times do we need to divide a 100 MHz clock signal by 2 to get 1 KHz? We use the following formula:

Number of times we need to halve the frequency =

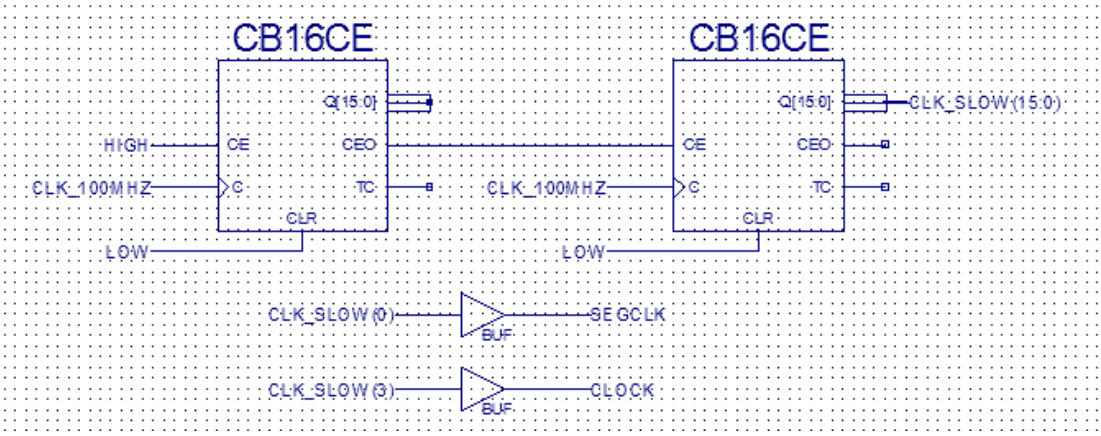
$$\log_2 (\text{Faster Frequency} / \text{Slower Frequency})$$

So for the 1 KHz signal, we need:

Number of times we need to halve the frequency =

$$\log_2 (100 \times 10^6 / 1 \times 10^3) = 16.6...$$

So, if the input clock to a binary counter is 100 MHz, the 17th bit of the output will have a frequency just slightly under 1 KHz. However, the largest binary counter provided by Xilinx is only 16-bit, therefore we need to cascade the two counters together by connecting **CEO** of previous stage to **CE** of next stage.

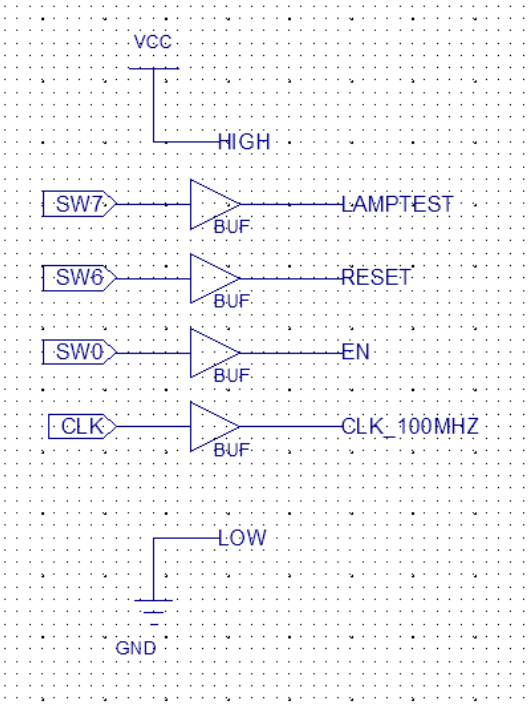


Note that bit 0 of the next stage is bit 16 of the overall counter. Likewise, bit 1 of the next stage is bit 17 of the whole counter. You can use this technique to slow the clock down even more.

Question: How many times do we have to halve the frequency to get 1 Hz for the timer from 100 MHz? Show all working below. Indicate which output bit you will use to drive the clock.

After picking the output bits for clock driving, we need to use a buffer to distribute the clock signal to the BCD counter and multiplexer counter. The reason why we can't clock the circuit directly from the counter output is due to the *fan-out limit* of each gate. Detailed explanation about fan-out limit of gates is beyond the scope of this course.

Finally, we interface the inputs to switches and push-buttons. It is suggested that **SW7** will be used for **LAMPTEST**, **SW6** for **RESET** and **SW0** for **EN**. **CLK** is connected to the on-board clock generator.



Verification on FPGA

We have already constructed the bulk of the BCD timer. The final piece of the puzzle is creating a constraints file for pin mapping. For your convenience, the table below summarises all of the pin connections needed for this exercise.

Net Name	**Pin**
SW0	T10
SW6	V8
SW7	T5
CLK	V10
SEGA0	N16
SEGA1	N15
SEGA2	P18
SEGA3	P17

Net Name	**Pin**
SEGDA	T17
SEGDB	T18
SEGDC	U17
SEGDD	U18
SEGDE	M14
SEGDF	N14
SEGDG	L14
SEGDP	M13

When you have completed the constraints file, implement the design. You will get warnings corresponding to **CLK_SLOW<15:4>** and **CLK_SLOW<2:1>** – these are only warnings and we can ignore these as we do not use those outputs. You may also get warnings about excessive clock skew, and unconnected **CEO** which are of no big consequence to this design. If no other errors occur, generate the programming file and upload the design to the FPGA.

To test the timer, first turn **SW0**, **SW6** and **SW7** off. All four 7-segment displays should be illuminated. If not, there is a fault within the multiplexer. Next turn **SW7** on and toggle the **SW6** switch. The display should be showing 0000 now. If not, there is a fault within the BCD counter. Finally, turn **SW0** on and the timer should begin counting from 0000. Turning **SW0** off should pause the timer.

Demonstrate the design to your demonstrator when your timer is running correctly.

Checkpoint 6	*Assessor*	*Marks (5)*	*Date*

— END —

Lab 7 – Electronic Handball Game

In this lab, you will be building a digital circuit design using Verilog that will implement: (i) a 1Hz clock (or faster) generator from the onboard 100MHz clock; (ii) bidirectional shift register with parallel load and (iii) an electronic handball game, where a player has to push a push-button switch on time to return a lamp ball (simulate a hand ball) that bounces back from the other end to stay in the match.

When designing digital circuits, we have the option of choosing a schematic-based design tool or one based on a Hardware Description Language, otherwise known as a HDL. Previously, you have used a schematic-based design tool to design your circuits; in this lab, we will instead be using Verilog to describe our design. You have already had some exposure to Verilog in the labs in building the Verilog Test Fixtures which were used to simulate your circuits – now you will design your actual circuit with it as well.

Design specification

You will build an electronic game of a hand ball. The hand ball is simulated by a moving lamp ball. At the start of the game, a single light is positioned at the leftmost position and it will start to move in the right direction when a player presses a *push-button* switch. The light reverses direction at the rightmost position and moves to the left. The player has to press the push-button again to reverse the direction of the light to right. If the player presses too soon or too late, the ball disappears and the light goes off and game over!

The circuit should have a *reset* switch to initialize the game at any time and *start* switch to place the light at the leftmost position initially. Both *start* and *reset* switches should be off during the game.

For this design, you will use the eight LEDs on the Nexy board to mimic the moving hand ball with LED7 being the starting position at leftmost and LED0 being the rightmost position. You may also use PB0 as the push-button switch, SW0 as reset switch and SW1 as start switch.

We will design the electronic game using an 8-bit Bi-directional shift register with parallel loading. The speed at which the light moves to the right and left depends on the clock that drives the shift register. If it is so fast, the player will not be able to respond on time. If it is too slow, the game will not be interesting or challenging. The on-board clock runs at 100MHz and will be too fast to drive the shift register. In this design, we will design a module that converts the fast on-board clock into a slower clock for driving the shift register and appropriate for the game. The other module we will need to design is an 8-bit bi-directional shift register with parallel loading. The block diagram for the complete design is illustrated in Figure 8.1.

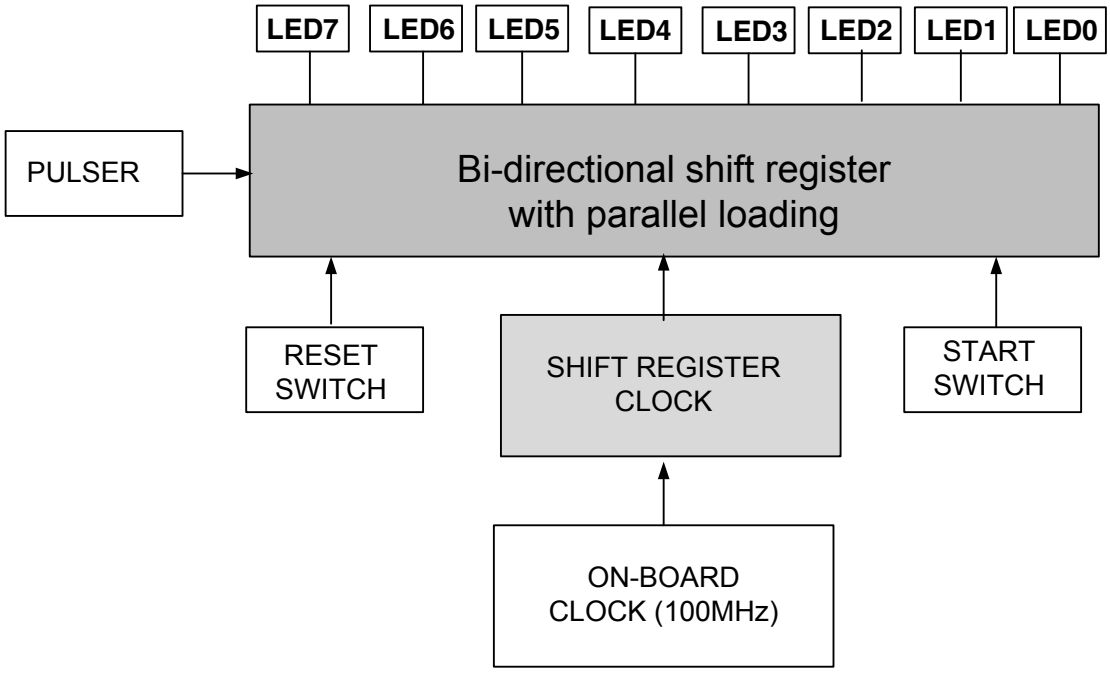


Figure 8.1: Block diagram for the complete design

Exercise: Shift register clock Module

Start a new project in Xilinx ISE called **LAMPBALL**, however, this time choose **HDL** under the **Top-level source type** dropdown.

The first module to be built is the *shift register clock* module. To create this module, click **New source** under **Project** menu and select **Verilog module** and enter **Shiftclock** in **File name** textbox. In **Define Module** window, enter port names and directions. The shift register clock module will have one input port,

named CLKIN, and one output port CLKOUT. Click **NEXT**, which takes you to the **summary** window that lists all the port names and directions. Click **Finish** to create the Verilog module (Shiftclock.v), which looks like Figure 8.2.

```
`timescale 1ns / 1ps
////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date:    07:23:22 01/22/2014
// Design Name:
// Module Name:    shiftclock
// Project Name:
// Target Devices:
// Tool versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
////////////////////////////////////////////////////////////////////////////////
module shiftclock(
    input CLKIN,
    output reg CLKOUT
    );

reg [25:0] counter;
parameter C0 = 26'd50000000;

// Your code goes here.

endmodule
```

Figure 8.2: Verilog module for a shift register clock

The module has only port declarations at this stage. It requires codes to be written so that it does what it is intended for. The function of the module is to create a slower clock from the fast onboard clock (100MHz). The first thing we need to decide is on the frequency of the slower clock. For the slower clock frequency of 1Hz, the module will have to output HIGH for 50million cycles of the onboard clock frequency and then LOW for the next 50million cycles of the clock frequency. This pattern will have to be repeated to generate the 1Hz clock.

Modify your module to include a 26–bit register counter and a parameter, C0, with a constant value of 26'd50000000.

Question: What do the constant, C0, stand for? Why do we need 26-bit register type?

Complete the module by writing the appropriate Verilog code that makes use of the constant and produces the 1Hz slow clock frequency.

We will test this code by generating a bit file to load onto the FPGA, but first, we need to create an appropriate constraints file to map the input and output to their respective pins. The input (**CLKIN**) for the module is the onboard clock, which is located at the pin "**V10**" and the output (**CLKOUT**), the generated clock, can be connected to one of the LEDs on board, say LED7, which is located at pin "**T11**". Create the constraints file (**Shiftclock.ucf**) and add it to the project.

Synthesize, **Implement** and **Generate Programming File** as you normally would. You should receive all green ticks. If so, use **Digilent Adept** to load **Shiftclock.bit** to the board and verify that your slow clock (shift register clock) generator works as expected that is the LED7 is switching ON and OFF in approximately 1s. If all is okay, proceed to create the next module.

Bi-directional Shift register with parallel load

The characteristics of an 8-bit bi-directional shift register with parallel loading, shown in Figure 8.3, is illustrated in table 8.1. The module has four functions, which is selected through S_o and S_1 inputs. When both S_o and S_1 are 0's, the 8-bit output remains unchanged. When both S_o and S_1 are 1's, the 8-bit inputs are loaded to the output bits at the arrival of positive edge clock. Let Q_A be the MSB of the value stored in the shift register, and Q_H be the LSB. When S_o is 1 and S_1 is 0, the output bits are shifted to right from Q_A to Q_H direction with Q_A taking the value of a serial input bit at **SIR**. When S_1 is 0 and S_1 is 1, the output bits shifted to left from Q_H to Q_A with Q_H taking the value of a serial input bit at **SIL**. The module can only perform four functions if the clear input (**CLR**) is HIGH otherwise all the output bits clears to 0's.

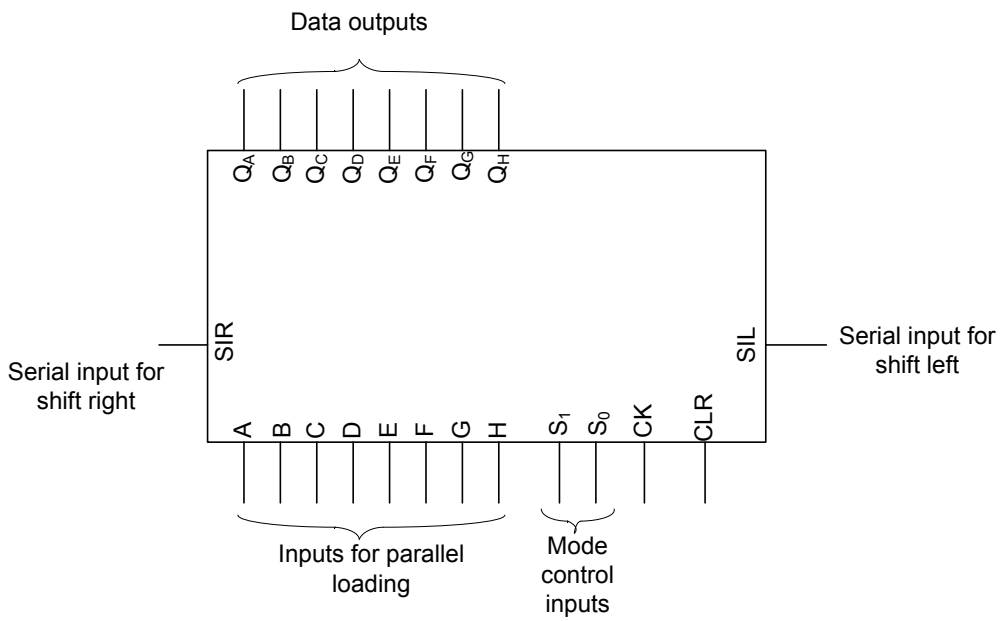


Figure 8.3: Schematic diagram of bi-directional shift register with parallel loading

Clear (CLR)	Clock (CK)	S_1	S_o	
0	X	X	X	Clear output bits to 0
1	↑	0	0	Output bits remain unchanged
1	↑	0	1	Shift right in the direction from Q_A to Q_H. SIR to QA
1	↑	1	0	Shift left in the direction from Q_H to Q_A. SIL to QH
1	↑	1	1	Parallel-load input data

Table 8.1: Characteristics of Bi-directional shift register

Now, we will create a Verilog module for the 8-bit bidirectional register with parallel load. To create this module, click **New source** under **Project** menu and select **Verilog module** and enter **Bidshift** in **File name** textbox. In **Define Module** window, enter port names and directions. The Bidshift module has six input ports (SRIN[7:0], SEL[1:0], CK, CLEAR, SIL,SIR) and one output port (SROUT[7:0]). Click **NEXT**, which takes you to the **summary** window that lists all the port names and directions. Click **Finish** to create the Verilog module (Bidshift.v), which looks like Figure 8.4.

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date:    13:05:53 01/22/2014
// Design Name:
// Module Name:    Bidshift
// Project Name:
// Target Devices:
// Tool versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////
module Bidshift(
    input [7:0] SRIN,
    input [1:0] SEL,
    output reg [7:0] SROUT,
    input CK,
    input CLEAR,
    input SIL,
    input SIR
    );
// Your code here

endmodule
```

Figure 8.4: Verilog module for Bi-directional register

The module has only port declarations at this stage. It requires codes that describe the behaviour of the 8-bit bi-directional shift register to be inserted into the module so that it does what it is intended for.

Complete the module by writing the appropriate Verilog code.

You will test this code by generating a bit file to load onto the FPGA. For that, you will need to create an appropriate constraints file to map the input and output to their respective pins and you will also need to set Bidshift.v as the top level module(right click on Bidshift.v and select Set as Top Module). Since you do not

have enough slide switches to use as input pins for the test, you may want to initialize the 8-bit inputs in the code using a keyword *assign*. For example, if you want to set all the 8-bit inputs to LOW.

```
assign  SRIN = 8'b00000000;
```

For the other input and output ports, you may use the pin-port association listed in Table 8.2. Although CK is associated with pin A8, the clock that drives the shift register should be slow enough to allow you to visually test the shifter module. This can be done by instantiating the Shiftclock module within the Bidshift module. The input to the instantiated module will be CK and the output of the shiftclock module will drive the bidirectional shifter. Create the constraints file (**Bidshift.ucf**) and add it to the project.

Ports	pins	Ports	pins
SEL[1]	SW3 (M8)	SROUT[7]	LED7 (T11)
SEL[0]	SW2 (V9)	SROUT[6]	LED6 (R11)
CK	V10	SROUT[5]	LED5(N11)
CLEAR	SW1 (T9)	SROUT[4]	LED4(M11)
SIL	SW0 (T10)	SROUT[3]	LED3(V15)
SIR	SW4 (N8)	SROUT[2]	LED2(U15)
		SROUT[1]	LED1(V16)
		SROUT[0]	LED0(U16)

Table 8.2: Ports and pins mapping for bidshift

Synthesize, **Implement** and **Generate Programming File** as you normally would. You should receive all green ticks. If so, use **Digilent Adept** to load **Bidshift.bit** to the board and verify that the bidirectional shift register works as expected. You may find recording your observation useful in the following table when you verify the operation of the bidirectional shift register.

SW0	SW1	SW2	SW3	SW4	Outputs (LEDs)[LED7:LED0]
1	0	X	X	1	
1	1	0	0	1	
1	1	1	0	1	
1	1	0	1	1	
1	1	1	1	1	

Table 8.3: Recording table for veryfying the operation of bidirectional shift register

Electronics handball game

The last module to create is the handball game module. The two modules built earlier will be used in this third module. The module will have four single bit input ports and one 8-bit bus output port.

Create a Verilog module for the handball game by clicking **New source** under **Project** menu, selecting **Verilog module** and entering **Handball** in **File name** textbox. In **Define Module** window, enter port names and directions. You may name the input ports as **PULSER, RESET, START, and CLKK** and the output bus as **LGOUT[7:0]**. Click **NEXT**, which takes you to the **summary** window that lists all the port names and directions. Click **Finish** to create the Verilog module (**Handball.v**), which looks like Figure 8.5.

```
`timescale 1ns / 1ps
////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date:    13:05:53 01/22/2014
// Design Name:
// Module Name:    Bidshift
// Project Name:
// Target Devices:
// Tool versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
////////////////////////////////////////////////////////////////////////////////
module Lampball2(
    output [7:0] LGOUT,
    input PULSER,
    input START,
    input RESET,
    input CLKK
    );
```

```
reg [1:0] S;
wire [7:0] LGIN;
wire MSB_IN, LSB_IN;

assign MSB_IN = 1'b0;
assign LSB_IN = 1'b0;
assign LGIN = 8'b10000000;


Shiftclock  SG1(CLKK,P);
Bidshift BS1(LGIN,S,LGOUT,P,RESET,MSB_IN,LSB_IN);
//Your code goes here

endmodule
```

Figure 8.5: Verilog module for electronics handball game

At this stage, the module has only port declarations. It requires codes that describe the behaviour of the game as provided in the design specification to be inserted so that it does what it is intended for.

Complete the module by writing the appropriate Verilog code. In order to help you with the Verilog code, the instantiations of **Shiftclock** and **Bidshift** modules and associated registers, wires and their assignments are included in Figure 8.5. You may need to create other registers depending on your particular approach.
Recall the game should behave as follows:

- At the start of the game, a single light is positioned at the leftmost position and it will start to move in the right direction when a player presses a *push-button (PULSER)* switch.
- The light reverses direction at the rightmost position and moves to the left.
- The player has to press the *push-button (PULSER)* again to reverse the direction of the light to right at the leftmost position. If the player presses too soon or too late, the ball disappears and the light goes off and game over!
- The circuit should have a *reset (RESET)* switch to initialize (clear all the LEDs) the game at any time and *start (START)* switch to place the light at the leftmost position initially.

- Both *start (START)* and *reset (RESET)* switches should be off during the game.

You will test your code by generating a bit file to load onto the FPGA. For that, you will need to create an appropriate constraints file to map the input and output to their respective pins and you will also need to set **Handball.v** as the top level module(right click on Bidshift.v and select Set as Top Module). The mapping follows what is stated in the design specification earlier. It is provided in the table below for convenience.

Ports	pins	Ports	pins
RESET	SW0 (T10)	LGOUT[7]	LED7 (T11)
START	SW1 (T9)	LGOUT[6]	LED6 (R11)
CLKK	V10	LGOUT[5]	LED5(N11)
PULSER	PB0 (C4)	LGOUT[4]	LED4(M11)
		LGOUT[3]	LED3(V15)
		LGOUT[2]	LED2(U15)
		LGOUT[1]	LED1(V16)
		LGOUT[0]	LED0(U16)

Table 8.4: Ports and pins mapping for Handball

Create the constraints file (**Handball.ucf**) and add it to the project.

Synthesize, **Implement** and **Generate Programming File** as you normally would. You should receive all green ticks (or Yellow warning may also be fine). If so, use **Digilent Adept** to load **Handball.bit** to the board and verify that the electronic game works as expected.

Increase the speed of the hand ball by increasing the clock frequency generated by the Shiftclock.v module to 20Hz, then 50Hz, and test your game and show to your demonstrator.

Checkpoint 7	*Assessor*	*Marks (5)*	*Date*

— END

Appendix A – Digilent Nexys 3 Board Reference Manual

1300 Henley Court
Pullman, WA 99163
509.334.6306
www.digilentinc.com

Nexys 3™ FPGA Board Reference Manual

Revised April 11, 2016
This manual applies to the Nexys 3 rev. B

Overview

The Nexys 3 is a complete, ready-to-use digital circuit development platform based on the Xilinx Spartan-6 LX16 FPGA. The Spartan-6 is optimized for high performance logic, and offers more than 50% higher capacity, higher performance, and more resources as compared to the Nexys 2's Spartan-3 500E FPGA.

Features include:

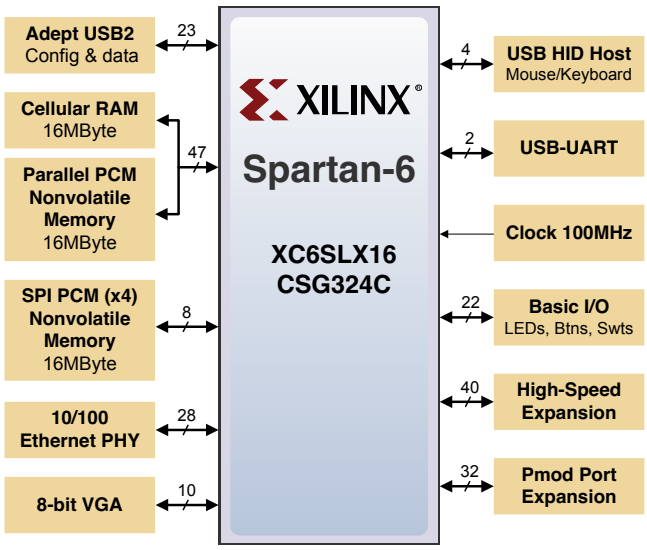
- Xilinx Spartan-6 LX16 FPGA in a 324-pin BGA package
- 16Mbyte Cellular RAM (x16)
- 16Mbytes SPI (quad mode) PCM non-volatile memory
- 16Mbytes parallel PCM non-volatile memory
- 10/100 Ethernet PHY
- On-board USB2 port for programming & data xfer
- USB-UART and USB-HID port (for mouse/keyboard)
- 8-bit VGA port
- 100MHz CMOS oscillator
- 72 I/Os routed to expansion connectors
- GPIO includes 8 LEDs, 5 buttons,8 slide switches and 4-digit seven-segment display
- USB2 programming cable included

In addition to the Spartan-6 FPGA, the Nexys 3 offers an improved collection of peripherals including 32Mbytes of Micron's latest Phase Change nonvolatile memory, a 10/100 Ethernet PHY, 16Mbytes of Cellular RAM, a USB-UART port, a USB host port for mice and keyboards, and an improved high-speed expansion connector. The large FPGA and broad set of peripherals make the Nexys 3 board an ideal host for a wide range of digital systems, including embedded processor designs based on Xilinx's MicroBlaze.

Nexys 3 is compatible with all Xilinx CAD tools, including ChipScope, EDK, and the free WebPack. The Nexys 3 uses Digilent's newest Adept USB2 system that offers FPGA and ROM programming, automated board tests, virtual I/O, and simplified user-data transfer facilities.

A comprehensive collection of board support IP and reference designs, and a large collection of add-on boards are available on the Digilent website. Please see the Nexys 3 page at www.digilentinc.com for more information.

Copyright Digilent, Inc. All rights reserved.
Other product and company names mentioned may be trademarks of their respective owners.

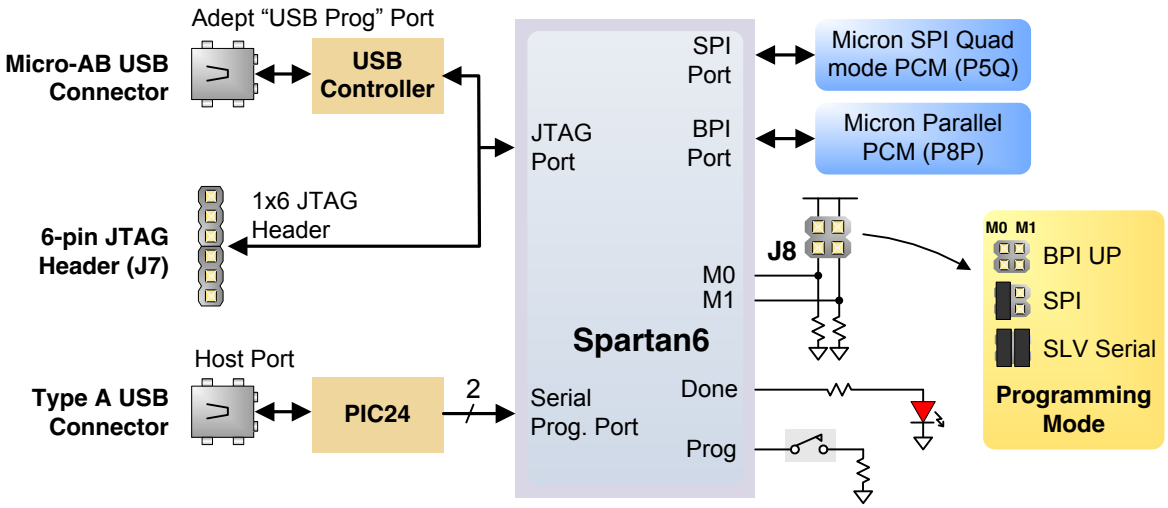


Spartan-6 LX16 features include:

- 2,278 slices each containing four 6-input LUTs and eight flip-flops
- 576Kbits of fast block RAM
- two clock tiles (four DCMs & two PLLs)
- 32 DSP slices
- 500MHz+ clock speeds

1 Configuration

After power-on, the Spartan-6 FPGA board must be configured (or programmed) before it can perform any functions. The FPGA can be configured in one of four ways: a PC can use the Adept "USB Prog" port to program the FPGA any time power is on; a configuration file stored in the non-volatile parallel PCM device can be transferred to the FPGA at power-on using the BPI-UP port; a file stored in the non-volatile serial (SPI) PCM device can be transferred to the FPGA using the SPI port; or a programming file can be transferred from a USB memory stick attached to the USB HID port. An on-board "mode" jumper (J8) selects between the programming modes as shown in the J8 Mode legend in the figure below. JTAG Mode can be accessed at any time without changing jumpers.



Programming files are stored in SRAM-based memory cells within the FPGA. This data defines the FPGA's logic functions and circuit connections, and it remains valid until it is erased by removing board power, by pressing the reset button attached to the PROG input, or by writing a new configuration file using the JTAG port.

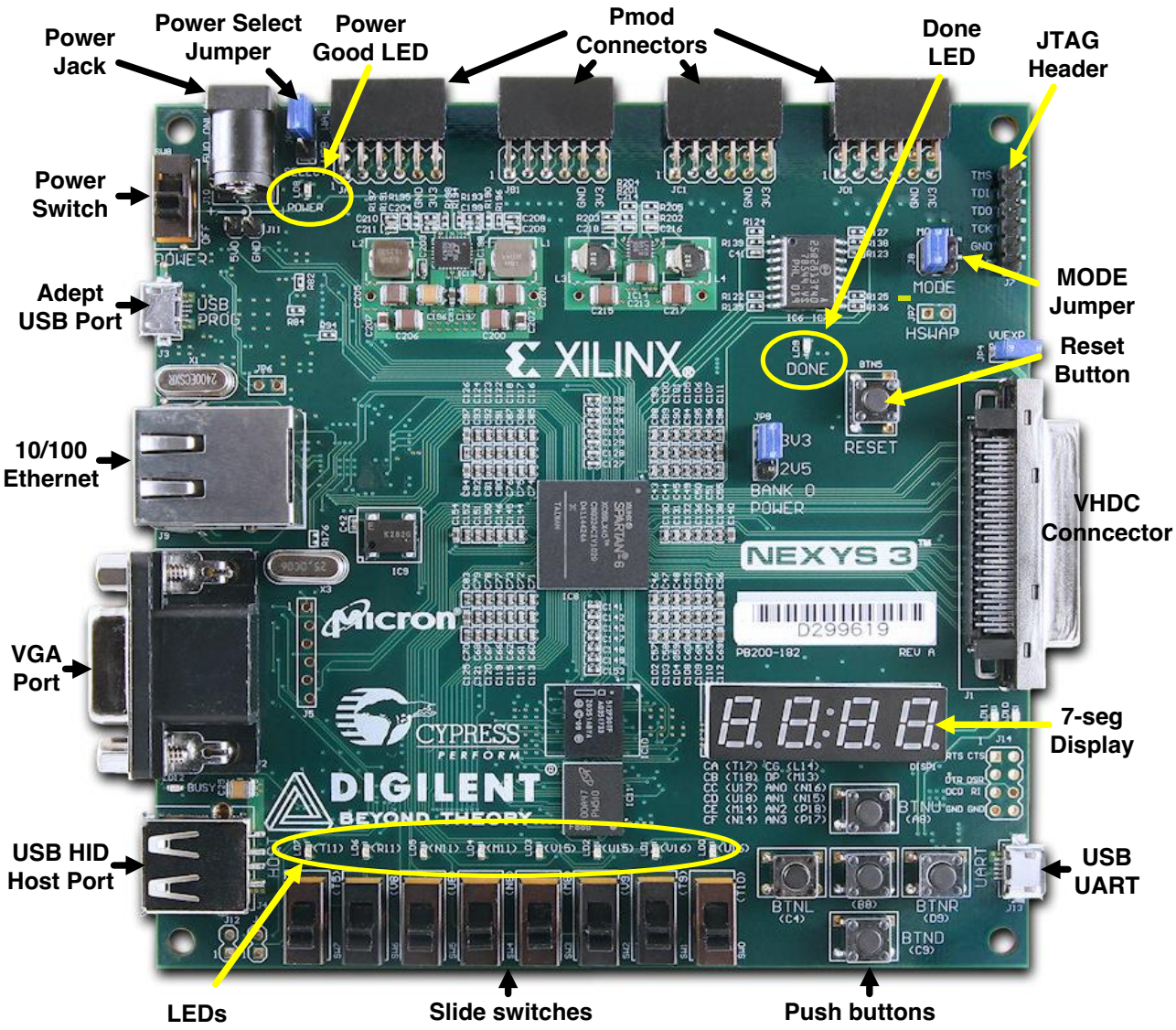
FPGA configuration files transferred via the JTAG port use the .bin or .svf file types, files transferred from a USB stick use the .bit file type, and BPI or SPI programming files can use .bit, .bin, or .mcs types. The ISE/WebPack or EDK software from Xilinx can create bit, svf, bin, or mcs files from VHDL, Verilog, or schematic-based source files

Copyright Digilent, Inc. All rights reserved.
Other product and company names mentioned may be trademarks of their respective owners.

(EDK is used for MicroBlaze™ embedded processor-based designs). Digilent's Adept software or Xilinx's iMPACT software can be used to program the FPGA or ROMs using the Adept USB port.

During JTAG programming, a .bit or .svf file is transferred from the PC to the FPGA using the Adept USB port. When programming a non-volatile PCM device, a .bit, .bin, or .mcs file is transferred to the in a two-step process. First, the FPGA is programmed with a circuit that can program PCM devices, and then data is transferred to the PCM device via the FPGA circuit (this complexity is hidden from the user – a simple "program ROM" interface is presented by the programming software. Note the PCM devices are next-generation Flash ROM devices, and they are often referred to as "Flash" or "ROM" memory). After the PCM device has been programmed, it can automatically configure the FPGA at a subsequent power-on or reset event as determined by the J8 jumper setting. Programming files stored in the PCM devices will remain until they are overwritten, regardless of power-cycle events.
The FPGA can be programmed from a memory stick attached to the USB-HID port if the stick contains a single .bit configuration file in the root directory, the J8 Programming Mode jumper is set to JTAG (both jumpers loaded), and board power is cycled. The FPGA will automatically reject any .bit files that are not built for the proper FPGA.

After being successfully programmed, the FPGA will cause the "Done" LED to illuminate. Pressing the Reset button at any time will reset the configuration memory in the FPGA. After being reset, the FPGA will immediately attempt to reprogram itself from one of the PCM devices if the J8 Mode jumper is set to BPI or SPI mode.



Copyright Digilent, Inc. All rights reserved.
Other product and company names mentioned may be trademarks of their respective owners.

Digilent's Adept software offers a simplified programming interface and many additional features as described below. The Adept USB port is fully compatible with all Xilinx tools, including the iMPACT programming software. The Adept features are always available, regardless of how the FPGA was programmed.

1.1 Adept System

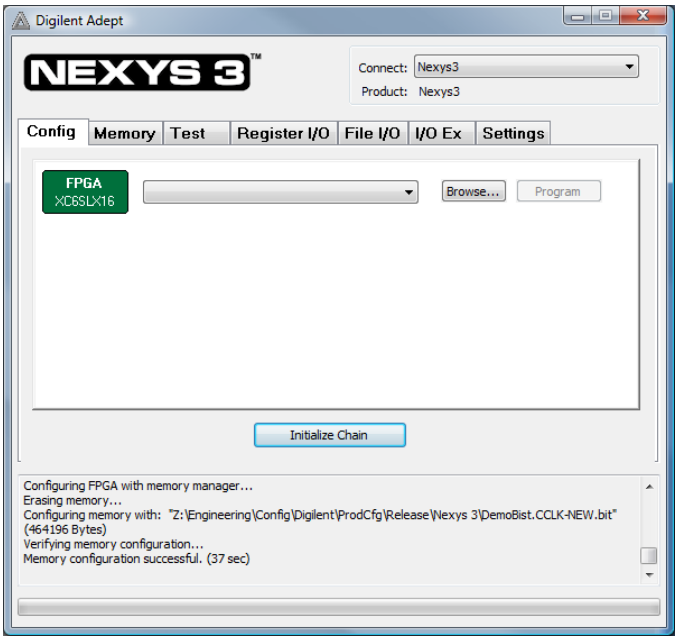
Digilent's Adept high-speed USB2 system can be used to program the FPGA and PCM devices, run automated board tests, add PC-based virtual I/O devices (like buttons, switches, and LEDs) to FPGA designs, and exchange register-based and file-based data with the FPGA. Adept automatically recognizes the Nexys 3 board and presents a graphical interface with tabs for each of these applications. Adept also includes public APIs/DLLs so that users can write applications to exchange data with the Nexys 3 board at up to 38Mbytes/sec. The Adept application, an SDK, and reference materials are freely downloadable from the Digilent website.

1.2 Programming Interface

To program the Nexys 3 board using Adept, first set up the board and initialize the software:

- plug in and attach the power supply
- plug in the USB cable to the PC and to the USB port on the board
- start the Adept software
- turn ON Nexys 3's power switch
- wait for the FPGA to be recognized.

Use the browse function to associate the desired .bit file with the FPGA, and click on the Program button. The configuration file will be sent to the FPGA, and a dialog box will indicate whether programming was successful. The configuration "done" LED will light after the FPGA has been successfully configured.



Before starting the programming sequence, Adept ensures that any selected configuration file contains the correct FPGA ID code – this prevents incorrect .bit files from being sent to the FPGA.

In addition to the navigation bar and browse and program buttons, the Config interface provides an Initialize Chain button, console window, and status bar. The Initialize Chain button is useful if USB communications with the board have been interrupted. The console window displays current status, and the status bar shows real-time progress when downloading a configuration file.

1.3 Memory Interface

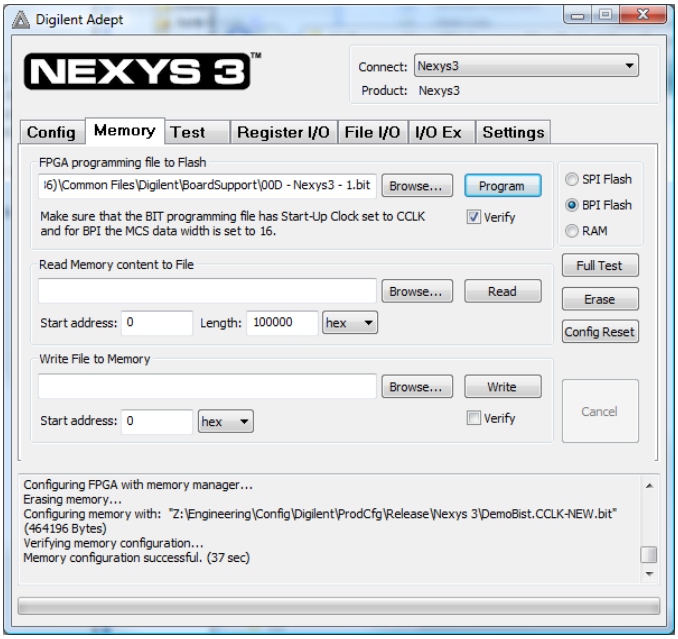
The Memory tab allows .bin, .bit, and .mcs configuration files to be transferred to the on-board BPI (parallel) or SPI (serial) PCM devices for subsequent FPGA programming, and allows user data files to be transferred to/from the PCM devices or RAM memories at user-specified addresses. The target memory is selected by clicking one of the three radio buttons in the upper-right corner.

Copyright Digilent, Inc. All rights reserved.
Other product and company names mentioned may be trademarks of their respective owners.

The configuration tool supports programming from any valid ROM file produced by the Xilinx tools. After programming, board power can either be cycled or the Reset button can be pressed to program the FPGA from the PCM device selected by the J8 mode jumper. If programming with a .bit file, the startup clock must be set to CCLK.

All three memory devices (the PCM's and the cellular RAM) can be fully tested by clicking the Full Test button. They can also be completely erased by clicking the Erase button.

The Read/Write tools allow data to be exchanged between files on the host PC and specified address ranges in the memory devices.

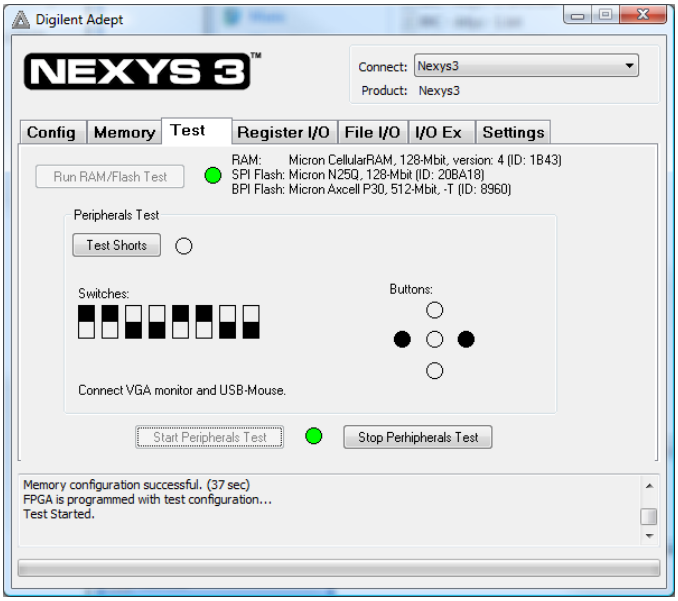


1.4 Test Interface

The test interface provides an easy way to verify many of the board's hardware circuits and interfaces. These are divided into two major categories: on-board memory (RAM and Flash) and peripherals. In both cases, the FPGA is configured with test and PC-communication circuits, overwriting any FPGA configuration that may have been present.

Clicking the Run RAM/Flash Test button will identify the CellularRam, SPI Flash, and BPI Flash memory by reading out and verifying the IDCODE on each memory. The memory contents will not be modified. To run a full test on a particular memory device, refer to the Full Test in the Memory Tab.

Clicking the Start Peripherals Test button will initialize GPIO and user I/O testing. Once the indicator near the Start Peripherals Test button turns green, all peripheral tests can be run.



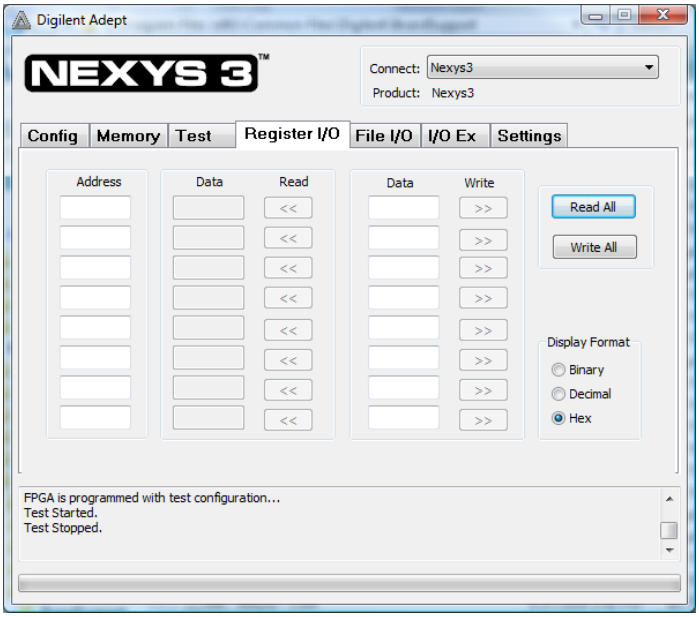
The Test Shorts feature checks all discrete I/O's for shorts to Vdd, GND, and neighboring I/O pins. The switches and buttons graphics show the current states of those devices on the Nexys 3 board. Connect a VGA monitor and USB mouse to visually test the J2 VGA port and J4 USB port respectively.

Copyright Digilent, Inc. All rights reserved.
Other product and company names mentioned may be trademarks of their respective owners.

1.5 Register I/O

The register I/O tab requires that a corresponding IP block, available in the Parallel Interface reference design (DpimRef.vhd) on the Adept page of the Digilent website, is included and active in the FPGA. This IP block provides an EPP-style interface, where an 8-bit address selects a register, and data read and write buttons transfer data to and from the selected address. Addresses entered into the address field must match the physical address included in the FPGA IP block.

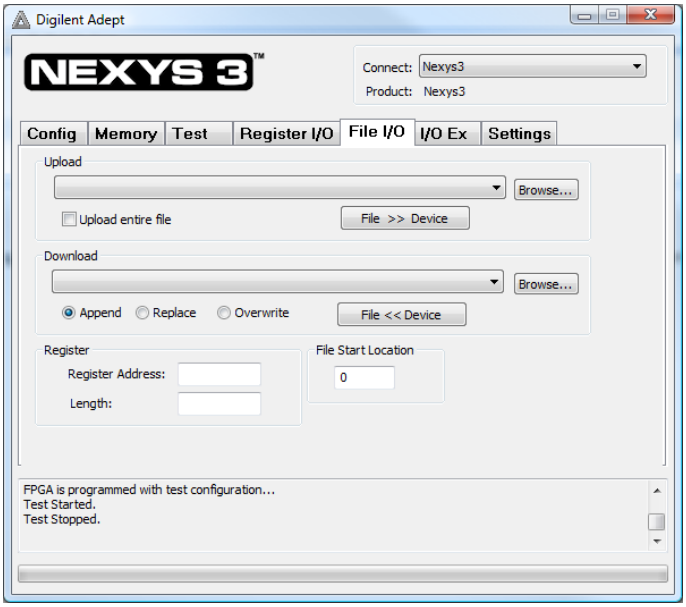
Register I/O provides an easy way to move small amounts of data into and out of specific registers in a given design. This feature greatly simplifies passing control parameters into a design, or reading low-frequency status information out of a design.



1.6 File I/O

The File I/O tab can transfer files between the PC and the Nexys 3 FPGA. A number of bytes (specified by the Length value) can be streamed into a specified register address from a file or out of a specified register address into a file. During upload and download, the file start location can be specified in terms of bytes.

As with the Register I/O tab, File I/O also requires specific IP to be available in the FPGA. This IP can include a memory controller for writing files into the on-board Ram and Flash memories.



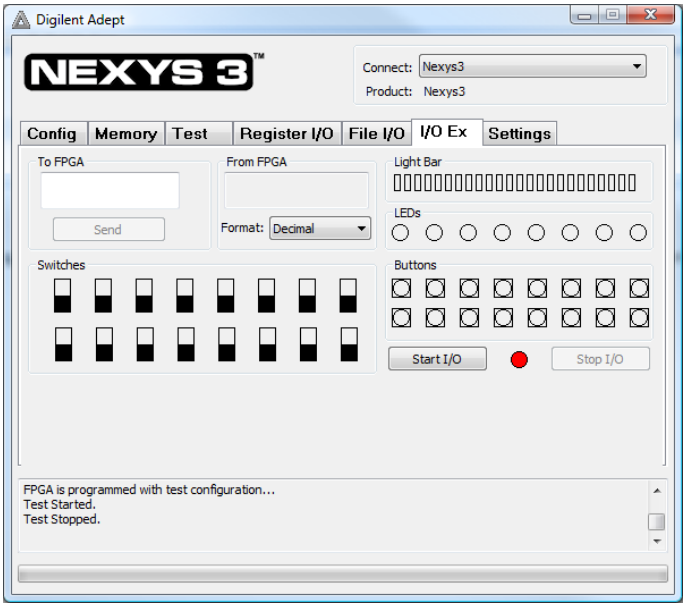
1.7 I/O Expand

The I/O Expand tab works with an IP block in the FPGA to provide additional simple I/O beyond the physical devices found on the Nexys 3 board. Virtual I/O devices include a 24-LED light bar, 16 slide switches, 16 push buttons, 8 discrete LEDs, a 32-bit register that can be sent to the FPGA, and a 32-bit register that can be read from the FPGA.

Copyright Digilent, Inc. All rights reserved.
Other product and company names mentioned may be trademarks of their respective owners.

The IP block, available in the Adept I/O Expansion reference design (AdeptIOExpansion.zip) on the Adept page of the Digilent website, provides a simple interface with well-defined signals. This IP block can easily be included in, and accessed from, user-defined circuits.

For more information, see the Adept documentation available at the Digilent website.



2 Power Supplies

The Nexys 3 board can receive power from the Adept USB port or from an external power supply. Jumper JP1 (near the power jack) determines which source is used.

The USB port can deliver enough power for the vast majority of designs. It is possible that a very demanding application, including an application that drives many peripheral boards, might require more power than can be delivered by the USB port. Some applications may also need to run without being connected to a PC's USB port. In either case, an external power supply or battery pack can be used by setting JP1 to "Wall".

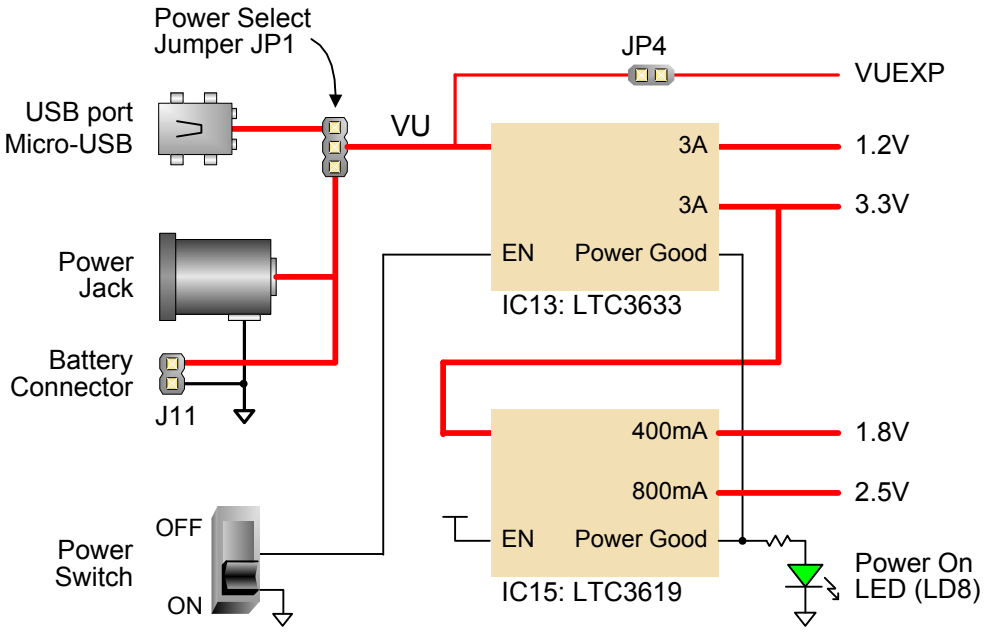
The main regulator on the Nexys 3 can accommodate input voltages up to 5.5VDC. An external DC wall-plug supply should provide at least five watts of input power, and use a coax center-positive 2.1mm internal-diameter plug. An external battery pack can also be used by connecting the battery's terminal leads to connector J11 (J11 is in parallel with the wall-plug power jack, so if a battery pack is connected, a wall plug should not be). An external battery pack should also be limited to 5.5VDC, and should be capable of delivering adequate power for the application.

Voltage regulator circuits from Linear Technology create the required 3.3V, 2.5V, 1.8V, and 1.2V supplies from the main power input. The table below provides additional information (typical currents depend strongly on FPGA configuration and the values provided are typical of medium size/speed designs).

Supply	Circuits	Device	Amps (max/typ)
3.3V	FPGA I/O, USB ports, Clocks, ROM & RAM I/O, Ethernet	IC13: LTC3633	3A / 200mA
2.5V	Optional voltage for Bank0 and VHDC connector	IC14: LTC3619	800mA / 0mA
1.2V	FPGA Core	IC13: LTC3633	3A / 0.2 to 1.0A
1.8V	RAM and ROM core	IC14: LTC3619	400mA / 0.1 to 0.3A

Table 1. Nexys 3 Power Supplies.

Copyright Digilent, Inc. All rights reserved.
Other product and company names mentioned may be trademarks of their respective owners.



The Nexys 3 power supplies are enabled (or turned on) by a logic-level Power switch (SW8). A power-good LED (LD8), driven by the wired-OR of the "power good" outputs on the supplies, indicates that all supplies are operating within 10% of nominal.

The VU output of the main power jumper (JP1) is available to the VHDC expansion connector if jumper JP4 is loaded. Care must be taken to ensure the VUEXP delivered to any attached expansion board is the correct voltage – since VU is driven directly from an attached supply, this means a supply of the proper voltage must be used (e.g., 5V).

3 Memory

The Nexys 3 board contains three external memories, all from Micron: a 128Mbit Cellular RAM (pseudo-static DRAM); a 128Mbit parallel non-volatile PCM (phase-change memory); and a 128Mbit serial PCM device. The Cellular RAM and parallel PCM device share a common bus, and the serial PCM is on a dedicated quad-mode (x4) SPI bus. The non-volatile PCM memories are byte and bit alterable without requiring a block erase, so they are faster and more versatile than conventional Flash in most applications.

The 16Mbyte Cellular RAM (Micron part number M45W8MW16) has a 16-bit bus that supports 8 or 16 bit data access. It can operate as a typical asynchronous SRAM with read and write cycle times of 70ns, or as a synchronous memory with an 80MHz bus. When operated as an asynchronous SRAM, the Cellular RAM automatically refreshes its internal DRAM arrays, allowing for a simplified memory controller (similar to any SRAM controller). When operated in synchronous mode, continuous transfers of up to 80MHz are possible.

The parallel PCM device (Micron part number NP8P128A13T1760E) is organized as 8Mwords of 16bits each. It contains 128 individually erasable 64K-blocks, one of which is subdivided into four 16K "parameter blocks" that can offer increased data protection. Normally, a device with a parameter block at the high end of the address space is loaded (a "top parameter" block device). The parallel PCM memory offers 115ns read cycle times, with 25ns page-mode reads within blocks. It has an internal 64-byte write buffer that can be written with 50ns cycle times, and the 64-byte buffer can be transferred to the Flash array in 120us (typical). The parallel PCM device also contains an SPI

Copyright Digilent, Inc. All rights reserved.
Other product and company names mentioned may be trademarks of their respective owners.

port for serial data transfer, but that function is not enabled on the Nexys 3 board (the ADV and WAIT signals are connected between the FPGA and PCM, but they serve no functions).

The Cellular RAM and parallel PCM share a common 16-bit data bus and 24-bit address bus. The Cellular RAM is byte addressable using the upper-byte and lower-byte signals (MT-UB and MT-LB), but the P8P PCM is configured for 16 byte operations only (it is not byte addressable). The output enable (OE) and write enable (WE) signals are shared by both devices, but each device has individual chip enable (CE) signals. Additionally, the Cellular RAM has clock (MT-CLK), wait (MT-WAIT), address valid (MT-ADV) and control register enable (MT_CRE) signals available to the FPGA for use with synchronous transfers, and the PCM device has Reset (RP#). With simple changes, the Nexys 3 board can accommodate either the PCM device or the older "P33" Flash device. The signal names in the Nexys 3 schematic reference the P33 device; the P33 ADV and WAIT signals are not used in by the PCM device.

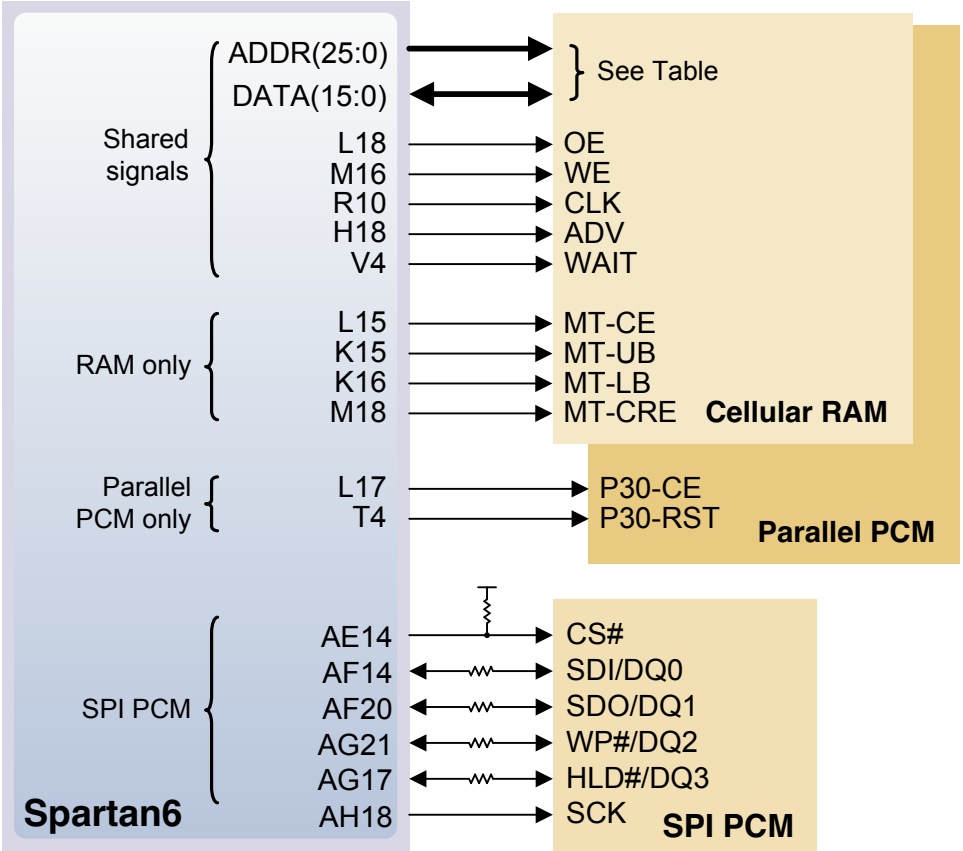
The 16Mbyte serial PCM device (Micron part number NP5Q128A13ESFC0E) is also bit alterable without requiring an erase cycle. It supports the legacy SPI protocol as well as the newer Quad I/O and Dual I/O protocols, at bus speeds up to 50MHz.

FPGA configuration files can be written to both PCM devices, and mode settings are available to cause the FPGA to automatically read a configuration from one of these devices at power on. A Spartan-6 LX16 configuration file requires about 512Kbytes of memory, leaving about 97% of the PCM devices available for user data.

Both PCM devices are loaded with configuration files at the factory. The SPI PCM device contains a file that configures the FPGA to test the Nexys 3 memory devices during manufacturing, and this file isn't needed after the board test is complete. The BPI PCM device contains a file that configures the Nexys 3 with a basic user demonstration program, and it can be used to verify board functions. This same .bit file is available for download from the Digilent website. If Mode jumper J8 is set to BPI mode and power is applied, the user demo configuration will be loaded. The demo drives a counter on the 7-segment display, drives the user LEDs on and off when the user switches are toggled, turns off digits on the 7-segment display when user buttons are pressed, and drives an image out the VGA port. A USB mouse can be connected to J4 for a simple visual demonstration.

Please refer to the manufacturer's data sheets and the reference designs posted on Digilent's website for more information about the memory devices.

Copyright Digilent, Inc. All rights reserved.
Other product and company names mentioned may be trademarks of their respective owners.



Address Bus			Data Bus	
ADDR25: F15	ADDR16: G13	ADDR7: H15	DATA15: T8	DATA6: T3
ADDR24: F16	ADDR15: E16	ADDR6: H16	DATA14: R8	DATA5: R3
ADDR23: C17	ADDR14: E18	ADDR5: G16	DATA13: U10	DATA4: V5
ADDR22: C18	ADDR13: K12	ADDR4: G18	DATA12: V13	DATA3: U5
ADDR21: F14	ADDR12: K13	ADDR3: J16	DATA11: U13	DATA2: V14
ADDR20: G14	ADDR11: F17	ADDR2: J18	DATA10: P12	DATA1: T14
ADDR19: D17	ADDR10: F18	ADDR1: K17	DATA9: P6	DATA0: R13
ADDR18: D18	ADDR9: H13	ADDR0: K18	DATA8: N5	
ADDR17: H12	ADDR8: H14		DATA7: R5	

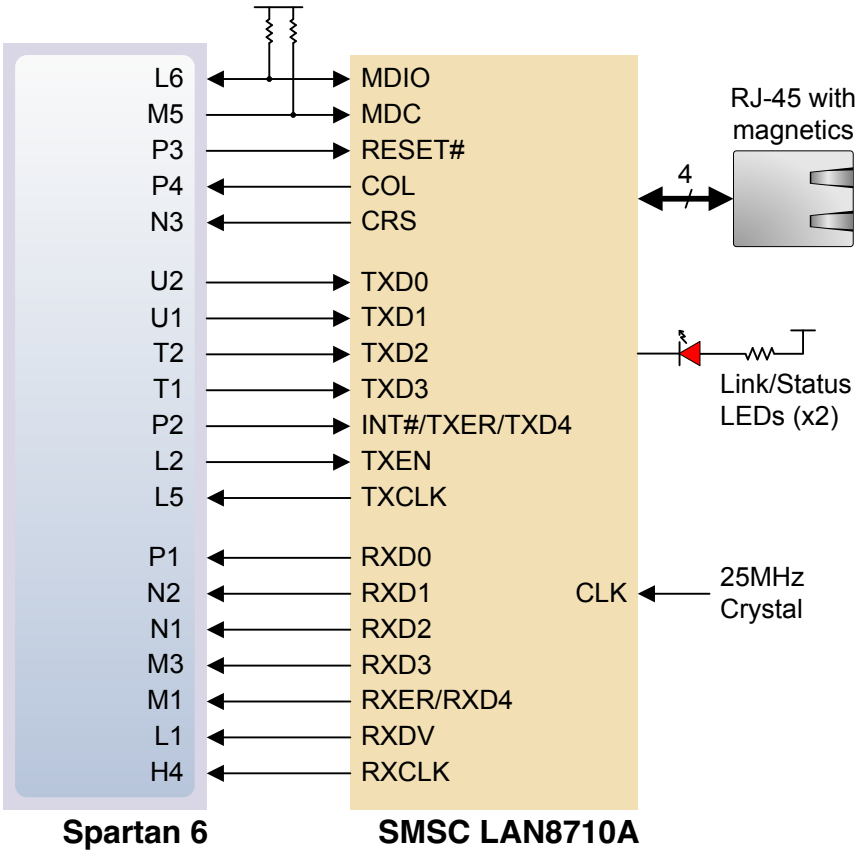
4 Ethernet PHY

The Nexys 3 board includes an SMSC 10/100 Ethernet PHY (SMSC part number LAN8710) paired with an RJ-45 Ethernet jack with integrated magnetics. EDK-based designs can access the PHY using either the xps_ethernetlite IP core or the xps_ll_temac IP core. The Nexys 3 Base System Builder (BSB) support package automatically generates a test application for the Ethernet MAC; this can be used as a reference for creating custom designs. ISE designs can use the IP Core Generator wizard to create an Ethernet MAC controller IP core. The SMSC PHY uses the MII interface and supports 10/100 Mb/s. At power-on reset, the PHY is set to the following defaults:

- MII mode interface
- 100Base-TX with auto negotiation enabled, advertising half-duplex, with CRS active during receive
- PHY address = 000

Copyright Digilent, Inc. All rights reserved.
Other product and company names mentioned may be trademarks of their respective owners.

Refer to the LAN8710A data sheet on the www.smsc.com website for further information.



5 Oscillators/Clocks

The Nexys 3 board includes a single 100MHz CMOS oscillator connected to pin V10 (V10 is the GCLK0 input in bank 2). The input clock can drive any or all of the four clock management tiles in the Spartan-6. Each tile includes two Digital Clock Managers (DCMs) and four Phase-Locked Loops (PLLs).

DCMs provide the four phases of the input frequency (0º, 90º, 180º, and 270º), a divided clock that can be the input clock divided by any integer from 2 to 16 or 1.5, 2.5, 3.5... 7.5, and two antiphase clock outputs that can be multiplied by any integer from 2 to 32 and simultaneously divided by any integer from 1 to 32.

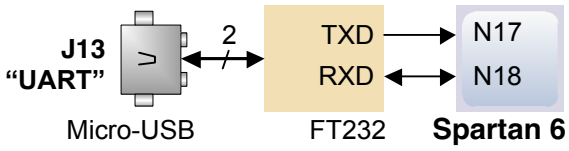
PLLs use VCOs that can be programmed to generate frequencies in the 400MHz to 1080MHz range by setting three sets of programmable dividers during FPAG configuration. VCO outputs have eight equally-spaced outputs (0º, 45º, 90º, 135º, 180º, 225º, 270º, and 315º) that can be divided by any integer between 1 and 128.

Please refer to the Spartan-6 data sheet at www.xilinx.com for further information on the clock management tiles.

Copyright Digilent, Inc. All rights reserved.
Other product and company names mentioned may be trademarks of their respective owners.

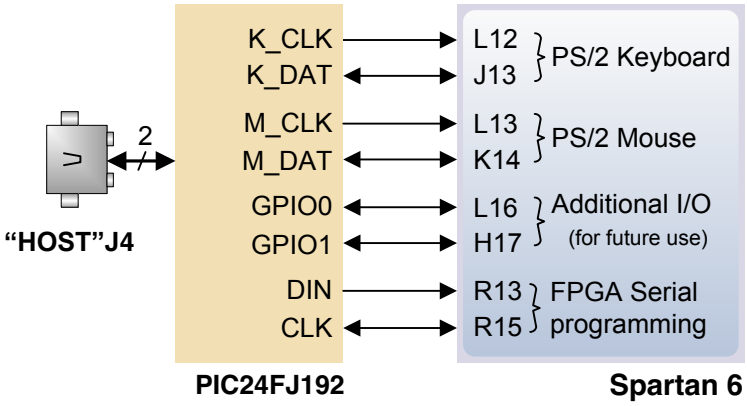
6 USB-UART Bridge (Serial Port)

The Nexys 3 includes an FTDI FT232 USB-UART bridge to allow PC applications to communicate with the board using standard Windows COM port commands. Free USB-COM port drivers, available from www.ftdichip.com under the "Virtual Com Port" or VCP heading, convert USB packets to UART/serial port data. Serial port data is exchanged with the FPGA using a two-wire serial port (TXD/RXD) and software flow control (XON/XOFF). After the drivers are installed, I/O commands from the PC directed to the COM port will produce serial data traffic on the N17 and N18 FPGA pins.



7 USB HID Host

A Microchip PIC24FJ192 microcontroller provides the Nexys 3 with USB H ID host capability. Firmware in the microcontroller can drive a mouse or a keyboard attached to the type A USB connector at J4 labeled "Host". Hub support is not currently available, so only a single mouse or a single keyboard can be used. The PIC24 drives four signals into the FPGA – two are used as a keyboard port following the keyboard PS/2 protocol, and two are used as a mouse port following the mouse PS/2 protocol.

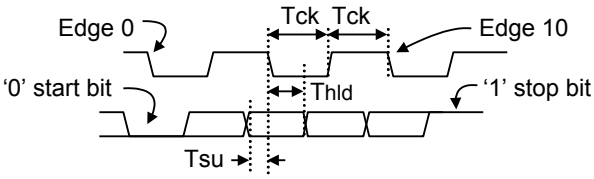


Two PIC24 I/O pins are also connected to the FPGA's two-wire serial programming port, so the FPGA can be programmed from a file stored on a USB memory stick. To program the FPGA, attach a memory stick containing a single .bit programming file in the root directory, load both M0 and M1 on J8 jumper, and cycle board power. This will cause the PIC processor to program the FPGA, and any incorrect bit files will automatically be rejected. Note the PIC24 reads the FPGA's mode, init, and done pins, and can drive the PROG pin as a part of the programming sequence.

7.1 HID Controller

To access the USB host controller, EDK designs can use the standard PS/2 core (non-EDK designs can use a simple state machine).

Mice and keyboards that use the PS/2 protocol[1] use a two-wire serial bus (clock and data) to communicate with a host device. Both use 11-bit words that include a start, stop, and



Symbol	Parameter	Min	Max
T_{CK}	Clock time	30us	50us
T_{SU}	Data-to-clock setup time	5us	25us
T_{HLD}	Clock-to-data hold time	5us	25us

[1]Not all keyboard manufacturers strictly adhere to the PS/2 specifications; some keyboards may not produce the proper signaling voltages or use the standard communication protocols. Compatibility with the USB host may vary between different keyboards.

Copyright Digilent, Inc. All rights reserved.
Other product and company names mentioned may be trademarks of their respective owners.

odd parity bit, but the data packets are organized differently, and the keyboard interface allows bi-directional data transfers (so the host device can illuminate state LEDs on the keyboard). Bus timings are shown in the figure. The clock and data signals are only driven when data transfers occur, and otherwise they are held in the idle state at logic '1'. The timings define signal requirements for mouse-to-host communications and bi-directional keyboard communications. A PS/2 interface circuit can be implemented in the FPGA to create a keyboard or mouse interface.

7.2 Keyboard

The keyboard uses open-collector drivers so the keyboard, or an attached host device, can drive the two-wire bus (if the host device will not send data to the keyboard, then the host can use input-only ports).

PS/2-style keyboards use scan codes to communicate key press data. Each key is assigned a code that is sent whenever the key is pressed. If the key is held down, the scan code will be sent repeatedly about once every 100ms. When a key is released, an F0 key-up code is sent, followed by the scan code of the released key. If a key can be shifted to produce a new character (like a capital letter), then a shift character is sent in addition to the scan code, and the host must determine which ASCII character to use. Some keys, called extended keys, send an E0 ahead of the scan code (and they may send more than one scan code). When an extended key is released, an E0 F0 key-up code is sent, followed by the scan code. Scan codes for most keys are shown in the figure. A host device can also send data to the keyboard. Below is a short list of some common commands a host might send.

ED Set Num Lock, Caps Lock, and Scroll Lock LEDs. Keyboard returns FA after receiving ED, then host sends a byte to set LED status: bit 0 sets Scroll Lock, bit 1 sets Num Lock, and bit 2 sets Caps lock. Bits 3 to 7 are ignored.

EE Echo (test). Keyboard returns EE after receiving EE.

F3 Set scan code repeat rate. Keyboard returns F3 on receiving FA, then host sends second byte to set the repeat rate.

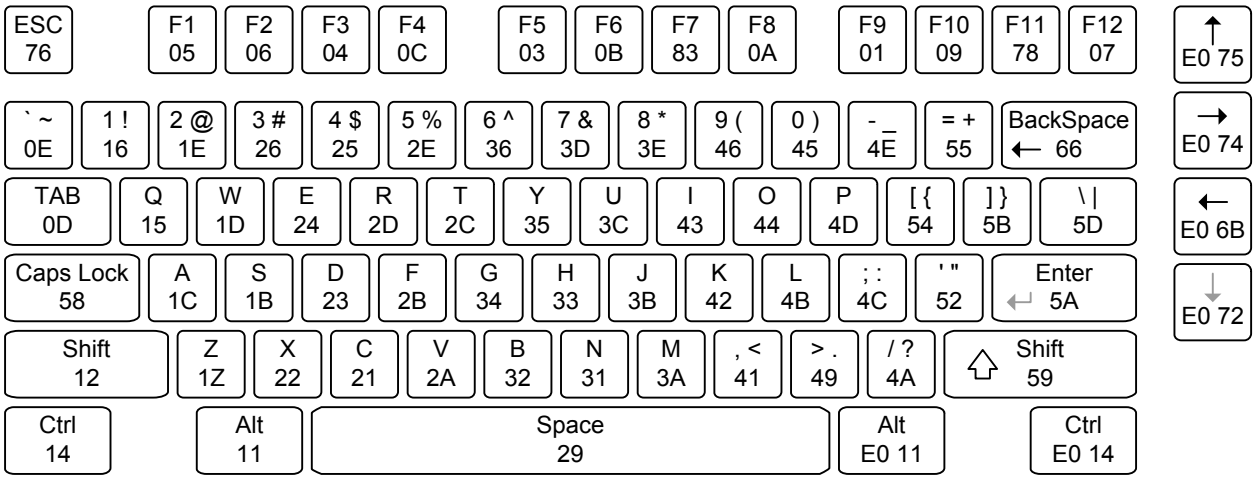
FE Resend. FE directs keyboard to re-send most recent scan code.

FF Reset. Resets the keyboard.

The keyboard can send data to the host only when both the data and clock lines are high (or idle). Since the host is the bus master, the keyboard must check to see whether the host is sending data before driving the bus. To facilitate this, the clock line is used as a "clear to send" signal. If the host pulls the clock line low, the keyboard must not send any data until the clock is released. The keyboard sends data to the host in 11-bit words that contain a '0' start bit, followed by 8-bits of scan code (LSB first), followed by an odd parity bit and terminated with a '1' stop bit. The keyboard generates 11 clock transitions (at 20 to 30KHz) when the data is sent, and data is valid on the falling edge of the clock.

Scan codes for most PS/2 keys are shown in the figure below.

Copyright Digilent, Inc. All rights reserved.
Other product and company names mentioned may be trademarks of their respective owners.

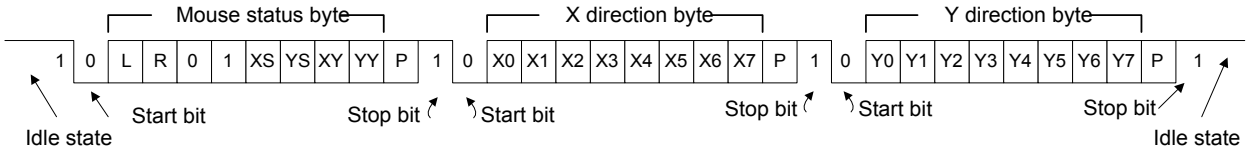


PS/2 keyboard scan codes.

7.3 Mouse

The mouse outputs a clock and data signal when it is moved, otherwise, these signals remain at logic '1'. Each time the mouse is moved, three 11-bit words are sent from the mouse to the host device. Each of the 11-bit words contains a '0' start bit, followed by 8 bits of data (LSB first), followed by an odd parity bit, and terminated with a '1' stop bit. Thus, each data transmission contains 33 bits, where bits 0, 11, and 22 are '0' start bits, and bits 11, 21, and 33 are '1' stop bits. The three 8-bit data fields contain movement data as shown in the figure above. Data is valid at the falling edge of the clock, and the clock period is 20 to 30KHz.

The mouse assumes a relative coordinate system wherein moving the mouse to the right generates a positive number in the X field, and moving to the left generates a negative number. Likewise, moving the mouse up generates a positive number in the Y field, and moving down represents a negative number (the XS and YS bits in the status byte are the sign bits – a '1' indicates a negative number). The magnitude of the X and Y numbers represent the rate of mouse movement – the larger the number, the faster the mouse is moving (the XV and YV bits in the status byte are movement overflow indicators – a '1' means overflow has occurred). If the mouse moves continuously, the 33-bit transmissions are repeated every 50ms or so. The L and R fields in the status byte indicate Left and Right button presses (a '1' indicates the button is being pressed).



Mouse data format.

8 VGA Port

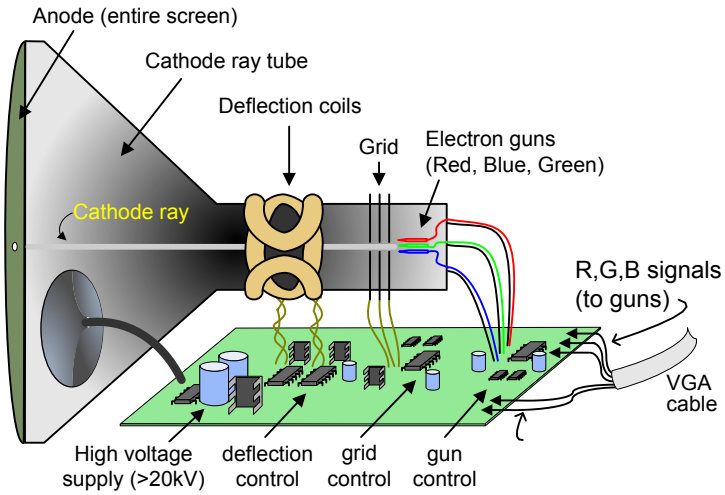
The Nexys 3 board uses 10 FPGA signals to create a VGA port with 8-bit color and the two standard sync signals (HS – Horizontal Sync, and VS – Vertical Sync). The color signals use resistor-divider circuits that work in conjunction with the 75-ohm termination resistance of the VGA display to create eight signal levels on the red and green VGA signals, and four on blue (the human eye is less sensitive to blue levels). This circuit, shown in figure 13, produces

Copyright Digilent, Inc. All rights reserved.
Other product and company names mentioned may be trademarks of their respective owners.

video color signals that proceed in equal increments between 0V (fully off) and 0.7V (fully on). Using this circuit, 256 different colors can be displayed, one for each unique 8-bit pattern. A video controller circuit must be created in the FPGA to drive the sync and color signals with the correct timing in order to produce a working display system.

8.1 VGA System Timing

VGA signal timings are specified, published, copyrighted and sold by the VESA organization (www.vesa.org). The following VGA system timing information is provided as an example of how a VGA monitor might be driven in 640 by 480 mode. For more precise information, or for information on other VGA frequencies, refer to documentation available at the VESA website.

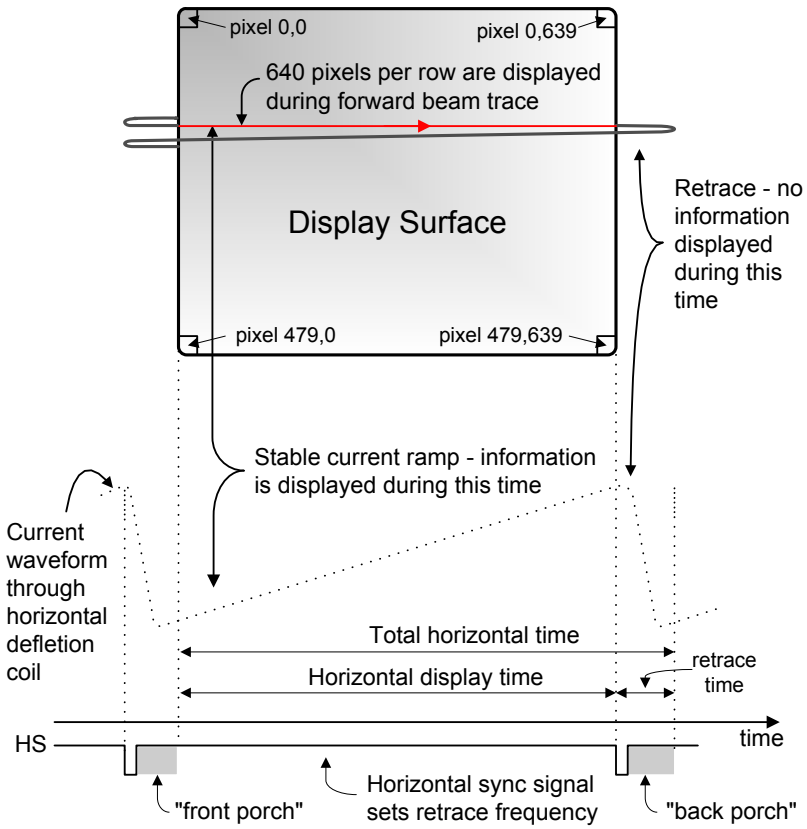


CRT-based VGA displays use amplitude-modulated moving electron beams (or cathode rays) to display information on a phosphor-coated screen. LCD displays use an array of switches that can impose a voltage across a small amount of liquid crystal, thereby changing light permittivity through the crystal on a pixel-by-pixel basis. Although the following description is limited to CRT displays, LCD displays have evolved to use the same signal timings as CRT displays (so the "signals" discussion below pertains to both CRTs and LCDs). Color CRT displays use three electron beams (one for red, one for blue, and one for green) to energize the phosphor that coats the inner side of the display end of a cathode ray tube (see illustration). Electron beams emanate from "electron guns" which are finely-pointed heated cathodes placed in close proximity to a positively charged annular plate called a "grid". The electrostatic force imposed by the grid pulls rays of energized electrons from the cathodes, and those rays are fed by the current that flows into the cathodes. These particle rays are initially accelerated towards the grid, but they soon fall under the influence of the much larger electrostatic force that results from the entire phosphor-coated display surface of the CRT being charged to 20kV (or more). The rays are focused to a fine beam as they pass through the center of the grids, and then they accelerate to impact on the phosphor-coated display surface. The phosphor surface glows brightly at the impact point, and it continues to glow for several hundred microseconds after the beam is removed. The larger the current fed into the cathode, the brighter the phosphor will glow.

Between the grid and the display surface, the beam passes through the neck of the CRT where two coils of wire produce orthogonal electromagnetic fields. Because cathode rays are composed of charged particles (electrons), they can be deflected by these magnetic fields. Current waveforms are passed through the coils to produce magnetic fields that interact with the cathode rays and cause them to transverse the display surface in a "raster" pattern, horizontally from left to right and vertically from top to bottom. As the cathode ray moves over the surface of the display, the current sent to the electron guns can be increased or decreased to change the brightness of the display at the cathode ray impact point.

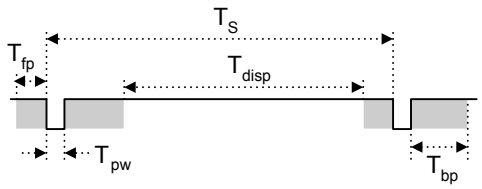
Copyright Digilent, Inc. All rights reserved.
Other product and company names mentioned may be trademarks of their respective owners.

Information is only displayed when the beam is moving in the "forward" direction (left to right and top to bottom), and not during the time the beam is reset back to the left or top edge of the display. Much of the potential display time is therefore lost in "blanking" periods when the beam is reset and stabilized to begin a new horizontal or vertical display pass. The size of the beams, the frequency at which the beam can be traced across the display, and the frequency at which the electron beam can be modulated determine the display resolution. Modern VGA displays can accommodate different resolutions, and a VGA controller circuit dictates the resolution by producing timing signals to control the raster patterns. The controller must produce synchronizing pulses at 3.3V (or 5V) to set the frequency at which current flows through the deflection coils, and it must ensure that video data is applied to the electron guns at the correct time. Raster video displays define a number of "rows" that corresponds to the number of horizontal passes the cathode makes over the display area, and a number of "columns" that corresponds to an area on each row that is assigned to one "picture element" or pixel. Typical displays use from 240 to 1200 rows and from 320 to 1600 columns. The overall size of a display and the number of rows and columns determines the size of each pixel.



Video data typically comes from a video refresh memory, with one or more bytes assigned to each pixel location (the Nexys 3 uses three bits per pixel). The controller must index into video memory as the beams move across the display, and retrieve and apply video data to the display at precisely the time the electron beam is moving across a given pixel.

A VGA controller circuit must generate the HS and VS timings signals and coordinate the delivery of video data based on the pixel clock. The pixel clock defines the time available to display one pixel of information. The VS signal defines the "refresh" frequency of the display, or the frequency at which all information on the display is redrawn. The minimum refresh frequency is a function of the display's phosphor and electron beam intensity, with practical refresh frequencies falling in the 50Hz to 120Hz range. The number of lines to be displayed at a given refresh frequency defines the horizontal "retrace" frequency. For a 640-pixel by 480-row display using a 25MHz pixel clock and 60 +/-1Hz refresh, the signal timings shown in the table at right

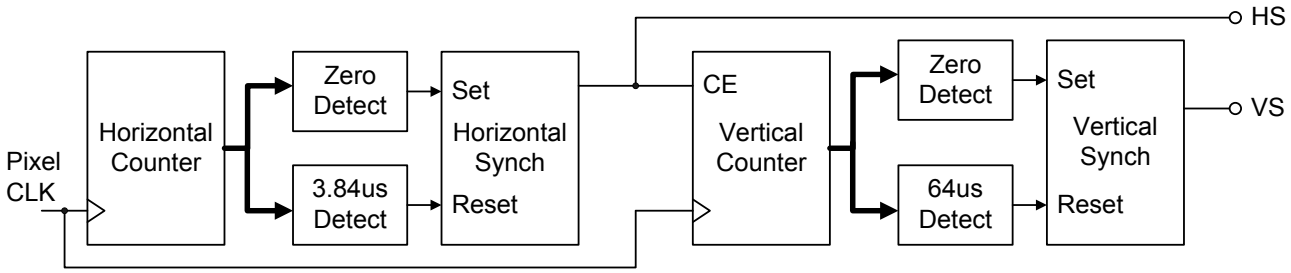


Symbol	Parameter	Vertical Sync			Horiz. Sync	
		Time	Clocks	Lines	Time	Clks
T_S	Sync pulse	16.7ms	416,800	521	32 us	800
T_{disp}	Display time	15.36ms	384,000	480	25.6 us	640
T_{pw}	Pulse width	64 us	1,600	2	3.84 us	96
T_{fp}	Front porch	320 us	8,000	10	640 ns	16
T_{bp}	Back porch	928 us	23,200	29	1.92 us	48

Copyright Digilent, Inc. All rights reserved.
Other product and company names mentioned may be trademarks of their respective owners.

can be derived. Timings for sync pulse width and front and back porch intervals (porch intervals are the pre- and post-sync pulse times during which information cannot be displayed) are based on observations taken from actual VGA displays.

A VGA controller circuit decodes the output of a horizontal-sync counter driven by the pixel clock to generate HS signal timings. This counter can be used to locate any pixel location on a given row. Likewise, the output of a vertical-sync counter that increments with each HS pulse can be used to generate VS signal timings, and this counter can be used to locate any given row. These two continually running counters can be used to form an address into video RAM. No time relationship between the onset of the HS pulse and the onset of the VS pulse is specified, so the designer can arrange the counters to easily form video RAM addresses, or to minimize decoding logic for sync pulse generation.

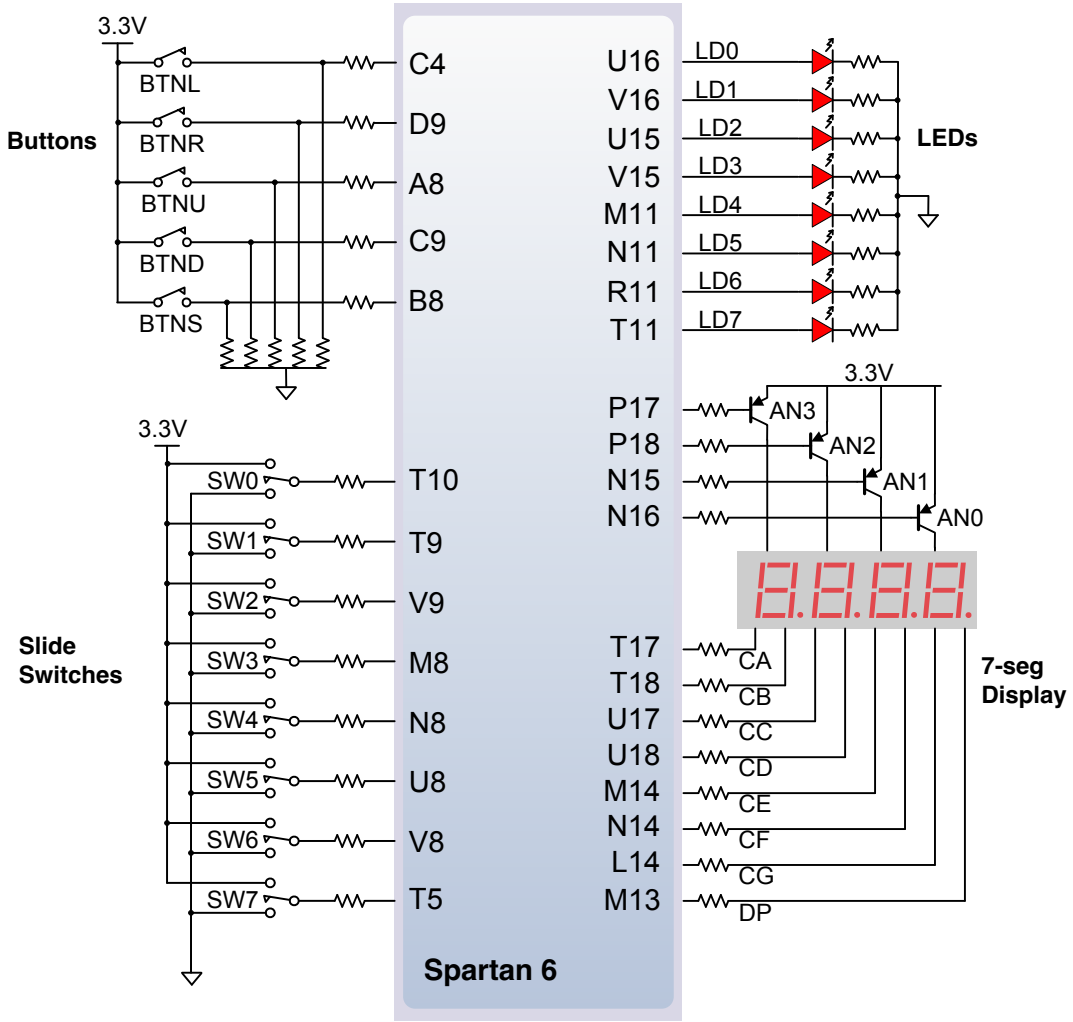


9 Basic I/O

The Nexys 3 board includes eight slide switches, five push buttons, eight individual LEDs, and a four digit seven-segment display. The pushbuttons and slide switches are connected to the FPGA via series resistors to prevent damage from inadvertent short circuits (a short circuit could occur if an FPGA pin assigned to a pushbutton or slide switch was inadvertently defined as an output). The pushbuttons are "momentary" switches that normally generate a low output when they are at rest, and a high output only when they are pressed. Slide switches generate constant high or low inputs depending on their position.

The eight individual high-efficiency LEDs are anode-connected to the FPGA via 390-ohm resistors, so they will turn on when a logic high voltage is applied to their respective I/O pin. Additional LEDs that are not user-accessible indicate power-on, FPGA programming status, and USB and Ethernet port status.

Copyright Digilent, Inc. All rights reserved.
Other product and company names mentioned may be trademarks of their respective owners.

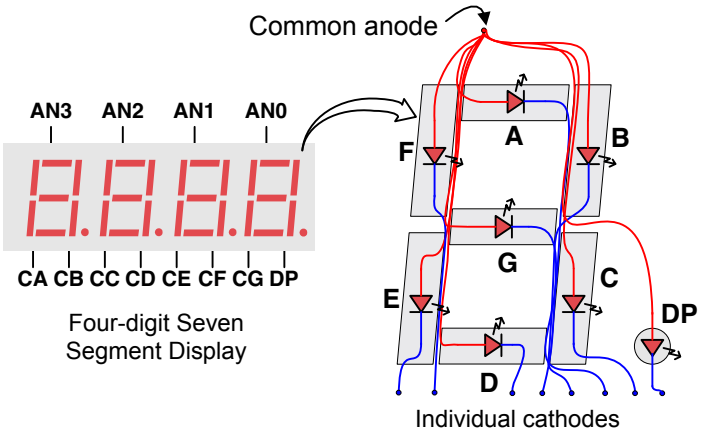


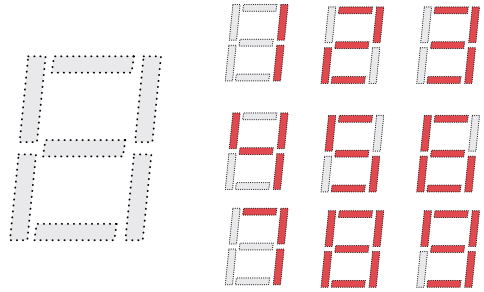
9.1 Seven-Segment Display

The Nexys 3 board contains a four-digit common anode seven-segment LED display. Each of the four digits is composed of seven segments arranged in a "figure 8" pattern, with an LED embedded in each segment. Segment LEDs can be individually illuminated, so any one of 128 patterns can be displayed on a digit by illuminating certain LED segments and leaving the others dark. Of these 128 possible patterns, the ten corresponding to the decimal digits are the most useful.

The anodes of the seven LEDs forming each digit are tied together into one "common anode" circuit node, but the LED cathodes remain separate. The common anode signals are available as four "digit enable" input signals to the 4-digit display. The cathodes of similar segments on all four displays are connected into seven circuit nodes labeled CA through CG (so, for example, the four "D" cathodes from the four digits are grouped together into a single circuit node called "CD"). These seven cathode signals are available as inputs to the 4-digit display. This signal connection scheme creates a multiplexed display, where the cathode signals are common to all digits but they can only illuminate the segments of the digit whose corresponding anode signal is asserted.

Copyright Digilent, Inc. All rights reserved.
Other product and company names mentioned may be trademarks of their respective owners.

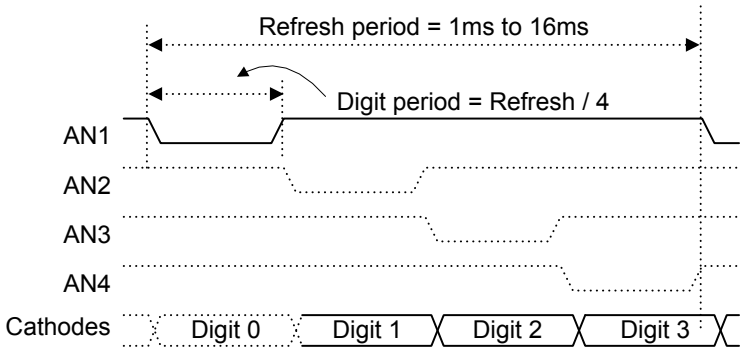




An un-illuminated seven-segment display, and nine illumination patterns corresponding to decimal digits

A scanning display controller circuit can be used to show a four-digit number on this display. This circuit drives the anode signals and corresponding cathode patterns of each digit in a repeating, continuous succession, at an update rate that is faster than the human eye can detect. Each digit is illuminated just one-quarter of the time, but because the eye cannot perceive the darkening of a digit before it is illuminated again, the digit appears continuously illuminated. If the update or "refresh" rate is slowed to around 45 hertz, most people will begin to see the display flicker.

In order for each of the four digits to appear bright and continuously illuminated, all four digits should be driven once every 1 to 16ms, for a refresh frequency of 1KHz to 60Hz. For example, in a 60Hz refresh scheme, the entire display would be refreshed once every 16ms, and each digit would be illuminated for ¼ of the refresh cycle, or 4ms. The controller must drive the cathodes with the correct pattern when the corresponding anode signal is driven. To illustrate the process, if AN0 is asserted while CB and CC are asserted, then a "1" will be displayed in digit position 1. Then, if AN1 is asserted while CA, CB and CC are asserted, then a "7" will be displayed in digit position 2. If AN0 and CB, CC are driven for 4ms, and then A1 and CA, CB, CC are driven for 4ms in an endless succession, the display will show "17" in the first two digits. An example timing diagram for a four-digit controller is provided.



10 Expansion Connectors

The Nexys 3 board has a 68-pin VHDC connector for high-speed/parallel I/O, and an 8-pin Pmod port for lower speed and lower pin-count I/O.

10.1 VHDC Connector

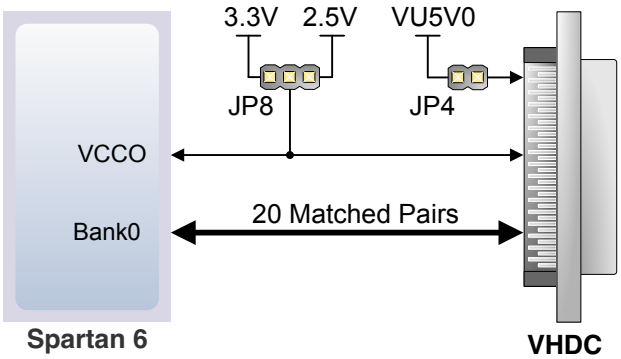
The VHDC connector includes 40 data signals (routed as 20 impedance-controlled matched pairs), 20 grounds (one per pair), and eight power signals. This connector, commonly used for SCSI-3 applications, can accommodate data rates of several hundred megahertz on every pin. Both board-to-board and board-to-cable mating connectors are available. Data sheets for the VHDC connector and for mating board and cable connectors can be found on the Digilent website, as well as on other vendor and distributor websites. Mating connectors and cables of various lengths are also available from Digilent and from distributors.

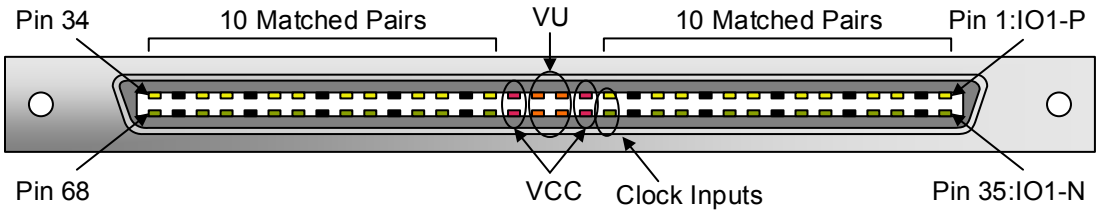
Copyright Digilent, Inc. All rights reserved.
Other product and company names mentioned may be trademarks of their respective owners.

All FPGA pins routed to the VHDC connector are located in FPGA I/O bank0. The FPGA's bank0 I/O power supply pins and the VHDC connector's four Vcc pins are connected together by a small, segregated power supply plane in the PCB. This sub-plane can be connected to 2.5V or 3.3V, depending on the position of jumper JP8. This arrangement allows peripheral boards and the FPGA to share the same Vcc and signaling voltage across the connector, whether it be 3.3V or 2.5V.

The unregulated board voltage VU5V0 (nominally 5V) is also routed to four other VHDC pins, supplying up to 1A of additional current to peripheral boards. A second jumper (JP4) allows the unregulated board voltage to be disconnected from the VHDC connector if desired.

All I/O's to the VHDC connector are routed as matched pairs to support LVDS signaling, commonly powered at 2.5V. The connector uses a symmetrical pinout (as reflected around the connector's vertical axis) so that peripheral boards as well as other system boards can be connected. Connector pins 15 and 49 are routed to FPGA clock input pins.





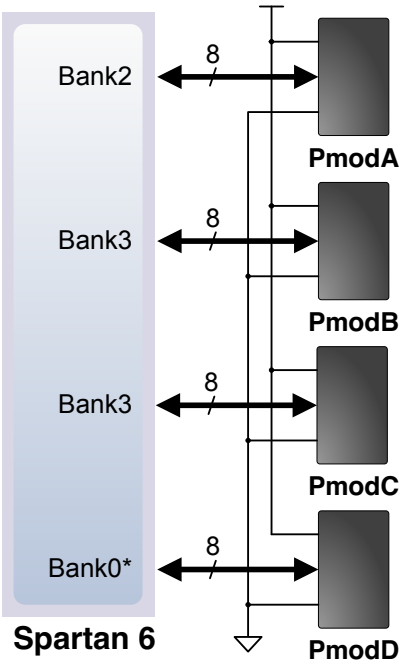
VHDC Connector Pinout			
IO1-P: B2	IO1-N: A2	IO11-P: C10	IO11-N: A10
IO2-P: D6	IO2-N: C6	IO12-P: G9	IO12-N: F9
IO3-P: B3	IO3-N: A3	IO13-P: B11	IO13-N: A11
IO4-P: B4	IO4-N: A4	IO14-P: B12	IO14-N: A12
IO5-P: C5	IO5-N: A5	IO15-P: C13	IO15-N: A13
IO6-P: B6	IO6-N: A6	IO16-P: B14	IO16-N: A14
IO7-P: C7	IO7-N: A7	IO17-P: F13	IO17-N: E13
IO8-P: D8	IO8-N: C8	IO18-P: C15	IO18-N: A15
IO9-P: B9	IO9-N: A9	IO19-P: D14	IO19-N: C14
IO10-P: D11	IO10-N: C11	IO20-P: B16	IO20-N: A16

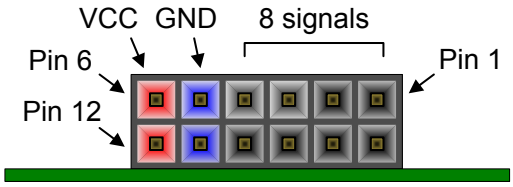
10.2 Pmod Ports

Pmod ports are 2x6 right-angle, 100-mil female connectors that mate with standard 2x6 pin headers available from a variety of catalog distributors. Each 12-pin Pmod port provides two 3.3V VCC signals (pins 6 and 12), two Ground signals (pins 5 and 11), and eight logic signals. VCC and Ground pins can deliver up to 1A of current. Pmod data

Copyright Digilent, Inc. All rights reserved.
Other product and company names mentioned may be trademarks of their respective owners.

signals are not matched pairs, and they are routed using best-available tracks without impedance control or delay matching.





Pmod Connectors – front view as loaded on PCB

Pmod Pinouts			
JA1: T12	JB1: K2	JC1: H3	JD1: G11
JA2: V12	JB2: K1	JC2: L7	JD2: F10
JA3: N10	JB3: L4	JC3: K6	JD3: F11
JA4: P11	JB4: L3	JC4: G3	JD4: E11
JA7: M10	JB7: J3	JC7: G1	JD7: D12
JA8: N9	JB8: J1	JC8: J7	JD8: C12
JA9: U11	JB9: K3	JC9: J6	JD9: F12
JA10: V11	JB10: K5	JC10: F2	JD10: E12

Digilent produces a large collection of Pmod accessory boards that can attach to the Pmod and VHDC expansion connectors to add ready-made functions like A/D's, D/A's, motor drivers, sensors, cameras and other functions. See www.digilentinc.com for more information.

11 Built-In Self Test

A demonstration configuration is loaded into the BPI PCM device on the Nexys 3 board during manufacturing. This demo bit file is available for download from the Digilent website. If the demo configuration is present in the BPI PCM device and the Nexys 3 board is powered on in BPI mode, a simple demo project will allow basic hardware verification. The demo drives a counter on the 7-segment display, drives the user LEDs on and off when the user switches are toggled, turns off digits on the 7-segment display when user buttons are pressed, and drives an image out the VGA port. A USB mouse can be connected to J4 for a simple visual demonstration.

If the demo configuration is not present in the BPI device, it can be downloaded from the Digilent website and programmed directly into the FPGA or reloaded into the PCM device using the Adept programming software. The same basic functionality is also available using the automated Test tab in the Adept application. Using the Test tab automatically loads a demo configuration into the FPGA, so no separate bit files or project need to be used.

All Nexys 3 boards are 100% tested during the manufacturing process. If any device on the Nexys 3 board fails test or is not responding properly, it is likely that damage occurred during transport or during use. Typical damage includes stressed solder joints and contaminants in switches and buttons resulting in intermittent failures. Stressed solder joints can be repaired by reheating and reflowing solder and contaminants can be cleaned with off-the-shelf electronics cleaning products. If a board fails test within the warranty period, it will be replaced at no cost. If a

Copyright Digilent, Inc. All rights reserved.
Other product and company names mentioned may be trademarks of their respective owners.

board fails test outside of the warranty period and cannot be easily repaired, Digilent can repair the board or offer a discounted replacement. Contact Digilent for more details.

Copyright Digilent, Inc. All rights reserved.
Other product and company names mentioned may be trademarks of their respective owners.

Appendix B – Digilent Nexys 3 Board Schematic

1300 Henley Court
Pullman, WA 99163
509.334.6306
www.digilentinc.com

Nexys 3™ FPGA Board Reference Manual

Revised April 11, 2016
This manual applies to the Nexys 3 rev. B

Overview

The Nexys 3 is a complete, ready-to-use digital circuit development platform based on the Xilinx Spartan-6 LX16 FPGA. The Spartan-6 is optimized for high performance logic, and offers more than 50% higher capacity, higher performance, and more resources as compared to the Nexys 2's Spartan-3 500E FPGA.

Features include:

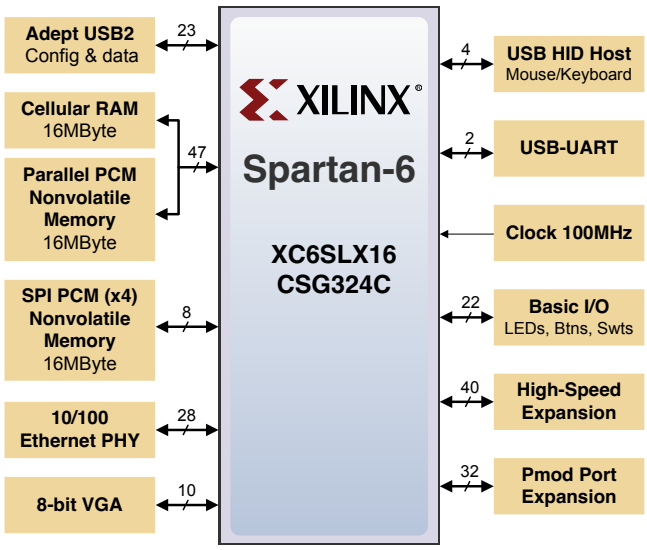
- Xilinx Spartan-6 LX16 FPGA in a 324-pin BGA package
- 16Mbyte Cellular RAM (x16)
- 16Mbytes SPI (quad mode) PCM non-volatile memory
- 16Mbytes parallel PCM non-volatile memory
- 10/100 Ethernet PHY
- On-board USB2 port for programming & data xfer
- USB-UART and USB-HID port (for mouse/keyboard)
- 8-bit VGA port
- 100MHz CMOS oscillator
- 72 I/Os routed to expansion connectors
- GPIO includes 8 LEDs, 5 buttons,8 slide switches and 4-digit seven-segment display
- USB2 programming cable included

In addition to the Spartan-6 FPGA, the Nexys 3 offers an improved collection of peripherals including 32Mbytes of Micron's latest Phase Change nonvolatile memory, a 10/100 Ethernet PHY, 16Mbytes of Cellular RAM, a USB-UART port, a USB host port for mice and keyboards, and an improved high-speed expansion connector. The large FPGA and broad set of peripherals make the Nexys 3 board an ideal host for a wide range of digital systems, including embedded processor designs based on Xilinx's MicroBlaze.

Nexys 3 is compatible with all Xilinx CAD tools, including ChipScope, EDK, and the free WebPack. The Nexys 3 uses Digilent's newest Adept USB2 system that offers FPGA and ROM programming, automated board tests, virtual I/O, and simplified user-data transfer facilities.

A comprehensive collection of board support IP and reference designs, and a large collection of add-on boards are available on the Digilent website. Please see the Nexys 3 page at www.digilentinc.com for more information.

Copyright Digilent, Inc. All rights reserved.
Other product and company names mentioned may be trademarks of their respective owners.

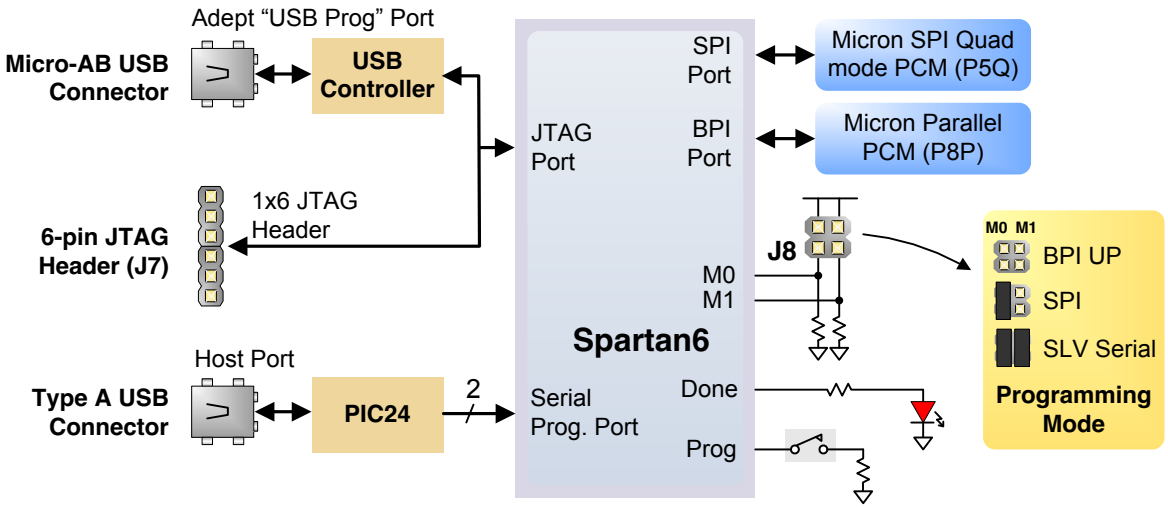


Spartan-6 LX16 features include:

- 2,278 slices each containing four 6-input LUTs and eight flip-flops
- 576Kbits of fast block RAM
- two clock tiles (four DCMs & two PLLs)
- 32 DSP slices
- 500MHz+ clock speeds

1 Configuration

After power-on, the Spartan-6 FPGA board must be configured (or programmed) before it can perform any functions. The FPGA can be configured in one of four ways: a PC can use the Adept "USB Prog" port to program the FPGA any time power is on; a configuration file stored in the non-volatile parallel PCM device can be transferred to the FPGA at power-on using the BPI-UP port; a file stored in the non-volatile serial (SPI) PCM device can be transferred to the FPGA using the SPI port; or a programming file can be transferred from a USB memory stick attached to the USB HID port. An on-board "mode" jumper (J8) selects between the programming modes as shown in the J8 Mode legend in the figure below. JTAG Mode can be accessed at any time without changing jumpers.



Programming files are stored in SRAM-based memory cells within the FPGA. This data defines the FPGA's logic functions and circuit connections, and it remains valid until it is erased by removing board power, by pressing the reset button attached to the PROG input, or by writing a new configuration file using the JTAG port.

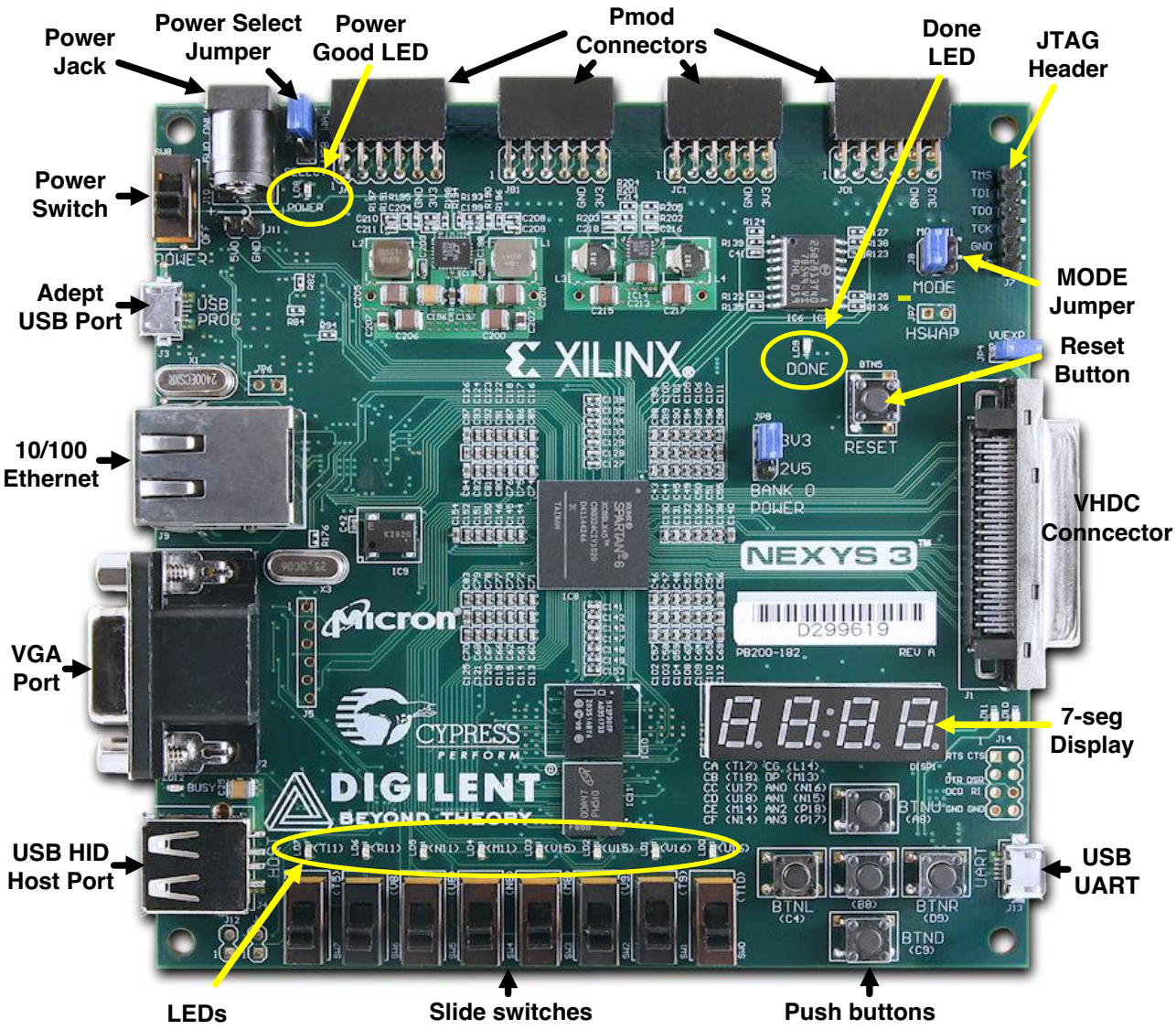
FPGA configuration files transferred via the JTAG port use the .bin or .svf file types, files transferred from a USB stick use the .bit file type, and BPI or SPI programming files can use .bit, .bin, or .mcs types. The ISE/WebPack or EDK software from Xilinx can create bit, svf, bin, or mcs files from VHDL, Verilog, or schematic-based source files

Copyright Digilent, Inc. All rights reserved.
Other product and company names mentioned may be trademarks of their respective owners.

(EDK is used for MicroBlaze™ embedded processor-based designs). Digilent's Adept software or Xilinx's iMPACT software can be used to program the FPGA or ROMs using the Adept USB port.

During JTAG programming, a .bit or .svf file is transferred from the PC to the FPGA using the Adept USB port. When programming a non-volatile PCM device, a .bit, .bin, or .mcs file is transferred to the in a two-step process. First, the FPGA is programmed with a circuit that can program PCM devices, and then data is transferred to the PCM device via the FPGA circuit (this complexity is hidden from the user – a simple "program ROM" interface is presented by the programming software. Note the PCM devices are next-generation Flash ROM devices, and they are often referred to as "Flash" or "ROM" memory). After the PCM device has been programmed, it can automatically configure the FPGA at a subsequent power-on or reset event as determined by the J8 jumper setting. Programming files stored in the PCM devices will remain until they are overwritten, regardless of power-cycle events.
The FPGA can be programmed from a memory stick attached to the USB-HID port if the stick contains a single .bit configuration file in the root directory, the J8 Programming Mode jumper is set to JTAG (both jumpers loaded), and board power is cycled. The FPGA will automatically reject any .bit files that are not built for the proper FPGA.

After being successfully programmed, the FPGA will cause the "Done" LED to illuminate. Pressing the Reset button at any time will reset the configuration memory in the FPGA. After being reset, the FPGA will immediately attempt to reprogram itself from one of the PCM devices if the J8 Mode jumper is set to BPI or SPI mode.



Copyright Digilent, Inc. All rights reserved.
Other product and company names mentioned may be trademarks of their respective owners.

Digilent's Adept software offers a simplified programming interface and many additional features as described below. The Adept USB port is fully compatible with all Xilinx tools, including the iMPACT programming software. The Adept features are always available, regardless of how the FPGA was programmed.

1.1 Adept System

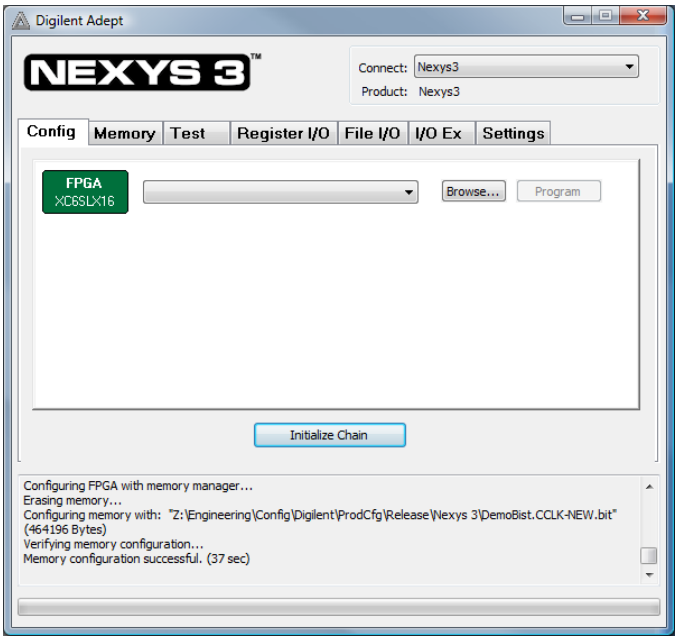
Digilent's Adept high-speed USB2 system can be used to program the FPGA and PCM devices, run automated board tests, add PC-based virtual I/O devices (like buttons, switches, and LEDs) to FPGA designs, and exchange register-based and file-based data with the FPGA. Adept automatically recognizes the Nexys 3 board and presents a graphical interface with tabs for each of these applications. Adept also includes public APIs/DLLs so that users can write applications to exchange data with the Nexys 3 board at up to 38Mbytes/sec. The Adept application, an SDK, and reference materials are freely downloadable from the Digilent website.

1.2 Programming Interface

To program the Nexys 3 board using Adept, first set up the board and initialize the software:

- plug in and attach the power supply
- plug in the USB cable to the PC and to the USB port on the board
- start the Adept software
- turn ON Nexys 3's power switch
- wait for the FPGA to be recognized.

Use the browse function to associate the desired .bit file with the FPGA, and click on the Program button. The configuration file will be sent to the FPGA, and a dialog box will indicate whether programming was successful. The configuration "done" LED will light after the FPGA has been successfully configured.



Before starting the programming sequence, Adept ensures that any selected configuration file contains the correct FPGA ID code – this prevents incorrect .bit files from being sent to the FPGA.

In addition to the navigation bar and browse and program buttons, the Config interface provides an Initialize Chain button, console window, and status bar. The Initialize Chain button is useful if USB communications with the board have been interrupted. The console window displays current status, and the status bar shows real-time progress when downloading a configuration file.

1.3 Memory Interface

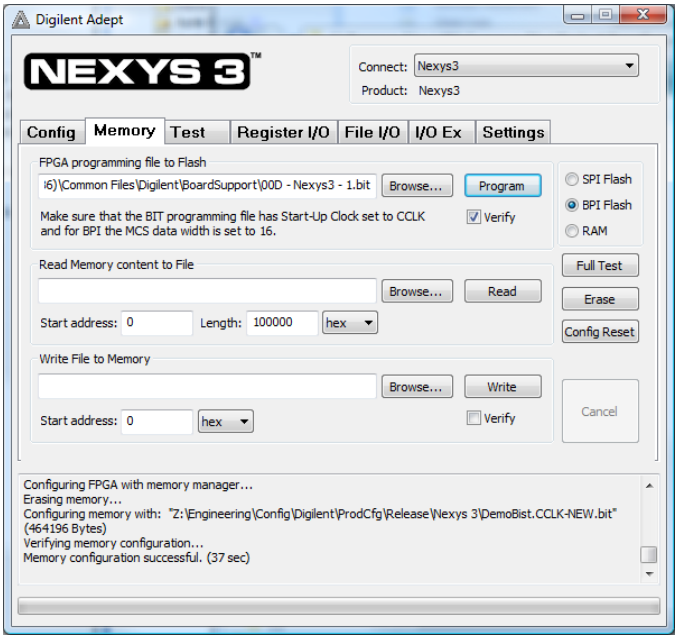
The Memory tab allows .bin, .bit, and .mcs configuration files to be transferred to the on-board BPI (parallel) or SPI (serial) PCM devices for subsequent FPGA programming, and allows user data files to be transferred to/from the PCM devices or RAM memories at user-specified addresses. The target memory is selected by clicking one of the three radio buttons in the upper-right corner.

Copyright Digilent, Inc. All rights reserved.
Other product and company names mentioned may be trademarks of their respective owners.

The configuration tool supports programming from any valid ROM file produced by the Xilinx tools. After programming, board power can either be cycled or the Reset button can be pressed to program the FPGA from the PCM device selected by the J8 mode jumper. If programming with a .bit file, the startup clock must be set to CCLK.

All three memory devices (the PCM's and the cellular RAM) can be fully tested by clicking the Full Test button. They can also be completely erased by clicking the Erase button.

The Read/Write tools allow data to be exchanged between files on the host PC and specified address ranges in the memory devices.

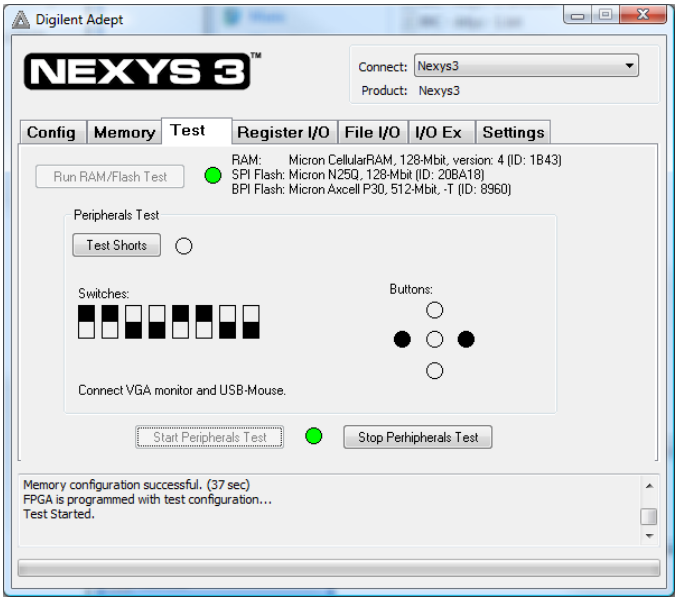


1.4 Test Interface

The test interface provides an easy way to verify many of the board's hardware circuits and interfaces. These are divided into two major categories: on-board memory (RAM and Flash) and peripherals. In both cases, the FPGA is configured with test and PC-communication circuits, overwriting any FPGA configuration that may have been present.

Clicking the Run RAM/Flash Test button will identify the CellularRam, SPI Flash, and BPI Flash memory by reading out and verifying the IDCODE on each memory. The memory contents will not be modified. To run a full test on a particular memory device, refer to the Full Test in the Memory Tab.

Clicking the Start Peripherals Test button will initialize GPIO and user I/O testing. Once the indicator near the Start Peripherals Test button turns green, all peripheral tests can be run.



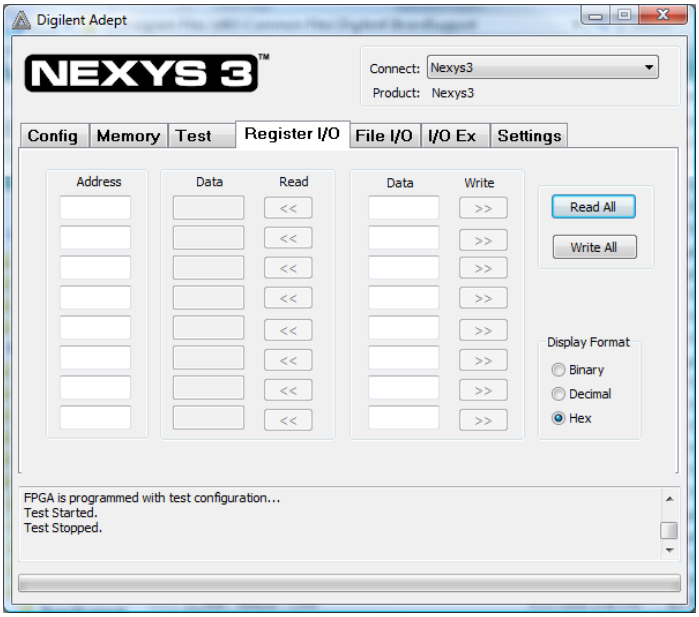
The Test Shorts feature checks all discrete I/O's for shorts to Vdd, GND, and neighboring I/O pins. The switches and buttons graphics show the current states of those devices on the Nexys 3 board. Connect a VGA monitor and USB mouse to visually test the J2 VGA port and J4 USB port respectively.

Copyright Digilent, Inc. All rights reserved.
Other product and company names mentioned may be trademarks of their respective owners.

1.5 Register I/O

The register I/O tab requires that a corresponding IP block, available in the Parallel Interface reference design (DpimRef.vhd) on the Adept page of the Digilent website, is included and active in the FPGA. This IP block provides an EPP-style interface, where an 8-bit address selects a register, and data read and write buttons transfer data to and from the selected address. Addresses entered into the address field must match the physical address included in the FPGA IP block.

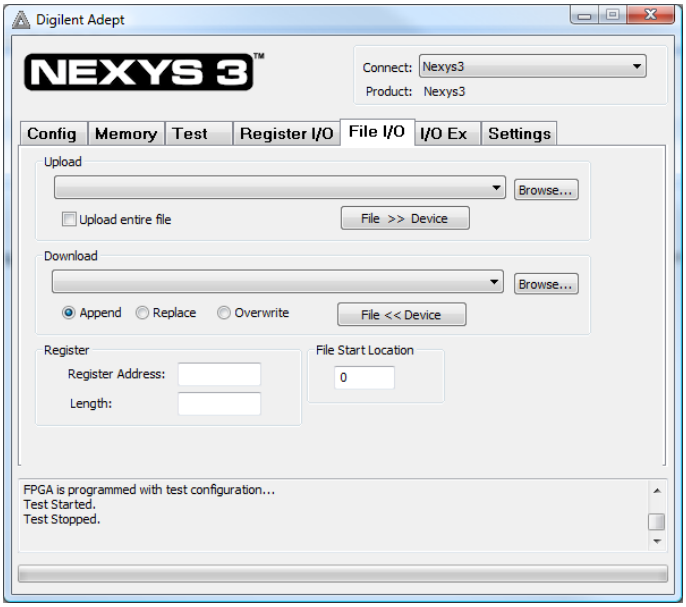
Register I/O provides an easy way to move small amounts of data into and out of specific registers in a given design. This feature greatly simplifies passing control parameters into a design, or reading low-frequency status information out of a design.



1.6 File I/O

The File I/O tab can transfer files between the PC and the Nexys 3 FPGA. A number of bytes (specified by the Length value) can be streamed into a specified register address from a file or out of a specified register address into a file. During upload and download, the file start location can be specified in terms of bytes.

As with the Register I/O tab, File I/O also requires specific IP to be available in the FPGA. This IP can include a memory controller for writing files into the on-board Ram and Flash memories.



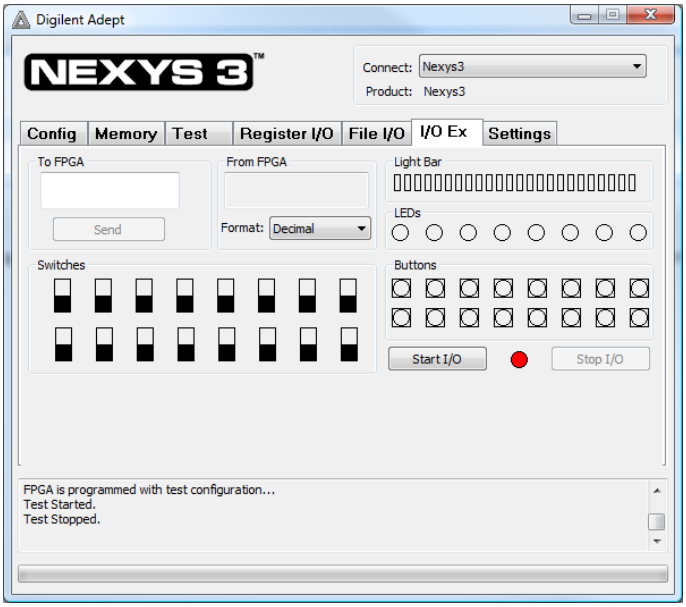
1.7 I/O Expand

The I/O Expand tab works with an IP block in the FPGA to provide additional simple I/O beyond the physical devices found on the Nexys 3 board. Virtual I/O devices include a 24-LED light bar, 16 slide switches, 16 push buttons, 8 discrete LEDs, a 32-bit register that can be sent to the FPGA, and a 32-bit register that can be read from the FPGA.

Copyright Digilent, Inc. All rights reserved.
Other product and company names mentioned may be trademarks of their respective owners.

The IP block, available in the Adept I/O Expansion reference design (AdeptIOExpansion.zip) on the Adept page of the Digilent website, provides a simple interface with well-defined signals. This IP block can easily be included in, and accessed from, user-defined circuits.

For more information, see the Adept documentation available at the Digilent website.



2 Power Supplies

The Nexys 3 board can receive power from the Adept USB port or from an external power supply. Jumper JP1 (near the power jack) determines which source is used.

The USB port can deliver enough power for the vast majority of designs. It is possible that a very demanding application, including an application that drives many peripheral boards, might require more power than can be delivered by the USB port. Some applications may also need to run without being connected to a PC's USB port. In either case, an external power supply or battery pack can be used by setting JP1 to "Wall".

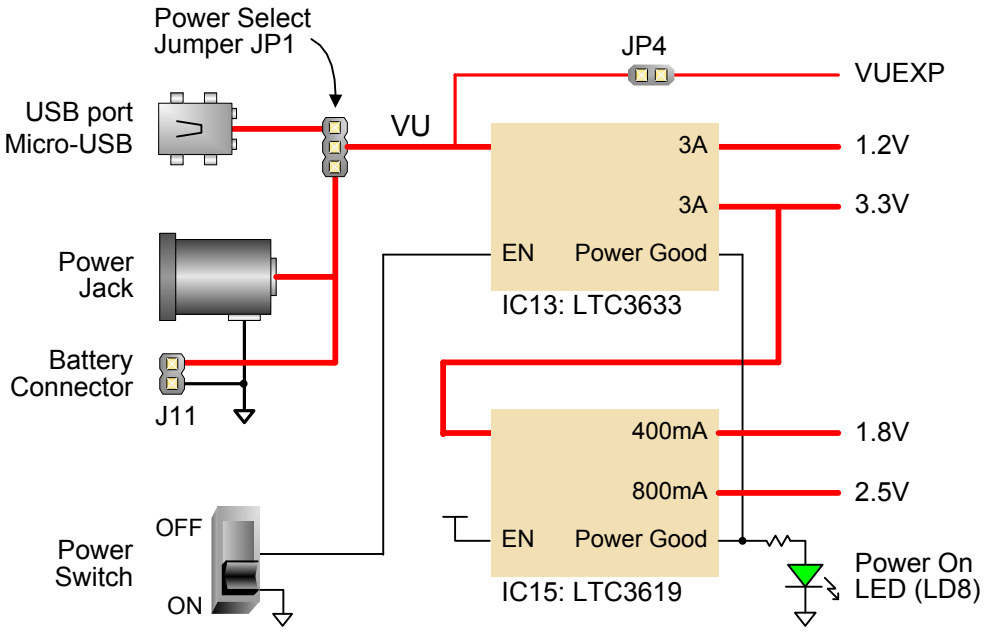
The main regulator on the Nexys 3 can accommodate input voltages up to 5.5VDC. An external DC wall-plug supply should provide at least five watts of input power, and use a coax center-positive 2.1mm internal-diameter plug. An external battery pack can also be used by connecting the battery's terminal leads to connector J11 (J11 is in parallel with the wall-plug power jack, so if a battery pack is connected, a wall plug should not be). An external battery pack should also be limited to 5.5VDC, and should be capable of delivering adequate power for the application.

Voltage regulator circuits from Linear Technology create the required 3.3V, 2.5V, 1.8V, and 1.2V supplies from the main power input. The table below provides additional information (typical currents depend strongly on FPGA configuration and the values provided are typical of medium size/speed designs).

Supply	Circuits	Device	Amps (max/typ)
3.3V	FPGA I/O, USB ports, Clocks, ROM & RAM I/O, Ethernet	IC13: LTC3633	3A / 200mA
2.5V	Optional voltage for Bank0 and VHDC connector	IC14: LTC3619	800mA / 0mA
1.2V	FPGA Core	IC13: LTC3633	3A / 0.2 to 1.0A
1.8V	RAM and ROM core	IC14: LTC3619	400mA / 0.1 to 0.3A

Table 1. Nexys 3 Power Supplies.

Copyright Digilent, Inc. All rights reserved.
Other product and company names mentioned may be trademarks of their respective owners.



The Nexys 3 power supplies are enabled (or turned on) by a logic-level Power switch (SW8). A power-good LED (LD8), driven by the wired-OR of the "power good" outputs on the supplies, indicates that all supplies are operating within 10% of nominal.

The VU output of the main power jumper (JP1) is available to the VHDC expansion connector if jumper JP4 is loaded. Care must be taken to ensure the VUEXP delivered to any attached expansion board is the correct voltage – since VU is driven directly from an attached supply, this means a supply of the proper voltage must be used (e.g., 5V).

3 Memory

The Nexys 3 board contains three external memories, all from Micron: a 128Mbit Cellular RAM (pseudo-static DRAM); a 128Mbit parallel non-volatile PCM (phase-change memory); and a 128Mbit serial PCM device. The Cellular RAM and parallel PCM device share a common bus, and the serial PCM is on a dedicated quad-mode (x4) SPI bus. The non-volatile PCM memories are byte and bit alterable without requiring a block erase, so they are faster and more versatile than conventional Flash in most applications.

The 16Mbyte Cellular RAM (Micron part number M45W8MW16) has a 16-bit bus that supports 8 or 16 bit data access. It can operate as a typical asynchronous SRAM with read and write cycle times of 70ns, or as a synchronous memory with an 80MHz bus. When operated as an asynchronous SRAM, the Cellular RAM automatically refreshes its internal DRAM arrays, allowing for a simplified memory controller (similar to any SRAM controller). When operated in synchronous mode, continuous transfers of up to 80MHz are possible.

The parallel PCM device (Micron part number NP8P128A13T1760E) is organized as 8Mwords of 16bits each. It contains 128 individually erasable 64K-blocks, one of which is subdivided into four 16K "parameter blocks" that can offer increased data protection. Normally, a device with a parameter block at the high end of the address space is loaded (a "top parameter" block device). The parallel PCM memory offers 115ns read cycle times, with 25ns page-mode reads within blocks. It has an internal 64-byte write buffer that can be written with 50ns cycle times, and the 64-byte buffer can be transferred to the Flash array in 120us (typical). The parallel PCM device also contains an SPI

Copyright Digilent, Inc. All rights reserved.
Other product and company names mentioned may be trademarks of their respective owners.

port for serial data transfer, but that function is not enabled on the Nexys 3 board (the ADV and WAIT signals are connected between the FPGA and PCM, but they serve no functions).

The Cellular RAM and parallel PCM share a common 16-bit data bus and 24-bit address bus. The Cellular RAM is byte addressable using the upper-byte and lower-byte signals (MT-UB and MT-LB), but the P8P PCM is configured for 16 byte operations only (it is not byte addressable). The output enable (OE) and write enable (WE) signals are shared by both devices, but each device has individual chip enable (CE) signals. Additionally, the Cellular RAM has clock (MT-CLK), wait (MT-WAIT), address valid (MT-ADV) and control register enable (MT_CRE) signals available to the FPGA for use with synchronous transfers, and the PCM device has Reset (RP#). With simple changes, the Nexys 3 board can accommodate either the PCM device or the older "P33" Flash device. The signal names in the Nexys 3 schematic reference the P33 device; the P33 ADV and WAIT signals are not used in by the PCM device.

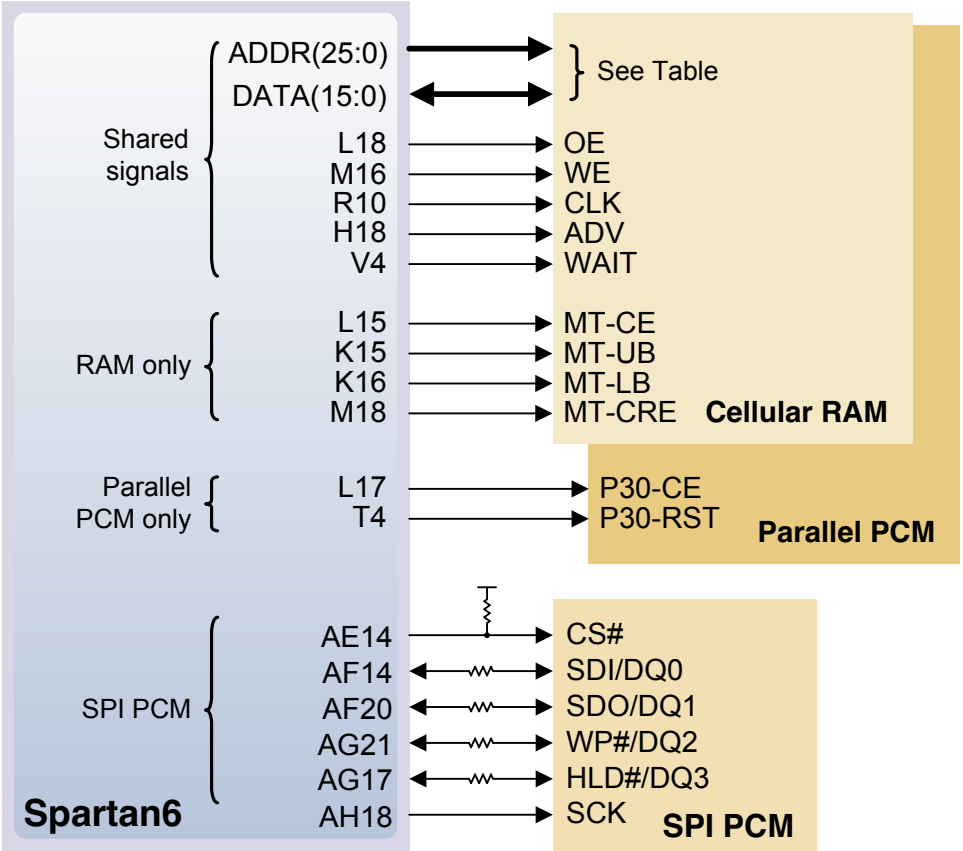
The 16Mbyte serial PCM device (Micron part number NP5Q128A13ESFC0E) is also bit alterable without requiring an erase cycle. It supports the legacy SPI protocol as well as the newer Quad I/O and Dual I/O protocols, at bus speeds up to 50MHz.

FPGA configuration files can be written to both PCM devices, and mode settings are available to cause the FPGA to automatically read a configuration from one of these devices at power on. A Spartan-6 LX16 configuration file requires about 512Kbytes of memory, leaving about 97% of the PCM devices available for user data.

Both PCM devices are loaded with configuration files at the factory. The SPI PCM device contains a file that configures the FPGA to test the Nexys 3 memory devices during manufacturing, and this file isn't needed after the board test is complete. The BPI PCM device contains a file that configures the Nexys 3 with a basic user demonstration program, and it can be used to verify board functions. This same .bit file is available for download from the Digilent website. If Mode jumper J8 is set to BPI mode and power is applied, the user demo configuration will be loaded. The demo drives a counter on the 7-segment display, drives the user LEDs on and off when the user switches are toggled, turns off digits on the 7-segment display when user buttons are pressed, and drives an image out the VGA port. A USB mouse can be connected to J4 for a simple visual demonstration.

Please refer to the manufacturer's data sheets and the reference designs posted on Digilent's website for more information about the memory devices.

Copyright Digilent, Inc. All rights reserved.
Other product and company names mentioned may be trademarks of their respective owners.



Address Bus			Data Bus	
ADDR25: F15	ADDR16: G13	ADDR7: H15	DATA15: T8	DATA6: T3
ADDR24: F16	ADDR15: E16	ADDR6: H16	DATA14: R8	DATA5: R3
ADDR23: C17	ADDR14: E18	ADDR5: G16	DATA13: U10	DATA4: V5
ADDR22: C18	ADDR13: K12	ADDR4: G18	DATA12: V13	DATA3: U5
ADDR21: F14	ADDR12: K13	ADDR3: J16	DATA11: U13	DATA2: V14
ADDR20: G14	ADDR11: F17	ADDR2: J18	DATA10: P12	DATA1: T14
ADDR19: D17	ADDR10: F18	ADDR1: K17	DATA9: P6	DATA0: R13
ADDR18: D18	ADDR9: H13	ADDR0: K18	DATA8: N5	
ADDR17: H12	ADDR8: H14		DATA7: R5	

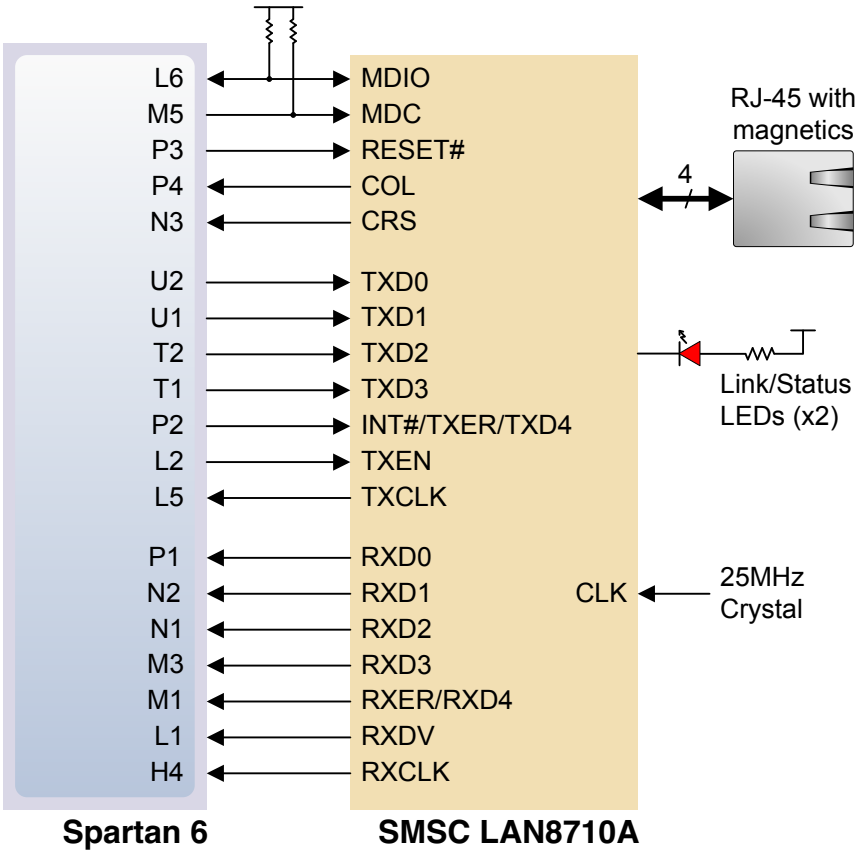
4 Ethernet PHY

The Nexys 3 board includes an SMSC 10/100 Ethernet PHY (SMSC part number LAN8710) paired with an RJ-45 Ethernet jack with integrated magnetics. EDK-based designs can access the PHY using either the xps_ethernetlite IP core or the xps_ll_temac IP core. The Nexys 3 Base System Builder (BSB) support package automatically generates a test application for the Ethernet MAC; this can be used as a reference for creating custom designs. ISE designs can use the IP Core Generator wizard to create an Ethernet MAC controller IP core. The SMSC PHY uses the MII interface and supports 10/100 Mb/s. At power-on reset, the PHY is set to the following defaults:

- MII mode interface
- 100Base-TX with auto negotiation enabled, advertising half-duplex, with CRS active during receive
- PHY address = 000

Copyright Digilent, Inc. All rights reserved.
Other product and company names mentioned may be trademarks of their respective owners.

Refer to the LAN8710A data sheet on the www.smsc.com website for further information.



5 Oscillators/Clocks

The Nexys 3 board includes a single 100MHz CMOS oscillator connected to pin V10 (V10 is the GCLK0 input in bank 2). The input clock can drive any or all of the four clock management tiles in the Spartan-6. Each tile includes two Digital Clock Managers (DCMs) and four Phase-Locked Loops (PLLs).

DCMs provide the four phases of the input frequency (0º, 90º, 180º, and 270º), a divided clock that can be the input clock divided by any integer from 2 to 16 or 1.5, 2.5, 3.5... 7.5, and two antiphase clock outputs that can be multiplied by any integer from 2 to 32 and simultaneously divided by any integer from 1 to 32.

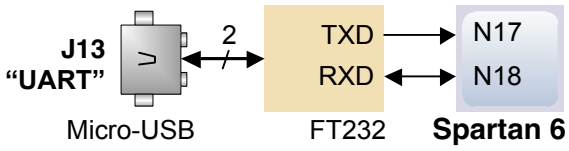
PLLs use VCOs that can be programmed to generate frequencies in the 400MHz to 1080MHz range by setting three sets of programmable dividers during FPAG configuration. VCO outputs have eight equally-spaced outputs (0º, 45º, 90º, 135º, 180º, 225º, 270º, and 315º) that can be divided by any integer between 1 and 128.

Please refer to the Spartan-6 data sheet at www.xilinx.com for further information on the clock management tiles.

Copyright Digilent, Inc. All rights reserved.
Other product and company names mentioned may be trademarks of their respective owners.

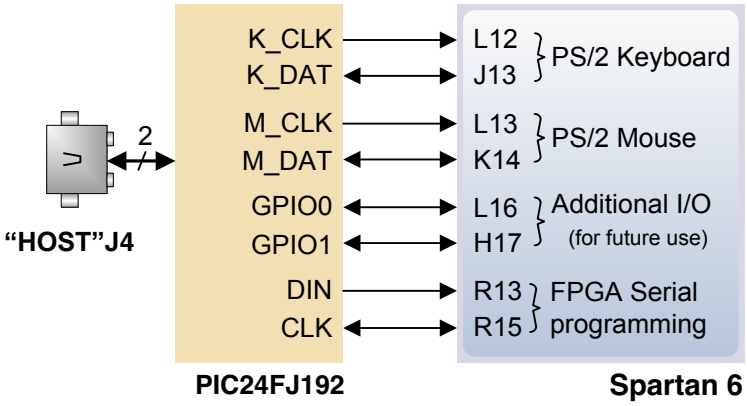
6 USB-UART Bridge (Serial Port)

The Nexys 3 includes an FTDI FT232 USB-UART bridge to allow PC applications to communicate with the board using standard Windows COM port commands. Free USB-COM port drivers, available from www.ftdichip.com under the "Virtual Com Port" or VCP heading, convert USB packets to UART/serial port data. Serial port data is exchanged with the FPGA using a two-wire serial port (TXD/RXD) and software flow control (XON/XOFF). After the drivers are installed, I/O commands from the PC directed to the COM port will produce serial data traffic on the N17 and N18 FPGA pins.



7 USB HID Host

A Microchip PIC24FJ192 microcontroller provides the Nexys 3 with USB H ID host capability. Firmware in the microcontroller can drive a mouse or a keyboard attached to the type A USB connector at J4 labeled "Host". Hub support is not currently available, so only a single mouse or a single keyboard can be used. The PIC24 drives four signals into the FPGA – two are used as a keyboard port following the keyboard PS/2 protocol, and two are used as a mouse port following the mouse PS/2 protocol.

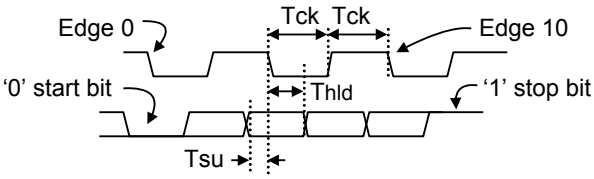


Two PIC24 I/O pins are also connected to the FPGA's two-wire serial programming port, so the FPGA can be programmed from a file stored on a USB memory stick. To program the FPGA, attach a memory stick containing a single .bit programming file in the root directory, load both M0 and M1 on J8 jumper, and cycle board power. This will cause the PIC processor to program the FPGA, and any incorrect bit files will automatically be rejected. Note the PIC24 reads the FPGA's mode, init, and done pins, and can drive the PROG pin as a part of the programming sequence.

7.1 HID Controller

To access the USB host controller, EDK designs can use the standard PS/2 core (non-EDK designs can use a simple state machine).

Mice and keyboards that use the PS/2 protocol[1] use a two-wire serial bus (clock and data) to communicate with a host device. Both use 11-bit words that include a start, stop, and



Symbol	Parameter	Min	Max
T_{CK}	Clock time	30us	50us
T_{SU}	Data-to-clock setup time	5us	25us
T_{HLD}	Clock-to-data hold time	5us	25us

[1]Not all keyboard manufacturers strictly adhere to the PS/2 specifications; some keyboards may not produce the proper signaling voltages or use the standard communication protocols. Compatibility with the USB host may vary between different keyboards.

Copyright Digilent, Inc. All rights reserved.
Other product and company names mentioned may be trademarks of their respective owners.

odd parity bit, but the data packets are organized differently, and the keyboard interface allows bi-directional data transfers (so the host device can illuminate state LEDs on the keyboard). Bus timings are shown in the figure. The clock and data signals are only driven when data transfers occur, and otherwise they are held in the idle state at logic '1'. The timings define signal requirements for mouse-to-host communications and bi-directional keyboard communications. A PS/2 interface circuit can be implemented in the FPGA to create a keyboard or mouse interface.

7.2 Keyboard

The keyboard uses open-collector drivers so the keyboard, or an attached host device, can drive the two-wire bus (if the host device will not send data to the keyboard, then the host can use input-only ports).

PS/2-style keyboards use scan codes to communicate key press data. Each key is assigned a code that is sent whenever the key is pressed. If the key is held down, the scan code will be sent repeatedly about once every 100ms. When a key is released, an F0 key-up code is sent, followed by the scan code of the released key. If a key can be shifted to produce a new character (like a capital letter), then a shift character is sent in addition to the scan code, and the host must determine which ASCII character to use. Some keys, called extended keys, send an E0 ahead of the scan code (and they may send more than one scan code). When an extended key is released, an E0 F0 key-up code is sent, followed by the scan code. Scan codes for most keys are shown in the figure. A host device can also send data to the keyboard. Below is a short list of some common commands a host might send.

ED Set Num Lock, Caps Lock, and Scroll Lock LEDs. Keyboard returns FA after receiving ED, then host sends a byte to set LED status: bit 0 sets Scroll Lock, bit 1 sets Num Lock, and bit 2 sets Caps lock. Bits 3 to 7 are ignored.

EE Echo (test). Keyboard returns EE after receiving EE.

F3 Set scan code repeat rate. Keyboard returns F3 on receiving FA, then host sends second byte to set the repeat rate.

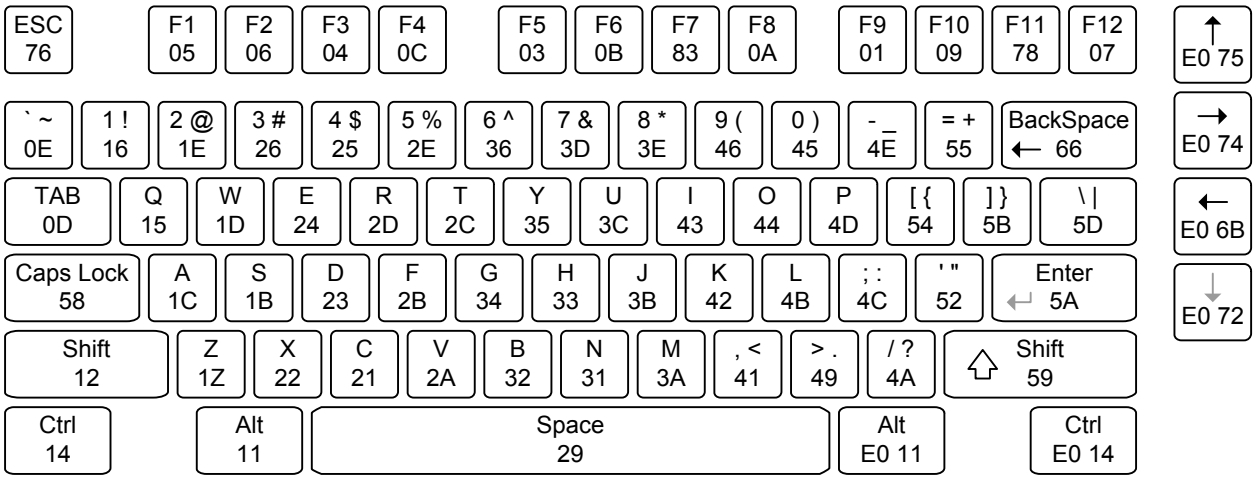
FE Resend. FE directs keyboard to re-send most recent scan code.

FF Reset. Resets the keyboard.

The keyboard can send data to the host only when both the data and clock lines are high (or idle). Since the host is the bus master, the keyboard must check to see whether the host is sending data before driving the bus. To facilitate this, the clock line is used as a "clear to send" signal. If the host pulls the clock line low, the keyboard must not send any data until the clock is released. The keyboard sends data to the host in 11-bit words that contain a '0' start bit, followed by 8-bits of scan code (LSB first), followed by an odd parity bit and terminated with a '1' stop bit. The keyboard generates 11 clock transitions (at 20 to 30KHz) when the data is sent, and data is valid on the falling edge of the clock.

Scan codes for most PS/2 keys are shown in the figure below.

Copyright Digilent, Inc. All rights reserved.
Other product and company names mentioned may be trademarks of their respective owners.

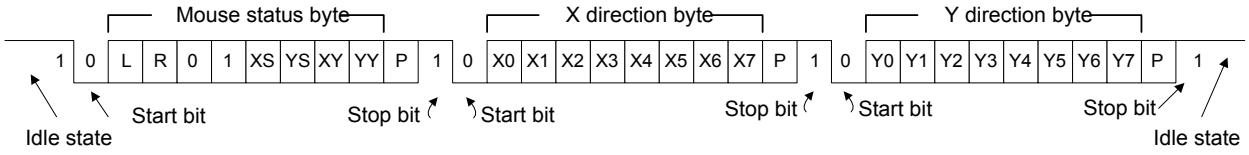


PS/2 keyboard scan codes.

7.3 Mouse

The mouse outputs a clock and data signal when it is moved, otherwise, these signals remain at logic '1'. Each time the mouse is moved, three 11-bit words are sent from the mouse to the host device. Each of the 11-bit words contains a '0' start bit, followed by 8 bits of data (LSB first), followed by an odd parity bit, and terminated with a '1' stop bit. Thus, each data transmission contains 33 bits, where bits 0, 11, and 22 are '0' start bits, and bits 11, 21, and 33 are '1' stop bits. The three 8-bit data fields contain movement data as shown in the figure above. Data is valid at the falling edge of the clock, and the clock period is 20 to 30KHz.

The mouse assumes a relative coordinate system wherein moving the mouse to the right generates a positive number in the X field, and moving to the left generates a negative number. Likewise, moving the mouse up generates a positive number in the Y field, and moving down represents a negative number (the XS and YS bits in the status byte are the sign bits – a '1' indicates a negative number). The magnitude of the X and Y numbers represent the rate of mouse movement – the larger the number, the faster the mouse is moving (the XV and YV bits in the status byte are movement overflow indicators – a '1' means overflow has occurred). If the mouse moves continuously, the 33-bit transmissions are repeated every 50ms or so. The L and R fields in the status byte indicate Left and Right button presses (a '1' indicates the button is being pressed).



Mouse data format.

8 VGA Port

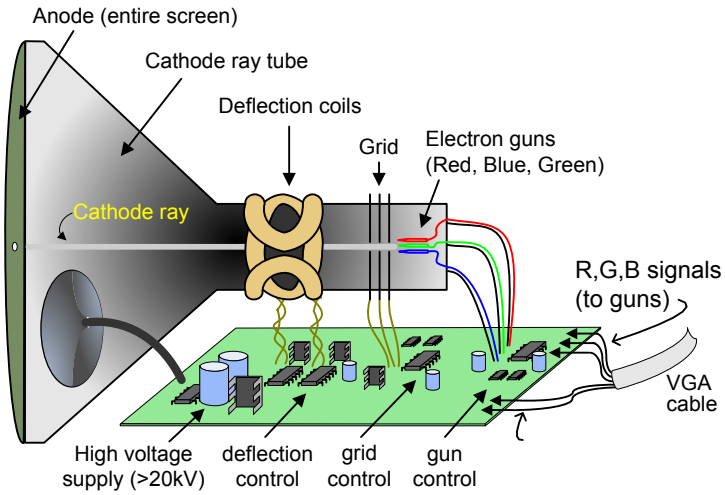
The Nexys 3 board uses 10 FPGA signals to create a VGA port with 8-bit color and the two standard sync signals (HS – Horizontal Sync, and VS – Vertical Sync). The color signals use resistor-divider circuits that work in conjunction with the 75-ohm termination resistance of the VGA display to create eight signal levels on the red and green VGA signals, and four on blue (the human eye is less sensitive to blue levels). This circuit, shown in figure 13, produces

Copyright Digilent, Inc. All rights reserved.
Other product and company names mentioned may be trademarks of their respective owners.

video color signals that proceed in equal increments between 0V (fully off) and 0.7V (fully on). Using this circuit, 256 different colors can be displayed, one for each unique 8-bit pattern. A video controller circuit must be created in the FPGA to drive the sync and color signals with the correct timing in order to produce a working display system.

8.1 VGA System Timing

VGA signal timings are specified, published, copyrighted and sold by the VESA organization (www.vesa.org). The following VGA system timing information is provided as an example of how a VGA monitor might be driven in 640 by 480 mode. For more precise information, or for information on other VGA frequencies, refer to documentation available at the VESA website.

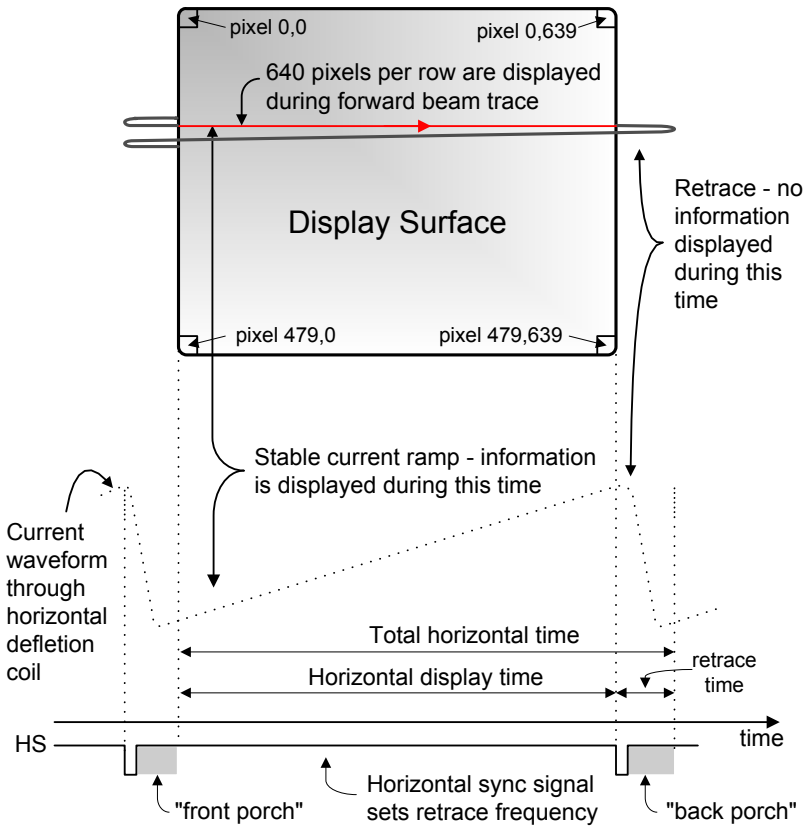


CRT-based VGA displays use amplitude-modulated moving electron beams (or cathode rays) to display information on a phosphor-coated screen. LCD displays use an array of switches that can impose a voltage across a small amount of liquid crystal, thereby changing light permittivity through the crystal on a pixel-by-pixel basis. Although the following description is limited to CRT displays, LCD displays have evolved to use the same signal timings as CRT displays (so the "signals" discussion below pertains to both CRTs and LCDs). Color CRT displays use three electron beams (one for red, one for blue, and one for green) to energize the phosphor that coats the inner side of the display end of a cathode ray tube (see illustration). Electron beams emanate from "electron guns" which are finely-pointed heated cathodes placed in close proximity to a positively charged annular plate called a "grid". The electrostatic force imposed by the grid pulls rays of energized electrons from the cathodes, and those rays are fed by the current that flows into the cathodes. These particle rays are initially accelerated towards the grid, but they soon fall under the influence of the much larger electrostatic force that results from the entire phosphor-coated display surface of the CRT being charged to 20kV (or more). The rays are focused to a fine beam as they pass through the center of the grids, and then they accelerate to impact on the phosphor-coated display surface. The phosphor surface glows brightly at the impact point, and it continues to glow for several hundred microseconds after the beam is removed. The larger the current fed into the cathode, the brighter the phosphor will glow.

Between the grid and the display surface, the beam passes through the neck of the CRT where two coils of wire produce orthogonal electromagnetic fields. Because cathode rays are composed of charged particles (electrons), they can be deflected by these magnetic fields. Current waveforms are passed through the coils to produce magnetic fields that interact with the cathode rays and cause them to transverse the display surface in a "raster" pattern, horizontally from left to right and vertically from top to bottom. As the cathode ray moves over the surface of the display, the current sent to the electron guns can be increased or decreased to change the brightness of the display at the cathode ray impact point.

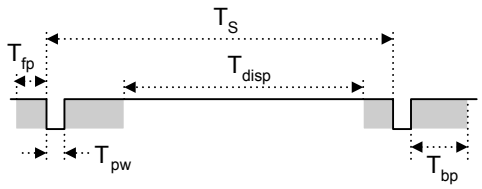
Copyright Digilent, Inc. All rights reserved.
Other product and company names mentioned may be trademarks of their respective owners.

Information is only displayed when the beam is moving in the "forward" direction (left to right and top to bottom), and not during the time the beam is reset back to the left or top edge of the display. Much of the potential display time is therefore lost in "blanking" periods when the beam is reset and stabilized to begin a new horizontal or vertical display pass. The size of the beams, the frequency at which the beam can be traced across the display, and the frequency at which the electron beam can be modulated determine the display resolution. Modern VGA displays can accommodate different resolutions, and a VGA controller circuit dictates the resolution by producing timing signals to control the raster patterns. The controller must produce synchronizing pulses at 3.3V (or 5V) to set the frequency at which current flows through the deflection coils, and it must ensure that video data is applied to the electron guns at the correct time. Raster video displays define a number of "rows" that corresponds to the number of horizontal passes the cathode makes over the display area, and a number of "columns" that corresponds to an area on each row that is assigned to one "picture element" or pixel. Typical displays use from 240 to 1200 rows and from 320 to 1600 columns. The overall size of a display and the number of rows and columns determines the size of each pixel.



Video data typically comes from a video refresh memory, with one or more bytes assigned to each pixel location (the Nexys 3 uses three bits per pixel). The controller must index into video memory as the beams move across the display, and retrieve and apply video data to the display at precisely the time the electron beam is moving across a given pixel.

A VGA controller circuit must generate the HS and VS timings signals and coordinate the delivery of video data based on the pixel clock. The pixel clock defines the time available to display one pixel of information. The VS signal defines the "refresh" frequency of the display, or the frequency at which all information on the display is redrawn. The minimum refresh frequency is a function of the display's phosphor and electron beam intensity, with practical refresh frequencies falling in the 50Hz to 120Hz range. The number of lines to be displayed at a given refresh frequency defines the horizontal "retrace" frequency. For a 640-pixel by 480-row display using a 25MHz pixel clock and 60 +/-1Hz refresh, the signal timings shown in the table at right

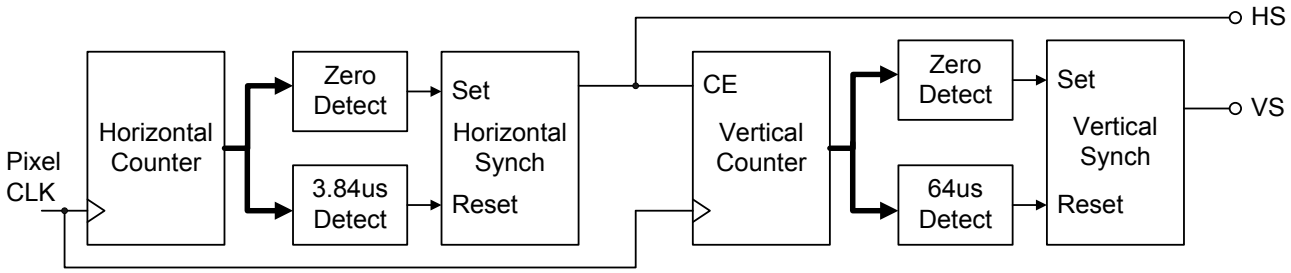


Symbol	Parameter	Vertical Sync			Horiz. Sync	
		Time	Clocks	Lines	Time	Clks
T_S	Sync pulse	16.7ms	416,800	521	32 us	800
T_{disp}	Display time	15.36ms	384,000	480	25.6 us	640
T_{pw}	Pulse width	64 us	1,600	2	3.84 us	96
T_{fp}	Front porch	320 us	8,000	10	640 ns	16
T_{bp}	Back porch	928 us	23,200	29	1.92 us	48

Copyright Digilent, Inc. All rights reserved.
Other product and company names mentioned may be trademarks of their respective owners.

can be derived. Timings for sync pulse width and front and back porch intervals (porch intervals are the pre- and post-sync pulse times during which information cannot be displayed) are based on observations taken from actual VGA displays.

A VGA controller circuit decodes the output of a horizontal-sync counter driven by the pixel clock to generate HS signal timings. This counter can be used to locate any pixel location on a given row. Likewise, the output of a vertical-sync counter that increments with each HS pulse can be used to generate VS signal timings, and this counter can be used to locate any given row. These two continually running counters can be used to form an address into video RAM. No time relationship between the onset of the HS pulse and the onset of the VS pulse is specified, so the designer can arrange the counters to easily form video RAM addresses, or to minimize decoding logic for sync pulse generation.

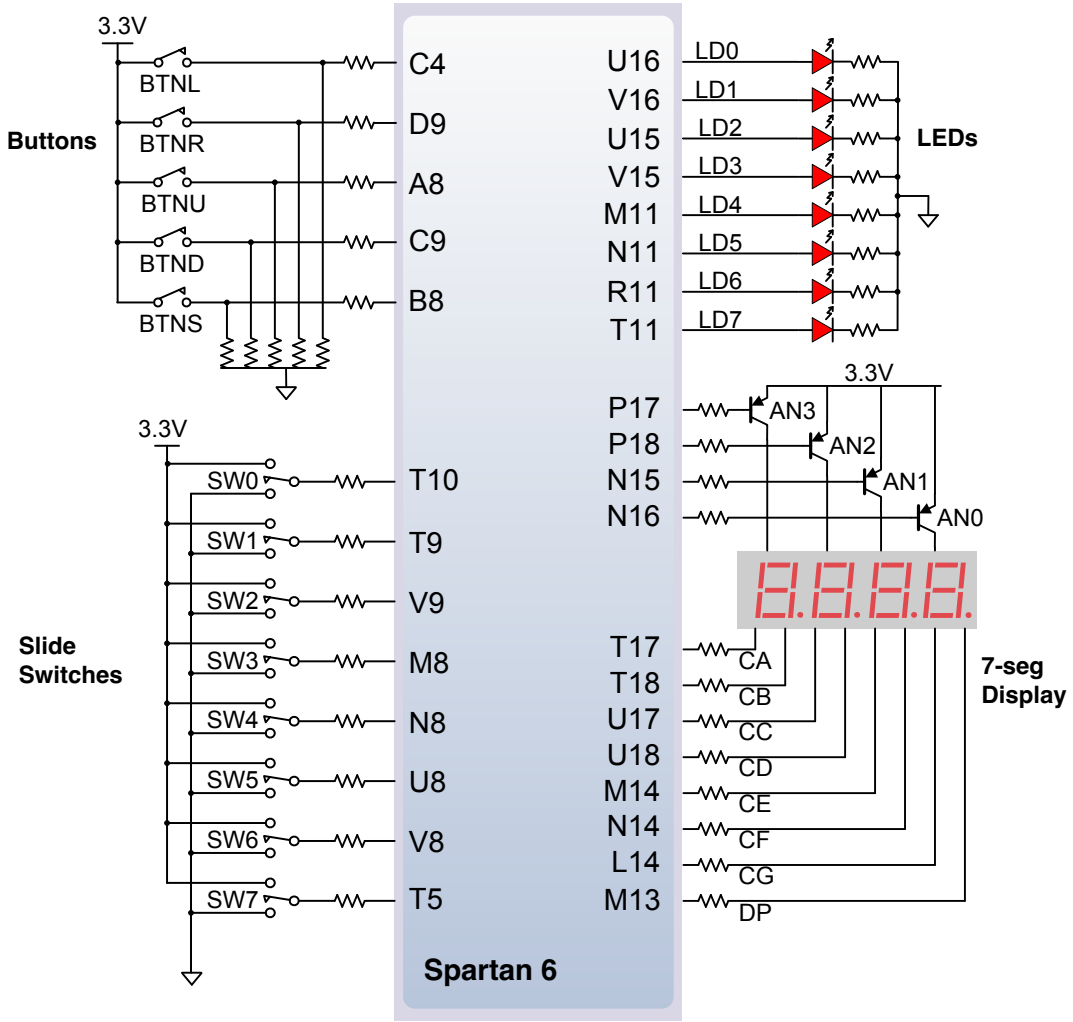


9 Basic I/O

The Nexys 3 board includes eight slide switches, five push buttons, eight individual LEDs, and a four digit seven-segment display. The pushbuttons and slide switches are connected to the FPGA via series resistors to prevent damage from inadvertent short circuits (a short circuit could occur if an FPGA pin assigned to a pushbutton or slide switch was inadvertently defined as an output). The pushbuttons are "momentary" switches that normally generate a low output when they are at rest, and a high output only when they are pressed. Slide switches generate constant high or low inputs depending on their position.

The eight individual high-efficiency LEDs are anode-connected to the FPGA via 390-ohm resistors, so they will turn on when a logic high voltage is applied to their respective I/O pin. Additional LEDs that are not user-accessible indicate power-on, FPGA programming status, and USB and Ethernet port status.

Copyright Digilent, Inc. All rights reserved.
Other product and company names mentioned may be trademarks of their respective owners.

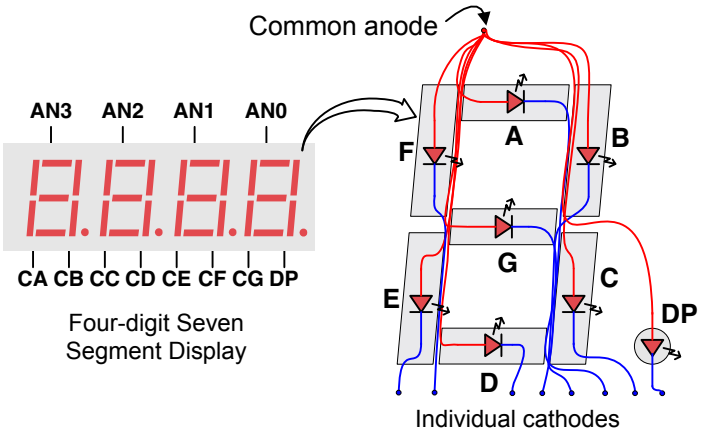


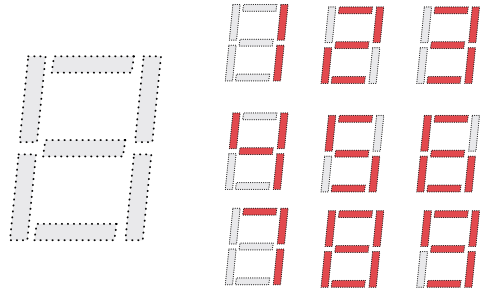
9.1 Seven-Segment Display

The Nexys 3 board contains a four-digit common anode seven-segment LED display. Each of the four digits is composed of seven segments arranged in a "figure 8" pattern, with an LED embedded in each segment. Segment LEDs can be individually illuminated, so any one of 128 patterns can be displayed on a digit by illuminating certain LED segments and leaving the others dark. Of these 128 possible patterns, the ten corresponding to the decimal digits are the most useful.

The anodes of the seven LEDs forming each digit are tied together into one "common anode" circuit node, but the LED cathodes remain separate. The common anode signals are available as four "digit enable" input signals to the 4-digit display. The cathodes of similar segments on all four displays are connected into seven circuit nodes labeled CA through CG (so, for example, the four "D" cathodes from the four digits are grouped together into a single circuit node called "CD"). These seven cathode signals are available as inputs to the 4-digit display. This signal connection scheme creates a multiplexed display, where the cathode signals are common to all digits but they can only illuminate the segments of the digit whose corresponding anode signal is asserted.

Copyright Digilent, Inc. All rights reserved.
Other product and company names mentioned may be trademarks of their respective owners.

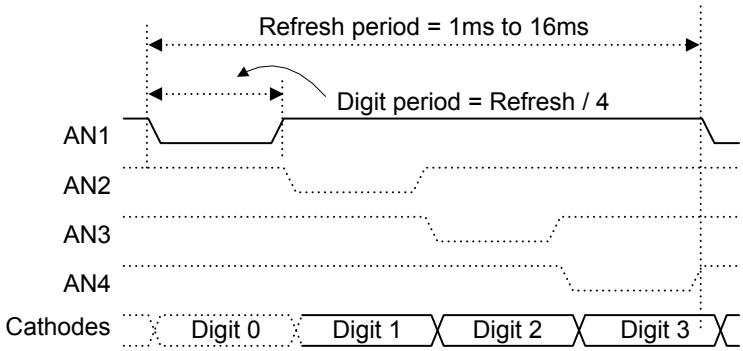




An un-illuminated seven-segment display, and nine illumination patterns corresponding to decimal digits

A scanning display controller circuit can be used to show a four-digit number on this display. This circuit drives the anode signals and corresponding cathode patterns of each digit in a repeating, continuous succession, at an update rate that is faster than the human eye can detect. Each digit is illuminated just one-quarter of the time, but because the eye cannot perceive the darkening of a digit before it is illuminated again, the digit appears continuously illuminated. If the update or "refresh" rate is slowed to around 45 hertz, most people will begin to see the display flicker.

In order for each of the four digits to appear bright and continuously illuminated, all four digits should be driven once every 1 to 16ms, for a refresh frequency of 1KHz to 60Hz. For example, in a 60Hz refresh scheme, the entire display would be refreshed once every 16ms, and each digit would be illuminated for ¼ of the refresh cycle, or 4ms. The controller must drive the cathodes with the correct pattern when the corresponding anode signal is driven. To illustrate the process, if AN0 is asserted while CB and CC are asserted, then a "1" will be displayed in digit position 1. Then, if AN1 is asserted while CA, CB and CC are asserted, then a "7" will be displayed in digit position 2. If AN0 and CB, CC are driven for 4ms, and then A1 and CA, CB, CC are driven for 4ms in an endless succession, the display will show "17" in the first two digits. An example timing diagram for a four-digit controller is provided.



10 Expansion Connectors

The Nexys 3 board has a 68-pin VHDC connector for high-speed/parallel I/O, and an 8-pin Pmod port for lower speed and lower pin-count I/O.

10.1 VHDC Connector

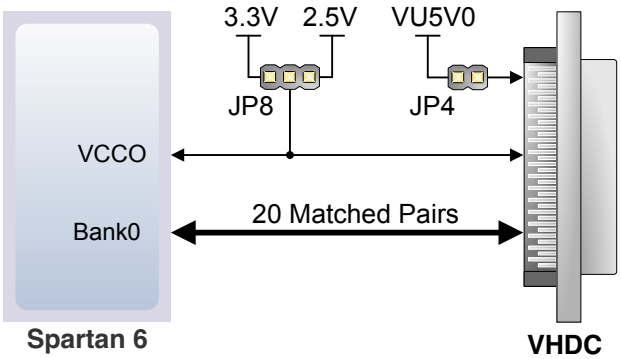
The VHDC connector includes 40 data signals (routed as 20 impedance-controlled matched pairs), 20 grounds (one per pair), and eight power signals. This connector, commonly used for SCSI-3 applications, can accommodate data rates of several hundred megahertz on every pin. Both board-to-board and board-to-cable mating connectors are available. Data sheets for the VHDC connector and for mating board and cable connectors can be found on the Digilent website, as well as on other vendor and distributor websites. Mating connectors and cables of various lengths are also available from Digilent and from distributors.

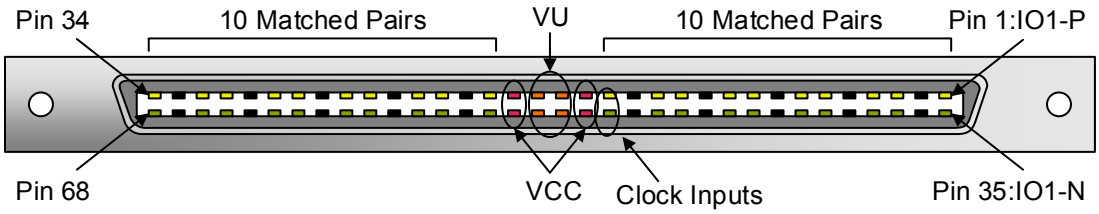
Copyright Digilent, Inc. All rights reserved.
Other product and company names mentioned may be trademarks of their respective owners.

All FPGA pins routed to the VHDC connector are located in FPGA I/O bank0. The FPGA's bank0 I/O power supply pins and the VHDC connector's four Vcc pins are connected together by a small, segregated power supply plane in the PCB. This sub-plane can be connected to 2.5V or 3.3V, depending on the position of jumper JP8. This arrangement allows peripheral boards and the FPGA to share the same Vcc and signaling voltage across the connector, whether it be 3.3V or 2.5V.

The unregulated board voltage VU5V0 (nominally 5V) is also routed to four other VHDC pins, supplying up to 1A of additional current to peripheral boards. A second jumper (JP4) allows the unregulated board voltage to be disconnected from the VHDC connector if desired.

All I/O's to the VHDC connector are routed as matched pairs to support LVDS signaling, commonly powered at 2.5V. The connector uses a symmetrical pinout (as reflected around the connector's vertical axis) so that peripheral boards as well as other system boards can be connected. Connector pins 15 and 49 are routed to FPGA clock input pins.





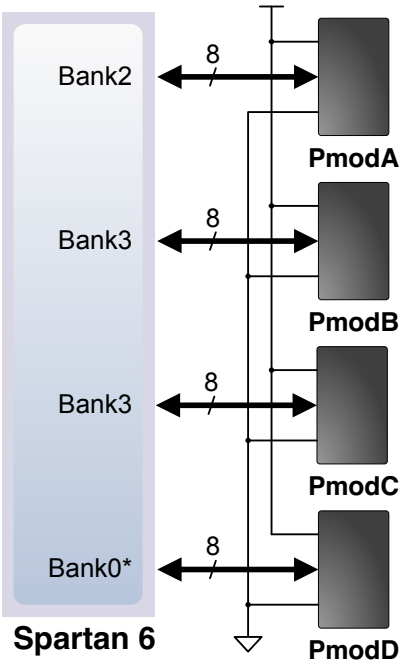
VHDC Connector Pinout			
IO1-P: B2	IO1-N: A2	IO11-P: C10	IO11-N: A10
IO2-P: D6	IO2-N: C6	IO12-P: G9	IO12-N: F9
IO3-P: B3	IO3-N: A3	IO13-P: B11	IO13-N: A11
IO4-P: B4	IO4-N: A4	IO14-P: B12	IO14-N: A12
IO5-P: C5	IO5-N: A5	IO15-P: C13	IO15-N: A13
IO6-P: B6	IO6-N: A6	IO16-P: B14	IO16-N: A14
IO7-P: C7	IO7-N: A7	IO17-P: F13	IO17-N: E13
IO8-P: D8	IO8-N: C8	IO18-P: C15	IO18-N: A15
IO9-P: B9	IO9-N: A9	IO19-P: D14	IO19-N: C14
IO10-P: D11	IO10-N: C11	IO20-P: B16	IO20-N: A16

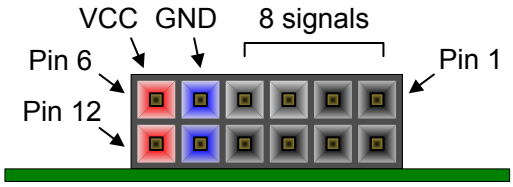
10.2 Pmod Ports

Pmod ports are 2x6 right-angle, 100-mil female connectors that mate with standard 2x6 pin headers available from a variety of catalog distributors. Each 12-pin Pmod port provides two 3.3V VCC signals (pins 6 and 12), two Ground signals (pins 5 and 11), and eight logic signals. VCC and Ground pins can deliver up to 1A of current. Pmod data

Copyright Digilent, Inc. All rights reserved.
Other product and company names mentioned may be trademarks of their respective owners.

signals are not matched pairs, and they are routed using best-available tracks without impedance control or delay matching.





Pmod Connectors – front view as loaded on PCB

Pmod Pinouts			
JA1: T12	JB1: K2	JC1: H3	JD1: G11
JA2: V12	JB2: K1	JC2: L7	JD2: F10
JA3: N10	JB3: L4	JC3: K6	JD3: F11
JA4: P11	JB4: L3	JC4: G3	JD4: E11
JA7: M10	JB7: J3	JC7: G1	JD7: D12
JA8: N9	JB8: J1	JC8: J7	JD8: C12
JA9: U11	JB9: K3	JC9: J6	JD9: F12
JA10: V11	JB10: K5	JC10: F2	JD10: E12

Digilent produces a large collection of Pmod accessory boards that can attach to the Pmod and VHDC expansion connectors to add ready-made functions like A/D's, D/A's, motor drivers, sensors, cameras and other functions. See www.digilentinc.com for more information.

11 Built-In Self Test

A demonstration configuration is loaded into the BPI PCM device on the Nexys 3 board during manufacturing. This demo bit file is available for download from the Digilent website. If the demo configuration is present in the BPI PCM device and the Nexys 3 board is powered on in BPI mode, a simple demo project will allow basic hardware verification. The demo drives a counter on the 7-segment display, drives the user LEDs on and off when the user switches are toggled, turns off digits on the 7-segment display when user buttons are pressed, and drives an image out the VGA port. A USB mouse can be connected to J4 for a simple visual demonstration.

If the demo configuration is not present in the BPI device, it can be downloaded from the Digilent website and programmed directly into the FPGA or reloaded into the PCM device using the Adept programming software. The same basic functionality is also available using the automated Test tab in the Adept application. Using the Test tab automatically loads a demo configuration into the FPGA, so no separate bit files or project need to be used.

All Nexys 3 boards are 100% tested during the manufacturing process. If any device on the Nexys 3 board fails test or is not responding properly, it is likely that damage occurred during transport or during use. Typical damage includes stressed solder joints and contaminants in switches and buttons resulting in intermittent failures. Stressed solder joints can be repaired by reheating and reflowing solder and contaminants can be cleaned with off-the-shelf electronics cleaning products. If a board fails test within the warranty period, it will be replaced at no cost. If a

Copyright Digilent, Inc. All rights reserved.
Other product and company names mentioned may be trademarks of their respective owners.

board fails test outside of the warranty period and cannot be easily repaired, Digilent can repair the board or offer a discounted replacement. Contact Digilent for more details.

Copyright Digilent, Inc. All rights reserved.
Other product and company names mentioned may be trademarks of their respective owners.

Appendix C – 7400 Series Datasheets

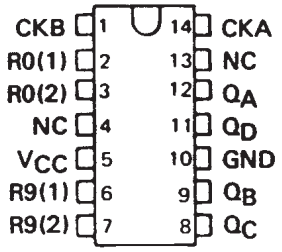
'90A, 'LS90 . . . Decade Counters

'92A, 'LS92 . . . Divide By-Twelve Counters

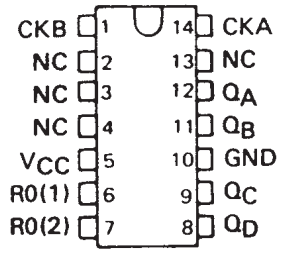
'93A, 'LS93 . . . 4-Bit Binary Counters

TYPES	TYPICAL POWER DISSIPATION
'90A	145 mW
'92A, '93A	130 mW
'LS90, 'LS92, 'LS93	45 mW

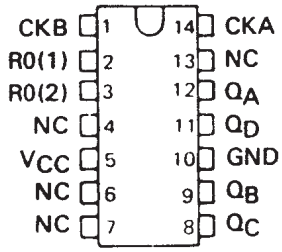
SN5490A, SN54LS90 . . . J OR W PACKAGE
SN7490A . . . N PACKAGE
SN74LS90 . . . D OR N PACKAGE
(TOP VIEW)



SN5492A, SN54LS92 . . . J OR W PACKAGE
SN7492A . . . N PACKAGE
SN74LS92 . . . D OR N PACKAGE
(TOP VIEW)



SN5493A, SN54LS93 . . . J OR W PACKAGE
SN7493 . . . N PACKAGE
SN74LS93 . . . D OR N PACKAGE
(TOP VIEW)



description

Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five for the '90A and 'LS90, divide-by-six for the '92A and 'LS92, and the divide-by-eight for the '93A and 'LS93.

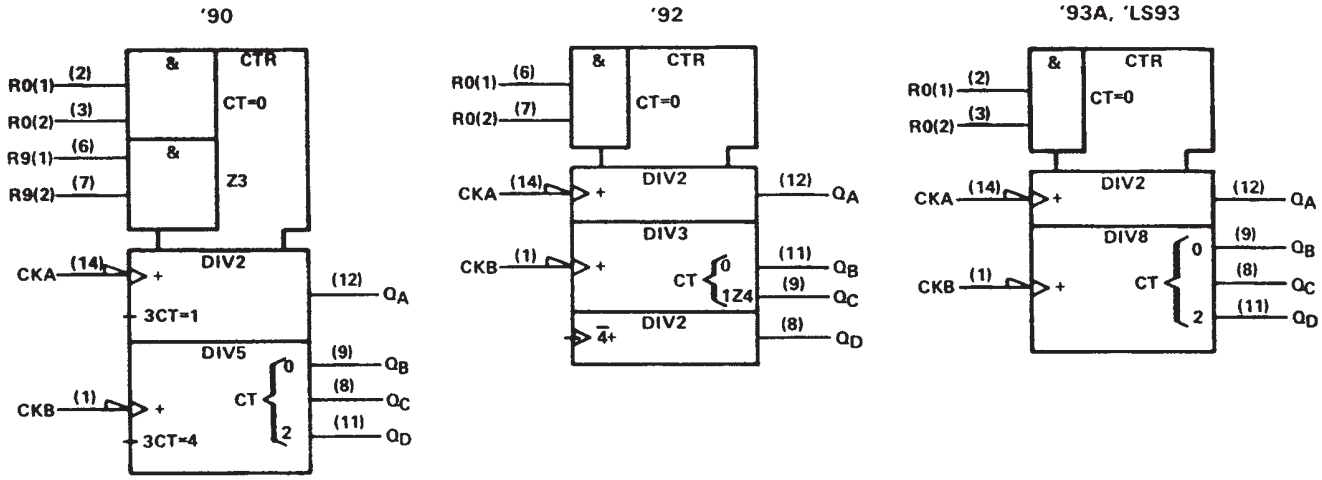
All of these counters have a gated zero reset and the '90A and 'LS90 also have gated set-to-nine inputs for use in BCD nine's complement applications.

To use their maximum count length (decade, divide-by-twelve, or four-bit binary) of these counters, the CKB input is connected to the Q_A output. The input count pulses are applied to CKA input and the outputs are as described in the appropriate function table. A symmetrical divide-by-ten count can be obtained from the '90A or 'LS90 counters by connecting the Q_D output to the CKA input and applying the input count to the CKB input which gives a divide-by-ten square wave at output Q_A.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 1988, Texas Instruments Incorporated

logic symbols†



†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

'90A, 'LS90
BCD COUNT SEQUENCE
(See Note A)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

'90A, 'LS90
BI-QUINARY (5-2)
(See Note B)

COUNT	OUTPUT			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

'92A, 'LS92
COUNT SEQUENCE
(See Note C)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	H	L	L	L
7	H	L	L	H
8	H	L	H	L
9	H	L	H	H
10	H	H	L	L
11	H	H	L	H

'90A, 'LS90
RESET/COUNT FUNCTION TABLE

RESET INPUTS				OUTPUT			
$R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

'92A, 'LS92, '93A, 'LS93
RESET/COUNT FUNCTION TABLE

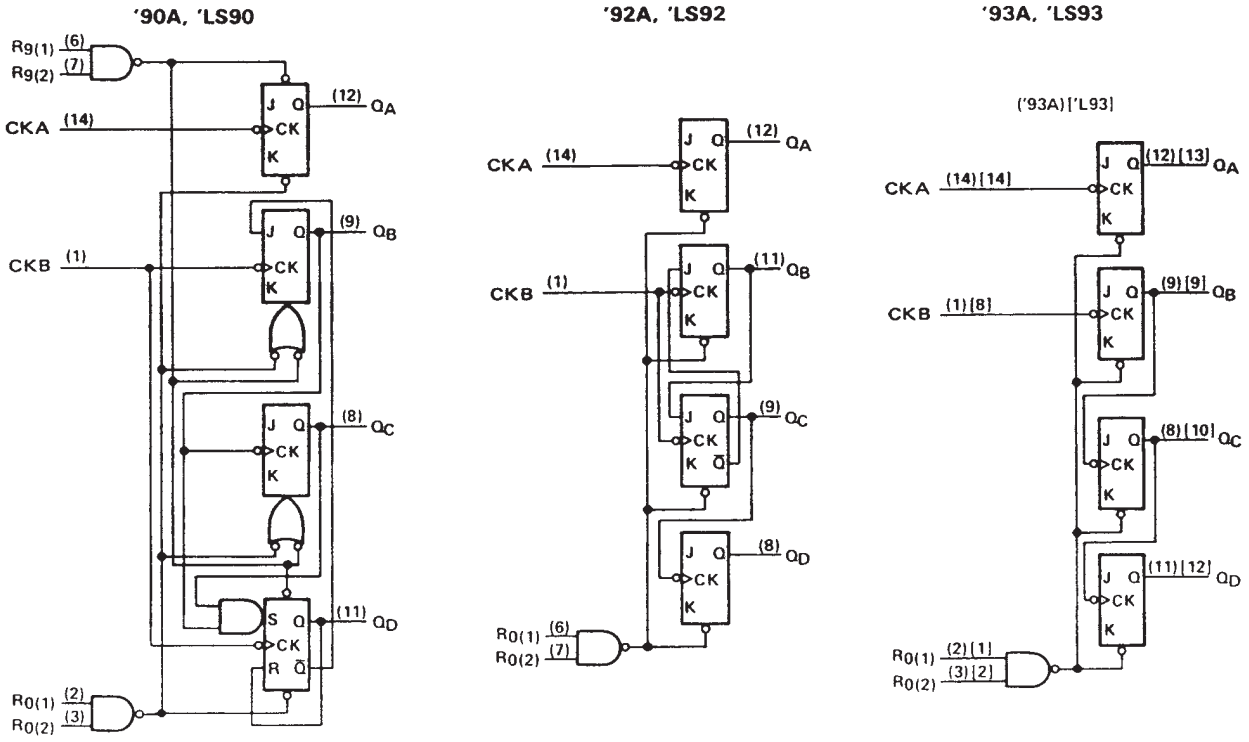
RESET INPUTS		OUTPUT			
$R_{0(1)}$	$R_{0(2)}$	Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

'93A, 'LS93
COUNT SEQUENCE
(See Note C)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

NOTES: A. Output Q_A is connected to input CKB for BCD count.
B. Output Q_D is connected to input CKA for bi-quinary count.
C. Output Q_A is connected to input CKB.
D. H = high level, L = low level, X = irrelevant

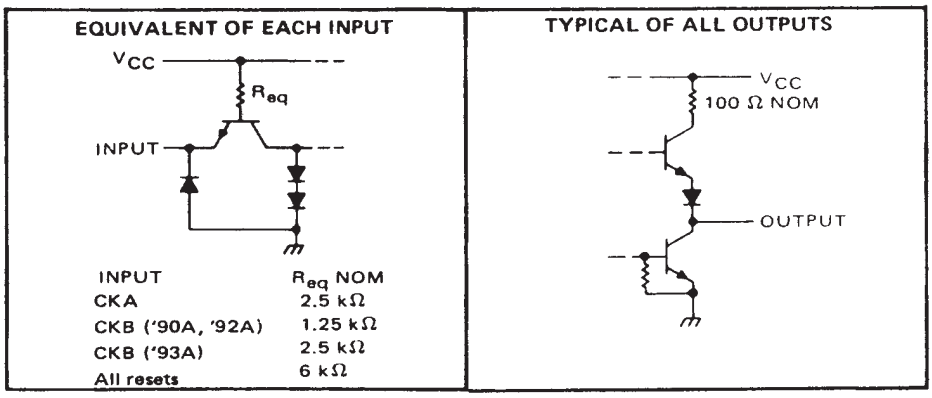
logic diagrams (positive logic)



The J and K inputs shown without connection are for reference only and are functionally at a high level.
Pin numbers shown in ( ) are for the 'LS93 and '93A and pin numbers shown in [ ] are for the 54L93.

schematics of inputs and outputs

'90A, '92A, '93A

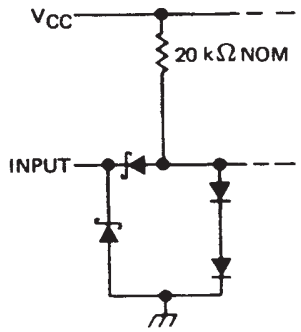


INPUT	R_{eq} NOM
CKA	2.5 kΩ
CKB ('90A, '92A)	1.25 kΩ
CKB ('93A)	2.5 kΩ
All resets	6 kΩ

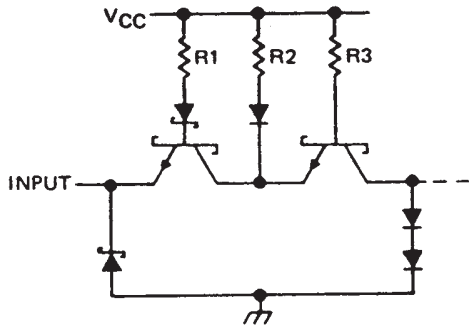
schematics of inputs and outputs (continued)

'LS90, 'LS92, 'LS93

EQUIVALENT OF EACH RESET INPUT

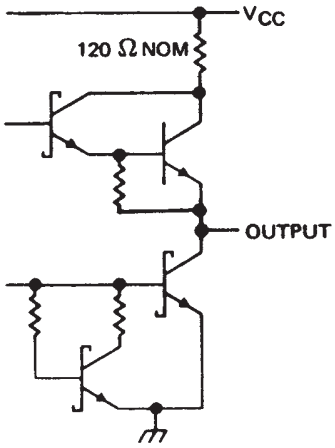


EQUIVALENT OF A AND B INPUTS



INPUT	NOMINAL VALUES R1	R2	R3
CKA	10 kΩ	10 kΩ	10 kΩ
CKB ('LS90, 'LS92)	6.7 kΩ	6.7 kΩ	5 kΩ
CKB ('LS93)	15 kΩ	15 kΩ	10 kΩ

TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN5490A, SN5492A, SN5493A . . . . . −55°C to 125°C
SN7490A, SN7492A, SN7493A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For these circuits, this rating applies between the two R_0 inputs, and for the '90A circuit, it also applies between the two R_9 inputs.

recommended operating conditions

		SN5490A, SN5492A SN5493A			SN7490A, SN7492A SN7493A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−800			−800	μA
Low-level output current, I_{OL}				16			16	mA
Count frequency, f_{count} (see Figure 1)	A input	0		32	0		32	MHz
	B input	0		16	0		16	
Pulse width, t_w	A input	15			15			ns
	B input	30			30			
	Reset inputs	15			15			
Reset inactive-state setup time, t_{su}		25			25			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER ¶			TEST CONDITIONS†		'90A MIN	'90A TYP‡	'90A MAX	'92A MIN	'92A TYP‡	'92A MAX	'93A MIN	'93A TYP‡	'93A MAX	UNIT
V_{IH}	High-level input voltage				2			2			2			V
V_{IL}	Low-level input voltage						0.8			0.8			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA				−1.5			−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA		2.4	3.4		2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA¶			0.2	0.4		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V				1			1			1	mA
I_{IH}	High-level input current	Any reset	V_{CC} = MAX, V_I = 2.4 V				40			40			40	μA
		CKA					80			80			80	
		CKB					120			120			80	
I_{IL}	Low-level input current	Any reset	V_{CC} = MAX, V_I = 0.4 V				−1.6			−1.6			−1.6	mA
		CKA					−3.2			−3.2			−3.2	
		CKB					−4.8			−4.8			−3.2	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	SN54'	−20		−57	−20		−57	−20		−57	mA
				SN74'	−18		−57	−18		−57	−18		−57	
I_{CC}	Supply current		V_{CC} = MAX, See Note 3			29	42		26	39		26	39	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.
¶ Q_A outputs are tested at I_{OL} = 16 mA plus the limit value for I_{IL} for the CKB input. This permits driving the CKB input while maintaining full fan-out capability.
NOTE 3: I_{CC} is measured with all outputs open, both R_0 inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'90A			'92A			'93A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}	CKA	Q_A	C_L = 15 pF, R_L = 400 Ω, See Figure 1	32	42		32	42		32	42		MHz
	CKB	Q_B		16			16			16			
t_{PLH}	CKA	Q_A			10	16		10	16		10	16	ns
t_{PHL}					12	18		12	18		12	18	
t_{PLH}	CKA	Q_D			32	48		32	48		46	70	ns
t_{PHL}					34	50		34	50		46	70	
t_{PLH}	CKB	Q_B			10	16		10	16		10	16	ns
t_{PHL}					14	21		14	21		14	21	
t_{PLH}	CKB	Q_C			21	32		10	16		21	32	ns
t_{PHL}					23	35		14	21		23	35	
t_{PLH}	CKB	Q_D			21	32		21	32		34	51	ns
t_{PHL}					23	35		23	35		34	51	
t_{PHL}	Set-to-0	Any			26	40		26	40		26	40	ns
t_{PLH}	Set-to-9	Q_A, Q_D			20	30							ns
t_{PHL}		Q_B, Q_C			26	40							

†f_{max} = maximum count frequency
t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)		7 V
Input voltage: R inputs		7 V
A and B inputs		5.5 V
Operating free-air temperature range:	SN54LS' Circuits	−55°C to 125°C
	SN74LS' Circuits	0°C to 70°C
Storage temperature range		−65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS90 SN54LS92 SN54LS93			SN74LS90 SN74LS92 SN74LS93			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−400			−400	μA
Low-level output current, I_{OL}				4			8	mA
Count frequency, f_{count} (see Figure 1)	A input	0		32	0		32	MHz
	B input	0		16	0		16	
Pulse width, t_w	A input	15			15			ns
	B input	30			30			
	Reset inputs	30			30			
Reset inactive-state setup time, t_{su}		25			25			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†			SN54LS90 SN54LS92			SN74LS90 SN74LS92			UNIT
						MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage					2			2			V
V_{IL}	Low-level input voltage							0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = V_{ILmax},	V_{IH} = 2 V, I_{OH} = −400 μA		2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V,	I_{OL} = 4 mA¶		0.25	0.4		0.25	0.4	V
					I_{OL} = 8 mA¶					0.35	0.5	
I_I	Input current at maximum input voltage	Any reset	V_{CC} = MAX,	V_I = 7 V				0.1			0.1	mA
		CKA	V_{CC} = MAX,	V_I = 5.5 V				0.2			0.2	
		CKB						0.4			0.4	
I_{IH}	High-level input current	Any reset	V_{CC} = MAX,	V_I = 2.7 V				20			20	μA
		CKA						40			40	
		CKB						80			80	
I_{IL}	Low-level input current	Any reset	V_{CC} = MAX,	V_I = 0.4 V				−0.4			−0.4	mA
		CKA						−2.4			−2.4	
		CKB						−3.2			−3.2	
I_{OS}	Short-circuit output current§		V_{CC} = MAX			−20		−100	−20		−100	mA
I_{CC}	Supply current		V_{CC} = MAX,	See Note 3	'LS90		9	15		9	15	mA
					'LS92		9	15		9	15	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
¶Q_A outputs are tested at specified I_{OL} plus the limit value of I_{IL} for the CKB input. This permits driving the CKB input while maintaining full fan-out capability.

NOTE 3: I_{CC} is measured with all outputs open, both R_O inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†			SN54LS93 MIN	SN54LS93 TYP‡	SN54LS93 MAX	SN74LS93 MIN	SN74LS93 TYP‡	SN74LS93 MAX	UNIT
V_{IH}	High-level input voltage					2			2			V
V_{IL}	Low-level input voltage							0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = –18 mA				–1.5			–1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, I_{OH} = –400 μA		2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = V_{IL} max	V_{IH} = 2 V,	I_{OL} = 4 mA¶		0.25	0.4		0.25	0.4	V
					I_{OL} = 8 mA¶					0.35	0.5	
I_I	Input current at maximum input voltage	Any reset	V_{CC} = MAX,	V_I = 7 V				0.1			0.1	mA
		CKA or CKB	V_{CC} = MAX,	V_I = 5.5 V				0.2			0.2	
I_{IH}	High-level input current	Any reset	V_{CC} = MAX,	V_I = 2.7 V				20			20	μA
		CKA or CKB						40			80	
I_{IL}	Low-level input current	Any reset	V_{CC} = MAX,	V_I = 0.4 V				–0.4			–0.4	mA
		CKA						–2.4			–2.4	
		CKB						–1.6			–1.6	
I_{OS}	Short-circuit output current§		V_{CC} = MAX			–20		–100	–20		–100	mA
I_{CC}	Supply current		V_{CC} = MAX,	See Note 3			9	15		9	15	mA

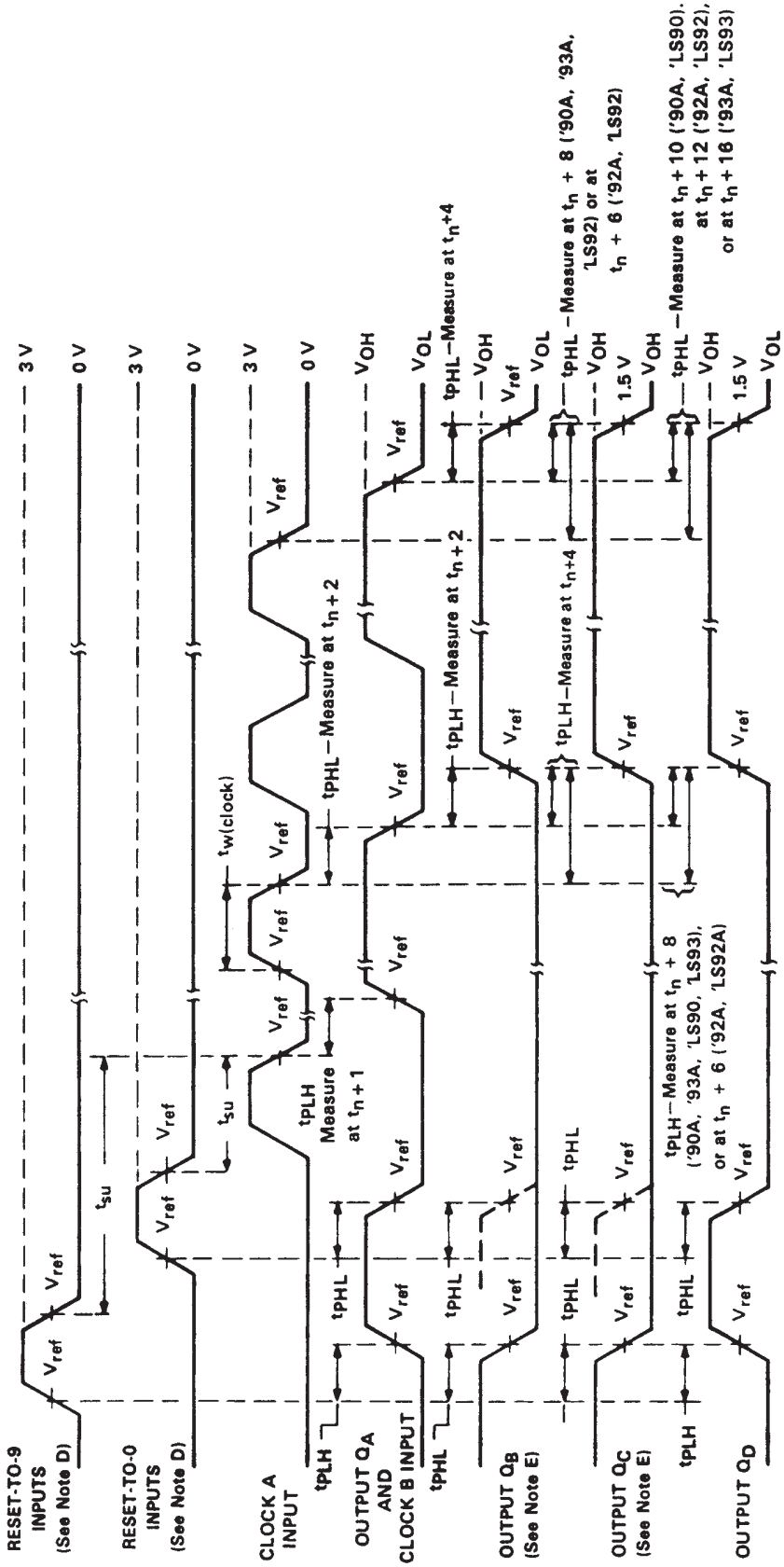
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
¶Q_A outputs are tested at specified I_{OL} plus the limit value for I_{IL} for the CKB input. This permits driving the CKB input while maintaining full fan-out capability.
NOTE 3: I_{CC} is measured with all outputs open, both R_0 inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER#	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS90 MIN	'LS90 TYP	'LS90 MAX	'LS92 MIN	'LS92 TYP	'LS92 MAX	'LS93 MIN	'LS93 TYP	'LS93 MAX	UNIT
f_{max}	CKA	Q_A	C_L = 15 pF, R_L = 2 kΩ, See Figure 1	32	42		32	42		32	42		MHz
	CKB	Q_B		16			16			16			
t_{PLH}	CKA	Q_A			10	16		10	16		10	16	ns
t_{PHL}					12	18		12	18		12	18	
t_{PLH}	CKA	Q_D			32	48		32	48		46	70	ns
t_{PHL}					34	50		34	50		46	70	
t_{PLH}	CKB	Q_B			10	16		10	16		10	16	ns
t_{PHL}					14	21		14	21		14	21	
t_{PLH}	CKB	Q_C			21	32		10	16		21	32	ns
t_{PHL}					23	35		14	21		23	35	
t_{PLH}	CKB	Q_D			21	32		21	32		34	51	ns
t_{PHL}					23	35		23	35		34	51	
t_{PHL}	Set-to-0	Any			26	40		26	40		26	40	ns
t_{PLH}	Set-to-9	Q_A, Q_D			20	30							ns
t_{PHL}		Q_B, Q_C			26	40							

#f_{max} = maximum count frequency
t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output

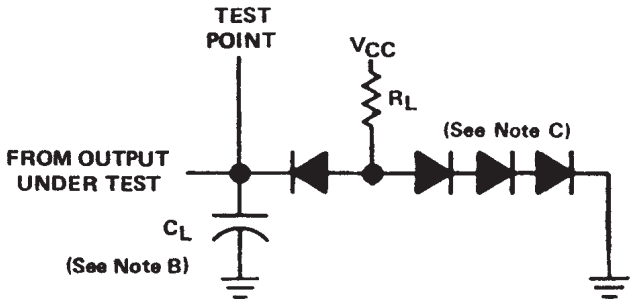
PARAMETER MEASUREMENT INFORMATION



NOTES: A. Input pulses are supplied by a generator having the following characteristics:
for '90A, '92A, '93A, $t_r \le 5$ ns, $t_f \le 5$ ns, PRR = 1 MHz, duty cycle = 50%, $Z_{out} \approx 50$ ohms;
for 'LS90, 'LS92, 'LS93, $t_r \le 15$ ns, $t_f \le 5$ ns, PRR = 1 MHz, duty cycle = 50%, $Z_{out} \approx 50$ ohms.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or equivalent.
D. Each reset input is tested separately with the other reset at 4.5 V.
E. Reference waveforms are shown with dashed lines.
F. For '90A, '92A, and '93A; V_{ref} = 1.5 V. For 'LS90, 'LS92, and 'LS93; V_{ref} = 1.3 V.

FIGURE 1A

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

NOTES: A. Input pulses are supplied by a generator having the following characteristics:
for '90A, '92A, '93A, $t_r \leq 5$ ns, $t_f \leq 5$ ns, PRR = 1 MHz, duty cycle = 50%, $Z_{out} \approx 50$ ohms;
for 'LS90, 'LS92, 'LS93, $t_r \leq 15$ ns, $t_f \leq 5$ ns, PRR = 1 MHz, duty cycle = 50%, $Z_{out} \approx 50$ ohms.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or equivalent.
D. Each reset input is tested separately with the other reset at 4.5 V.
E. Reference waveforms are shown with dashed lines.
F. For '90A, '92A, and '93A; V_{ref} = 1.5 V. For 'LS90, 'LS92, and 'LS93; V_{ref} = 1.3 V.

FIGURE 1B

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
7603201CA	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
7603201DA	ACTIVE	CFP	W	14	1	None	Call TI	Level-NC-NC-NC
7700101CA	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
7700101DA	ACTIVE	CFP	W	14	1	None	Call TI	Level-NC-NC-NC
JM38510/31501BCA	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
JM38510/31501BDA	ACTIVE	CFP	W	14	1	None	Call TI	Level-NC-NC-NC
JM38510/31502BCA	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
JM38510/31502BDA	ACTIVE	CFP	W	14	1	None	Call TI	Level-NC-NC-NC
SN5490AJ	LIFEBUY	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
SN5492AJ	OBSOLETE	CDIP	J	14		None	Call TI	Call TI
SN54LS90J	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
SN54LS93J	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
SN7490AN	OBSOLETE	PDIP	N	14		None	Call TI	Call TI
SN7492AN	OBSOLETE	PDIP	N	14		None	Call TI	Call TI
SN7493AN	OBSOLETE	PDIP	N	14		None	Call TI	Call TI
SN74LS90D	ACTIVE	SOIC	D	14	50	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74LS90DR	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74LS90N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS92D	ACTIVE	SOIC	D	14	50	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74LS92DR	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74LS92N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS92N3	OBSOLETE	PDIP	N	14		None	Call TI	Call TI
SN74LS92NSR	ACTIVE	SO	NS	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74LS93D	ACTIVE	SOIC	D	14	50	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74LS93DR	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74LS93N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS93N3	OBSOLETE	PDIP	N	14		None	Call TI	Call TI
SN74LS93NSR	ACTIVE	SO	NS	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SNJ5490AJ	LIFEBUY	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
SNJ5490AW	LIFEBUY	CFP	W	14	1	None	Call TI	Level-NC-NC-NC
SNJ5492AJ	OBSOLETE	CDIP	J	14		None	Call TI	Call TI
SNJ5492AW	OBSOLETE	CFP	W	14		None	Call TI	Call TI
SNJ54LS90J	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
SNJ54LS90W	ACTIVE	CFP	W	14	1	None	Call TI	Level-NC-NC-NC

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
SNJ54LS93J	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
SNJ54LS93W	ACTIVE	CFP	W	14	1	None	Call TI	Level-NC-NC-NC

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
None: Not yet available Lead (Pb-Free).
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

Copyright © 2005, Texas Instruments Incorporated

This datasheet has been download from:

www.datasheetcatalog.com

Datasheets for electronics components.

SN74LS47

BCD to 7-Segment Decoder/Driver

The SN74LS47 are Low Power Schottky BCD to 7-Segment Decoder/Drivers consisting of NAND gates, input buffers and seven AND-OR-INVERT gates. They offer active LOW, high sink current outputs for driving indicators directly. Seven NAND gates and one driver are connected in pairs to make BCD data and its complement available to the seven decoding AND-OR-INVERT gates. The remaining NAND gate and three input buffers provide lamp test, blanking input/ripple-blanking output and ripple-blanking input.

The circuits accept 4-bit binary-coded-decimal (BCD) and, depending on the state of the auxiliary inputs, decodes this data to drive a 7-segment display indicator. The relative positive-logic output levels, as well as conditions required at the auxiliary inputs, are shown in the truth tables. Output configurations of the SN74LS47 are designed to withstand the relatively high voltages required for 7-segment indicators.

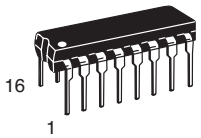
These outputs will withstand 15 V with a maximum reverse current of 250 μA. Indicator segments requiring up to 24 mA of current may be driven directly from the SN74LS47 high performance output transistors. Display patterns for BCD input counts above nine are unique symbols to authenticate input conditions.

The SN74LS47 incorporates automatic leading and/or trailing-edge zero-blanking control (RBI and RBO). Lamp test (LT) may be performed at any time which the BI/RBO node is a HIGH level. This device also contains an overriding blanking input (BI) which can be used to control the lamp intensity by varying the frequency and duty cycle of the BI input signal or to inhibit the outputs.

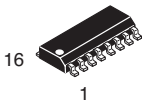
- Lamp Intensity Modulation Capability (BI/RBO)
- Open Collector Outputs
- Lamp Test Provision
- Leading/Trailing Zero Suppression
- Input Clamp Diodes Limit High-Speed Termination Effects

ON Semiconductor
Formerly a Division of Motorola
http://onsemi.com

LOW POWER SCHOTTKY



PLASTIC N SUFFIX CASE 648



SOIC D SUFFIX CASE 751B

GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
T_A	Operating Ambient Temperature Range	0	25	70	°C
I_{OH}	Output Current – High $\overline{BI/RBO}$			–50	μA
I_{OL}	Output Current – Low $\overline{BI/RBO}$ $\overline{BI/RBO}$			3.2	mA
$V_{O(off)}$	Off–State Output Voltage a to g			15	V
$I_{O(on)}$	On–State Output Current a to g			24	mA

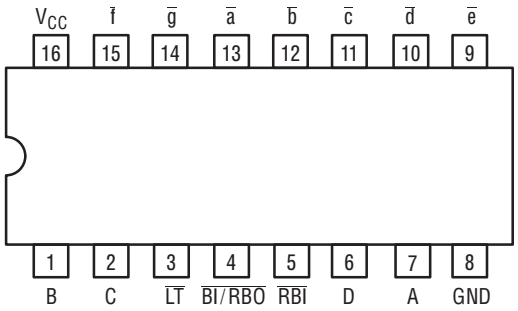
ORDERING INFORMATION

Device	Package	Shipping
SN74LS47N	16 Pin DIP	2000 Units/Box
SN74LS47D	16 Pin	2500/Tape & Reel

© Semiconductor Components Industries, LLC, 1999

December, 1999 – Rev. 6
Publication Order Number:
SN74LS47/D

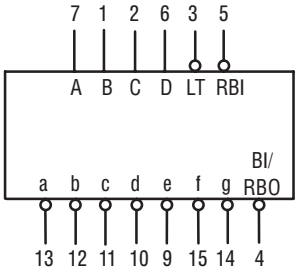
CONNECTION DIAGRAM DIP (TOP VIEW)



PIN NAMES		**LOADING** (Note a) HIGH	LOW
A, B, C, D	BCD Inputs	0.5 U.L.	0.25 U.L.
$\overline{RBI}$	Ripple–Blanking Input	0.5 U.L.	0.25 U.L.
$\overline{LT}$	Lamp–Test Input	0.5 U.L.	0.25 U.L.
$\overline{BI}/\overline{RBO}$	Blanking Input or	0.5 U.L.	0.75 U.L.
	Ripple–Blanking Output	1.2 U.L.	2.0 U.L.
$\overline{a}$, to $\overline{g}$	Outputs	Open–Collector	15 U.L.

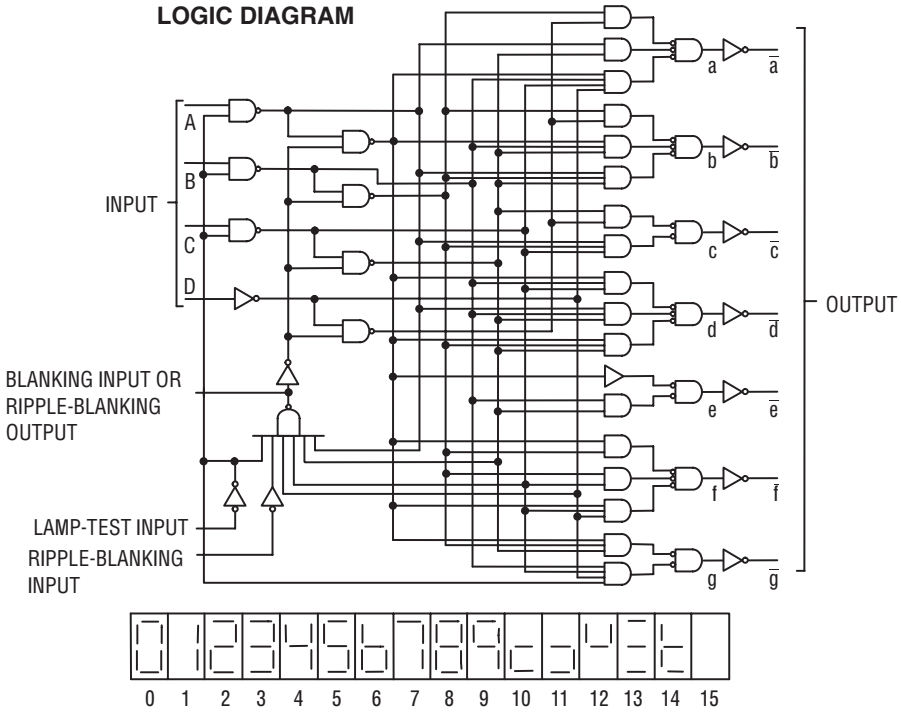
NOTES:
a) 1 Unit Load (U.L.) = 40 μA HIGH, 1.6 mA LOW.
b) Output current measured at V_{OUT} = 0.5 V
The Output LOW drive factor is 15 U.L. for Commercial (74) Temperature Ranges.

LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

LOGIC DIAGRAM



NUMERICAL DESIGNATIONS — RESULTANT DISPLAYS

TRUTH TABLE

	INPUTS							OUTPUTS							
DECIMAL OR FUNCTION	$\overline{LT}$	$\overline{RBI}$	D	C	B	A	$\overline{BI/RBO}$	$\overline{a}$	$\overline{b}$	$\overline{c}$	$\overline{d}$	$\overline{e}$	$\overline{f}$	$\overline{g}$	NOTE
0	H	H	L	L	L	L	H	L	L	L	L	L	L	H	A
1	H	X	L	L	L	H	H	H	L	L	H	H	H	H	A
2	H	X	L	L	H	L	H	L	L	H	L	L	H	L	
3	H	X	L	L	H	H	H	L	L	L	L	H	H	L	
4	H	X	L	H	L	L	H	H	L	L	H	H	L	L	
5	H	X	L	H	L	H	H	L	H	L	L	H	L	L	
6	H	X	L	H	H	L	H	H	H	L	L	L	L	L	
7	H	X	L	H	H	H	H	L	L	L	H	H	H	H	
8	H	X	H	L	L	L	H	L	L	L	L	L	L	L	
9	H	X	H	L	L	H	H	L	L	L	H	H	L	L	
10	H	X	H	L	H	L	H	H	H	H	L	L	H	L	
11	H	X	H	L	H	H	H	H	H	L	L	H	H	L	
12	H	X	H	H	L	L	H	H	L	H	H	H	L	L	
13	H	X	H	H	L	H	H	L	H	H	L	H	L	L	
14	H	X	H	H	H	L	H	H	H	H	L	L	L	L	
15	H	X	H	H	H	H	H	H	H	H	H	H	H	H	
$\overline{BI}$	X	X	X	X	X	X	L	H	H	H	H	H	H	H	B
$\overline{RBI}$	H	L	L	L	L	L	L	H	H	H	H	H	H	H	C
$\overline{LT}$	L	X	X	X	X	X	H	L	L	L	L	L	L	L	D

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

NOTES:

(A) $\overline{BI}/\overline{RBO}$ is wire-AND logic serving as blanking Input (BI) and/or ripple-blanking output ($\overline{RBO}$). The blanking out (BI) must be open or held at a HIGH level when output functions 0 through 15 are desired, and ripple-blanking input ($\overline{RBI}$) must be open or at a HIGH level if blanking of a decimal 0 is not desired. X = input may be HIGH or LOW.

(B) When a LOW level is applied to the blanking input (forced condition) all segment outputs go to a LOW level regardless of the state of any other input condition.

(C) When ripple-blanking input ($\overline{RBI}$) and inputs A, B, C, and D are at LOW level, with the lamp test input at HIGH level, all segment outputs go to a HIGH level and the ripple-blanking output (RBO) goes to a LOW level (response condition).

(D) When the blanking input/ripple-blanking output ($\overline{BI}/\overline{RBO}$) is open or held at a HIGH level, and a LOW level is applied to lamp test input, all segment outputs go to a LOW level.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Theshold Voltage for All Inputs	
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Threshold Voltage for All Inputs	
V_{IK}	Input Clamp Diode Voltage		−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage, $\overline{BI/RBO}$	2.4	4.2		V	V_{CC} = MIN, I_{OH} = −50 μA, V_{IN} = V_{IN} or V_{IL} per Truth Table	
V_{OL}	Output LOW Voltage $\overline{BI/RBO}$		0.25	0.4	V	I_{OL} = 1.6 mA	V_{CC} = MIN, V_{IN} = V_{IN} or V_{IL} per Truth Table
			0.35	0.5	V	I_{OL} = 3.2 mA	
$I_{O\ (off)}$	Off-State Output Current $\overline{a}$ thru $\overline{g}$			250	μA	V_{CC} = MAX, V_{IN} = V_{IN} or V_{IL} per Truth Table, $V_{O\ (off)}$ = 15 V	
$V_{O\ (on)}$	On-State Output Voltage $\overline{a}$ thru $\overline{g}$		0.25	0.4	V	$I_{O\ (on)}$ = 12 mA	V_{CC} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table
			0.35	0.5	V	$I_{O\ (on)}$ = 24 mA	
I_{IH}	Input HIGH Current			20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
				0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current $\overline{BI/RBO}$ Any Input except $\overline{BI/RBO}$			−1.2 −0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS} $\overline{BI/RBO}$	Output Short Circuit Current (Note 1)	−0.3		−2.0	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current		7.0	13	mA	V_{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
t_{PHL} t_{PLH}	Propagation Delay, Address Input to Segment Output			100 100	ns ns	V_{CC} = 5.0 V C_L = 15 pF
t_{PHL} t_{PLH}	Propagation Delay, $\overline{RBI}$ Input To Segment Output			100 100	ns ns	

AC WAVEFORMS

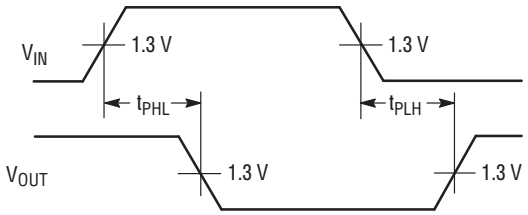


Figure 1.

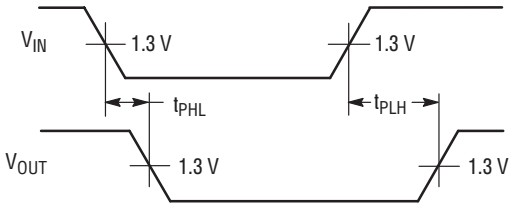
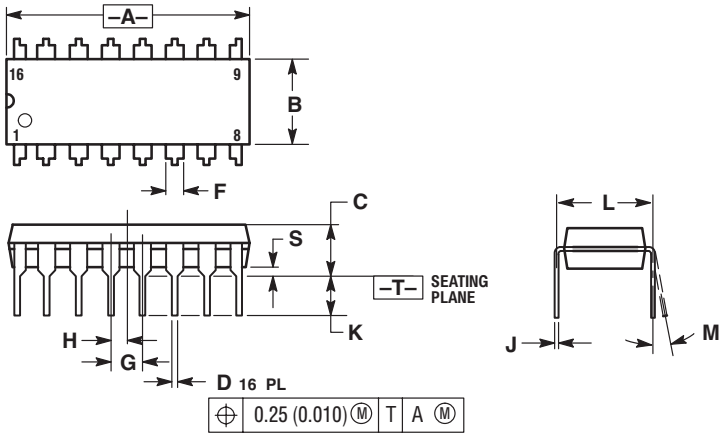


Figure 2.

PACKAGE DIMENSIONS

N SUFFIX
PLASTIC PACKAGE
CASE 648–08
ISSUE R

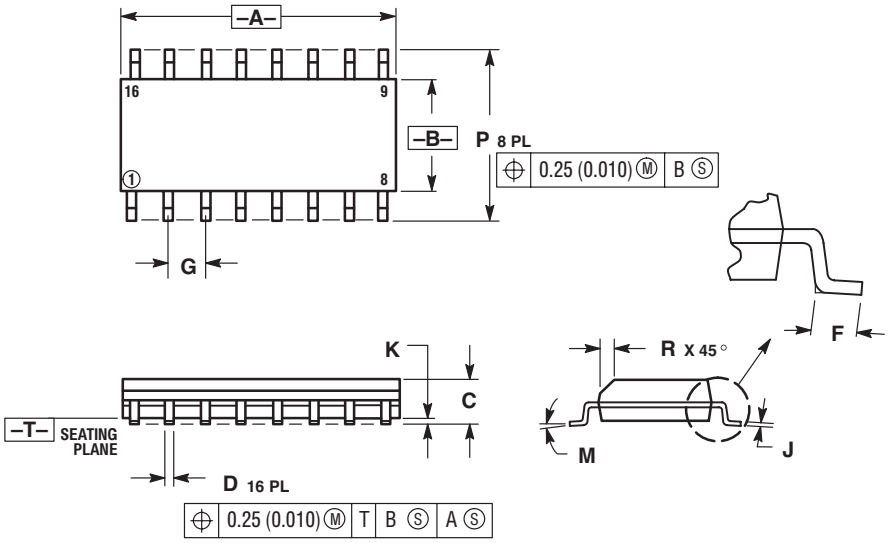


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

PACKAGE DIMENSIONS

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B–05
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

Notes

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer.

PUBLICATION ORDERING INFORMATION

North America Literature Fulfillment:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303–675–2175 or 800–344–3860 Toll Free USA/Canada
Fax: 303–675–2176 or 800–344–3867 Toll Free USA/Canada
Email: ONlit@hibbertco.com

N. American Technical Support: 800–282–9855 Toll Free USA/Canada

EUROPE: LDC for ON Semiconductor – European Support
German **Phone:** (+1) 303–308–7140 (M–F 2:30pm to 5:00pm Munich Time)
Email: ONlit–german@hibbertco.com
French **Phone:** (+1) 303–308–7141 (M–F 2:30pm to 5:00pm Toulouse Time)
Email: ONlit–french@hibbertco.com
English **Phone:** (+1) 303–308–7142 (M–F 1:30pm to 5:00pm UK Time)
Email: ONlit@hibbertco.com

ASIA/PACIFIC: LDC for ON Semiconductor – Asia Support
Phone: 303–675–2121 (Tue–Fri 9:00am to 1:00pm, Hong Kong Time)
Toll Free from Hong Kong 800–4422–3781
Email: ONlit–asia@hibbertco.com

JAPAN: ON Semiconductor, Japan Customer Focus Center
4–32–1 Nishi–Gotanda, Shinagawa–ku, Tokyo, Japan 141–8549
Phone: 81–3–5487–8345
Email: r14153@onsemi.com

Fax Response Line: 303–675–2167
800–344–3810 Toll Free USA/Canada

ON Semiconductor Website: http://onsemi.com

For additional information, please contact your local
Sales Representative.

This datasheet has been downloaded from:

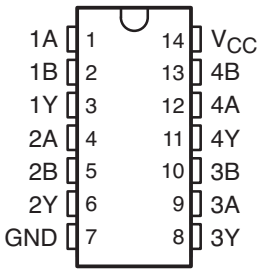
www.DatasheetCatalog.com

Datasheets for electronic components.

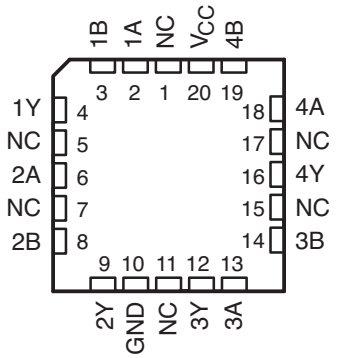
SCLS100E – DECEMBER 1982 – REVISED AUGUST 2003

- **Wide Operating Voltage Range of 2 V to 6 V**
- **Outputs Can Drive Up To 10 LSTTL Loads**
- **Low Power Consumption, 20-μA Max I_{CC}**
- **Typical t_{pd} = 10 ns**
- **±4-mA Output Drive at 5 V**
- **Low Input Current of 1 μA Max**
- **True Logic**

SN54HC86 . . . J OR W PACKAGE
SN74HC86 . . . D, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54HC86 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

These devices contain four independent 2-input exclusive-OR gates. They perform the Boolean function $Y = A \oplus B$ or $Y = \overline{A}B + A\overline{B}$ in positive logic.

A common application is as a true/complement element. If one of the inputs is low, the other input is reproduced in true form at the output. If one of the inputs is high, the signal on the other input is reproduced inverted at the output.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – N	Tube of 25	SN74HC86N	SN74HC86N
	SOIC – D	Tube of 50	SN74HC86D	HC86
		Reel of 2500	SN74HC86DR	
		Reel of 250	SN74HC86DT	
	SOP – NS	Reel of 2000	SN74HC86NSR	HC86
	TSSOP – PW	Tube of 90	SN74HC86PW	HC86
		Reel of 2000	SN74HC86PWR	
		Reel of 250	SN74HC86PWT	
–55°C to 125°C	CDIP – J	Tube of 25	SNJ54HC86J	SNJ54HC86J
	CFP – W	Tube of 150	SNJ54HC86W	SNJ54HC86W
	LCCC – FK	Tube of 55	SNJ54HC86FK	SNJ54HC86FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2003, Texas Instruments Incorporated

On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

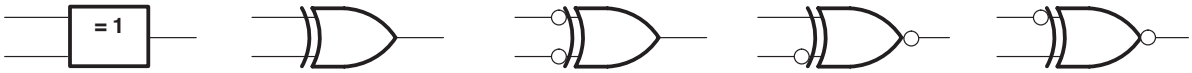
FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

exclusive-OR logic

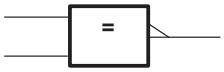
An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.

Exclusive OR



These are five equivalent exclusive-OR symbols valid for an ’HC86 gate in positive logic; negation may be shown at any two ports.

Logic Identity Element

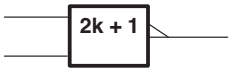


The output is active (low) if all inputs stand at the same logic level (i.e., A = B).

Even-Parity Element

The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.

Odd-Parity Element



The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) . . . . . ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND . . . . . ±50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package . . . . . 86°C/W
N package . . . . . 80°C/W
NS package . . . . . 76°C/W
PW package . . . . . 113°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			SN54HC86			SN74HC86			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V			0.5			0.5	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 6 V			1.8			1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise/fall time	V_{CC} = 2 V			1000			1000	ns
		V_{CC} = 4.5 V			500			500	
		V_{CC} = 6 V			400			400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC86		SN74HC86		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –4 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –5.2 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	$V_I = V_{IH}$ or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	$V_I = V_{CC}$ or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	$V_I = V_{CC}$ or 0,	I_O = 0	6 V			2		40		20	μA
C_i			2 V to 6 V		3	10		10		10	pF

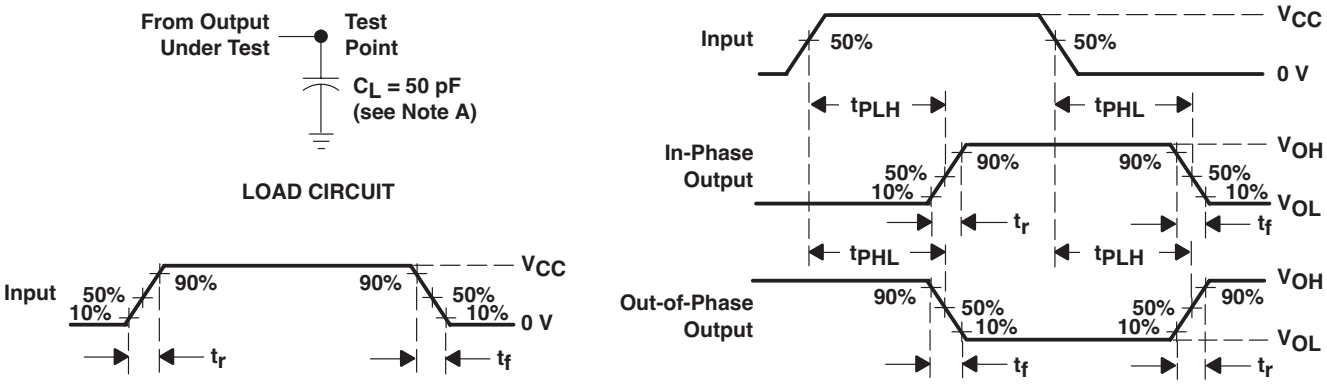
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC86		SN74HC86		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	2 V		40	100		150		125	ns
			4.5 V		12	20		30		25	
			6 V		10	17		25		21	
t_t		Y	2 V		28	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	No load	35	pF

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. The outputs are measured one at a time with one input transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
Low Power Wireless	www.ti.com/lpw	Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2007, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
5962-8404601VCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type
5962-8404601VDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
84046012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
8404601CA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type
8404601DA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
JM38510/65202BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type
SN54HC86J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type
SN74HC86D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC86DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC86DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC86DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC86DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC86DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC86DT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC86DTE4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC86DTG4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC86N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74HC86NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74HC86NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC86NSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC86NSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC86PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC86PWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC86PWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC86PWLE	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI
SN74HC86PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC86PWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC86PWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
SN74HC86PWT	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC86PWTE4	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC86PWTG4	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SNJ54HC86FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54HC86J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type
SNJ54HC86W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

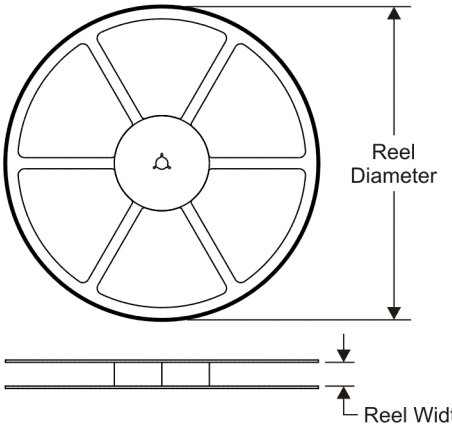
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54HC86, SN54HC86-SP, SN74HC86 :
- Automotive: SN74HC86-Q1

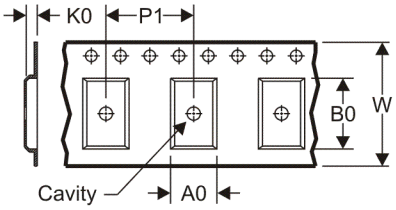
NOTE: Qualified Version Definitions:
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

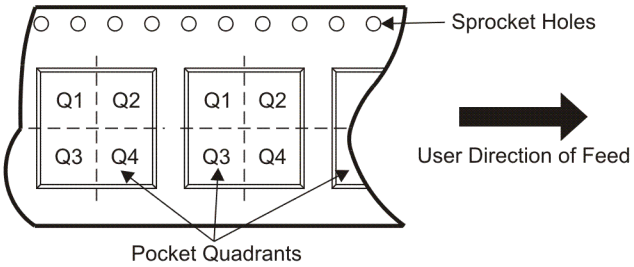


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

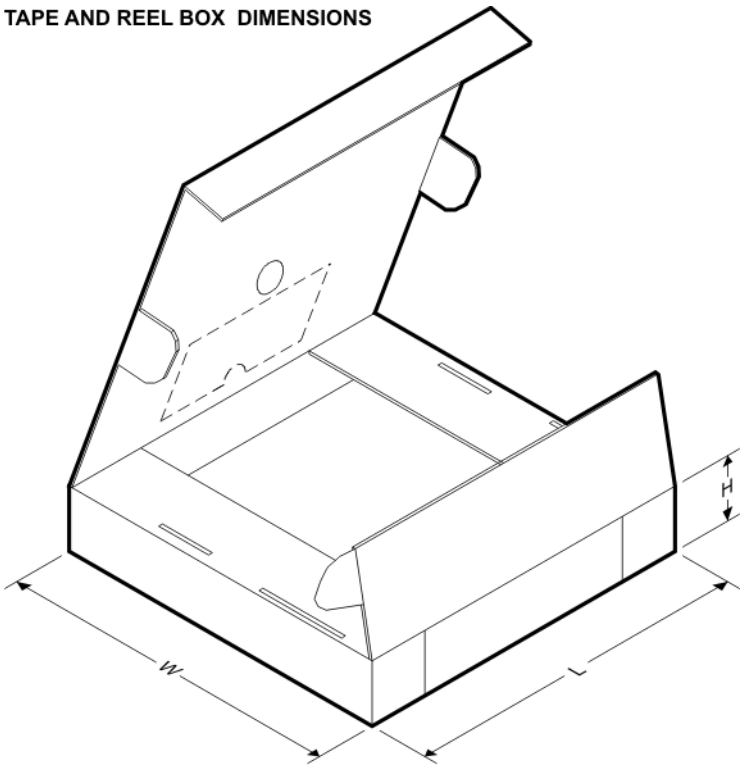
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC86DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC86DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC86NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74HC86PWR	TSSOP	PW	14	2000	330.0	12.4	7.0	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

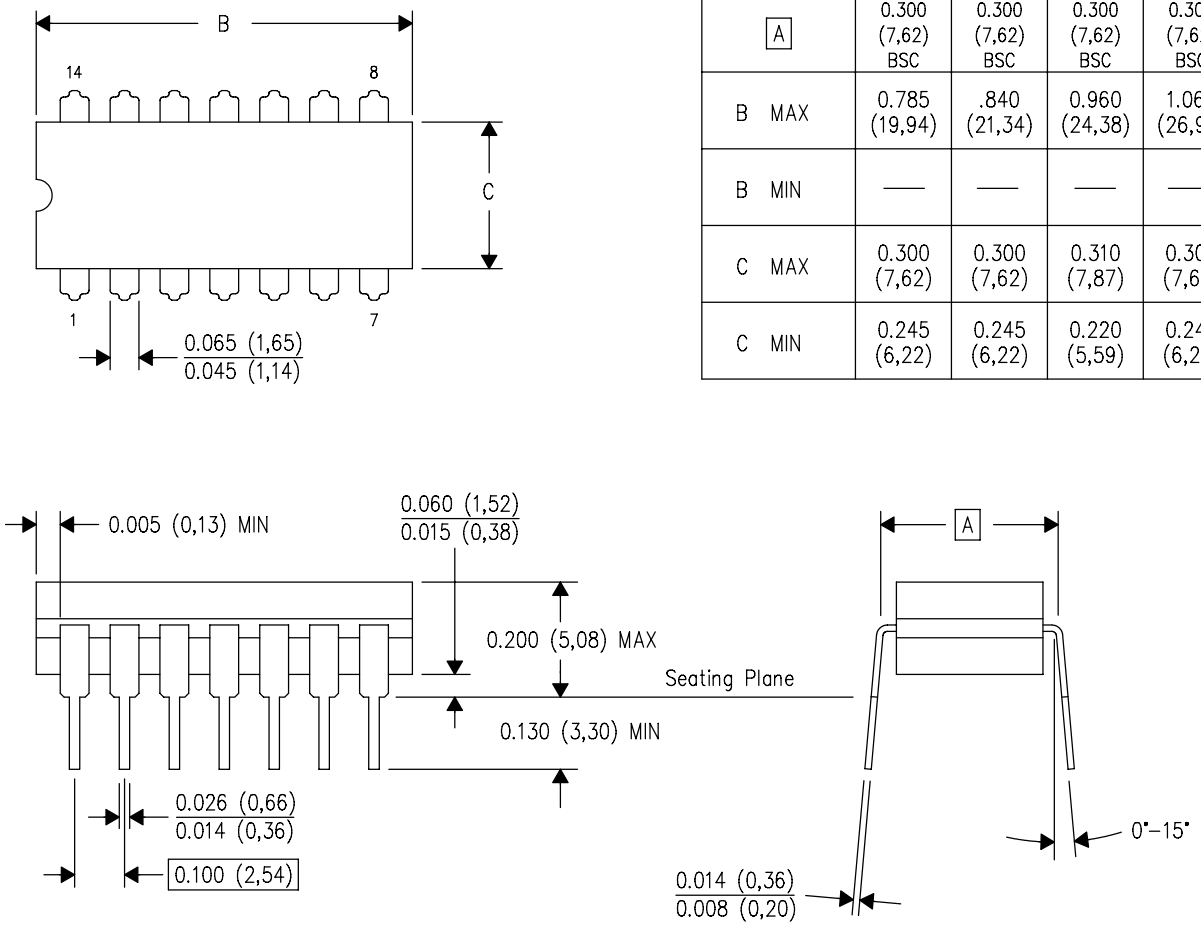


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC86DR	SOIC	D	14	2500	346.0	346.0	33.0
SN74HC86DR	SOIC	D	14	2500	333.2	345.9	28.6
SN74HC86NSR	SO	NS	14	2000	346.0	346.0	33.0
SN74HC86PWR	TSSOP	PW	14	2000	346.0	346.0	29.0

J (R–GDIP–T**) CERAMIC DUAL IN–LINE PACKAGE

14 LEADS SHOWN



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

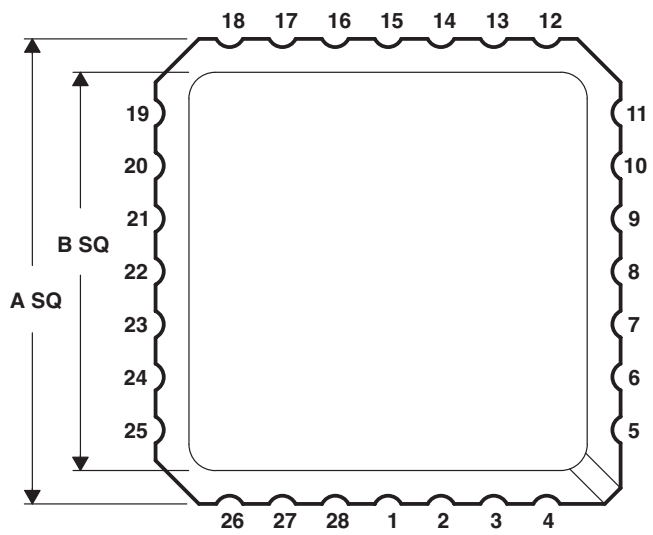
4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

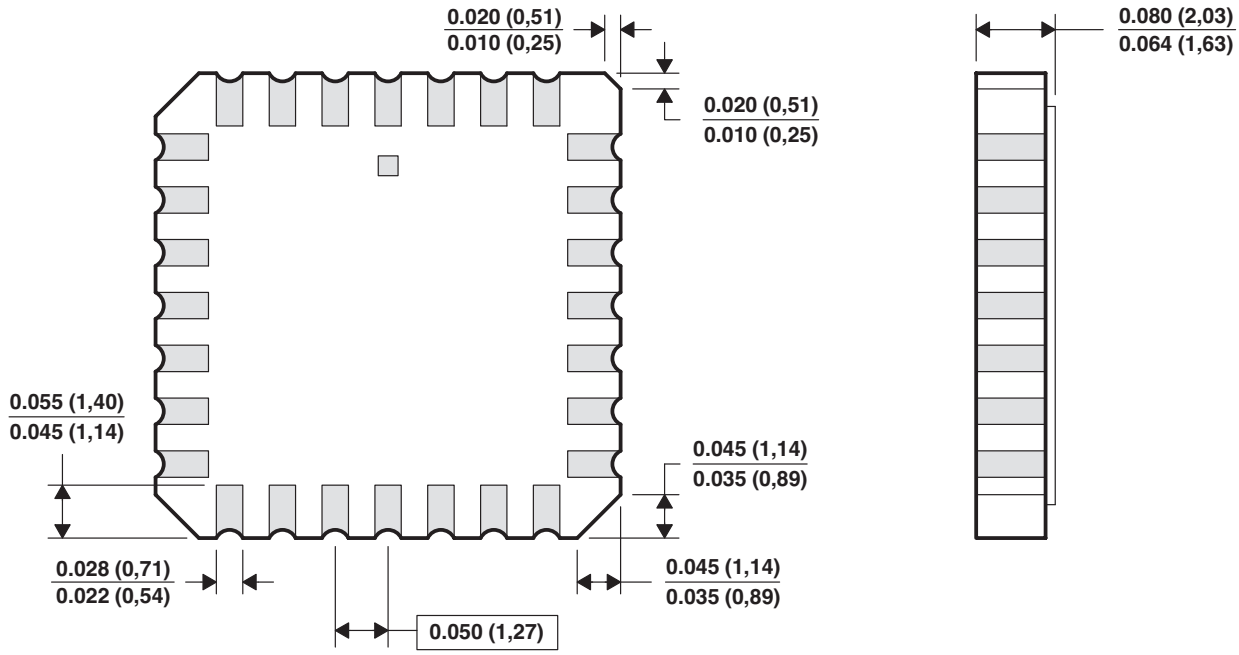
FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

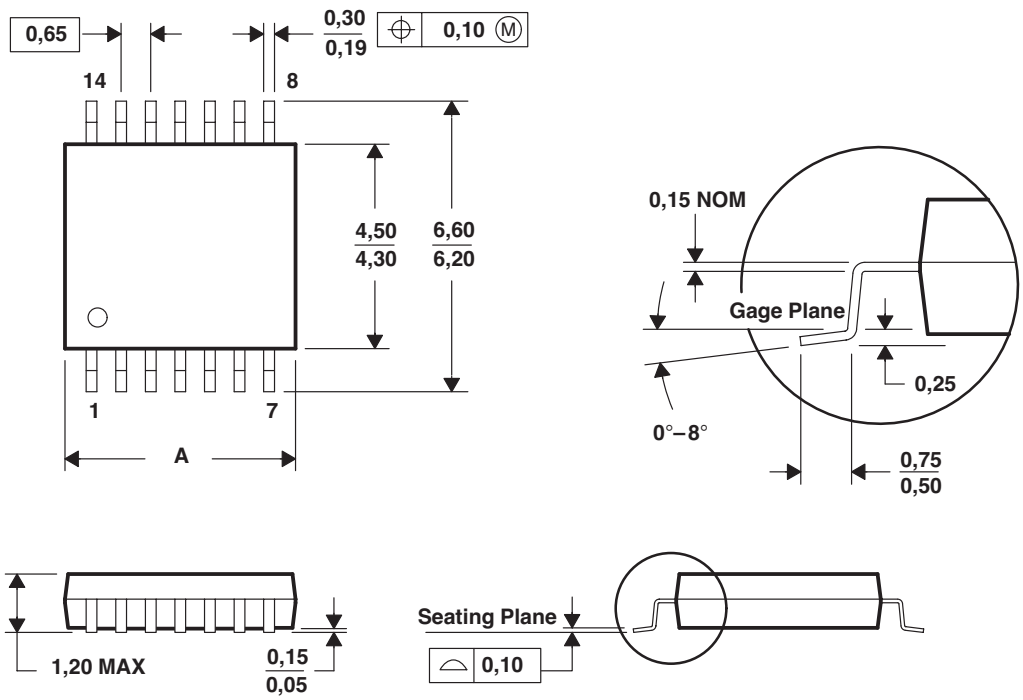


4040140/D 10/96

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MS-004

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

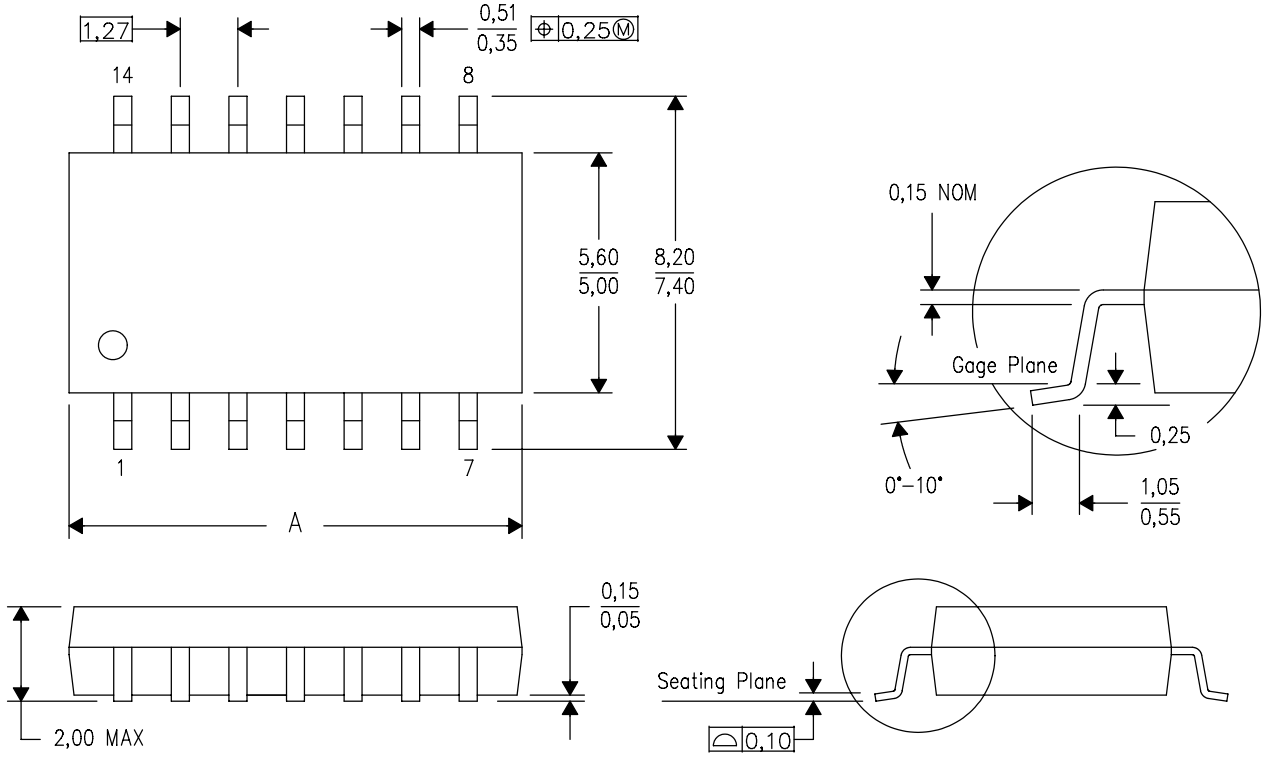
4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN

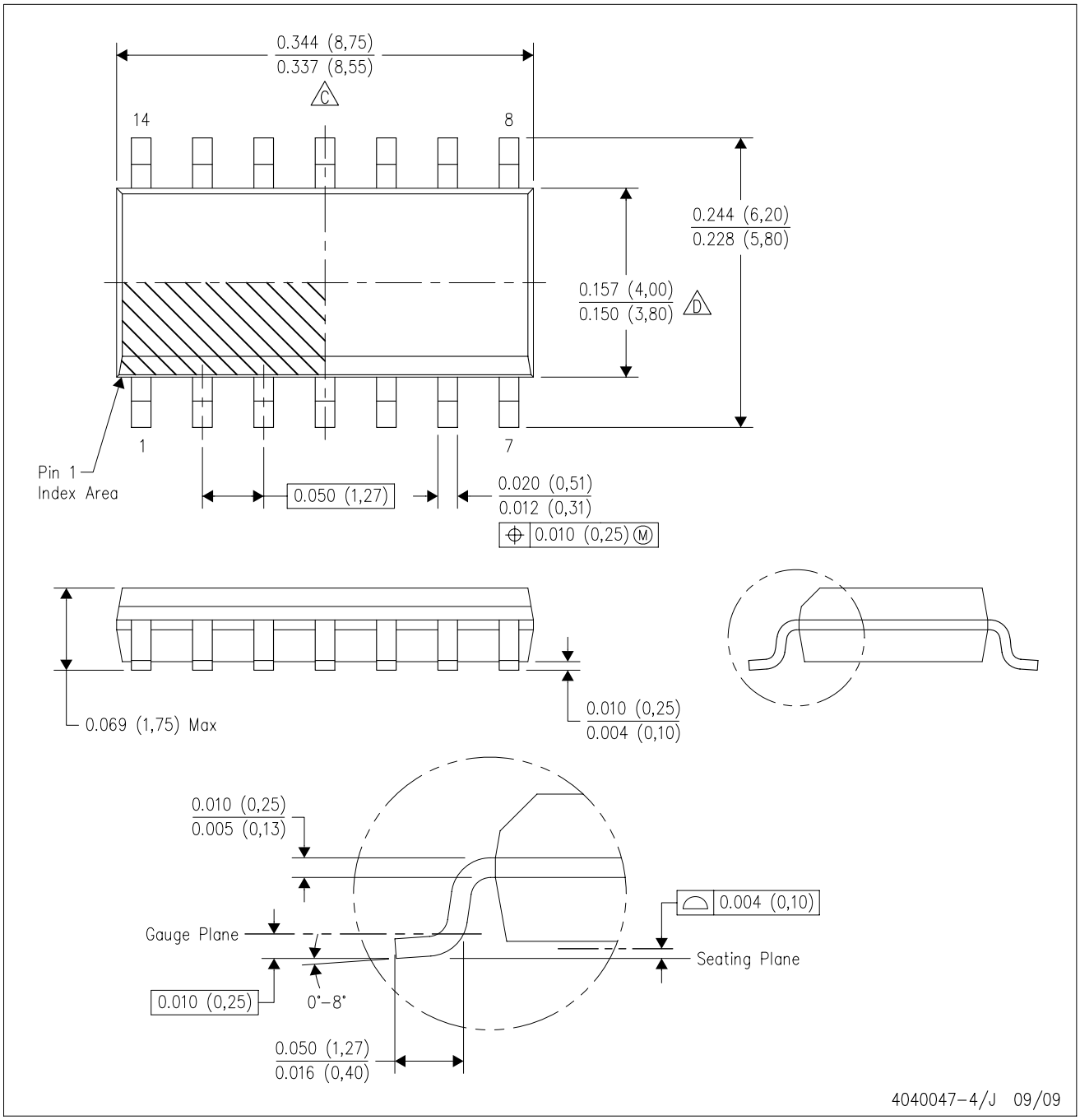


DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

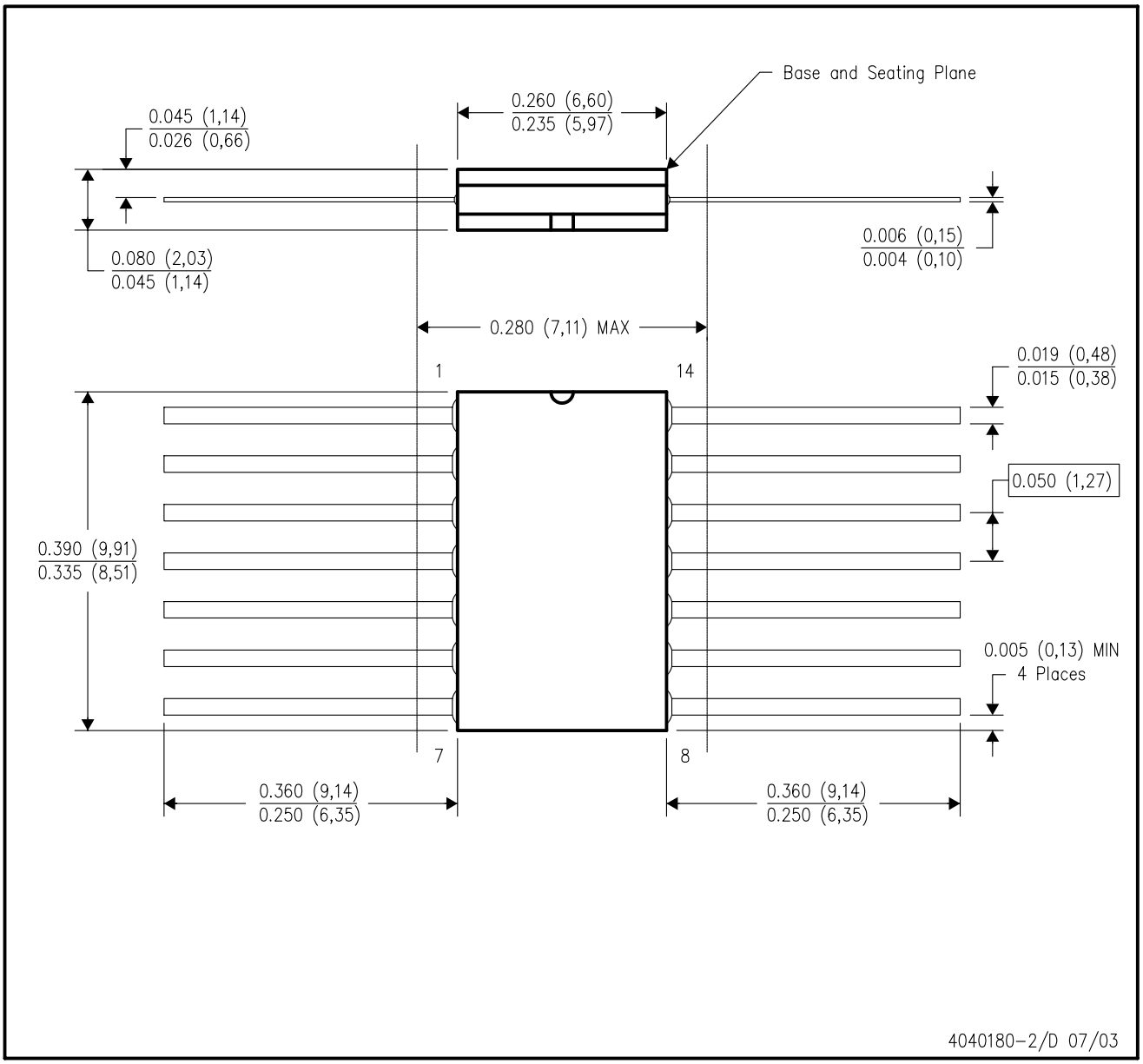
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

D (R–PDSO–G14) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AB.

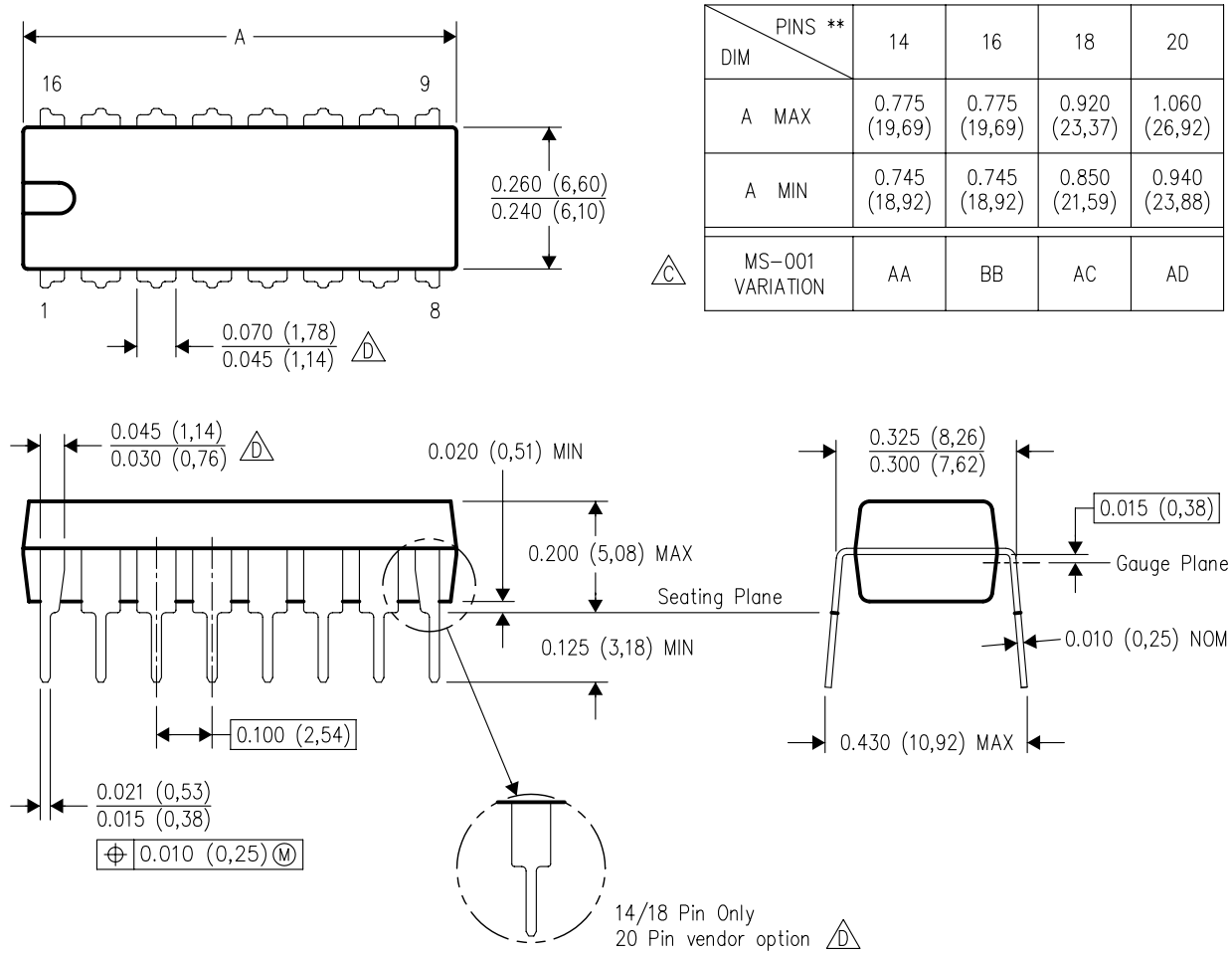
W (R–GDFP–F14) CERAMIC DUAL FLATPACK



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14 and JEDEC MO–092AB

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

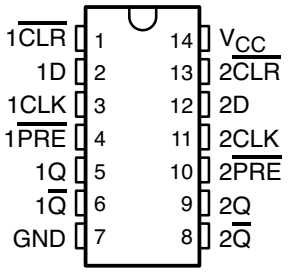


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD

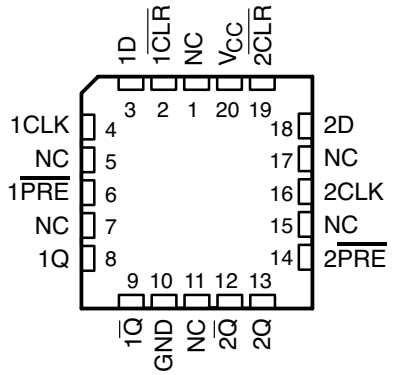
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

- **Wide Operating Voltage Range of 2 V to 6 V**
- **Outputs Can Drive Up To 10 LSTTL Loads**
- **Low Power Consumption, 40-μA Max I_{CC}**
- **Typical t_{pd} = 15 ns**
- **±4-mA Output Drive at 5 V**
- **Low Input Current of 1 μA Max**

SN54HC74 . . . J OR W PACKAGE
SN74HC74 . . . D, DB, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54HC74 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

The ’HC74 devices contain two independent D-type positive-edge-triggered flip-flops. A low level at the preset ($\overline{PRE}$) or clear ($\overline{CLR}$) inputs sets or resets the outputs, regardless of the levels of the other inputs. When $\overline{PRE}$ and $\overline{CLR}$ are inactive (high), data at the data (D) input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of CLK. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – N	Tube of 25	SN74HC74N	SN74HC74N
	SOIC – D	Tube of 50	SN74HC74D	HC74
		Reel of 2500	SN74HC74DR	
		Reel of 250	SN74HC74DT	
	SOP – NS	Reel of 2000	SN74HC74NSR	HC74
	SSOP – DB	Reel of 2000	SN74HC74DBR	HC74
	TSSOP – PW	Tube of 90	SN74HC74PW	HC74
		Reel of 2000	SN74HC74PWR	
		Reel of 250	SN74HC74PWT	
–55°C to 125°C	CDIP – J	Tube of 25	SNJ54HC74J	SNJ54HC74J
	CFP – W	Tube of 150	SNJ54HC74W	SNJ54HC74W
	LCCC – FK	Tube of 55	SNJ54HC74FK	SNJ54HC74FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2003, Texas Instruments Incorporated

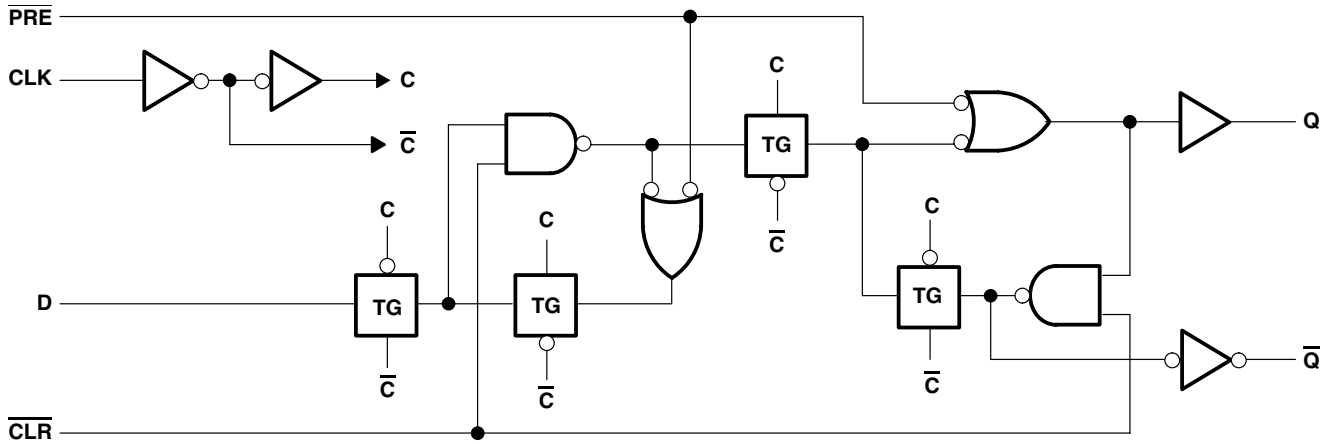
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H†	H†
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

† This configuration is nonstable; that is, it does not persist when $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) . . . . . ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND . . . . . ±50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package . . . . . 86°C/W
DB package . . . . . 96°C/W
N package . . . . . 80°C/W
NS package . . . . . 76°C/W
PW package . . . . . 113°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			SN54HC74			SN74HC74			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V			0.5			0.5	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 6 V			1.8			1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise/fall time	V_{CC} = 2 V			1000			1000	ns
		V_{CC} = 4.5 V			500			500	
		V_{CC} = 6 V			400			400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC74		SN74HC74		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –4 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –5.2 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	$V_I = V_{IH}$ or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	$V_I = V_{CC}$ or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	$V_I = V_{CC}$ or 0,	I_O = 0	6 V			4		80		40	μA
C_i			2 V to 6 V		3	10		10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			V_{CC}	T_A = 25°C		SN54HC74		SN74HC74		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		2 V		6		4.2		5	MHz
			4.5 V		31		21		25	
			6 V	0	36	0	25	0	29	
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	2 V	100		150		125		ns
			4.5 V	20		30		25		
			6 V	17		25		21		
		CLK high or low	2 V	80		120		100		
			4.5 V	16		24		20		
			6 V	14		20		17		
t_{su}	Setup time before CLK↑	Data	2 V	100		150		125		ns
			4.5 V	20		30		25		
			6 V	17		25		21		
		$\overline{PRE}$ or $\overline{CLR}$ inactive	2 V	25		40		30		
			4.5 V	5		8		6		
			6 V	4		7		5		
t_h	Hold time, data after CLK↑		2 V	0		0		0		ns
			4.5 V	0		0		0		
			6 V	0		0		0		

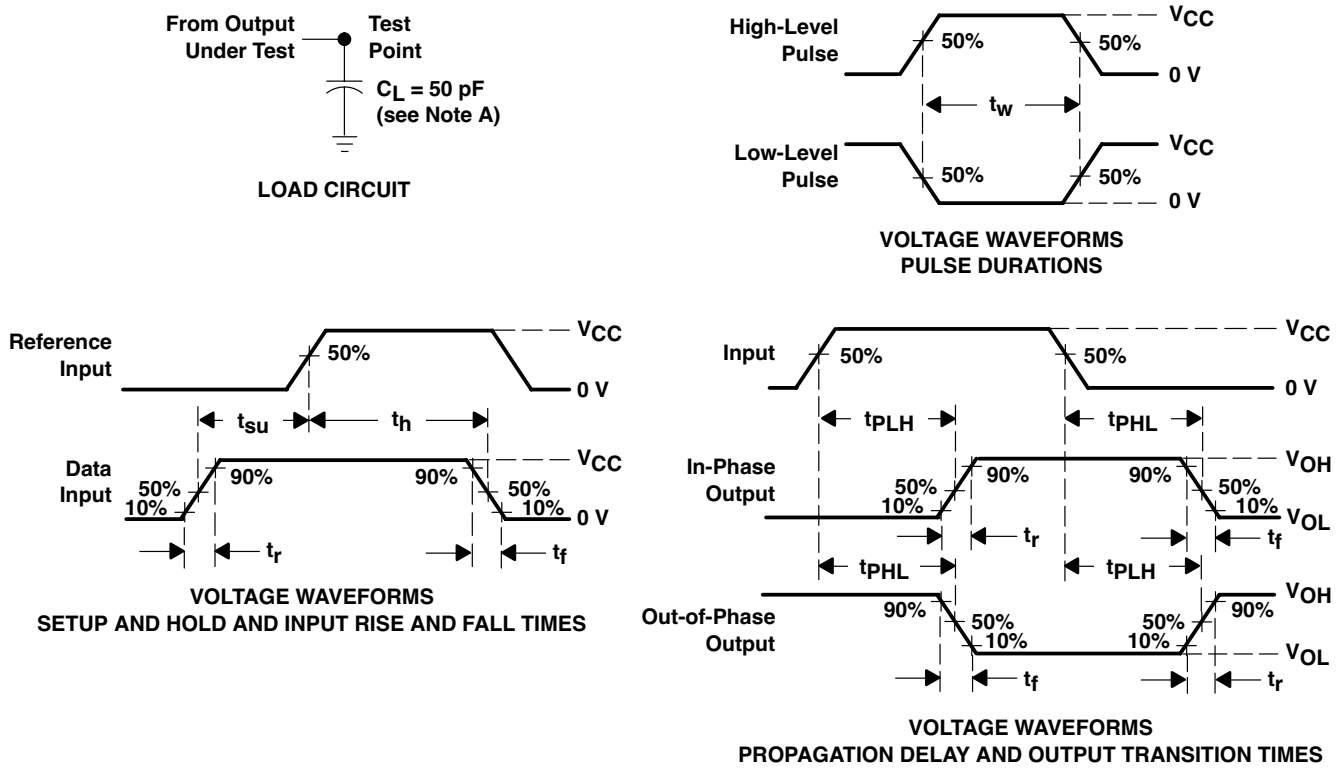
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC74		SN74HC74		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	6	10		4.2		5		MHz
			4.5 V	31	50		21		25		
			6 V	36	60		25		29		
t_{pd}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	2 V		70	230		345		290	ns
			4.5 V		20	46		69		58	
			6 V		15	39		59		49	
	CLK	Q or $\overline{Q}$	2 V		70	175		250		220	
			4.5 V		20	35		50		44	
			6 V		15	30		42		37	
t_t		Q or $\overline{Q}$	2 V		28	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per flip-flop	No load	35	pF

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
Low Power Wireless	www.ti.com/lpw	Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2007, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
5962-8405601VCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type
5962-8405601VDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
84056012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
8405601CA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type
8405601DA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
JM38510/65302B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
JM38510/65302BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type
JM38510/65302BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
SN54HC74J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type
SN74HC74ADBLE	OBSOLETE	SSOP	DB	14		TBD	Call TI	Call TI
SN74HC74D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC74DBLE	OBSOLETE	SSOP	DB	14		TBD	Call TI	Call TI
SN74HC74DBR	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC74DBRG4	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC74DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC74DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC74DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC74DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC74DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC74DT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC74DTE4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC74DTG4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC74N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74HC74N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN74HC74NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74HC74NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC74NSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC74NSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC74PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC74PWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS &	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
						no Sb/Br)		
SN74HC74PWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC74PWLE	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI
SN74HC74PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC74PWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC74PWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC74PWT	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC74PWTE4	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC74PWTG4	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SNJ54HC74FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54HC74J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type
SNJ54HC74W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54HC74, SN54HC74-SP, SN74HC74 :
- Automotive: SN74HC74-Q1

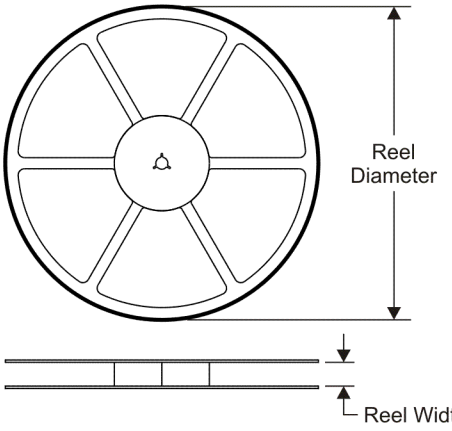
- Enhanced Product: SN74HC74-EP

NOTE: Qualified Version Definitions:

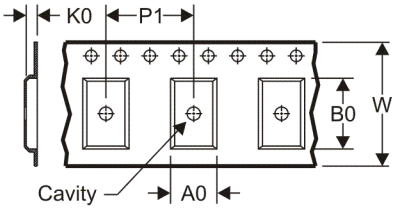
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

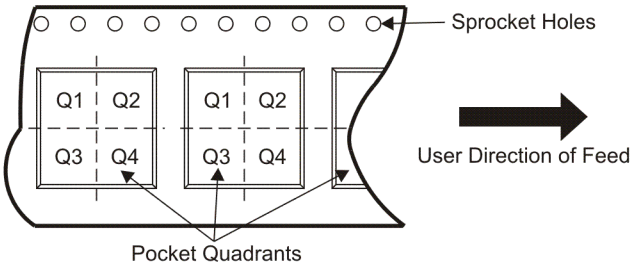


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

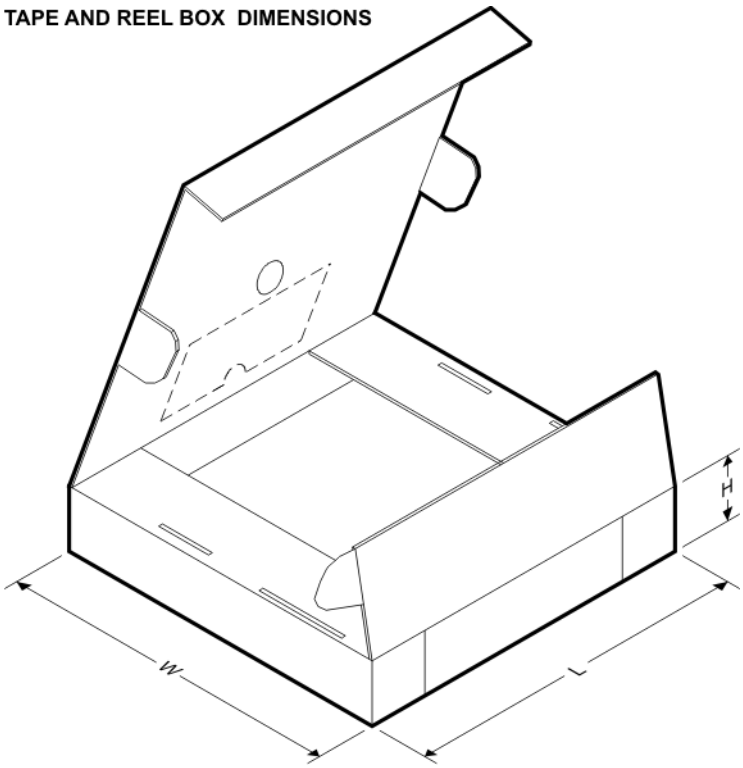
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC74DBR	SSOP	DB	14	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN74HC74DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC74DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC74NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74HC74PWR	TSSOP	PW	14	2000	330.0	12.4	7.0	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

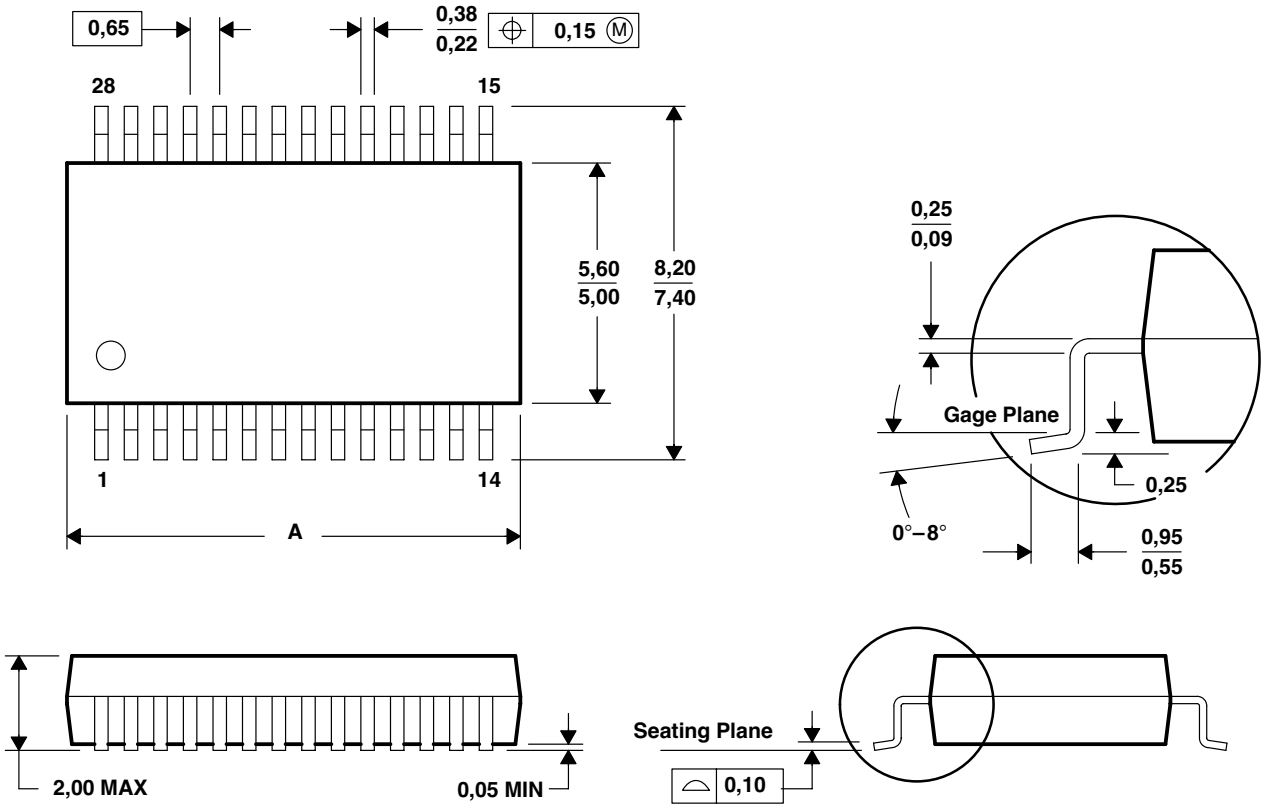


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC74DBR	SSOP	DB	14	2000	346.0	346.0	33.0
SN74HC74DR	SOIC	D	14	2500	346.0	346.0	33.0
SN74HC74DR	SOIC	D	14	2500	333.2	345.9	28.6
SN74HC74NSR	SO	NS	14	2000	346.0	346.0	33.0
SN74HC74PWR	TSSOP	PW	14	2000	346.0	346.0	29.0

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

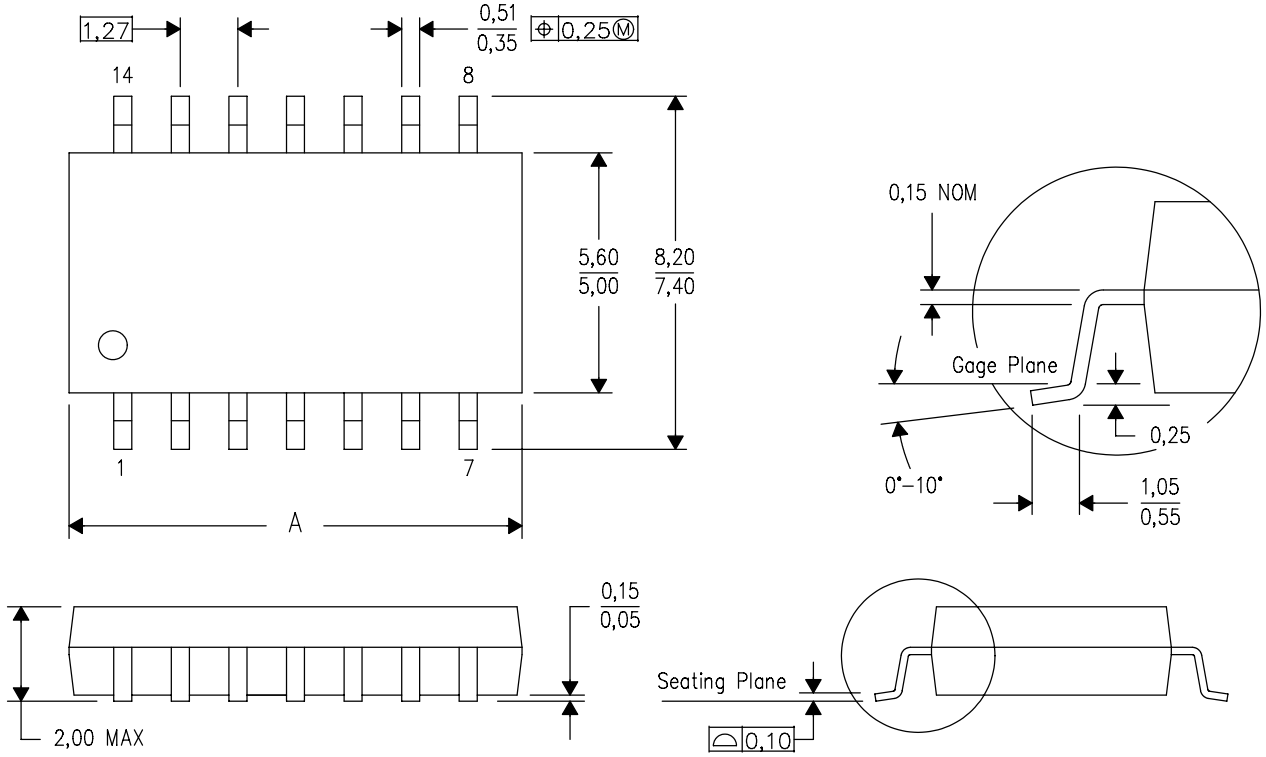
4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

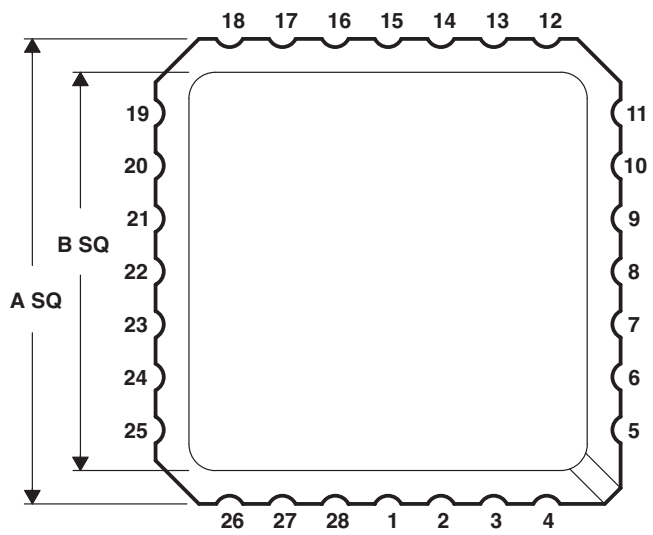
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

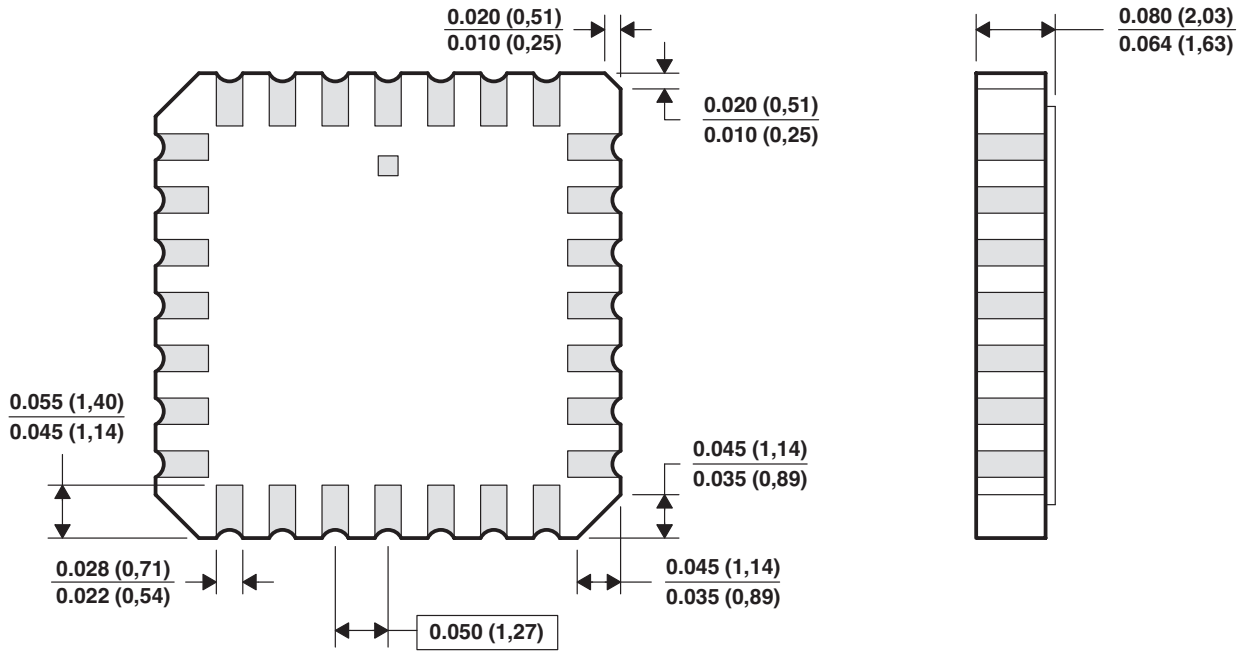
FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

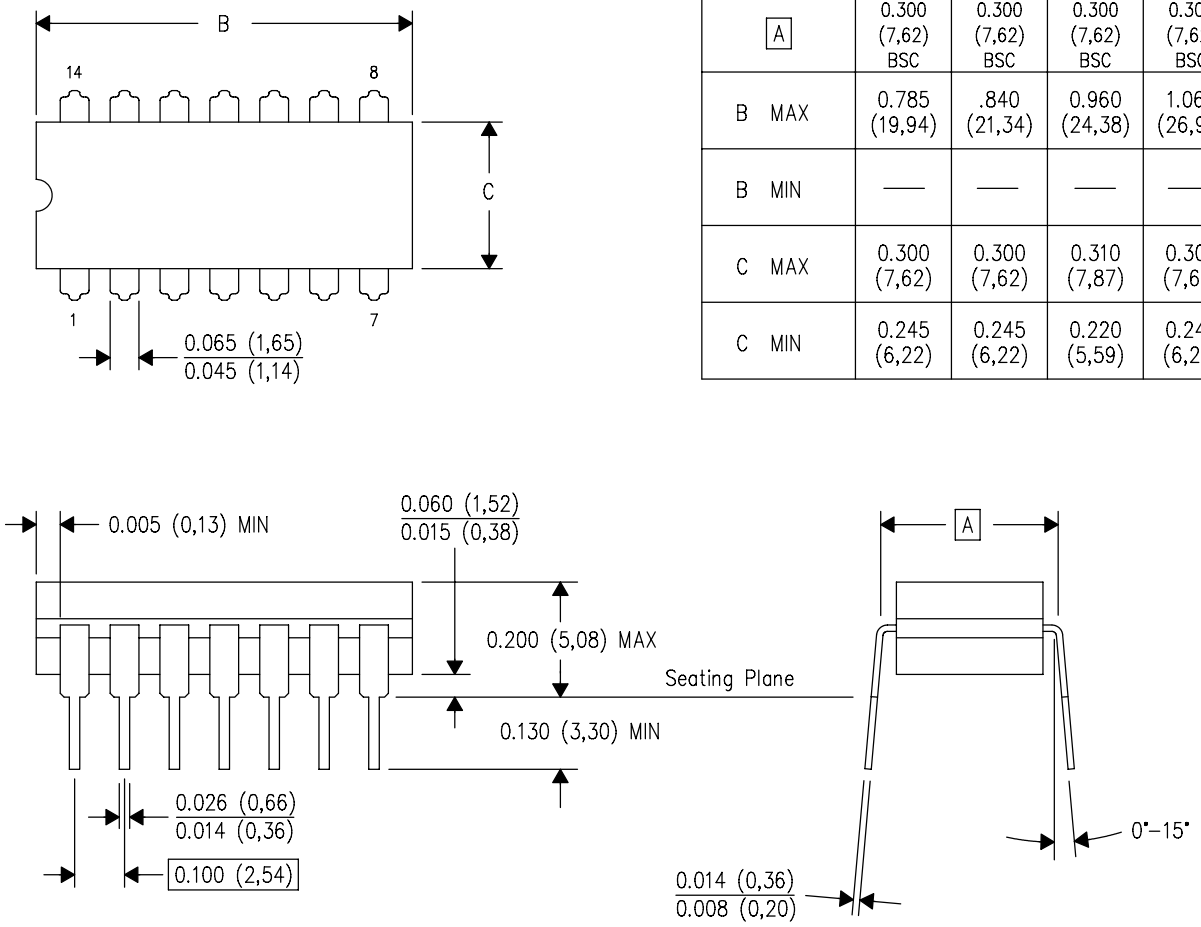


4040140/D 10/96

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MS-004

J (R–GDIP–T**) CERAMIC DUAL IN–LINE PACKAGE

14 LEADS SHOWN



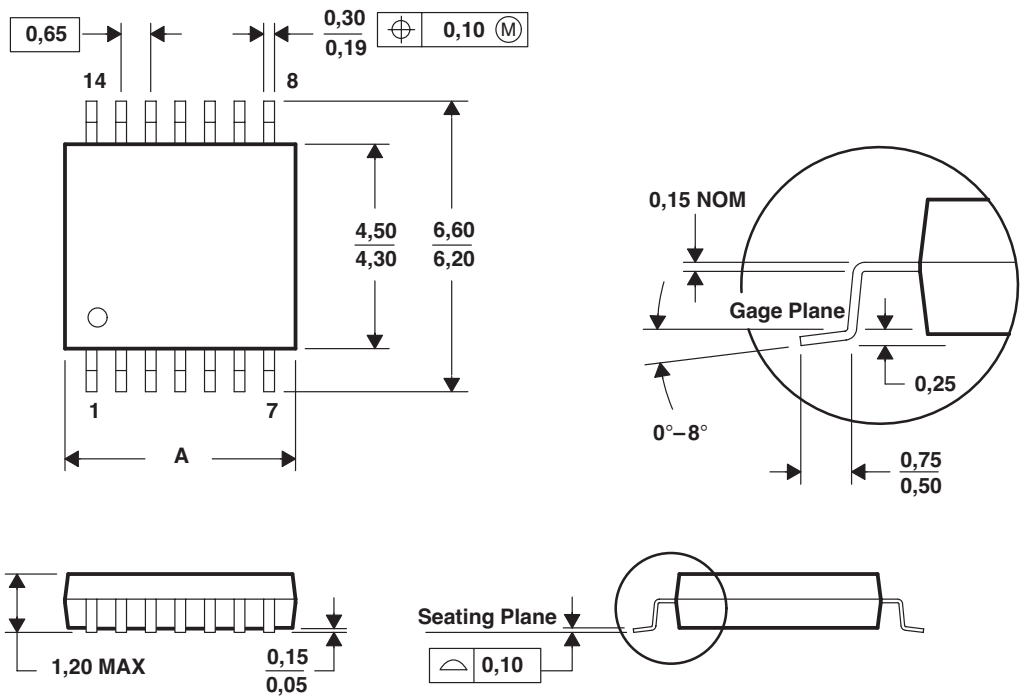
DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN

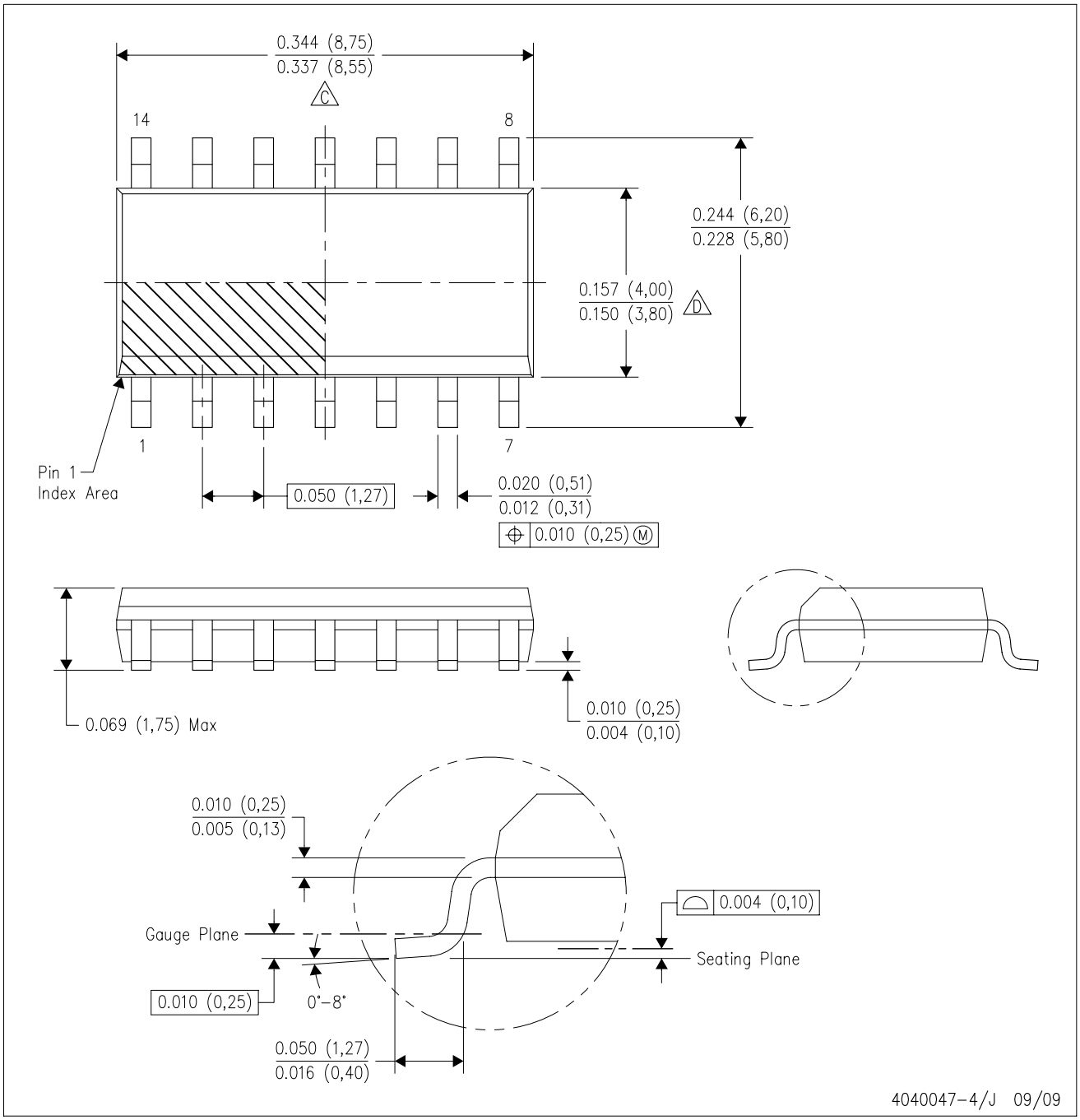


DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

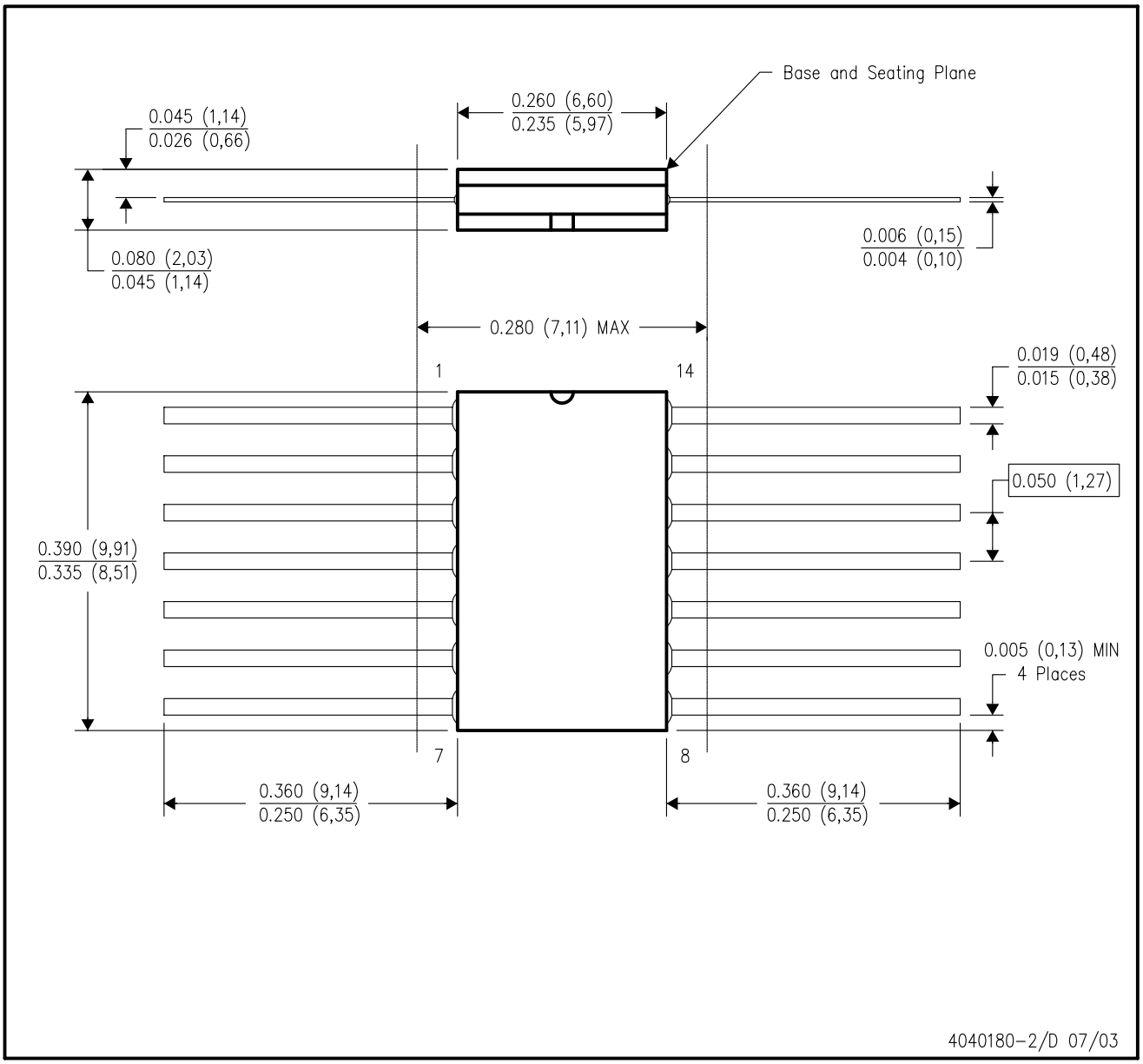
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

D (R–PDSO–G14) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AB.

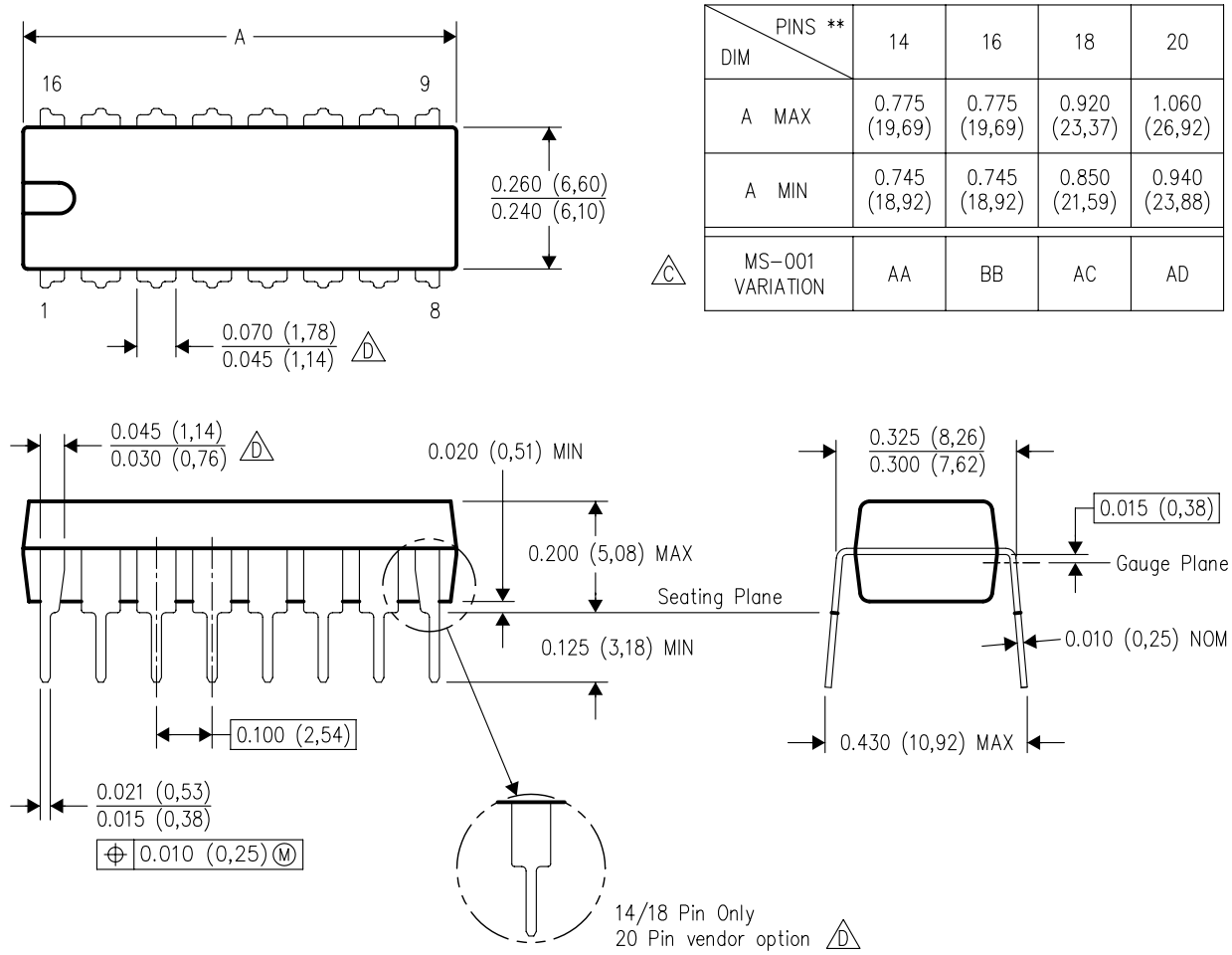
W (R–GDFP–F14) CERAMIC DUAL FLATPACK



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14 and JEDEC MO–092AB

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

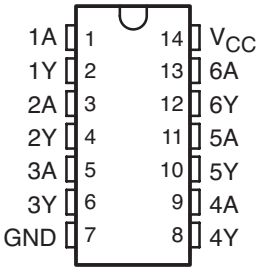
Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DLP® Products	www.dlp.com	Broadband	www.ti.com/broadband
DSP	dsp.ti.com	Digital Control	www.ti.com/digitalcontrol
Clocks and Timers	www.ti.com/clocks	Medical	www.ti.com/medical
Interface	interface.ti.com	Military	www.ti.com/military
Logic	logic.ti.com	Optical Networking	www.ti.com/opticalnetwork
Power Mgmt	power.ti.com	Security	www.ti.com/security
Microcontrollers	microcontroller.ti.com	Telephony	www.ti.com/telephony
RFID	www.ti-rfid.com	Video & Imaging	www.ti.com/video
RF/IF and ZigBee® Solutions	www.ti.com/lprf	Wireless	www.ti.com/wireless

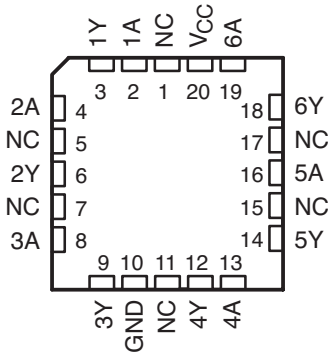
Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2009, Texas Instruments Incorporated

- **Wide Operating Voltage Range of 2 V to 6 V**
- **Outputs Can Drive Up To 10 LSTTL Loads**
- **Low Power Consumption, 20-μA Max I_{CC}**
- **Typical t_{pd} = 11 ns**
- **±4-mA Output Drive at 5 V**
- **Low Input Current of 1 μA Max**

SN54HC14 . . . J OR W PACKAGE
SN74HC14 . . . D, DB, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54HC14 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

These Schmitt-trigger devices contain six independent inverters. They perform the Boolean function $Y = \overline{A}$ in positive logic.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – N	Tube of 25	SN74HC14N	SN74HC14N
	SOIC – D	Tube of 50	SN74HC14D	HC14
		Reel of 2500	SN74HC14DR	
		Reel of 250	SN74HC14DT	
	SOP – NS	Reel of 2000	SN74HC14NSR	HC14
	SSOP – DB	Reel of 2000	SN74HC14DBR	HC14
	TSSOP – PW	Tube of 90	SN74HC14PW	HC14
		Reel of 2000	SN74HC14PWR	
		Reel of 250	SN74HC14PWT	
–55°C to 125°C	CDIP – J	Tube	SNJ54HC14J	SNJ54HC14J
	CFP – W	Tube	SNJ54HC14W	SNJ54HC14W
	LCCC – FK	Tube	SNJ54HC14FK	SNJ54HC14FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

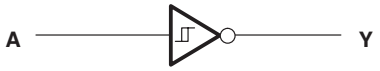
Copyright © 2004, Texas Instruments Incorporated

On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

FUNCTION TABLE
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) . . . . . ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND . . . . . ±50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package . . . . . 86°C/W
DB package . . . . . 96°C/W
N package . . . . . 80°C/W
NS package . . . . . 76°C/W
PW package . . . . . 113°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		SN54HC14			SN74HC14			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	2	5	6	2	5	6	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
T_A	Operating free-air temperature	–55		125	–40		85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	$T_A = 25°C$			SN54HC14		SN74HC14		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{T+}			2 V	0.7	1.2	1.5	0.7	1.5	0.7	1.5	V
			4.5 V	1.55	2.5	3.15	1.55	3.15	1.55	3.15	
			6 V	2.1	3.3	4.2	2.1	4.2	2.1	4.2	
V_{T-}			2 V	0.3	0.6	1	0.3	1	0.3	1	V
			4.5 V	0.9	1.6	2.45	0.9	2.45	0.9	2.45	
			6 V	1.2	2	3.2	1.2	3.2	1.2	3.2	
$V_{T+} - V_{T-}$			2 V	0.2	0.6	1.2	0.2	1.2	0.2	1.2	V
			4.5 V	0.4	0.9	2.1	0.4	2.1	0.4	2.1	
			6 V	0.5	1.3	2.5	0.5	2.5	0.5	2.5	
V_{OH}	$V_I = V_{IH}$ or V_{IL}	$I_{OH} = -20\ \mu A$	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		$I_{OH} = -4$ mA	4.5 V	3.98	4.3		3.7		3.84		
		$I_{OH} = -5.2$ mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	$V_I = V_{IH}$ or V_{IL}	$I_{OL} = 20\ \mu A$	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		$I_{OL} = 4$ mA	4.5 V		0.17	0.26		0.4		0.33	
		$I_{OL} = 5.2$ mA	6 V		0.15	0.26		0.4		0.33	
I_I	$V_I = V_{CC}$ or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	$V_I = V_{CC}$ or 0,	$I_O = 0$	6 V			2		40		20	μA
C_i			2 V to 6 V		3	10		10		10	pF

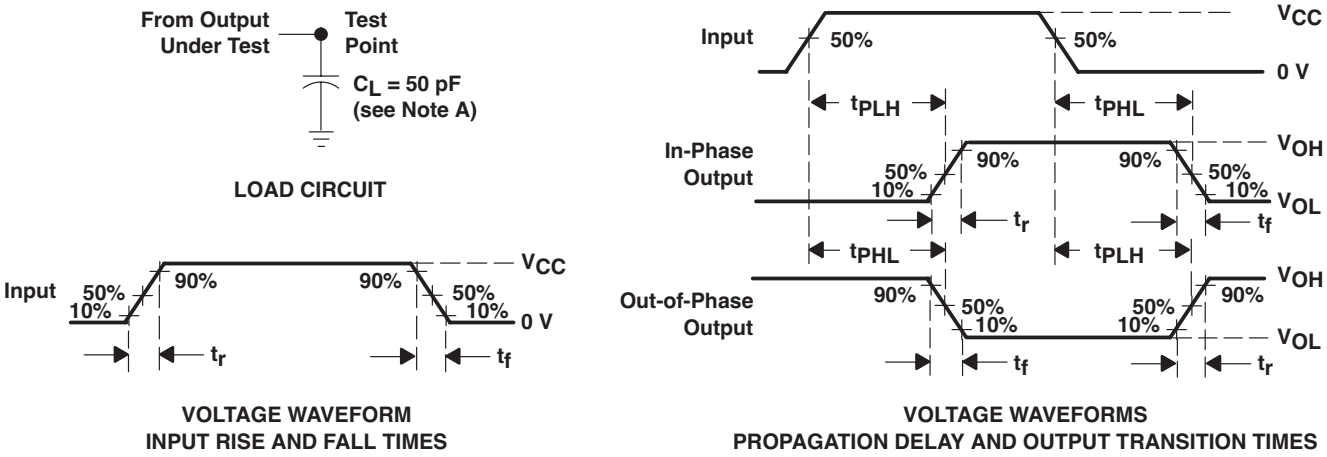
switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25°C$			SN54HC14		SN74HC14		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	2 V		55	125		190		155	ns
			4.5 V		12	25		38		31	
			6 V		11	21		32		26	
t_t		Y	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

operating characteristics, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per inverter	No load	20	pF

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. The outputs are measured one at a time, with one input transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
Low Power Wireless	www.ti.com/lpw	Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2007, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
5962-8409101VCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type
5962-8409101VDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
84091012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
8409101CA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type
8409101DA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
JM38510/65702BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type
JM38510/65702BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
SN54HC14J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type
SN74HC14D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC14DBR	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC14DBRE4	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC14DBRG4	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC14DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC14DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC14DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC14DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC14DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC14DT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC14DTE4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC14DTG4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC14N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74HC14N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN74HC14NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74HC14NSLE	OBSOLETE	SO	NS	14		TBD	Call TI	Call TI
SN74HC14NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC14NSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC14NSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC14PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC14PWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
SN74HC14PWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC14PWLE	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI
SN74HC14PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC14PWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC14PWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC14PWT	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC14PWTE4	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC14PWTG4	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SNJ54HC14FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54HC14J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type
SNJ54HC14W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

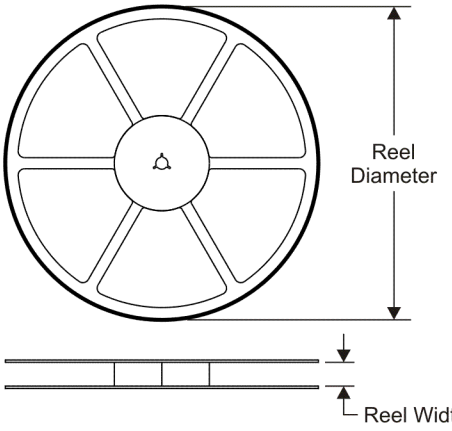
OTHER QUALIFIED VERSIONS OF SN54HC14, SN54HC14-SP, SN74HC14 :
- Automotive: SN74HC14-Q1

NOTE: Qualified Version Definitions:

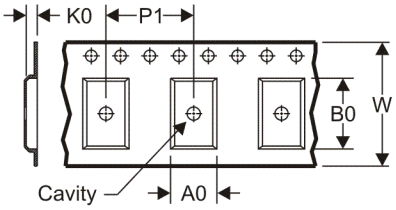
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

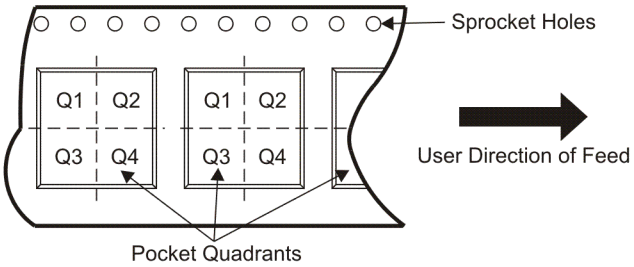


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

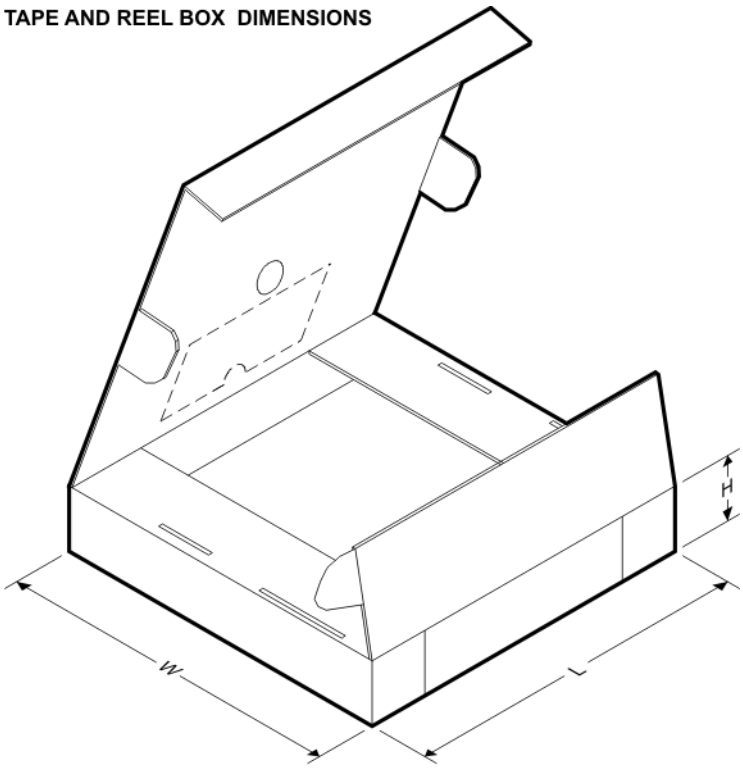
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC14DBR	SSOP	DB	14	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN74HC14DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC14DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC14NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74HC14PWR	TSSOP	PW	14	2000	330.0	12.4	7.0	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

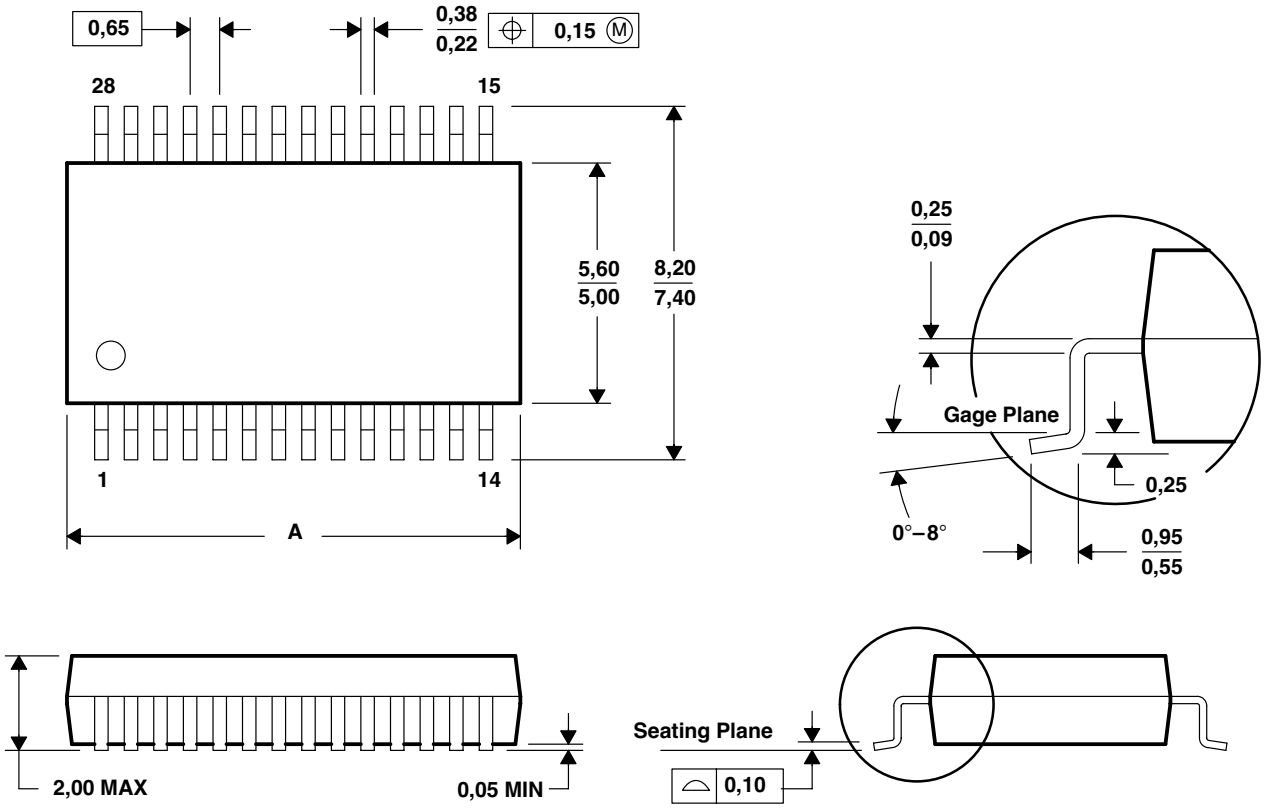


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC14DBR	SSOP	DB	14	2000	346.0	346.0	33.0
SN74HC14DR	SOIC	D	14	2500	333.2	345.9	28.6
SN74HC14DR	SOIC	D	14	2500	346.0	346.0	33.0
SN74HC14NSR	SO	NS	14	2000	346.0	346.0	33.0
SN74HC14PWR	TSSOP	PW	14	2000	346.0	346.0	29.0

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

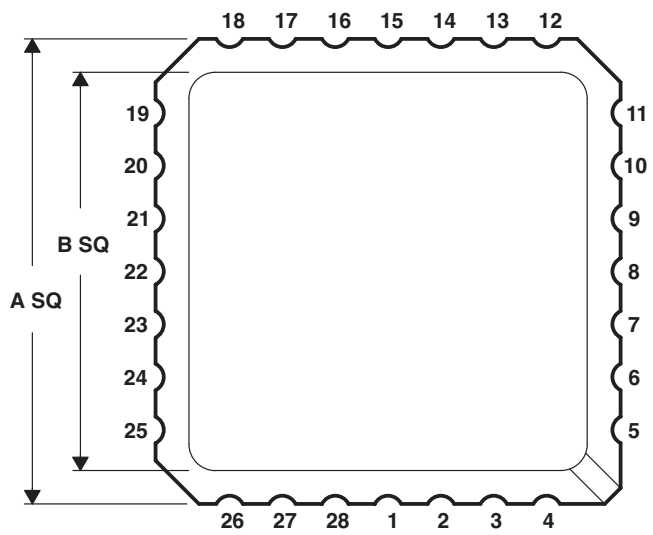
4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

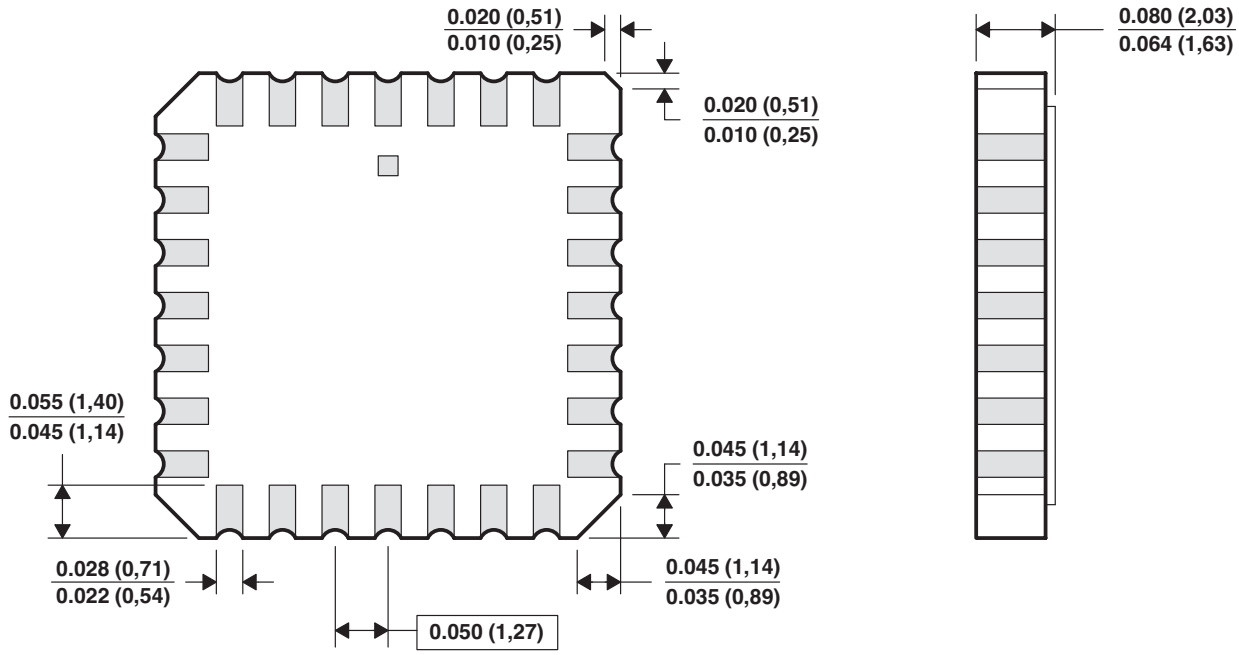
FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

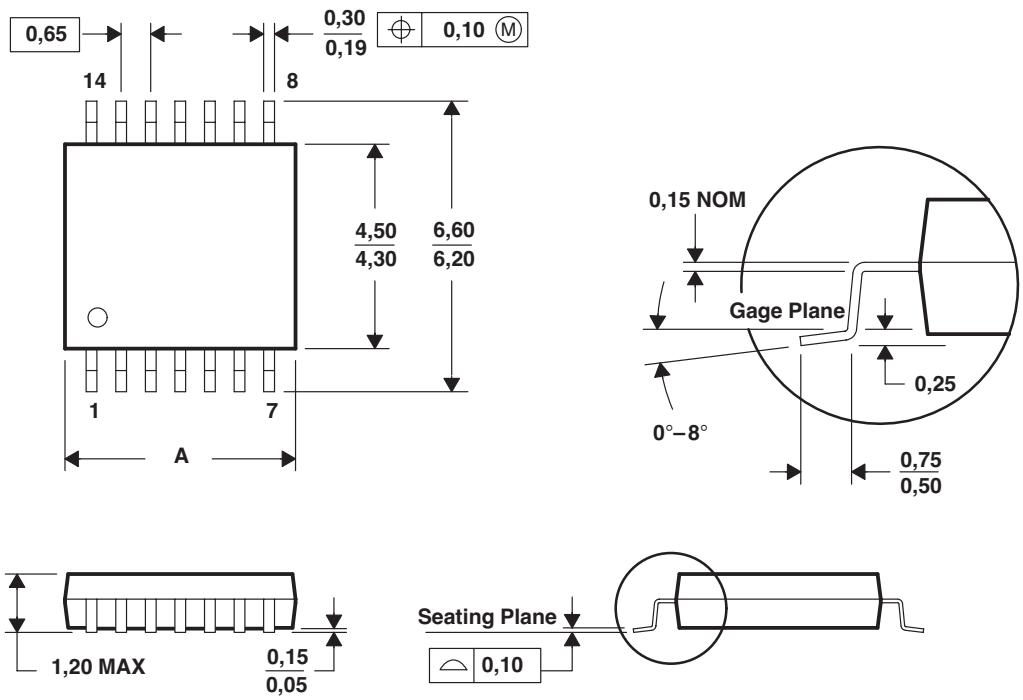


4040140/D 10/96

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MS-004

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



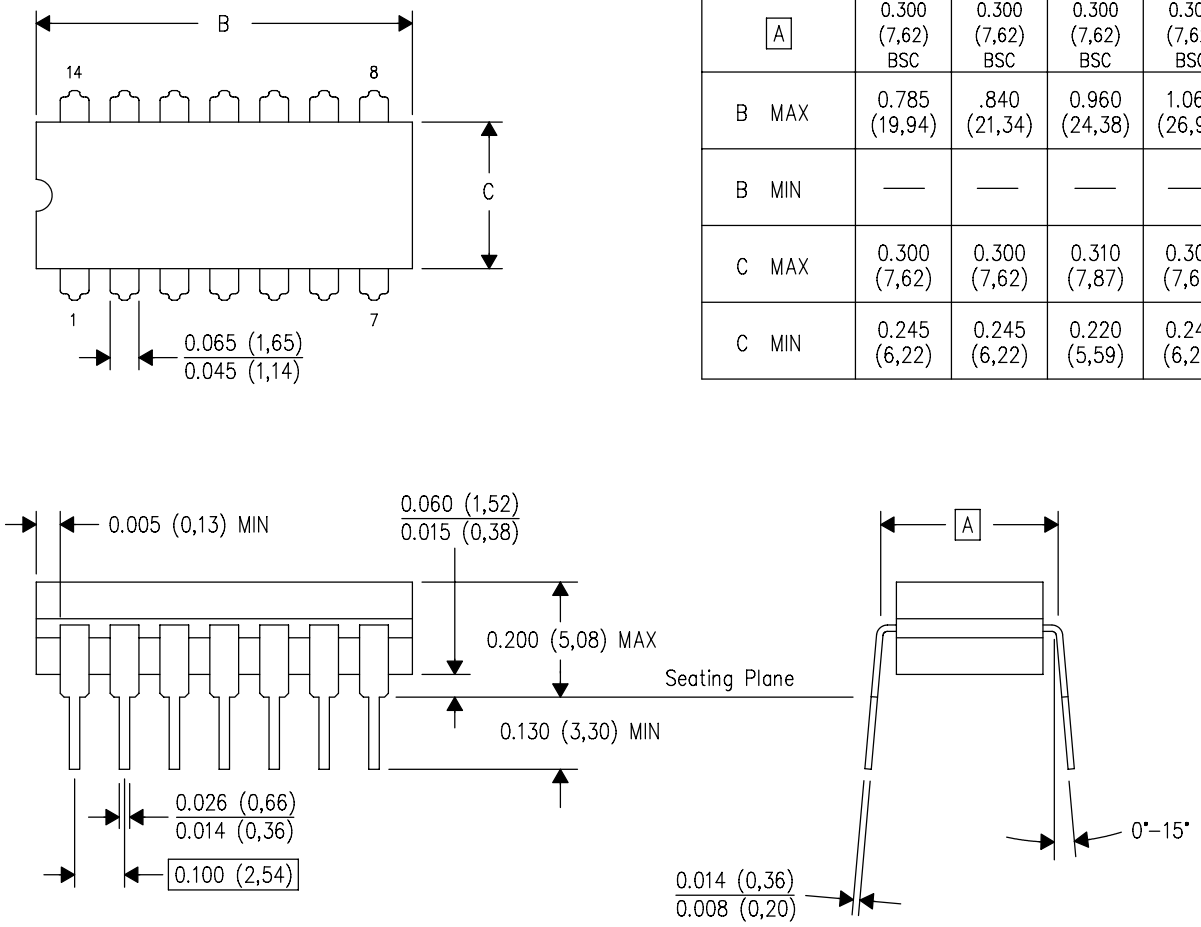
DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

J (R–GDIP–T**) CERAMIC DUAL IN–LINE PACKAGE

14 LEADS SHOWN



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

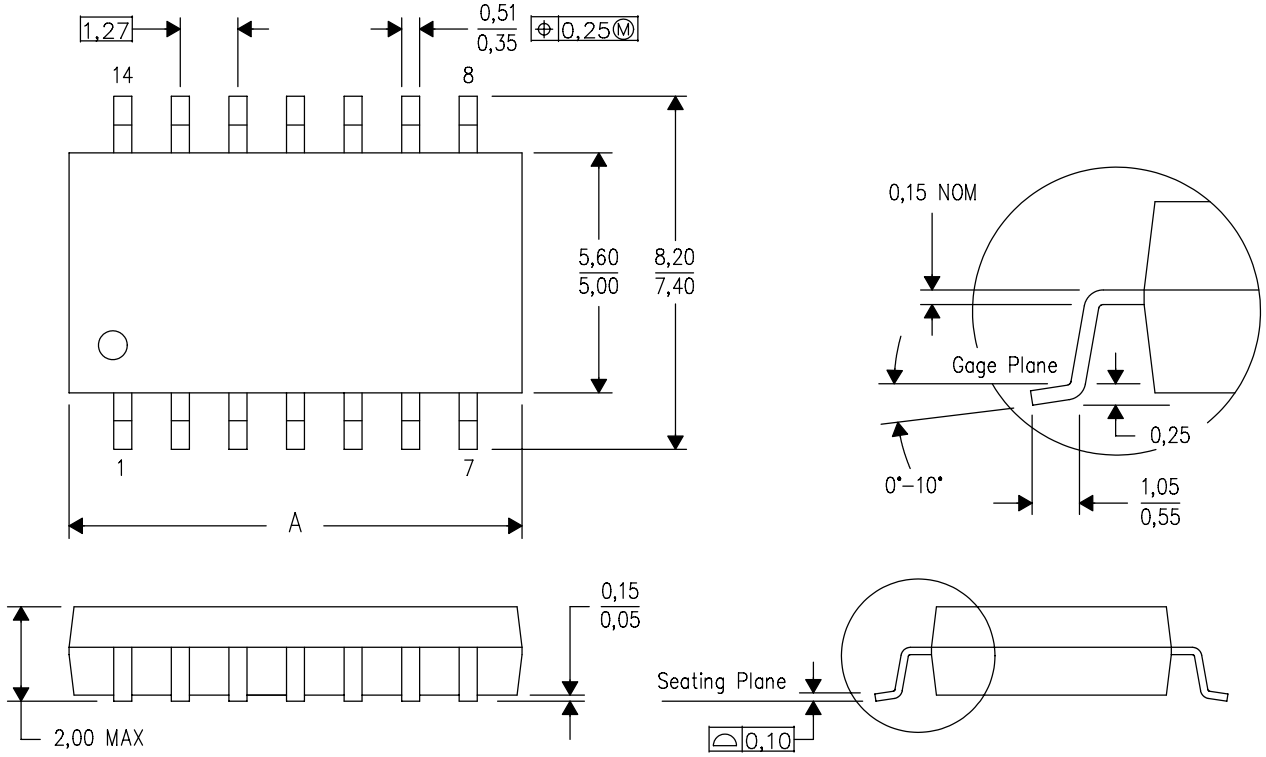
4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN

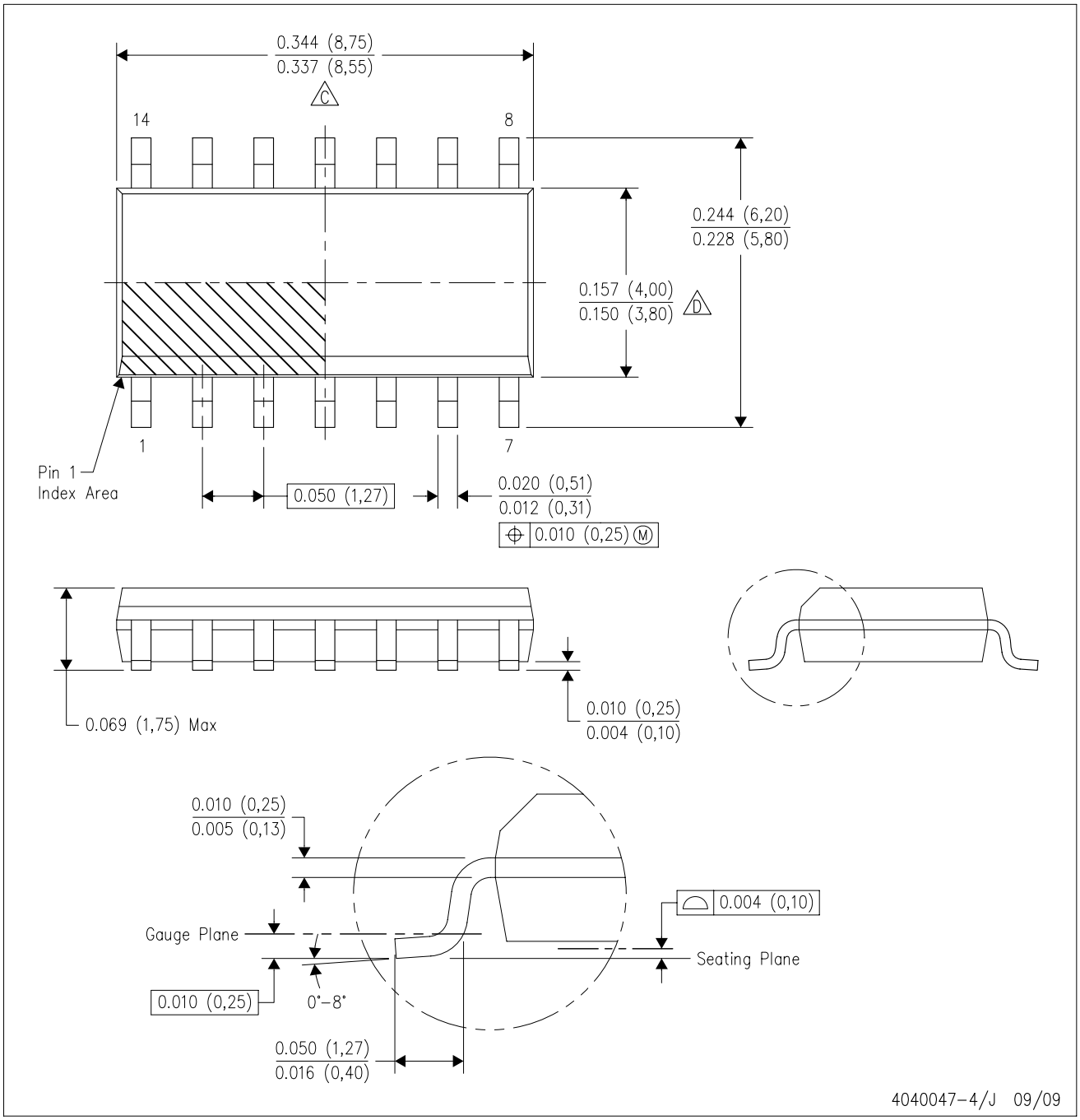


DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

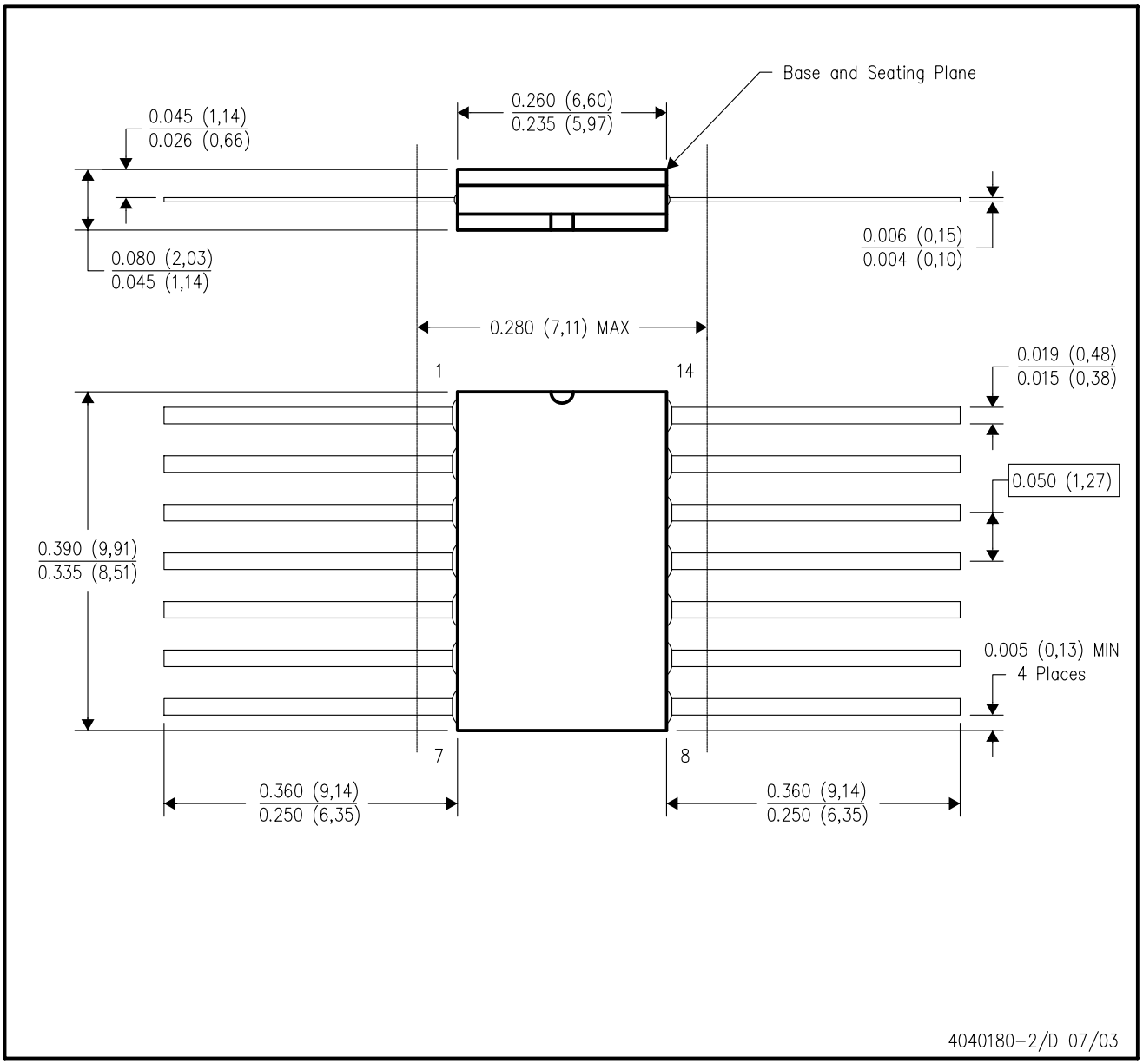
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

D (R–PDSO–G14) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AB.

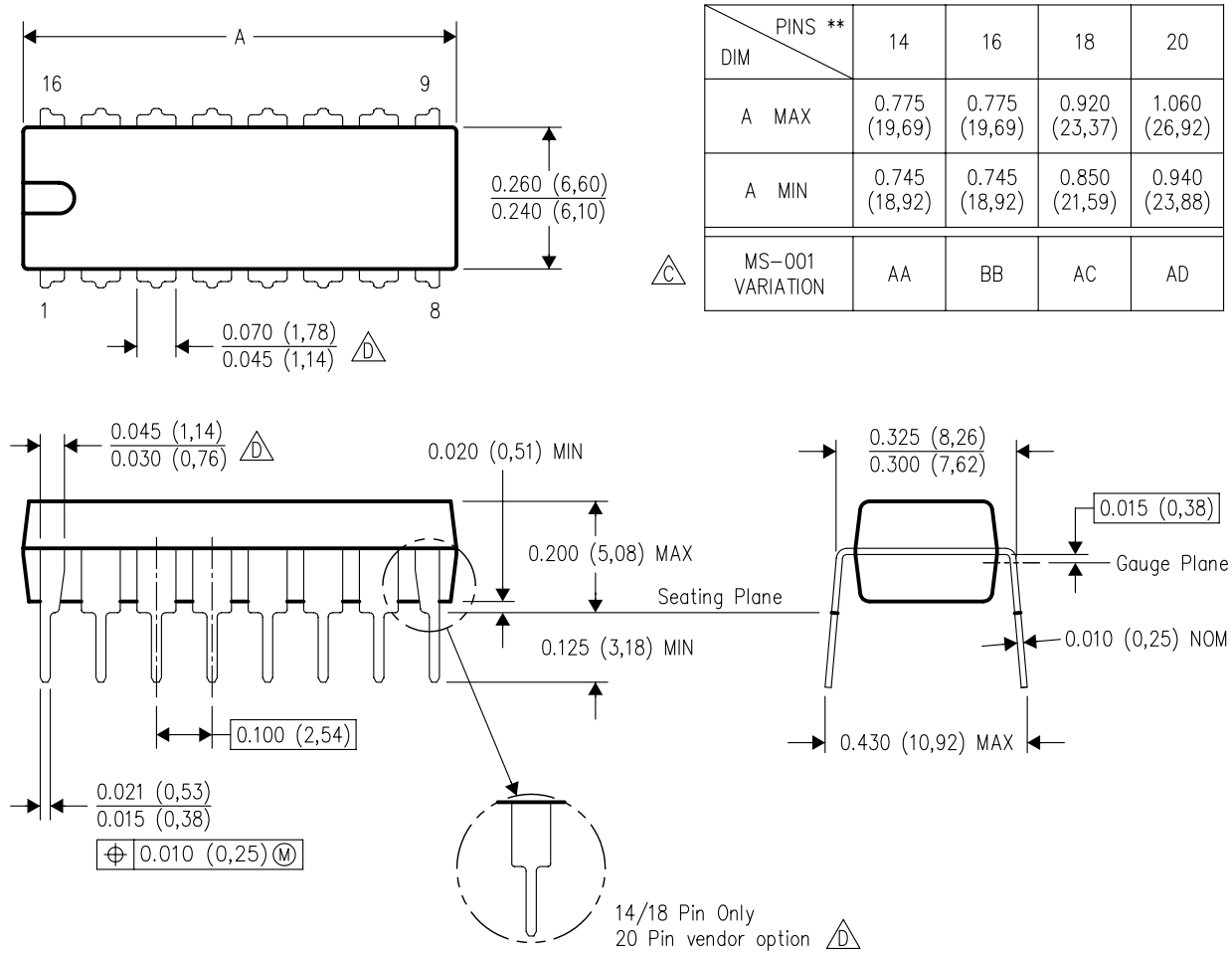
W (R–GDFP–F14) CERAMIC DUAL FLATPACK



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14 and JEDEC MO–092AB

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



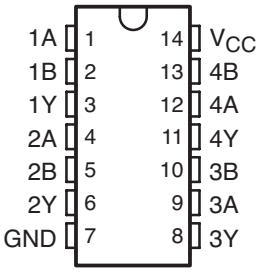
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

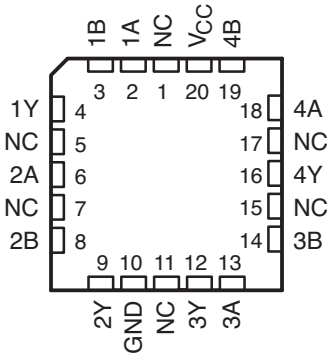
SCLS181E – DECEMBER 1982 – REVISED AUGUST 2003

- **Wide Operating Voltage Range of 2 V to 6 V**
- **Outputs Can Drive Up To 10 LSTTL Loads**
- **Low Power Consumption, 20-μA Max I_{CC}**
- **Typical t_{pd} = 8 ns**
- **±4-mA Output Drive at 5 V**
- **Low Input Current of 1 μA Max**

SN54HC00 . . . J OR W PACKAGE
SN74HC00 . . . D, DB, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54HC00 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

The ’HC00 devices contain four independent 2-input NAND gates. They perform the Boolean function $Y = \overline{A \bullet B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – N	Tube of 25	SN74HC00N	SN74HC00N
	SOIC – D	Tube of 50	SN74HC00D	HC00
		Reel of 2500	SN74HC00DR	
		Reel of 250	SN74HC00DT	
	SOP – NS	Reel of 2000	SN74HC00NSR	HC00
	SSOP – DB	Reel of 2000	SN74HC00DBR	HC00
	TSSOP – PW	Tube of 90	SN74HC00PW	HC00
		Reel of 2000	SN74HC00PWR	
		Reel of 250	SN74HC00PWT	
–55°C to 125°C	CDIP – J	Tube of 25	SNJ54HC00J	SNJ54HC00J
	CFP – W	Tube of 150	SNJ54HC00W	SNJ54HC00W
	LCCC – FK	Tube of 55	SNJ54HC00FK	SNJ54HC00FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2003, Texas Instruments Incorporated

On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

logic diagram (positive logic)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) . . . . . ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND . . . . . ±50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package . . . . . 86°C/W
DB package . . . . . 96°C/W
N package . . . . . 80°C/W
NS package . . . . . 76°C/W
PW package . . . . . 113°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			SN54HC00			SN74HC00			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V			0.5			0.5	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 6 V			1.8			1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise/fall time	V_{CC} = 2 V			1000			1000	ns
		V_{CC} = 4.5 V			500			500	
		V_{CC} = 6 V			400			400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	$T_A = 25°C$			SN54HC00		SN74HC00		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL}	$I_{OH} = -20\ \mu A$	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		$I_{OH} = -4$ mA	4.5 V	3.98	4.3		3.7		3.84		
		$I_{OH} = -5.2$ mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	$V_I = V_{IH}$ or V_{IL}	$I_{OL} = 20\ \mu A$	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		$I_{OL} = 4$ mA	4.5 V		0.17	0.26		0.4		0.33	
		$I_{OL} = 5.2$ mA	6 V		0.15	0.26		0.4		0.33	
I_I	$V_I = V_{CC}$ or 0		6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	$V_I = V_{CC}$ or 0,	$I_O = 0$	6 V			2		40		20	μA
C_i			2 V to 6 V		3	10		10		10	pF

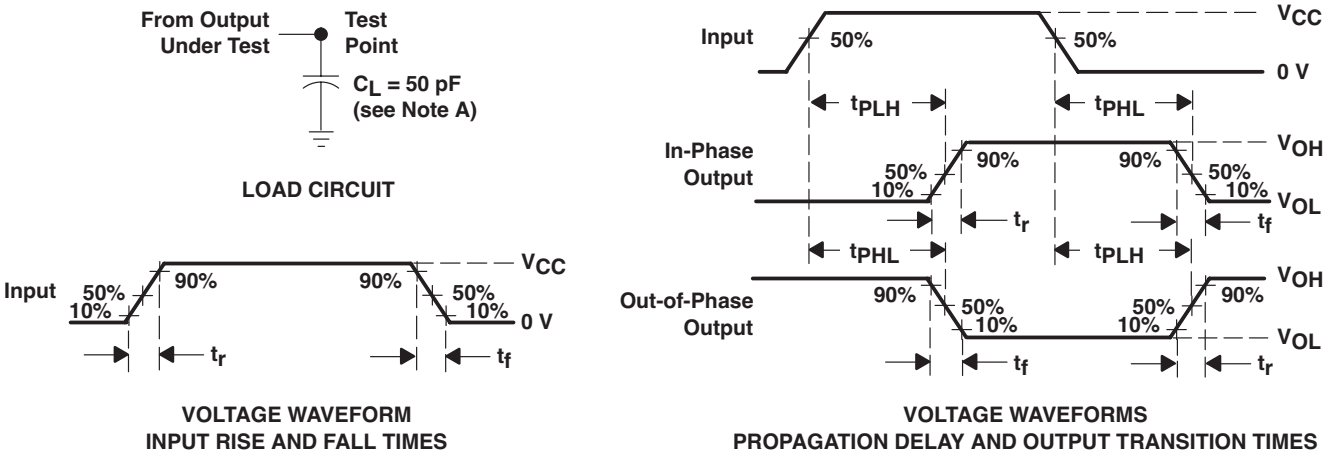
switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25°C$			SN54HC00		SN74HC00		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A or B	Y	2 V		45	90		135		115	ns
			4.5 V		9	18		27		23	
			6 V		8	15		23		20	
t_t		Y	2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

operating characteristics, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per gate	No load	20	pF

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. The outputs are measured one at a time with one input transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
5962-8403701VCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type
5962-8403701VDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
84037012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
8403701CA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type
8403701DA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
JM38510/65001B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
JM38510/65001BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type
JM38510/65001BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type
SN54HC00J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type
SN74HC00D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC00DBR	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC00DBRE4	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC00DBRG4	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC00DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC00DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC00DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC00DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC00DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC00DT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC00DTE4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC00DTG4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC00N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74HC00N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI
SN74HC00NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74HC00NSLE	OBSOLETE	SO	NS	14		TBD	Call TI	Call TI
SN74HC00NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC00NSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC00NSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC00PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN74HC00PWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC00PWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC00PWLE	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI
SN74HC00PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC00PWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC00PWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC00PWT	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC00PWTE4	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HC00PWTG4	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SNJ54HC00FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54HC00J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type
SNJ54HC00W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54HC00, SN54HC00-SP, SN74HC00 :

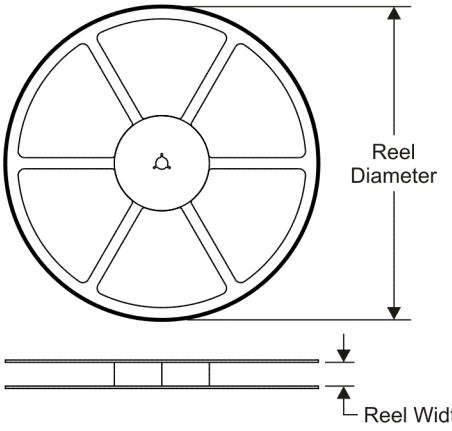
- Automotive: SN74HC00-Q1

NOTE: Qualified Version Definitions:

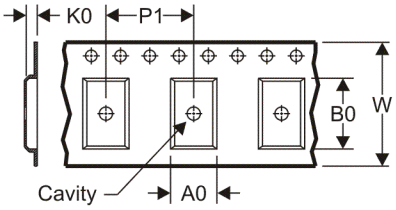
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

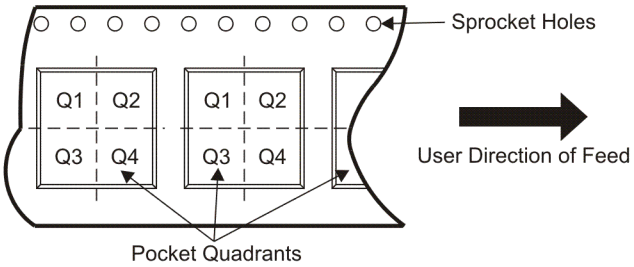


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

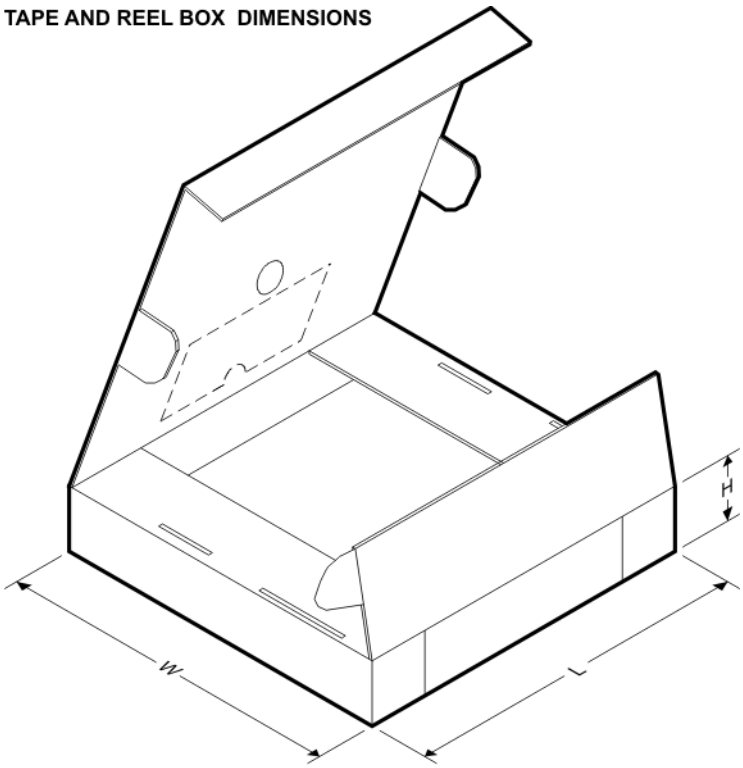
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC00DBR	SSOP	DB	14	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN74HC00DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC00DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC00NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74HC00PWR	TSSOP	PW	14	2000	330.0	12.4	7.0	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

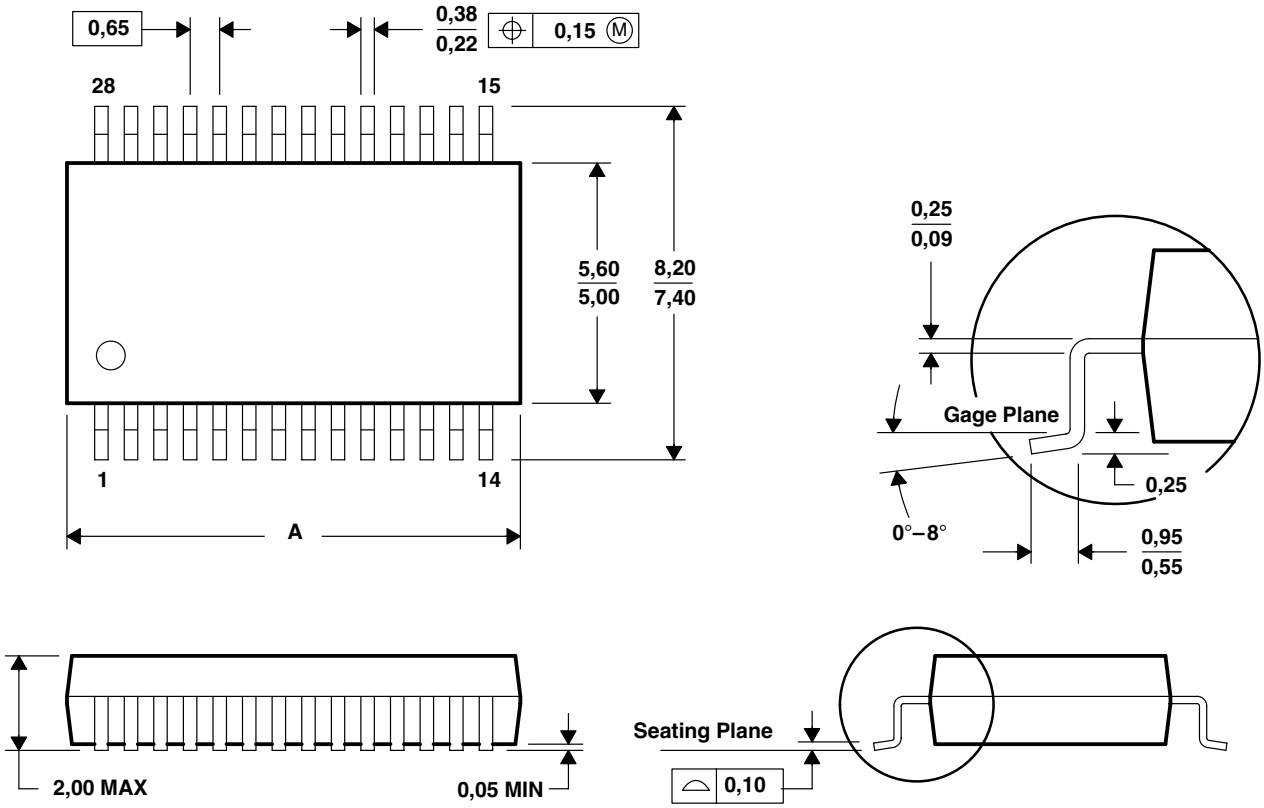


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC00DBR	SSOP	DB	14	2000	346.0	346.0	33.0
SN74HC00DR	SOIC	D	14	2500	346.0	346.0	33.0
SN74HC00DR	SOIC	D	14	2500	333.2	345.9	28.6
SN74HC00NSR	SO	NS	14	2000	346.0	346.0	33.0
SN74HC00PWR	TSSOP	PW	14	2000	346.0	346.0	29.0

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

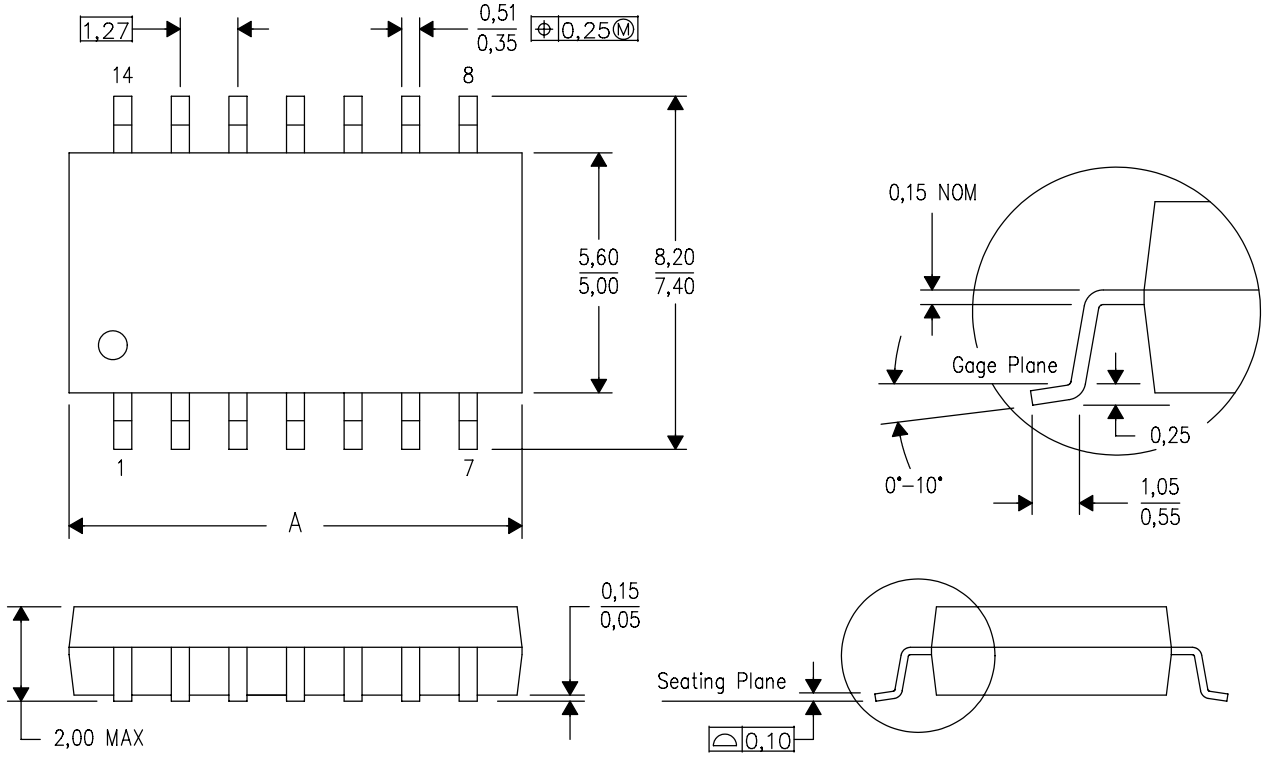
4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

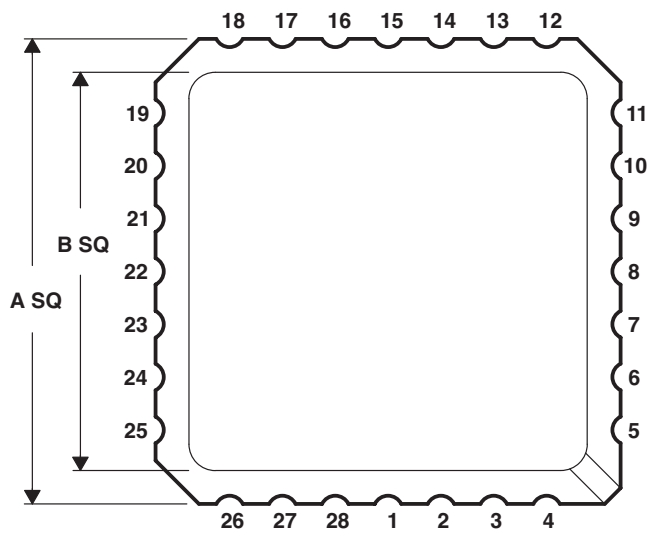
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

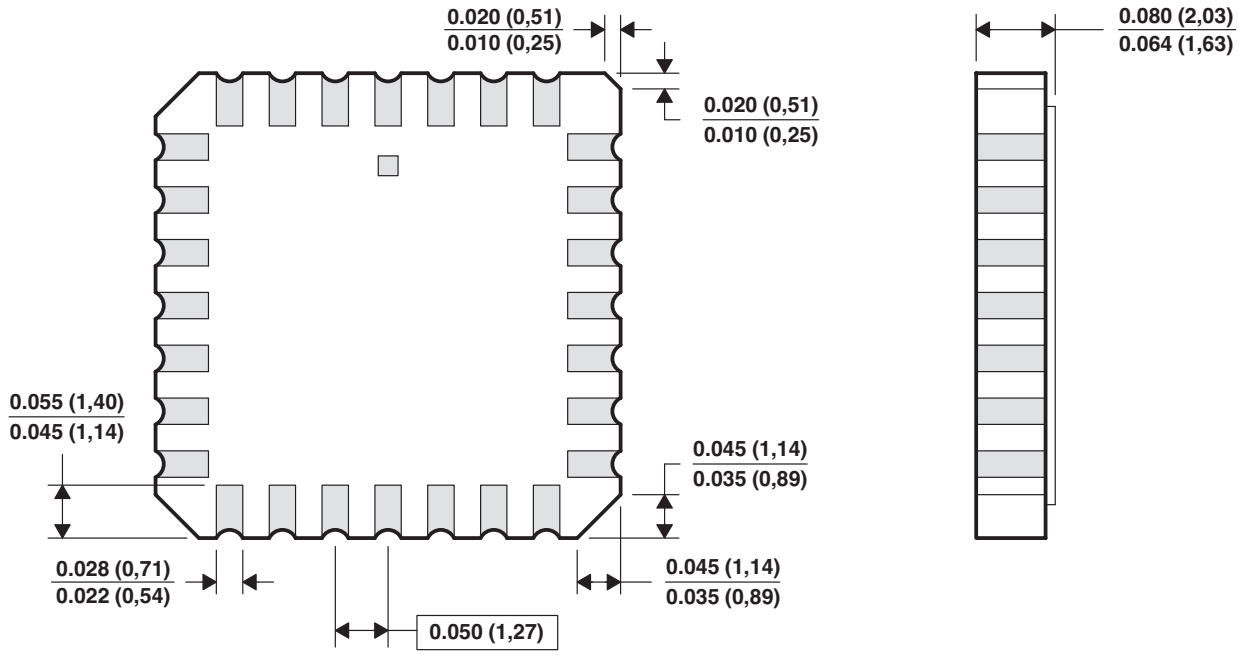
FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

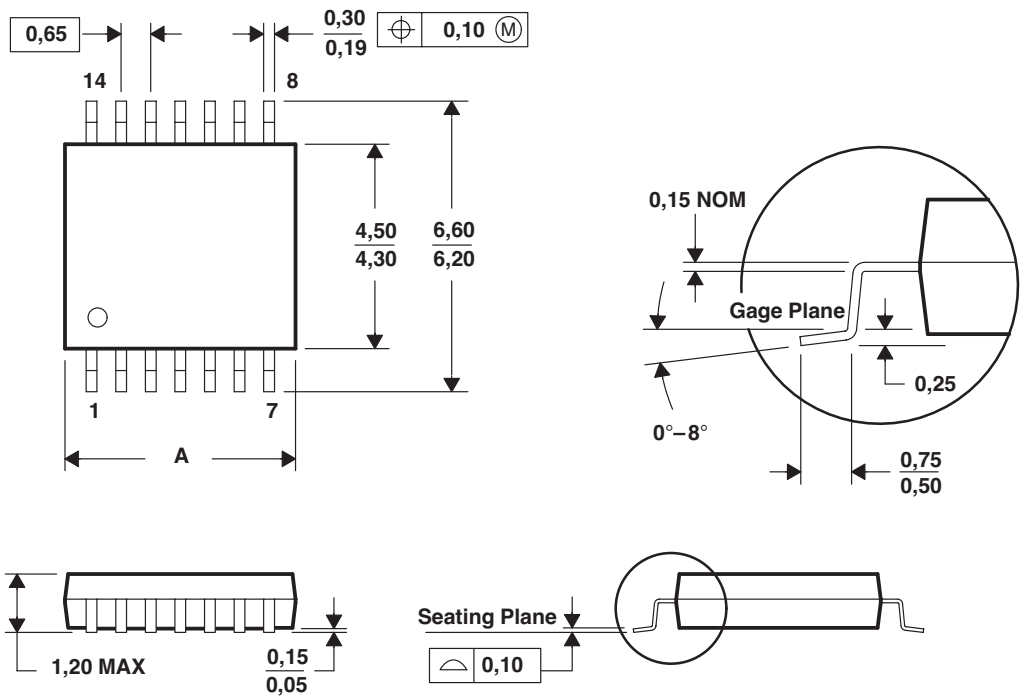


4040140/D 10/96

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MS-004

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



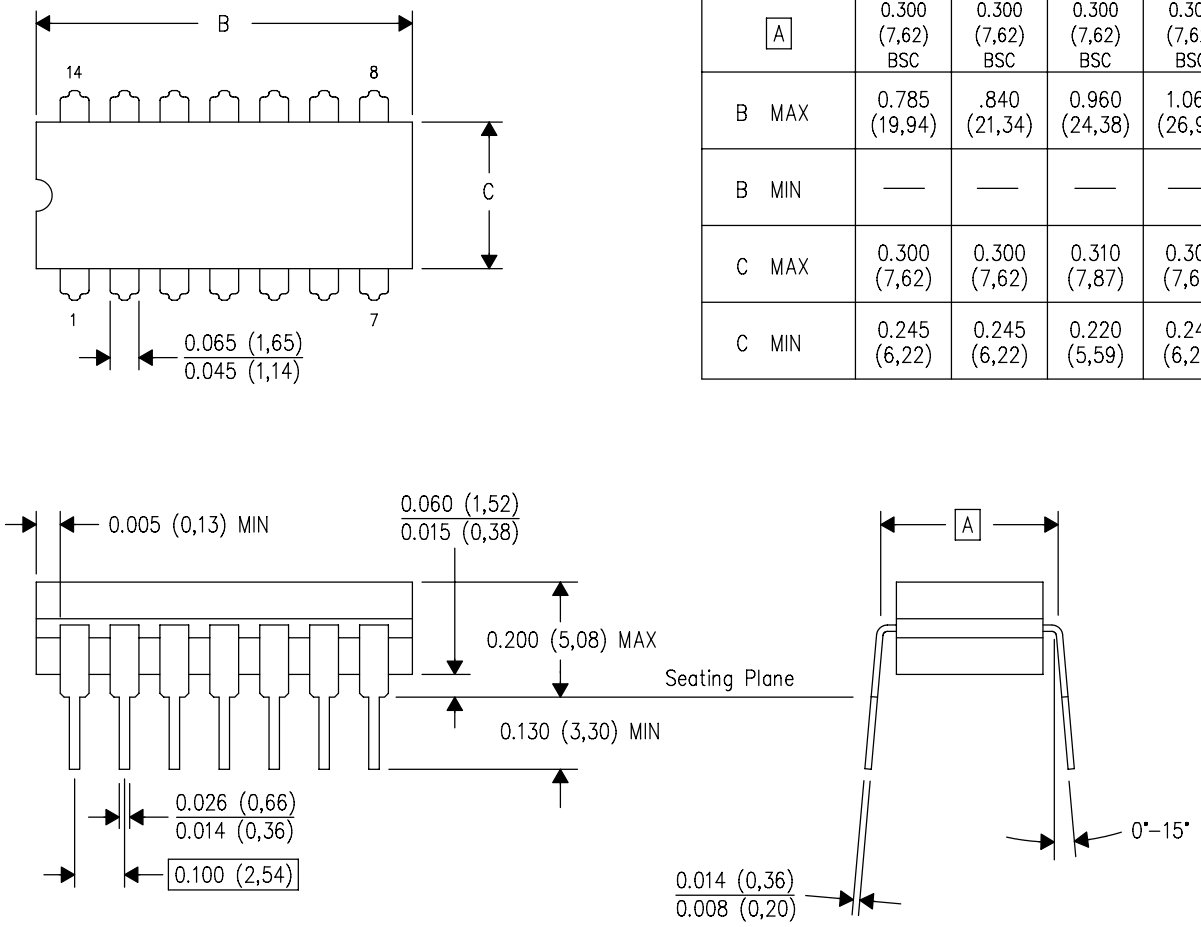
DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

J (R–GDIP–T**) CERAMIC DUAL IN–LINE PACKAGE

14 LEADS SHOWN

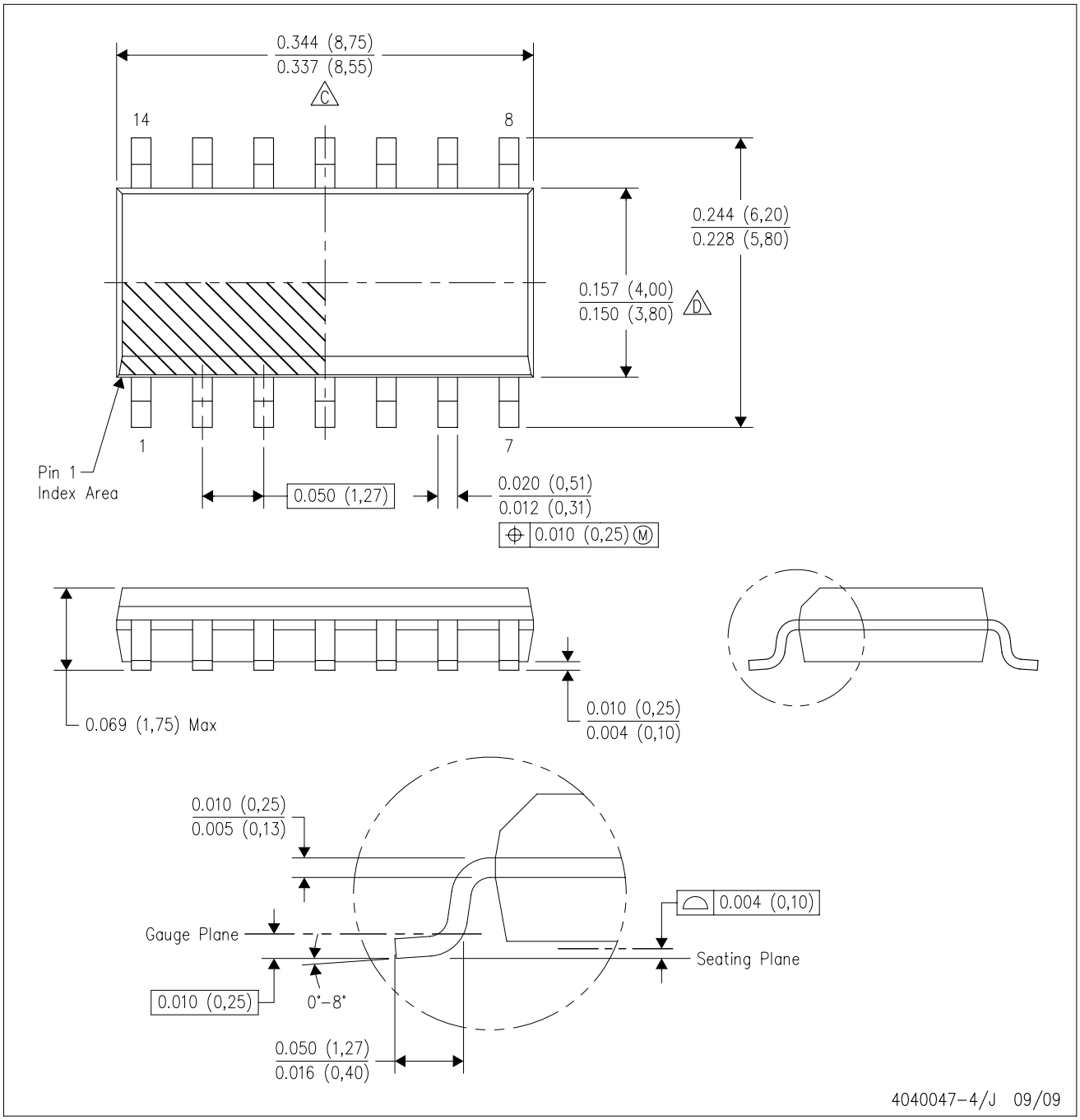


DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

4040083/F 03/03

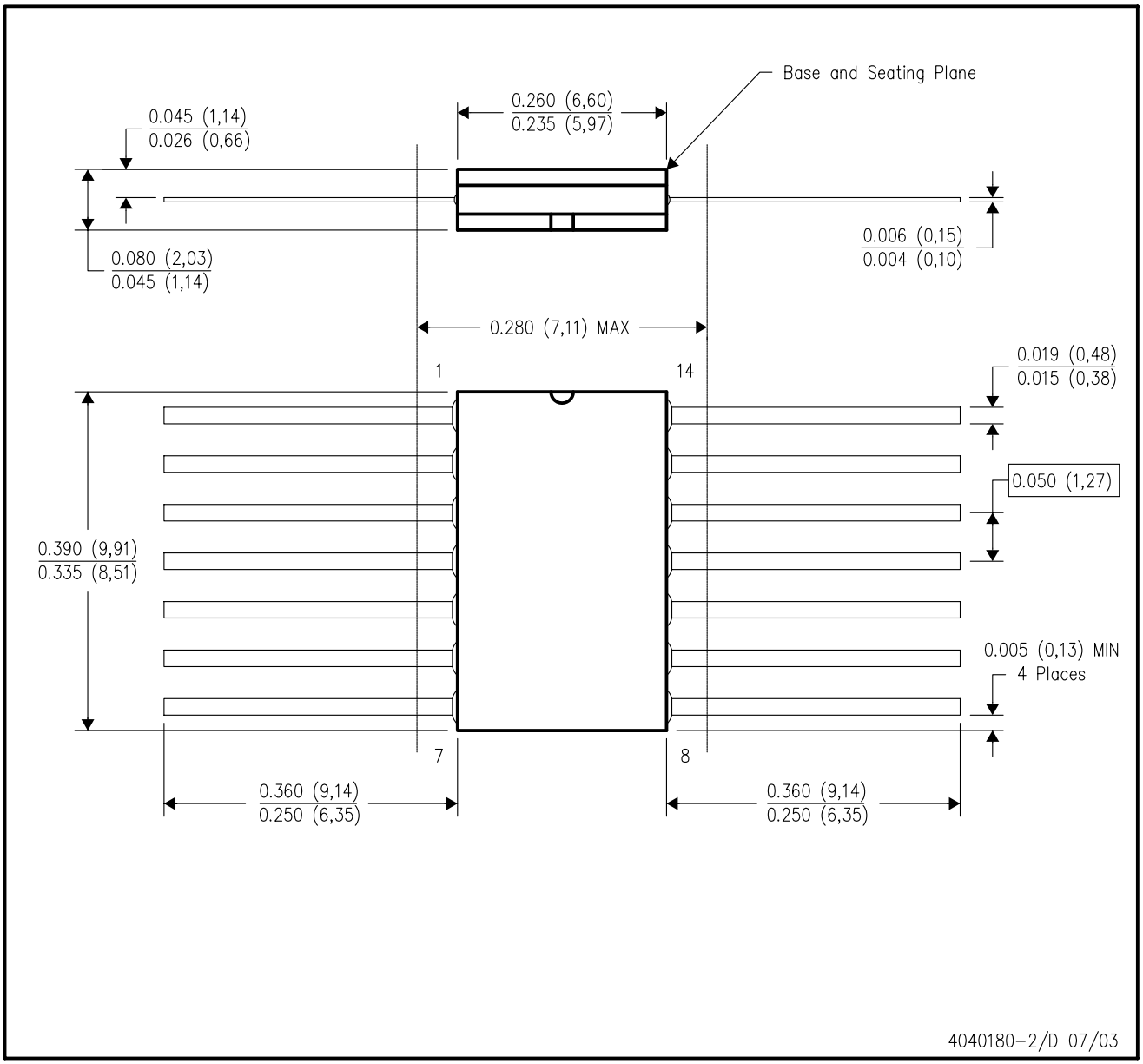
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

D (R–PDSO–G14) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AB.

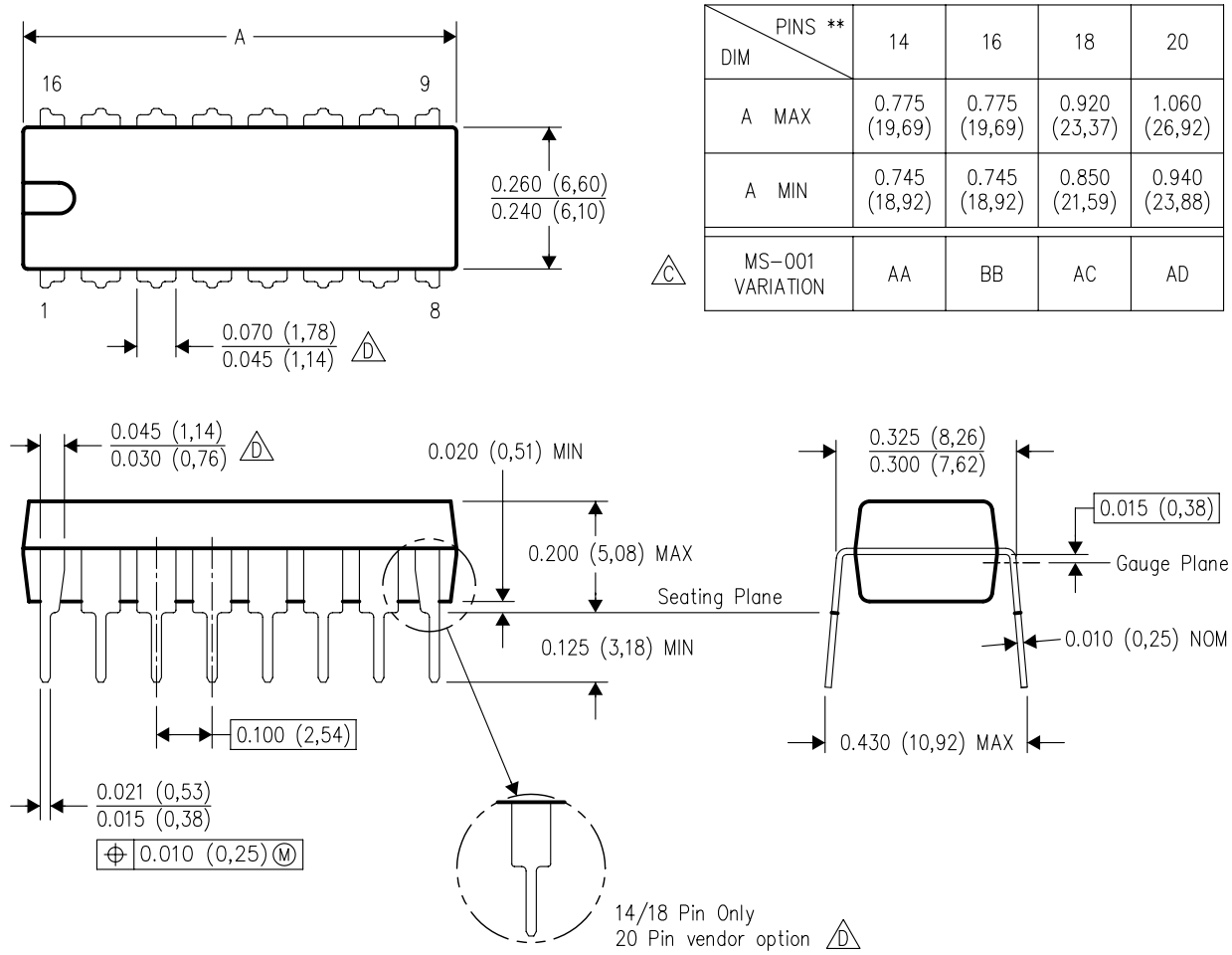
W (R–GDFP–F14) CERAMIC DUAL FLATPACK



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14 and JEDEC MO–092AB

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DLP® Products	www.dlp.com	Broadband	www.ti.com/broadband
DSP	dsp.ti.com	Digital Control	www.ti.com/digitalcontrol
Clocks and Timers	www.ti.com/clocks	Medical	www.ti.com/medical
Interface	interface.ti.com	Military	www.ti.com/military
Logic	logic.ti.com	Optical Networking	www.ti.com/opticalnetwork
Power Mgmt	power.ti.com	Security	www.ti.com/security
Microcontrollers	microcontroller.ti.com	Telephony	www.ti.com/telephony
RFID	www.ti-rfid.com	Video & Imaging	www.ti.com/video
RF/IF and ZigBee® Solutions	www.ti.com/lprf	Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2009, Texas Instruments Incorporated