The University of New South Wales

School of Electrical Engineering and Telecommunications

ELEC2141: Digital Circuit Design

Final Examination

Session 1, 2016

- Reading time: 10 minutes.
- Time allowed: 3 hours.
- This paper contains 5 questions on 8 total pages.
- Total marks available: 100.
- This final examination contributes 60% to the total course assessment.
- All questions are of equal value. Part marks are as indicated.
- Answer all questions.
- Answer each question in a separate answer booklet.
- Write the question number attempted on the cover of each answer booklet.
- The exam paper may be retained by the candidate.
- Authorized examination materials: University approved calculators.
- Any assumptions found to be necessary in answering the questions should be stated explicitly.
- All answers must be written in ink. Except where they are expressly required, pencils may be used only for drawing, sketching or graphical work.

Question 1. (20 marks)

i) Consider the following Boolean function F:

F(A,B,C,D) = $AC\left(\overline{B}+D\right)+\overline{A}C\left(\overline{B}+\overline{D}\right)+BC(\overline{A}+\overline{D}\,)$

a) Assuming that the function F is implemented using basic logic gates (NOT, AND and NOR gates), find the total gate input-cost of the implementation. **[1 mark]**

b) Draw the truth table for the function F. **[2 marks]**

c) Express the function F as a Sum-of-Minterms (you may use the "little m" short cut notation). **[2 marks]**

d) Express the function F as a Product-of-Maxterms (you may use the "big M" short-cut notation) **[2 marks]**

e) Simplify the function F using Karnaugh map and express it as the Sum-of-Products. List all prime implicants and essential prime implicants. **[4 marks]**

f) Simplify the function F using Karnaugh map and express it as the Product-of-Sums. **[3 marks]**

g) Using your minimal Sum-of-Products expression from part (e), draw the logic diagram (circuit) using NAND gates only. Assume no complemented signals are available. **[2 marks]**

h) For your design in part (g), find the reduction in the total gate-input cost as compared to the implementation in part (a). **[1 mark]**

ii) Convert (23B4.A5) in base 12 number system to a base 5 number system. **[3 marks]**

Question 2. (20 marks)

Consider the synchronous sequential circuit, which is based on T flip flops (TFF), as shown in Fig. 1.

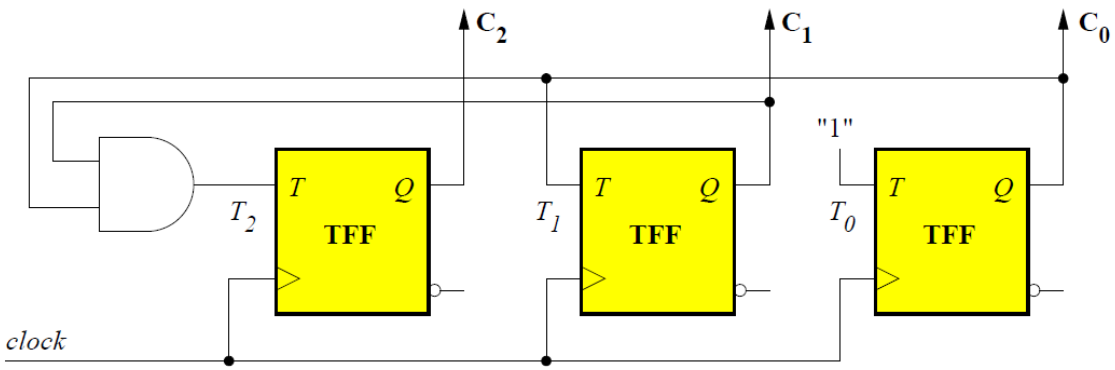


Fig. 1: Synchronous sequential circuit

i) Derive the state table and draw the state diagram for the circuit shown above. The outputs of the system are C_2, C_1 and C_o. You can treat C_o as the least significant bit. **[6 marks]**

ii) Specify the type of the state machine described by the circuit shown in Fig. 1**.** **[2 marks]**

iii) Based on your answer in (i), what does this circuit implement? **[3 marks]**

iv) Redesign the circuit using JK flip flops (JKFF) **[6 marks]**

v) With the initial state 110, find the output of the system after 20 clock cycles. **[3marks]**

Question 3. (20 marks)

i) Design a sequential binary subtractor. Two binary sequences of an arbitrary length, corresponding to the two operands for the subtraction operation, are applied to the inputs A and B, where the least-significant bit (LSB) of each sequence arrives first. The binary difference of the two numbers is produced as a corresponding output time sequence on the output Z, where the LSB is delivered first. You may assume input A as minuend and B as subtrahend.

a) Derive the state diagram for a Mealy-type system. **[3 marks]**

b) Implement the state diagram in (a) using D flip-flops and whatever combinational gates you may need and sketch neatly the resulting circuit. **[4 marks]**

c) Write a Verilog HDL structural description of your circuit in (b) **[3 marks]**

d) Derive the state diagram for a Moore-type system. **[4 marks]**

ii) In a bit serial design, a less than operation is needed. Fig. 2 shows the representation of the bit serial architecture. The required logic block is labeled with < symbol. The block takes the registers A and B in a serial fashion with least significant bit first. The less than block (<) takes inputs from register A and B and a third input C from a single bit register. There is a signal LSB which indicates the start of the operation, which is used to either set or reset the register that holds the C value.

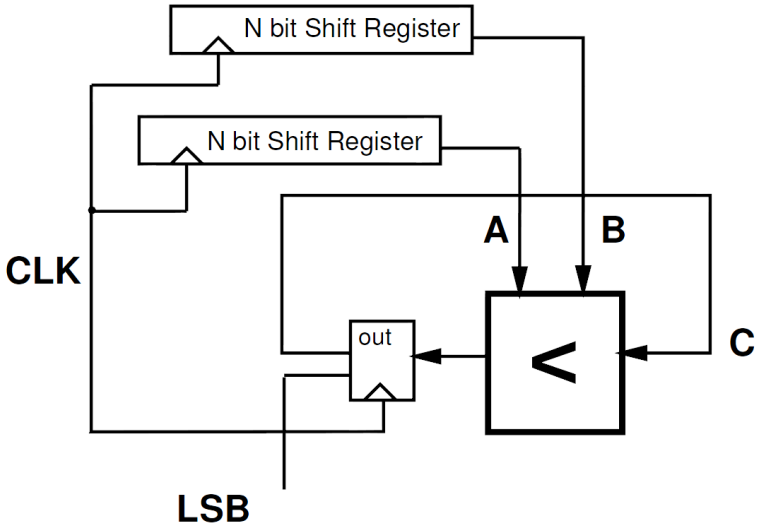


Fig. 2: Representation of bit serial less than block digital circuit

a) Should C be set HIGH or LOW at the start of operation for the correct operation of your less than block? **[2 marks]**

b) Design a logic circuit using NAND gates only for the less than block that can compare register A and B setting C HIGH if A is less than B else setting C LOW. The comparison assumes the contents of the registers are unsigned. You must ensure that your design is optimized. **[4 marks]**

Question 4. (20 marks)

i) Consider the following Verilog HDL code

```
module seq_det (CLK, RESET, X, Z);
 input CLK, RESET, X;
 output  Z;
 reg  [1:0]  state, next-state;
 parameter  A= 2'b00,  B=2'b01,  C=2'b10, D= 2b'11;
 reg Z;

always @ (posedge CLK or posedge RESET)
begin
    if  (RESET == 1)
       state <= A;
   else
     state <= next_state;
 end

always @ (X or state)
      begin
       case (state)
            A:   if (X)  next_state = B; else next_state = A;
            B:   if (X)  next_state = D; else next_state = A;
            C:   if (X)  next_state = C; else next_state = A;
            D:   if (X)  next_state = C; else next_state = A;
       endcase
      end

always @ (X or state)
      begin
       case (state)
            A:  Z = 0;
            B:  Z =  X? 0:1;
            C:  Z =  X? 0:1;
            D:  Z =  X? 0:1;
       endcase
      end
 endmodule
```

a) What type of sequential circuit is described by the above Verilog HDL code? **[2 marks]**

b) Suppose the above Verilog HDL code is synthesized using an appropriate CAD tool. Draw the possible synthesized circuit. **[4 marks]**

c) With initial state of B, find the sequences of the output for an input sequences of 0101100 **[2 marks]**

ii) Given $AB = 0$ and $A + B = 1$, use Boolean algebraic manipulation to prove that

$$\bar{A}(B + C)(\bar{A} + B)(\mathrm{A} + \mathrm{B}) = BC$$

[4 marks]

iii) Suppose you are given a task to design a 9-to-512-line decoder using only two input AND and NOT gates, outline the procedure you will follow and indicate the total gate input cost of your design.

[4 marks]

iv) Consider the following Verilog HDL code

```
module Unknown_beh (
 output  reg   [3:0]   A,
 input         [3:0]   I,
 input         s1,s0,D,E,CLK,C

 );
always @ (posedge CLK, negedge C)
  if (C == 0)  A <= 4'b0000;
  else
    case ({s1,s0})
      2'b00:  A <= A;
      2'b01:  A <= {D, A[3:1]};
      2'b10:  A <= {A[2:0],E};
      2'b11:  A <= I;
    endcase
endmodule
```

a) What is the digital circuit described by the code? **[2 marks]**

b) Is this a Mealy or a Moore type system? **[2 marks]**

Question 5. (20 marks)

i) Design a combinational circuit whose input is a 4-bit number and whose output is the 2s complement of the input number.

   a) Implement your design using only XOR and AND logic gates. Inverters are not available.
   [4 Marks]

   b) Implement your design using at least one functional block (decoder, multiplexer etc) and any number of logic gates of your choice. You only need to show the implementation for the most significant output bit.
   [2 marks]

   c) Implement your design using a CMOS complex gate. You only need to show the implementation for the most significant output bit. **[3 marks]**

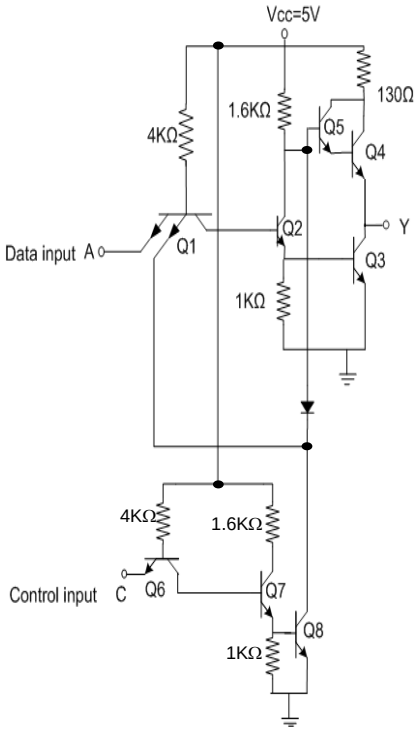
ii) Redesign the combinational circuit in (i) as a sequential 2s complement generator. The generator takes in the binary input number as a sequence of bits with Least Significant Bit (LSB) arriving first and generates the 2s complement output number also as a sequence of bits with LSB being delivered first. Show your implementation using D-flip flop and any other gates of your choice.
[4 Marks]

iii) Consider the following 16-bit long binary codes stored in register R1 and R2 of a 16-bit microprocessor datapath

R1 = 0x8F15
R2 = 0xAB97

Assuming that the binary codes expressed as hexadecimal values above are in 2s complement binary formats and a 16-bit binary addition of the two registers is performed by the micro-processor. Determine the values of the status flags V, N, Z, and C of the micro-processor.
[4 marks]

iv) Fig. 3 is a TTL gate. List the state of each transistor (OFF or ON) and the output (Y) in each of the following conditions: (a) when C is low and A is low; (b) when C is low and A is high; and (c) when C is high.



[3 marks]

Fig. 3 : TTL gate

END OF EXAMINATION PAPER