SCHOOL OF ELECTRICAL ENGINEERING & TELECOMMUNICATIONS

ELEC2141 – DIGITAL CIRCUIT DESIGN

MID-TERM ONLINE EXAMINATION (Version A)

TERM 1, 2020

- Time allowed: 1 hour 10 minutes in total. The time includes reading time and preparation time for submission.
- This paper contains 2 questions on the 2 following pages.
- Total marks available: 100.
- This mid semester examination contributes 15% to the total course assessment.
- All questions are of equal value. Part marks are as indicated.
- Answer all questions.
- All answers must be written clearly in ink on clean sheets of A4 paper (lined paper is also allowed).
- Write down the version of your examination (Version A) on the first page of your answering sheet.
- This is an open-book exam. You may reference to the lecture notes or online materials.
- The exam paper can be saved on your computer for later reference.
- Any assumptions found to be necessary in answering the questions should be stated explicitly.
- Scanned or photographed answers must be readable. Unclear answers will not be marked.
- Acceptable submission file types: .pdf, .doc, docs, jpeg, jpg, png.
- Do not submit more than 20 files.
- Candidates must retain the original answers as proof, if requested.

Question 1 (50 marks)

a) Consider the following Boolean function F:

$$F(A,B,C,D) = \bar{A}(CD + \bar{D}) + A(\bar{B}\bar{C} + C\bar{D})$$

Assuming that the function F is implemented using basic logic gates (NOT, AND and OR gates),

i. Find the total gate input-cost of the implementation. **[3 marks]**

ii. Express the function F as a Sum-of-Minterms (you may use the "little m" short cut notation). **[4 marks]**

iii. Draw the truth table for the function F. **[4 marks]**

iv. Simplify the function F using a Karnaugh map and express it as the Sum-of-Products. List all prime implicants and essential prime implicants. **[6 marks]**

v. Express the function F as a Product-of-Sums. List all prime implicants and essential prime implicants. **[6 marks]**

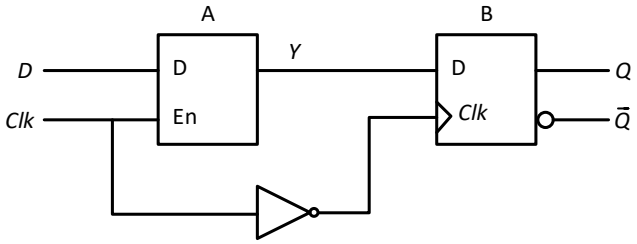
vi. For your design in part (iv), find the reduction in the total gate-input cost as compared to part (i). **[3 marks]**

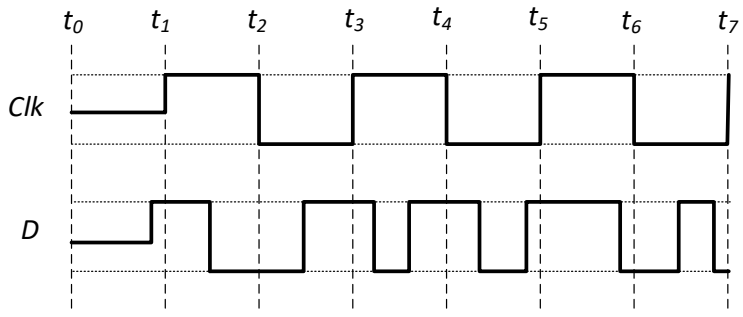
vii. Using your minimal Sum-of-Products expression from part (iv), draw the logic diagram (circuit) using NOT, AND and OR gates. **[5 marks]**

b) Convert the numbers in the table below from the given base to the other two bases. Limit the number of digits in the fraction part to three for the binary form. Show all your workings. **[9 marks]**

binary	hexadecimal	octal
		654.7

c) Assuming that the D and Clk inputs shown in the diagram below are applied to the circuit, draw the waveforms for Y and Q. What is the name of storage element A and storage element B? **[10 marks]**





Question 2 (50 marks)

a)

i. Using Boolean algebra, prove the identity: **[3 marks]**

$$X + Y = X \oplus \mathrm{Y} + XY$$

ii. Therefore, or otherwise, find an expression for the function

$$H(A, B, C) = A\bar{B} + AB\bar{C} + \bar{A}B$$

which uses only XOR and AND gates. **[4 marks]**

b) Consider the following Boolean function G:

$$G(A, B, C, D) = \Pi M(3,4,7,11,12,13,14,15)$$

i. Using Boolean algebraic manipulation, show that the optimised expression is $G = \bar{B}\bar{D} + \bar{A}\bar{C}D + A\bar{B}\bar{C} + \bar{A}C\bar{D}$. **[13 marks]**

ii. Implement the logic circuit of (i) using NAND only gates, assuming no complemented signals are available. **[5 marks]**

c) Design a digital system with the following characteristics and criteria. There are four inputs (*A, B, C, D*) and one output (*Z*) to the system. The output *Z* is true (i.e. logic "1") when the 4-bit binary value *ABCD* is less than or equal to 7 and the binary input value is odd. When the binary value of *ABCD* is greater than 7, the *Z* follows the result of the expression $B \oplus C$. You can assume A is the most significant bit and *D* is the least significant bit.

i. Draw the truth table for the four inputs (*A, B, C, D*) and output (*Z*). **[8 marks]**

ii. Express the function *Z* as a sum-of-minterms (you may use the "little m" notation). **[4 marks]**

iii. Implement the Boolean function with a 4x1 multiplexer and minimum number of 2-input external gates and inverters only. Do not assume that complements are available. **[6 marks]**

d) Design a 4-to-X line decoder, where X is the number of outputs of the decoder. Assume input A_0 is the least significant bit and A_3 is the most significant bit. Design the decoder that takes BCD inputs of 0 to 11 using the minimum number of two input AND and NOT gates (You may use block diagrams- drawing logical gates is not required). Outline the design procedure you may follow and label all inputs and outputs of the decoder. Indicate the total gate input cost of your design. **[7 marks]**

END OF EXAMINATION PAPER