The University of New South Wales

ELEC2141: Digital Circuit Design

Tutorial Week 10 – Digital IC Logic Families

1. Following are the specifications for the Schottky TTL 74S00 quadruple two-input NAND gates:

Parameter	Name	Value
VCC	Supply Voltage	5V
ICCH	High-level supply current (four gates)	10mA
ICCL	Low-level supply current (four gates)	20mA
VOH	High-level output voltage (min)	2.7V
VOL	Low-level output voltage (max)	0.5V
VIH	High-level input voltage (min)	2V
VIL	Low-level input voltage (max)	0.8V
IOH	High-level output current (max)	1mA
IOL	Low-level output current (max)	20mA
IIH	High level input current(max)	0.05mA
IIL	Low level input current (max)	2mA
tPLH	Low-to-high delay	3ns
tPHL	High-to-low delay	3ns

   Calculate the fan-out, power dissipation, propagation delay, and noise margin of the Schottky NAND gate.

2.
   a. Determine the high-level output voltage of the RTL gate for a fan-out of 5.
   b. Determine the minimum input voltage required to drive an RTL transistor to saturation when hfe = 20.
   c. From the results in parts (a) and (b), determine the noise margin of the RTL gate when the input is high and the fan-out is 5.
3. Show that the output transistor of the DTL gate given in Fig. 1 goes into saturation when all inputs are high. Assume that hfe = 20.

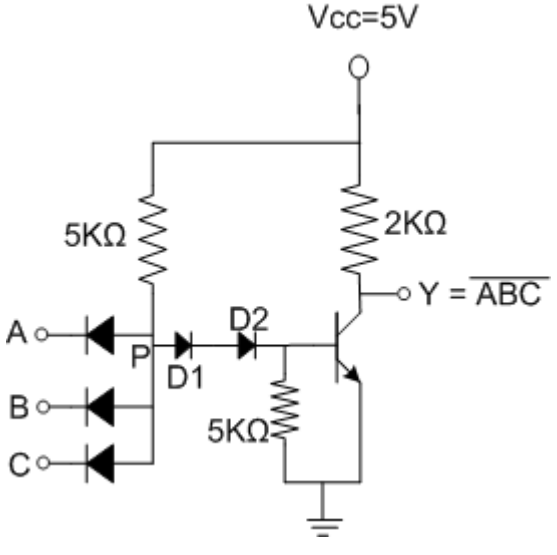

Fig. 1

4. Connect the output Y of the DTL gate (Fig. 1) to N inputs of other, similar gates. Assume that the output transistor is saturated and its base current is 0.44mA. Let hfe = 20.
    a. Calculate the current in the 2-KΩ resistor.
    b. Calculate the current coming from each input connected to the gate.
    c. Calculate the total collector current in the output transistor as a function of N.
    d. Find the value of N that will keep the transistor in saturation.
    e. What is the fan-out of the gate?
5. Let all inputs in the open-collector TTL gate given in Fig. 2 be in the high state of 3V.
    a. Determine the voltages in the base, collector, and emitter of all transistors in the circuit.
    b. Determine the minimum hfe of Q2 which ensures that this transistor caturates.
    c. Calculate the base current of Q3.
    d. Assume that the minimum hfe of Q3 is 6.18. What is the maximum current that can be tolerated in the collector to ensure saturation of Q3?
    e. What is the minimum value of RL that can be tolerated to ensure saturation of Q3?

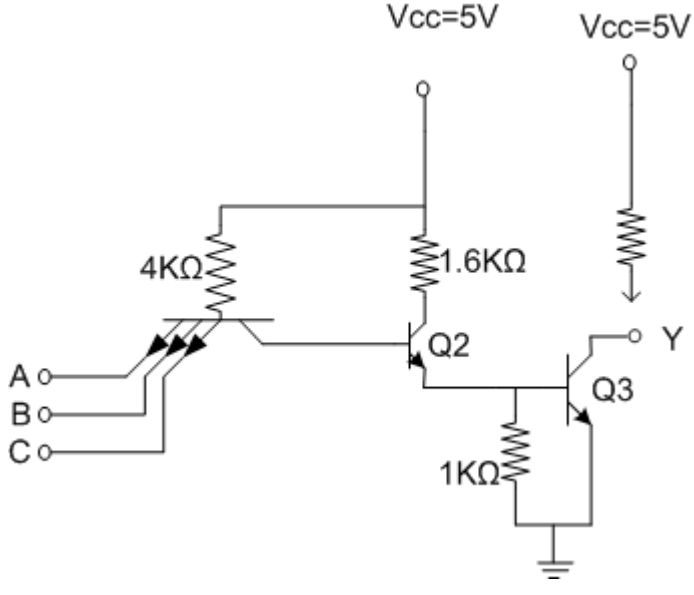

Fig 2

6. For the following conditions, list the transistors that are off and the transistors that are conducting in the three-state TTL gate of Fig. 3 (for Q1 and Q6, it is necessary to list the states in the base-emitter and base-collector junctions separately):
    a. When C is low and A is low.
    b. When C is low and A is high.
    c. When C is high.

    What is the state of the output in each case?

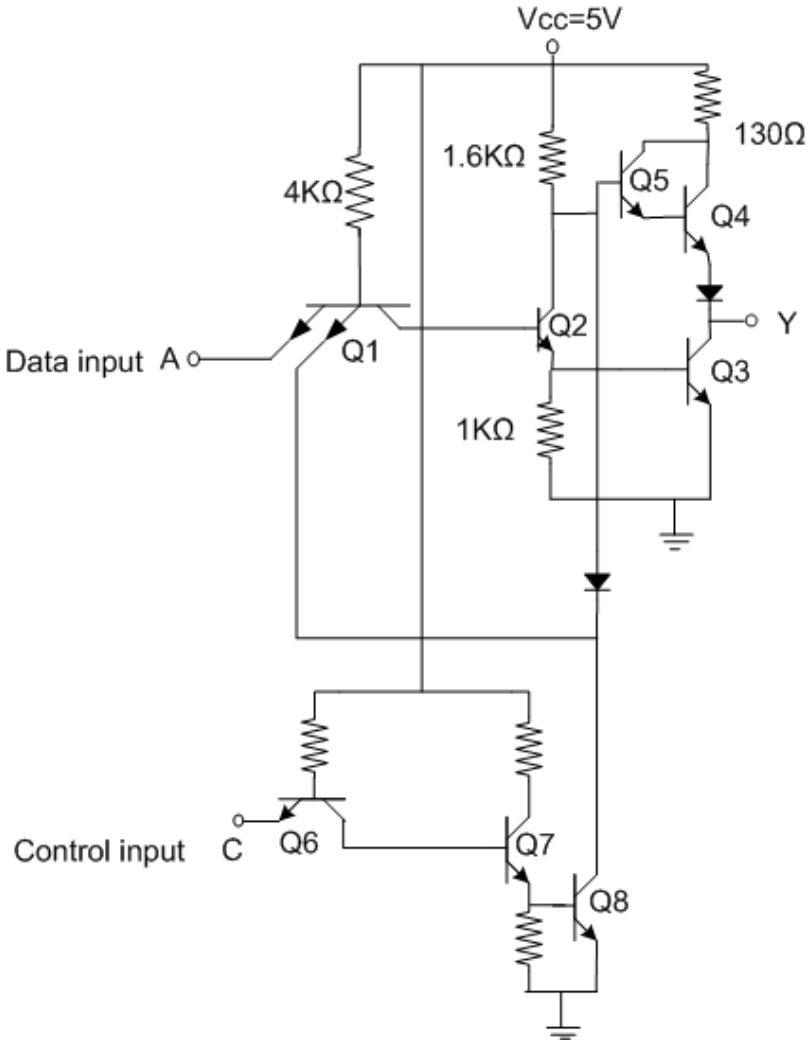

Fig. 3

7. Find the logic function realized by the following CMOS circuit in Fig. 4.

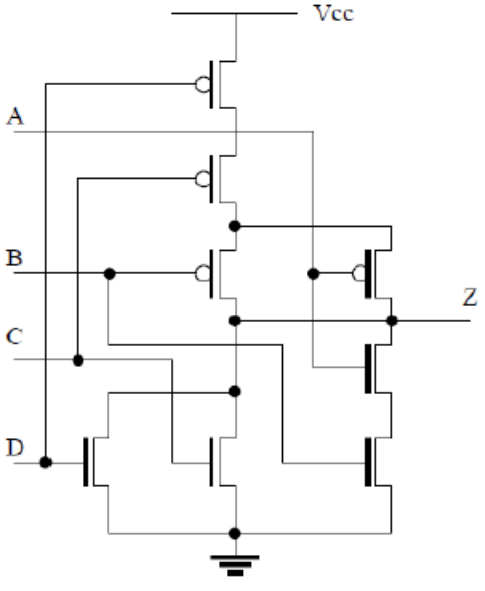

Fig. 4

8. Derive a CMOS complex gate for each of the following functions:

    a. $F = XY + XZ$
    b. $F = XY + XZ + YZ$
    c. $F = \overline{XY + WZ}$
    d. $F = A \oplus B \oplus C$

9. Find the CMOS complex gate circuit for each of the following functions. In each case, use a minimum number of transistors.

    a. $F(X, Y, Z) = YZ + \bar{X}Z + \bar{X}Y\bar{Z}$
    b. $F(A, B, C, D) = A\bar{D} + A\bar{B} + BD + BC$

10. Find the CMOS complex gate circuit for each of the following functions:

    a. $F(A, B, C, D) = (A + \bar{C})(\bar{A} + C)(B + \bar{D})(\bar{B} + D)$
    b. $F(W, X, Y, Z) = \sum m(4,7,9,11,12,13,14,15) + d(3, 10)$

11. Construct a 4-to-1-line multiplexer using transmission gates and inverters.