Assignment marking guideline:

Assignment I has two design problems. Each of them will be marked out of 50. The marking breakdown is outlined below

1. Design approach: (10 marks)
    - Explain clearly the design approach (are you using functional blocks? hierarchical design? Five or four variable k-maps?) (4)
    - Any assumptions made must be explicitly stated (1)
    - You may concisely re-write the specification including your design assumptions if needed (5)
2. Formulation: (10 marks)
    - Draw any truth table required and clearly indicate input and output columns (10)
        - If appropriate "Do not care conditions" are not used, two marks will be deducted
        - Wrong Truth table – deduct 5 marks
    - Show any hierarchical block diagram if used.
    - If Boolean function is generated directly from the specification, explain how you arrive at the Boolean function and clearly indicate the function. (10)
        - Boolean function – 5 marks
        - Correct explanation – 5 marks
3. Optimization: (10 marks)
    - Show all K-maps used and indicate clearly which essential prime implicates or prime implicates are selected in your optimized Boolean expression (8)
        - If the Boolean expression is not correct or not optimized correctly, 1mark will be deducted per expression
    - If multi-level circuit implementation is employed, show the optimization steps
    - Indicate GIC of your optimized design (2)
4. Circuit implementation (10 marks)
    - Draw logic diagram. It has to be neat and clearly labelled (inputs and outputs) (7)
    - Indicate clearly your particular choice of implementation (NAND only, NOR only etc) (3)
5. Verification (10 marks)
    - Draw the schematics of your implementation in Xilinx ISE
    - Write the Verilog test file (attach the file). (5)
    - Include the simulation result from Xilinx (attach the file). It has to clearly show the waveforms for all inputs and output. (5)