The University of New South Wales

School of Electrical Engineering and Telecommunications

ELEC2141: Digital Circuit Design

Final Examination

Session 1, 2010

- Time allowed: 3 hours.
- This paper contains this page and FIVE (5) Questions on 5 other pages.
- Total marks available: 100.
- All questions are of equal value. Part marks are as indicated.
- **Answer all questions.**
- Answer EACH question in a SEPARATE book.
- Write your student name and number at the top of the pink answer page attached to this paper.
- The exam paper may be retained by the candidate.
- Authorized examination materials: University approved calculators.
- Any assumptions found to be necessary in answering the questions should be stated explicitly.
- All answers must be written in ink. Except where they are expressly required, pencils may be used only for drawing, sketching or graphical work.

Question 1. (20 marks)

i) Consider the Boolean function:

$$F(W, X, Y, Z) = \sum m(0, 1, 3, 6, 7, 8, 9, 11, 12, 14)$$

a) Draw the Karnaugh map for the function *F*. **[1 mark]**

b) List all of the prime implicants of *F*. **[2 marks]**

c) List all of the essential prime implicants of *F*. **[2 marks]**

d) Find a minimal Sum-of-Products expression for *F*. **[1 mark]**

e) Using factorization, find an expression for *F* which minimizes the gate-input cost of the function. **[1 mark]**

f) Calculate the gate-input cost (inverters included) of the expression found in part (e). **[2 marks]**

ii) Using Boolean algebra, prove the identity:

$$A\bar{B}\bar{C} + ABD + \bar{A}BC + \bar{B}C\bar{D} = A\bar{B}\bar{D} + A\bar{C}D + BCD + \bar{A}C\bar{D}$$

[5 marks]

iii) For the following addition operation, between two 16-bit numbers (represented in Hexadecimal notation), where the numbers are interpreted as <u>signed</u> values:

0x8A42 + 0xD957

a) Derive the 16-bit result and express it in Hexadecimal notation. **[2 marks]**

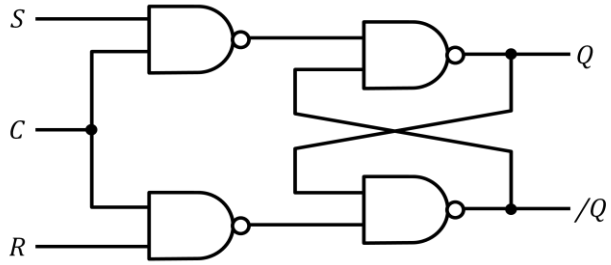
b) Determine whether an overflow occurred, stating the reasoning for your answer. **[2 marks]**

iv) List one advantage and one disadvantage of a Carry-Lookahead Adder over a Ripple-Carry Binary Adder. **[2 marks]**

Please turn over - Question 2 on next page.

Question 2. (20 marks)

Consider the following logic diagram for an SR-Latch with Control:

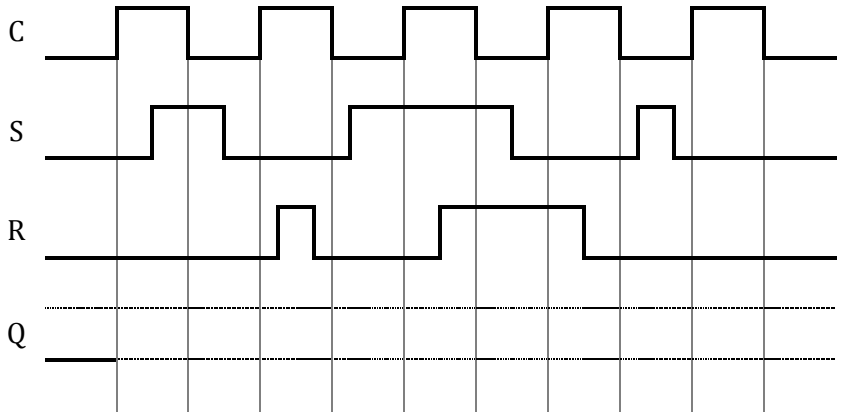


i) Write the corresponding function table for all input combinations. **[3 marks]**

ii) Describe what sequence of inputs would lead to a race-condition and explain how this may settle to an unknown outputs state. **[3 marks]**

iii) By using the SR-Latch above as a building block, draw the logic diagram for a Master-Slave SR Flip-Flop, indicating the inputs and outputs clearly. In your diagram, you may use the standard symbol for an SR-Latch with Control. **[3 marks]**

iv) For a Master-Slave SR Flip-Flop, carefully draw the output waveform, *Q*, obtained in response to the given input waveforms. The answer to this part **must** be drawn on the pink page attached to the examination paper. **[5 marks]**



v) Using a diagram, show how you would modify the Master-Slave SR Flip-Flop in order to obtain a Positive Edge-Triggered D Flip-Flop. **[3 marks]**

vi) Explain how a D Flip-Flop solves the race-condition problem and hence avoids an unknown outputs state. **[3 marks]**

Please turn over - Question 3 on next page.

Question 3. (20 marks)

A synchronous sequential circuit has one input *X*, and one output *Z*. The output becomes 1 if and only if just one of three (3) bits, which include the present input bit and the last two (2) input bits, is a 1. For example, a possible input/output sequence may be:

X:	0	0	1	0	1	1	0	0	1	1	1	0	0	1	0	1	0	0	1	1
Z:	X	X	1	1	0	0	0	1	1	0	0	0	1	1	1	0	1	1	1	0

i) Derive a state diagram for the desired machine, indicating clearly what each state represents. State whether your machine is a Mealy or Moore machine.
Hint: Using a minimal Mealy machine, you can do this with four (4) states; however solutions with more states are possible. **[8 marks]**

ii) Demonstrate the sequence of states and outputs when the input sequence is 010010110010. **[4 marks]**

iii) Suppose that the design specification has changed. Now, the output is to become 1 if and only if just one of the following three (3) bits is a 1: the present input bit and the last two (2) output bits. Again for example, a possible input/output sequence may be:

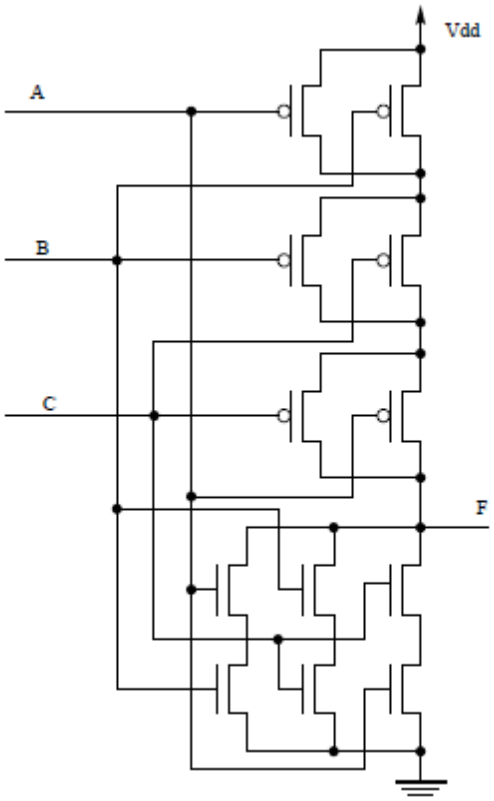
X:	X	X	0	0	1	0	1	1	0	1	1	0	0	0	1	0	1	1	0	
Z:	1	1	0	1	0	1	0	0	0	1	0	1	1	0	0	0	1	0	1	

Derive a new state diagram for the altered machine. **[8 marks]**

Please turn over - Question 4 on next page.

Question 4. (20 marks)

i) Consider the following CMOS circuit:



a) Find the truth table corresponding to the function *F* implemented by the circuit. **[3 marks]**

b) Determine the equations of the pull-up network and the pull-down network for the function *F*. Using Boolean algebra show that these equations are equivalent. **[3 marks]**

c) Draw the logic diagram for a NOR-only implementation for *F*. Assume the signals *A*, *B*, and *C* are available, as well as the power rails (V_{DD} and GND). You may use only NOR gates of two or more inputs. **[6 marks]**

ii) Using transmission-gates and any additional MOS transistors, implement a 2-to-1-Line Multiplexer. **[4 marks]**

iii) Draw the circuit which represents the function $F = AB + C$ using MOS transistors. **[4 marks]**

Please turn over - Question 5 on next page.

Question 5. (20 marks)

Consider the following Verilog program, which implements a synchronous sequential circuit:

```
module ssc(CLK, X, Z);
      input CLK, X;
      output Z;
      reg [2:0] state;
      parameter  A = 3'b000, B = 3'b001, C = 3'b010,
                 D = 3'b011, E = 3'b100, F = 3'b101;

      always @(posedge CLK) begin
            case (state)
                  A: state <= X ? B : A;
                  B: state <= X ? D : E;
                  C: state <= X ? B : D;
                  D: state <= X ? B : C;
                  E: state <= X ? F : B;
                  F: state <= X ? C : E;
            endcase
      end

      always @(state) begin
            case (state)
                  A, C, D, F: Z <= 0;
                  B, E:       Z <= 1;
            endcase
      end
endmodule
```

i) Determine whether this code implements a Mealy machine or a Moore machine. **[1 mark]**

ii) Write the state transition table for the machine. **[4 marks]**

iii) Minimize the number of states and derive the reduced state transition table (*Hint*: this can be done using four states). **[6 marks]**

iv) Convert the reduced machine to its alternate type. That is, if it is a Mealy machine, convert it to a Moore type or vice-versa. Describe the machine using both a state transition table and a state diagram. **[6 marks]**

v) Using the state diagram obtained in part (iv), and starting from the equivalent state to State A in the Verilog program, write the sequence of outputs corresponding to the input sequence 1010100100. **[3 marks]**

End of paper.