The University of New South Wales

ELEC2141: Digital Circuit Design

Tutorial Week 5 – Midterm review

1. Convert the numbers in the table below from the given base to the other bases. Limit the number of digits in the fraction part to six for the binary form. Show all your workings.

binary	decimal	base-5	hexadecimal	octal
			3D5.E	
	782.25			

2. Simplify the following Boolean functions using algebraic manipulation to a minimum number of literals

   i. $F(A,B,C) = A \oplus B \oplus C + \bar{A}\bar{B}\bar{C} + \bar{A}BC + A\bar{B}C + AB\bar{C}$

   ii. $G(A,B,C,D) = ABD + A\bar{B}\bar{C} + A\bar{B}C\bar{D}$

3. Consider the following Boolean function F:

$$F(A,B,C,D) = (\bar{A} + \bar{B} + D)(\bar{A} + \bar{D}) + AC + BD$$

   Assuming that the function F is implemented using basic logic gates (NOT, AND and OR gates),

   i. Find the total gate input-cost of the implementation

   ii. Express the function F as a sum-of-minterms

   iii. Simplify the function F using a Karnaugh map and express it as the sum-of-products. List all prime implicants and essential prime implicants

   iv. Express the function as a product-of-sums

   v. For your design in part (iii), find the reduction in the total gate input cost as compared to part (i)

   vi. Draw the logic circuit using NAND only gates assuming no complemented signals are available

4. Design a combination circuit which can detect prime numbers from 0 to 15. There should be a single output line, which is 1 if the input is a prime number, otherwise the output line would be 0.

   i. Implement the function with a 4-to-16-line decoder and OR gates.

   ii. Implement the function with a 4x1 multiplexer and the minimum number of 2-input external gates and inverters only. Do not assume that complements are available

5. Design a circuit to implement the following pair of Boolean equations, using factoring to simplify.

$$X = ADF + AEF + BDF + BEF + CDF + CEF$$
$$Y = A\bar{D}\bar{E} + B\bar{D}\bar{E} + C\bar{D}\bar{E}$$

   Draw the final logic diagram for the overall circuit diagram and compare the gate input cost to the SOP form of circuit given above.

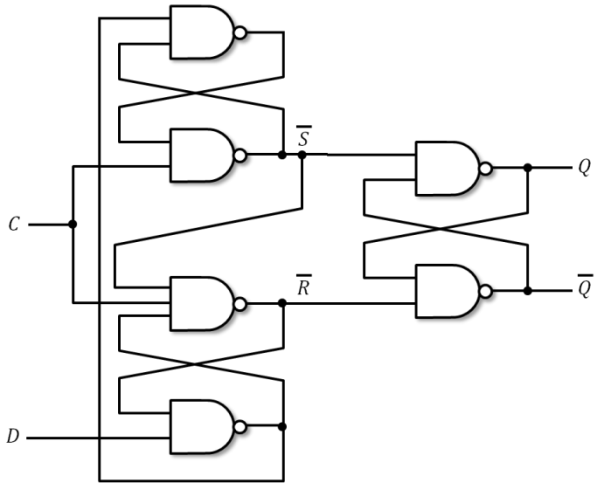
Where referenced, questions are taken from the textbook:

M. Mano, C. R. Kime and T. Martin, Logic and Computer Design Fundamentals, 5th Edition (Global Edition), Pearson, 2016

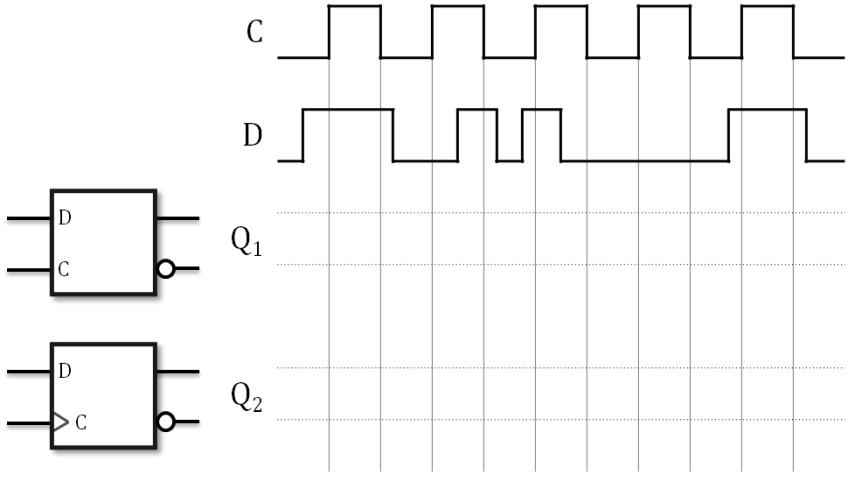
6. Implement the function below using XOR and AND gates only. Then construct the circuit using interconnecting three-state buffers and inverters.

$$H = A\bar{B}C\bar{D} + \bar{A}BC\bar{D} + A\bar{B}\bar{C}D + \bar{A}B\bar{C}D$$

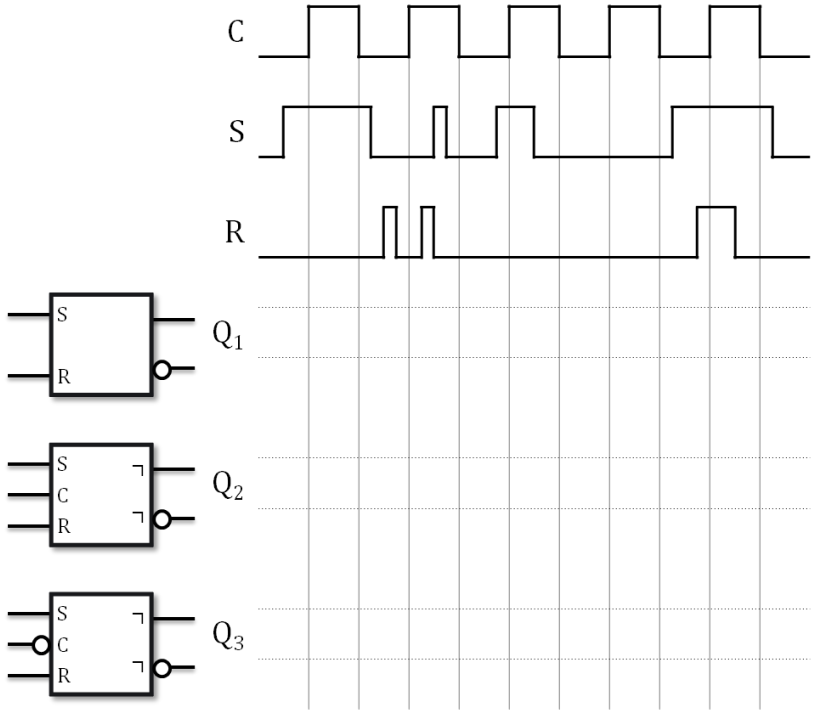
7. **(4-3)** A popular alternative design for a positive-edge-triggered D flip-flop is shown in the figure below. Manually simulate the circuit to determine whether its functional behavior is identical to that of the D flip-flop circuit presented in lectures.



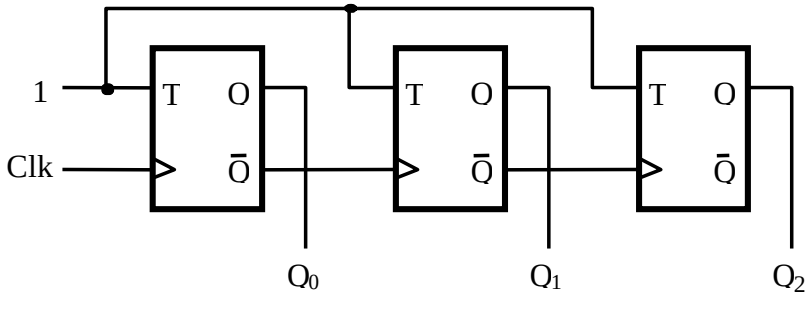
8. **(4-4)** *Clock* and *D* waveforms, one latch, and one flip-flop are shown in the figure below. For the latch and the flip-flop, carefully sketch the output waveform, Q_i, obtained in response to the input waveforms. Assume that the propagation delay of the storage elements is negligible. Initially, all storage elements store 0.

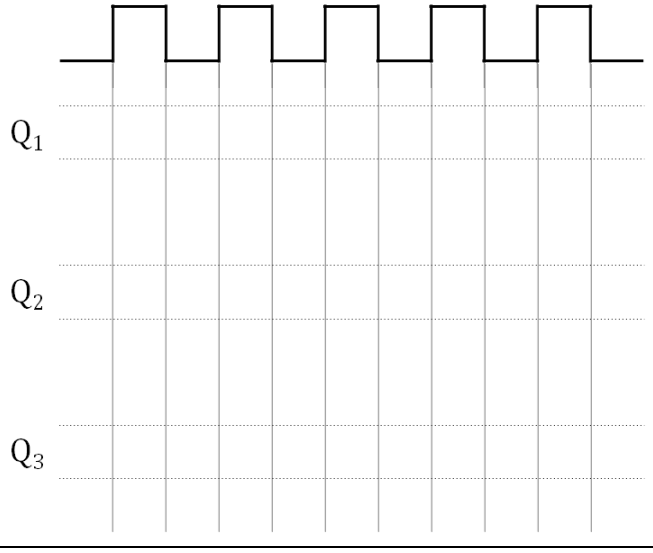


9. *Clock*, *S* and *R* waveforms, one latch and two flip-flops are shown in the figure below. For the latch and the flip-flops, carefully sketch the output waveform, Q_i, obtained in response to the input waveforms. Assume that the propagation delay of the storage elements is negligible. Initially, all storage elements store 0.



10. Draw the timing sequence of the circuit below with three T flip-flops. What is the circuit doing?





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