Name:_____

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SCHOOL OF ELECTRICAL ENGINEERING & TELECOMMUNICATIONS

ELEC2141 – DIGITAL CIRCUIT DESIGN

FINAL EXAMINATION

SESSION 1, 2018

- Reading time: 10 minutes.
- Time allowed: 2 hours.
- This paper contains 4 questions on 4 total pages.
- Total marks available: 100.
- This final examination contributes 50% to the total course assessment.
- All questions are of equal value. Part marks are as indicated.
- Answer all questions.
- Answer each question in a separate answer booklet.
- Write the question number attempted on the cover of each answer booklet.
- The exam paper may be retained by the candidate.
- Authorized examination materials: University approved calculators.
- Any assumptions found to be necessary in answering the questions should be stated explicitly.
- All answers must be written in ink. Except where they are expressly required, pencils may be used only for drawing, sketching or graphical work.

Question 1 (25 marks)

Consider the following Boolean function F:

$$\mathrm{F}(A,B,C,D) = A\bar{B}(C+D) + (\bar{A}+B)AC + \bar{B}C(A+\bar{D}) + CD(\overline{A+B})$$

Assuming that the function F is implemented using basic logic gates (NOT, AND and OR gates),

a) Find the total gate input-cost of the implementation.[2 marks]

b) Draw the truth table for the function F. [3 marks]

c) Express the function F as a sum-of-minterms (you may use the “little m” short cut notation). [3 marks]

d) Express the function F as a product-of-maxterms (you may use the “big M” short-cut notation) [3 marks]

e) Simplify the function F using Karnaugh map and express it as the sum-of-products. List all prime implicants and essential prime implicants. [5 marks]

f) Simplify the function F using Karnaugh map and express it as the product-of-sums. [4 marks]

g) For your design in part (e), find the reduction in the total gate-input cost as compared to the implementation in part (a). [2 marks]

h) Find the new simplified sum-of-products function if don’t care conditions are added at $\sum d(6,7)$. [3 marks]

Question 2 (25 marks)

i. Implement a state machine that outputs three signals names RED, GREEN, and BLUE and with a single CHANGE input. As long as CHANGE is high, the outputs go high one at a time in this specific order RED, GREEN, RED, BLUE, RED, GREEN, RED, BLUE, ... However, when CHANGE is low, the output that is high at present stays high until CHANGE is set to high.

a) Derive the state diagram for a Moore-type system. [4 marks]

b) Derive the state diagram for a Mealy-type system. [4 marks]

c) Construct the state transition table for the state diagram in (b) [3 marks]

d) Implement the state diagram in (b) using D flip-flops and whatever combinational gates you may need and neatly sketch the resulting circuit. [5 marks]

e) Write a Verilog HDL structural description of your circuit in (d) [4 marks]

ii. Convert (597.892) in base 10 number system to the binary system. Show all your workings. [5 marks]

Question 3 (25 marks)

i. Perform the following operations involving eight-bit signed values:

11011111	01110101
+10111000	-11010110

a) Derive the 8-bit result. [6 marks]

b) Determine the value of the N, Z, C, V flags. [4 marks]

c) Using the flags, or otherwise, determine whether an overflow occurred. [2 marks]

ii. Consider the following Verilog program:

```
module shift4bit (clk, in, out1, out2, out3, out4);
      input clk, in;
      output out1, out2, out3, out4;
      reg      out1, out2, out3, out4;

      always @(posedge clk) begin
            out4 = out3;
            out3 = out2;
            out2 = out1;
            out1 = in;
      end
end module
```

a) In one sentence, describe the overall function of this module. [2 marks]

b) Give a brief description of each of the inputs and outputs, and how they are being used. [5 marks]

iii. Derive a CMOS complex gate for the Boolean function F below

$$\mathrm{F}(A, B, C) = AB + AC + BC$$

Use as few transistors as possible. [6 marks]

Question 4 (25 marks)

i. Consider the following Boolean function F below

$$\mathrm{F}(A, B, C) = \bar{B}\bar{C} + AB$$

a) Implement the circuit for F using NAND gates only. Assume no complemented signals are available. [4 marks]

b) Implement the circuit for F using a 3-to-8 decoder and external logic gates. [4 marks]

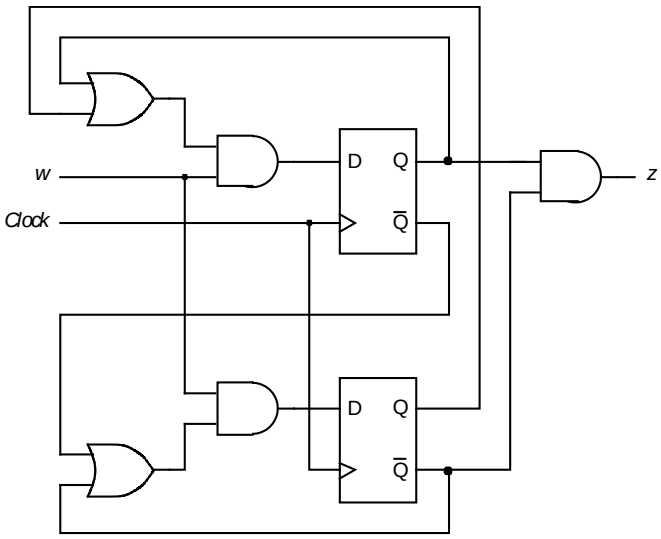
c) Implement the circuit for F using a 2-to-1 multiplexer and external logic gates. Connect input A to the selection line. [4 marks]

ii. Consider a 4-to-2 priority encoder with the following input priority: $D_1 > D_3 > D_0 > D_2$.

a) Draw the truth table for the three outputs A_1, A_0 and V. [2 marks]

b) Derive simplified expression for all three outputs. [6 marks]

iii. Consider the circuit shown below.



a) Derive the state table for the circuit [3 marks]

b) For what sequence of inputs at w, is the output z = 1? [2 marks]

END OF EXAMINATION PAPER