The University of New South Wales

School of Electrical Engineering and Telecommunications

ELEC2141: Digital Circuit Design

Mid-term Examination

Session 1, 2017

- Reading time: 10 minutes.
- Time allowed: 1 hour.
- This paper contains 2 questions on 3 total pages.
- Total marks available: 100.
- This final examination contributes 10% to the total course assessment.
- All questions are of equal value. Part marks are as indicated.
- Answer all questions.
- Answer each question in a separate answer booklet.
- Write the question number attempted on the cover of each answer booklet.
- The exam paper may not be retained by the candidate.
- Authorized examination materials: University approved calculators.
- Any assumptions found to be necessary in answering the questions should be stated explicitly.
- All answers must be written in ink. Except where they are expressly required, pencils may be used only for drawing, sketching or graphical work.

Question 1. (50 marks)

i) Consider the following Boolean function F:

F(A,B,C,D) = $\left[\left(\overline{A}+\overline{B}+C\right)\left(B+\overline{C}\right)\left(A+\overline{B}+\overline{D}\right)\right]+AC\overline{D}+B\overline{C}D$

a) Assuming that F is implemented using the basic logic gates, find the total gate input cost of the realization. **[2.5 mark]**

b) Draw the truth table for the function F. **[5 marks]**

c) Express the function F as a Sum-of-Minterms (you may use the "little m" short cut notation). **[5 marks]**

d) Express the function F as a Product-of-Maxterms (you may use the "big M" short-cut notation) **[5 marks]**

e) Using a Karnaugh map, express the function as a minimal Sum-of-Products. List all prime implicants and essential prime implicants. **[7.5 marks]**

f) Using a Karnaugh map, express the function F as a minimal Product-of-Sums. **[5 marks]**

g) Using your minimal Sum-of-Products expression from part (e), draw the logic diagram (circuit) using NAND gates only. Assume no complemented signals are available. **[5 marks]**

h) Apply factoring and decomposition to minimize the Boolean expression in part (e) further and calculate the reduction in the total gate-input cost as compared to the implementation in part (a). **[7.5 marks]**

ii) Using Boolean algebraic manipulation, prove that

$$A\overline{D}+\overline{A}B+\overline{C}D+\overline{B}C=\left(\bar{A}+\overline{B}+\overline{C}+\overline{D}\right)(A+B+C+D)$$

[7.5 marks]

Question 2. (50 marks)

i) Convert (16B4.A) in base 13 number system to a base 6 number system. You may limit the number of digits in the fraction part to three. **[7.5 marks]**

ii) Suppose you are given a task to design a 9-to-512-line decoder using only two input AND and NOT gates, outline the design procedure you may follow and indicate the total input gate cost of your design.

[7.5 marks]

iii) You are to design a combinational circuit with three data inputs: D_2, D_1, D_0; two control inputs: C_1 and C_0, and two outputs: R_1 and R_0. R_1 and R_0 should be the remainder after dividing the binary number formed from D_2, D_1, D_0 by the number formed by C_1, C_0. Note that division by zero will never be requested. [For example, if D_2,D_1,D_0 = 111 and C_1,C_0 =10, then R_1, R_0 = 01; that is, the remainder of 7 divided by 2 is 1]

a) Briefly describe the design approach you may follow. **[5 marks]**
b) Based on your approach in (a), implement your design only for R_1. **[10 marks]**
c) Implement your design only for R_1 using at least one functional block (decoder, multiplexer etc) and any number of logic gates of your choice. **[10 marks]**
d) Implement your design for R_1 using only XOR and AND logic gates. Inverters are not available. **[10 Marks]**

End of paper.