The University of New South Wales

ELEC2141: Digital Circuit Design

Tutorial Week 5 – Midterm review

1. Convert the numbers in the table below from the given base to the other bases.

Converting $3D5.E_{16}$ to decimal

$$3D5.E_{16} = 3 \times 16^2 + 13 \times 16 + 5 + 14 \times 16^{-1}$$
$$= 768 + 208 + 5 + 0.875$$
$$= 981.875_{10}$$

Converting 981.875_{10} to base-5

Integer part | Fraction part

5	981	
	196	1
	39	1
	7	4
	1	2

$0.875 \times 5 = 4.375$	4
$0.375 \times 5 = 1.875$	1
$0.875 \times 5 = 4.375$	4
$0.375 \times 5 = 1.875$	1

$$981.875_{10} = 12411.4141_5$$

Converting $3D5.E_{16}$ to binary

3	D	5	.	E
0011	1101	0101		1110

$$3D5.E_{16} = 1111010101.1110$$

Converting 1111010101.1110_2 to octal

$$\underbrace{001}_{1}\underbrace{111}_{7}\underbrace{010}_{2}\underbrace{101}_{5}.\underbrace{111}_{7}0$$

$$3D5.E_{16} = 1725.7$$

Where referenced, questions are taken from the textbook:

M. Mano, C. R. Kime and T. Martin, Logic and Computer Design Fundamentals, 5th Edition (Global Edition), Pearson, 2016

Converting 782.25_{10} to base-5

Integer

$$
\begin{array}{r|l|l}
5 & 782 & \\
 & 156 & 2 \\
 & 31 & 1 \\
 & 6 & 1 \\
 & 1 & 1
\end{array}
$$

Fraction

$0.25 \times 5 = 1.25$ 1
$0.25 \times 5 = 1.25$ 1
$0.25 \times 5 = 1.25$ 1
$0.25 \times 5 = 1.25$ 1

$782.25_{10} = 11112.1111$

Converting 782.25_{10} to hexadecimal

Integer

$$
\begin{array}{r|l|l}
16 & 782 & \\
 & 48 & 14 = E \\
 & 3 & 0
\end{array}
$$

Fraction

$0.25 \times 16 = 4$

$782.25_{10} = 30E.4_{16}$

Converting $30E.4_{16}$ to binary

3 0 E . 4
0011 0000 1110 . 0100

$30E.4_{16} = 1100001110.01_2$

Converting 1100001110.01_2 to octal

$\underbrace{001}\underbrace{100}\underbrace{001}\underbrace{110}.\underbrace{010}$

1 4 1 6 . 4

$30E.4_{16} = 1416.4_8$

binary	decimal	base-5	hexadecimal	octal
1111010101.111	981.875	12411.4141	3D5.E	1725.7
1100001110.01	782.25	11112.1111	30E.4	1416.4

2. Simplify the following Boolean functions using algebraic manipulation to a minimum number of literals

   i. $F(A,B,C) = A\oplus B\oplus C + \bar{A}\bar{B}\bar{C} + \bar{A}BC + A\bar{B}C + AB\bar{C}$

   ii. $G(A,B,C,D) = ABD + A\bar{B}\bar{C} + A\bar{B}C\bar{D}$

2.

(i) $F = A\oplus B\oplus C + \bar{A}\bar{B}\bar{C} + \bar{A}BC + A\bar{B}C + AB\bar{C}$

$= A\oplus B\oplus C + (\bar{A}\bar{B} + AB)\bar{C} + (\bar{A}B + A\bar{B})C$

$\bar{A}B + A\bar{B} = A\oplus B = X$

$\overline{A\oplus B} = \overline{\bar{A}B + A\bar{B}} = \bar{A}\bar{B} + AB = \bar{X}$

$\Rightarrow f = A\oplus B\oplus C + (\overline{A\oplus B})\bar{C} + (A\oplus B)C$

$= A\oplus B\oplus C + \underbrace{\bar{X}\bar{C} + XC}_{\overline{X\oplus C}}$

$= A\oplus B\oplus C + (\overline{X\oplus C})$

$= A\oplus B\oplus C + (\overline{A\oplus B\oplus C})$

$= 1$

(ii) $G = ABD + A\bar{B}\bar{C} + A\bar{B}C\bar{D}$

$= ABD + A\bar{B}(\bar{C} + C\bar{D})$

Note: $X + Y = X + \bar{X}Y$

$\Rightarrow G = ABD + A\bar{B}(\bar{C} + \bar{D})$

$= ABD + A\bar{B}\bar{C} + A\bar{B}\bar{D}$

3. Consider the following Boolean function F:

$$F(A,B,C,D) = (\bar{A}+\bar{B}+D)(\bar{A}+\bar{D}) + AC + BD$$

3. (i) $F = (\bar{A}+\bar{B}+D)(\bar{A}+\bar{D}) + AC + BD$

$GIC = 9\,(\text{literals}) + 3\,(\text{inv}) + 5\,(\text{terms})$
$= 17$

i) Opening

$F = \underbrace{\bar{A}\bar{A}}_{\bar{A}} + \bar{A}\bar{B} + \bar{A}D + \bar{A}\bar{D} + \bar{B}\bar{D} + \underbrace{\cancel{D\bar{D}}}_{0} + AC + BD$

$= \bar{A} + \bar{A}\bar{B} + \bar{A}D + \bar{A}\bar{D} + \bar{B}\bar{D} + AC + BD$

$\bar{A}$ will include all minterms with $\bar{A}$

$\Rightarrow \bar{A} = \underset{0}{\bar{A}\bar{B}\bar{C}\bar{D}} + \underset{4}{\bar{A}B\bar{C}\bar{D}} + \underset{2}{\bar{A}\bar{B}C\bar{D}} + \underset{6}{\bar{A}BC\bar{D}}$
$+ \underset{1}{\bar{A}\bar{B}\bar{C}D} + \underset{5}{\bar{A}B\bar{C}D} + \underset{3}{\bar{A}\bar{B}CD} + \underset{7}{\bar{A}BCD}$

$\bar{A}\bar{B}$, $\bar{A}D$, $\bar{A}\bar{D}$ will be give minterms include in those obtained $\bar{A}$ (0 − 7)

$AC = AC(B+\bar{B})(D+\bar{D})$
$= AC(BD + \bar{B}D + B\bar{D} + \bar{B}\bar{D})$

$= \underset{15}{ABCD} + \underset{11}{A\bar{B}CD} + \underset{14}{ABC\bar{D}} + \underset{10}{A\bar{B}C\bar{D}}$

$BD = BD(A+\bar{A})(C+\bar{C})$
$= BD(AC + \bar{A}C + A\bar{C} + \bar{A}\bar{C})$

$= \underset{15}{ABCD} + \underset{7}{\bar{A}BCD} + \underset{13}{AB\bar{C}D} + \underset{5}{\bar{A}B\bar{C}D}$

$\bar{B}\bar{D} = \bar{B}\bar{D}(A+\bar{A})(C+\bar{C})$
$= \bar{B}\bar{D}(AC + \bar{A}C + A\bar{C} + \bar{A}\bar{C})$

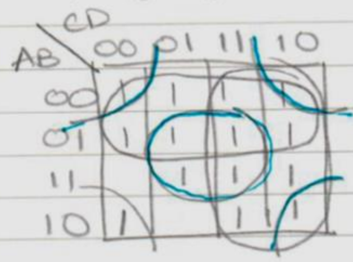
$= \underset{10}{A\bar{B}C\bar{D}} + \underset{2}{\bar{A}\bar{B}C\bar{D}} + \underset{8}{A\bar{B}\bar{C}\bar{D}} + \underset{0}{\bar{A}\bar{B}\bar{C}\bar{D}}$

$F = \Sigma m(0,1,2,3,4,5,6,7,8,10,11,13,14,15)$

Where referenced, questions are taken from the textbook:
M. Mano, C. R. Kime and T. Martin, Logic and Computer Design Fundamentals, 5th Edition (Global Edition), Pearson, 2016

(iii)

Simplifying using a K-map

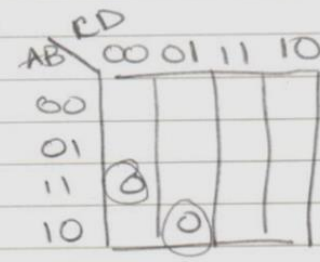


All prime implicants are essential

$\bar{A}, C, BD, \bar{B}\bar{D}$

$F = \bar{A} + C + BD + \bar{B}\bar{D}$

(iv)



$F = (\bar{A}+\bar{B}+C+D)(\bar{A}+B+C+\bar{D})$

or

$\bar{F} = \overline{AB\bar{C}\bar{D} + A\bar{B}\bar{C}D}$

$= (\overline{AB\bar{C}\bar{D}})(\overline{A\bar{B}\bar{C}D})$

$= (\bar{A}+\bar{B}+C+D)(\bar{A}+B+C+\bar{D})$

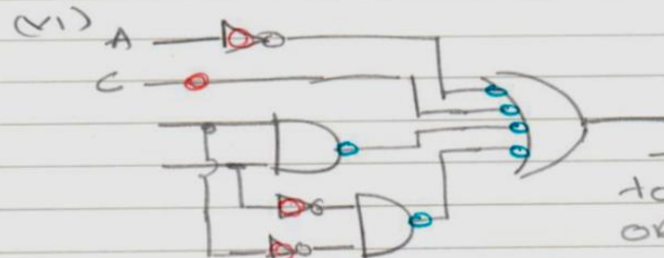
(v) $F = \bar{A} + C + BD + \bar{B}\bar{D}$

$GIC = 6(\text{no of literals}) + 2(\text{terms}) + 3(\text{inv})$

$= 11$

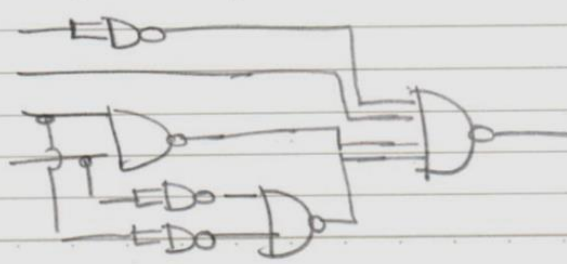
Reduction $= 17 - 11 = 6$

(vi)



AND-OR imp

- Adding bubbles to convert AND & OR to NAND
- Adding inverters where no pairs
- Replacing inverters with NANDs too



4. Design a combination circuit which can detect prime numbers from 0 to 15. There should be a single output line, which is 1 if the input is a prime number, otherwise the output line would be 0.

For numbers 0-15 will need 4 bits (A,B,C,D)
Output is single bit (Y)

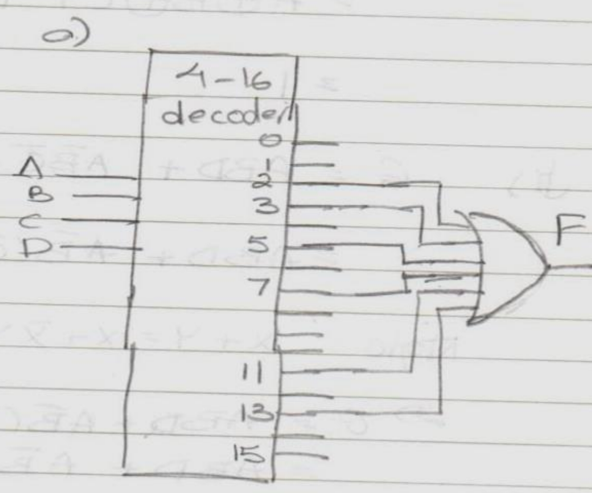
Y=1 when ABCD is prime
prime numbers are 2,3,5,7,11,13

Drawing truth table

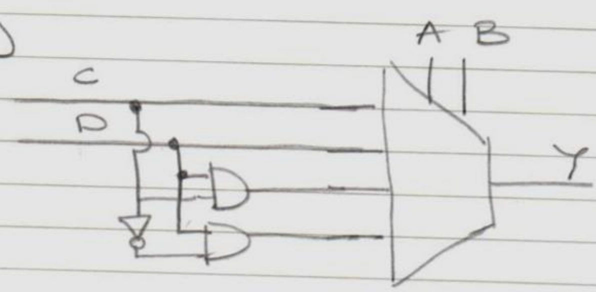
	A	B	C	D	Y
	0	0	0	0	0
	0	0	0	1	0
Y=C	0	0	1	0	1
	0	0	1	1	1
	0	1	0	0	0
	0	1	0	1	1
Y=D	0	1	1	0	0
	0	1	1	1	1
	1	0	0	0	0
	1	0	0	1	0
Y=CD	1	0	1	0	0
	1	0	1	1	1
	1	1	0	0	0
	1	1	0	1	1
$Y=\bar{C}D$	1	1	1	0	0
	1	1	1	1	0

$Y = \Sigma m(2,3,5,7,11,13)$

a)



b)



A,B are at select; C,D at input

Where referenced, questions are taken from the textbook:

M. Mano, C. R. Kime and T. Martin, Logic and Computer Design Fundamentals, 5th Edition (Global Edition), Pearson, 2016

5. Design a circuit to implement the following pair of Boolean equations, using factoring to simplify.

5. factoring both functions

$X = AD F + AEF + BDF + B E F + CDF + CEF$

$= (AD + AE + BD + BE + CD + CE)F$

$= [(A+B+C)D + (A+B+C)E]F$

$= [(A+B+C)(D+E)]F$

$Y = A\bar{D}\bar{E} + B\bar{D}\bar{E} + C\bar{D}\bar{E}$

$= (A+B+C)\bar{D}\bar{E}$

Let $T_1 = A+B+C$

$T_2 = D+E \Rightarrow \bar{T}_2 = \overline{D+E} = \bar{D}\bar{E}$

$\Rightarrow X = T_1 T_2 F$

$Y = T_1 \bar{T}_2$

Original GIC X = 18(literals) + 6(terms) = 24

GIC Y = 9(literals) + 3(terms) + 2(inv)

= 14

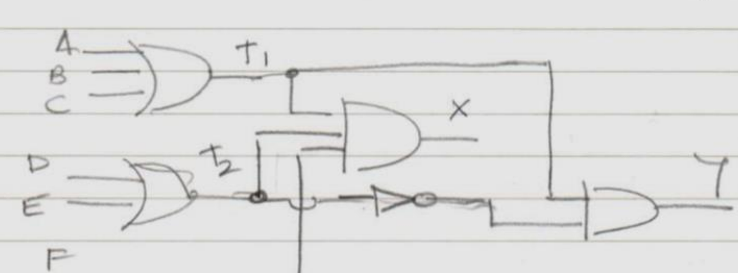
Total GIC = 24 + 14 = 38

Optimized GIC $T_1 = 3$ $T_2 = 2$ inv = 1

$X = 3$ $Y = 2$

Total GIC = 3 + 3 + 2 + 2 + 1 = 11

GIC reduction = 38 − 11 = 27



6. Implement the function below using XOR and AND gates only. Then construct the circuit using interconnecting three-state buffers and inverters.

$$H = A\bar{B}C\bar{D} + \bar{A}BC\bar{D} + A\bar{B}\bar{C}D + \bar{A}B\bar{C}D$$

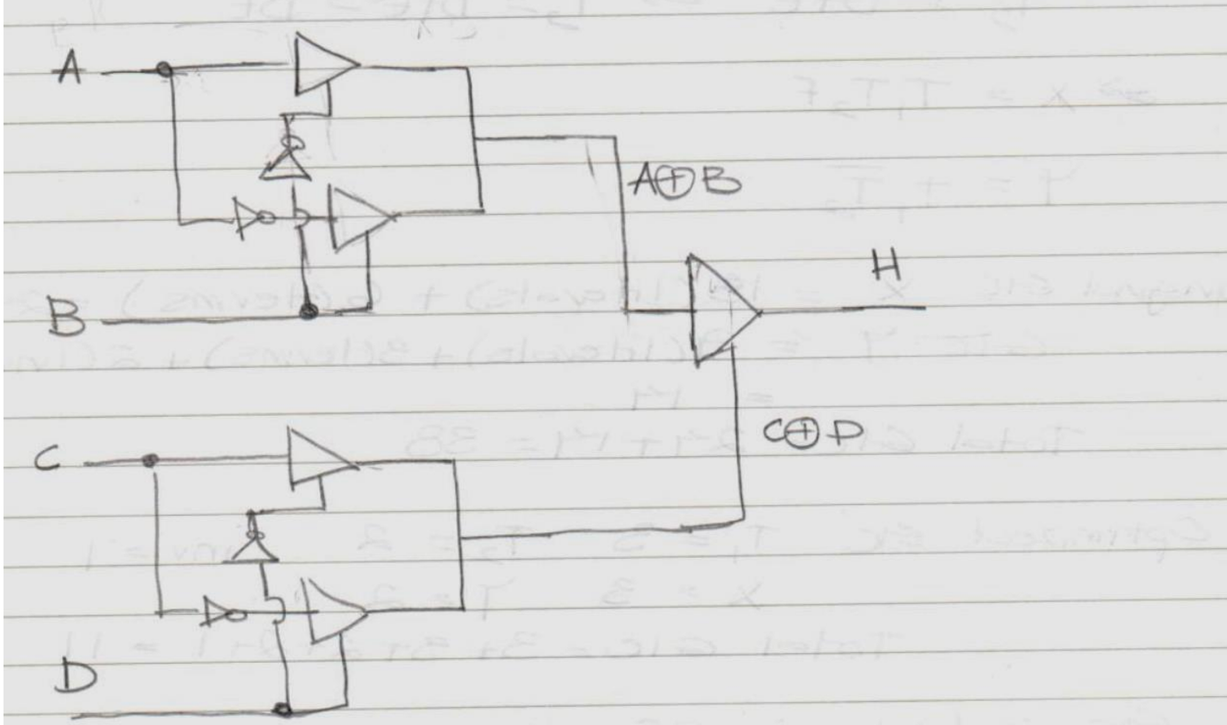
Factoring H

$$H = A\bar{B}(C\bar{D} + \bar{C}D) + \bar{A}B(C\bar{D} + \bar{C}D)$$

$$= (A\bar{B} + \bar{A}B)(C\bar{D} + \bar{C}D)$$

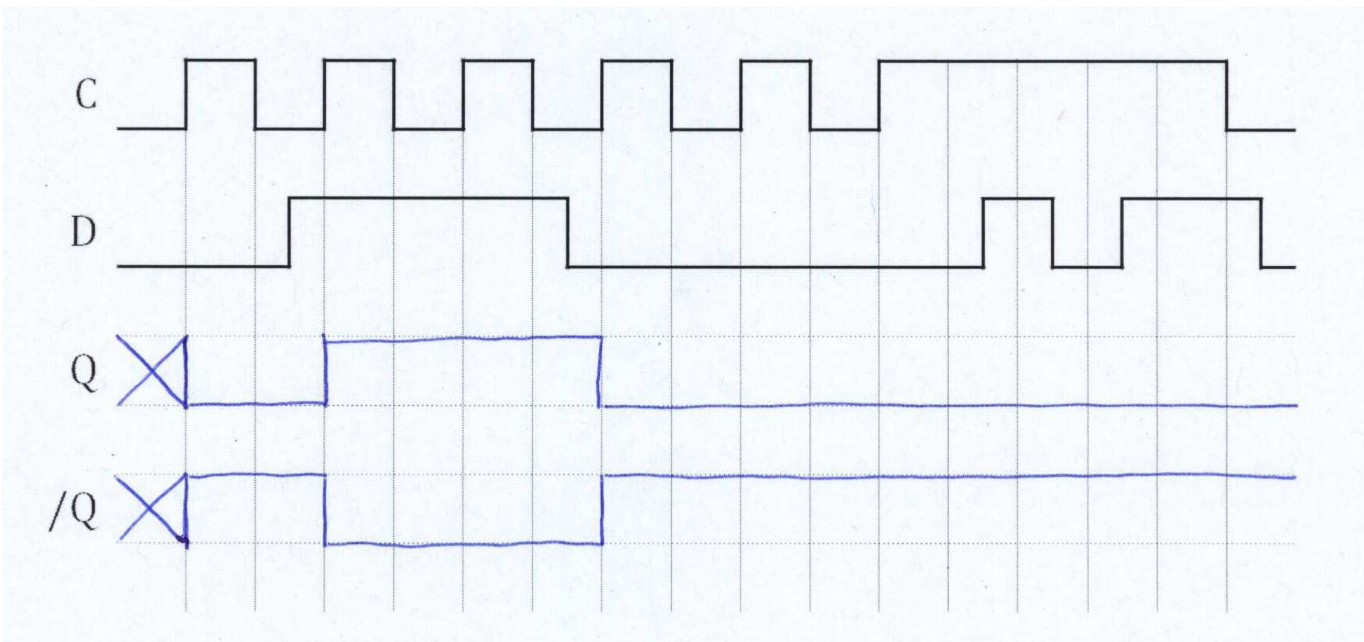
$$= (A \oplus B)(C \oplus D)$$

To implement using 3-state buffers, will implement each XOR separately and bring together in final 3-state buffer

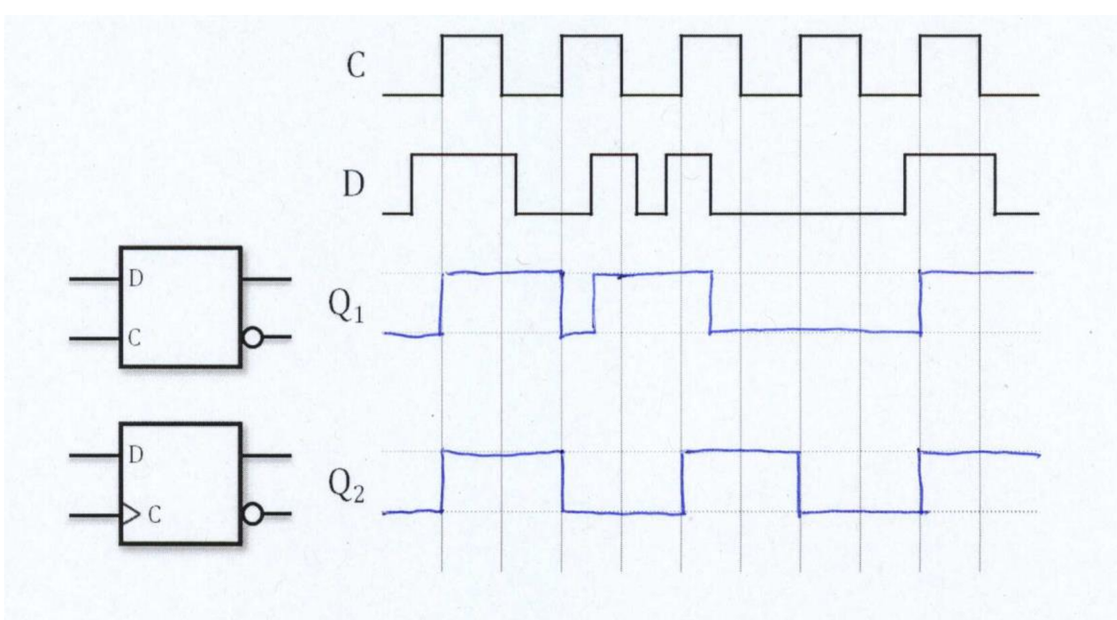


7. Simulate the circuit to determine whether its functional behavior is identical to that of the D flip-flop circuit presented in lectures

Manually tracking the circuit can see that circuit behave like a D flip-flop circuit.



8. *Clock* and *D* waveforms, one latch, and one flip-flop are shown in the figure below. For the latch and the flip-flop, carefully sketch the output waveform, Q_i, obtained in response to the input waveforms.



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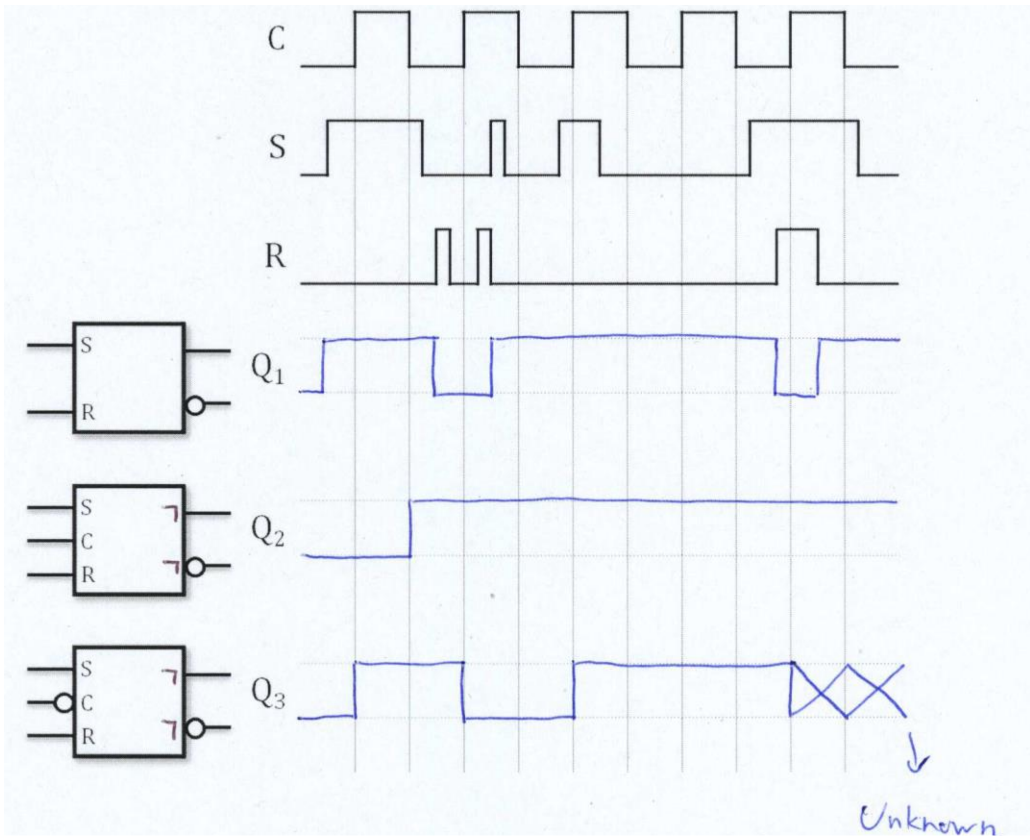
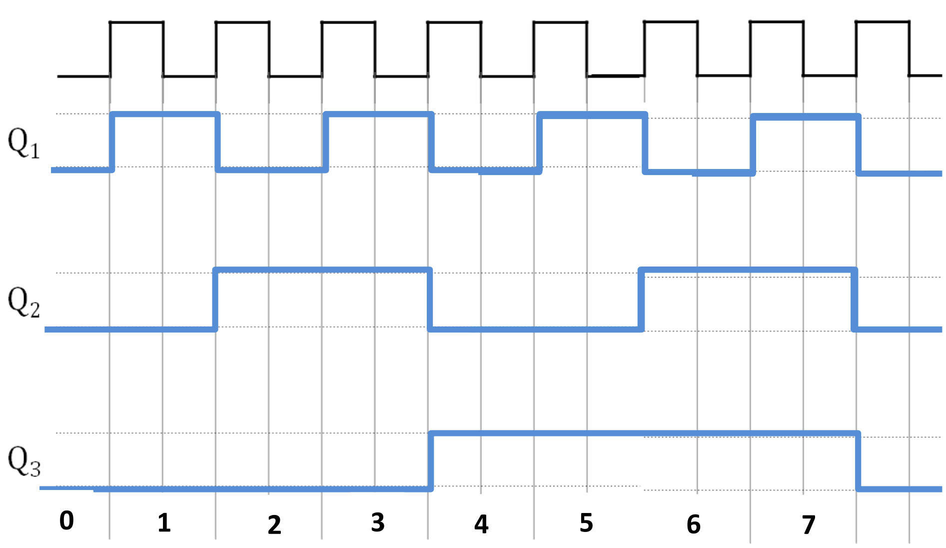
9. *Clock*, *S* and *R* waveforms, one latch and two flip-flops are shown in the figure below. For the latch and the flip-flops, carefully sketch the output waveform, Q_i, obtained in response to the input waveforms.

The last bit is unknown due to a race condition in the master slave condition. Can settle at $Q_3 = 0$ or $Q_3 = 1$



10. Draw the timing sequence of the circuit below with three T flip-flops. What is the circuit doing?

The circuit is a three bit counter



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