The University of New South Wales

School of Electrical Engineering and Telecommunications

ELEC2141: Digital Circuit Design

Final Examination

Session 1, 2012

- Reading time: 10 minutes.
- Time allowed: 3 hours.
- This paper contains 5 questions on 6 total pages.
- Total marks available: 100.
- This final examination contributes 60% to the total course assessment.
- All questions are of equal value. Part marks are as indicated.
- Answer all questions.
- Answer each question in a separate answer booklet.
- Write the question number attempted on the cover of each answer booklet.
- The exam paper may be retained by the candidate.
- Authorized examination materials: University approved calculators.
- Any assumptions found to be necessary in answering the questions should be stated explicitly.
- All answers must be written in ink. Except where they are expressly required, pencils may be used only for drawing, sketching or graphical work.

Question 1. (20 marks)

i) Consider the following truth table:

W	X	Y	Z	F
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	1
1	1	1	1	0

a) Express the function *F* as a Sum-of-Minterms (you may use the "little *m*" short-cut notation). **[1 mark]**

b) Express the function *F* as a Product-of-Maxterms (you may use the "big M" short-cut notation). **[2 marks]**

With the aid of a Karnaugh map:

c) List all of the prime implicants of *F*. **[2 marks]**

d) List all of the essential prime implicants of *F*. **[2 marks]**

e) Find a minimal Sum-of-Products expression for *F*. **[2 marks]**

f) Find a minimal Product-of-Sums expression for *F*. **[2 marks]**

g) Using your minimal Sum-of-Products expression from part (e), draw the logic diagram (circuit) using NAND gates only. Note that you may only use NAND gates with 3 inputs or less. Assume no complemented signals are available. **[3 marks]**

h) For your design in part (g), find the total gate-input cost. **[2 marks]**

ii) Using Boolean algebra, prove the identity:

$$(A + B)(\bar{A} + C)(B + C) = (A + B)(\bar{A} + C)$$

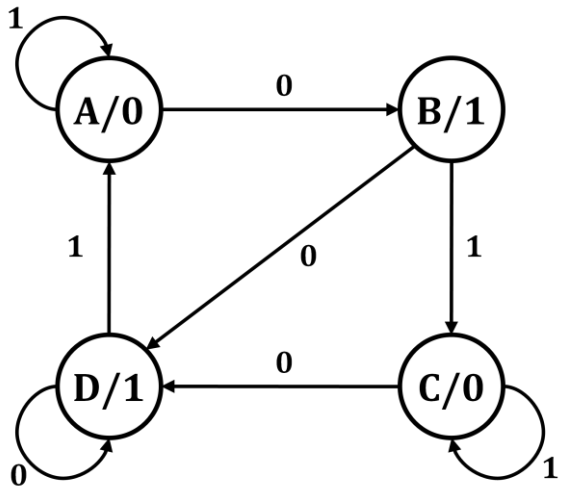
[4 marks]

Question 2 on the next page.

Question 2. (20 marks)

i) Convert the duodecimal (base 12) number: **3A57.17**$_{(12)}$ to senary (base 6). Show all working. **[5 marks]**

ii) Consider the following state diagram for a Moore state machine where *A*, *B*, *C*, and *D* are the state names:



a) Explain the difference between a Moore and a Mealy state machine. **[2 marks]**

b) Construct the state transition table for the state diagram above. **[2 marks]**

c) Minimize the number of states and derive the reduced state transition table. **[3 marks]**

d) Convert the reduced Moore state machine into a Mealy one, showing both the state diagram and the state transition table. **[3 marks]**

e) Implement the reduced Moore state machine from part (c) in Verilog code, clearly stating the names for the inputs, outputs and states. **[5 marks]**

Please turn over - Question 3 on the next page.

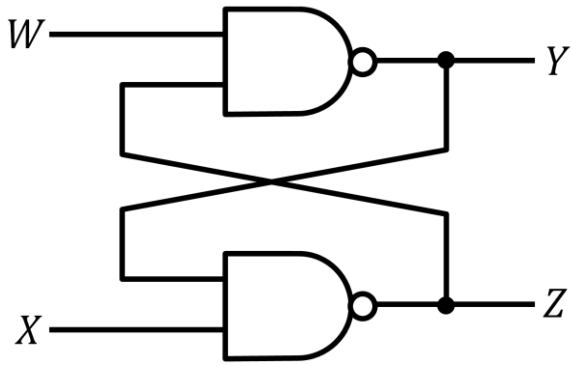
Question 3. (20 marks)

i) Consider the following state transition table:

Current State q_1q_0	Next State X = 0 Q_1Q_0	Next State X = 1 Q_1Q_0
00	00	01
01	00	10
10	00	01
11	11	00

Draw the logic diagram that implements the machine using J-K flip-flops. **[7 marks]**

ii) Consider the following circuit:



a) What basic digital element is implemented by this circuit? **[1 mark]**

b) From your answer to part (a), give the inputs (*W*, *X*) and outputs (*Y*, *Z*) more meaningful names and describe their operation. **[2 marks]**

c) Extend this circuit into a clocked D-latch and give the function table for all input combinations. **[3 marks]**

d) By using multiple instances of the clocked D-latch from part (c) and additional logic, construct a positive edge-triggered D flip-flop. **[3 marks]**

e) Modify the D flip-flop from part (d) to include synchronous, active-high, Set and Reset (*S* and *R*) inputs. State which of the inputs in your design dominates. **[4 marks]**

Question 4 on the next page.

Question 4. (20 marks)

i) Consider the following function:

$$F = \overline{(AB + C)D}$$

a) Construct a CMOS complex gate which gives the same truth table as that of the Boolean function *F*. **[5 marks]**

b) Draw the logic diagram (circuit) for a NAND-only implementation of *F*. Assume the signals *A*, *B*, *C* and *D* are available, as well as the power rails (V_{DD} and GND). You may use only NAND gates with two inputs. **[4 marks]**

c) Construct the truth table for the function *F* and subsequently show how *F* may be implemented using only a decoder and one multiple-inputs NOR gate. **[3 marks]**

ii) Write a Verilog module for a Prime Number Detector. Assume that the input/output declarations for the module are as follows:

```
module Prime(N, F);
   input [3:0] N;
   output F;

   // Your code goes here

endmodule
```

Show all working. Marks will be awarded for using correct syntax. **[8 marks]**

Please turn over - Question 5 on the next page.

Question 5. (20 marks)

Design an 8-bit serial-to-parallel converter with a comparator output flag as per the following specifications:

The design should have 3 input signals: ***CLK***, ***RST***, and ***X***.
The design should have 9 output signals: ***b[7:0]*** and ***F***.

Input *X* forms a serial input of concatenated unsigned 8-bit numbers (one bit per rising edge of *CLK*, LSB first). The *RST* input is asserted High to reset the system. The input stream will be valid once *RST* is de-asserted.
That is: the LSB of the first 8-bit number will appear on the first rising clock edge after *RST* is de-asserted, followed by the other 7 bits of the number, followed immediately by the next 8-bit number, and so on.

Once each 8-bit string has been read, the output *b[7:0]* will change to contain the whole number, and hold the value until the next 8-bit input is read. That is: the output only changes once per 8 clock cycles.

In addition, the output *F* should be asserted High if the 8-bit output is less than (decimal) 30, or asserted Low otherwise (greater or equal to 30).

For your design, draw the complete logic diagram (circuit), clearly indicating the inputs, outputs, and any blocks used.
In your design, you may use logic gates with any number of inputs, as well as any fundamental digital building blocks taught in lectures (such as multiplexers, encoders, decoders, latches, flip-flops, etc.).

In addition, write a short paragraph describing the operation of your design.

[20 marks]

End of paper.