Name:_____

Student ID:_____

Signature:_____

SCHOOL OF ELECTRICAL ENGINEERING & TELECOMMUNICATIONS

ELEC2141 – DIGITAL CIRCUIT DESIGN

MID-TERM EXAMINATION

TERM 1, 2019

- Reading time: 5 minutes.
- Time allowed: 1 hour in total.
- This paper contains 2 questions on the 2 following pages.
- Total marks available: 100.
- This mid semester examination contributes 15% to the total course assessment.
- All questions are of equal value. Part marks are as indicated.
- Answer all questions.
- Answer each question in a separate answer booklet.
- Write the question number attempted on the cover of each answer booklet.
- The exam paper may not be retained by the candidate.
- Authorized examination materials: University approved calculators.
- Any assumptions found to be necessary in answering the questions should be stated explicitly.
- All answers must be written in ink. Except where they are expressly required, pencils may be used only for drawing, sketching or graphical work.

Question 1 (50 marks)

a) Consider the following Boolean function F:

$$F(A, B, C, D) = \bar{C}D + AB\bar{C} + AB\bar{D} + \bar{A}\bar{B}D$$

Assuming that the function F is implemented using basic logic gates (NOT, AND and OR gates),

i. Find the total gate input-cost of the implementation. [3 marks]

ii. Express the function F as a sum-of-minterms (you may use the "little m" short cut notation). [4 marks]

iii. Simplify the function F using a Karnaugh map and express it as the sum-of-products. List all prime implicants and essential prime implicants. [8 marks]

iv. Express the function F as a product-of-sums. List all prime implicants and essential prime implicants. [8 marks]

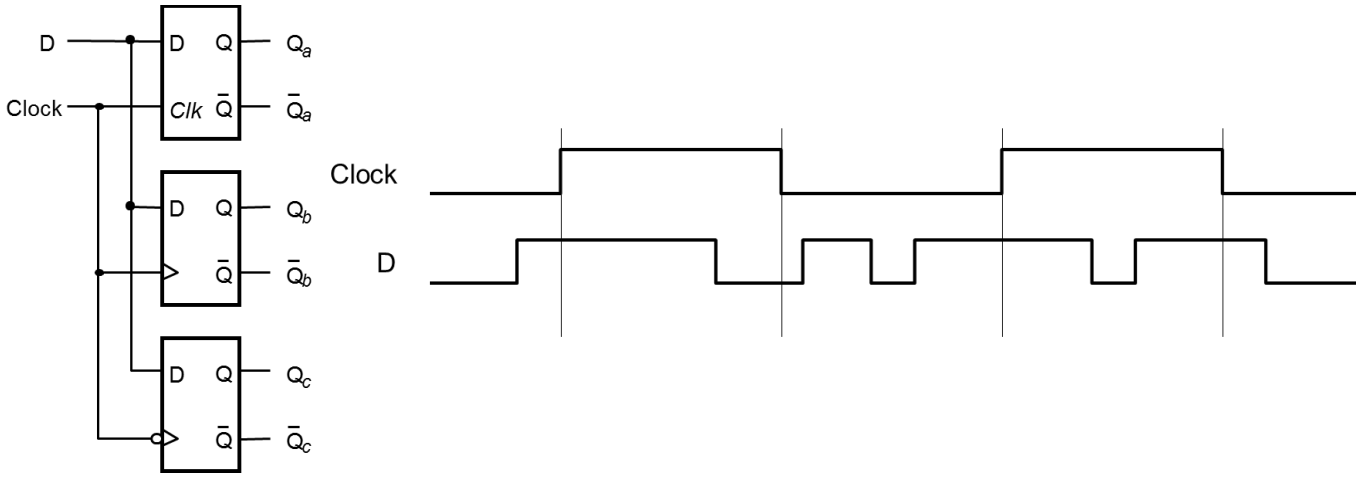
v. For your design in part (iii), find the reduction in the total gate-input cost as compared to part (i). [3 marks]

b) Using a 4-to-16 decoder, a 4-to-1 multiplexer and any additional logic required, design a circuit that compares two 2-bit input binary numbers, $X = X_1X_0$ and $Y = Y_1Y_0$, and produces an output F with the result. Two input lines S_1, S_0 are used to select which of the four comparison functions from below appear at the output F:

EQ = 1 when X and Y are equal
GT = 1 when X is greater than Y
LE = 1 when X is less than Y
NULL = 0

Draw the full circuit. Clearly state any assumptions [15 marks].

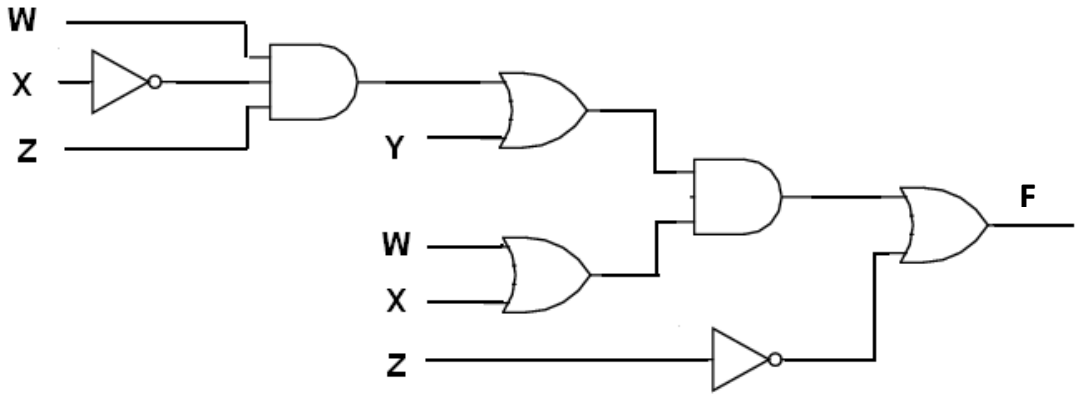
c) Assuming that the D and Clock inputs shown in the diagram below are applied to the circuit below, draw the waveforms for Q_a, Q_b and Q_c. [9 marks]


D
Clock
D
Q
Clk
Q
Q_a
$\bar{Q}_a$
Q_b
$\bar{Q}_b$
Q_c
$\bar{Q}_c$
Clock
D

Question 2 (50 marks)

a) Convert octal 453.25 to base-7 and binary. Limit the number of digits in the fraction part to four. Show all your workings. [16 marks]

b) For the circuit below:



i. Write the Boolean function for the output F. [4 marks]

ii. Use algebraic simplification to optimise the function to its minimal form. [7 marks]

iii. Implement the optimised Boolean function using 2, 3 or 4 input NOR only gates. Do not assume that complements are available. [8 marks]

c) The truth table for the a 1-bit subtractor computing $D = A - B$, with BL (borrow to the left) is shown below

A	B	D	BL
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

i. Design a 1-bit combinational subtractor with two data inputs (A, B), a borrow from the right input (BR), a borrow request to the left output (BL) and difference output D using only XOR, AND and inverter logic gates. [10 marks]

ii. Show how you would cascade your design to form a 4-bit subtractor. [5 marks]

END OF EXAMINATION PAPER