Cover page

Model Name: PCE-2129/2029 A101-2

Version:	A101-2	PCB P/N:	19A1212901-01	Update Date:	2018/07/02

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Title	01_Cover page	
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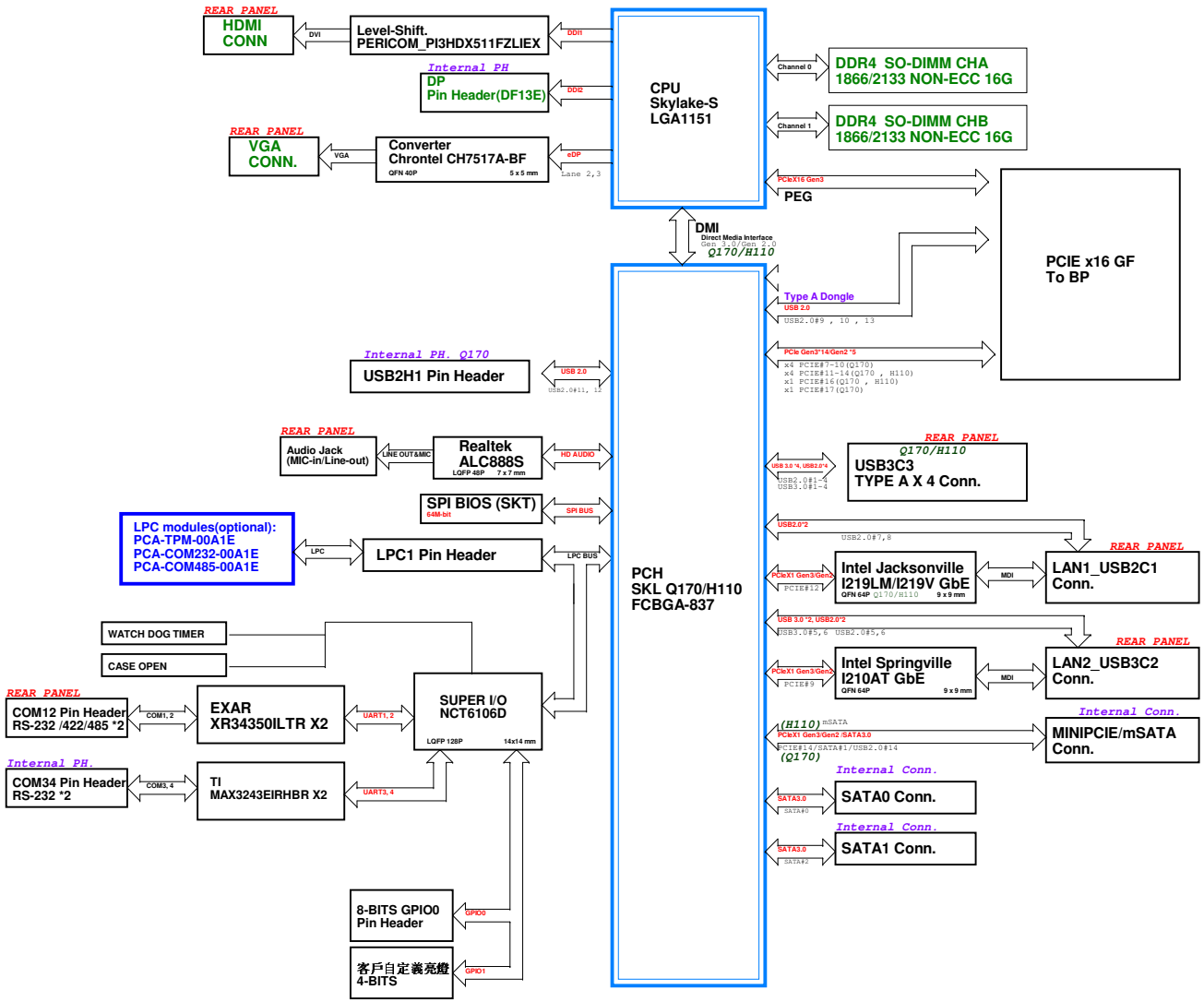
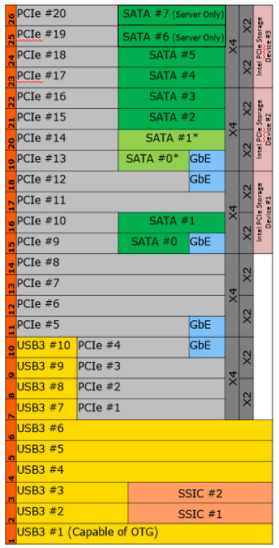
Block Diagram

PCE-2129/2029 A101-1

20180625
Update ok





	PCE-2029 H110	PCE-2129 Q170
26	N/A	x4 Riser
25	N/A	
24	N/A	
23	N/A	
22		
21	Internal SATA1	Internal SATA1
20	mSATA	mPCIE/mSATA
19	Internal SATA0	Internal SATA0
18	LAN1 (PHY, I219V)	LAN1 (PHY, I219LM)
17	N/A	x1 Riser
16	x1 Riser	x1 Riser
15	LAN2 (I210AT)	LAN2 (I210AT)
14	x4 Riser	x4 Riser
13		
12		
11		
10	N/A	x4 Riser
9	N/A	
8	N/A	
7	N/A	
6	N/A	LAN2_USB3C2(Rear) (USB3.0)(I210)
5	N/A	LAN2_USB3C2(Rear) (USB3.0)(I210)
4	USB3C3(Rear) (USB3.0)	USB3C3(Rear) (USB3.0
3	USB3C3(Rear) (USB3.0)	USB3C3(Rear) (USB3.0
2	USB3C3(Rear) (USB3.0)	USB3C3(Rear) (USB3.0
1	USB3C3(Rear) (USB3.0)	USB3C3(Rear) (USB3.0

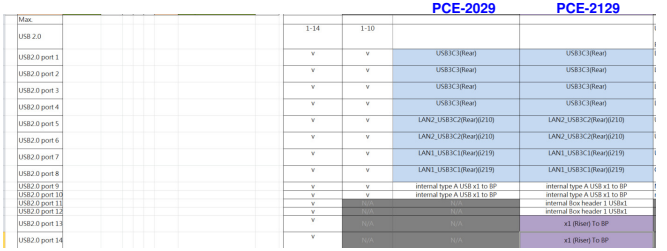


Table 1-2. PCH-H SKUs

Features	PCE-2029 H110	H170	HM170	QM170	Z170	B150	Q150	PCE-2129 Q170
Intel® Rapid Storage Technology	AHCI Mode	Full Features[8]	Full Features[8]	Full Features[8]	Full Features[8]	AHCI Mode	AHCI Mode	Full Features[8]
Total USB 3.0 Ports	4	8	8	8	10	6	8	10
Total USB 2.0 Ports	10[1]	14[3]	12[2]	12[2]	14[3]	12[2]	14[3]	14[3]
Total SATA 3.0 Ports (Max 6 Gb/s)	4	6	4	4	6	6	6	6
Total PCI Express* Lanes (Gen)	6 (2.0)	16 (3.0)	16 (3.0)	16 (3.0)	20 (3.0)	8 (3.0)	10 (3.0)	20 (3.0)
Total Intel® RST capable PCIe and SATA Express[4] Storage Devices	0	2[6]	2[6]	2[6]	3[7]	0	0	3[7]
Processor dgfx bifurcation support	No	No	Yes[5]	Yes[5]	Yes[5]	No	No	Yes[5]

Notes:
1. USB 2.0 port numbers: 1-10
2. USB 2.0 port numbers: 1-12
3. USB 2.0 port numbers: 1-14
4. SATA Express Capable Ports (x2)
5. PCIe configuration 1x16, or 2x8 or 2x4 or 1x8 are supported
6. Intel® RST PCIe supports RAID configuration 0/1.
7. Intel® RST PCIe supports RAID configuration 0/1/5
8. Full featured includes SATA RAID 0/1/5/10 support

MODEL IO LIST

Orcad BOM	CPU	PCH	MEMORY SUPPORT	VGA1	HDMI	DVI	DP2/DVI3	LAN1	LAN2	COM3 , 4	COM1 , 2	GPIO	USB2.0	USB2.0	USB3.0	SATA3.0	MINIPCIE/mSATA	LPC	Expansion Conn.	B/B Conn.	Audio	CFast
			Cable							Cable		Cable	PH	Conn.	Conn.	Conn.	Conn.	Conn.	Conn.	Conn.		Conn.
Part_Number_Value	Skylake-S	PCH -H	DDR4 SO-DIMM 1866/2133 NON-ECC	CH7517A-BF	PI3HDX511FZLIEX	1	0	Intel I219LM	Intel I210AT	RS-232 *2	RS-232/422/485 *2	1	2	2	6	3	1/1 either 1	1	0	0	MIC-in/ Line-out	0
Part_Number_2129Q	Skylake-S	Q170	DDR4 SO-DIMM 1866/2133 NON-ECC	CH7517A-BF	PI3HDX511FZLIEX	1	0	Intel I219LM	Intel I210AT	RS-232 *2	RS-232/422/485 *2	1	2	2	6	3	1/1 either 1	1	0	0	MIC-in/ Line-out	0
Part_Number_2029H	Skylake-S	H110	DDR4 SO-DIMM 1866/2133 NON-ECC	CH7517A-BF	PI3HDX511FZLIEX	1	0	Intel I219V	Intel I210AT	RS-232 *2	RS-232/422/485 *2	1	0	4	4	3	mSATA	1	0	NA	MIC-in/ Line-out	0

PCA-TPM-00A1E
PCA-COM232-00A1E
PCA-COM485-00A1E

MIC-7900
10G Module
RJ45

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Title	02_Block Diagram	
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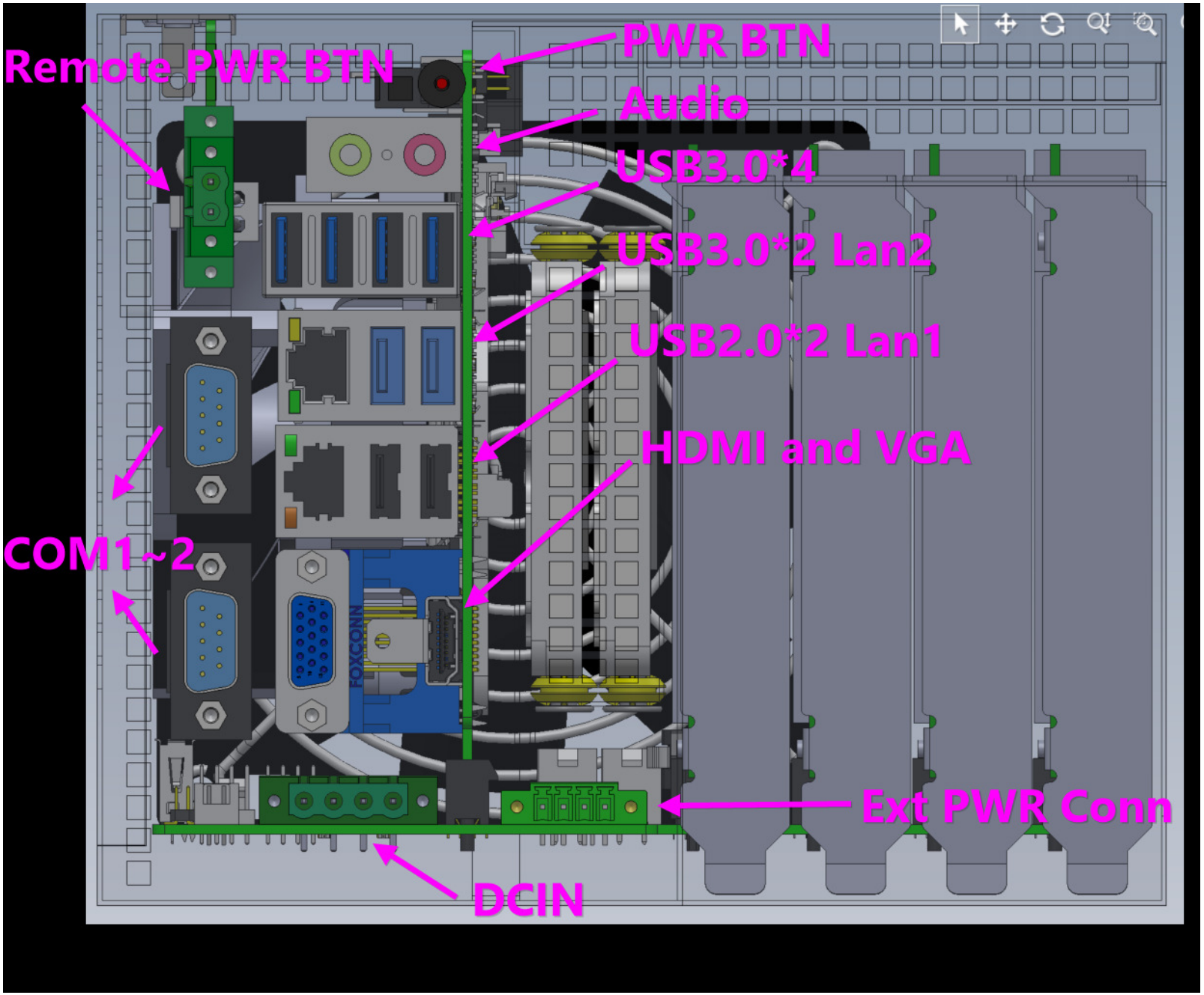
Outline



ADVANTECH		
Title	03_Outline	
Size	Document Number PCE-2129(2029)	Rev A101-2
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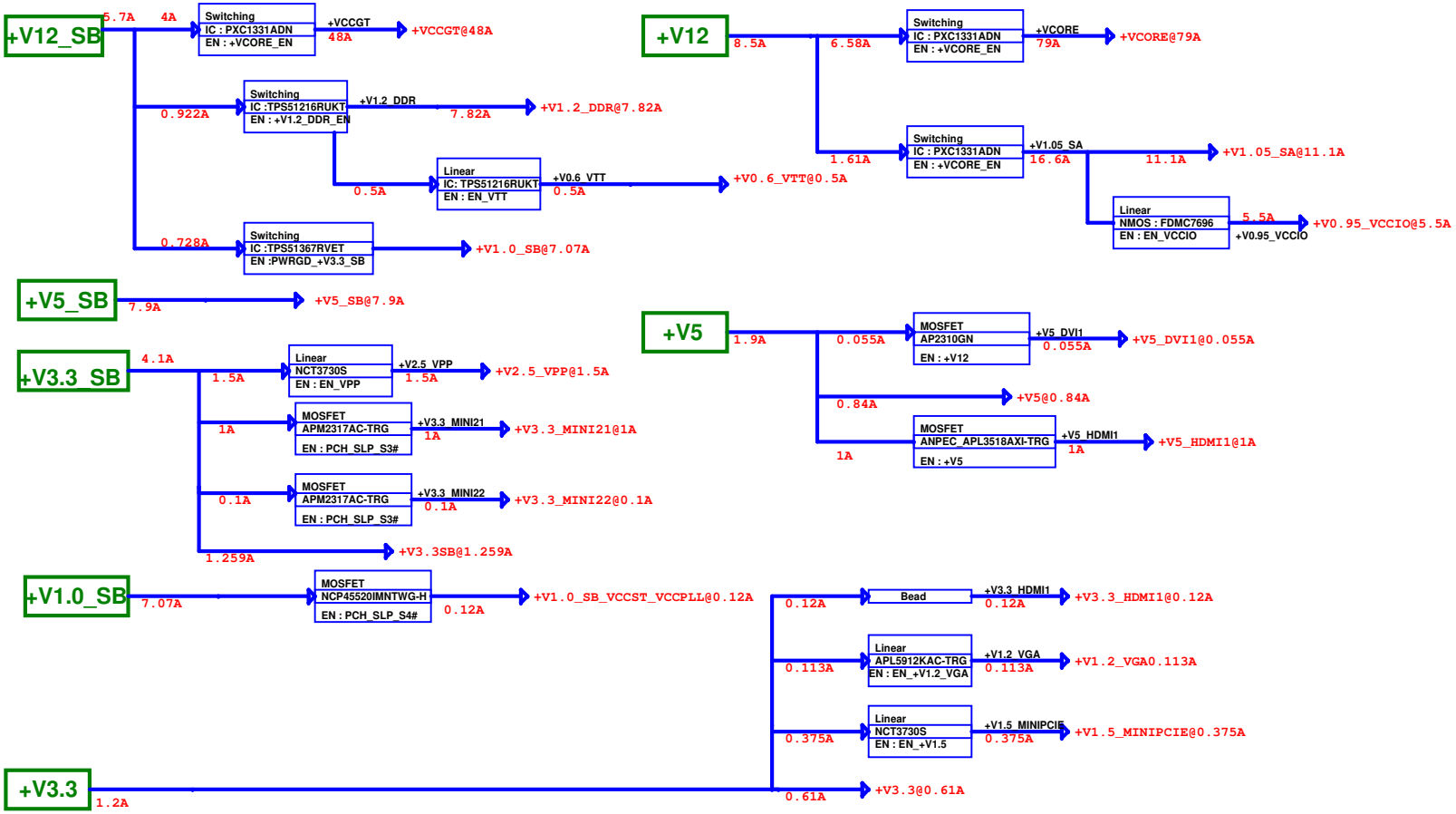
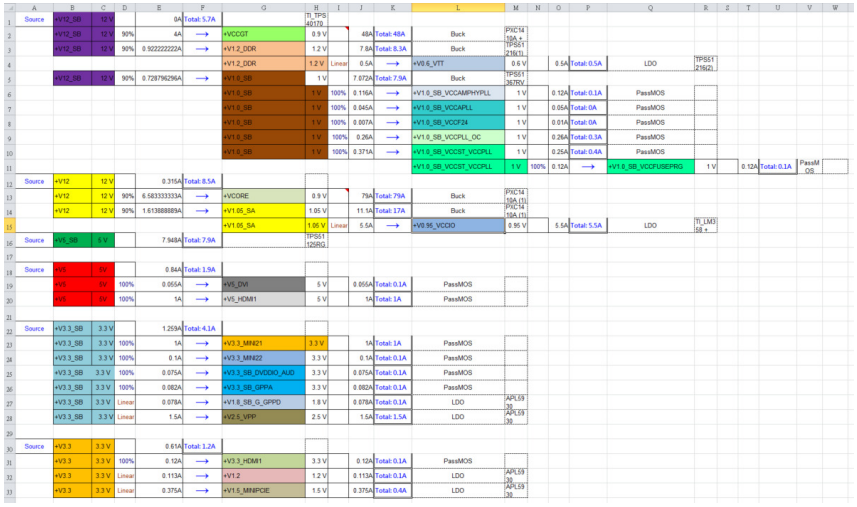
PCE-2129 / PCE-2029 POWER DELIVERY

20180626
Update ok





Total 损耗功率: 19.70 W

Source Power Input Discount 电源及Watt

OrCAD Net name	Voltage	Max Current (A)	P = I x V	Max Power (W)
+V12	12 V	8.51 A	→	102.15 W
+V12_SB	12 V	5.65 A	→	67.81 W
+V5	5V	1.90 A	→	9.48 W
+V5_SB	5 V	7.95 A	→	39.74 W
+V3.3	3.3 V	1.22 A	→	4.02 W
+V3.3_SB	3.3 V	4.09 A	→	13.51 W
		0.00 A		
		0.00 A		
		0.00 A		
		0.00 A		
		0.00 A		
		0.00 A		
		0.00 A		
		Total (Watt)		236.70 W

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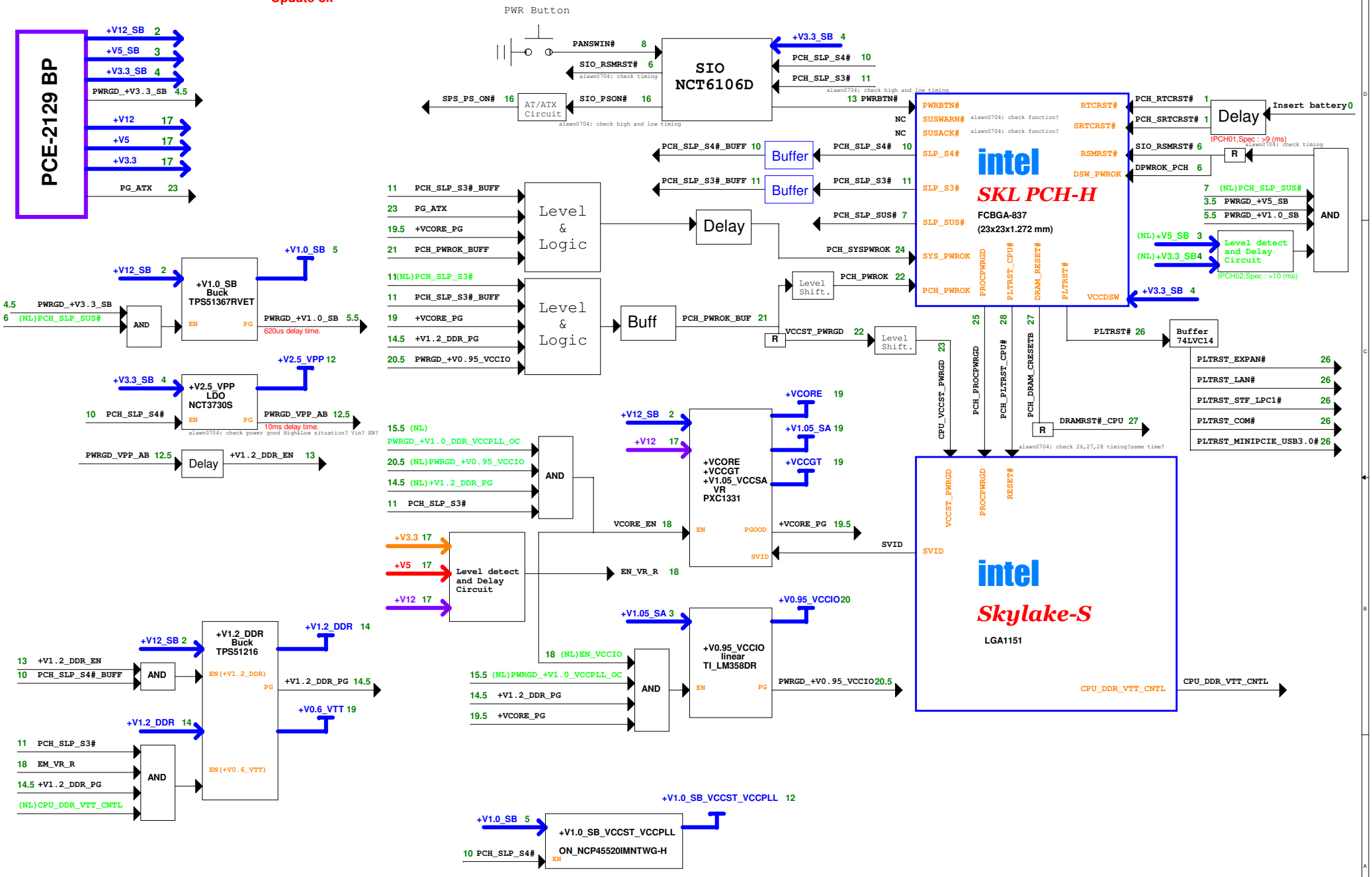
Power On Sequence

20180702
Update ok



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Title	05_Power On Sequence	
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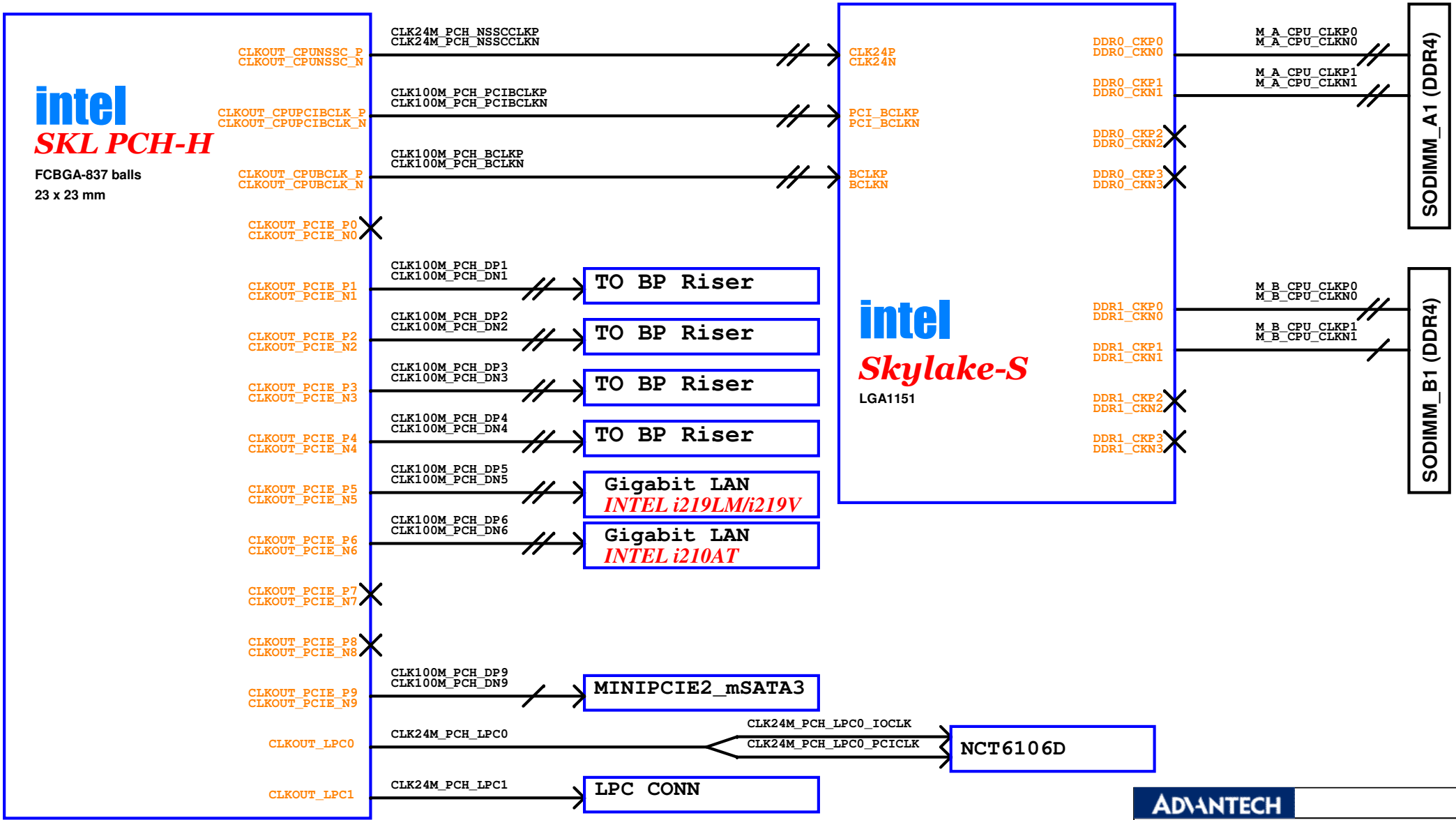
Clocks Distribution

20180625
Update ok



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Title	06_Clocks Distribution	
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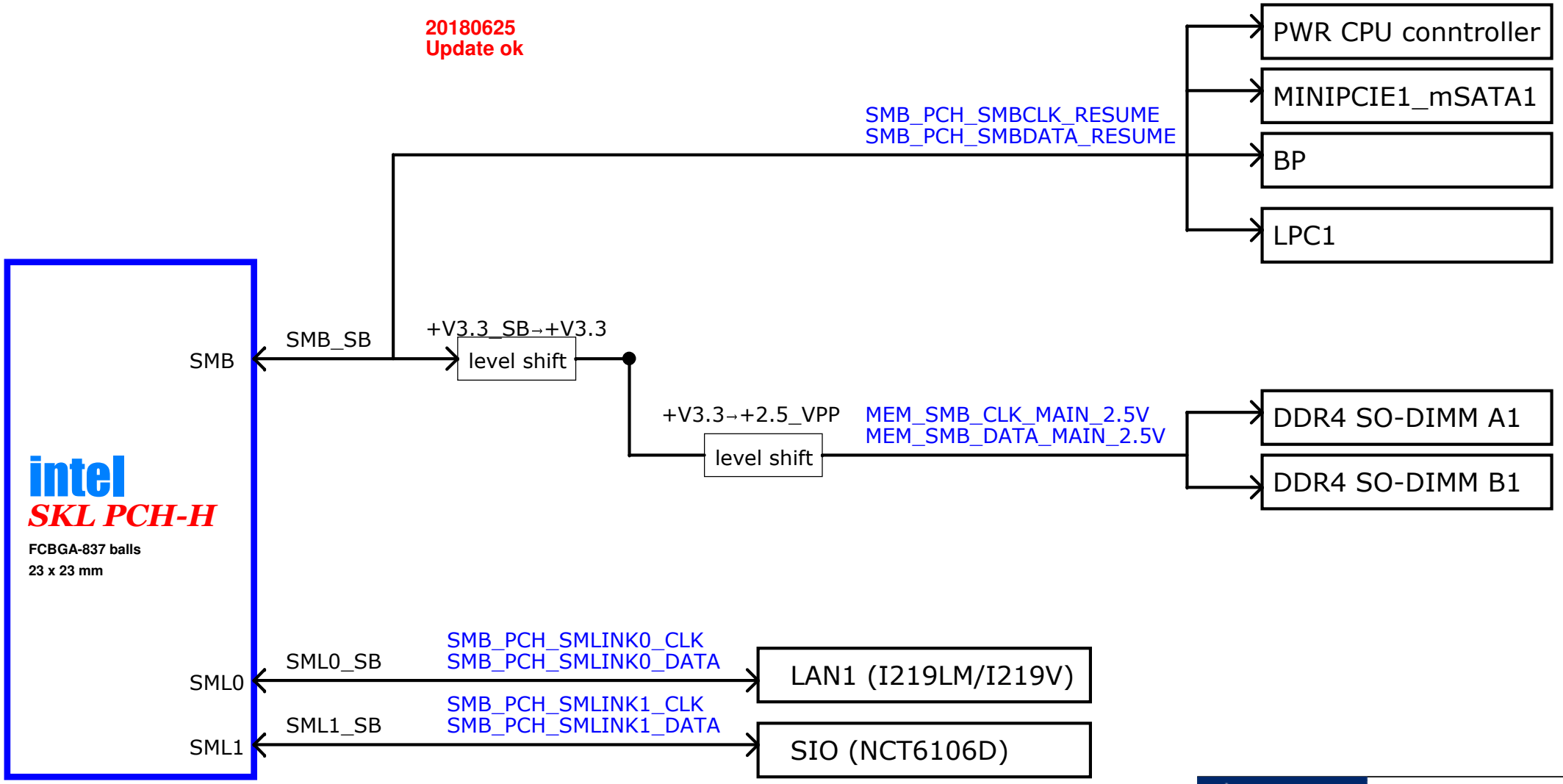
SMBUS Distribution

20180625
Update ok



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Title	07_SMBUS Distribution	
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GPIO LIST

alawn0704(OR): GPIO Follow AIIS-3400

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Title	08_GPIO LIST		
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Identify ID					
	GPP_G8	For PCH Q170 =1 ; H110=0 R8561@ R8564@			
	GPP_G9	For Display DDI2 ; DP=1 ; DVI=0			
	GPP_G10	Reserve			

USB Power Plane/VGA	撥到1位置	撥到8位置	撥到2位置	撥到7位置	撥到4位置	撥到5位置	
LAN1_USB2C1_1	S0	S5	X	X	X	X	
LAN2_USB3C2_1	S0	S5	X	X	X	X	
USB3C1	X	X	S0	S5	X	X	
VGA	X	X	X	X	no force on	force on	

Parameter	Value	Help Text
SATA / PCIe Combo Port 0	PCIe (or GbE)	This setting configures the PCIe port to operate as either PCIe Port 9 or SATA Port 0. For further details on Flex I/O see Skylake H / LP Platform Controller Hub EDS. 0A
SATA / PCIe Combo Port 1	PCIe (or GbE)	This setting configures the PCIe port to operate as either PCIe Port 10 or SATA Port 1. For further details on Flex I/O see Skylake H / LP Platform Controller Hub EDS. 1A
SATA / PCIe Combo Port 2	SATA	This setting configures the PCIe port to operate as either PCIe Port 13 or SATA Port 0. For further details on Flex I/O see Skylake H / LP Platform Controller Hub EDS. 0B
SATA / PCIe Combo Port 3	GPIO	This setting configures the PCIe port to operate as either PCIe Port 14 or SATA Port 1. For further details on Flex I/O see Skylake H / LP Platform Controller Hub EDS. 1B
SATA / PCIe Combo Port 4	SATA	This setting configures the PCIe port to operate as either PCIe Port 15 or SATA Port 2. For further details on Flex I/O see Skylake H / LP Platform Controller Hub EDS.
SATA / PCIe Combo Port 5	SATA	This setting configures the PCIe port to operate as either PCIe Port 16 or SATA Port 3. For further details on Flex I/O see Skylake H / LP Platform Controller Hub EDS.
SATA / PCIe Combo Port 6	PCIe (or GbE)	This setting configures the PCIe port to operate as either PCIe Port 17 or SATA Port 4. For further details on Flex I/O see Skylake H / LP Platform Controller Hub EDS.
SATA / PCIe Combo Port 7	PCIe (or GbE)	This setting configures the PCIe port to operate as either PCIe Port 18 or SATA Port 5. For further details on Flex I/O see Skylake H / LP Platform Controller Hub EDS.
SATA / PCIe Combo Port 8	PCIe (or GbE)	This setting configures the PCIe port to operate as either PCIe Port 19 or SATA Port 6. For further details on Flex I/O see Skylake H Platform Controller Hub EDS. Note: Valid only for Workstation / Server.
SATA / PCIe Combo Port 9	PCIe (or GbE)	This setting configures the PCIe port to operate as either PCIe Port 20 or SATA Port 7. For further details on Flex I/O see Skylake H Platform Controller Hub EDS. Note: Valid only for Workstation / Server.

ADVANTECH

Title: IDENTIFY ID SW1 SETTING

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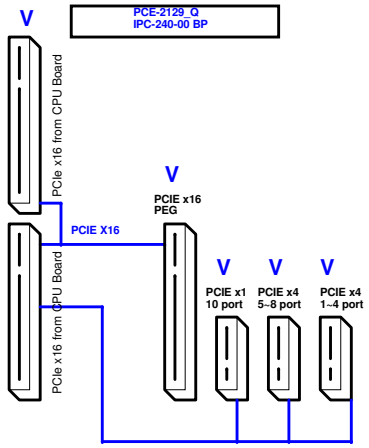

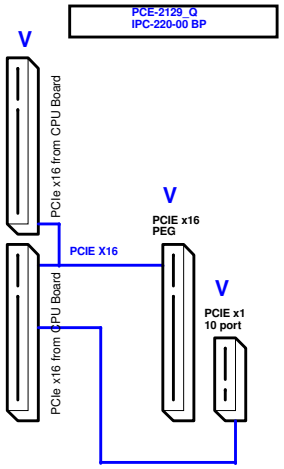

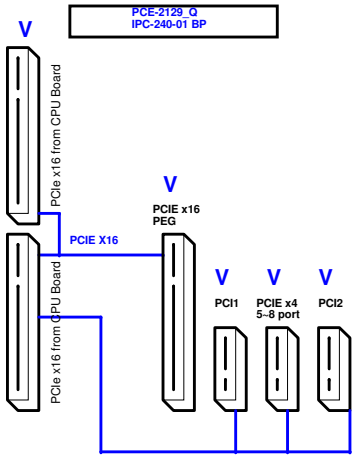

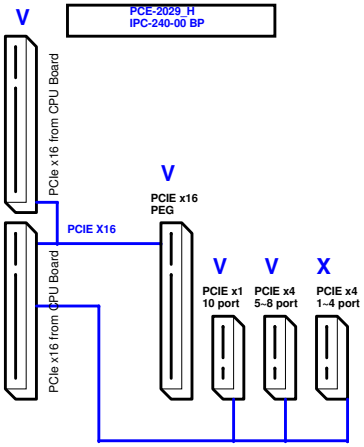

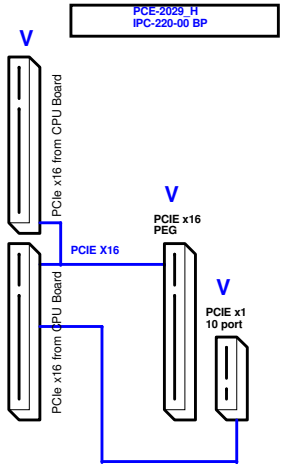

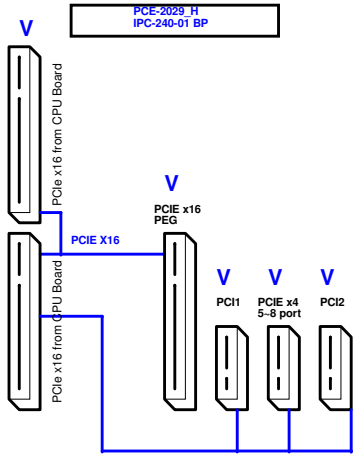

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Title	BLANK	
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A101-1
Wesley0626: Move +V3.3 and +V5 and +V12
ATX_PWROK to BP

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Title	BLANK	
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PWR [VCORE+VSA PWM IC]

+VCORE Iomax=79A
+V1.05_SA Iomax=12.3A
+VCCGT Iomax=51A

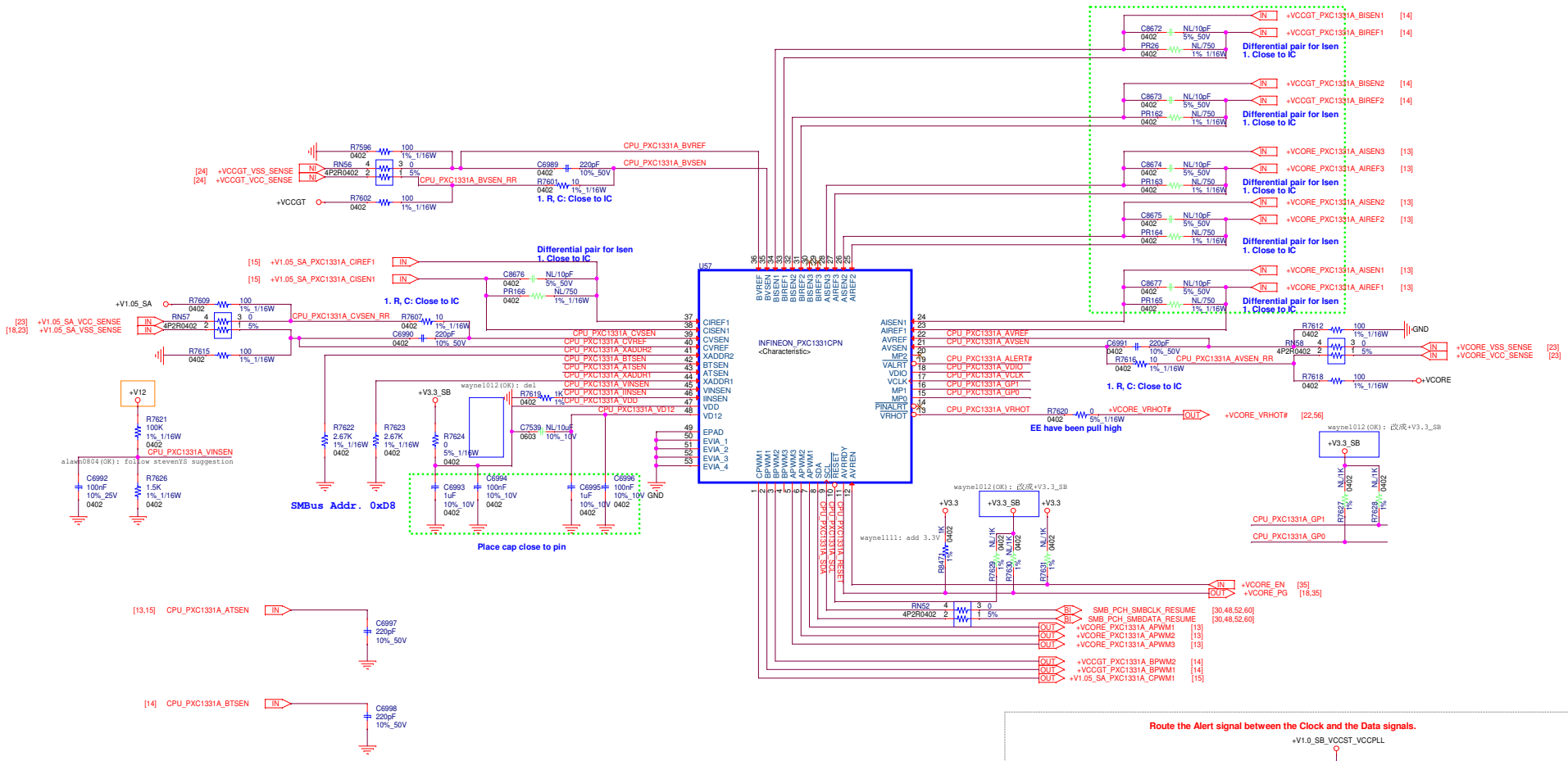
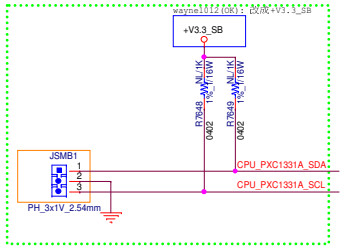
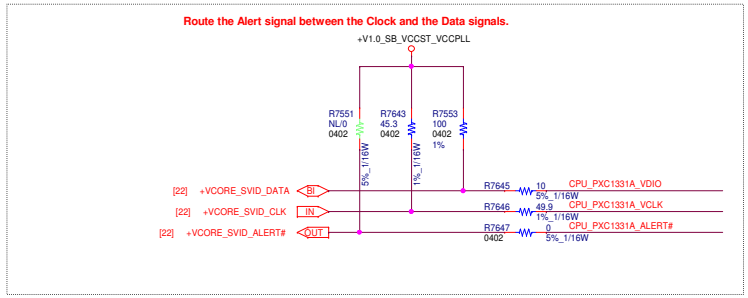


Table 6: Device I2C Slave Address

Resistor-to-GND (1%)		XADDR2							
		2.26 kΩ	2.67 kΩ	3.16 kΩ	4.02 kΩ	5.36 kΩ	8.06 kΩ	16.0 kΩ	Open
XADDR1	2.26 kΩ	FC	DC	BC	9C	7C	5C	3C	1C
	2.67 kΩ	F8	D8	B8	98	78	58	38	reserved
	3.16 kΩ	F4	D4	B4	94	74	54	34	14
	4.02 kΩ	F0	D0	B0	90	70	50	30	10
	5.36 kΩ	EC	CC	AC	8C	6C	4C	2C	0C
	8.06 kΩ	E8	C8	A8	88	68	48	28	08
	16.0 kΩ	E4	C4	A4	84	64	44	24	04
	Open	E0	C0	A0	80	60	40	20	reserved



For program purpose



ADVANTECH			
Title	12_PWR CPU_Controller		
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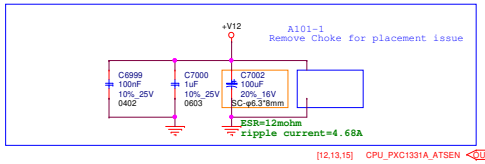
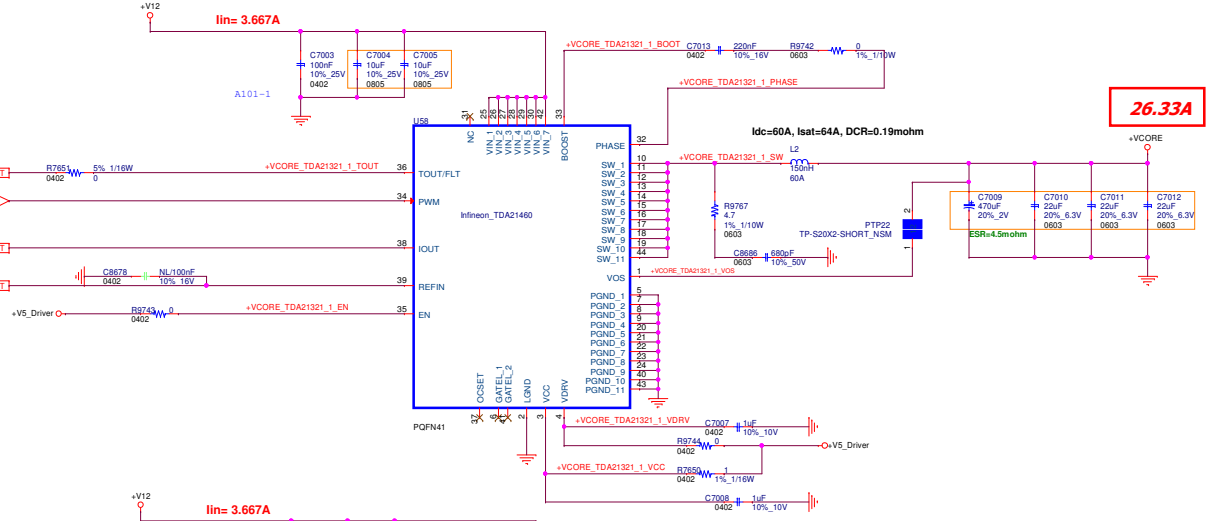
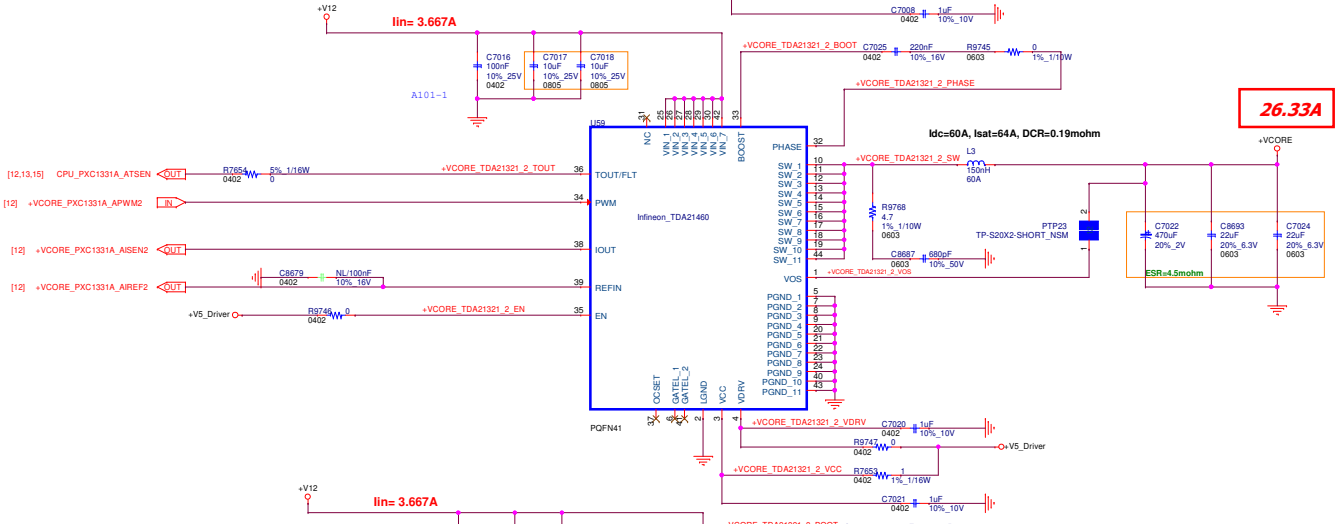
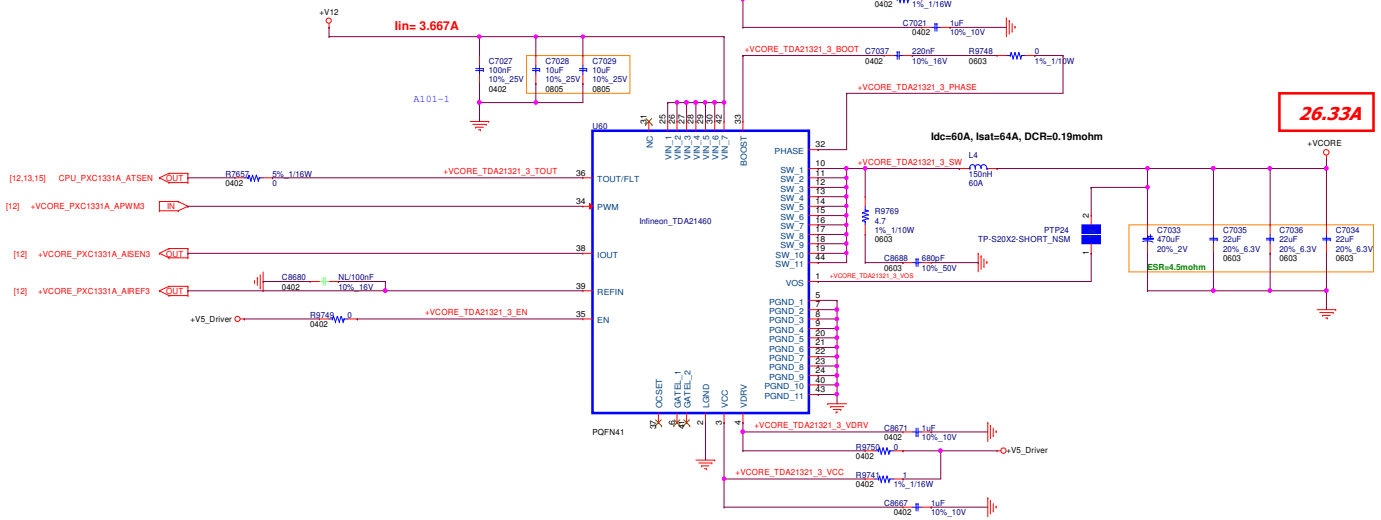
PWR [VCORE_Phase1-3]

+VCORE Iomax=79A









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Title	13_PWR +VCORE_Phase1-3		
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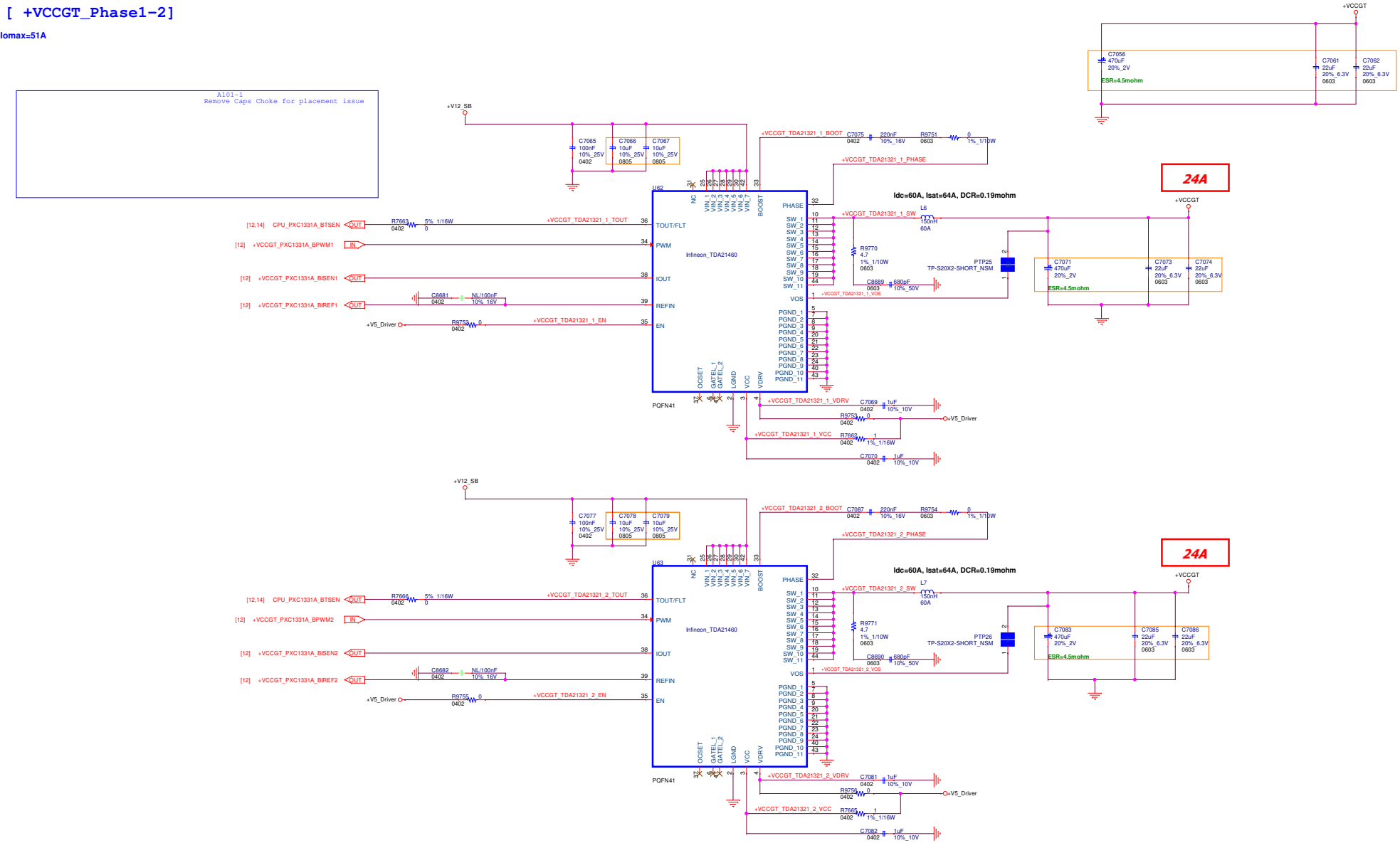
PWR [+VCCGT_Phase1-2]

+VCCGT Iomax=51A

A101-1
Remove Caps Choke for placement issue



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Title	14_PWR +VCCGT_Phase1-2	
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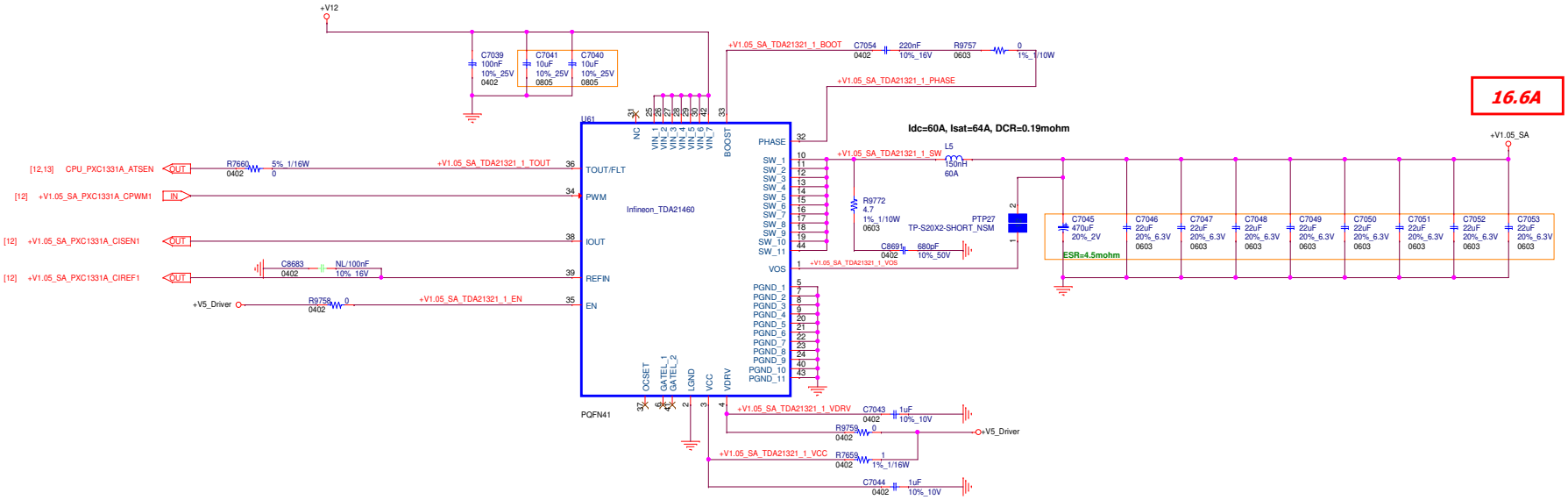
PWR [VSA_Phase1]

+V1.05_SA Iomax=12.3A



Title	15_PWR +VCCSA		
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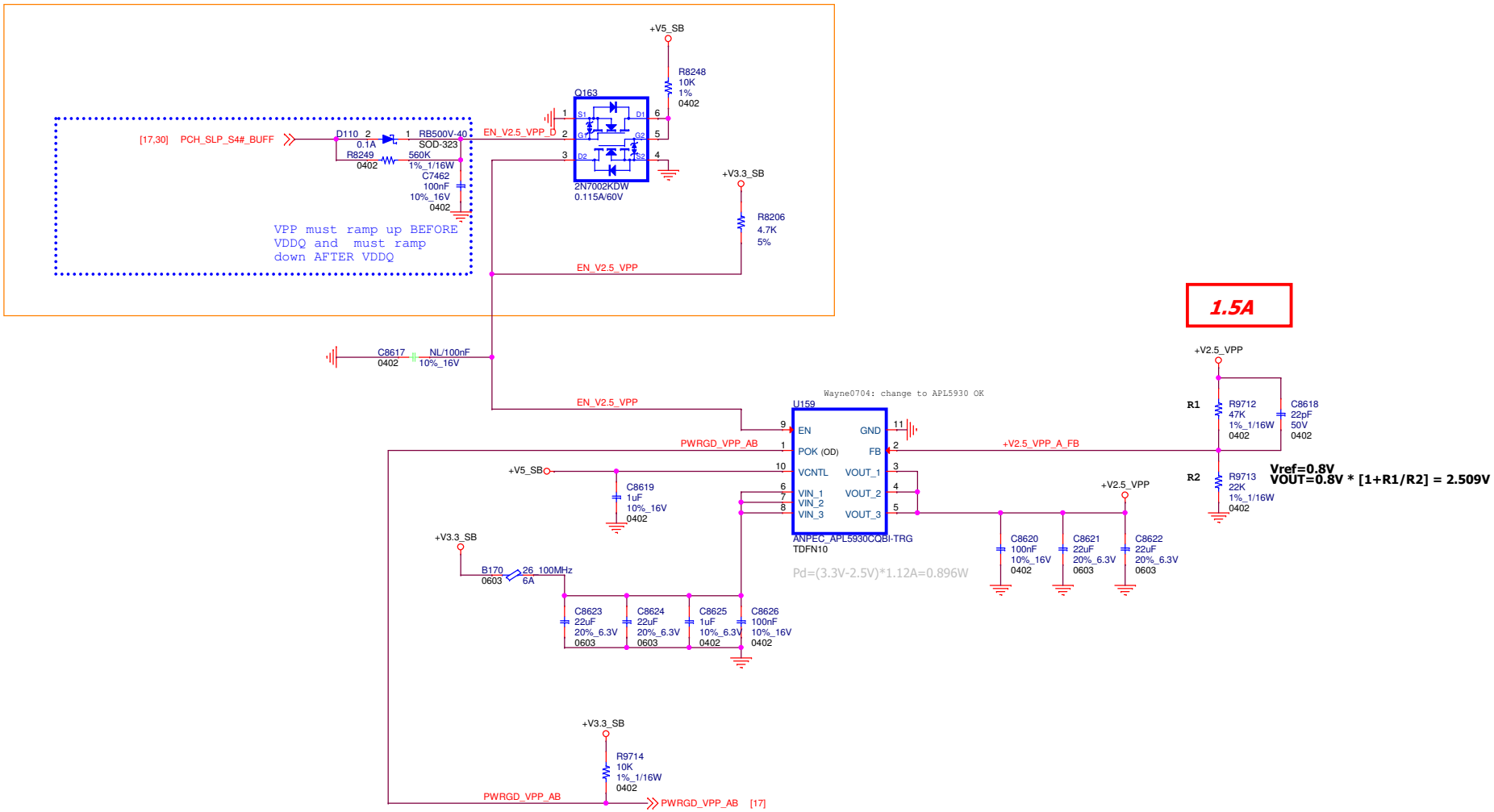
PWR DDR4 +V2.5_VPP



ADVANTECH		
Title	16_PWR DDR4 +V2.5_VPP	
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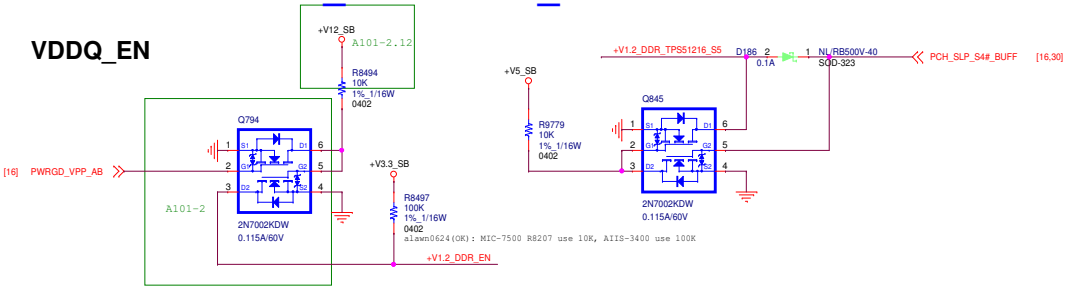
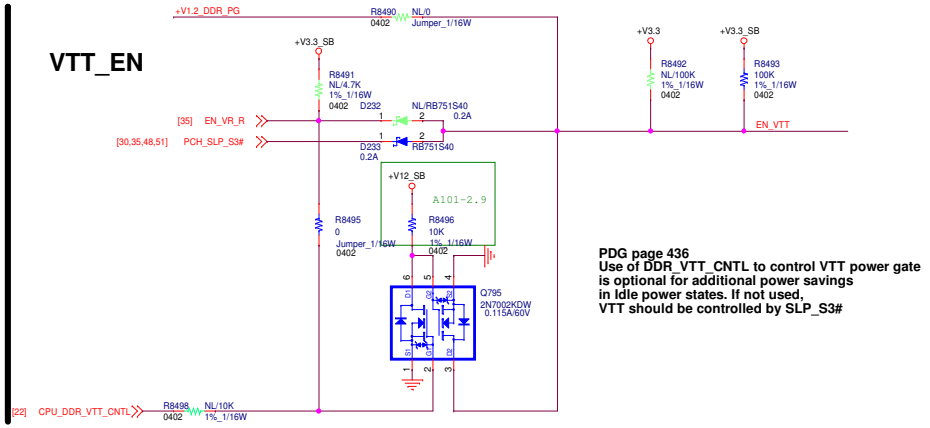
PWR DDR4 +V1.2_DDR/+V0.6_VTT

VDDQ_EN

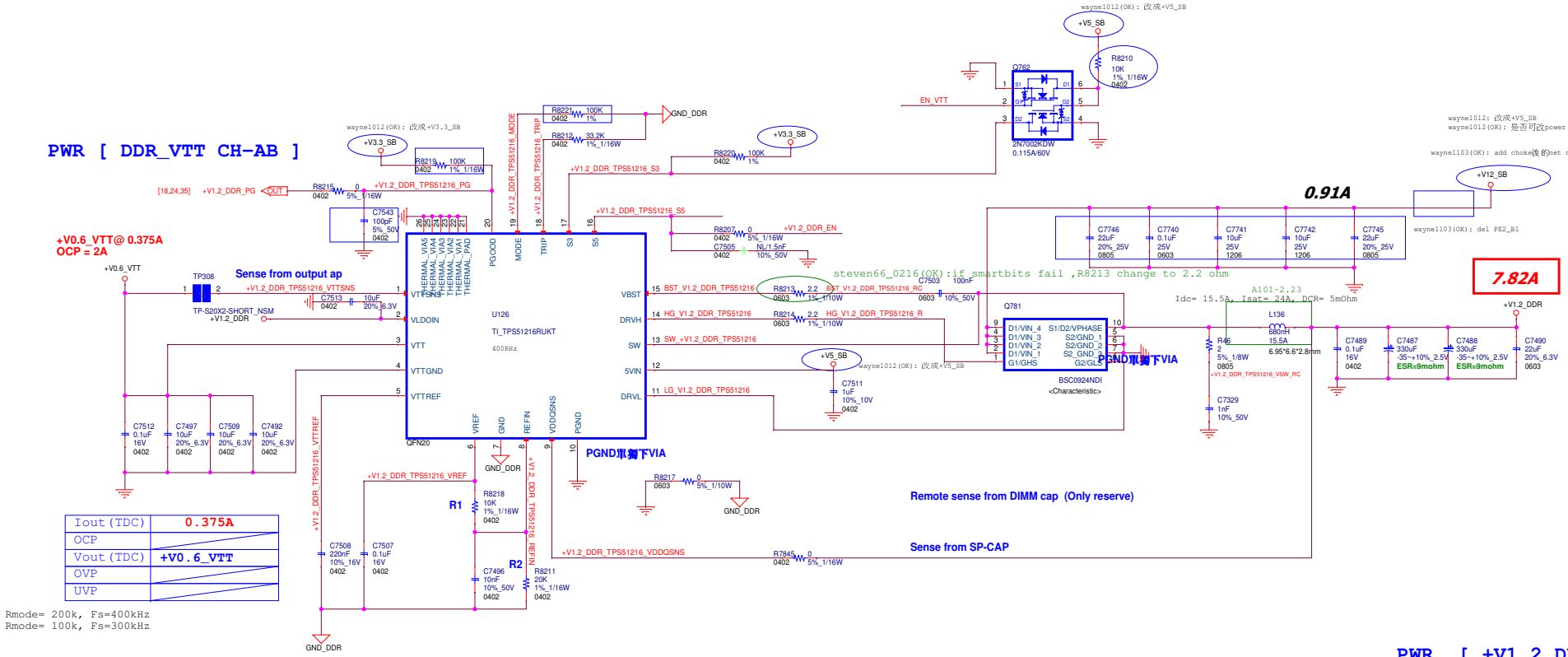


VTT_EN



PDG page 436
Use of DDR_VTT_CNTL to control VTT power gate is optional for additional power savings in Idle power states. If not used, VTT should be controlled by SLP_S3#

PWR [DDR_VTT CH-AB]



Iout(TDC)	0.375A
OCP	
Vout(TDC)	+V0.6_VTT
OVP	
UVP	

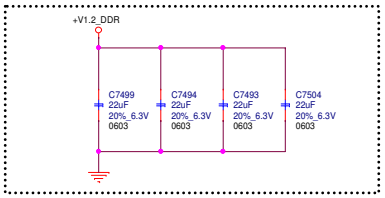
Rmode= 200k, Fs=400kHz
Rmode= 100k, Fs=300kHz

Vtrip(mV) = Rtrip(Kohm) x 10uA = 33.2Kx10uA = 332mV
Iocl = Vtrip /8 x Rdson + Iripple/2
= Vtrip / 8 x Rdson + (1/ (2 x L x f)) x ((Vin-Vout)xVout)/Vin
= 332mV / 8 x 4.6mohm + 1.676
~= 10.698A

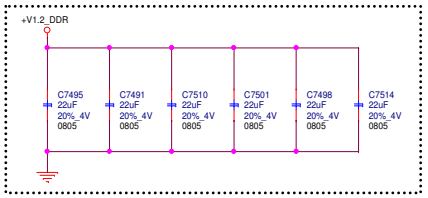
R2 = R1 / [(Vref / Vout) -1]
= 10K / [(1.8 / 1.2) - 1]
=20K

Table 2. MODE Selection

MODE NO.	RESISTANCE BETWEEN MODE AND GND (kΩ)	SWITCHING FREQUENCY (kHz)	DISCHARGE MODE
3	200	400	Tracking
2	100	300	
1	68	300	Non-tracking
0	47	400	



DIMM to CPU socket



close to DIMM

PWR [+V1.2_DDR PWM IC]

Power rail: +V1.2_DDR
Iomax=8.19A
OCP=10.698A
Fsw=400KHz
Delta I=3.353A
1/2 Delta I=1.675A
SS=1.1ms

ADVANTECH

Title	17_PWR DDR4 +V1.2_DDR/+V0.6_VTT	
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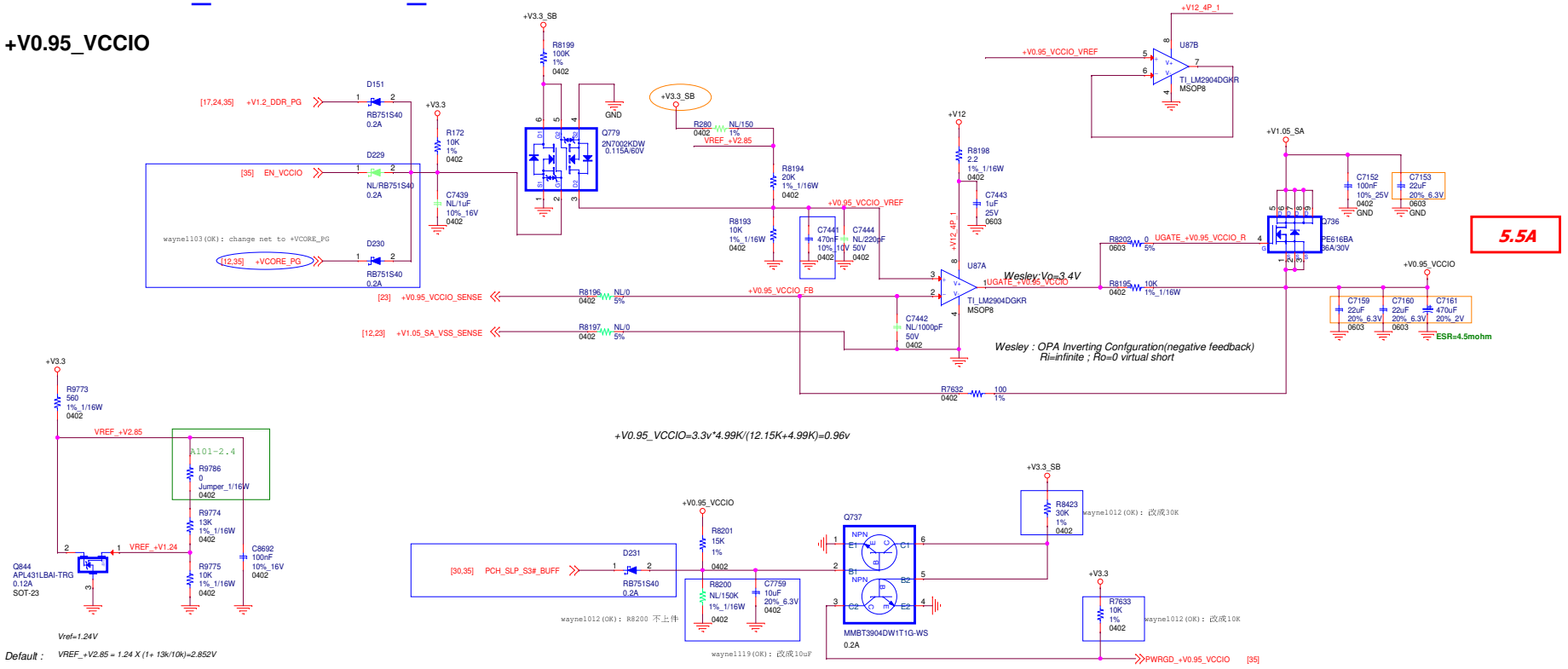
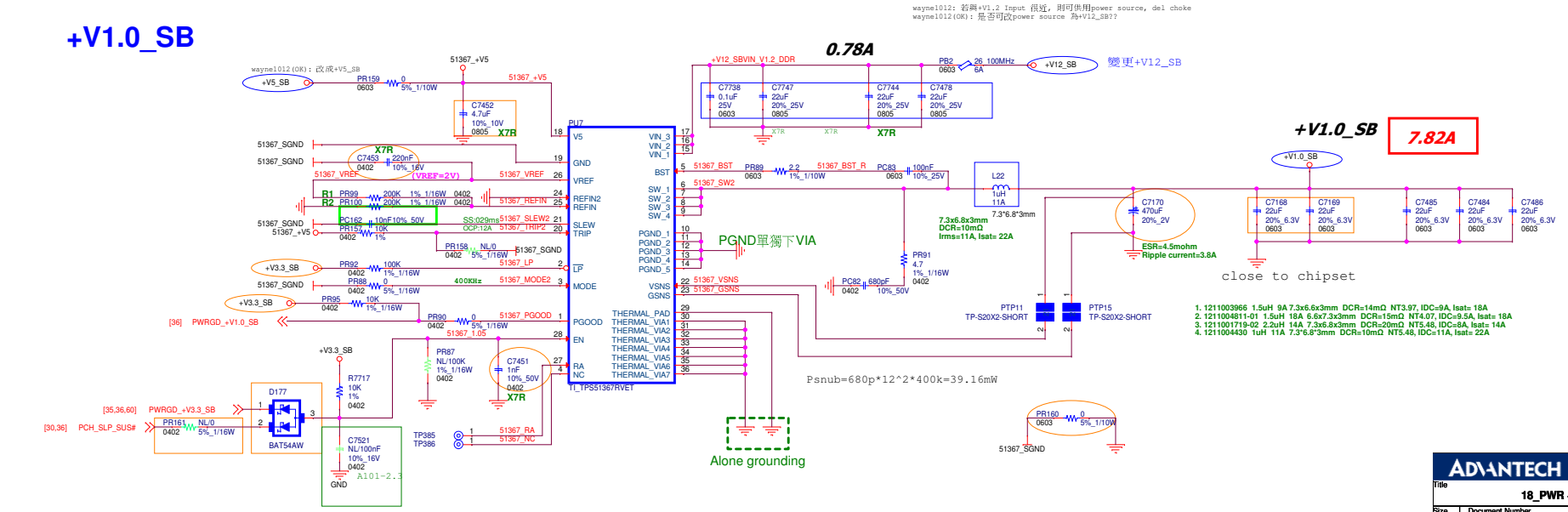
PWR +V0.95_VCCIO/+V1.0_SB

+V0.95_VCCIO



+V1.0_SB



Output Voltage use "TPS51367_2_3 Design Tool_0.53C.xls" to know R1 and R2

ADVANTECH

Title	18_PWR +V0.95_VCCIO/+V1.0_SB	
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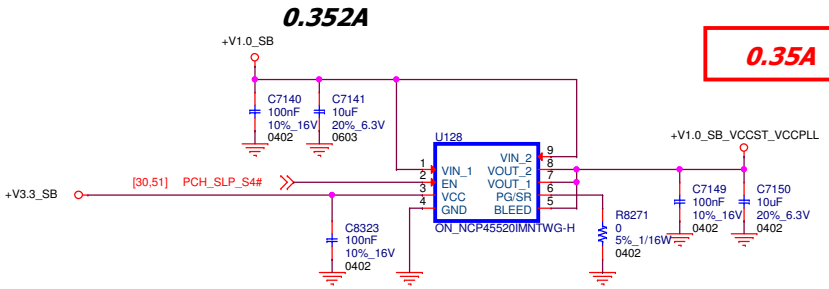
PWR [CPU_VCCPLL_OC]

A101-1
Wesley0626: Del +V1.0_SB_VCCPLL_OC

PWR [CPU_VCCST_VCCPLL]



ADVANTECH

Title	19_PWR VCCST/VCCPLL_OC	
Size	Document Number PCE-2129(2029)	Rev A101-2
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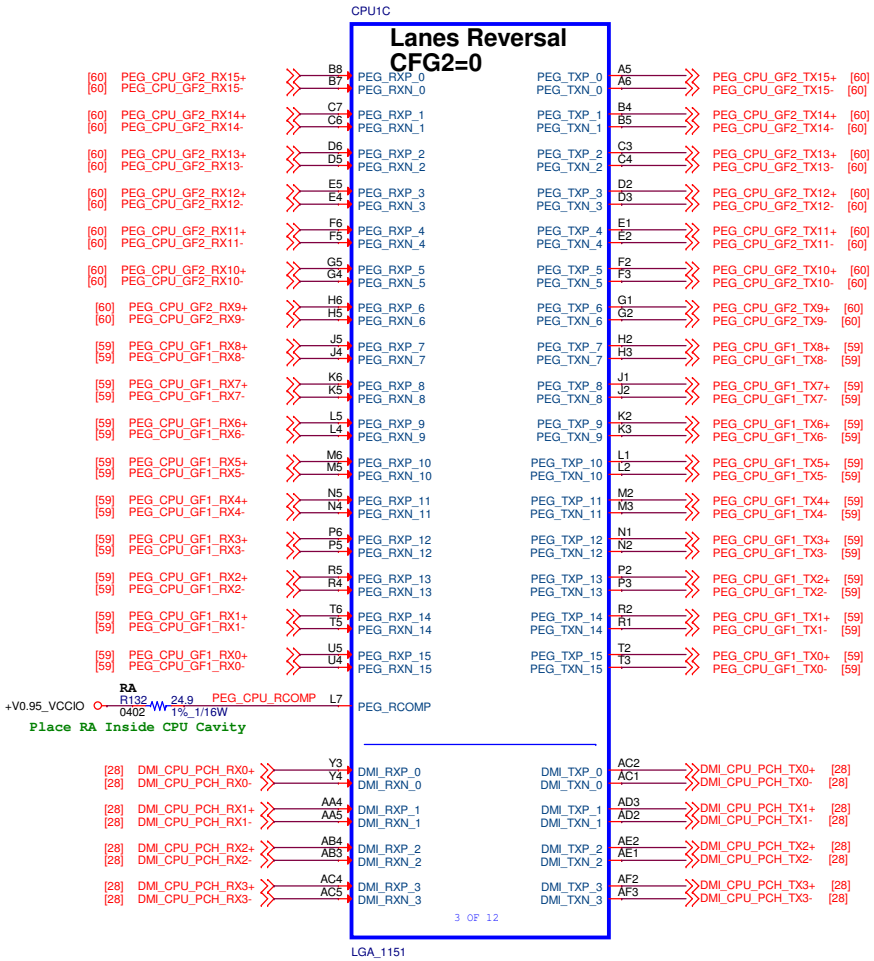
CPU PEG/DMI/DDI



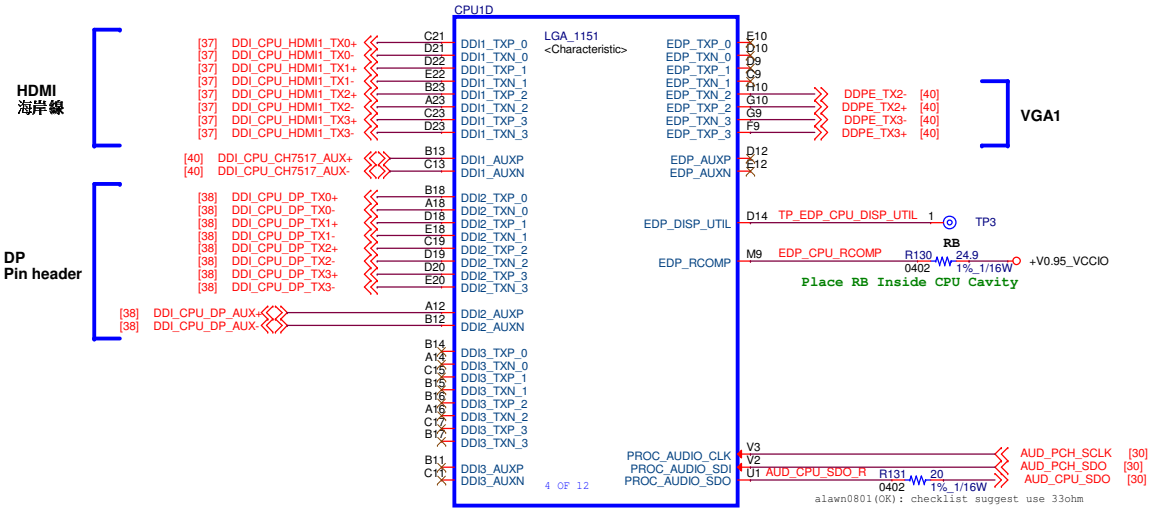


Table 2-24. embedded DisplayPort* (eDP*)/DDI Ports Availability

Ports	Port name in VBT	Y/U-Processor Line [3,4]	H-Processor Line [3,4]	S-Processor Line (DT) [3,4]	S-Processor Line (AIO) [3,4]
DDI0 - eDP*	Port A	Yes	Yes	No[1]	Yes
DDI1	Port B	Yes	Yes	Yes	Yes
DDI2	Port C	Yes	Yes	Yes	Yes
DDI3	Port D	No[5]	Yes	Yes	Yes
DDI4 - eDP*	Port E	No	Yes[2]	Yes[2]	Yes[2]

Notes:
1. Port A is for embedded display. No Embedded display for DT.
2. Port E is bifurcated from eDP*, need to use available AUX (if HDMI* is in used).
   a. For example, DT can use eDP_AUX for VGA converter which is available as free Design but HPD must be used as DDPE_HPD3.
3. 3xDDC (DDPB, DDPC, DDPD) are valid for all processor SKUs (for Y/U-processor lines DDC signals description, refer to PCH-U/Y EDSDatasheet Volume 1 CDI#545659).
4. 5xHPD (PCH) inputs (eDP_HPD, DDPB_HPD0, DDPC_HPD1, DDPD_HPD2, DDPE_HPD3) are valid for all processor SKUs.
5. No Port D for U-processor line, DDI3_AUX are exists as reserved.
6. VBT provides a configuration option to select the four AUX channels A/B/C/D for a given port, based on how the aux channel lines are connected physically on the board

Display Signal Mapping

Table 50-4. Digital Display Interface Signal Mapping

Port	DDI PROCESSOR Pin Names	Display Port Mapping	HDMI* Mapping
Port 1	DDI1_TXN[0]	DDI1_LANE0_DN	HDMIxC_TX2_DN
	DDI1_TXP[0]	DDI1_LANE0_DP	HDMIxC_TX2_DP
	DDI1_TXN[1]	DDI1_LANE1_DN	HDMIxC_TX1_DN
	DDI1_TXP[1]	DDI1_LANE1_DP	HDMIxC_TX1_DP
	DDI1_TXN[2]	DDI1_LANE2_DN	HDMIxC_TX0_DN
	DDI1_TXP[2]	DDI1_LANE2_DP	HDMIxC_TX0_DP
	DDI1_TXN[3]	DDI1_LANE3_DN	HDMIxC_CLK_DN
	DDI1_TXP[3]	DDI1_LANE3_DP	HDMIxC_CLK_DP
	DDPB_HPD	DDI1_HPD_Q	DDI1_HPD_Q
	DDPB_CTRLCLK	NA	DDI1_CTRL_CK
	DDPB_CTRLDATA	NA	DDI1_CTRL_DATA
Port 2	DDI2_TXN[0]	DDI2_LANE0_DN	HDMIxC_TX2_DN
	DDI2_TXP[0]	DDI2_LANE0_DP	HDMIxC_TX2_DP
	DDI2_TXN[1]	DDI2_LANE1_DN	HDMIxC_TX1_DN
	DDI2_TXP[1]	DDI2_LANE1_DP	HDMIxC_TX1_DP
	DDI2_TXN[2]	DDI2_LANE2_DN	HDMIxC_TX0_DN
	DDI2_TXP[2]	DDI2_LANE2_DP	HDMIxC_TX0_DP
	DDI2_TXN[3]	DDI2_LANE3_DN	HDMIxC_CLK_DN
	DDI21_TXP[3]	DDI2_LANE3_DP	HDMIxC_CLK_DP
	DDPC_HPD	DDI2_HPD_Q	DDI2_HPD_Q
	DDPC_CTRLCLK	NA	DDI2_CTRL_CK
	DDPC_CTRLDATA	NA	DDI2_CTRL_DATA
Port 3	DDI3_TXP[0]	DDI3_LANE0_DP	HDMIx_TX2_DP
	DDI3_TXN[0]	DDI3_LANE0_DN	HDMIx_TX2_DN
	DDI3_TXP[1]	DDI3_LANE1_DP	HDMIx_TX1_DP
	DDI3_TXN[1]	DDI3_LANE1_DN	HDMIx_TX1_DN
	DDI3_TXP[2]	DDI3_LANE2_DP	HDMIx_TX0_DP
	DDI3_TXN[2]	DDI3_LANE2_DN	HDMIx_TX0_DN
	DDI3_TXP[3]	DDI3_LANE3_DP	HDMIx_CLK_DP
	DDI3_TXN[3]	DDI3_LANE3_DN	HDMIx_CLK_DN
	Hot plug detect used by HDMI Port 3	DDPD_HPD	DDI3_HPD_Q
	HDMI DDC lines for Port 3	DDPD_CTRLCLK	DDI3_CTRL_CK
		DDPD_CTRLDATA	DDI3_CTRL_DATA

ADVANTECH

Title	20_CPU PEG/DMI/DDI	
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CPU DDR4 MA/MB

M_A_CPU_MA[16..0] [26]
M_A_CPU_DQ[63..0] [26]
M_A_CPU_DQSP[8..0] [26]
M_A_CPU_DQSN[8..0] [26]
M_A_CPU_ECC[7..0] [26]

M_B_CPU_MA[16..0] [27]
M_B_CPU_DQ[63..0] [27]
M_B_CPU_DQSP[8..0] [27]
M_B_CPU_DQSN[8..0] [27]
M_B_CPU_ECC[7..0] [27]

CPU1A

LGA_1151
<Characteristic>

1 OF 12

CPU1B

LGA_1151
<Characteristic>

2 OF 12

Title	21_CPU DDR4 MA/MB	
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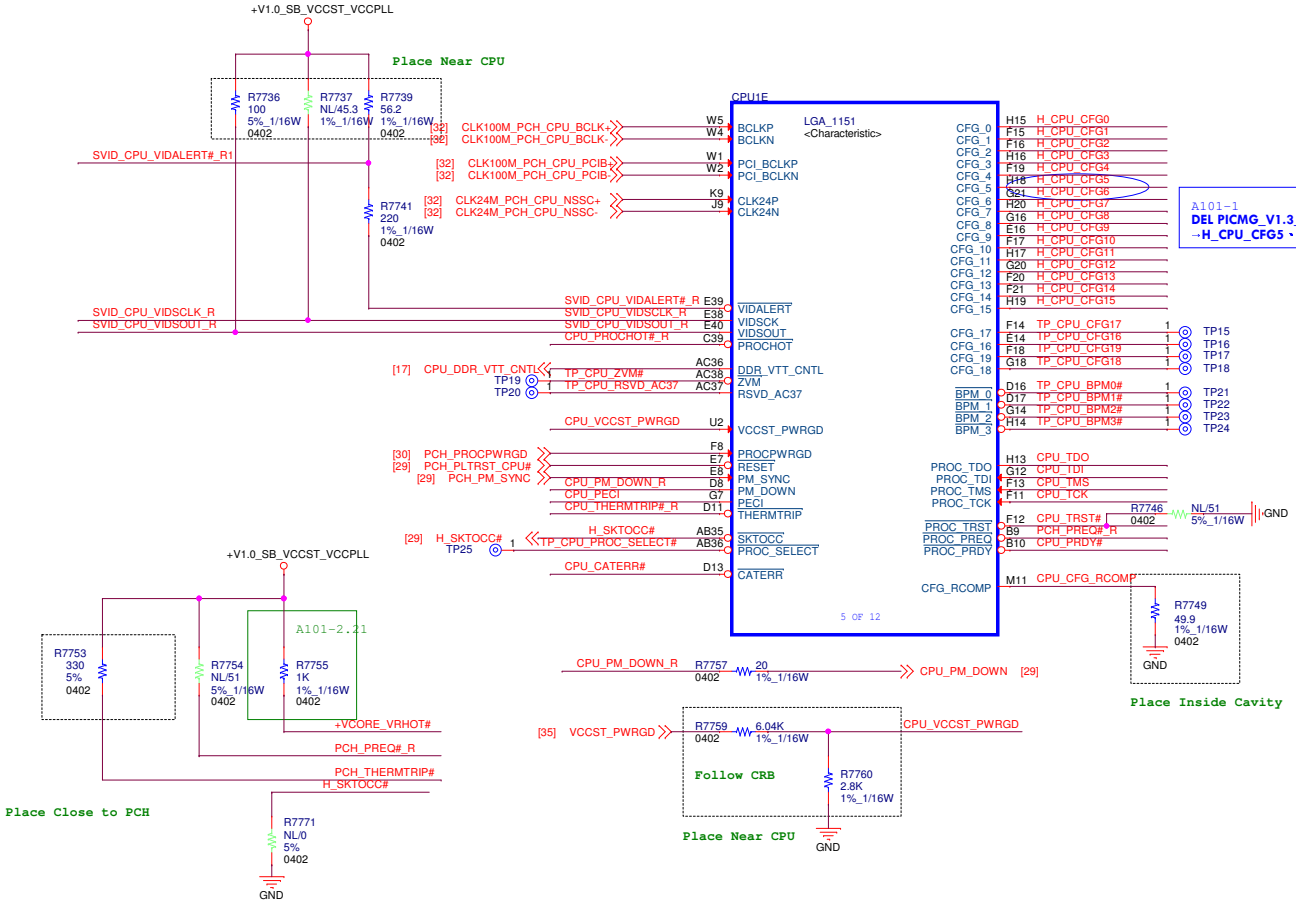
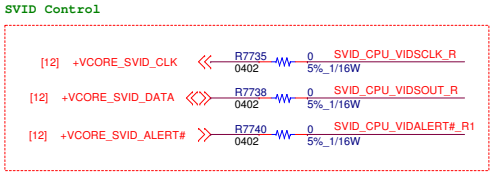
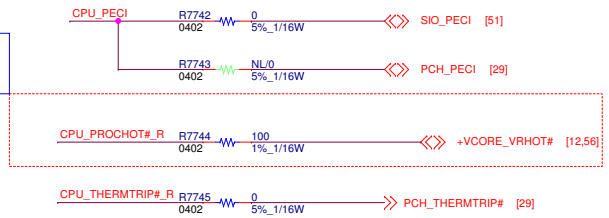
CPU MISC/CFG

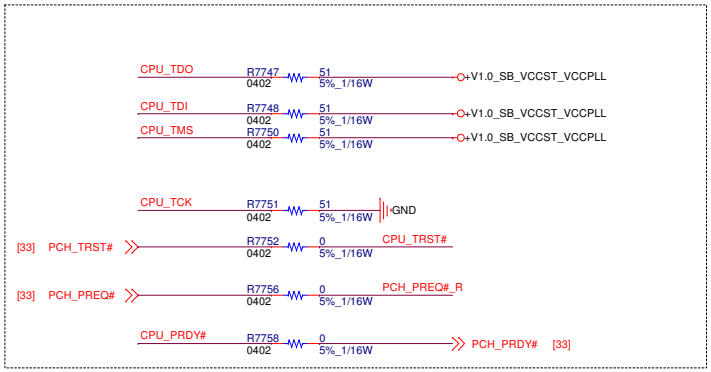


SVID Control

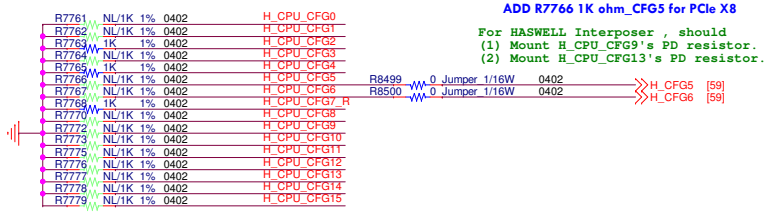




JTAGE



Configuration Signals:



ADD R7766 1K ohm_CFG5 for PCIe X8

For HASWELL Interposer , should
(1) Mount H_CPU_CFG9's PD resistor.
(2) Mount H_CPU_CFG13's PD resistor.

Error Signal

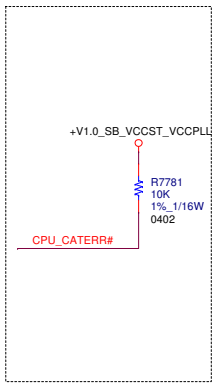


Table 2-17. PCI Express* Bifurcation and Lane Reversal Mapping

Bifurcation	Link Width			Config. Signals			Lanes													
	0:1:0	0:1:1	0:1:2	CFG [6]	CFG [5]	CFG [2]	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1x16	x16	N/A	N/A	1	1	1	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1x16 **Reversed**	x16	N/A	N/A	1	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2x8	x8	x8	N/A	1	0	1	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
2x8 **Reversed**	x8	x8	N/A	1	0	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
1x8+2x4	x8	x4	x4	0	0	1	0	1	2	3	4	5	6	7	0	1	2	3	0	1	2	3
1x8+2x4 **Reversed**	x8	x4	x4	0	0	0	3	2	1	0	3	2	1	0	7	6	5	4	3	2	1	0

Notes:
1. For CFG bus further details, refer to Section 6.4.
2. Support is also provided for narrow width and use devices with lower number of lanes (that is, usage on x4 configuration), however further bifurcation is not supported.
3. In case that more than one device is connected, the device with the highest lane count, should always be connected to the lower lanes, as follows:
   — Connect lane 0 of 1st device to lane 0.
   — Connect lane 0 of 2nd device to lane 8.
   — Connect lane 0 of 3rd device to lane 12.

   For example:
   a. When using 1x8 + 2x4, the 8 lane device must use lanes 0:7.
   b. When using 1x4 + 1x2, the 4 lane device must use lanes 0:3, and other 2 lanes device must use lanes 8:9.
   c. When using 1x4 + 1x2 + 1x1, 4 lane device must use lanes 0:3, two lane device must use lanes 8:9, one lane device must use lane 12.

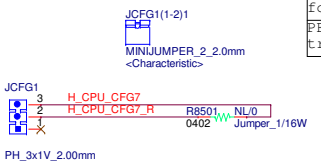
CFG[0]: Stall reset sequence after PCU PLL lock until de-asserted:
– 1 = (Default) Normal Operation;No stall.
– 0 = Stall.

CFG[2]: PCI Express* Static x16 Lane Numbering Reversal.
– 1 = (Default) Normal operation
– 0 = Lane numbers reversed.

CFG[4]: eDP enable:
– 1 = Disabled.
– 0 = (Default) Enabled.

CFG[6:5]: PCI Express* Bifurcation
– 00 = 1 x8, 2 x4 PCI Express*
– 01 = reserved
– 10 = 2 x8 PCI Express*
– 11 = (Default) 1 x16 PCI Express*

CFG[7]: PEG Training:
– 1 = (default) PEG Train immediately following RESET# de assertion.
– 0 = PEG Wait for BIOS for training.



Mode	Jumper Setting
PEG Train immediately following RESET# de-assertion.	1-2 Short (Default)
PEG Wait for BIOS for training.	2-3 Short

ADVANTECH

Title	22_CPU MISC/CFG	
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CPU VCORE/VCCSA POWER

0.55(V)~1.5(V)@+VCORE

79(A)@+VCORE

Place Caps at TOP socket edge

C7174 22uF 20%_6.3V 0603
C7175 22uF 20%_6.3V 0603
C7176 22uF 20%_6.3V 0603
C7171 22uF 20%_6.3V 0603

Place all above caps on TOP side of CPU cavity

C7173 22uF 20%_6.3V 0603
C7183 22uF 20%_6.3V 0603
C7184 22uF 20%_6.3V 0603
C7185 22uF 20%_6.3V 0603
C7186 22uF 20%_6.3V 0603
C7187 22uF 20%_6.3V 0603
C7192 22uF 20%_6.3V 0603
C7193 22uF 20%_6.3V 0603
C7194 22uF 20%_6.3V 0603
C7195 22uF 20%_6.3V 0603
C7196 22uF 20%_6.3V 0603
C7197 22uF 20%_6.3V 0603
C8704 22uF 20%_6.3V 0603
C8703 22uF 20%_6.3V 0603
C7198 22uF 20%_6.3V 0603
C7199 22uF 20%_6.3V 0603
C7200 22uF 20%_6.3V 0603
C7201 22uF 20%_6.3V 0603

Place all below caps on BOTTOM side near CPU socket

C7204 22uF 20%_6.3V 0603
C7205 22uF 20%_6.3V 0603
C7206 22uF 20%_6.3V 0603
C7207 22uF 20%_6.3V 0603
C7208 22uF 20%_6.3V 0603
C7209 22uF 20%_6.3V 0603
C7210 22uF 20%_6.3V 0603
C7211 22uF 20%_6.3V 0603
C7212 22uF 20%_6.3V 0603
C7213 22uF 20%_6.3V 0603
C7214 22uF 20%_6.3V 0603
C7215 22uF 20%_6.3V 0603

+VCORE

CPU1G
LGA_1151
<Characteristic>

VCC_A25 A25, VCC_A26 A26, VCC_A27 A27, VCC_A28 A28, VCC_A29 A29, VCC_A30 A30, VCC_B25 B25, VCC_B27 B27, VCC_B29 B29, VCC_B31 B31, VCC_B32 B32, VCC_B33 B33, VCC_B34 B34, VCC_B35 B35, VCC_B36 B36, VCC_B37 B37, VCC_C25 C25, VCC_C26 C26, VCC_C27 C27, VCC_C28 C28, VCC_C29 C29, VCC_C30 C30, VCC_C32 C32, VCC_C34 C34, VCC_C36 C36, VCC_D25 D25, VCC_D27 D27, VCC_D29 D29, VCC_D31 D31, VCC_D32 D32, VCC_D33 D33, VCC_D34 D34, VCC_D35 D35, VCC_D36 D36, VCC_E24 E24, VCC_E25 E25, VCC_E26 E26, VCC_E27 E27, VCC_E28 E28, VCC_E29 E29, VCC_E30 E30, VCC_E32 E32, VCC_E34 E34, VCC_E36 E36, VCC_F23 F23, VCC_F24 F24, VCC_F25 F25, VCC_F27 F27, VCC_F29 F29, VCC_F31 F31, VCC_G30 G30, VCC_G32 G32, VCC_H22 H22, VCC_H23 H23, VCC_H25 H25, VCC_H27 H27, VCC_H29 H29, VCC_H31 H31

VCC_AJ11 AJ11, VCC_AJ13 AJ13, VCC_AJ15 AJ15, VCC_AJ17 AJ17, VCC_AJ19 AJ19, VCC_AJ21 AJ21

VCC_H32 H32, VCC_J21 J21, VCC_F32 F32, VCC_F33 F33, VCC_F34 F34, VCC_G23 G23, VCC_G24 G24, VCC_G25 G25, VCC_G26 G26, VCC_G27 G27, VCC_G28 G28, VCC_G29 G29, VCC_J22 J22, VCC_J23 J23, VCC_J24 J24, VCC_J25 J25, VCC_J26 J26, VCC_J27 J27, VCC_J28 J28, VCC_J29 J29, VCC_J30 J30, VCC_J31 J31, VCC_K16 K16, VCC_K18 K18, VCC_K20 K20, VCC_K21 K21, VCC_K23 K23, VCC_K25 K25, VCC_K27 K27, VCC_K29 K29, VCC_K31 K31, VCC_L14 L14, VCC_L15 L15, VCC_L16 L16, VCC_L17 L17, VCC_L18 L18, VCC_L19 L19, VCC_L20 L20, VCC_L21 L21, VCC_L22 L22, VCC_L23 L23, VCC_L24 L24, VCC_L25 L25, VCC_L26 L26, VCC_L27 L27, VCC_L28 L28, VCC_L29 L29, VCC_L30 L30, VCC_M13 M13, VCC_M14 M14, VCC_M16 M16, VCC_M18 M18, VCC_M20 M20, VCC_M22 M22, VCC_M24 M24, VCC_M26 M26, VCC_M28 M28, VCC_M30 M30

VCC_AJ12 AJ12, VCC_AJ14 AJ14, VCC_AJ16 AJ16, VCC_AJ18 AJ18, VCC_AJ20 AJ20, VCC_AJ22 AJ22

7 OF 12

VCC_SENSE C38, VSS_SENSE D38

R7784 0402 NL/49.9 1% 1/16W

+VCORE_VCC_SENSE [12]
+VCORE_VSS_SENSE [12]

11.1(A)@+V1.05_SA

+V1.05_SA

Place all caps inside CPU socket cavity TOP

C7177 47uF 20%_6.3V 0805
C7178 47uF 20%_6.3V 0805

5.5(A)@+V0.95_VCCIO

Place all caps inside CPU socket cavity TOP

C8713 1nF 10%_50V 0402
C7182 22uF 20%_6.3V 0603
C7188 22uF 20%_6.3V 0603
C7189 22uF 20%_6.3V 0603
C7190 22uF 20%_6.3V 0603
C7191 22uF 20%_6.3V 0603

+V0.95_VCCIO

CPU1L
LGA_1151
<Characteristic>

VCCSA_1 AA7, VCCSA_2 AB6, VCCSA_3 AB7, VCCSA_4 AB8, VCCSA_5 AC7, VCCSA_6 AC8, VCCSA_7 N7, VCCSA_8 P7, VCCSA_9 R7, VCCSA_10 T7, VCCSA_11 U7, VCCSA_12 Y6, VCCSA_13 Y7, VCCSA_14 Y8, VCCSA_15 W7, VCCSA_16 V7, VCCSA_17 AA6

VCCIO_1 AK11, VCCIO_2 AK14, VCCIO_3 AK24, VCCIO_4 AJ23, VCCIO_5 M8, VCCIO_6 P8, VCCIO_7 T8, VCCIO_8 U8, VCCIO_9 W8

VCCST_V5 V5, VCCST_V6 V6, VCCPLL V4

+V1.0_SB_VCCST_VCCPLL
+V1.0_SB_VCCFUSEPRG

0.25(A)@+V1.0_VCCST_VCCPLL
0.12(A)@+V1.0_VCCST
0.13(A)@+V1.0_VCCPLL

C7202 22uF 20%_6.3V 0603
C7203 1uF 10%_6.3V 0402

Place caps at TOP socket edge

2.8(A)@+V1.2_VDDQ

+V1.2_DDR

Place caps in socket edge TOP

C7179 22uF 20%_6.3V 0603
C7180 22uF 20%_6.3V 0603
C7172 22uF 20%_6.3V 0603
C7181 22uF 20%_6.3V 0603

VDDQ_AT18 AT18, VDDQ_AT21 AT21, VDDQ_AU13 AU13, VDDQ_AU15 AU15, VDDQ_AU15 AU19, VDDQ_AU19 AU23, VDDQ_AU23 AV11, VDDQ_AV11 AV17, VDDQ_AV17 AV21, VDDQ_AV21 AW10, VDDQ_AW10 AW14, VDDQ_AW14 AW25, VDDQ_AW25 AY12, VDDQ_AY12 AY16, VDDQ_AY16 AY18, VDDQ_AY18 AY23, VDDQ_AY23

0.26(A)@VCCPLL_OC

+V1.2_DDR

VCCPLL_OC AJ9

R7782 0402 0 5%_1/16W

VccPLL_OC power rail is directly tied to VDDQ VR.

Place caps in socket cavity BOTTOM

Place caps in socket cavity BOTTOM/TOP

+V1.0_OPC

2.5(A)@+V1.0_OPC

VCCOPC_AJ30 AJ30, VCCOPC_AJ27 AJ27, VCCOPC_AJ28 AJ28, VCCOPC_AJ29 AJ29, VCCOPC_AK27 AK27

+V1.0_EOPIO

2.8(A)@+V1.0_EOPIO

0.05(A)@+V1.8_SB_G_OPC

VCCEOPIO_1 AJ25, VCCEOPIO_2 AJ26

+V1.8_SB_G_OPC

VCC_OPC_1P8_AB37 AB37, VCC_OPC_1P8_AB38 AB38

VCCSA_SENSE AD5, VCCIO_SENSE AF4, VSS_SAIO_SENSE AE4

+V1.05_SA_VCC_SENSE [12]
+V0.95_VCCIO_SENSE [18]
+V1.05_SA_VSS_SENSE [12,18]

VCCOPC_SENSE AK21, VCCEOPIO_SENSE AJ24, VSSOPC_EOPIO_SENSE AK22

TP_VCCOPC_SENSE
TP_VCCEOPIO_SENSE
TP_VSS_OPC_EOPIO_SENSE

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+V1.0_SB_VCCST_VCCPLL — R7789 0 0603 5%_1/10W — +V1.0_SB_VCCFUSEPRG

+V1.05_SA

C7530 47uF 20%_6.3V 0805
C7529 47uF 20%_6.3V 0805
C7525 47uF 20%_6.3V 0805
C7526 47uF 20%_6.3V 0805
C7527 47uF 20%_6.3V 0805
C7528 47uF 20%_6.3V 0805

close to CPU socket

ADVANTECH

Title	23_CPU VCORE/VCCSA POWER		
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0.55(V)~1.5(V)@+VCCGT

116(A)@+VCCGT

0.55(V)~1.5(V)@+VCCGTX

14(A)@+VCCGTX

+VCCGT

+VCCGTX

Place caps on TOP side socket cavity

C7217 22uF 20%_6.3V 0603 GND
C7218 22uF 20%_6.3V 0603 GND
C7219 22uF 20%_6.3V 0603 GND
C7220 22uF 20%_6.3V 0603 GND
C7221 22uF 20%_6.3V 0603 GND
C7222 22uF 20%_6.3V 0603 GND

Place cap in socket edge TOP

C8701 22uF 20%_6.3V 0603 GND
C8702 22uF 20%_6.3V 0603 GND
C8699 22uF 20%_6.3V 0603 GND
C8700 22uF 20%_6.3V 0603 GND
C7223 22uF 20%_6.3V 0603 GND
C7224 22uF 20%_6.3V 0603 GND
C7216 22uF 20%_6.3V 0603 GND

Place caps on Backside under socket cavity

C7225 22uF 20%_6.3V 0603 GND
C7226 22uF 20%_6.3V 0603 GND
C7227 22uF 20%_6.3V 0603 GND
C7228 22uF 20%_6.3V 0603 GND
C7229 22uF 20%_6.3V 0603 GND
C7230 22uF 20%_6.3V 0603 GND
C7231 22uF 20%_6.3V 0603 GND

CPU1H

LGA_1151
<Characteristic>

AA34	VCCGT_1	VCCGTX_F35	F35
AA35	VCCGT_2	VCCGTX_G34	G34
AA36	VCCGT_3	VCCGTX_G35	G35
AA37	VCCGT_4	VCCGTX_H33	H33
AA38	VCCGT_5	VCCGTX_H34	H34
AB33	VCCGT_6	VCCGTX_J33	J33
AB34	VCCGT_7	VCCGTX_J35	J35
G36	VCCGT_8	VCCGTX_K32	K32
G37	VCCGT_9	VCCGTX_K34	K34
G38	VCCGT_10	VCCGTX_L31	L31
G39	VCCGT_11	VCCGTX_L33	L33
G40	VCCGT_12	VCCGTX_M32	M32
H36	VCCGT_13		
H38	VCCGT_14		
H40	VCCGT_15		
J36	VCCGT_16		
J37	VCCGT_17		
J38	VCCGT_18		
J39	VCCGT_19		
J40	VCCGT_20		
K36	VCCGT_21		
K38	VCCGT_22		
K40	VCCGT_23		
L34	VCCGT_24		
L35	VCCGT_25		
L36	VCCGT_26		
L37	VCCGT_27		
L38	VCCGT_28		
L39	VCCGT_29		
L40	VCCGT_30		
M33	VCCGT_31		
M34	VCCGT_32		
M36	VCCGT_33		
M38	VCCGT_34		
M40	VCCGT_35		
N34	VCCGT_36		
N35	VCCGT_37		
N36	VCCGT_38		
N37	VCCGT_39		
N38	VCCGT_40		
N39	VCCGT_41		
N40	VCCGT_42		
P33	VCCGT_43		
P34	VCCGT_44		
P36	VCCGT_45		
P38	VCCGT_46		
P40	VCCGT_47		
R34	VCCGT_48		
R35	VCCGT_49		
R36	VCCGT_50		
R37	VCCGT_51		
R38	VCCGT_52		
R39	VCCGT_53		
R40	VCCGT_54		
T33	VCCGT_55		
T34	VCCGT_56		
T36	VCCGT_57		
T38	VCCGT_58		
T40	VCCGT_59		
U34	VCCGT_60		
U35	VCCGT_61		
U36	VCCGT_62		
U37	VCCGT_63		
U38	VCCGT_64		
U39	VCCGT_65		
U40	VCCGT_66		
V33	VCCGT_67		
V34	VCCGT_68		
V36	VCCGT_69		
V38	VCCGT_70		
V40	VCCGT_71		
W34	VCCGT_72		
W35	VCCGT_73		
W36	VCCGT_74		
W37	VCCGT_75		
W38	VCCGT_76	VCCGT_SENSE	F39
Y33	VCCGT_77	VSSGT_SENSE	F38
Y34	VCCGT_78		
Y36	VCCGT_79	VCCGTX_SENSE	F37
Y38	VCCGT_80	VSSGTX_SENSE	F36

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F39 +VCCGT_VCC_SENSE [12]
F38 +VCCGT_VSS_SENSE [12]
F37 TP_+VCCGTX_VCC_SENSE
F36 TP_+VCCGTX_VSS_SENSE

CPU1J

LGA_1151
<Characteristic>

TP26	TP_CPU_J8	J8	RSVD_TP_J8
TP27	TP_CPU_J7	J7	RSVD_TP_J7
TP29	TP_CPU_L8	L8	RSVD_TP_L8
TP30	TP_CPU_K8	K8	RSVD_TP_K8
TP31	TP_CPU_AV1	AV1	RSVD_TP_AV1
TP32	TP_CPU_AW2	AW2	RSVD_TP_AW2
		H8	VSS_H8
TP38	TP_CPU_K10	K10	RSVD_K10
TP39	TP_CPU_L10	L10	RSVD_L10
TP40	TP_CPU_J17	J17	RSVD_J17
TP41	TP_CPU_B39	B39	RSVD_B39
TP42	TP_CPU_J19	J19	RSVD_J19
TP44	TP_CPU_C40	C40	RSVD_C40
		G8	VSS_G8
		AY3	VSS_AY3
[33] PCH_2_CPU_TRIGGER	CPU_2_PCH_TRIGGER_R	D1	PROC_TRIGIN
		B3	PROC_TRIGOUT
TP49	TP_CPU_L12_R1_P_R	L12	RSVD_L12
TP50	TP_CPU_K12_R1_N_R	K12	RSVD_K12

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GND

RSVD_TP_H11	H11	TP_CPU_H11	TP33
RSVD_TP_H12	H12	TP_CPU_H12	TP28
RSVD_TP_AW38	AW38	TP_CPU_AW38	TP34
RSVD_TP_AV39	AV39	TP_CPU_AV39	TP35
RSVD_AU39	AU39	TP_CPU_AU39	TP36
RSVD_AU40	AU40	TP_CPU_AU40	TP37
VSS_AT15	AT15		
VSS_AR23	AR23		
VSS_AR22	AR22		
RSVD_J15	J15	TP_RSVD_CPU_J15	TP43
RSVD_J14	J14	TP_RSVD_CPU_J14	TP45
RSVD_AU9	AU9	TP_RSVD_CPU_AU9	TP46
RSVD_AU10	AU10	TP_RSVD_CPU_AU10	TP47
RSVD_J13	J13	TP_RSVD_CPU_J13	TP48
RSVD_K13	K13	CPU_LGC_SPARE1	
RSVD_J11	J11	LGC_SPARE2	
RSVD_D15	D15	TP_CPU_RSVD_D15	TP51
RSVD_K11	K11	TP_CPU_RSVD_K11	TP52

GND

LGC_SPARE2 — R7795 0402 NL/0 5%_1/16W — DRAMRST#_CPU [26,27,30]

CPU_2_PCH_TRIGGER_R — R7796 0402 20 1%_1/16W — CPU_2_PCH_TRIGGER [33]

[17,18,35] +V1.2_DDR_PG — R7797 0402 NL/1.2K 1%_1/16W — CPU_LGC_SPARE1

R7798 NL/560 1%_1/16W 0402 GND

ADVANTECH

Title	24_CPU VCCGT/VCCGTX POWER	
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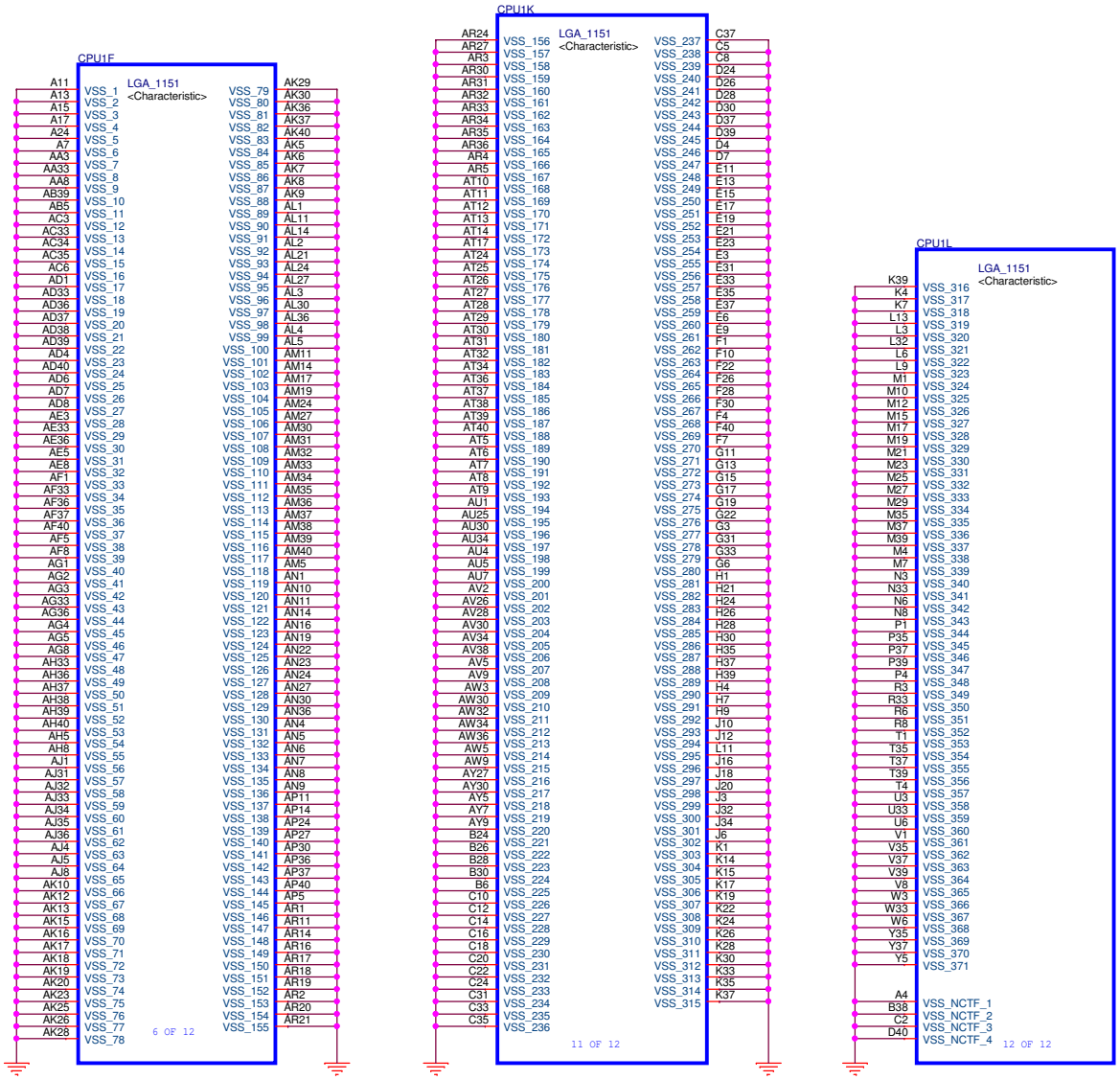
CPU GND



ADVANTECH

Title	25_CPU GND	
Size	Document Number PCE-2129(2029)	Rev A101-2
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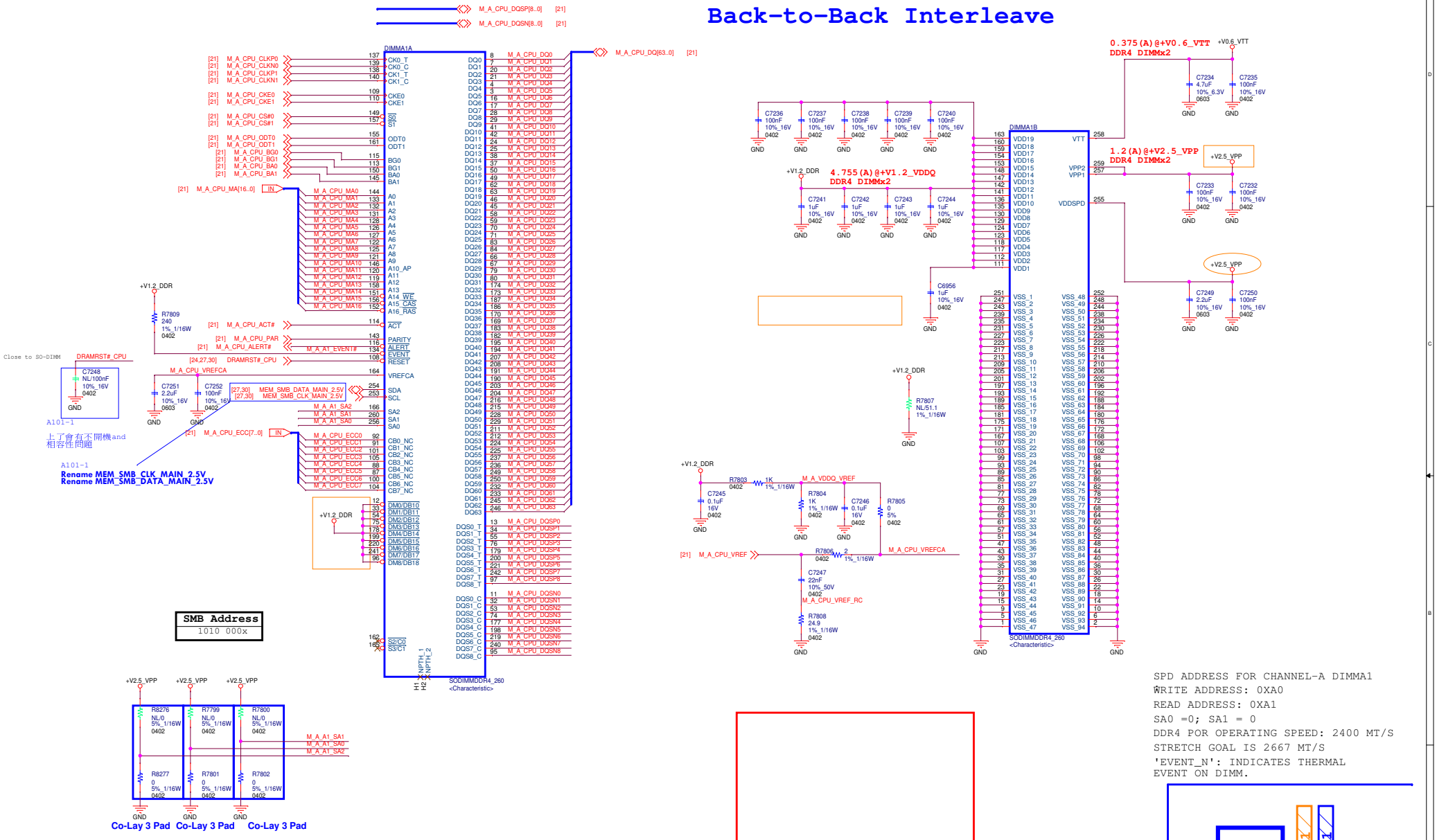
DDR4 SKT [CH-A1] / DIP TYPE

Attend : 1651002910-01

Back-to-Back Interleave



Title	26_DDR4 SODIMM A1		
Size	Document Number	PCE-2129(2029)	Rev A1-2
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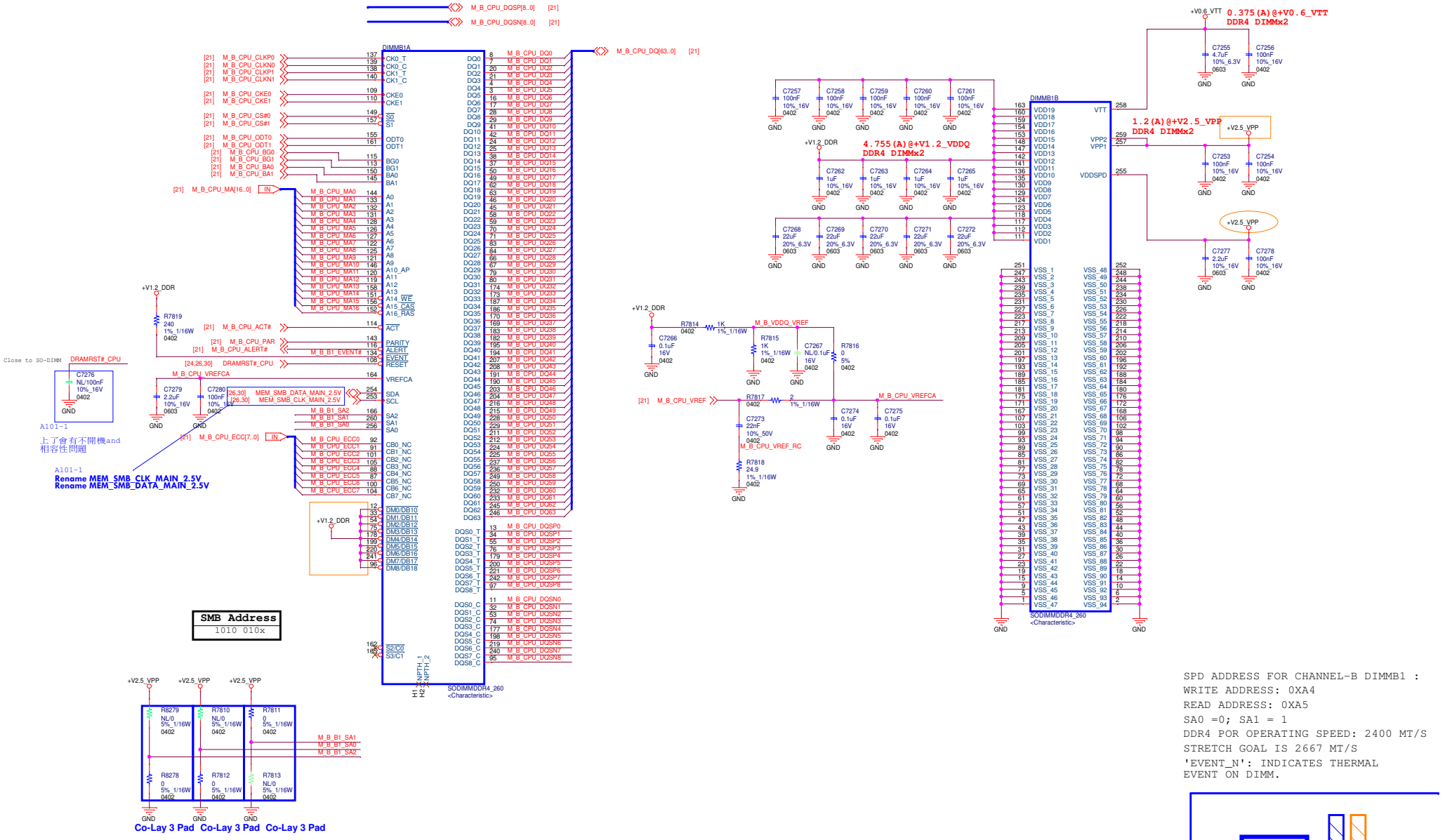
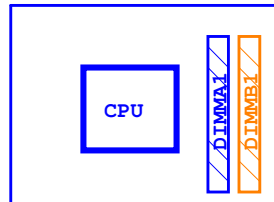
DDR4 SKT [CH-B1] / DIP TYPE

Attend : 1651002910-01



SPD ADDRESS FOR CHANNEL-B DIMMB1 :
WRITE ADDRESS: 0XA4
READ ADDRESS: 0XA5
SA0 =0; SA1 = 1
DDR4 POR OPERATING SPEED: 2400 MT/S
STRETCH GOAL IS 2667 MT/S
'EVENT_N': INDICATES THERMAL EVENT ON DIMM.



ADVANTECH

Title	27_DDR4 SODIMM B1	
Size	Document Number PCE-2129(2029)	Rev A1-2
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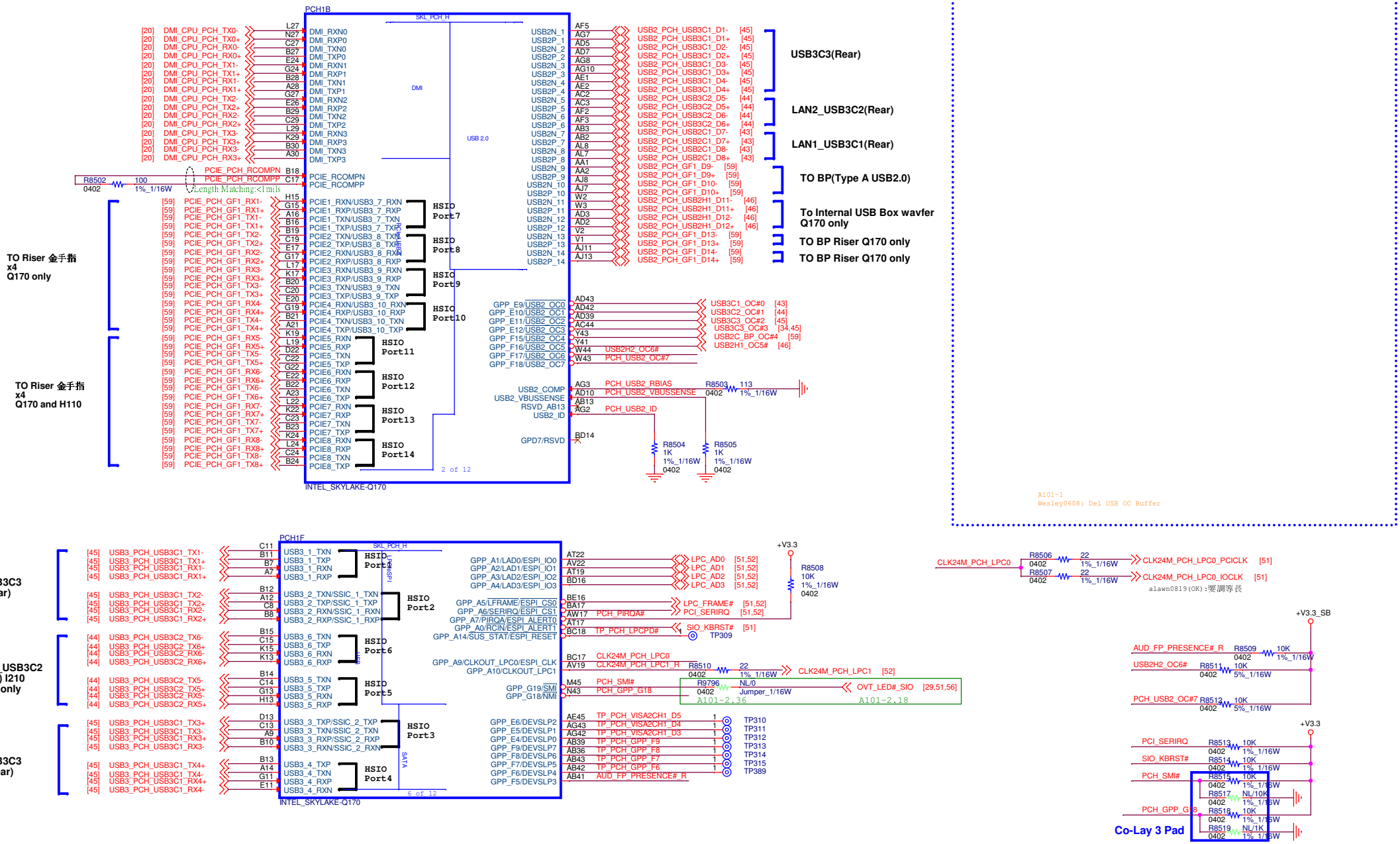
PCH DMI/PCIE/USB/LPC



Title	28_PCH DMI/PCIE/USB/LPC
Size	Document Number: PCE-2129(2029)
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PCH PCIE/SATA/DDC

PCH1C
SKL_PCH_H
INTEL_SKYLAKE-Q170
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HSIO Port15 → PCIE9_RXN/SATA0A_RXN, PCIE9_RXP/SATA0A_RXP, PCIE9_TXN/SATA0A_TXN, PCIE9_TXP/SATA0A_TXP → LAN2 (I210)
HSIO Port16 → PCIE10_RXN/SATA1A_RXN, PCIE10_RXP/SATA1A_RXP, PCIE10_TXN/SATA1A_TXN, PCIE10_TXP/SATA1A_TXP → x1 TO BP
HSIO Port21 → PCIE15_RXN/SATA2_RXN, PCIE15_RXP/SATA2_RXP, PCIE15_TXN/SATA2_TXN, PCIE15_TXP/SATA2_TXP → SATA Conn2
HSIO Port22 → PCIE16_RXN/SATA3_RXN, PCIE16_RXP/SATA3_RXP, PCIE16_TXN/SATA3_TXN, PCIE16_TXP/SATA3_TXP
HSIO Port23 → PCIE17_RXN/SATA4_RXN, PCIE17_RXP/SATA4_RXP, PCIE17_TXN/SATA4_TXN, PCIE17_TXP/SATA4_TXP
HSIO Port24 → PCIE18_RXN/SATA5_RXN, PCIE18_RXP/SATA5_RXP, PCIE18_TXN/SATA5_TXN, PCIE18_TXP/SATA5_TXP
HSIO Port17 → PCIE11_TXP, PCIE11_TXN, PCIE11_RXP, PCIE11_RXN → x1 TO BP Q170 only
HSIO Port20 → PCIE14_TXN/SATA1B_TXN, PCIE14_TXP/SATA1B_TXP, PCIE14_RXN/SATA1B_RXN, PCIE14_RXP/SATA1B_RXP → MINIPCIE/mSATA
HSIO Port19 → PCIE13_TXN/SATA0B_TXN, PCIE13_TXP/SATA0B_TXP, PCIE13_RXN/SATA0B_RXN, PCIE13_RXP/SATA0B_RXP → SATA Conn1
HSIO Port18 → PCIE12_TXP, PCIE12_TXN, PCIE12_RXP, PCIE12_RXN → LAN1 (PHY,I219V)
HSIO Port26 → PCIE20_TXP/SATA7_TXP, PCIE20_TXN/SATA7_TXN, PCIE20_RXP/SATA7_RXP, PCIE20_RXN/SATA7_RXN
HSIO Port25 → PCIE19_TXP/SATA6_TXP, PCIE19_TXN/SATA6_TXN, PCIE19_RXP/SATA6_RXP, PCIE19_RXN/SATA6_RXN

CLINK: CL_CLK, CL_DATA, CL_RST
FAN: GPP_G8/FAN_PWM_0, GPP_G9/FAN_PWM_1, GPP_G10/FAN_PWM_2, GPP_G11/FAN_PWM_3, GPP_G0/FAN_TACH_0, GPP_G1/FAN_TACH_1, GPP_G2/FAN_TACH_2, GPP_G3/FAN_TACH_3, GPP_G4/FAN_TACH_4, GPP_G5/FAN_TACH_5, GPP_G6/FAN_TACH_6, GPP_G7/FAN_TACH_7
PCIDATA

PCB_ID0, PCB_ID1, PCB_ID2, TP_PCH_GPP_G11 (TP316, GPIO for BIOS Control)
COM1_TERM, COM1_MODE0, COM1_MODE1, VGA1_HDMI1_OC#, DP1_OC#, PCH_SV_DETECT, OVT_LED#_SIO (TP390)
PCH_CONFIG_JUMPER, PCH_RSVD, PCH_GP39_GFX_CRB_DETECT, PCH_SV_ADVANCE_GP48
GPP_F10/SCLOCK, GPP_F11/SLOAD, GPP_F13/SDATAOUT0, GPP_F12/SDATAOUT1
GPP_E8/SATALED → SATA_PCH_LED# [56,60]
GPP_E0/SATAXPCIE0/SATAGP0 … GPP_F4/SATAXPCIE7/SATAGP7 → SATAXPCIE0 … SATAXPCIE5, PCH_GPP_F3, PCH_GPP_F4
GPP_F21/EDP_BKLTCTL, GPP_F20/EDP_BKLTEN, GPP_F19/EDP_VDDEN → COM2_TERM, COM2_MODE0, COM2_MODE1
THERMTRIP → PCH_THERMTRIP#_R; PECI → PCH_PECI; PM_SYNC → PCH_PM_SYNC_R; PLTRST_PROC → PCH_PLTRST_CPU#; PM_DOWN → CPU_PM_DOWN

PCH1E
SKL_PCH_H
INTEL_SKYLAKE-Q170
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DDPB_HPD, DDPC_HPD, DDPE_VGA_HPD → GPP_I0/DDPB_HPD0, GPP_I1/DDPC_HPD1, GPP_I2/DDPD_HPD2, GPP_I3/DDPE_HPD3
EDP_HPD → GPP_I4/EDP_HPD
GPP_I7/DDPC_CTRLCLK … GPP_I10/DDPD_CTRLDATA → DDPC_CLK, DDPC_DATA, DDPB_CLK, DDPB_DATA
GPP_F14 … GPP_H23 → H_SKTOCC#_R, PCH_VCORE_VBOOST_CTRL, GPP_F22, PCH_IVCAM_DFU, TP_PCH_PEGSLOT1_PWREN1 (TP317), PCH_SPI_TPM_PIRQ, PCH_TEST_SETUP_MENU, PCH_AMT_LED

H_SKTOCC#_R R8522 0 Jumper_1/16W 0402 → H_SKTOCC# [22]
PCH_VCORE_VBOOST_CTRL, EDP_HPD: R8523 10K 1% 1/16W 0402; R8524 100K 1% 1/16W 0402

+V3.3
DDPB_CLK R8525 2.2K 1% 1/16W 0402
DDPB_DATA R8526 2.2K 1% 1/16W 0402
DDPC_CLK R8527 2.2K 1% 1/16W 0402
DDPC_DATA R8528 2.2K 1% 1/16W 0402
GPP_F22 R8529 10K 1% 1/16W 0402
DP1_OC# R9156 1K 1% 1/16W 0402
PCH_SPI_TPM_PIRQ R8530 8.2K 5% 1/16W 0402
PCH_AMT_LED R8531 10K 1% 1/16W 0402
→ +V3.3_SB

DDPB_CTRLDATA
This signal has a weak internal pull-down.
LOW:Port B is not detected. (Default)
HIGH:Port B is detected.

DDPC_CTRLDATA
This signal has a weak internal pull-down.
LOW:Port B is not detected. (Default)
HIGH:Port B is detected.

SATA_PCH_SATA1_TX-, SATA_PCH_SATA1_TX+, SATA_PCH_SATA1_RX-, SATA_PCH_SATA1_RX+
PCIE_PCH_LAN1_TX12+, PCIE_PCH_LAN1_TX12-, PCIE_PCH_LAN1_RX12+, PCIE_PCH_LAN1_RX12-
PCIE_PCH_MINI_TX14-, PCIE_PCH_MINI_TX14+, PCIE_PCH_MINI_RX14-, PCIE_PCH_MINI_RX14+
PCIE_PCH_GF1_TX11+, PCIE_PCH_GF1_TX11-, PCIE_PCH_GF1_RX11+, PCIE_PCH_GF1_RX11-
PCIE_PCH_LAN2_RX9-, PCIE_PCH_LAN2_RX9+, PCIE_PCH_LAN2_TX9-, PCIE_PCH_LAN2_TX9+
PCIE_PCH_GF1_RX10-, PCIE_PCH_GF1_RX10+, PCIE_PCH_GF1_TX10-, PCIE_PCH_GF1_TX10+
SATA_PCH_SATA2_RX-, SATA_PCH_SATA2_RX+, SATA_PCH_SATA2_TX-, SATA_PCH_SATA2_TX+

SATAXPCIE0 → R8532 0 Jumper_1/16W NEW PU 3.3 → MINIPCIE2_MSATA [48]
R9789 NL/0 Jumper_1/16W A101-2.13

Wesley0702: Follow CRB PD 1k

PCH_IVCAM_DFU, PCH_TEST_SETUP_MENU → R8534 10K; R8535 NL/10K; R8536 10K; R8538 NL/0 (all 0402 1%_1/16W) → +V3.3
Co-Lay 3 Pad
(Default)

TEST SETUP MENU	BOARD STYLE
0	TEST SETUP MENU ENABLED
1	DISABLED

alawn0819: 確認PCH_CONFIG_JUMPER的準位(EDS)，為何上件的表格怪怪的
alawn0704: what's this
Wesley0702: 此分壓是Follow CRB setting

RC: R8540 1K 1% 1/16W 0402 → +V3.3
RA: PCH_SPKR [30,34,50,58] R8544 NL/2.2K 0402 1%_1/16W; PCH_GSPI0_MOSI [31,34] R8546 NL/2.2K 0402 1%_1/16W
RB: R8547 10K 1% 1/16W 0402
PCH_CONFIG_JUMPER
STUFF RA FOR LPT-H
STUFF RB FOR SKL PCH H

RECOVER/CONFIGURE	MODE
Stuff RC, Not Stuff RA & RB	NORMAL
Not Stuff RA & RB & RC	CONFIGURE
Not Stuff RA & RB & RC	RECOVERY (Default)

SATA_PCH_LED#, PCH_GPP_F3, PCH_GPP_F4, PCH_PM_SYNC_R: R8539 10K; R8541 NL/10K; R8542 NL/10K; R8543 30 (all 1% 1/16W 0402) → +V3.3
PCH_PM_SYNC [22]

+V1.0_SB_VCCST_VCCPLL
R8545 75 1% 1/16W 0402 Place Close to PCH

alawn0819(OK): PDG suggest 1K, 使用75ohm使PCH_THERMTRIP#較大較不易受到干擾
PCH_THERMTRIP#_R R8548 560 1% 1/16W 0402 → PCH_THERMTRIP# [22]

C7760 NL/470pF 5%_50V; R8537 1K 1%_1/16W 0402 → PCH_PECI [22]

GFX SELECT

	GFX STYLE
0	NORMAL GFX (Default)
1	CUSTOMER GFX

SV ADVANCE

	BOARD STYLE
1	NORMAL MENU (Default)
0	SV ADVANCE MENU

OVT_LED#_SIO: R8549 10K
PCH_SV_DETECT: R8551 NL/10K; R8553 10K
PCH_RSVD: R8555 10K; R8557 NL/0
PCH_GP39_GFX_CRB_DETECT: R8559 NL/10K
PCH_SV_ADVANCE_GP48: R8562 10K; R8565 20K; R8568 NL/0
(all 0402 1%_1/16W) → +V3.3
Co-Lay 3 Pad

alawn0819: 不用時是GPIO, default是in or out
SATAXPCIE0: R8550 10K
SATAXPCIE1: R8552 NL/10K; R9776 NL/10K
SATAXPCIE2: R8554 NL/10K; R8556 NL/10K
SATAXPCIE3: R8558 NL/10K; R8560 NL/10K
SATAXPCIE4: R8563 10K; R8566 NL/10K
SATAXPCIE5: R8569 NL/10K; R8572 NL/10K
(all 0402 1%_1/16W) → +V3.3
Co-Lay 3 Pad

SATA0B / PCIe13
PCIe SATAXPCIE0 pin is '0'
SATA SATAXPCIE0 pin is '1' (default)
SATA1B / PCIe14
PCIe SATAXPCIE1 pin is '0'
SATA SATAXPCIE1 pin is '1' (default)
SATA2 / PCIe15
SATA SATAXPCIE2 pin is '0'
PCIe SATAXPCIE2 pin is '1' (default)
SATA3 / PCIe16
SATA SATAXPCIE3 pin is '0'
PCIe SATAXPCIE3 pin is '1' (default)
SATA4 / PCIe17
SATA SATAXPCIE4 pin is '0'
PCIe SATAXPCIE4 pin is '1' (default)
SATA5 / PCIe18
PCIe SATAXPCIE5 pin is '0'
SATA SATAXPCIE5 pin is '1' (default)

Identify ID	
GPP_G8=PCB_ID0	For Q170 =1 ; H110=0
GPP_G9=PCB_ID1	For DDI2 ; DP=1 ; DVI=0
GPP_G10=PCB_ID2	Reserve

PCB_ID0, PCB_ID1, PCB_ID2: R8561 10K; R8567 10K; R8573 10K; R8564 NL/10K; R8570 NL/10K; R8575 10K
(all 0402 1%_1/16W) → +V3.3_SB
Co-Lay 3 Pad

ADVANTECH

Title	29_PCH PCIE/SATA/DDC
Size	Document Number: PCE-2129(2029) Rev: A101-2
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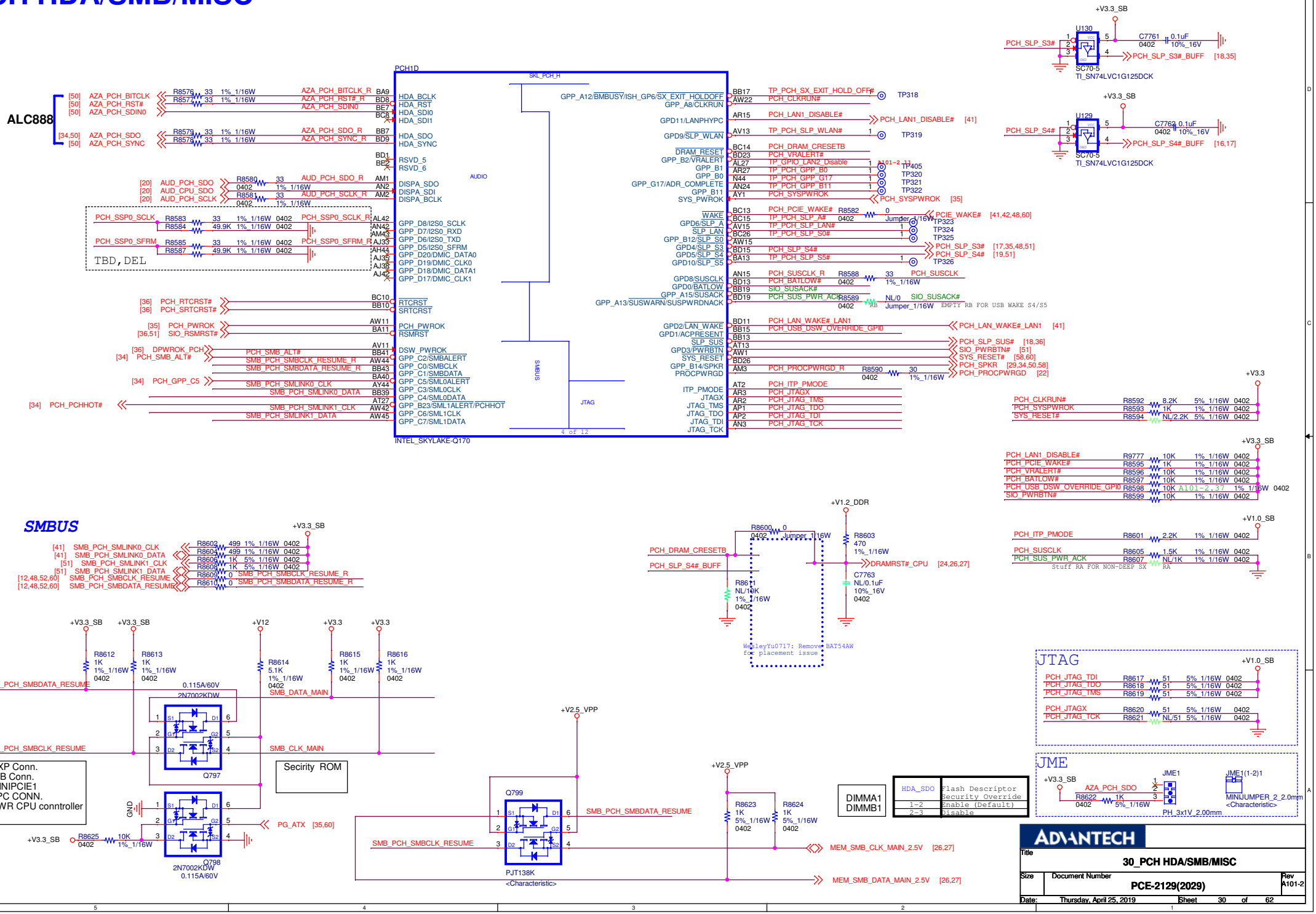
PCH HDA/SMB/MISC



ADVANTECH

Title	30_PCH HDA/SMB/MISC	
Size	Document Number PCE-2129(2029)	Rev A101-2
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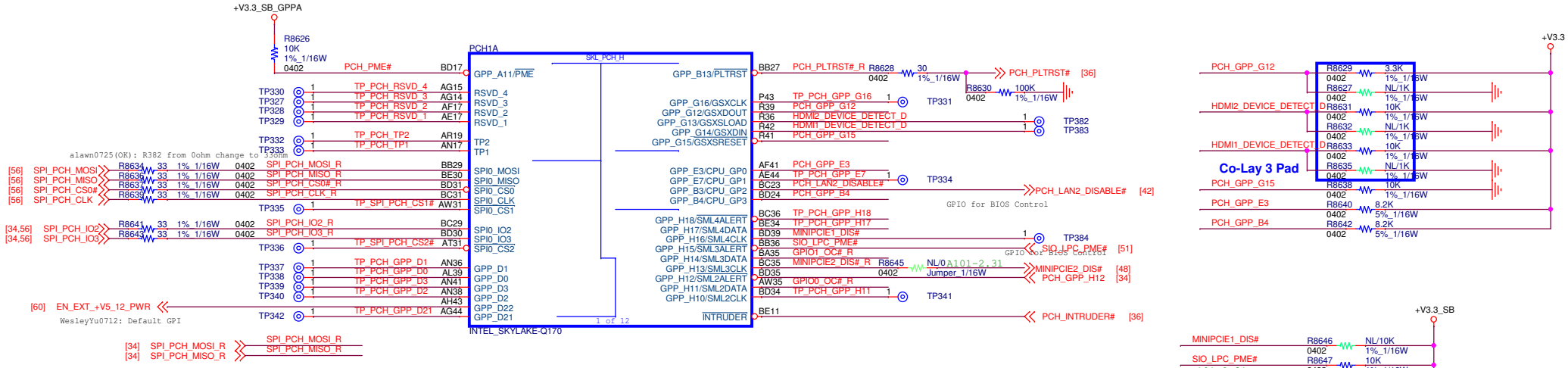
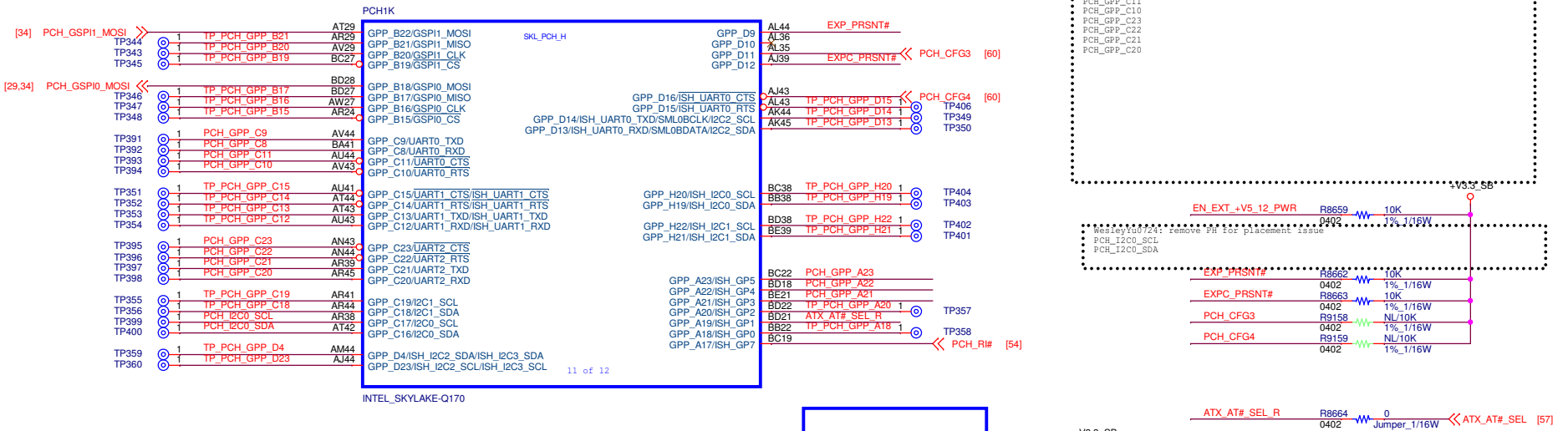
PCH SPI



If UART interface is used, 50 K? pull-up resistors to 3.3V
are required on all UART signals.If the interface is not used,
the signals can be used as GPIO.
If GPIO functionality is also not used, the signals can be left as no- connect.



If I2C interfaces are not used, the signals can be
used as GPIOs instead. If the GPIO functionality is
also not used, the signals can be left as no-connect.

ADVANTECH

Title	31_PCH SPI	
Size	Document Number PCE-2129(2029)	Rev A101-2
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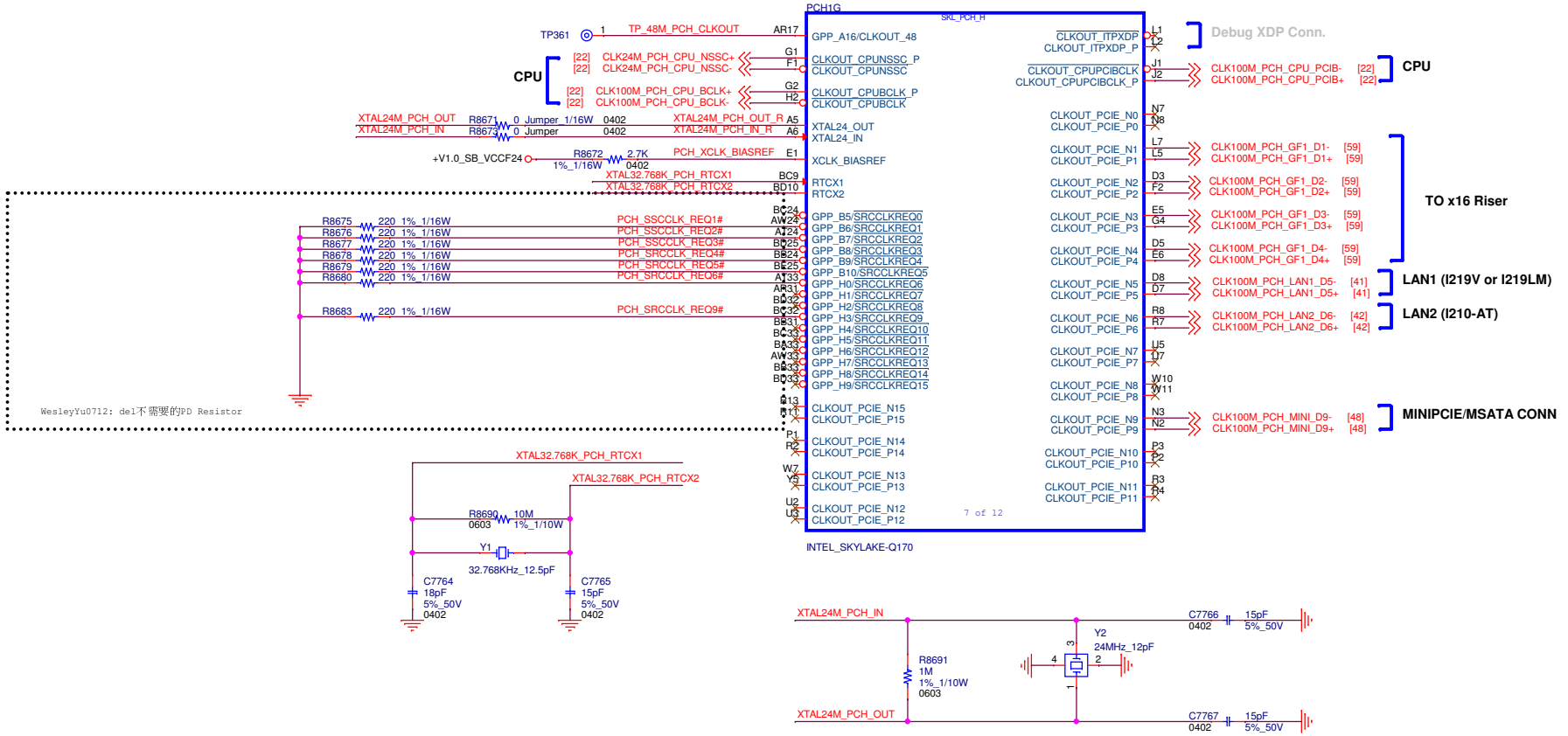
PCH CLOCK



Title	32_PCH CLOCK		
Size	Document Number		Rev
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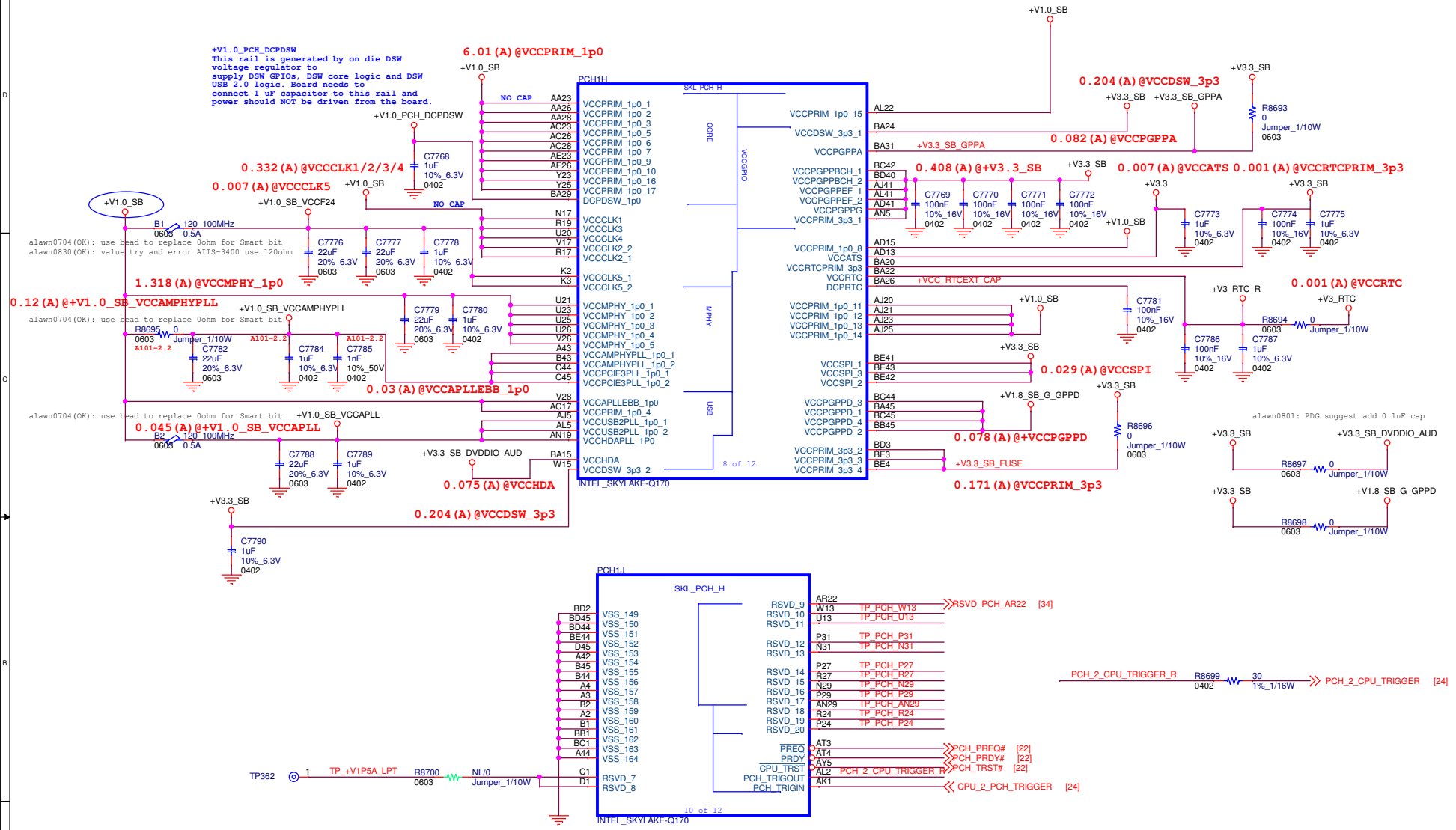
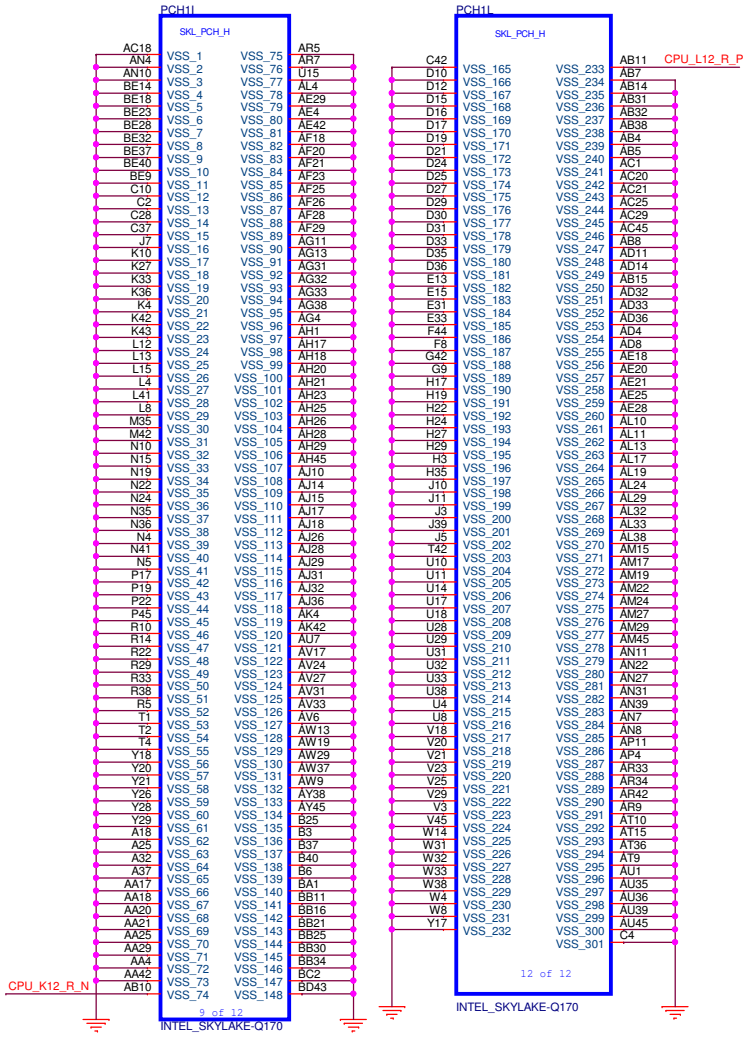
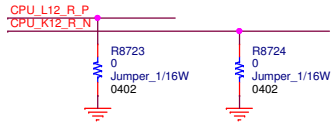
PCH POWER


+V1.0_PCH_DCPDSW
This rail is generated by on die DSW voltage regulator to supply DSW GPIOs, DSW core logic and DSW USB 2.0 logic. Board needs to connect 1 uF capacitor to this rail and power should NOT be driven from the board.
6.01 (A) @VCCPRIM_1p0
0.332 (A) @VCCCLK1/2/3/4
0.007 (A) @VCCCLK5
1.318 (A) @VCCMPHY_1p0
0.12 (A) @+V1.0_SB_VCCAMPHYPLL
0.03 (A) @VCCAPLLEBB_1p0
0.045 (A) @+V1.0_SB_VCCAPLL
0.075 (A) @VCCHDA
0.204 (A) @VCCDSW_3p3
0.204 (A) @VCCDSW_3p3
0.082 (A) @VCCPGPPA
0.408 (A) @+V3.3_SB
0.007 (A) @VCCATS
0.001 (A) @VCCRTCPRIM_3p3
0.001 (A) @VCCRTC
0.029 (A) @VCCSPI
0.078 (A) @+VCCPGPPD
0.171 (A) @VCCPRIM_3p3
PCH1H
SKL_PCH_H
INTEL_SKYLAKE-Q170
8 of 12
PCH1J
10 of 12
alawn0704(OK): use bead to replace 0ohm for Smart bit
alawn0830(OK): value try and error AIIS-3400 use 120ohm
alawn0801: PDG suggest add 0.1uF cap
PCH_2_CPU_TRIGGER_R
TP362
TP_+V1P5A_LPT

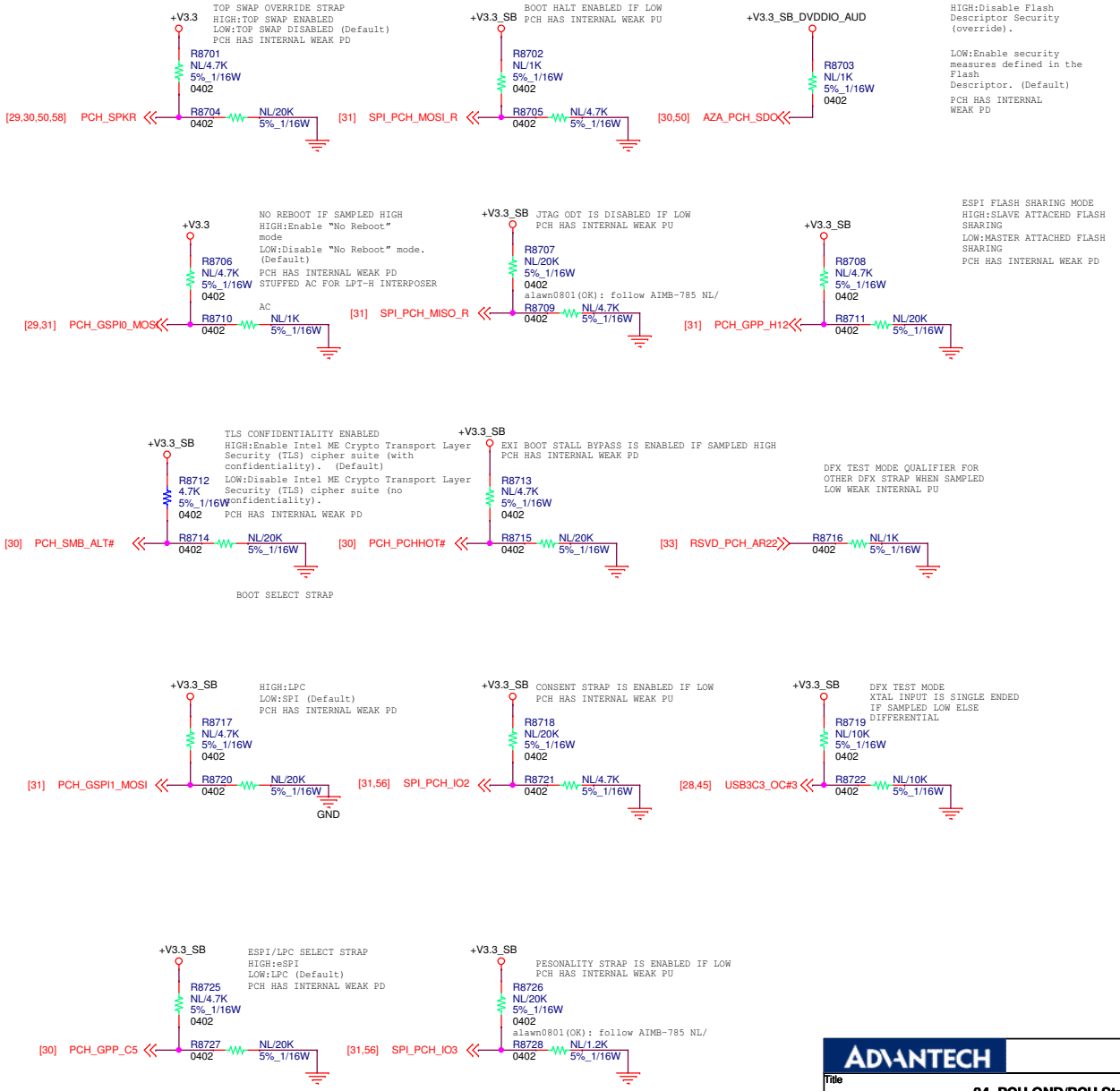
PCH GND/PCH Strap Option





PCH Strap Option

coLayout use 3 pad



ADVANTECH

Title	34_PCH GND/PCH Strap Option	
Size	Document Number PCE-2129(2029)	Rev A101-2
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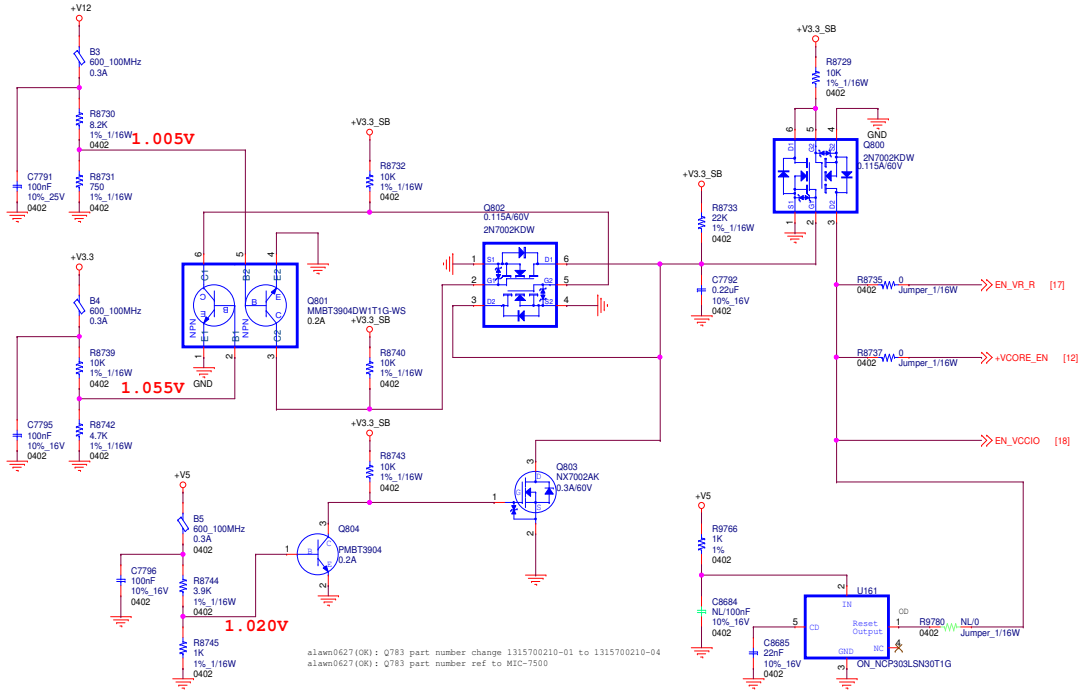
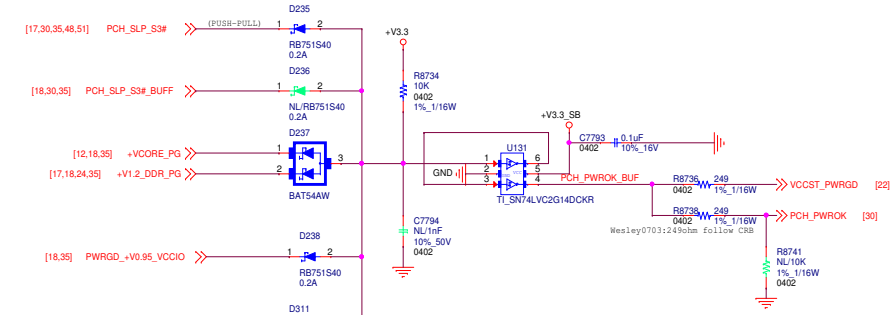
VCCIOEN/VREN/POK/SYSPOK

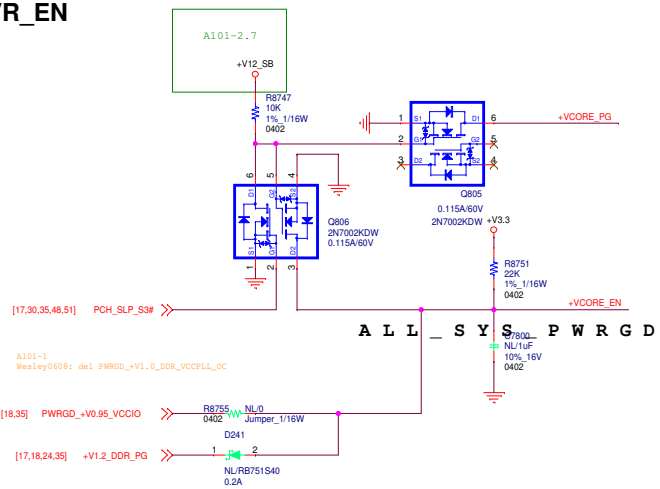
Main Power Ready



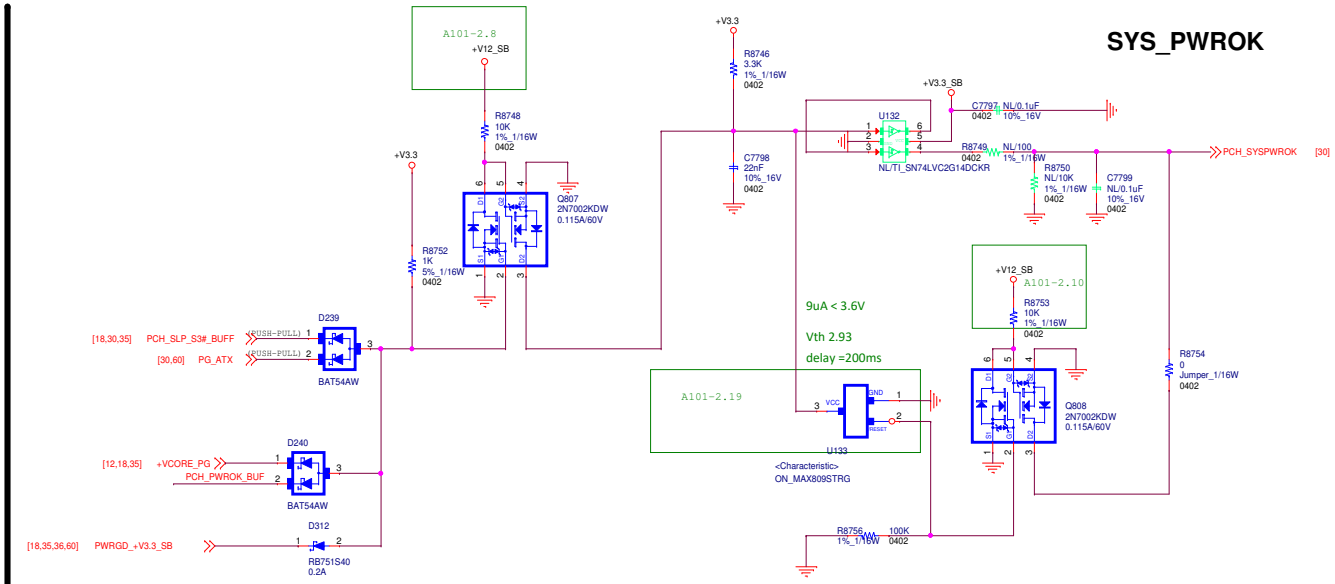
PWROK



VR_EN



SYS_PWROK



ADVANTECH

Title	35_VCCIOEN/VREN/POK/SYSPOK	
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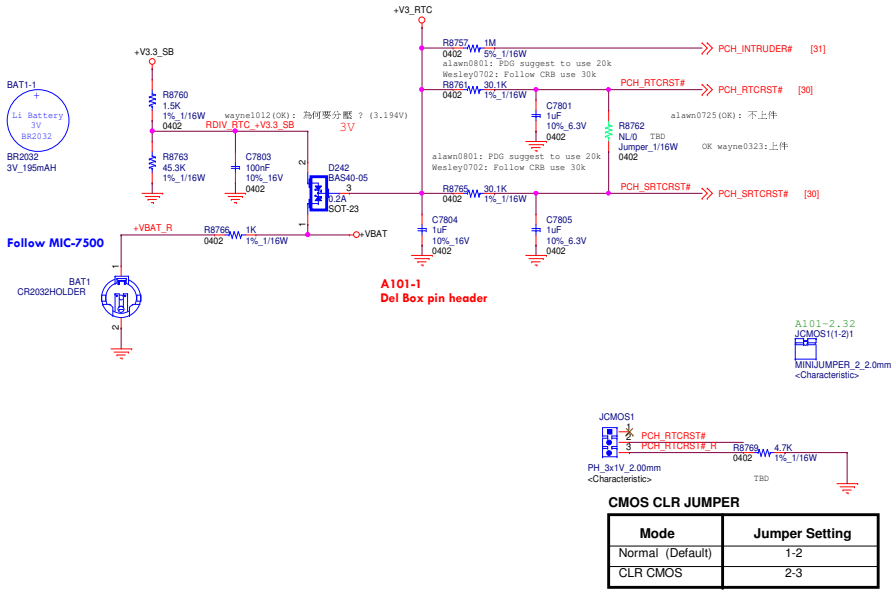
RTCRST#/RSMRST#/PLTRST#

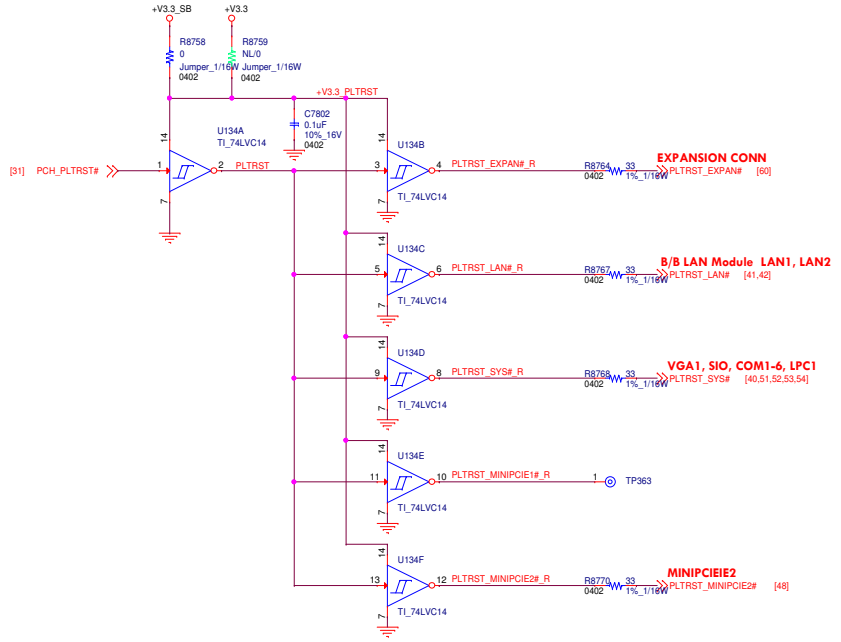
RTCRST#



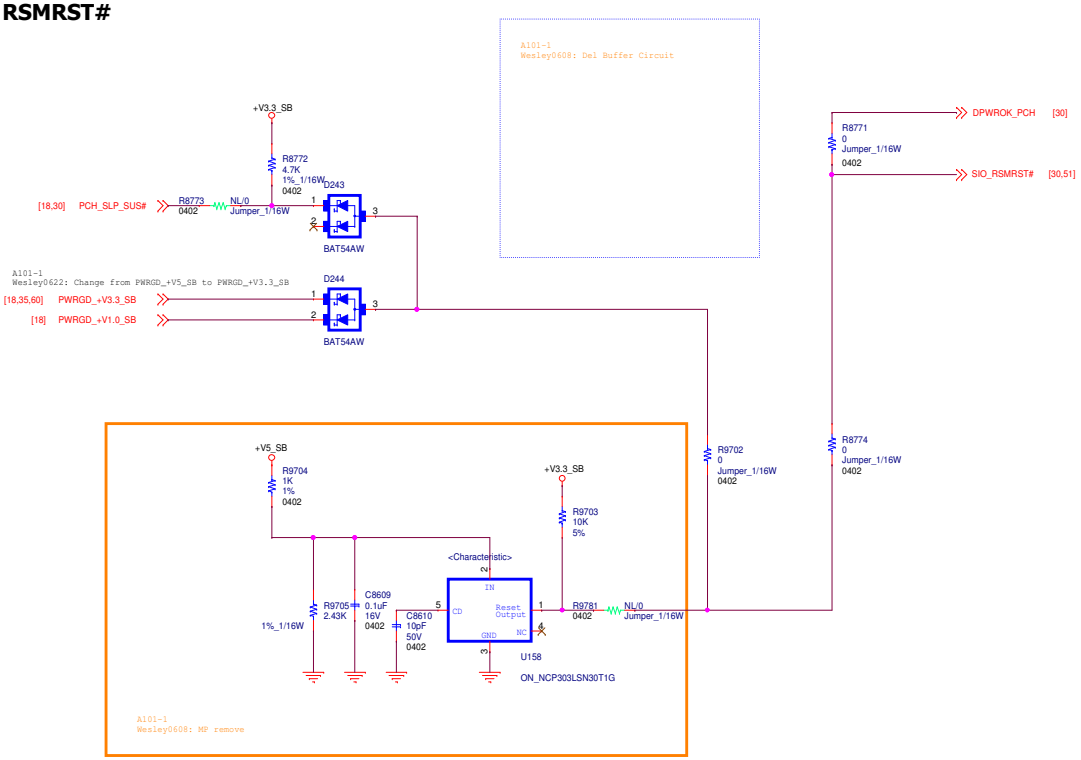
CMOS CLR JUMPER

Mode	Jumper Setting
Normal (Default)	1-2
CLR CMOS	2-3

PLTRST#



RSMRST#



ADVANTECH

Title	36_RTCRST#/RSMRST#/PLTRST#	
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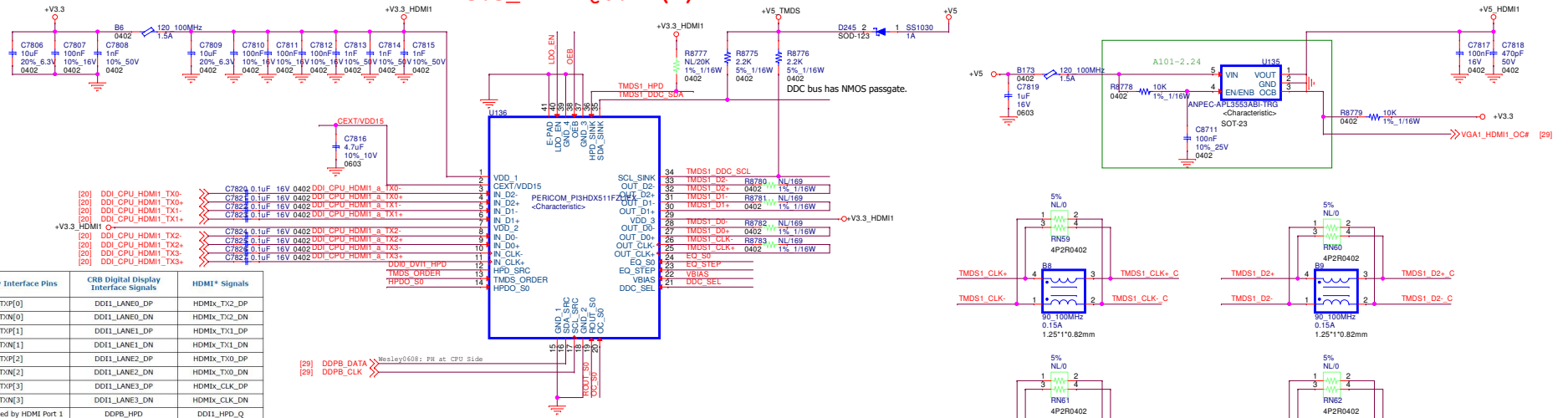
DDI Port C to HDMI

william : 線路參考5580DB

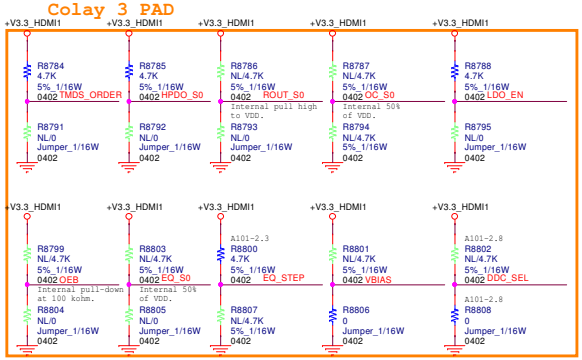
+V5_TMDS@0.055(A)

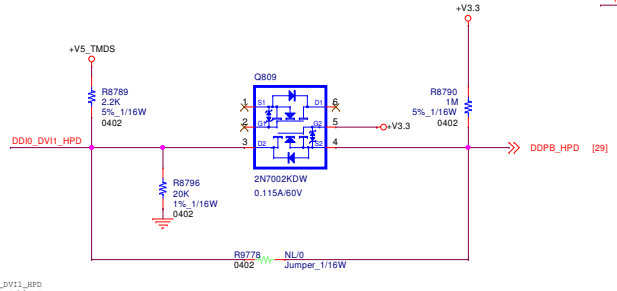
+V3.3_HDMI1@0.12(A)

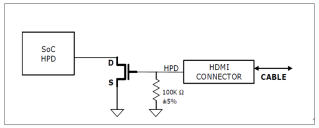


Port	Digital Display Interface Pins	CRB Digital Display Interface Signals	HDMI* Signals
Port 1	DDI1_TXP[0]	DDI1_LANE0_DP	HDMIx_TX2_DP
	DDI1_TXN[0]	DDI1_LANE0_DN	HDMIx_TX2_DN
	DDI1_TXP[1]	DDI1_LANE1_DP	HDMIx_TX1_DP
	DDI1_TXN[1]	DDI1_LANE1_DN	HDMIx_TX1_DN
	DDI1_TXP[2]	DDI1_LANE2_DP	HDMIx_TX0_DP
	DDI1_TXN[2]	DDI1_LANE2_DN	HDMIx_TX0_DN
	DDI1_TXP[3]	DDI1_LANE3_DP	HDMIx_CLK_DP
	DDI1_TXN[3]	DDI1_LANE3_DN	HDMIx_CLK_DN
	Hot plug detect used by HDMI Port 1	DDPB_HPD	DDI1_HPD_Q
	HDMI DDC lines for Port 1	DDPB_CTRLCLK	DDI1_CTRL_CK
		DDPB_CTRLDATA	DDI1_CTRL_DATA

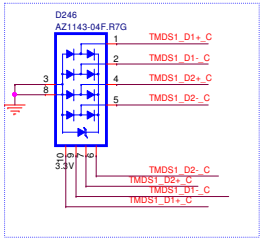
Colay 3 PAD





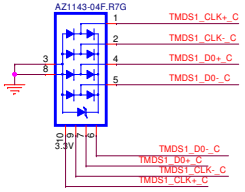


ESD Protection Arrays

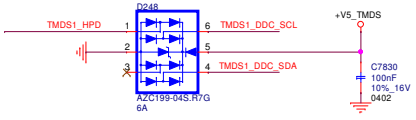


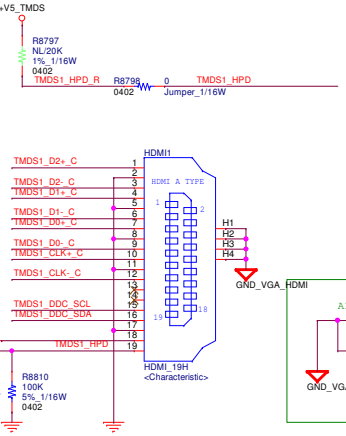
Close to Connector

ESD Protection Arrays



Close to Connector





TMDS Pin Order Configuration Table

TMDS_ORDER	Functional Description	Note
0	CLK/D0/D1/D2 pin order	
1 or *NC*	D2/D1/D0/CLK pin order	Default

DDC mode selection DDC_SEL Configuration Table

DDC_SEL	Functional Description	Note
0	Active DDC Buffer	Default
1 or *NC*	Passive Switch	

LDO Enable Configuration Table

LDO_EN	Functional Description		Note
	Pin 1	Pin 2	
0	3.3V	1.5V	Dual power supply mode 3.3/1.5V
1	3.3V	External capacitor	Recommend 2.2~4.7uF pull down capacitor.Default

Pre-emphasis Truth Table

Output pre-emphasis setting		Functional Description		Notes
ROUT_S0	OC_S0	Single-end Vswing	Pre-emphasis	
0	*0*	500 mV	0 dB	Open drain output.
	NC or VDD/2	500 mV	1.5 dB	Open drain output.
	1	500 mV	2.5 dB	Open drain output
1	*0*	500 mV	0 dB	Double termination
	NC or VDD/2	500 mV	1.5 dB	Double termination.Default
	1	500 mV	2.5 dB	Double termination

TMDS Input Termination Voltage Control VBIAS Truth Table

VBIAS	Functional Description
1, *NC*	HDMI input. VBIAS ties to VDD.
0	DisplayPort input. VBIAS ties to GND. Default

EQ Step Selection Control EQ_STEP Truth Table

EQ_STEP	Functional Description
1, *NC*	2.5, 5, 7.5dB EQ setting with EQ_S0 control pin Default
0	5, 10, 15dB EQ setting with EQ_S0 control pin

Sink side Hot Plug Detect HPD_SINK Truth Table

HPD_SINK	Functional Description
1	Normal mode
0	Disable output signal for power saving mode Default

Source side Hot Plug Detect Output Control HPDO_S0 Truth Table

HPDO_S0	Functional Description
1 or *NC*	Open drain output. Default
0	Inverted Buffer output of HPD_SINK signal

Output Enable Conrol Truth Table

OEB	Functional Description
0	Active Low. Normal mode Default
1	Disable output signal for power saving mode

Output Data Signals EQ_S0 Configuration Truth Table

EQ_S0	Functional Description		Note
	EQ_STEP = *1*	EQ_Step = *0*	
0	2.5 dB	5 dB	TMDS Clock(CLK) channel EQ is always fixed as 3dB without pre-emphasis.
NC , *VDD/2*	5 dB Default	10 dB	
1	7.5 dB	15 dB	

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Title: 39_Display HDMI/Level Shifter

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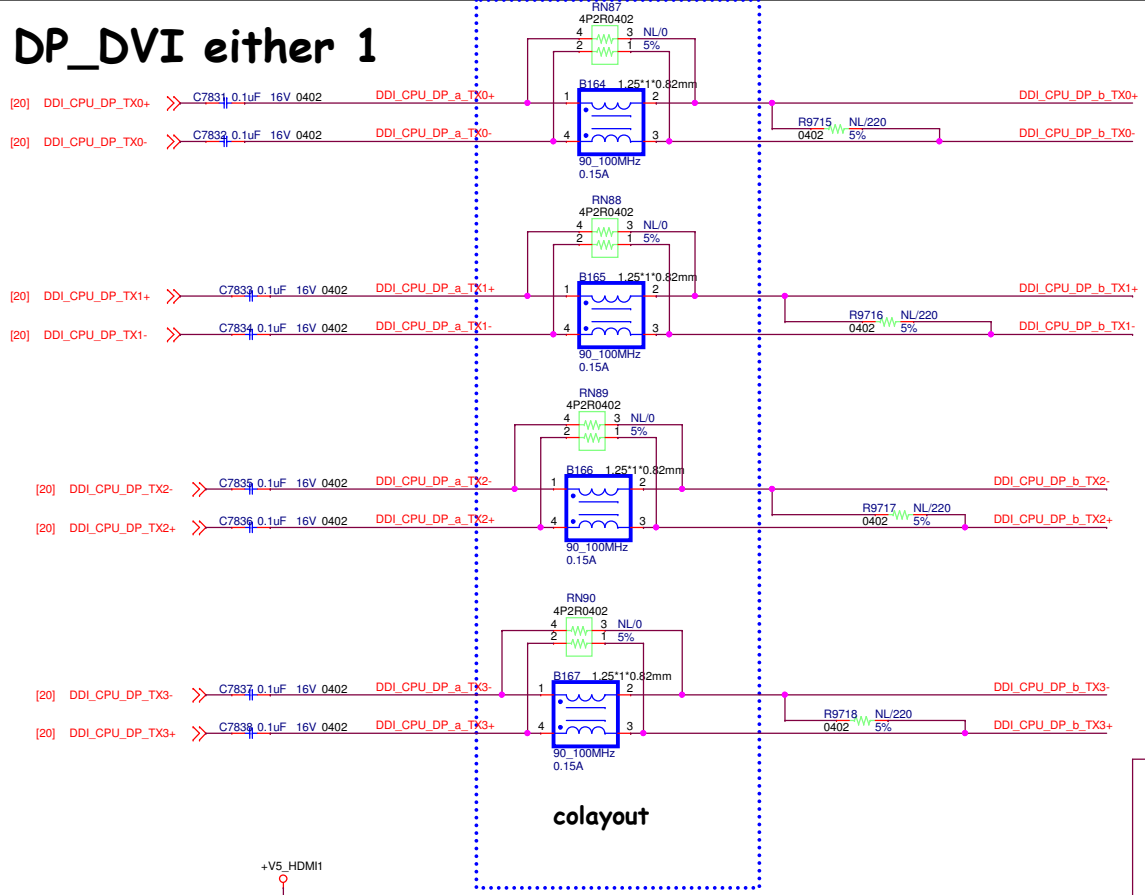
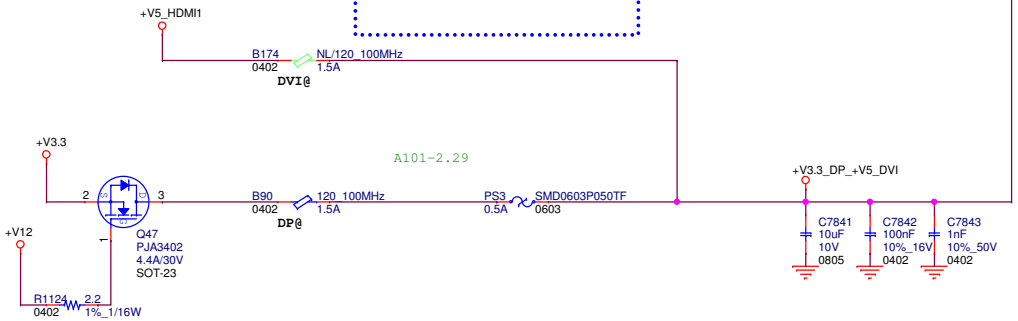
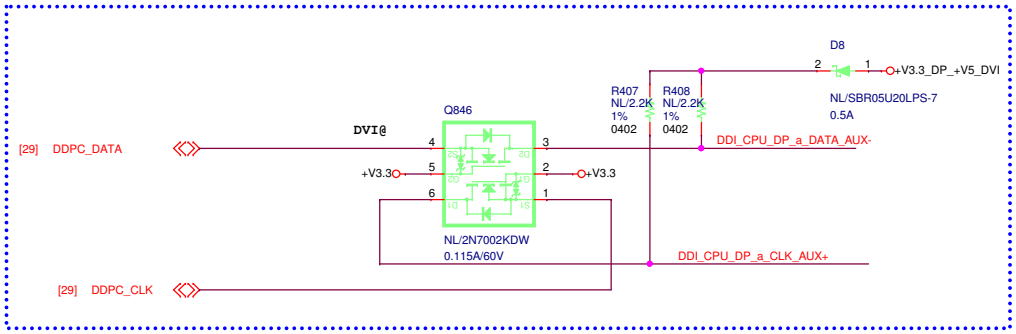
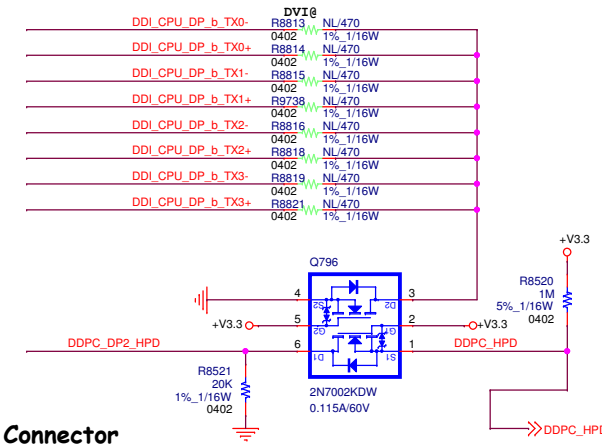
DP_DVI either 1



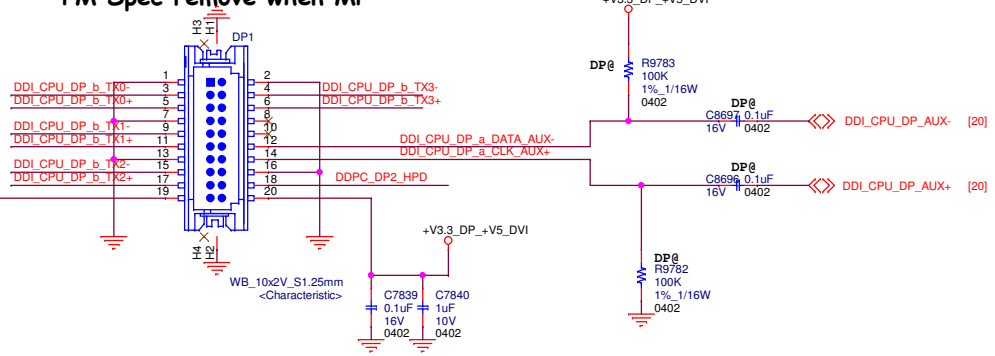
colayout



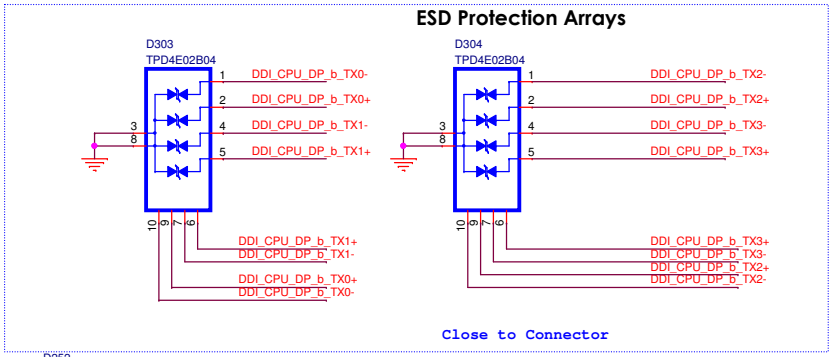


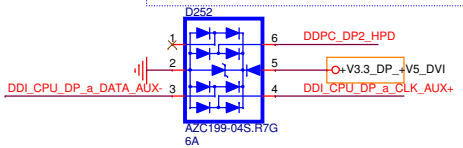


DP Connector
PM Spec remove when MP



ESD Protection Arrays





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Title	Display DP_DVI_PH	
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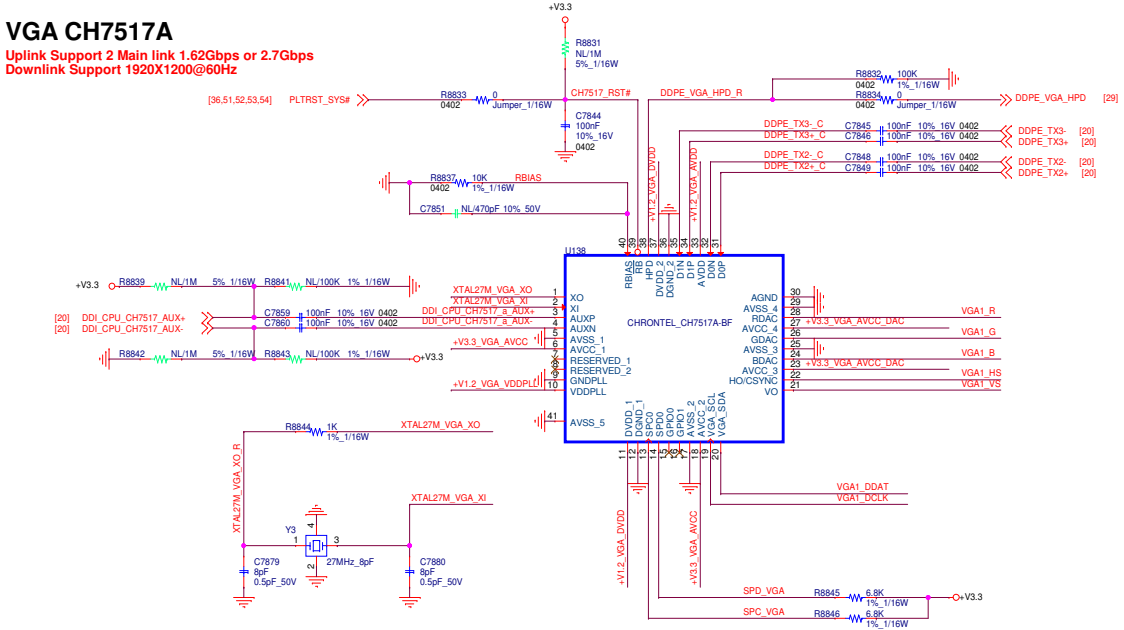
Display VGA1/CH7517

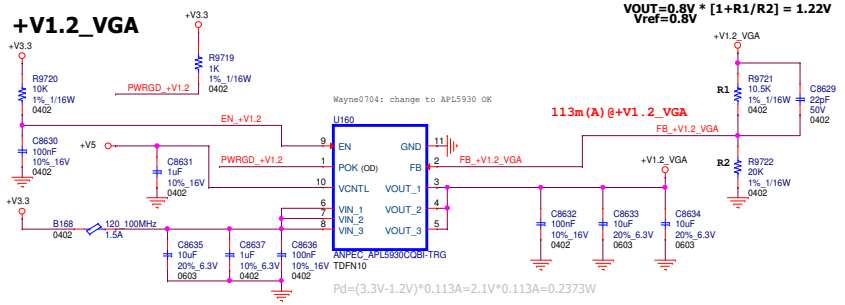
VGA CH7517A

Uplink Support 2 Main link 1.62Gbps or 2.7Gbps
Downlink Support 1920X1200@60Hz

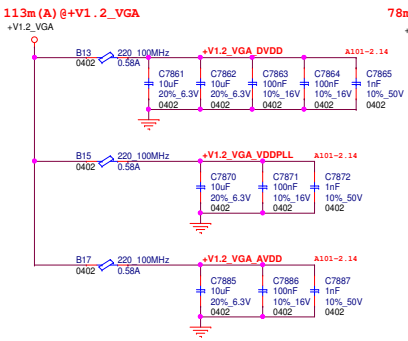


+V1.2_VGA

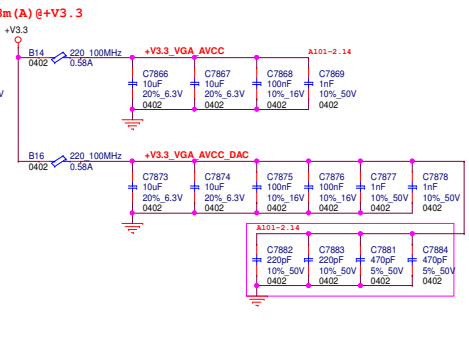
VOUT=0.8V * [1+R1/R2] = 1.22V
Vref=0.8V



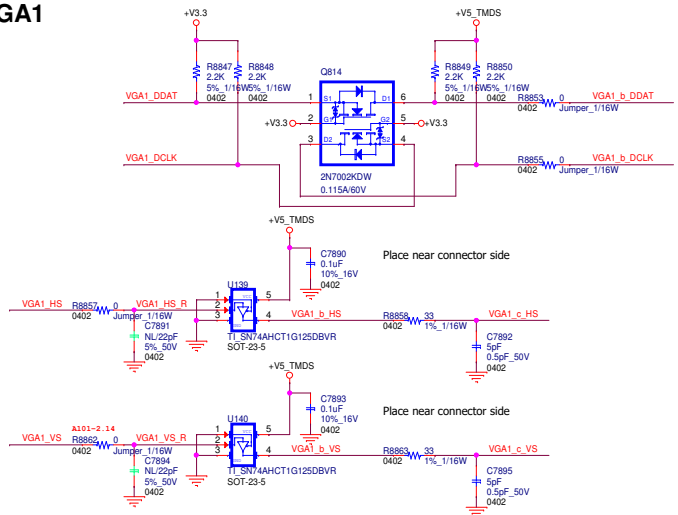
113m(A)@+V1.2_VGA

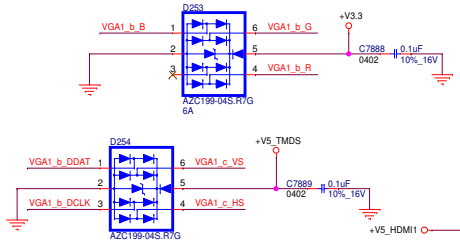


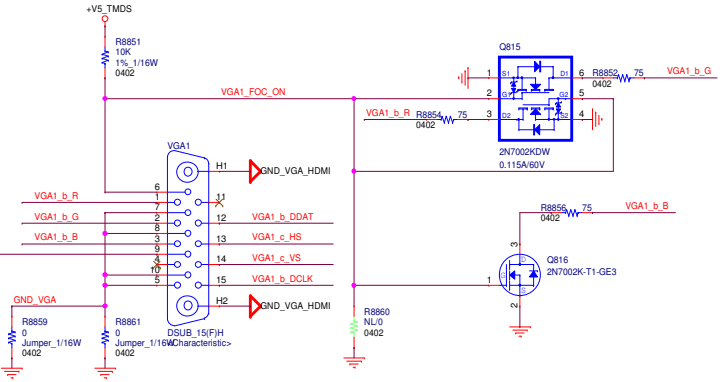
78m(A)@+V3.3

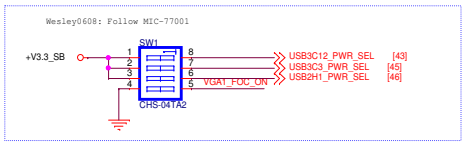


VGA1

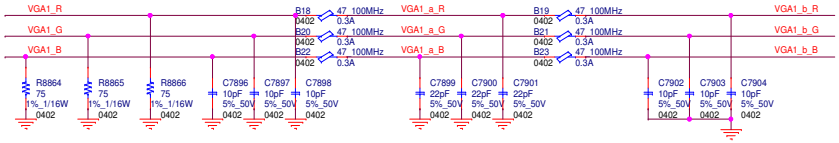








Z=37.5ohm
Z=75ohm for long distance
Z=50ohm for short distance



ADVANTECH		
Title	40_Display VGA1/CH7517	
Size	Document Number PCE-2129(2029)	Rev A101-2
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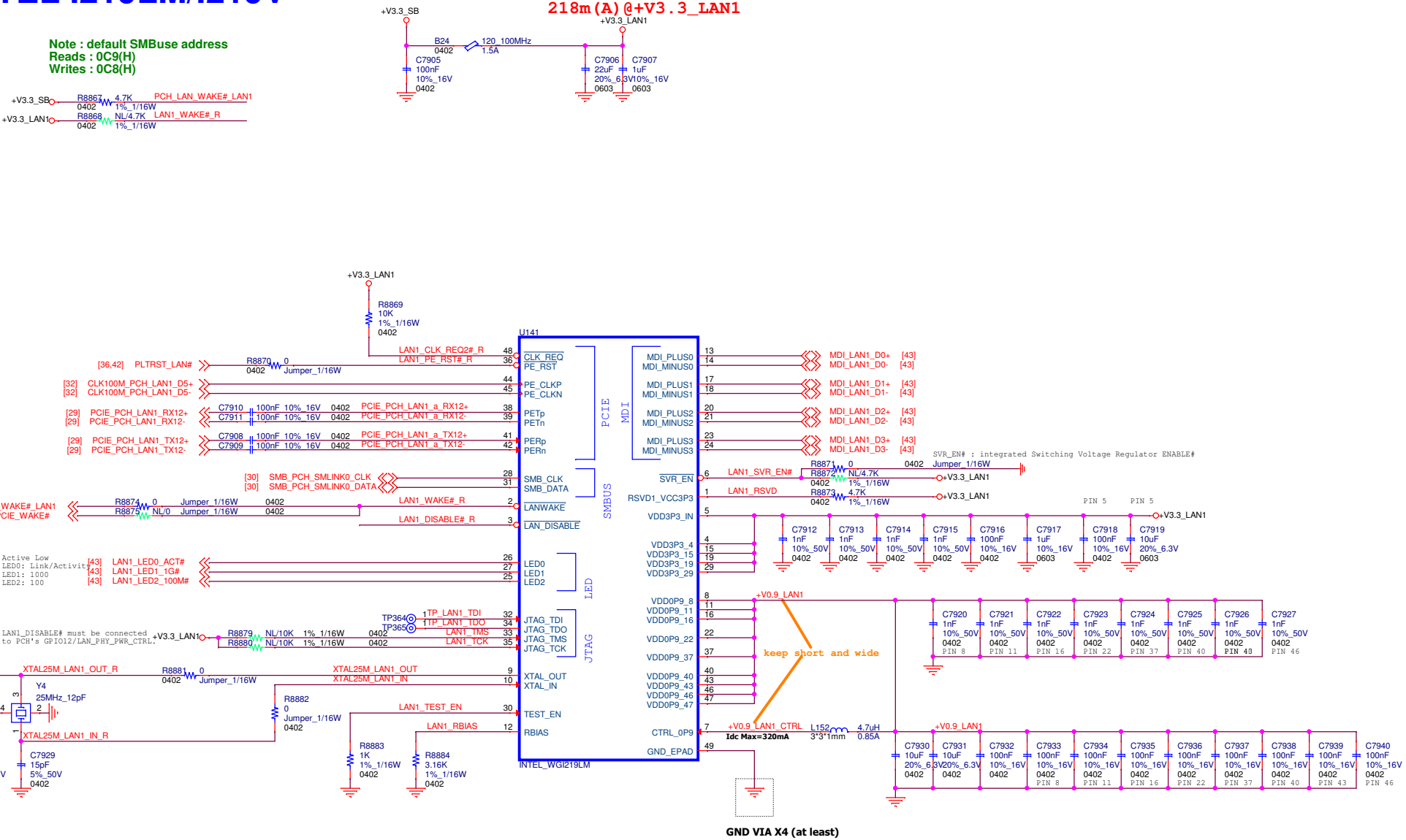
LAN1 INTEL I219LM/I219V

Note : default SMBuse address
Reads : 0C9(H)
Writes : 0C8(H)

218m(A)@+V3.3_LAN1



Title	41_LAN1 INTEL I219LM/I219V		
Size	Document Number	PCE-2129(2029)	Rev A101-2
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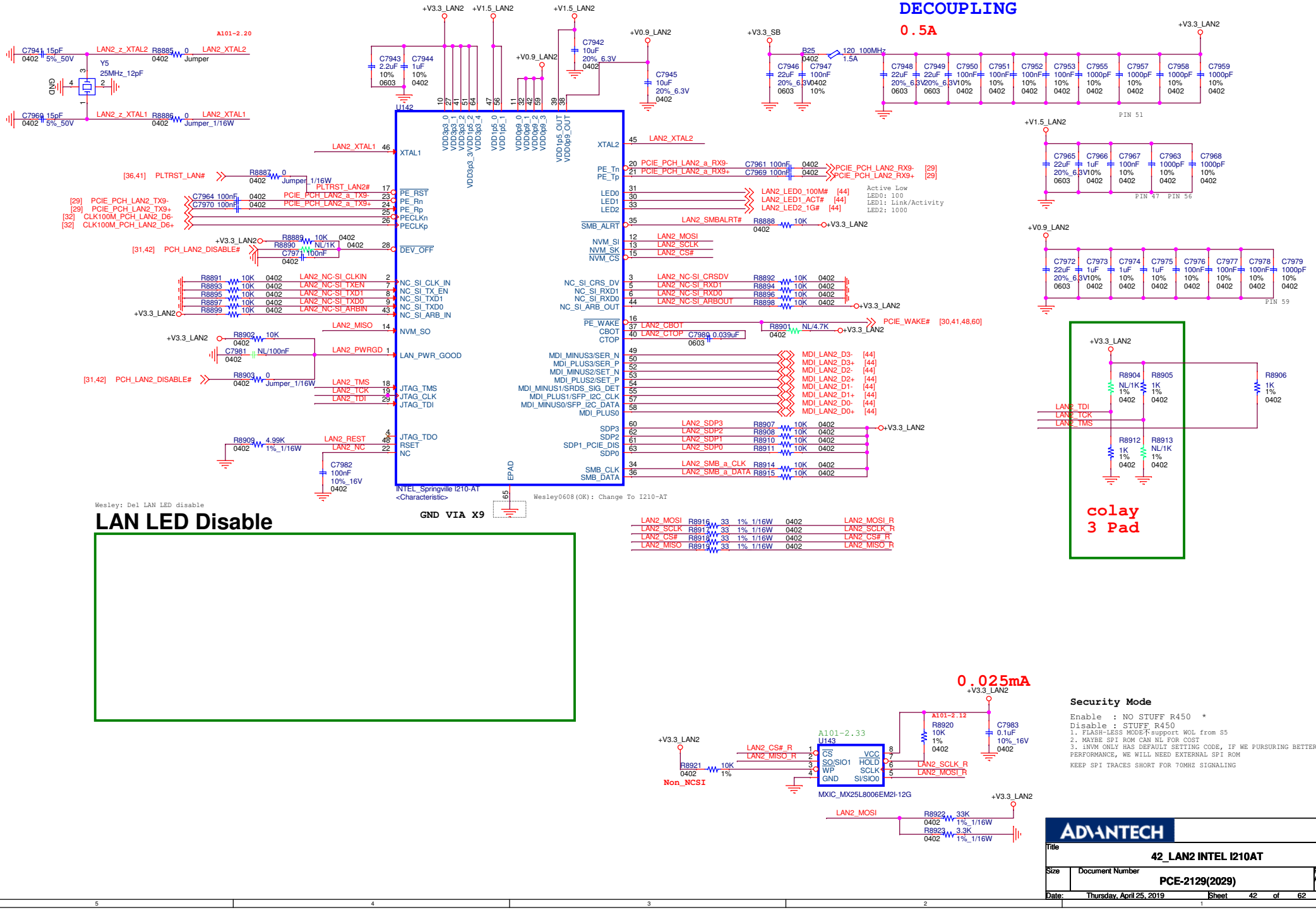
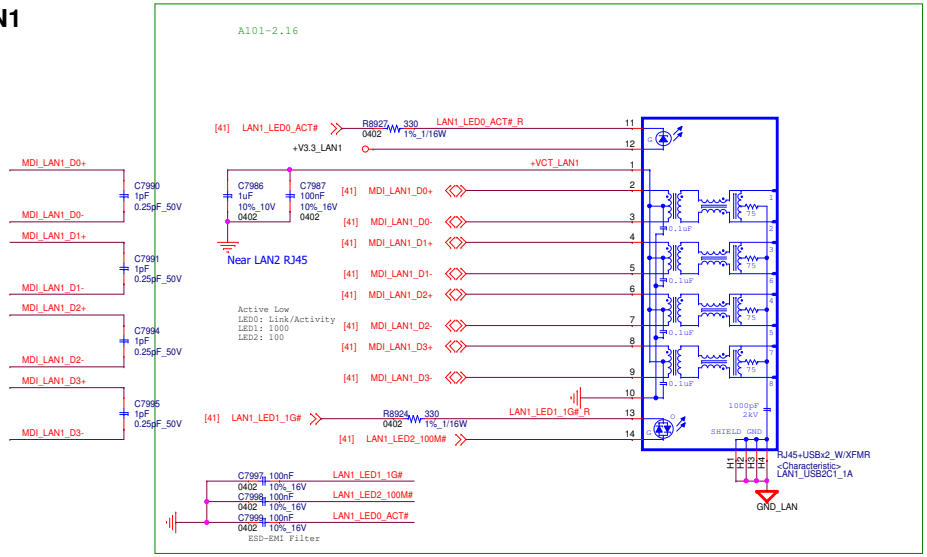
LAN2 INTEL I210AT

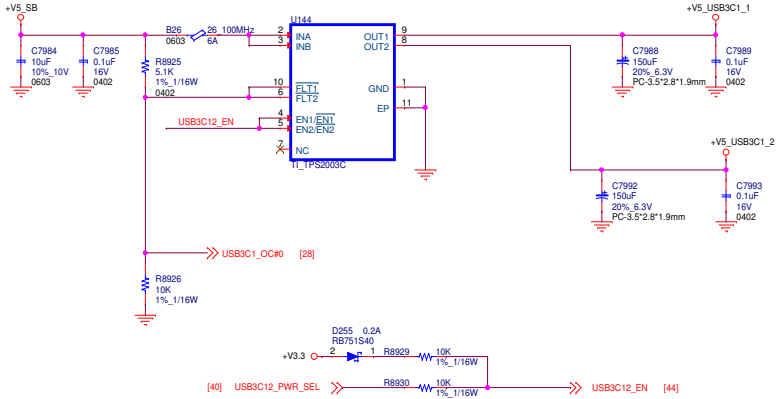


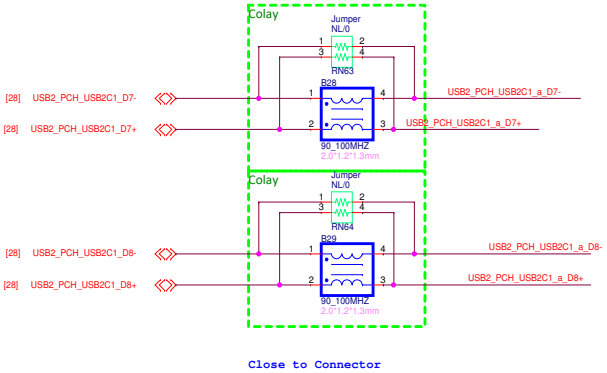
CONN LAN1/USB2C1

LAN1

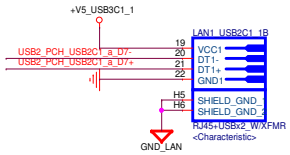


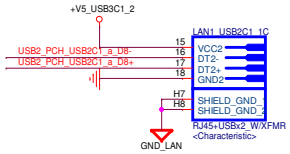
Power for USB2C1





USB PORT 1/2

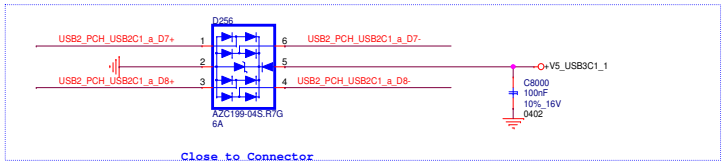


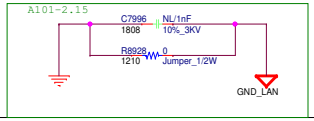


Giga LAN connector Left Side : Green/Orange LED	
Status	Display
10Mbps	Always turn off
100Mbps	Orange
1000Mbps	Green

Right Side : Green LED	
Status	Display
Link status	Always turn on without transmitting/receiving data
Activity status	Flash

ESD Protection Arrays





ADVANTECH

Title	43_CONN LAN1/USB3_12	
Size	Document Number: PCE-2129(2029)	Rev: A101-2
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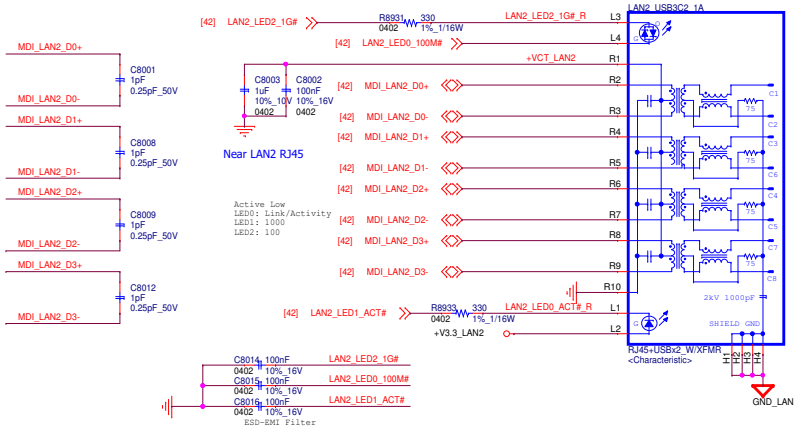
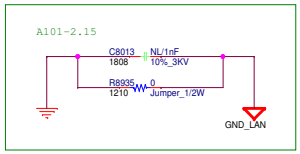
CONN LAN2/USB3C2

LAN2

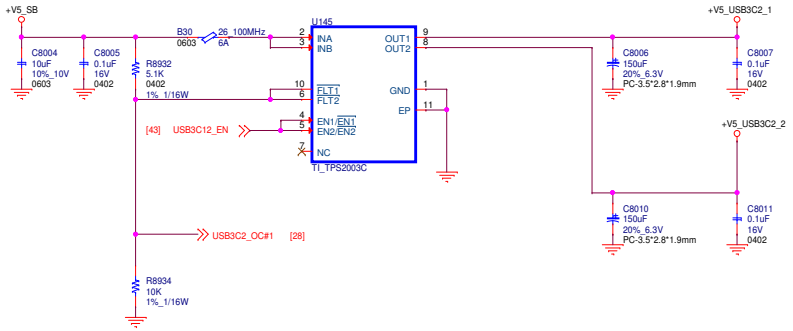


Giga LAN connector Left Side : Green/Orange LED	
Status	Display
10Mbps	Always turn off
100Mbps	Orange
1000Mbps	Green

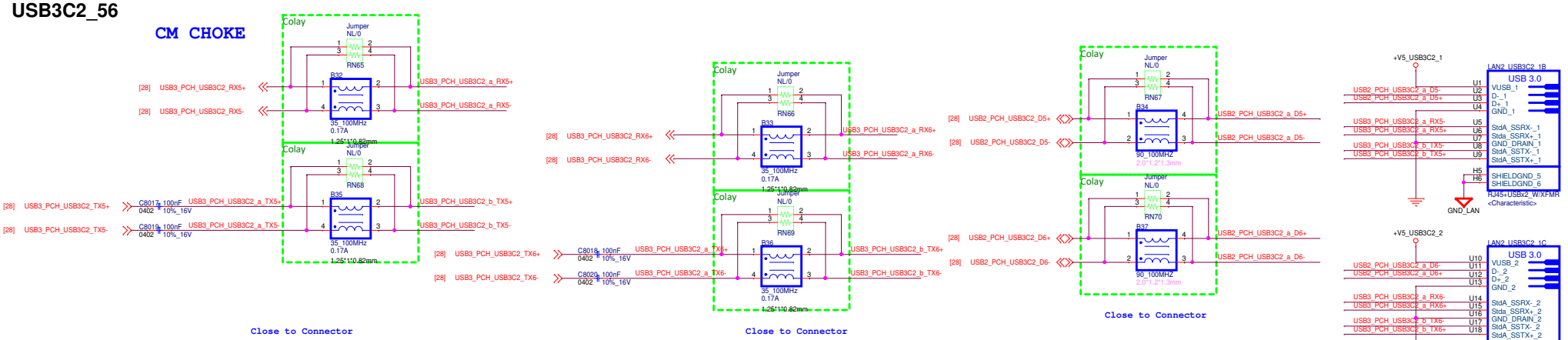
Right Side : Green LED	
Status	Display
Link status	Always turn on without transmitting/receiving data
Activity status	Flash



Power for USB3C2



USB3C2_56



USB2.0 Port 3-4

USB3.0 Port 3-4

ADVANTECH			
Title	44_CONN LAN2/USB3_34		
Size	Document Number PCE-2129(2029)		Rev A101-2
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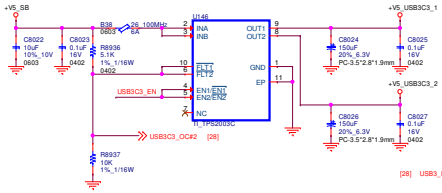
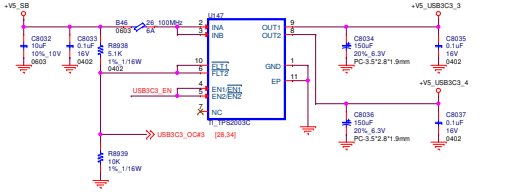
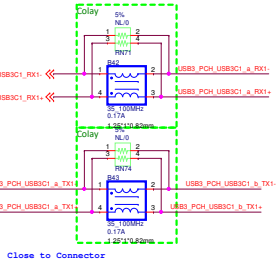
+V5_USB3C3_12@1.8(A)

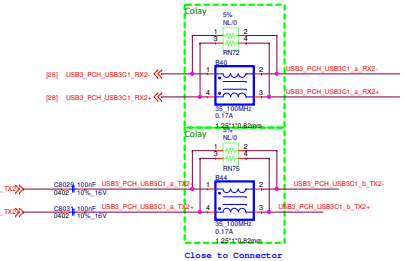


+V5_USB3C3_34@1.8(A)

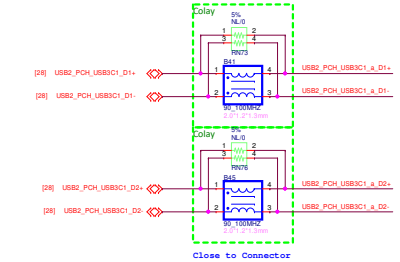




Close to Connector

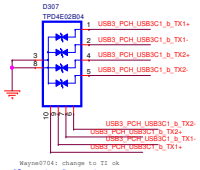


Close to Connector



Close to Connector

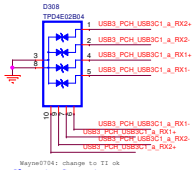
ESD Protection Arrays



Wayne0704: change to TI ok

Close to Connector

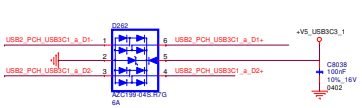
ESD Protection Arrays



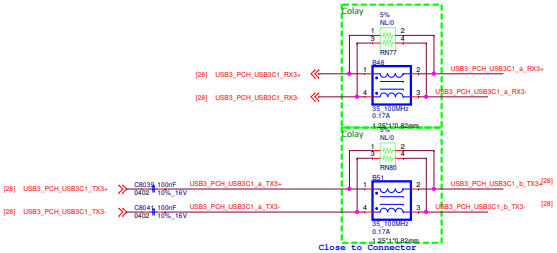
Wayne0704: change to TI ok

Close to Connector

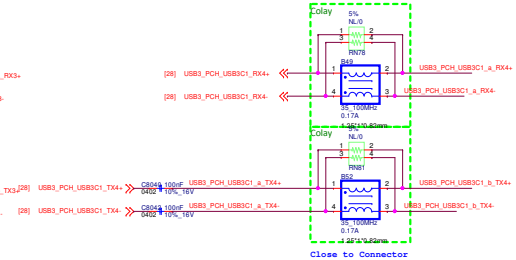
ESD Protection Arrays



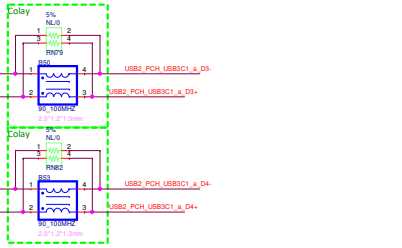
Close to Connector



Close to Connector

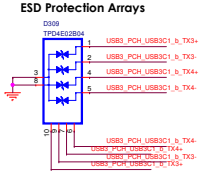


Close to Connector



Close to Connector

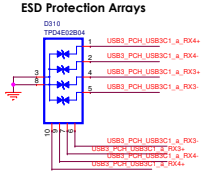
ESD Protection Arrays



Wayne0704: change to TI ok

Close to Connector

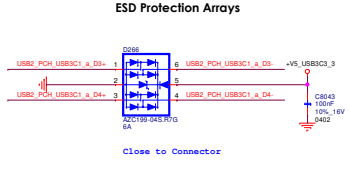
ESD Protection Arrays



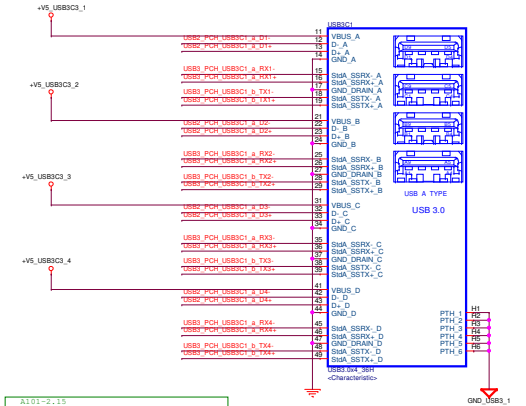
Wayne0704: change to TI ok

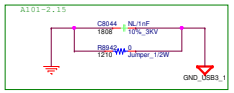
Close to Connector

ESD Protection Arrays



Close to Connector





ADVANTECH

Title	45_CONN USB32C3	
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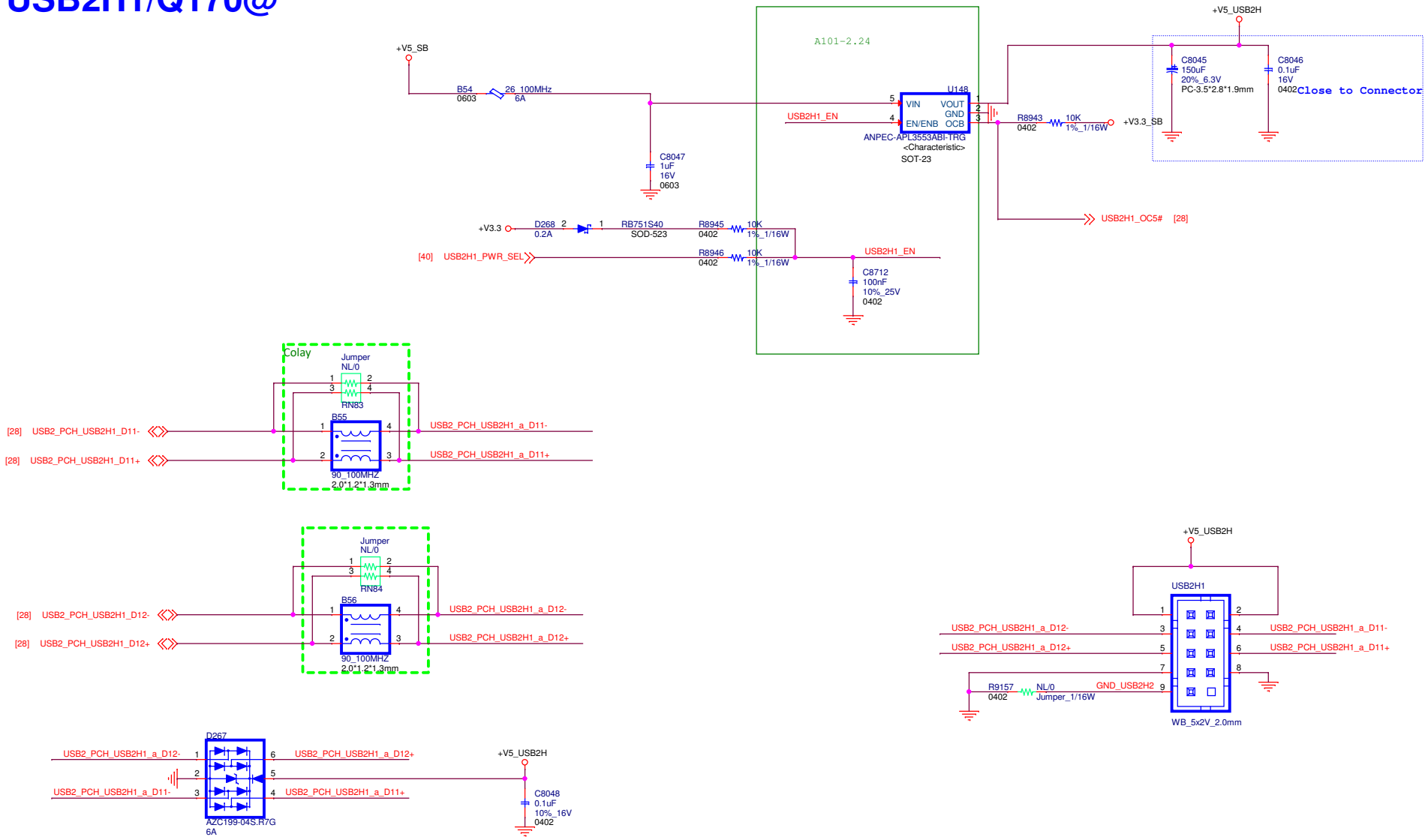
Internal USB2H1/Q170@



ADVANTECH

Title	46_CONN USB2.0_11~14	
Size	Document Number PCE-2129(2029)	Rev A101-2
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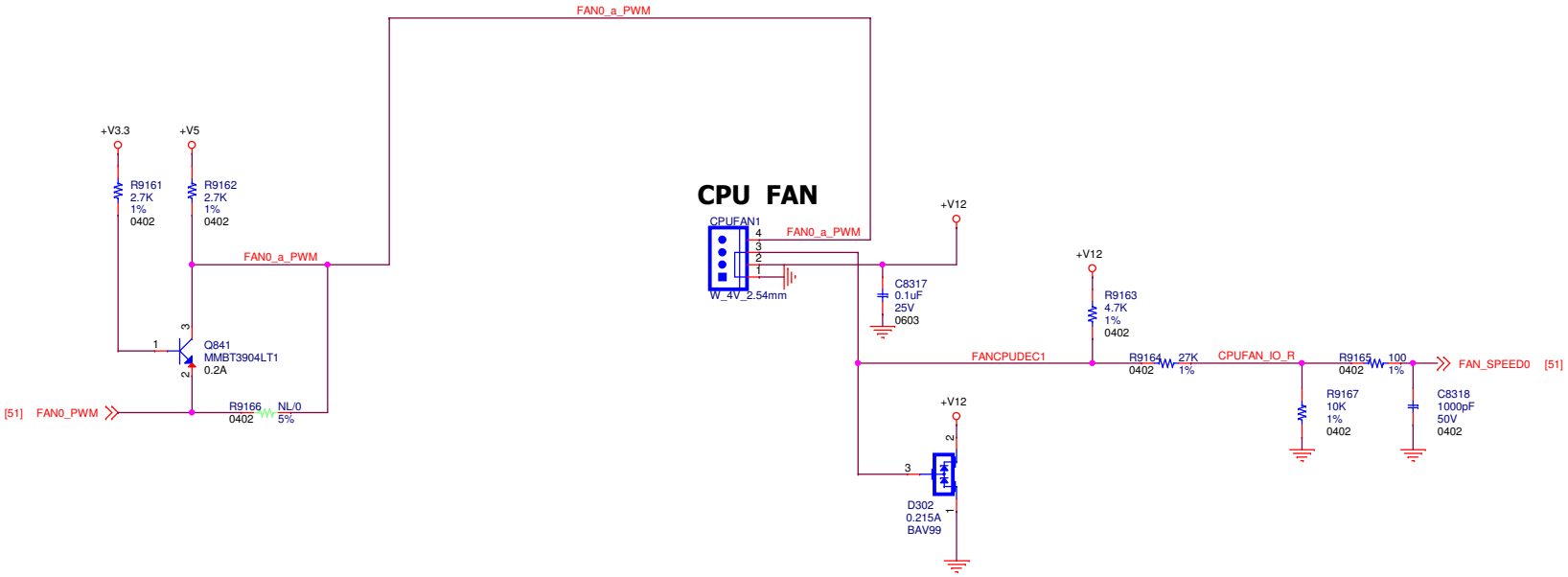
CPU FAN CONTROL
Refer AIIS-3410



ADVANTECH		
Title	CPU FAN	
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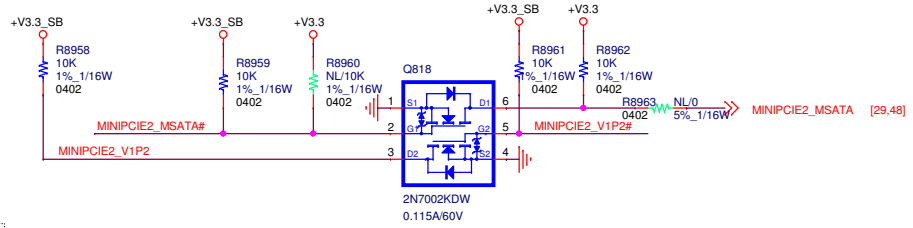
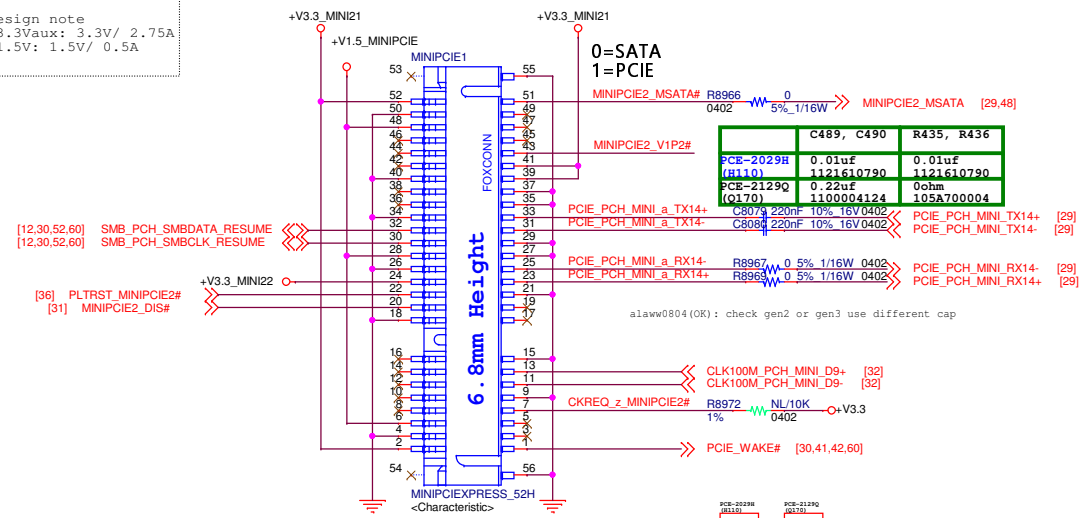
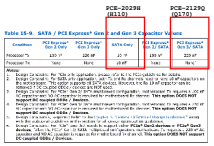
CONN MINIPCIE/mSATA Q170
mSATA H110

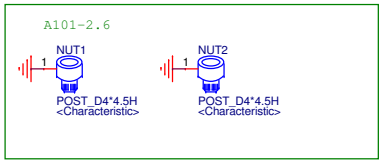


Design note
+3.3Vaux: 3.3V/ 2.75A
+1.5V: 1.5V/ 0.5A



	C489, C490	R435, R436
PCE-2029H (H110)	0.01uf 1121610790	0.01uf 1121610790
PCE-2129Q (Q170)	0.22uf 1100004124	0ohm 105A700004



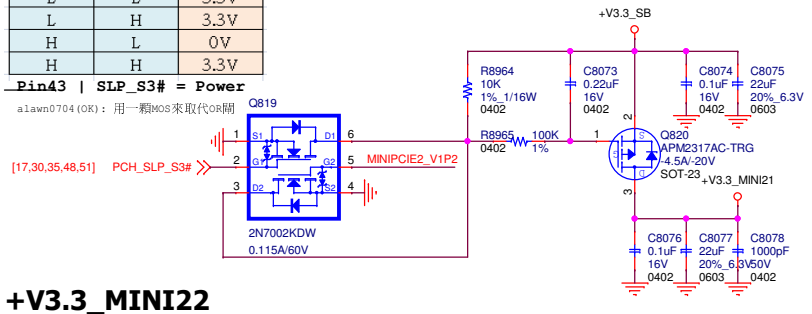


+V3.3_MINI21

Power of Pin2, 39, 41, 52		
Pin43	SLP_S3#	Power
L	L	3.3V
L	H	3.3V
H	L	0V
H	H	3.3V

Pin43 | SLP_S3# = Power

alawn0704(OK): 用一顆MOS來取代OR閘



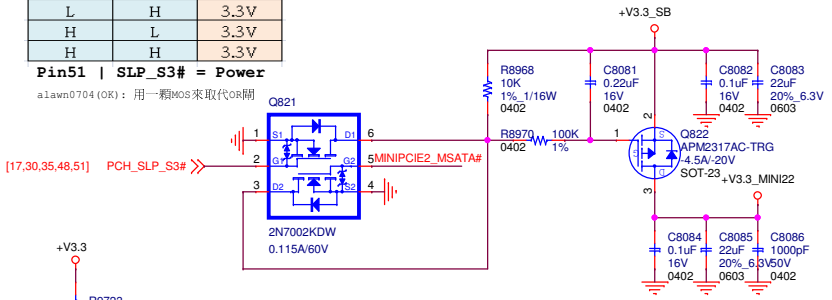
+V3.3_MINI22

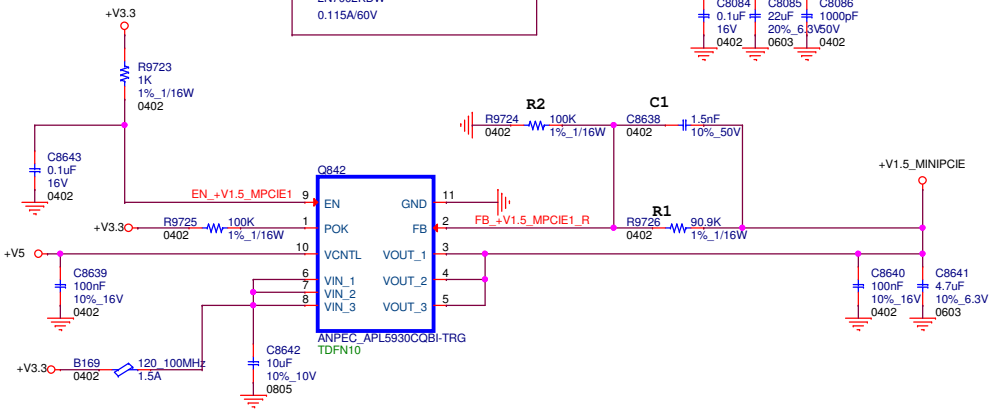
Power of Pin24		
Pin51	SLP_S3#	Power
L	L	0V
L	H	3.3V
L	H	3.3V
H	H	3.3V

Pin51 | SLP_S3# = Power

0.6A

alawn0704(OK): 用一顆MOS來取代OR閘



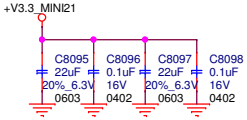


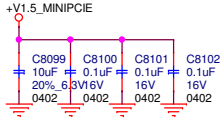
Wayne0704: change to APL5930 OK

Vout =0.8* (1+R1/R2)
Vout =0.8* (1+90.9/100)=1.52V

Pin	mini-pcie 1.1	mini-pcie 1.2	mSATA	
2	3.3V	3.3Vaux	3.3V	+V3.3_MINI21
24	3.3Vaux	3.3Vaux	3.3V	+V3.3_MINI22
39	Reserved*	3.3Vaux	3.3V	+V3.3_MINI21
41	Reserved*	3.3Vaux	3.3V	+V3.3_MINI21
52	3.3V	3.3Vaux	3.3V	+V3.3_MINI21

Spec.	Mini PCIe 1.1	Mini PCIe 1.2	mSATA
Pin43	Reserved (H)	GND (L)	NC (H)
Pin51	Reserved (H)	Reserved (H)	Presences Detection (GND->L)





ADVANTECH

Title	mPCIE/mSATA	
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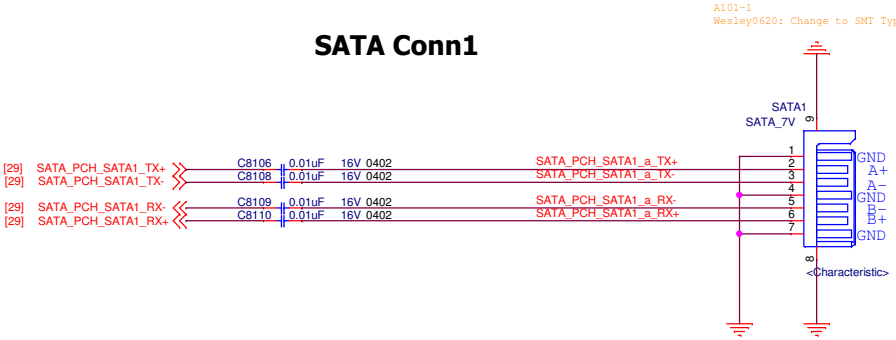
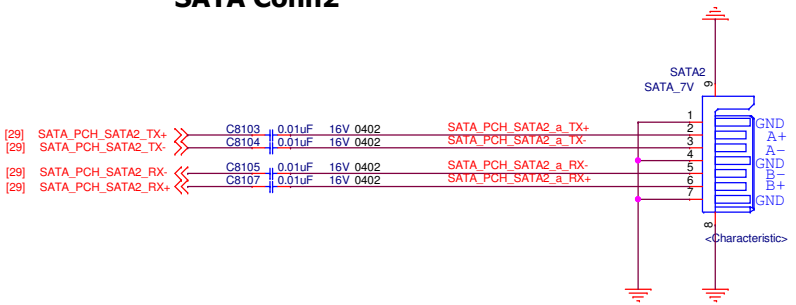
CONN SATA1 , 2

SATA Conn1

A101-1
Wesley0620: Change to SMT Type Conn



SATA Conn2



ADVANTECH

Title	SATA CONN 1 and 2	
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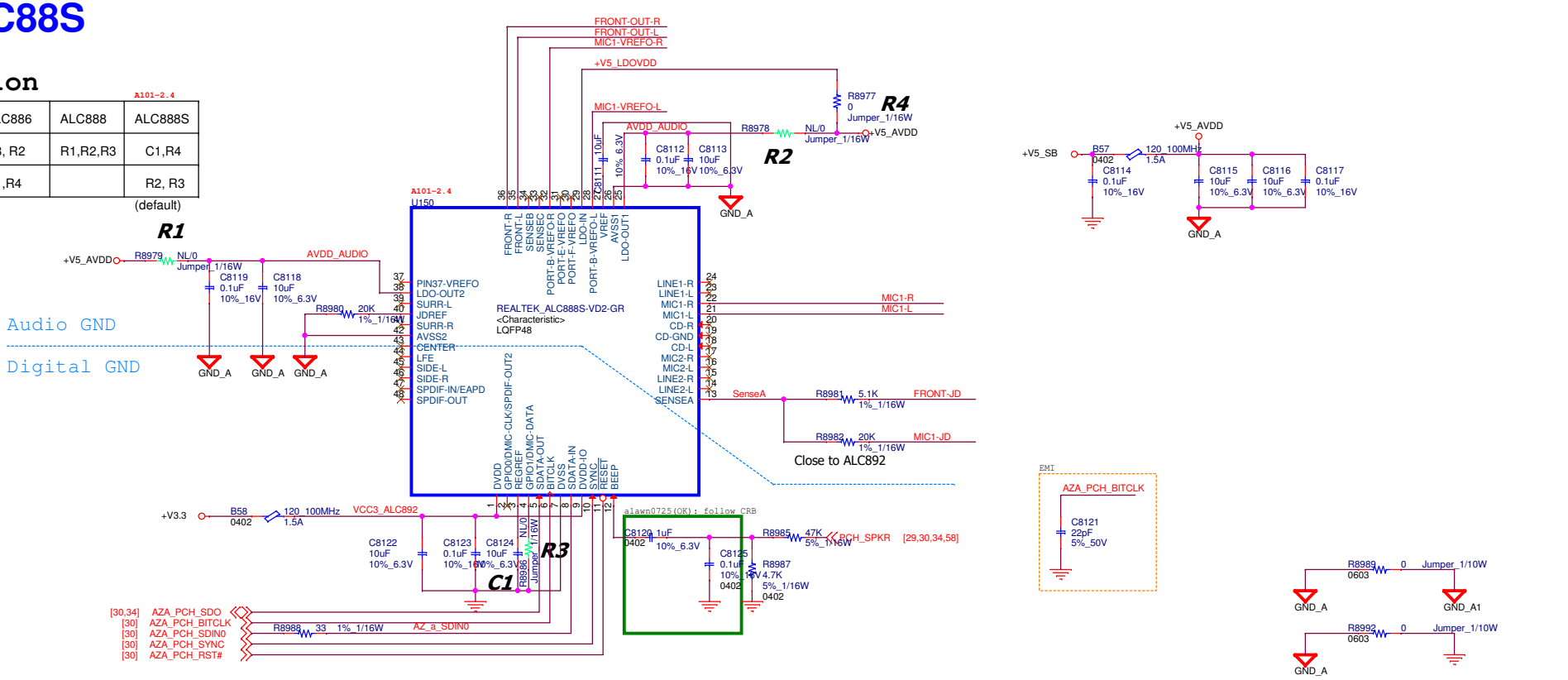
Audio ALC88S

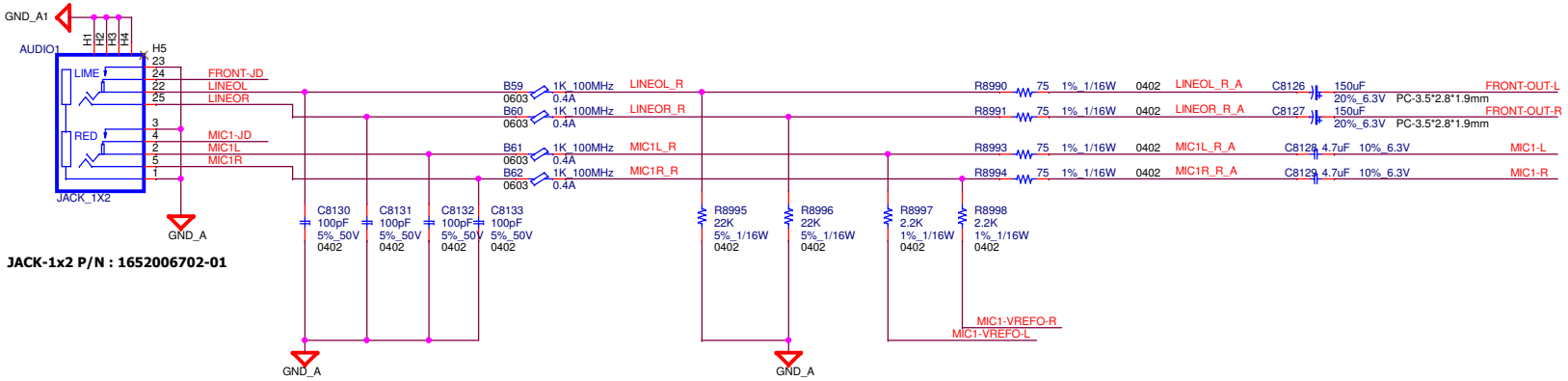
IC BOM Option

	ALC892	ALC886	ALC888	ALC888S
Stuff	C1,R4	R3, R2	R1,R2,R3	C1,R4
Empty	R2, R3	C1,R4		R2, R3

A101-2.4 (default)



AUDIO_JACK1



JACK-1x2 P/N : 1652006702-01

William0418 : 0 ohm change to 3KV

Title	50_Audio ALC888S		
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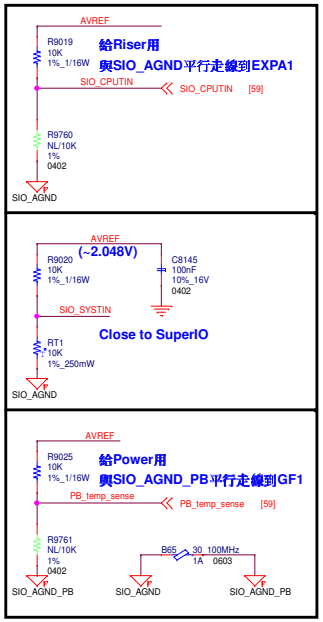
SIO NCT6106D

SIO old version 1410022361

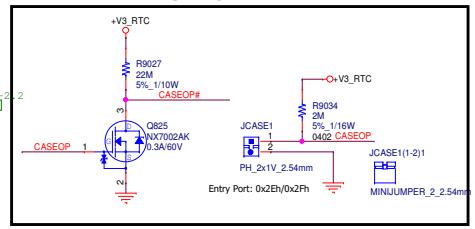
Thermistor



POWER ON SETTING PIN

PIN	Name	0	1	Strapping Power
51	UART1_RTS#	2E	4E	3VCC
52	UART1_DTR#	24M Clock Source	48M Clock Source	3VCC
54	UART1_SOUT	GPIO to PORT80 Disable	GPIO to PORT80 Enable	3VCC
106	SUPLED	UART	DSW	3VSB
111	UART3_RTS#	SOUTC to 80port disable	SOUTC to 80port enable	3VCC
112	UART3_DTR#	SOUTE to 80port disable	SOUTE to 80port enable	3VCC

JCASE1 : case open pin header



Title	51_SIO NCT6106D
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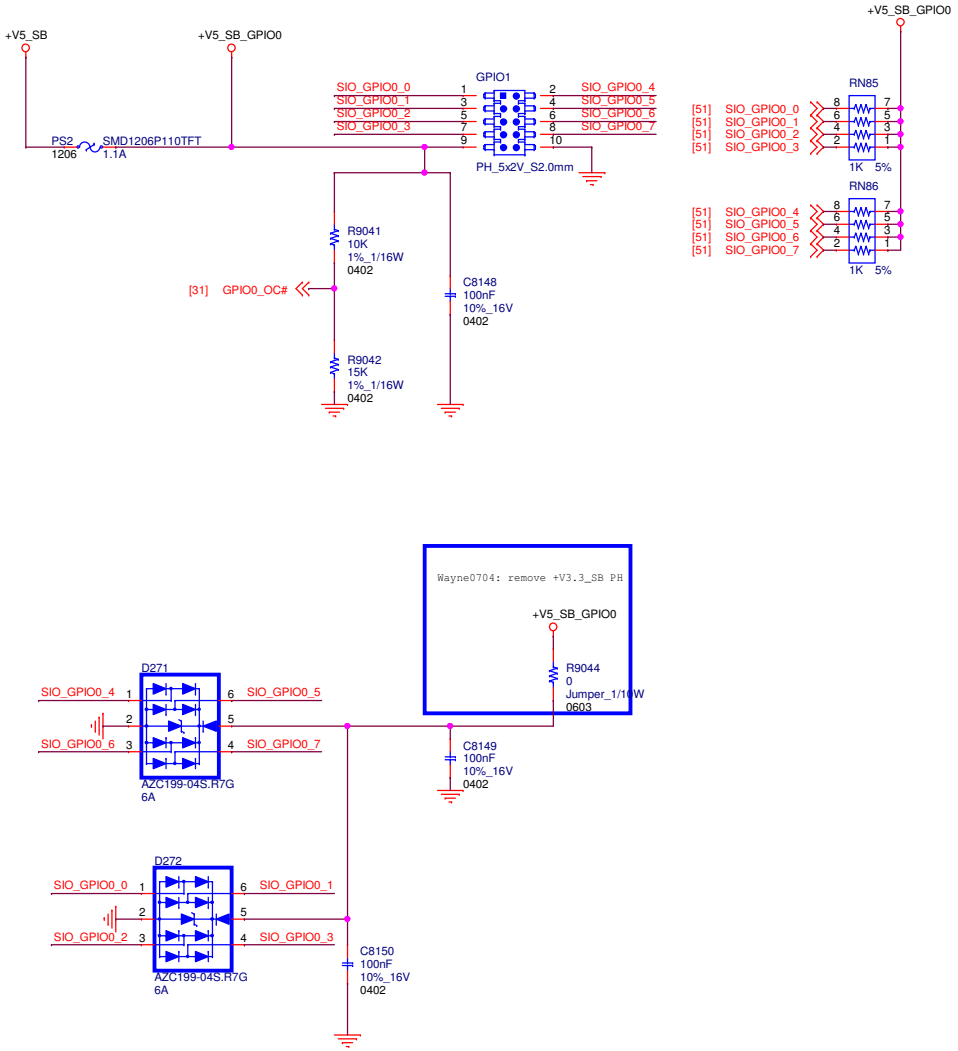
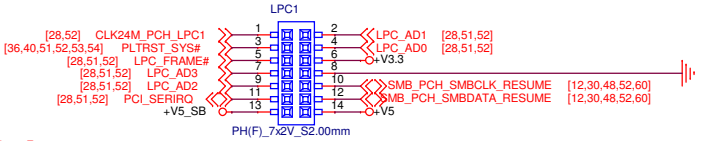
CONN GPIO0/LPC1

8 bit GPIO0



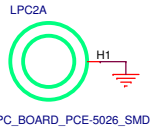
LPC1 for isolation COM module

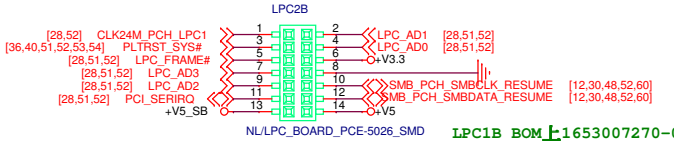


0.5(A)@+V5_SB

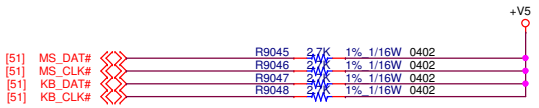
0.5(A)@+V3.3

0.5(A)@+V5





LPC1B BOM 1653007270-01:
Part_Number 00A0000083
Part_Number_Value 1653007270-01



A101-1
Wesley0608: Del K.B. & MOUSE

ADVANTECH

Title	52_CONN GPIO0, 1/LPC1/KBMS1	
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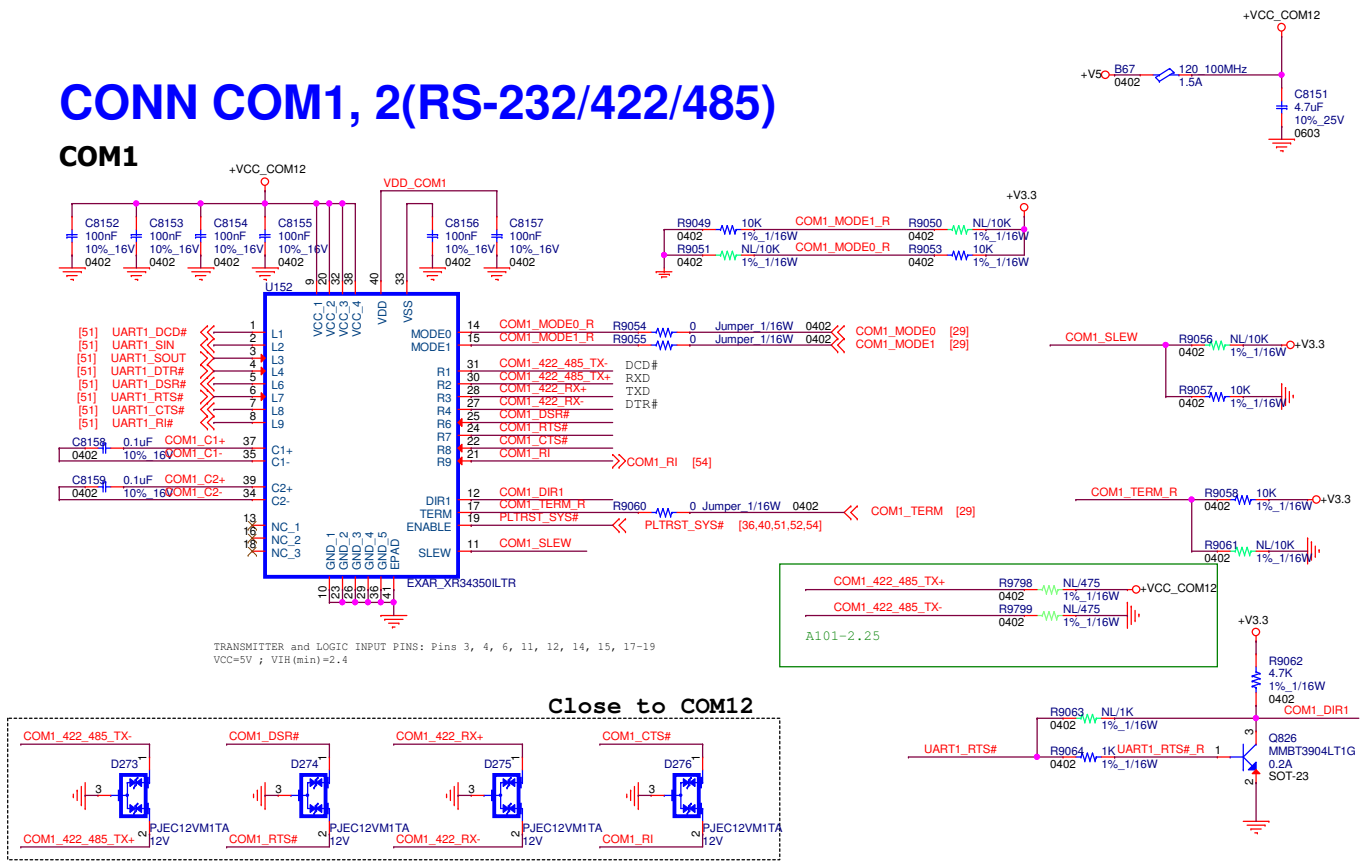
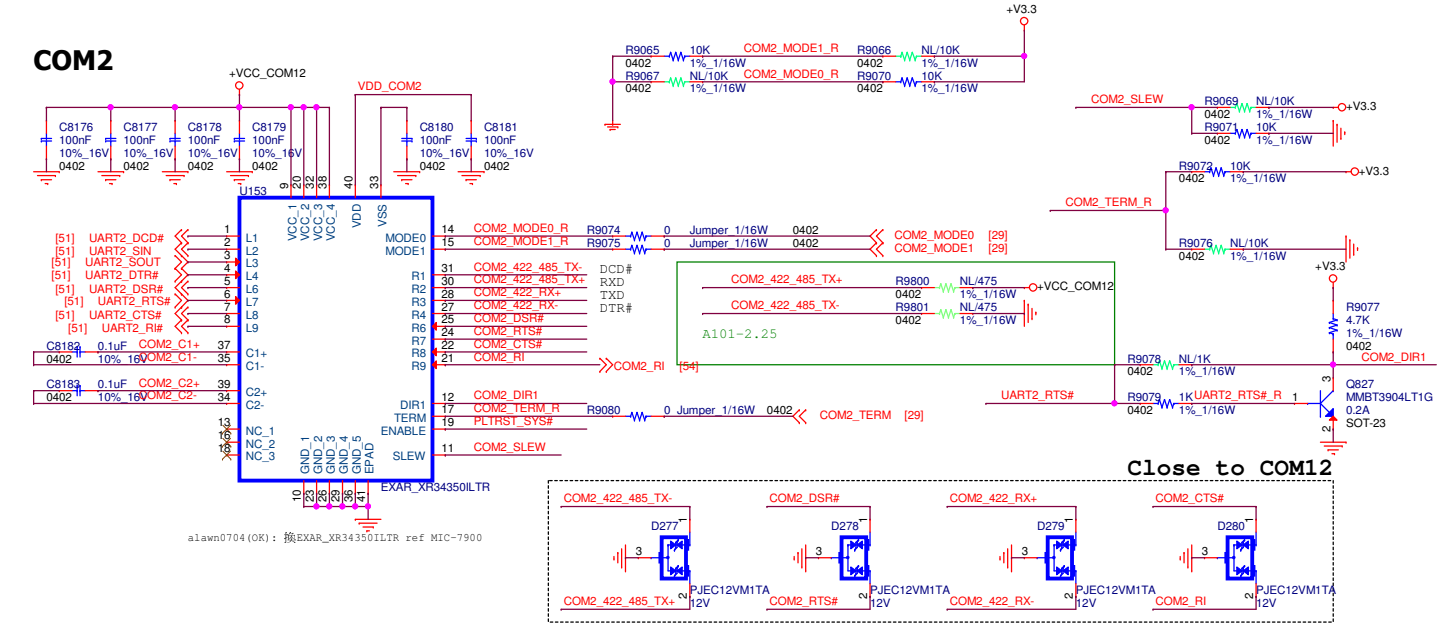
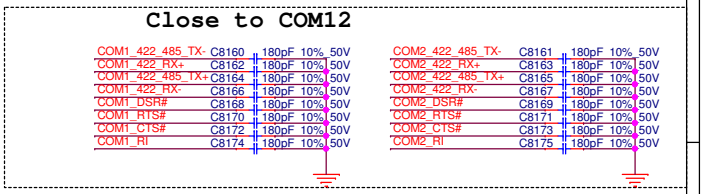
CONN COM1, 2(RS-232/422/485)

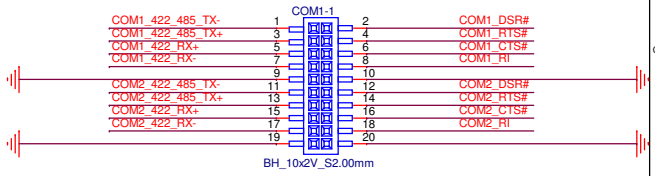
COM1



COM2







COM1/2 SP339E	LOOP BACK	RS-232	RS-485 half duplex	RS-485/422 full duplex
Mode0	0	1	0	1
Mode1	0	0	1	1
TERM	X	X	1	1
SLEW	0	0	0	0

TERM : Enables RS-485/422 receiver termination
SLEW : SLEW = VCC enables 250kbps slew limiting in all modes

Pin	RS-232	RS-422	RS-485
1	COM1_DCD	TXD-	Data-
2	COM1_SIN#	TXD+	Data+
3	COM1_SOUT#	RXD+	NC
4	COM1_DTR	RXD-	NC
5	GND	GND	GND
6	COM1_DSR	NC	NC
7	COM1_RTS	NC	NC
8	COM1_CTS	NC	NC
9	COM1_RI	NC	NC
10	GND_F	GND_F	GND_F
11	GND_F	GND_F	GND_F

ADVANTECH

Title	53_CONN COM1, 2(RS-232/422/485)	
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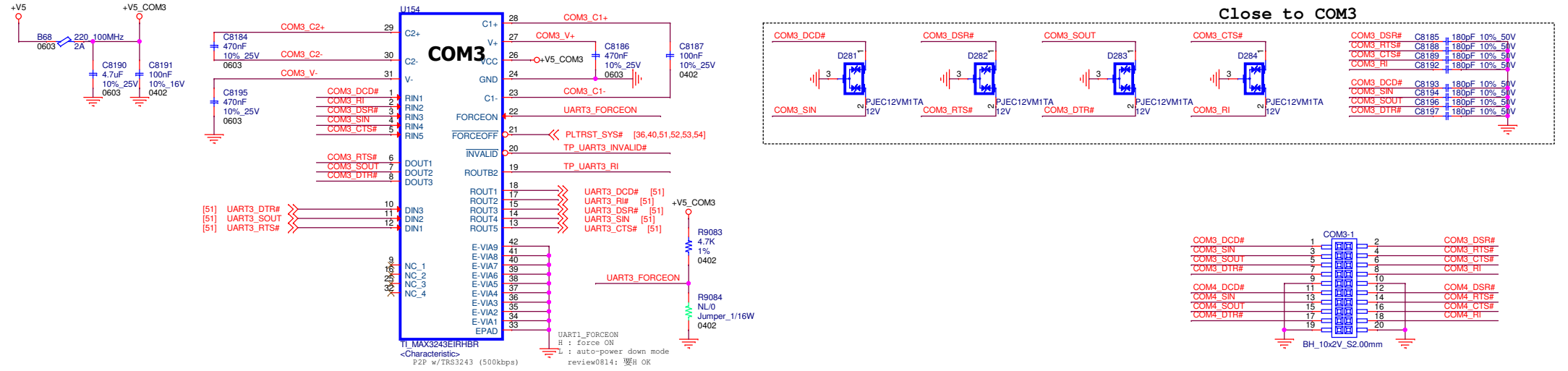
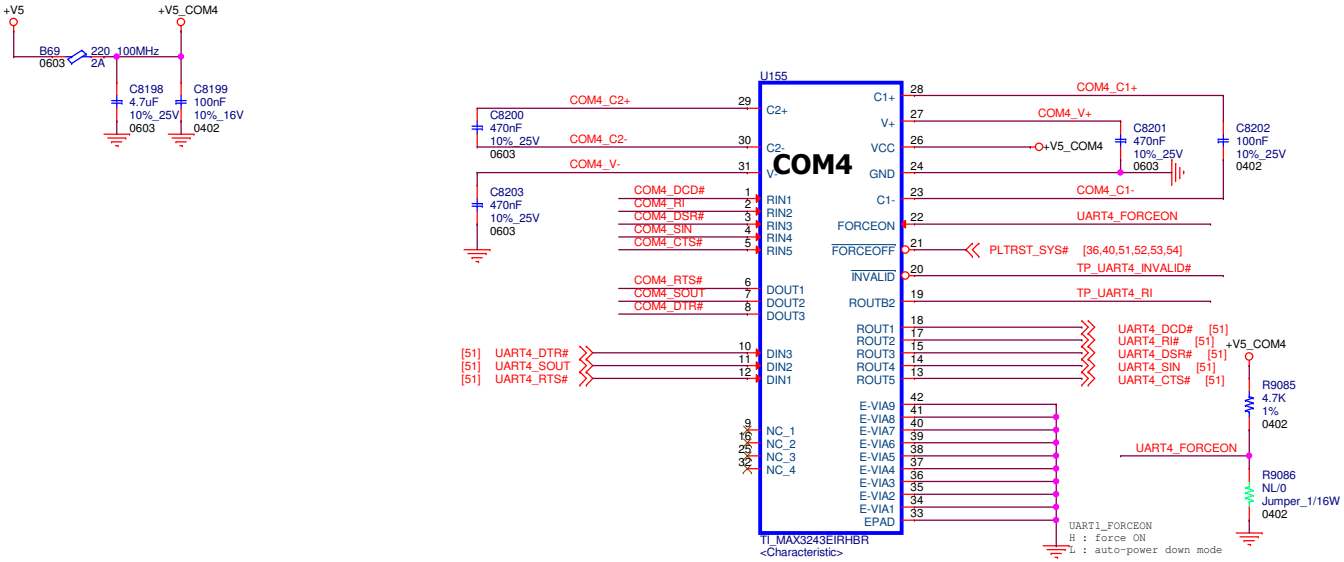
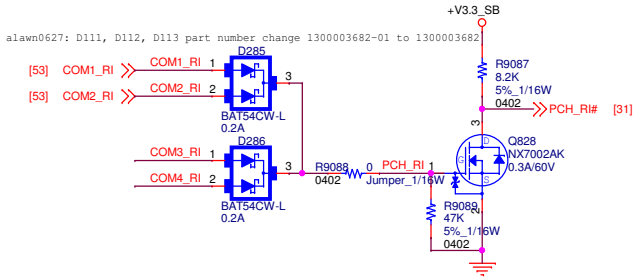
CONN COM3, 4(RS-232)/RING ON



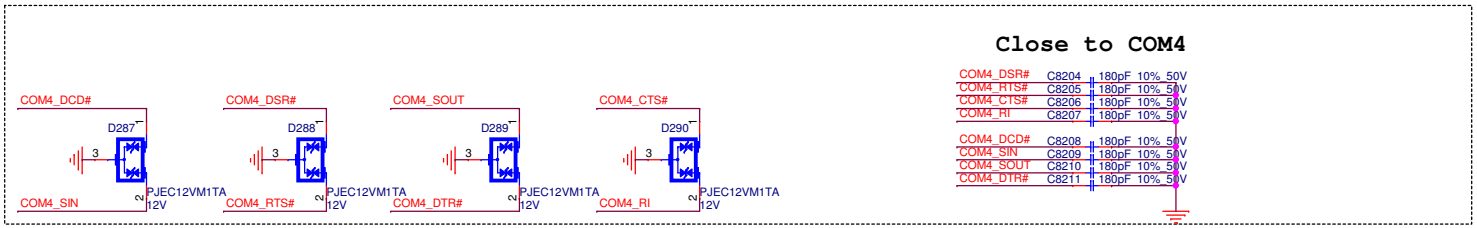
Close to COM3



Ring ON



Close to COM4



ADVANTECH

Title	54_CONN COM3, 4(RS-232)/RING ON	
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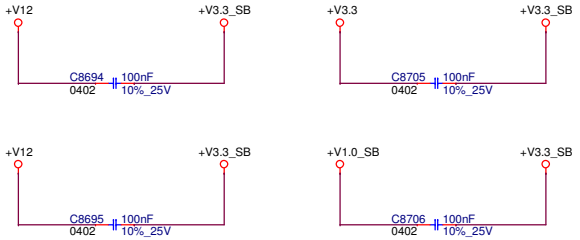
Stitching Capacitors



ADVANTECH		
Title		
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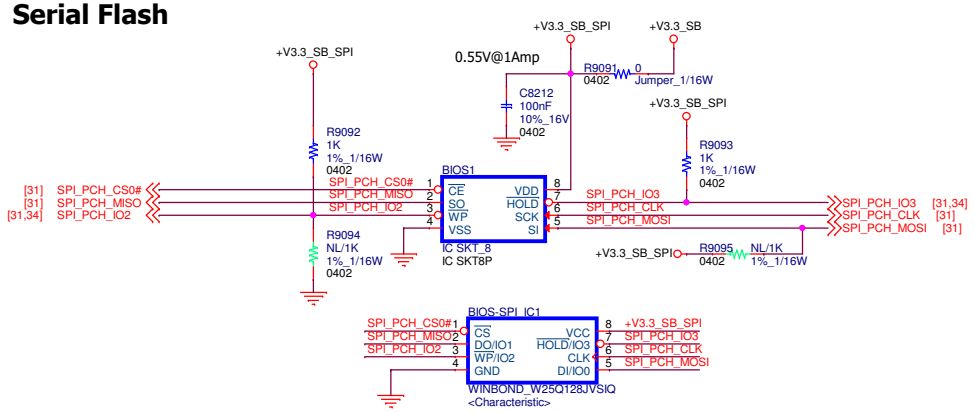
SPI/Security/LED

Serial Flash



A101-2.17

D Type Flip Flop

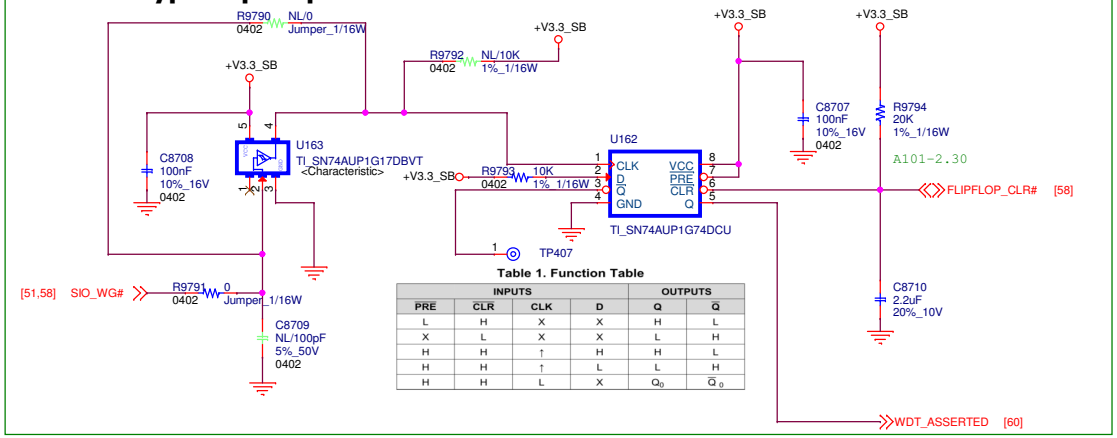
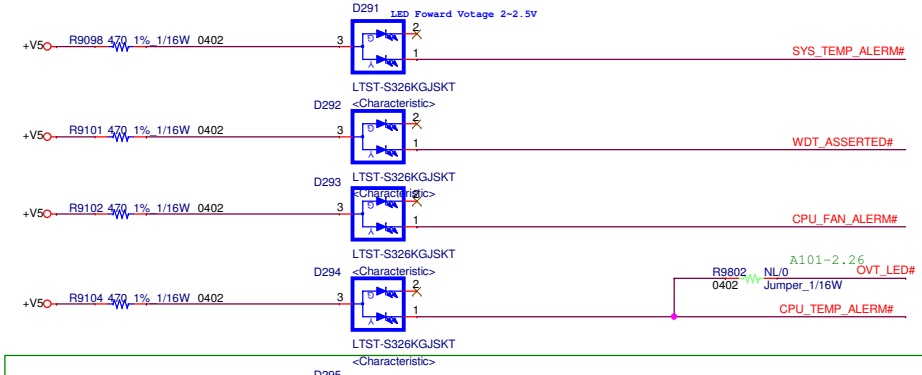
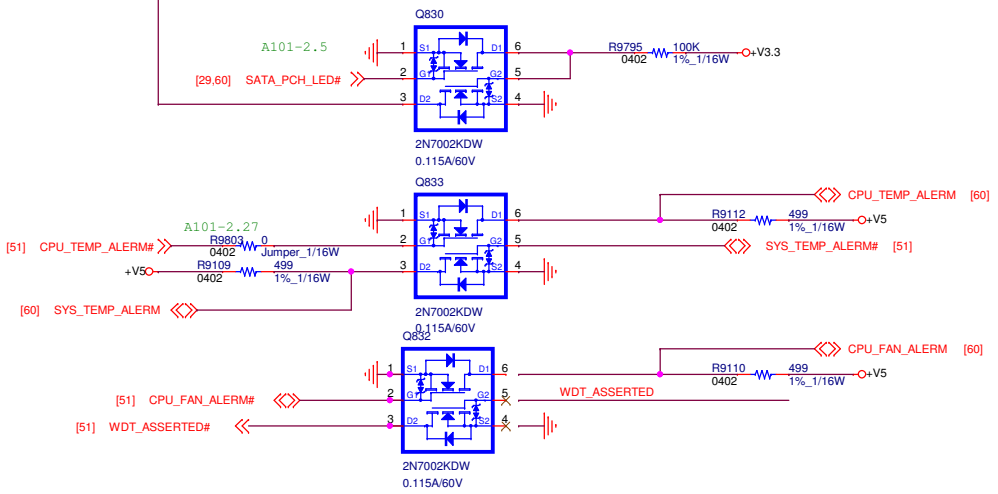


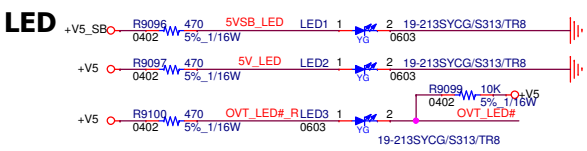
Table 1. Function Table

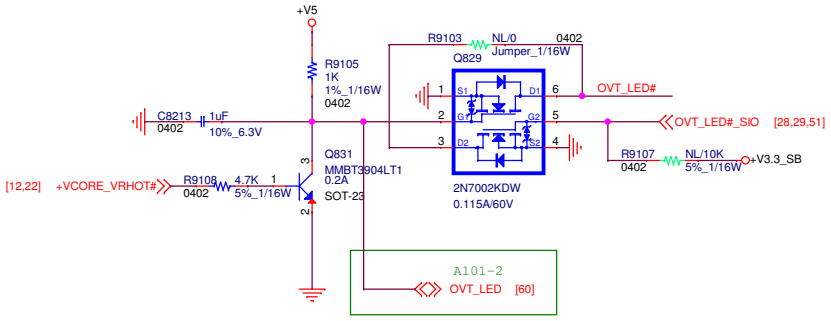
INPUTS				OUTPUTS	
PRE	CLR	CLK	D	Q	Q̄
L	H	X	X	H	L
X	L	X	X	L	H
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\bar{Q}_0$





LED





ADVANTECH

Title	56_SPI/Security/LED	
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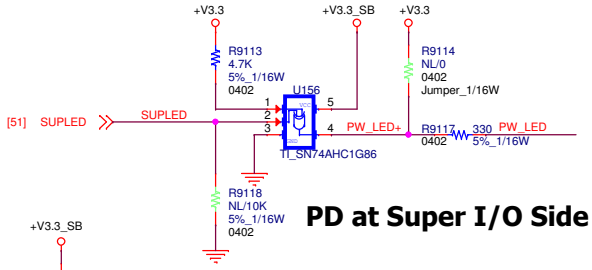
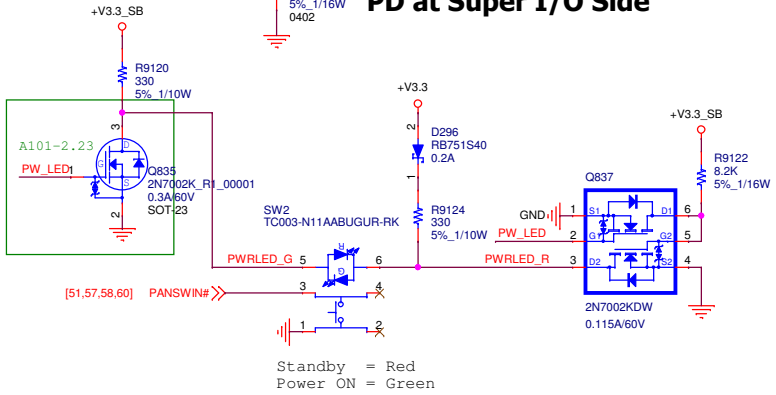
PWRBTN/AT_ATX Mode

PWRBTN

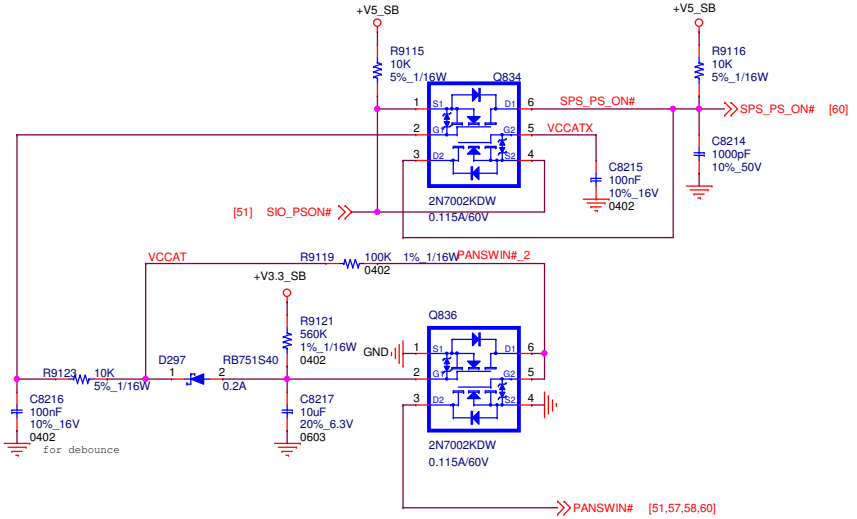


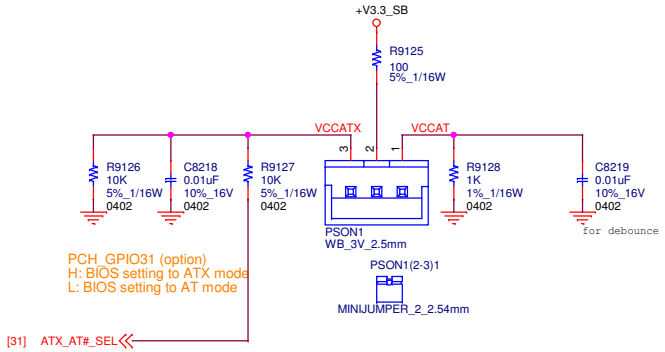
PD at Super I/O Side

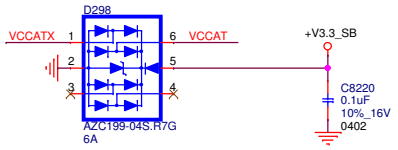


Standby = Red
Power ON = Green

ATX/AT Mode Selection







Mode	Jumper Setting
AT	1-2 Short
ATX	2-3 Short (Default)

ADVANTECH

Title	57_PWRBTN/AT_ATX Mode	
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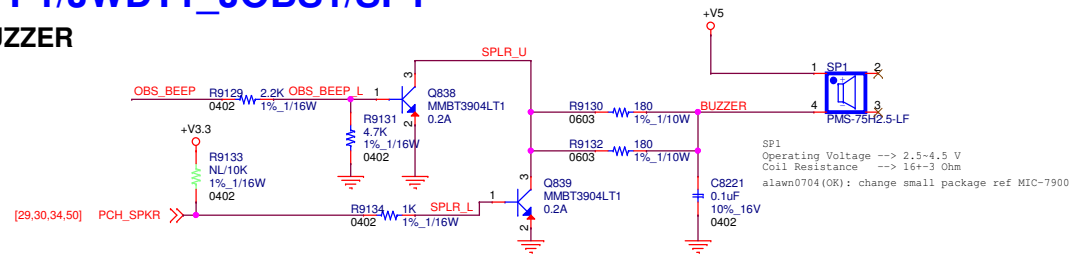
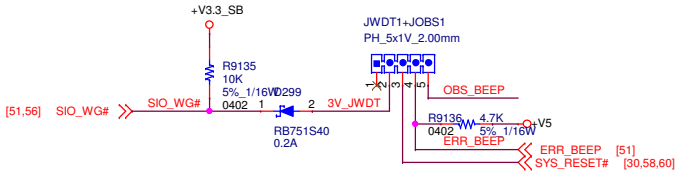
JFP1/JWDT1_JOBS1/SP1

BUZZER



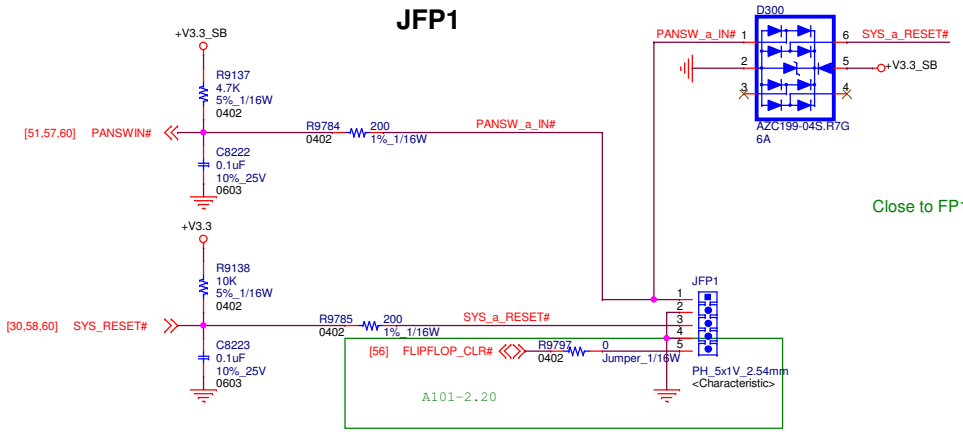
JWDT1_JOBS1



JWDT1_JOBS1(2-3)1
MINIJUMPER_2_2.0mm
<Characteristic>

JWDT1_JOBS1(4-5)1
MINIJUMPER_2_2.0mm
<Characteristic>

JFP1



Close to FP1

A101-1
Wesley0608: Del Remote PWRBTN Conn and move to BP

ADVANTECH

Title	58_JFP1/JWDT1_JOBS1/SP1	
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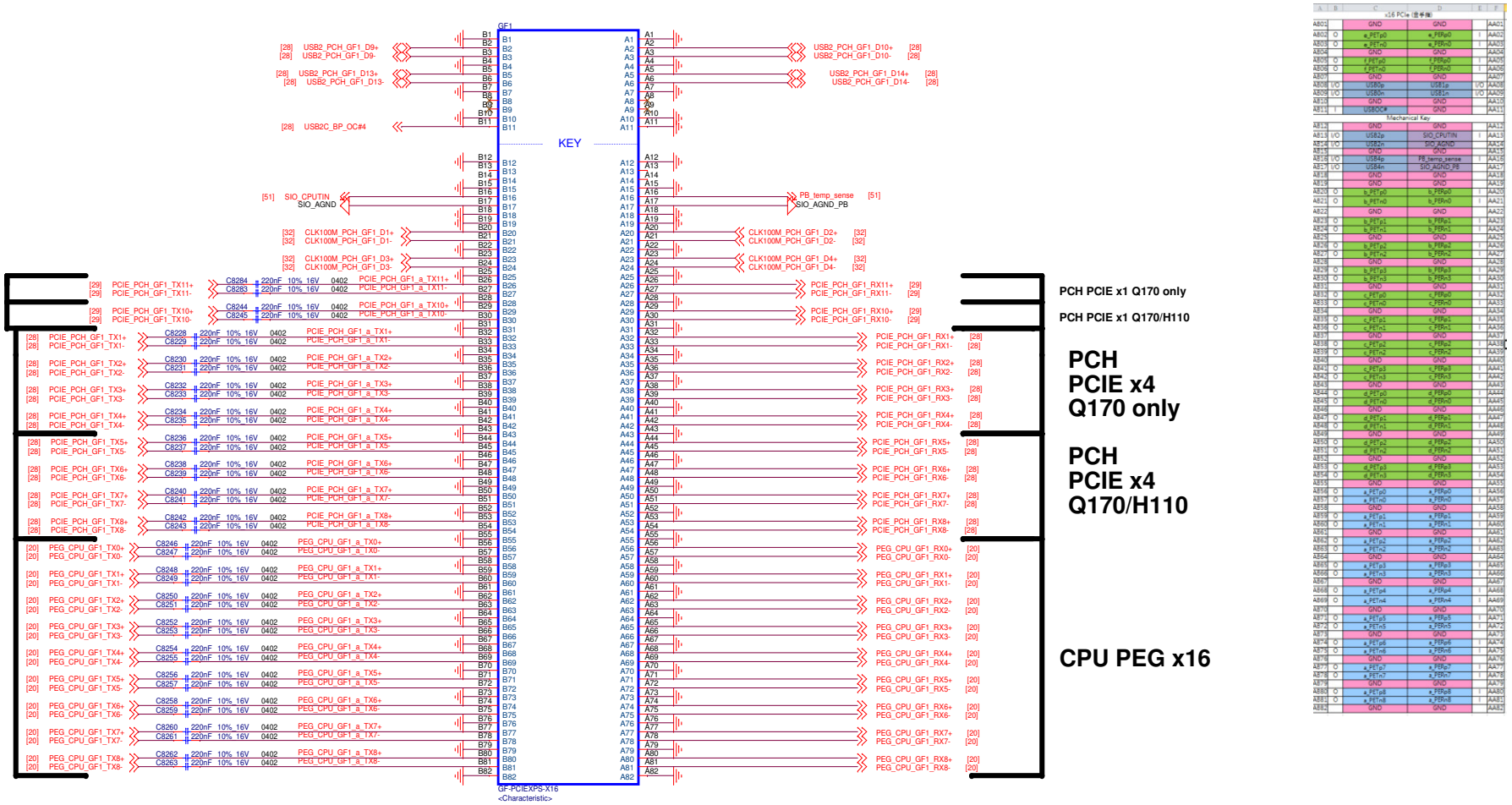
PCIE x16 GF A

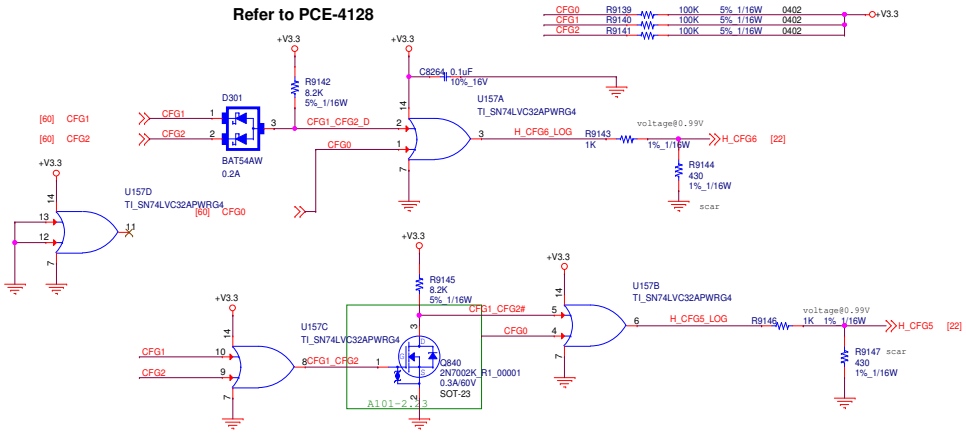
	C8236~C8243
PCE-2029 (U110)	0.1uF 1100000332
PCE-2129 (Q170)	0.22uF 1100004124



OTG Table

PCI-E x16 / x8 / x4 Configuration Table

From BP				To CPU1		
CFG0	CFG1	CFG2		H_CFG6	H_CFG5	PEG
1	---	---	→	1	1	1 x16
0	1	1	→	1	0	2 x8
0	1	0	→	0	0	1 x8/2 x4
0	0	0	→	0	1	4 x4(Reserved)



Title	59_CONN EXPANSION Module
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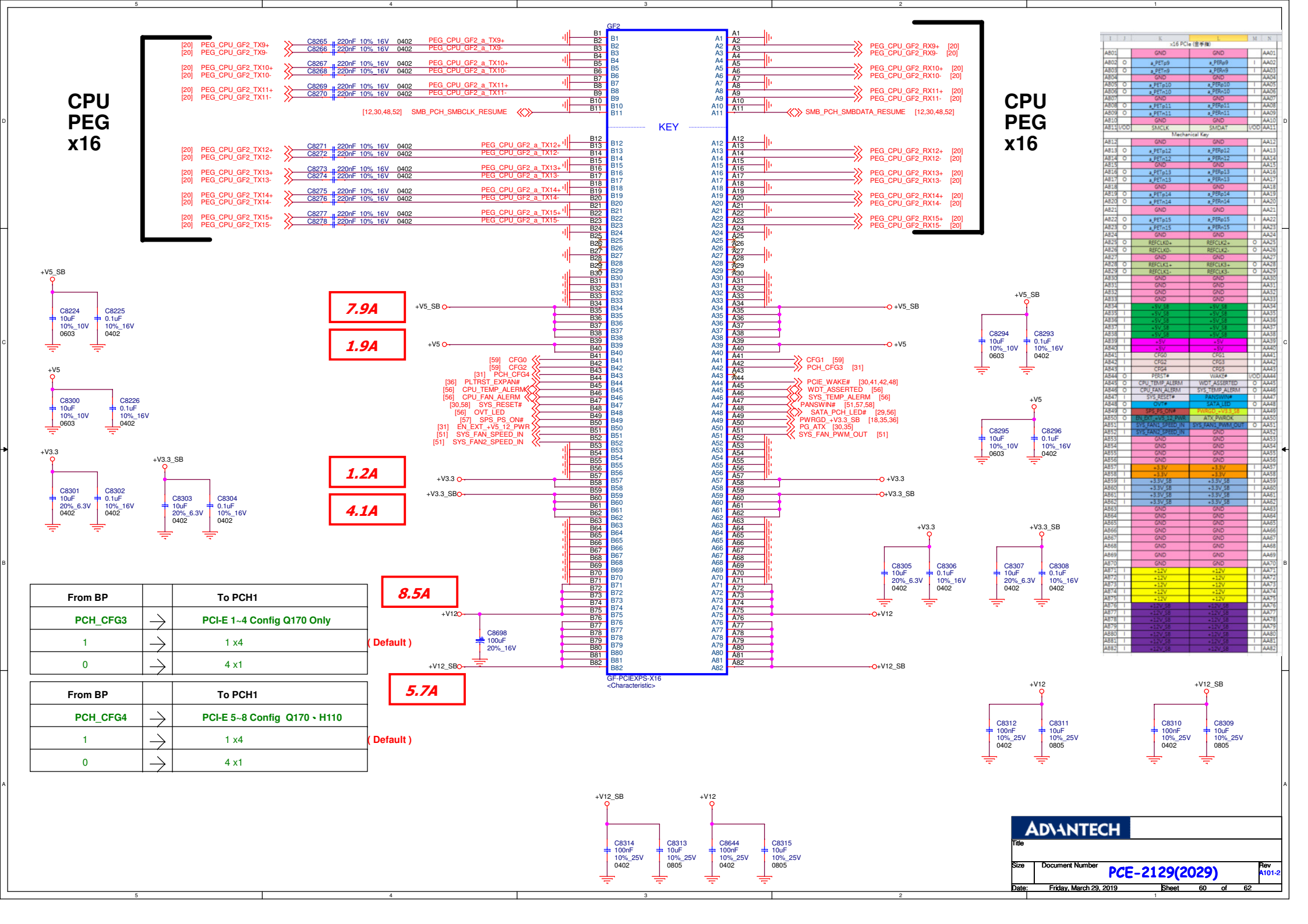

From BP		To PCH1	
PCH_CFG3	→	PCI-E 1~4 Config Q170 Only	
1	→	1 x4	(Default)
0	→	4 x1	

From BP		To PCH1	
PCH_CFG4	→	PCI-E 5~8 Config Q170、H110	
1	→	1 x4	(Default)
0	→	4 x1	

Title			
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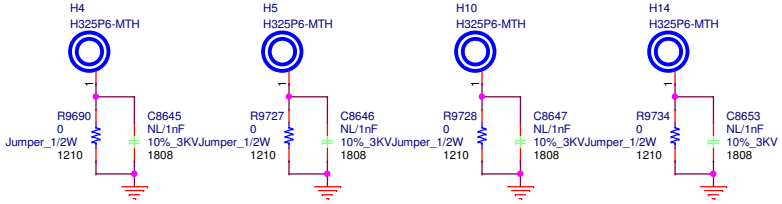
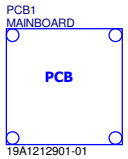
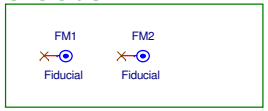
Other BOM



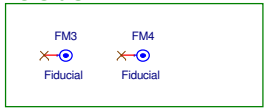


19A1212901-01
PCB PCE-2129 A101-2 L:8 C:G 1.6MM FR4

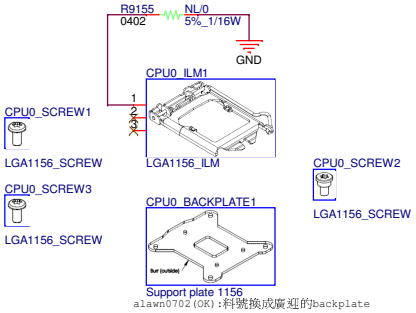
CPU side



IO side

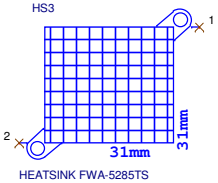


ILM + BP



alawn0702(OK):料號換成廣延的backplate

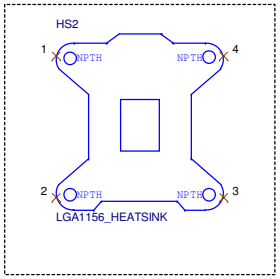
PCH Heatsink



HEATSINK FWA-5285TS

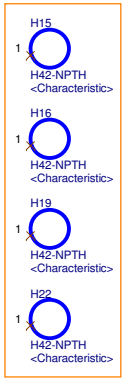
ILM + BP KEEP OUT ZONE

LGA1156_HEATSINK



Place to bottom side
For component keep used.

A101-1
Add



	CPU	ME	Lan Chip	PCH
96912029000	Intel Skylake-S Desktop CPU i7-6700, 3.4GHz, 8M, 65W ; i7-6700TE , 2.4GHz, 8M, 35W i5-6500, 3.2GHz, 6M, 65W; i5-6500TE, 2.3GHz, 6M, 35W i3-6100, 2.7GHz, 4M, 35W; i3-6100TE, 2.7GHz, 4M, 35W G4400TE, 2.9GHz, 3M, 35W G3900TE, 2.6GHz, 2M, 35W Intel Kabylake-S Desktop CPU i7-7700, 3.6 GHz, 8 MB, 65W ; i7-7700T, 2.9 GHz, 8 MB, 35W ; i5-7500, 3.4 GHz, 6 MB, 65W ; i5-7500T, 2.7 GHz, 6 MB, 35W ; i3-7101E, 3.9 GHz, 3 MB, 65W; i3-7101TE, 3.4 GHz, 3 MB, 35W;	Consumer	I219-V 1410026041-01	H110
96912129000		Corporate	I219-LM(v-Pro) 1410025503-01	Q170
96912129100	PCE-2129 With DVI			

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Title	61_Other BOM	
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History

ECOP-134766 A101-1 PCB: 19A1212900-01 (8 Layer) RD: WesleyYu.Su 2018/07/02
1. First Release

ECOP-137130 A101-2 PCB: 19A6S52001 (8 Layer) RD: WesleyYu.Su 2018/11/30
1. PCB: Change PCB P/N from 19A1212900-01 to 19A1212901-01 -->Modify to A101-2 version
2. SIO: Change R9033 from NL to 1k for GPIO -->Add R9033上件
3. PWR: Remove C7521 for SIO_RSMRST# AT power down glitch -->There is a glitch at SIO_RSMRST# when system power off
4. PWR: Add a resistor 0ohm R9786 series R9774 for power rail +V0.95_VCCIO -->reserve R9786 for +V0.95_VCCIO adjust
5. SATA: Modify SATA_PCH_LED# signal for inverse issue. -->PCH SATA_PCH_LED# sink current only 3mA ; so add a MOS
6. mPCIE: NUT1 and NUT2 change to 1910004105 for mPCIE鎖上高度問題 -->原上件太高
7. +VCORE_EN: R8747 change to PH +V12_SB for suprise power down +VCORE_EN spike -->There is a glitch at +VCORE_EN when system surprise power down.
8. N331270422 : R8748 change to PH +V12_SB for suprise power down N331270422 spike -->There is a glitch at N331270422 when system surprise power down.
9. PCH_SLP_S3#: R8496 change to 10k and Pull High to +V12_SB for PCH_SLP_S3# power on spike -->There is a glitch at PCH_SLP_S3# when system surprise power down.
10. PCH_SYSPWROK: R8753 change to PH +V12_SB for suprise power down PCH_SYSPWROK spike -->There is a glitch at PCH_SYSPWROK when system surprise power down.
11. Jumper: Jumper 1653302122 change to 1653005287-01 for DFM Jumper for DFM High Light -->Change Jumper
12. +V1.2_DDR_EN: R8494 change Pull High to +V12_SB for power on/off +V1.2_DDR_EN glitch -->There is a glitch at +V1.2_DDR_EN when system surprise power down.
13. mSATA: Reserve R9789 for mSATA and mPCIE SW strap from FITC -->Reserve R9789 for match FITC HSIO
14. IMVP8: Add IMVP8 firmware to U57 for 1420045642 -->Update Firmware
15. Isolation: C7828、C8013、C7996、C8044 set to NL and R8809、R8935、R8928 、R8942 set to pop -->將隔離電容移除上ohm for EMI
16. LAN1_USB2C1_1: Adjust Lan LAN1_USB2C1_1 for reverse -->Lan 1 reverse change
17. D type Flipflop: Add C8707 C8708 C8709 C8710 R9790 R9791 R9792 R9793 R9794 U162 U163 for D type flip flop as Product spec watch dog light
 -->New spec for Watch dog use D type flipflop"
18. SMI#: Add R9796 0 ohm for PCH SMI# and connect to OVT_LED#_SIO at Super I/O -->Connect Super I/O SMI# to Host
19. Delay IC: Change U133 from 1410001299 to 1410023343-01 for Steve suggestion -->(other project on/off issue)
20. JFP1: JFP1 change from 4 pin to 5 pin for clear D type flip flop at WDT assert reset. -->For WDT LED reset
21. PROCHOT#: R7755 change from 75 ohm to 1k for prochot# pull to low level. -->Follow PDG and change PH to 1k
22. Phase out: Change L136 from 1211003965 to 1211006026-01 for compoent phase out CMC suggestion -->Componet phase out and follow CMC suggestion
23. Phase out: Change Q840,Q835 from 1310004697-01 to 1310006283-01 for phase out issue CMC suggestion (2n7002) -->Componet phase out and follow CMC suggestion
24. Phase out: Change U148,U135 from 1410023435-01 to 1410028464-01 for phase out issue ANPEC eFuse -->Componet phase out and follow CMC suggestion
25. EXAR_XR34350ILTR: Reserve R9798 R9799 R9800 R9801 for fail safe -->Reserve resistor
26. OVT_LED# : Reserve R9802 and connect to OVT_LED# for CPU_TEMP_ALERM# -->Reserve resistor
27. CPU_TEMP_ALERM: Add R9803 for CPU_TEMP_ALERM#(R9802 either one) -->Reserve resistor ; back up use prochot
28. WDT_ASSERTED# : Reserve R9804 for WDT_ASSERTED# from Super IO -->Reserve resistor
29. DVI: Change B174 connection for DVI power to device -->When DVI is on and use eFUSE. So change connection

ECOP-139010 A101-2 PCB: 19A1212901-01 (8 Layer) RD: WesleyYu.Su 2018/11/30
30. LED(ECOP-139010): R9794 change from 10k to 20k ohm ; C8710 change from 0.1uf to 2.2uf(1100009083) -->WDT LED keep on when boot
31. Wifi(ECOP-139010): R8648=10k ohm ; remove R8645 -->R8648上件 for EWM-W151h SSID issue , MINIPCIE2_DIS# keep low change from BIOS control to HW control
32. Jumper(ECOP-140219): Update PCE-2129/2029 BOM jumper Name from JCOMS1(1-2)1 to JCMOS1(1-2)1 -->DFM request modify jumper Name from JCOMS1(1-2)1 to JCMOS1(1-2)1
33. Lan Firmware: Delete 2080007727 on IMG-1
Change 1410024453-01 to 1420046765 on U143 -- -->For 工廠需求更新刪除２０８階and Add 142 for LAN"
34. 收斂2N7002(ECOP-139958): Change 1315700214 to 1310006408-01*28 on All -->for 收斂2n7002
35. 缺料(ECOP-139958): Change 1310004127 to 1310005750-01*1 on Q736 --> ｆｏｒ 缺料問題
36. SMI(ECOP-140166): Delete 105A700004*1 on R9796 -->Remove R9796 to disconnect reserve circuit of PCH_SMI# and OVT_LED#_SIO
37. ACPRESENT: Add R8598 at 105A50103A 10k -->for Scar Wake up for I219

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