AIIS-5410P Schematic

Version:	A101-4	PCB P/N:	19A1541003-01	Update Date:	2016/1/25

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Title	01_ Index	
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AIIS-5410P Block Diagram

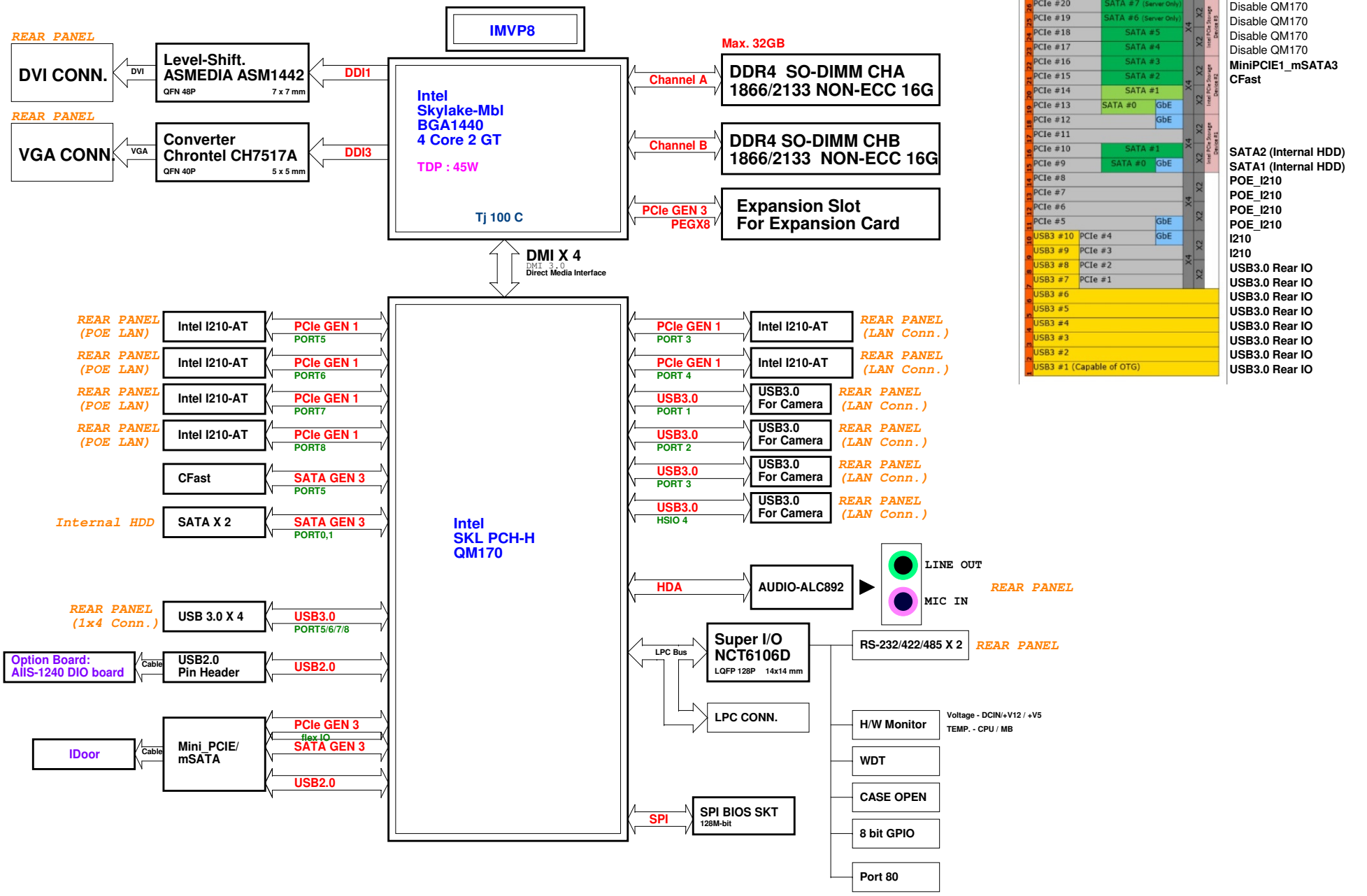

Figure 3-1. HSIO Muxing on SKL PCH-H

Disable QM170
Disable QM170
Disable QM170
Disable QM170
MiniPCIE1_mSATA3
CFast

SATA2 (Internal HDD)
SATA1 (Internal HDD)
POE_I210
POE_I210
POE_I210
POE_I210
I210
I210
USB3.0 Rear IO
USB3.0 Rear IO
USB3.0 Rear IO
USB3.0 Rear IO
USB3.0 Rear IO
USB3.0 Rear IO
USB3.0 Rear IO
USB3.0 Rear IO

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Title	02_Block Diagram		
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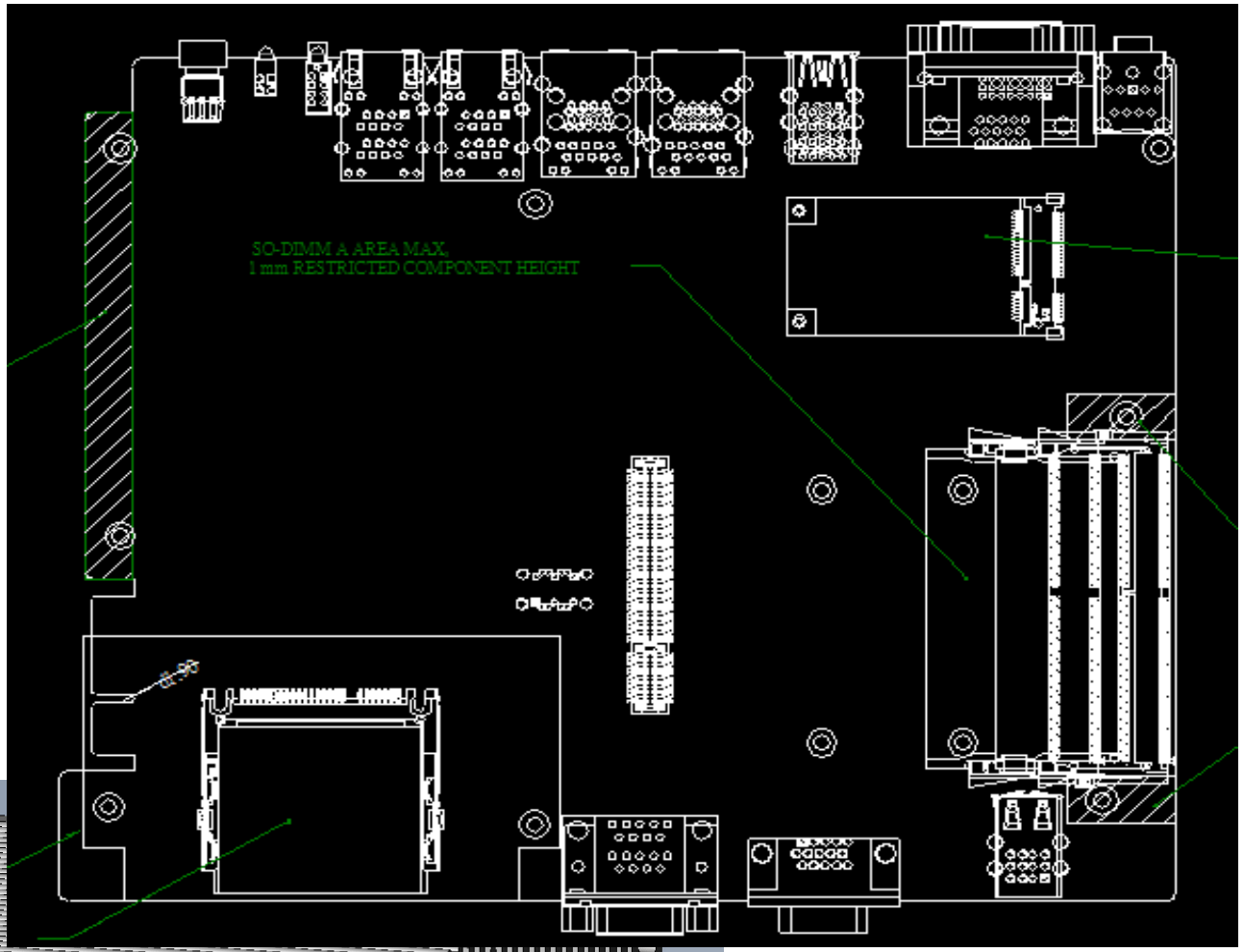
AIIS-5410P
System & Rear I/O



waynel105: update picture

ADVANTECH			
Title	03_Panel outline		
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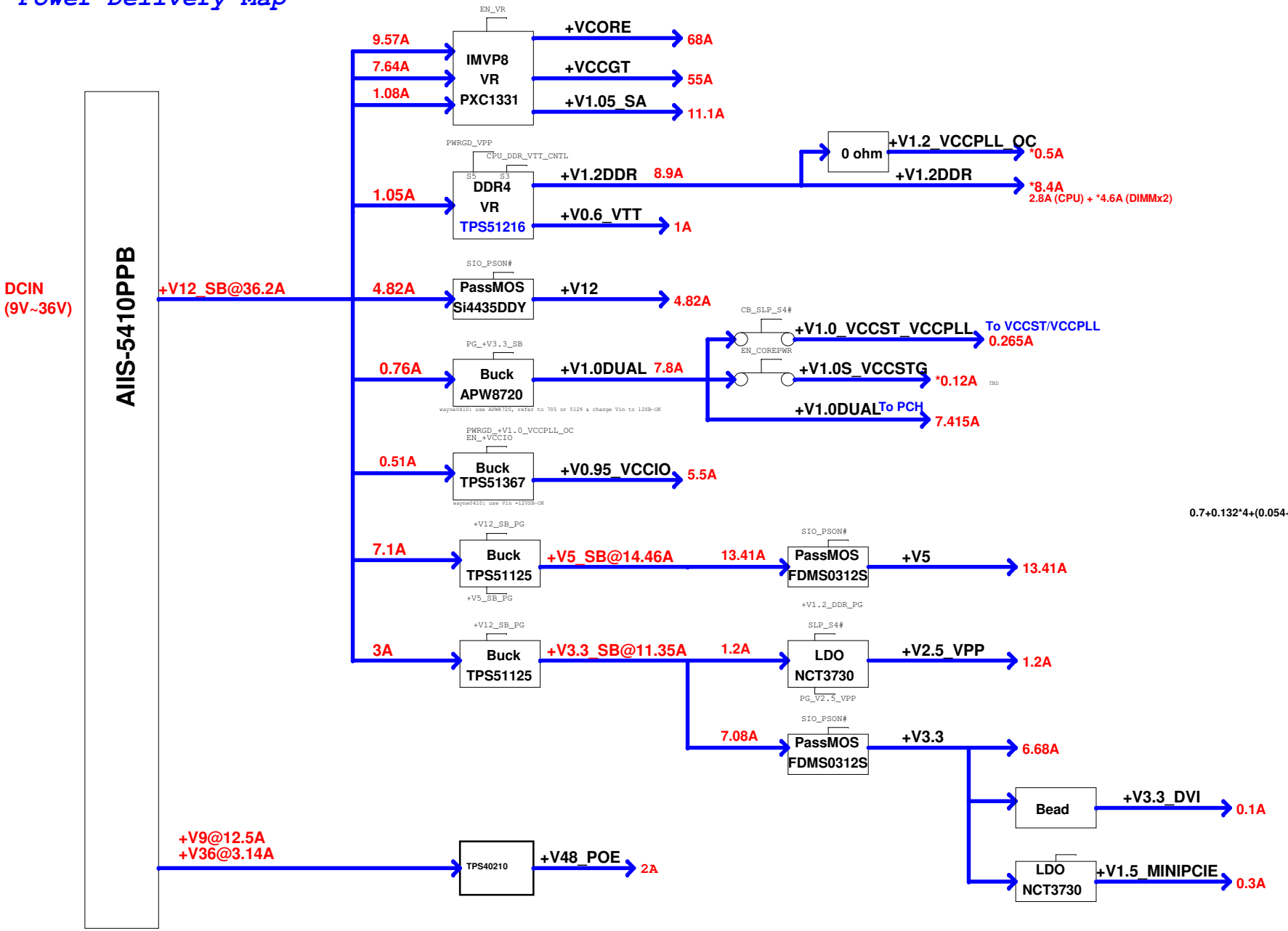
Power Delivery Map



Skylake BGA1440 42e 45W

+VCC_CPU: VCC	68A
+VGT_CPU: VccGT	55A
+VGTU_CPU: VccGTX	NA
+VSA_CPU: VccSA	11.1A
+V0.95_VCCIO: VccIO	5.5A
+V1.0S_VCCST: VccST	0.12A
+V1.0S_VCCST: VccPLL	0.145A
+V1.0S_VCCSTG: VccSTG	0.12A
+V1.2S_VCCPLLOC: VccPLL_OC	0.5A
+V1.2DDR: VDDQ	2.8A
+V1.05_OPC: VccOPC	NA
+V1.8S: VccOPC_1P8	NA
+V1.1_0.85_EOPIO: VccEOPIO	NA

DDR4 SO-UDIMM x2

+V1.2DDR: VDDQ	4.6A*
+V2.5_VPP: VPP	*2A
+V0.6_VTT: VTT	*1A

PCH

VCCPRIM_1p0	2.899A
VCCCLK1	0.021A
VCCCLK2	0.137A
VCCCLK3	0.05A
VCCCLK4	0.024A
VCCCLK5	0.006A
VCCMPHY_1p0	2.698A
VCCHDAPLL_1p0	0.033A
VCCAMPHYPLL_1p0	0.08A
VCCAPLLEBB_1p0	0.03A
VCCMIPIPLL_1p0	0.03A
VCCUSB2PLL_1p0	0.012A
+V1.0DUAL	6.02A
VCCPGPPA	0.082A
VCCPGPPBCH	0.229A
VCCPGPPD	0.078A
VCCPGPPEF	0.114A
VCCPGPPG	0.065A
VCCSPI	0.029A
VCCATS	0.07A
VCCHDA	0.06A
VCCPRIM_3p3	0.117A
VCCDSW_3p3	0.195A
VCCRTCPRIM_3p3	0.001A
VCCRTC	0.001A
+V3.3A	1.059A

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Title: 04_Power Delivery Map

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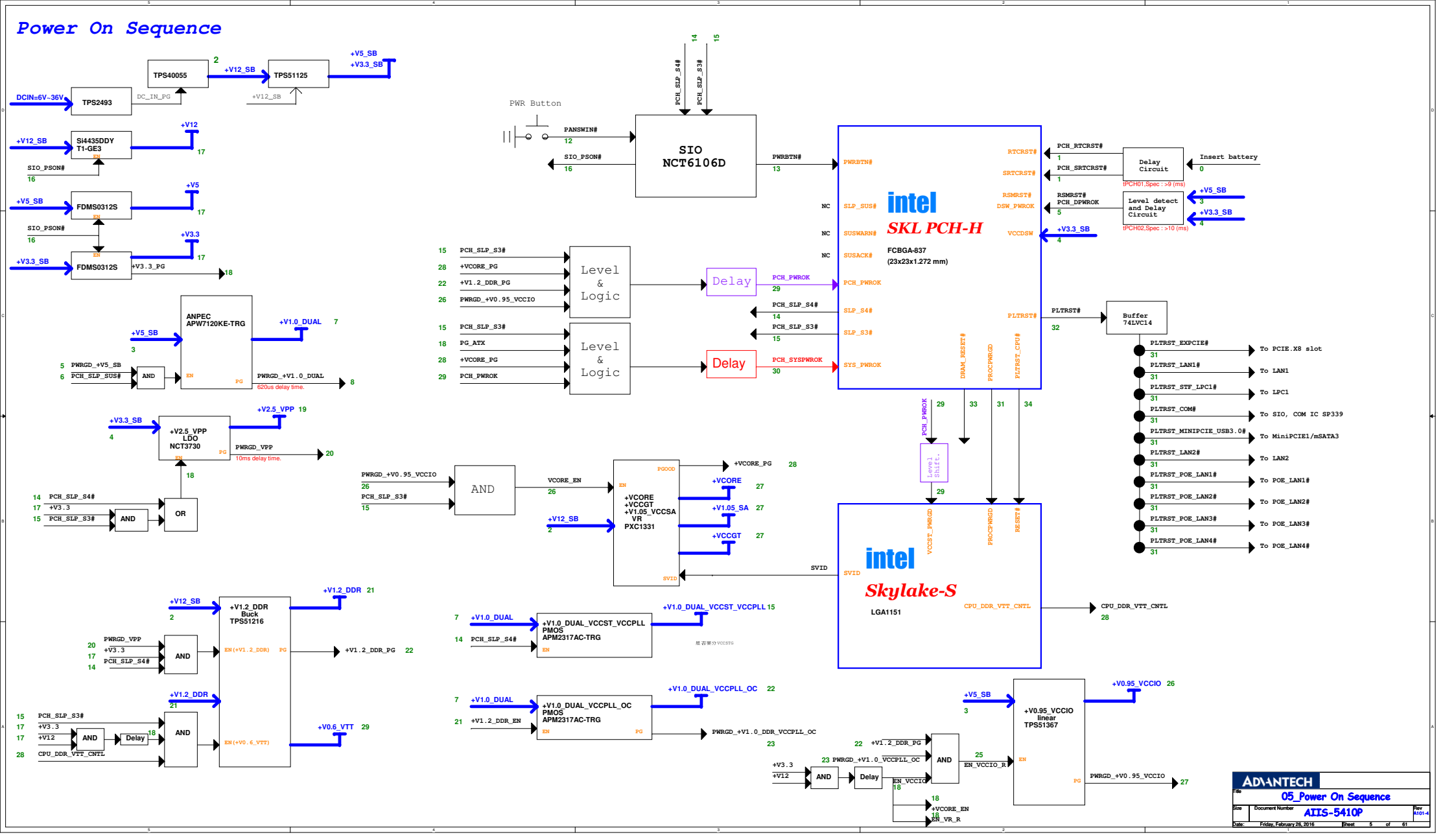
Power On Sequence



Title	05_Power On Sequence
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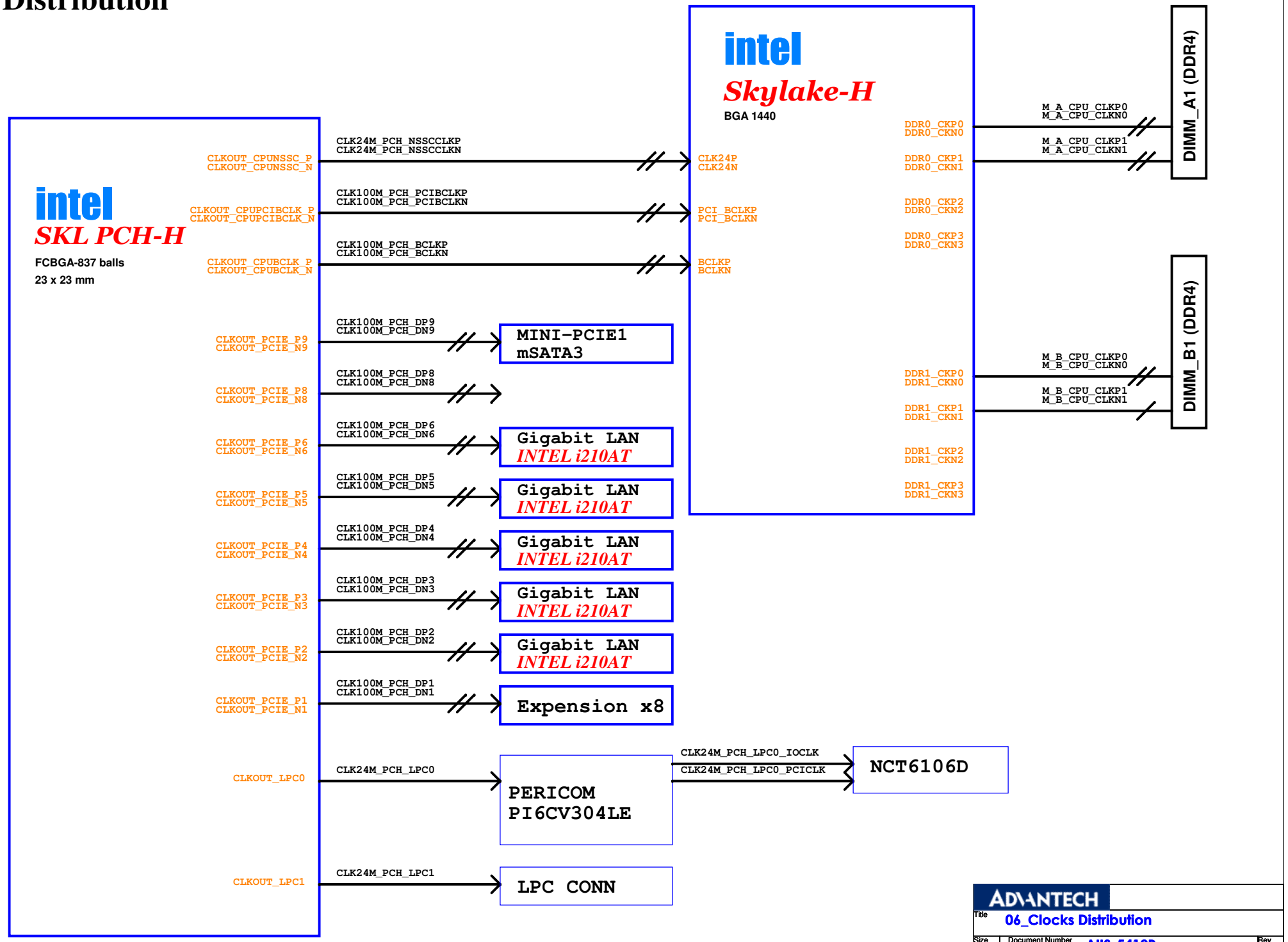
Clock Distribution



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Title	06_Clocks Distribution	
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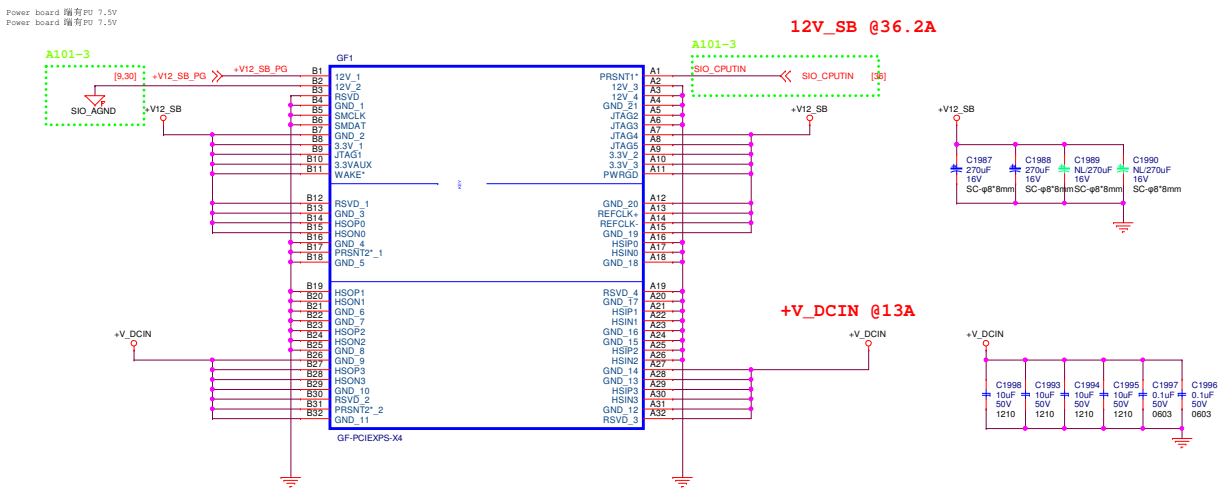
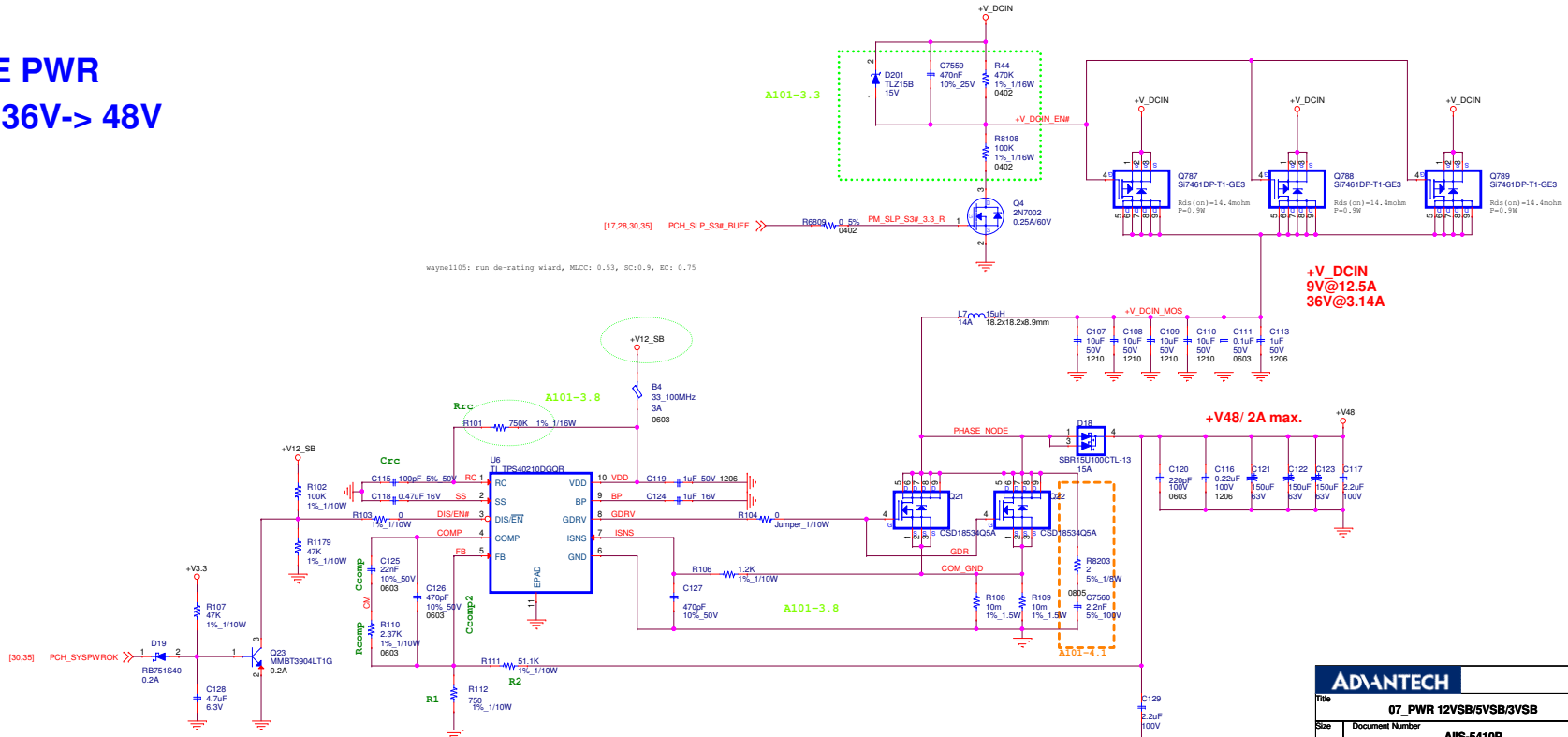
PWR +V_DCIN/+V12_SB/+V5_SB/+V3.3_SB



wayne1105: update picture

x4 PCIe Connector B			
AB01	PWROK	DCIN_IMON	AA01
AB02	DCIN_PG	GND	AA02
AB03	GND	GND	AA03
AB04	GND	GND	AA04
AB05	GND	GND	AA05
AB06	GND	GND	AA06
AB07	+12V_SB	+12V_SB	AA07
AB08	+12V_SB	+12V_SB	AA08
AB09	+12V_SB	+12V_SB	AA09
AB10	+12V_SB	+12V_SB	AA10
AB11	+12V_SB	+12V_SB	AA11
Mechanical Key			
AB12	+12V_SB	+12V_SB	AA12
AB13	+12V_SB	+12V_SB	AA13
AB14	+12V_SB	+12V_SB	AA14
AB15	+12V_SB	+12V_SB	AA15
AB16	GND	GND	AA16
AB17	GND	GND	AA17
AB18	GND	GND	AA18
AB19	GND	GND	AA19
AB20	GND	GND	AA20
AB21	GND	GND	AA21
AB22	GND	GND	AA22
AB23	GND	GND	AA23
AB24	GND	GND	AA24
AB25	GND	GND	AA25
AB26	+V_DCIN	GND	AA26
AB27	+V_DCIN	+V_DCIN	AA27
AB28	+V_DCIN	+V_DCIN	AA28
AB29	+V_DCIN	+V_DCIN	AA29
AB30	+V_DCIN	+V_DCIN	AA30
AB31	+V_DCIN	+V_DCIN	AA31
AB32	+V_DCIN	+V_DCIN	AA32

POE PWR
9V~36V-> 48V



ADVANTECH

Title	07_PWR 12VSB/5VSB/3VSB	
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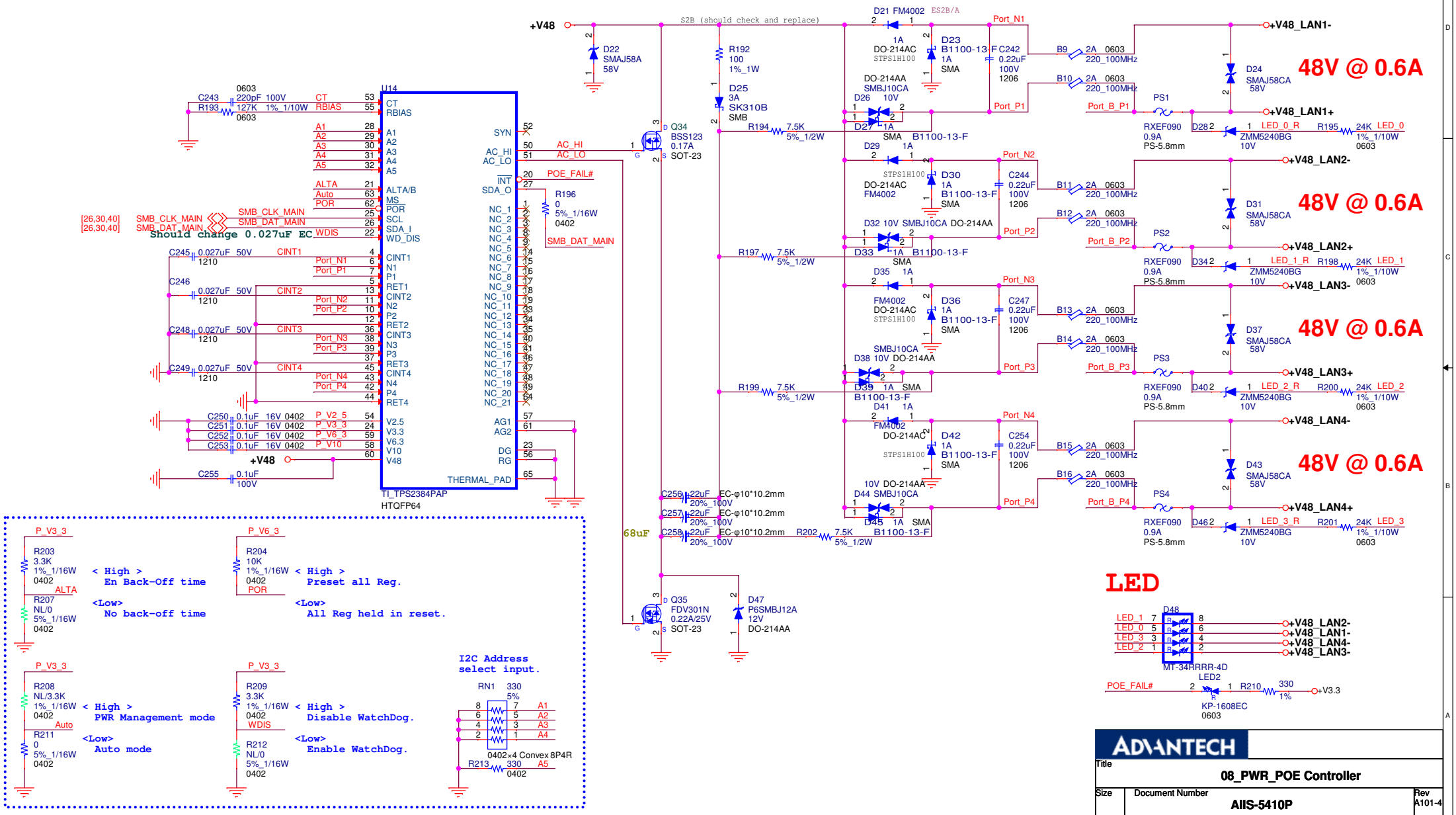
POE CONTROLLER (PSE)



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Title	08_PWR_POE Controller
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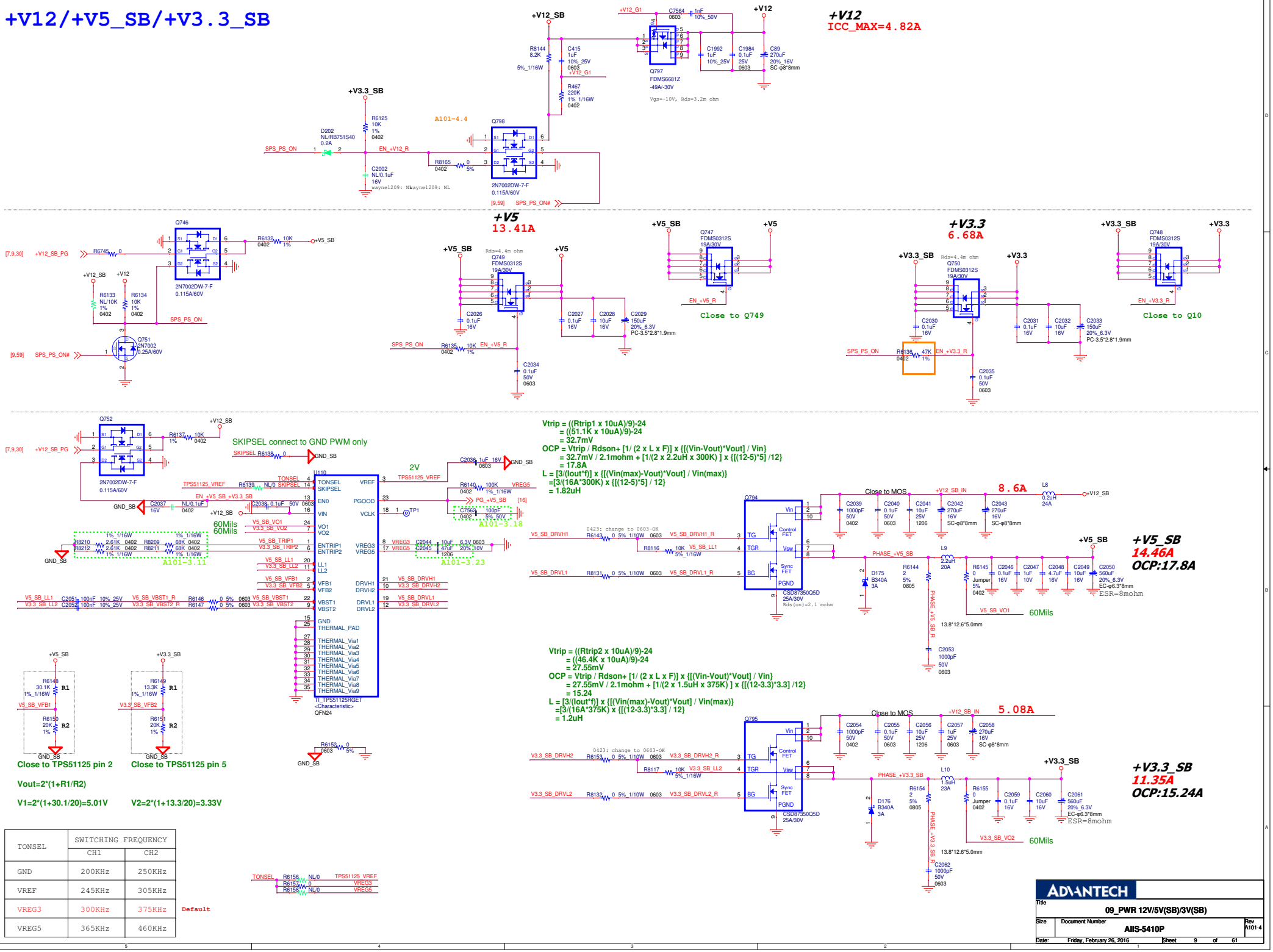
+V12/+V5_SB/+V3.3_SB



TONSEL	SWITCHING FREQUENCY	
	CH1	CH2
GND	200KHz	250KHz
VREF	245KHz	305KHz
VREG3	300KHz	375KHz
VREG5	365KHz	460KHz

Default

ADVANTECH

Title	09_PWR 12V/5V(SB)/3V(SB)	
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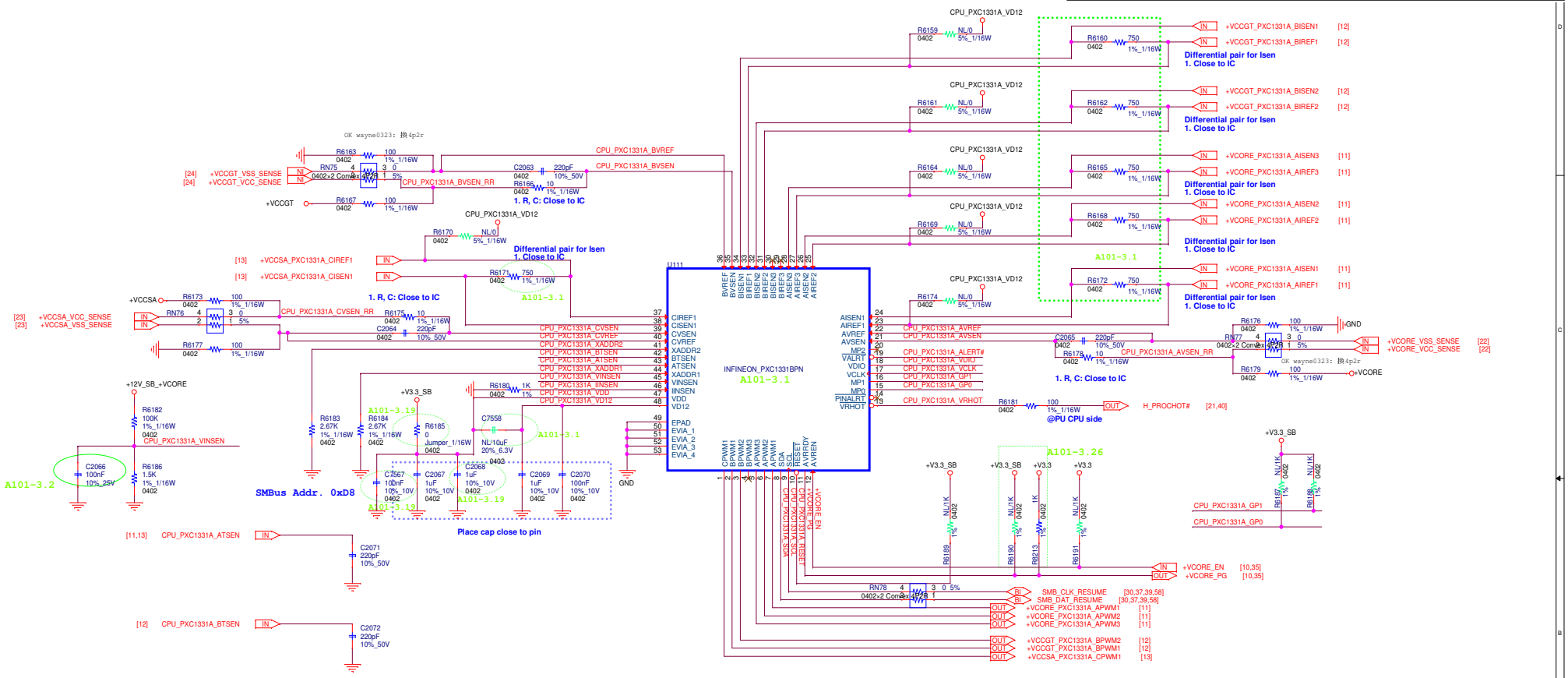
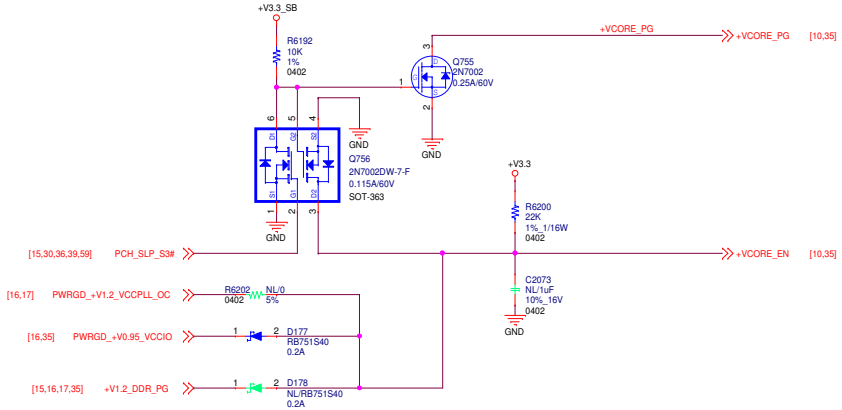
PWR [VCORE+VSA PWM IC]

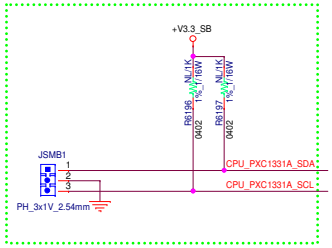
+VCORE Iomax=68A
+VCCSA Iomax=11.1A
+VCCGT Iomax=55A

Resistor-to-GND (1%)	XADDR2							
	2.26 kΩ	2.67 kΩ	3.16 kΩ	4.02 kΩ	5.36 kΩ	8.06 kΩ	16.0 kΩ	Open
XADDR1 2.26 kΩ	FC	DC	BC	9C	7C	5C	3C	1C
XADDR1 2.67 kΩ	F8	D8	B8	98	78	58	38	reserved
XADDR1 3.16 kΩ	F4	D4	B4	94	74	54	34	14
XADDR1 4.02 kΩ	F0	D0	B0	90	70	50	30	10
XADDR1 5.36 kΩ	EC	CC	AC	8C	6C	4C	2C	0C
XADDR1 8.06 kΩ	E8	C8	A8	88	68	48	28	08
XADDR1 16.0 kΩ	E4	C4	A4	84	64	44	24	04
XADDR1 Open	E0	C0	A0	80	60	40	20	reserved

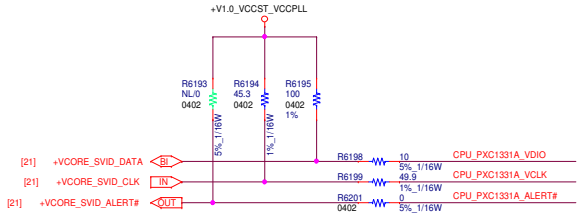


VR_ENABLE





For program purpose



Routing: Need to follow intel criteria.

ADVANTECH			
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PWR [VCORE_Phase1-3]

+VCORE Iomax=68A

+V12_VIN_+VCORE@18.29A

+V12_SB

+12V_SB_+VCORE

L11 0.2uH 24A 7.3x6.6x3mm

C2074 10uF 10%_25V 0805 GND
C2075 10uF 10%_25V 0805 GND
C2076 270uF 16V SC-φ8*8mm GND
C2077 270uF 16V SC-φ8*8mm

lin= 3.2A

+12V_SB_+VCORE

C2081 220nF 10%_16V
C2082 1uF 10%_10V 0402
R6203 0402 1 1%_1/16W
C2083 1uF 10%_10V 0402
+VCORE_TDA21321_1_VCIN

+V5

C2078 220nF 10%_25V 0603
C2079 10uF 10%_25V 0805
C2080 10uF 10%_25V 0805
A101-1 1206 => 0805
OK wayne0316: change part

U112

[10] +VCORE_PXC1331A_APWM1 IN → PWM
[10,11,13] CPU_PXC1331A_ATSEN OUT
R6204 0402 5% 1/16W 0
Fit wayne0323: 確認是否可移除
debug減溫保護會用到
+VCORE_TDA21321_1_TMON → TMON/FAULT
+VCORE_TDA21321_1_IMONREF → IMONREF
+VCORE_TDA21321_1_BOOT → BOOT
+VCORE_TDA21321_1_PHASE → PHASE
OFF
IMON
INFINEON_TDA21321
<Characteristic>
A101-3.1
A101-1
0603 -> 0402
R6205 0 Jumper_1/16W 0402
C2088 100nF 10%_25V 0402
[10] +VCORE_PXC1331A_AIREF1 OUT
[10] +VCORE_PXC1331A_AISEN1 OUT
C2089 10pF 5%_50V

+12V_SB_+VCORE

+VCORE_TDA21321_1_SW

L12 150nH 55A

Idc=55A, Isat=64A, DCR=0.19mohm

+VCORE

A101-1
820uF EC- φ 6.3*8mm => 470uF PC-7.3*4.3*1.9mm
ESR=7mohm => ESR=4.5mohm

C2084 470uF 20%_2V PC-7.3*4.3*1.9mm ESR=4.5mohm
C2085 22uF 20%_4V 0805
C2086 22uF 20%_4V 0805
C2087 22uF 20%_4V 0805
A101-1 6.3V => 4V
OK wayne0316: change part

+Vcore 22.6A

0423: add 470uf-OK

+12V_SB_+VCORE

C7574 10uF 10%_25V 0805
C7575 10uF 10%_25V 0805
C7576 10uF 10%_25V 0805
C7577 10uF 10%_25V 0805
C7578 10uF 10%_25V 0805
C7579 10uF 10%_25V 0805
C7580 10uF 10%_25V 0805
C7581 10uF 10%_25V 0805

+12V_SB_+VCORE

C7569 10uF 10%_25V 0805
C7570 1uF 10%_25V 0603
C7568 100nF 10%_25V 0402

A101-3

+VCORE

C2090 470uF 20%_2V PC-7.3*4.3*1.9mm

lin= 3.2A

+12V_SB_+VCORE

C2094 220nF 10%_16V
C2095 1uF 10%_10V 0402
R6206 0402 1 1%_1/16W
C2096 1uF 10%_10V 0402
+VCORE_TDA21321_2_VCIN

+V5

C2091 220nF 10%_25V 0603
C2092 10uF 10%_25V 0805
C2093 10uF 10%_25V 0805
A101-1 1206 => 0805

U113

[10] +VCORE_PXC1331A_APWM2 IN → PWM
[10,11,13] CPU_PXC1331A_ATSEN OUT
R6207 0402 5% 1/16W 0
Fit wayne0323: 確認是否可移除
debug減溫保護會用到
+VCORE_TDA21321_2_TMON → TMON/FAULT
+VCORE_TDA21321_2_IMONREF → IMONREF
+VCORE_TDA21321_2_BOOT → BOOT
+VCORE_TDA21321_2_PHASE → PHASE
OFF
IMON
INFINEON_TDA21321
<Characteristic>
A101-3.1
A101-1
0603 -> 0402
R6208 0 Jumper_1/16W 0402
C2100 100nF 10%_25V 0402
[10] +VCORE_PXC1331A_AIREF2 OUT
[10] +VCORE_PXC1331A_AISEN2 OUT
C2101 10pF 5%_50V

+12V_SB_+VCORE

+VCORE_TDA21321_2_SW

L13 150nH 55A

Idc=55A, Isat=64A, DCR=0.19mohm

+VCORE

A101-1
820uF EC- φ 6.3*8mm => 470uF PC-7.3*4.3*1.9mm
ESR=7mohm => ESR=4.5mohm

C2097 470uF 20%_2V PC-7.3*4.3*1.9mm ESR=4.5mohm
C2098 22uF 20%_4V 0805
C2099 22uF 20%_4V 0805
A101-1 6.3V => 4V
OK wayne0316: change part
OK wayne0316: 2V以下用4V 22uf
OK wayne0316: 2V以下用4V 22uf

+Vcore 22.6A

lin= 3.2A

+12V_SB_+VCORE

C2105 220nF 10%_16V
C2106 1uF 10%_10V 0402
R6209 0402 1 1%_1/16W
C2107 1uF 10%_10V 0402
+VCORE_TDA21321_3_VCIN

+V5

C2102 220nF 10%_25V 0603
C2103 10uF 10%_25V 0805
C2104 10uF 10%_25V 0805
A101-1 1206 => 0805
OK wayne0316: change part

U114

[10] +VCORE_PXC1331A_APWM3 IN → PWM
[10,11,13] CPU_PXC1331A_ATSEN OUT
R6210 0402 5% 1/16W 0
Fit wayne0323: 確認是否可移除
debug減溫保護會用到
+VCORE_TDA21321_3_TMON → TMON/FAULT
+VCORE_TDA21321_3_IMONREF → IMONREF
+VCORE_TDA21321_3_BOOT → BOOT
+VCORE_TDA21321_3_PHASE → PHASE
OFF
IMON
INFINEON_TDA21321
<Characteristic>
A101-3.1
A101-1
0603 -> 0402
R6211 0 Jumper_1/16W 0402
C2112 100nF 10%_25V 0402
[10] +VCORE_PXC1331A_AIREF3 OUT
[10] +VCORE_PXC1331A_AISEN3 OUT
C2113 10pF 5%_50V

+12V_SB_+VCORE

+VCORE_TDA21321_3_SW

L14 150nH 55A

Idc=55A, Isat=64A, DCR=0.19mohm

+VCORE

A101-1
820uF EC- φ 6.3*8mm => 470uF PC-7.3*4.3*1.9mm
ESR=7mohm => ESR=4.5mohm

C2108 470uF 20%_2V PC-7.3*4.3*1.9mm ESR=4.5mohm
C2109 22uF 20%_4V 0805
C2110 22uF 20%_4V 0805
C2111 22uF 20%_4V 0805
A101-1 6.3V => 4V
OK wayne0316: change part
OK wayne0316: 2V以下用4V 22uf
OK wayne0316: 2V以下用4V 22uf

+Vcore 22.6A

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Title	11_PWR +VCORE_Phase1-3	
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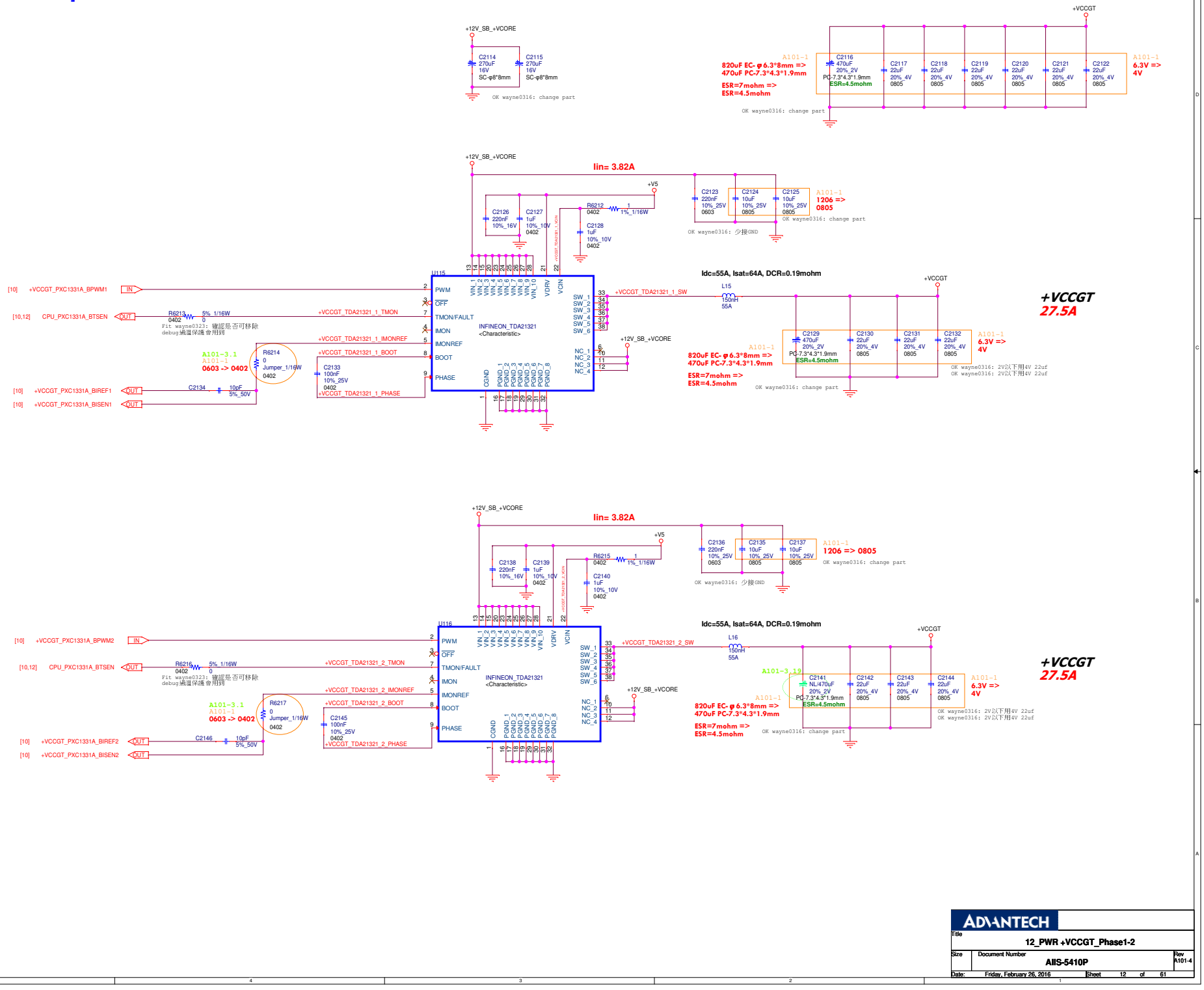
PWR [+VCCGT_Phase1-2]

+VCCGT Iomax=55A



Title	12_PWR +VCCGT_Phase1-2		
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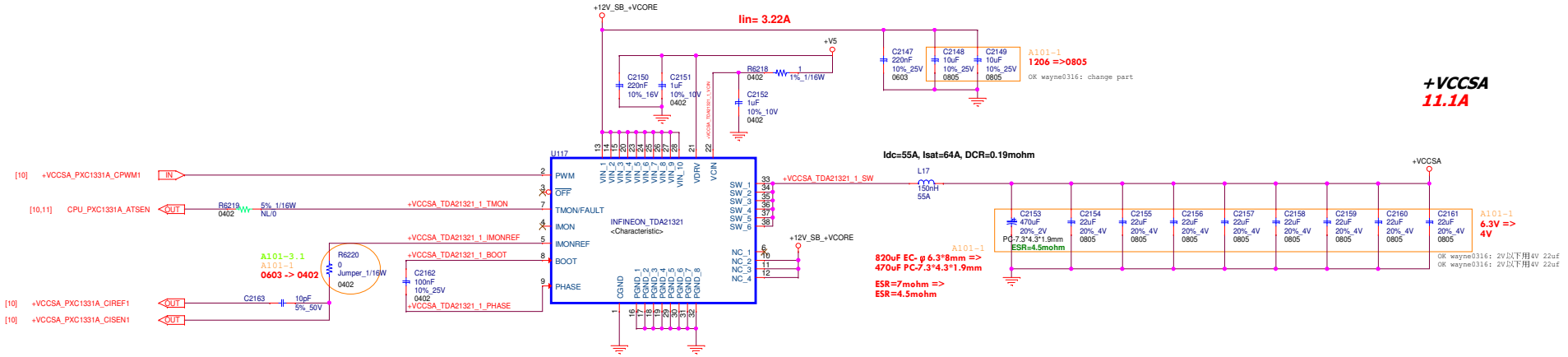
PWR [VSA_Phase1]

+V1.05_SA Iomax=11.1A



ADVANTECH			
Title	13_PWR +VCCSA		
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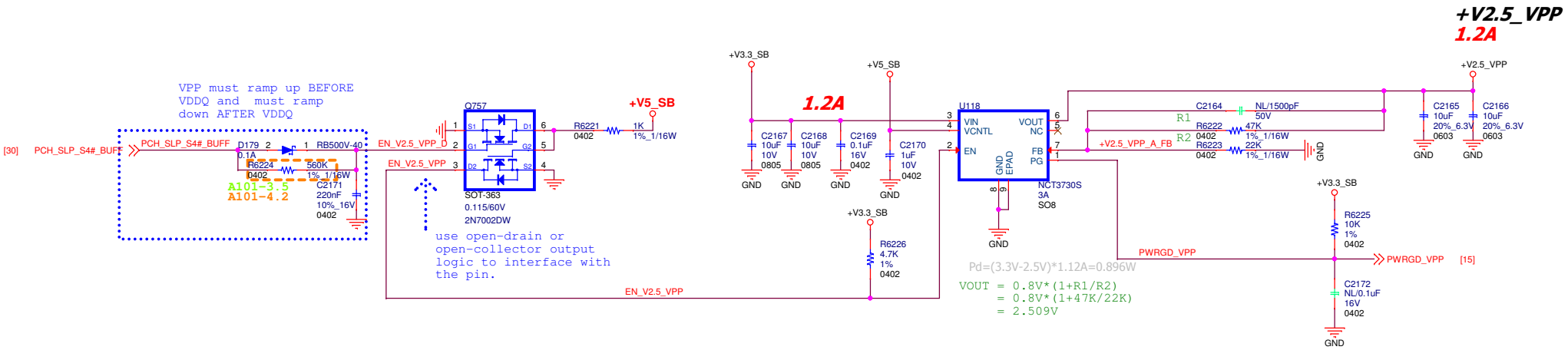
PWR [DDR_VPP CH-AB]



ADVANTECH

Title	14_PWR DDR4 +V2.5_VPP	
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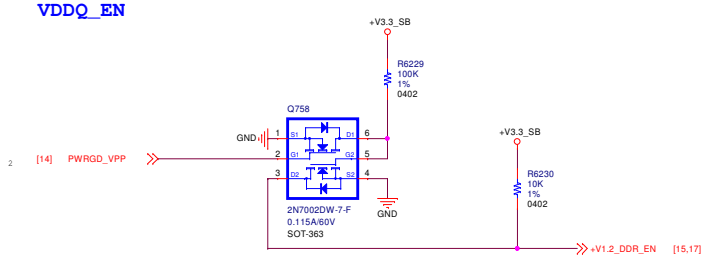
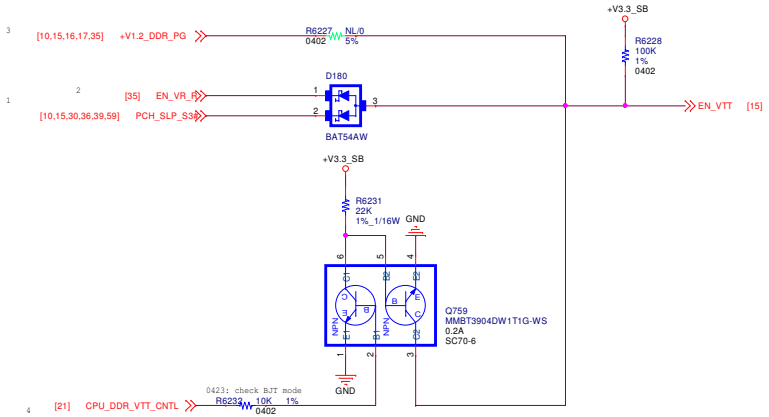
+V1.2_DDR/+V0.6_VTT

VDDQ_EN

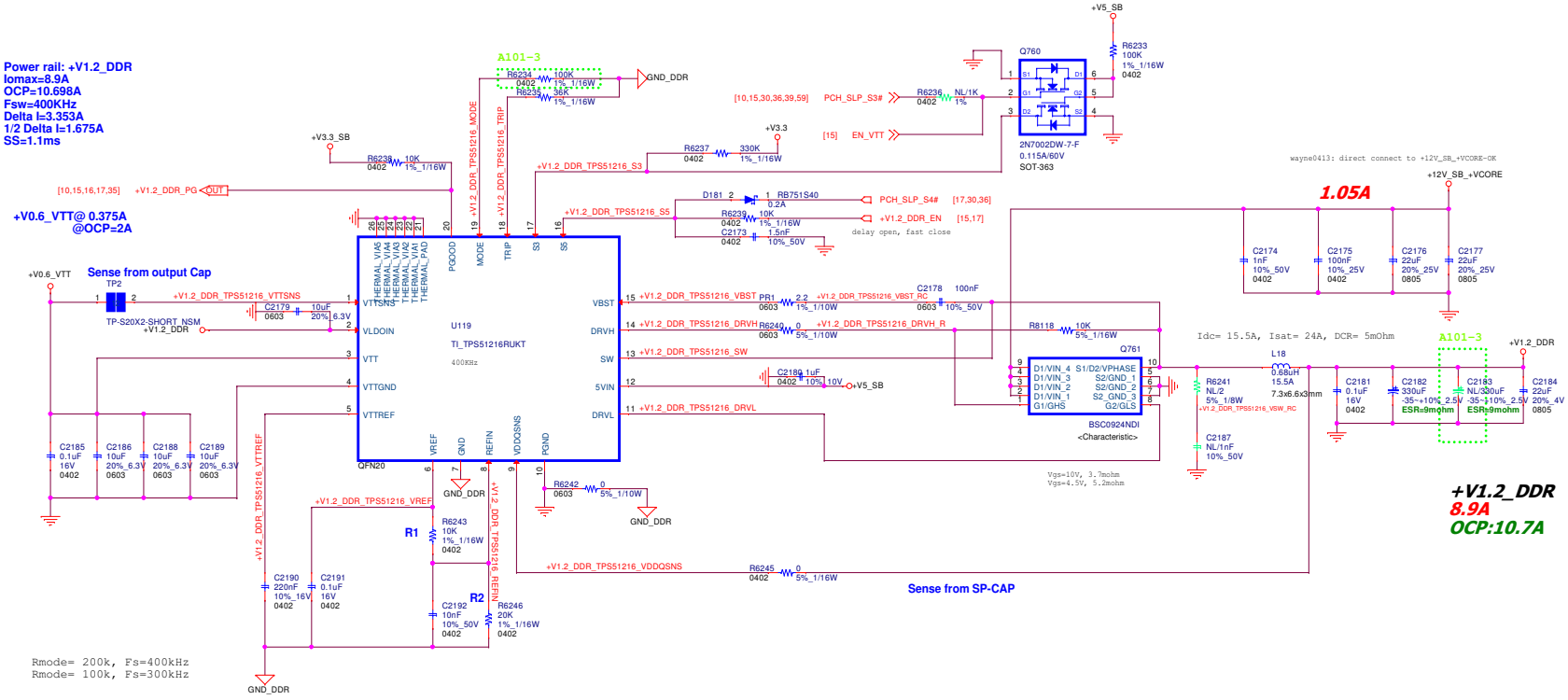


VTT_EN



Power rail: +V1.2_DDR
Iomax=8.9A
OCP=10.698A
Fsw=400KHz
Delta I=3.353A
1/2 Delta I=1.675A
SS=1.1ms

+V0.6_VTT@ 0.375A
@OCP=2A




```
Rmode= 200k, Fs=400kHz
Rmode= 100k, Fs=300kHz
```

```
Vtrip(mV) = Rtrip(Kohm) x 10uA = 36Kx10uA = 360mV
Iocl = Vtrip /8 x Rdson + Iripple/2
     = Vtrip / 8 x Rdson + (1/ (2 x L x f)) x ((Vin-Vout)xVout)/Vin
     = 360mV / 8 x 4.6mohm +  1.08
     ~= 10.86A
```

```
R2 = R1 / [(Vref / Vout) -1]
    = 10K / [(1.8 / 1.2) - 1]
    =20K
```

Table 2. MODE Selection

MODE NO.	RESISTANCE BETWEEN MODE AND GND (kΩ)	SWITCHING FREQUENCY (kHz)	DISCHARGE MODE
3	200	400	Tracking
2	100	300	
1	68	300	Non-tracking
0	47	400	

ADVANTECH

Title	15_PWR DDR4 +V1.2_DDR/+V0.6_VTT	
Size	Document Number: AIIS-5410P	Rev: A101-4
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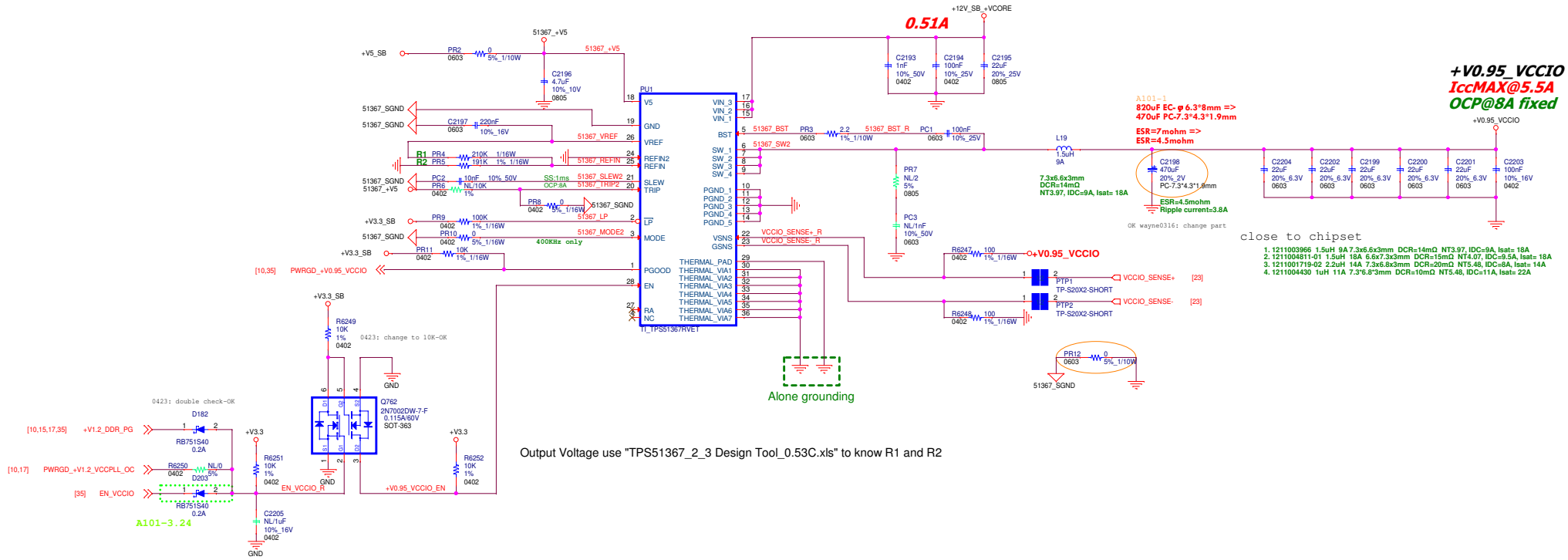
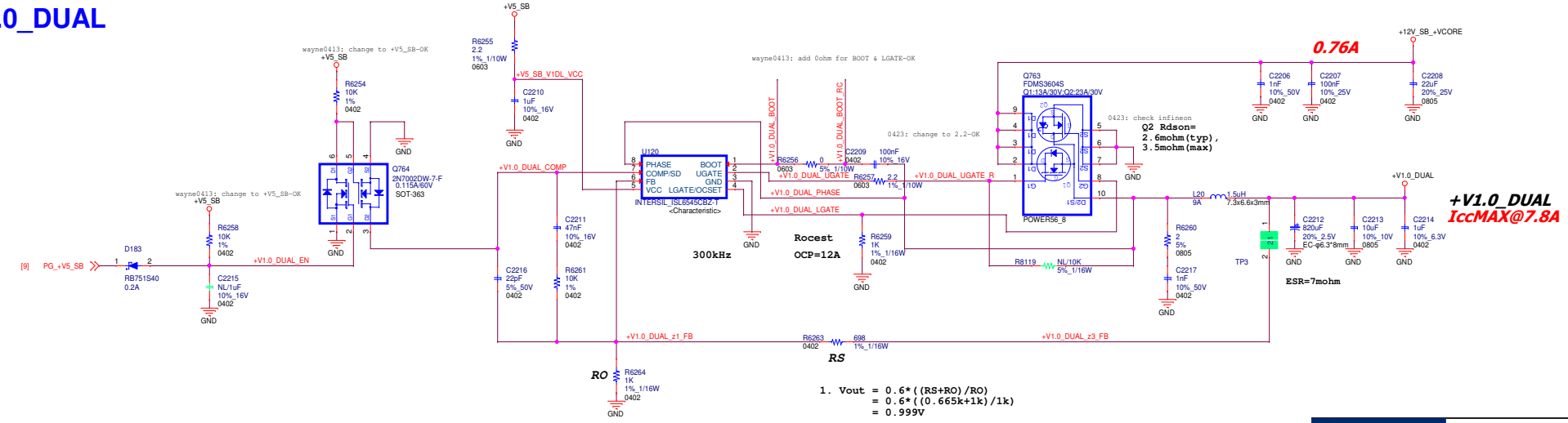
+V0.95_VCCIO



Output Voltage use "TPS51367_2_3 Design Tool_0.53C.xls" to know R1 and R2

+V1.0_DUAL



1. Vout = 0.6*((RS+RO)/RO)
= 0.6*((0.665k+1k)/1k)
= 0.999V

ADVANTECH			
Title	16_PWR +V1.0_DUAL/+V0.95_VCCIO		
Size	Document Number	AIIS-5410P	Rev A101-4
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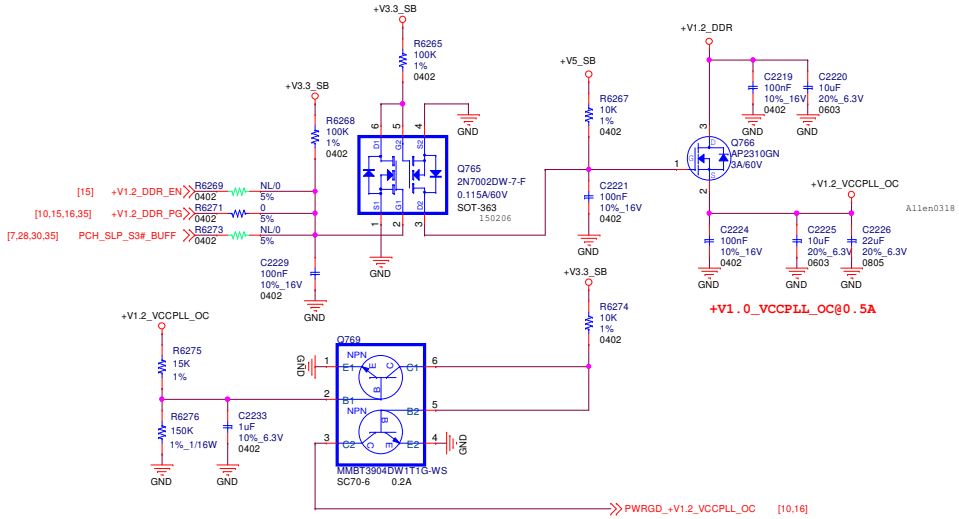
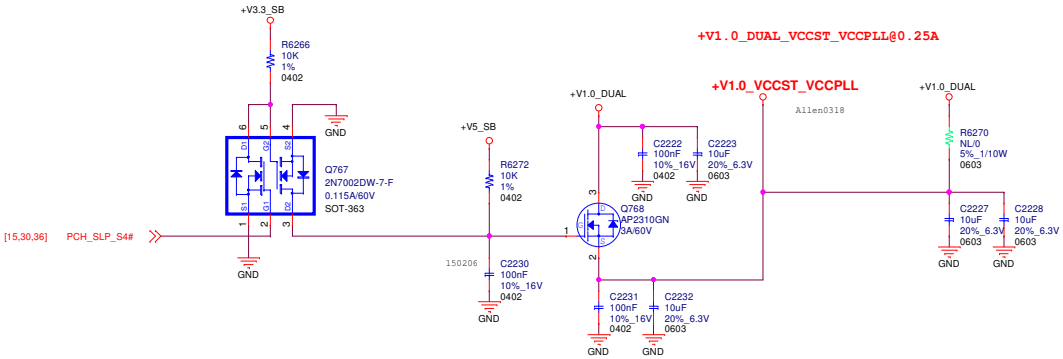
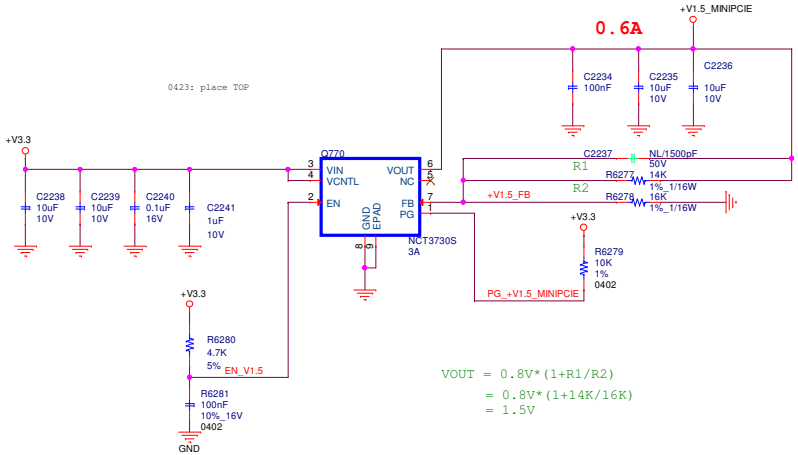
PWR [CPU_VCCPLL_OC]



PWR [CPU_VCCST_VCCPLL]



+V1.5_MINIPCIE



Title	17_PWR VCCST/+V1.5_MINIPCIE	
Size	Document Number: AIIS-5410P	Rev: A101-4
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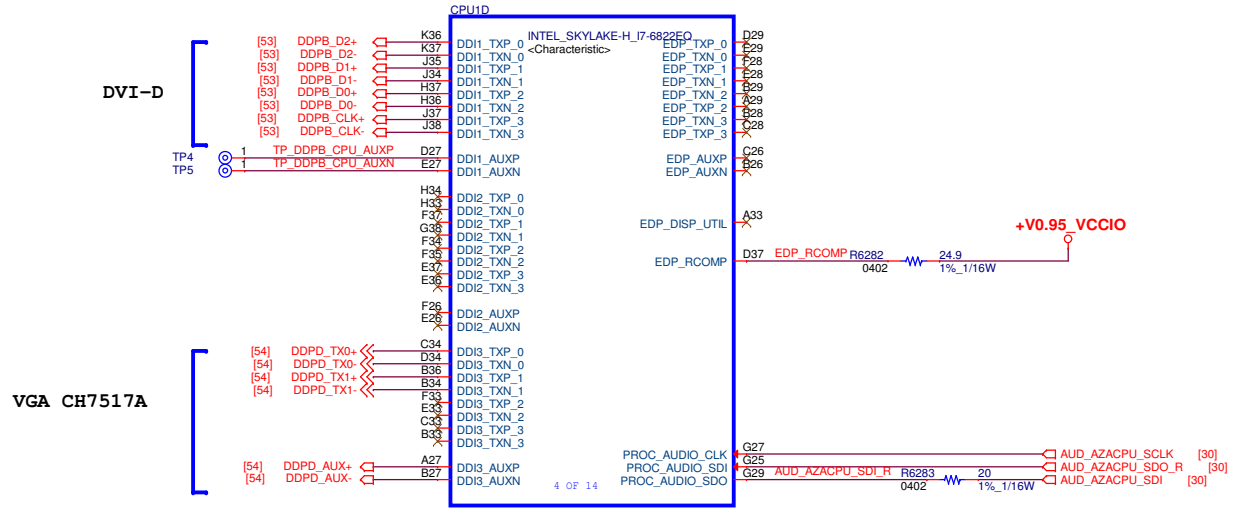
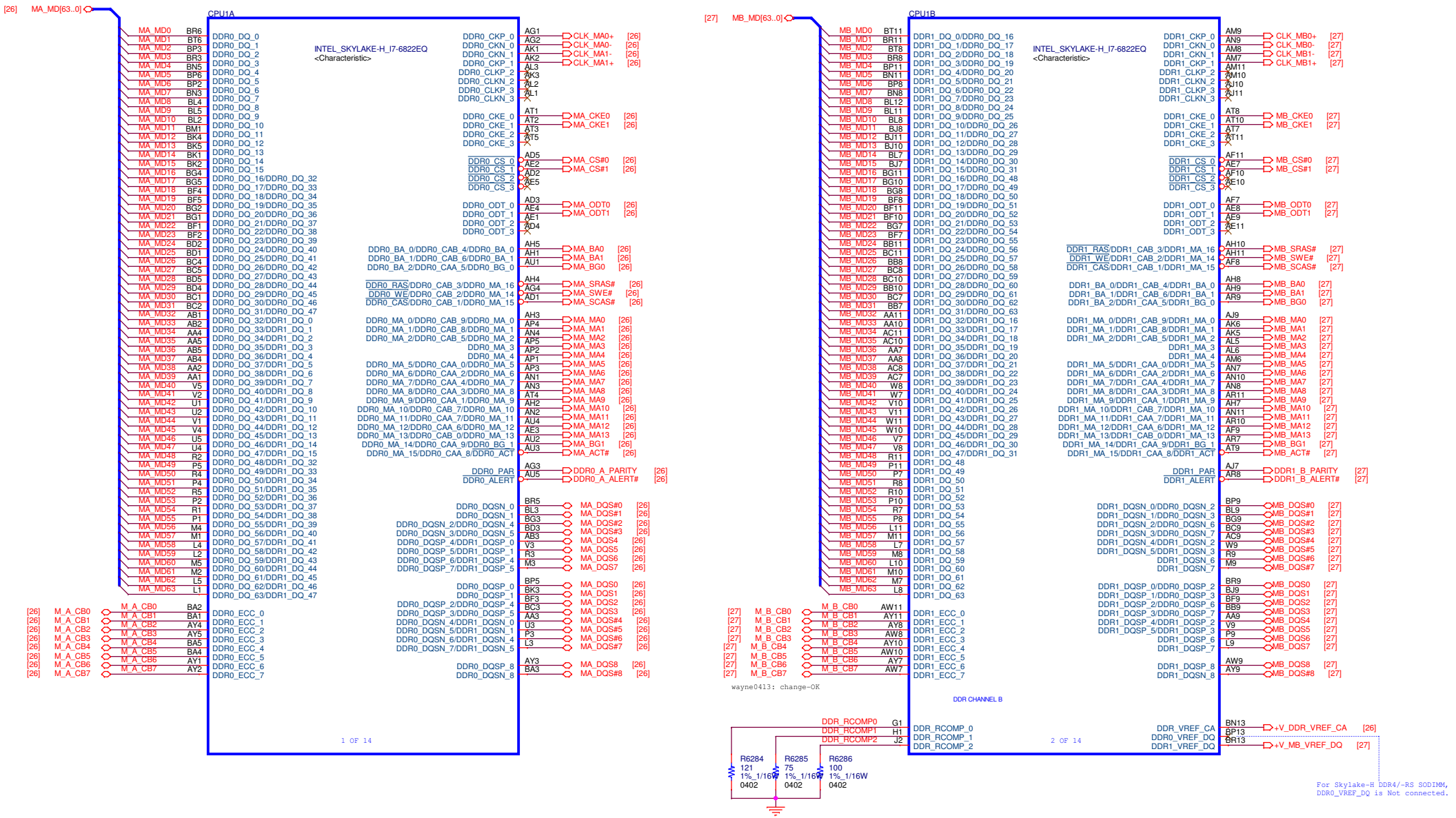
Skylake-H DDI/eDP



ADVANTECH			
Title	18_SKYLAKE-H DDI/eDP		
Size	Document Number AIIS-5410P		Rev A101-4
Date: Friday, February 26, 2016	Sheet 18 of 61		

Skylake-H Memory



Title	19_SKYLAKE-H Memory
Size	Document Number AIIS-5410P Rev A101-4
Date:	Friday, February 26, 2016 Sheet 19 of 61

Skylake-H PCIE/DMI

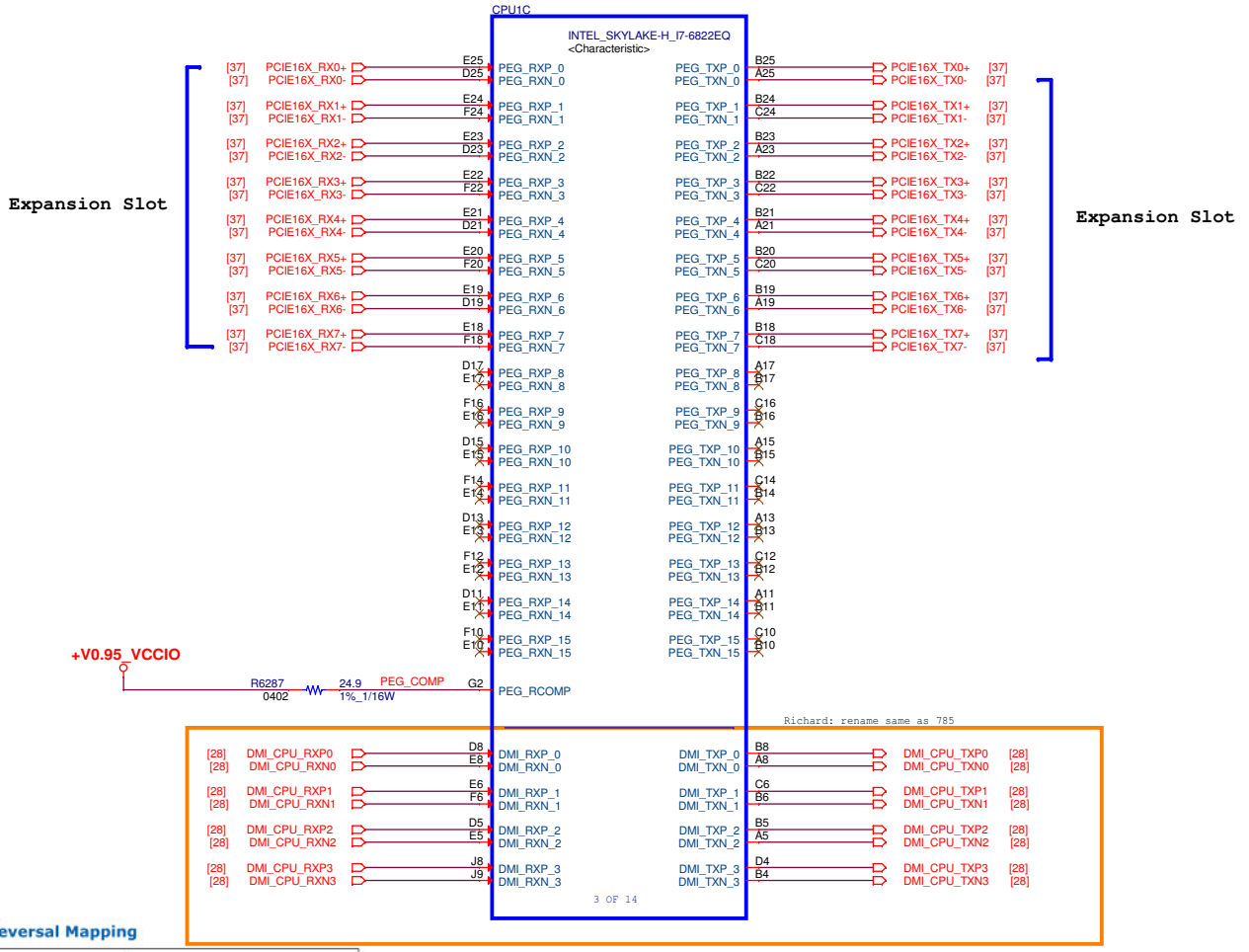


Table 2-17. PCI Express* Bifurcation and Lane Reversal Mapping

Bifurcation	Link Width			Config. Signals			Lanes													
	0:1:0	0:1:1	0:1:2	CFG [6]	CFG [5]	CFG [2]	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1x16	x16	N/A	N/A	1	1	1	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1x16 **Reversed**	x16	N/A	N/A	1	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2x8	x8	x8	N/A	1	0	1	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
2x8 **Reversed**	x8	x8	N/A	1	0	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
1x8+2x4	x8	x4	x4	0	0	1	0	1	2	3	4	5	6	7	0	1	2	3	0	1	2	3
1x8+2x4 **Reversed**	x8	x4	x4	0	0	0	3	2	1	0	3	2	1	0	7	6	5	4	3	2	1	0

Notes:

1. For CFG bus further details, refer to Section 6.4.
2. Support is also provided for narrow width and use devices with lower number of lanes (that is, usage on x4 configuration), however further bifurcation is not supported.
3. In case that more than one device is connected, the device with the highest lane count, should always be connected to the lower lanes, as follows:
   - Connect lane 0 of 1st device to lane 0.
   - Connect lane 0 of 2nd device to lane 8.
   - Connect lane 0 of 3rd device to lane 12.

   For example:
   a. When using 1x8 + 2x4, the 8 lane device must use lanes 0:7.
   b. When using 1x4 + 1x2, the 4 lane device must use lanes 0:3, and other 2 lanes device must use lanes 8:9.
   c. When using 1x4 + 1x2 + 1x1, 4 lane device must use lanes 0:3, two lane device must use lanes 8:9, one lane device must use lane 12.

ADVANTECH

Title	20_SKYLAKE-H PCIE/DMI		
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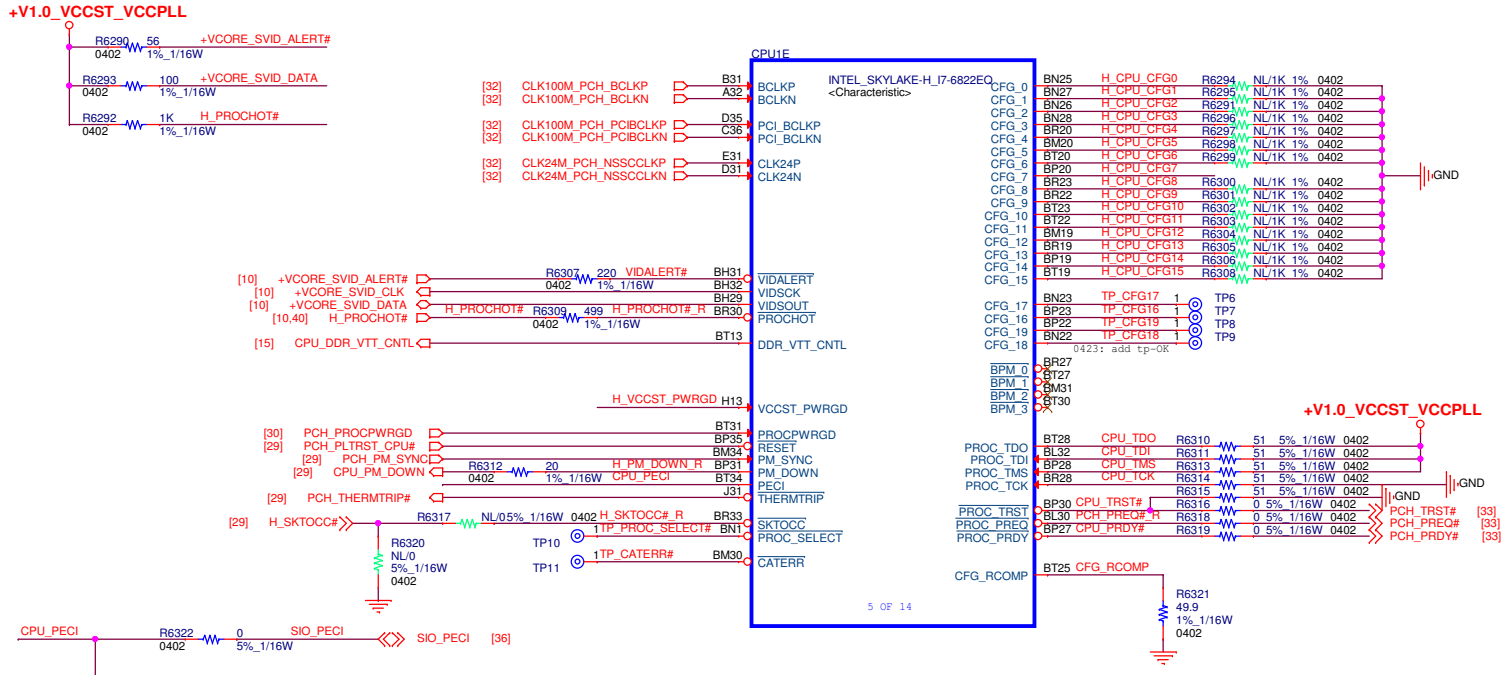
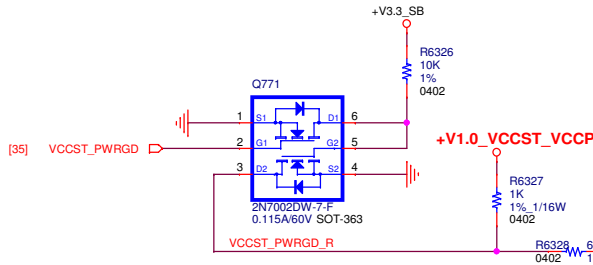
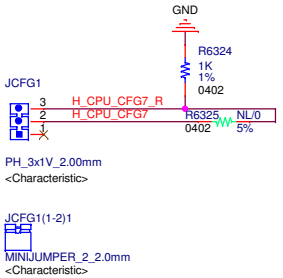
Skylake-H CFG





Mode	Jumper Setting
PEG Train immediately following RESET# de assertion.	1-2 Short (Default)
PEG Wait for BIOS for training.	2-3 Short

wayne0413: 保留 jumper-OK



Configuration Signals:

CFG[0]: Stall reset sequence after PCU PLL lock until de-asserted:
- 1 = (Default) Normal Operation;No stall.
- 0 = Stall.

CFG[2]: PCI Express* Static x16 Lane Numbering Reversal.
- 1 = (Default) Normal operation
- 0 = Lane numbers reversed.

CFG[4]: eDP enable:
- 1 = Disabled.
- 0 = (Default) Enabled.

CFG[6:5]: PCI Express* Bifurcation
- 00 = 1 x8, 2 x4 PCI Express*
- 01 = reserved
- 10 = 2 x8 PCI Express*
- 11 = (Default) 1 x16 PCI Express*

CFG[7]: PEG Training:
- 1 = (default) PEG Train immediately following RESET# de assertion.
- 0 = PEG Wait for BIOS for training.

ADVANTECH		
Title	21_SKYLAKE-H CFG/JTAG	
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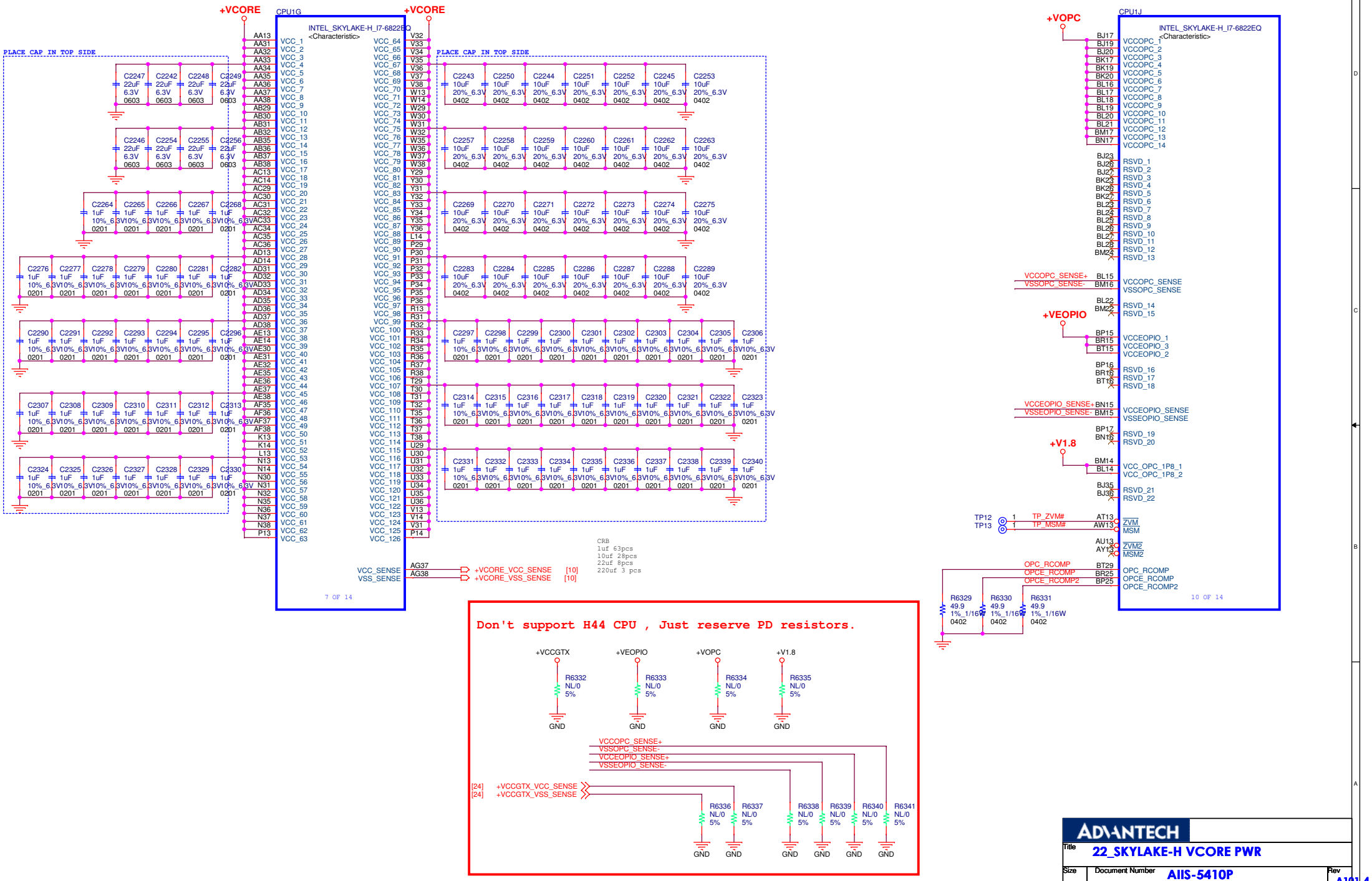
Skylake-H VCORE

wayne0413: change follow CRB cap. qty.-OK



Title	22_SKYLAKE-H VCORE PWR		
Size	Document Number AIIS-5410P		Rev A101-4
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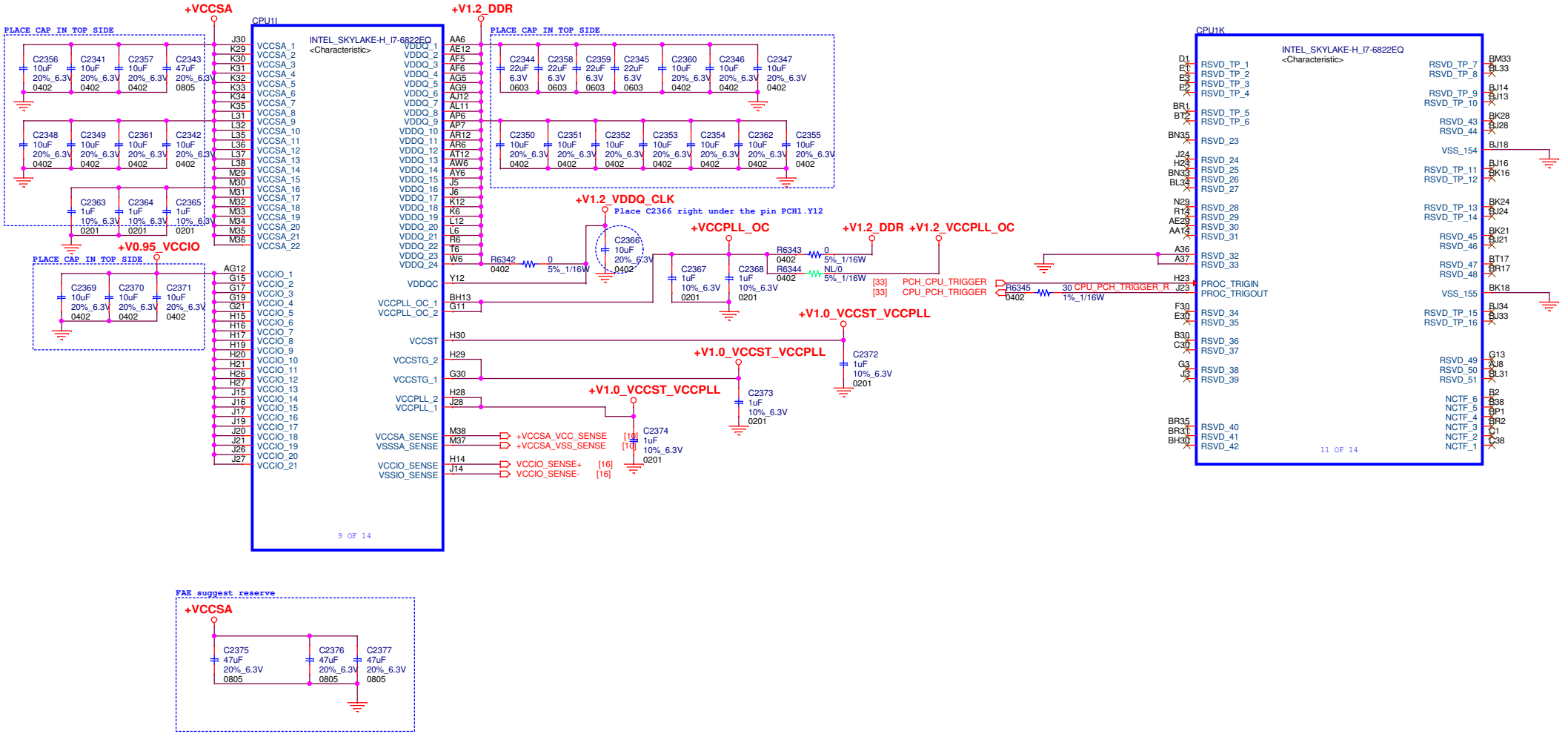
Skylake-H VCCSA

wayne0413: change follow CRB cap. qty.-OK



ADVANTECH

Title	23_SKYLAKE-H VCCSA PWR	
Size	Document Number AIIS-5410P	Rev A101-4
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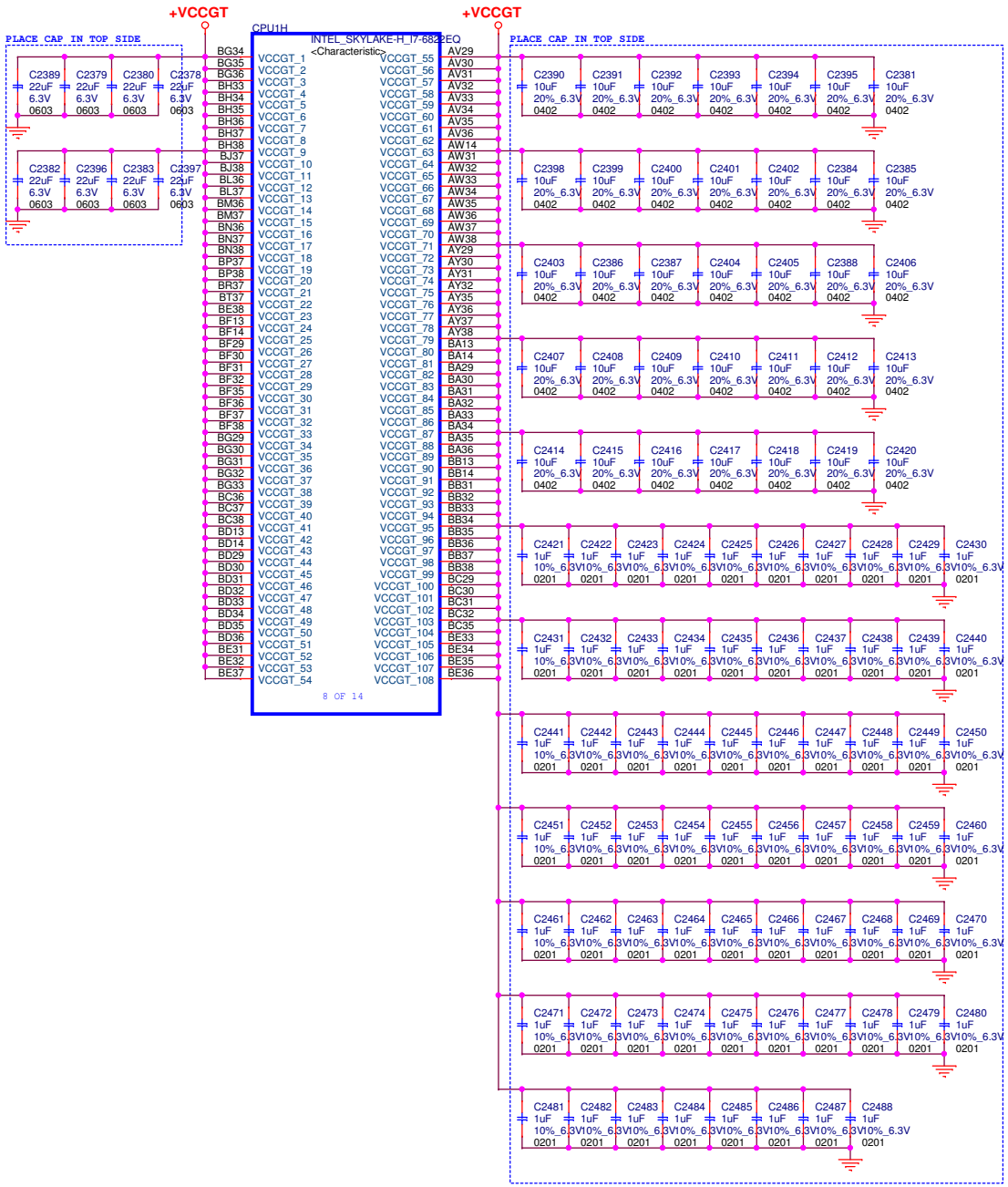
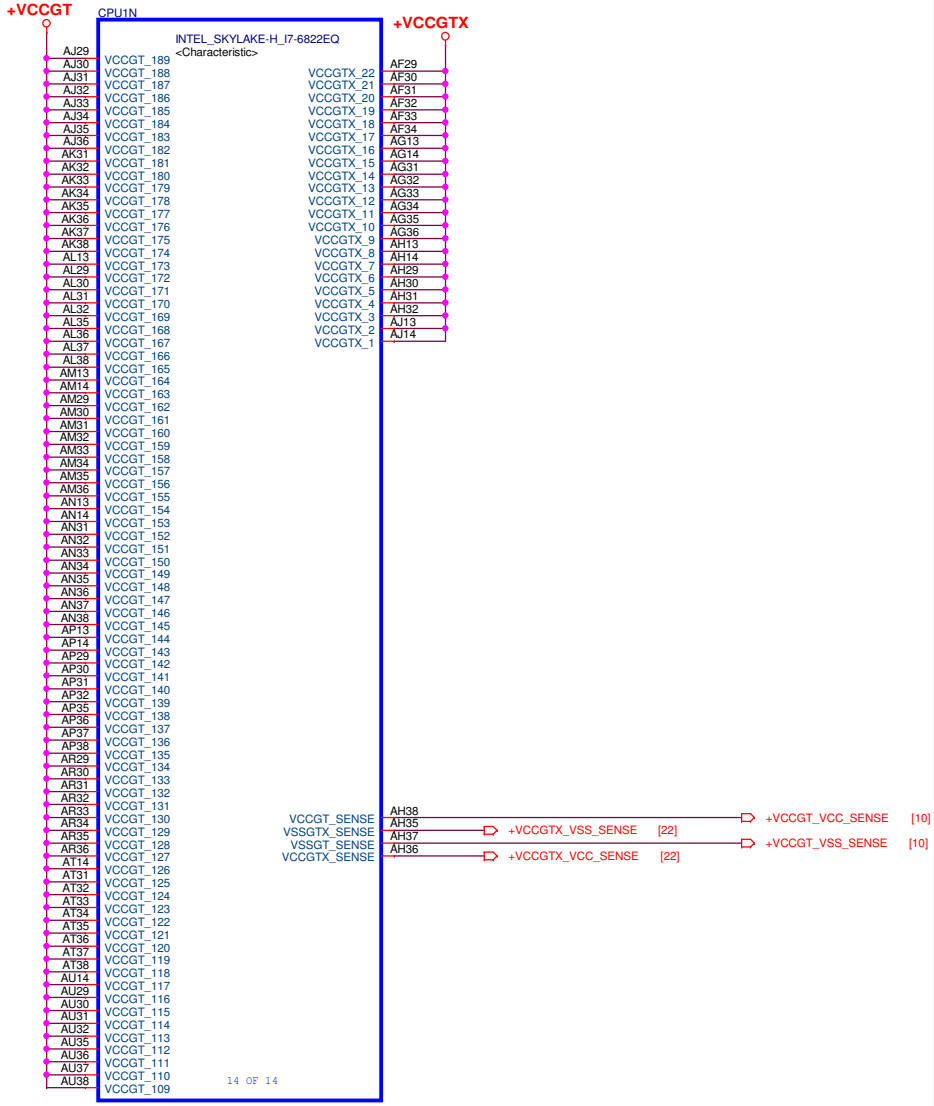
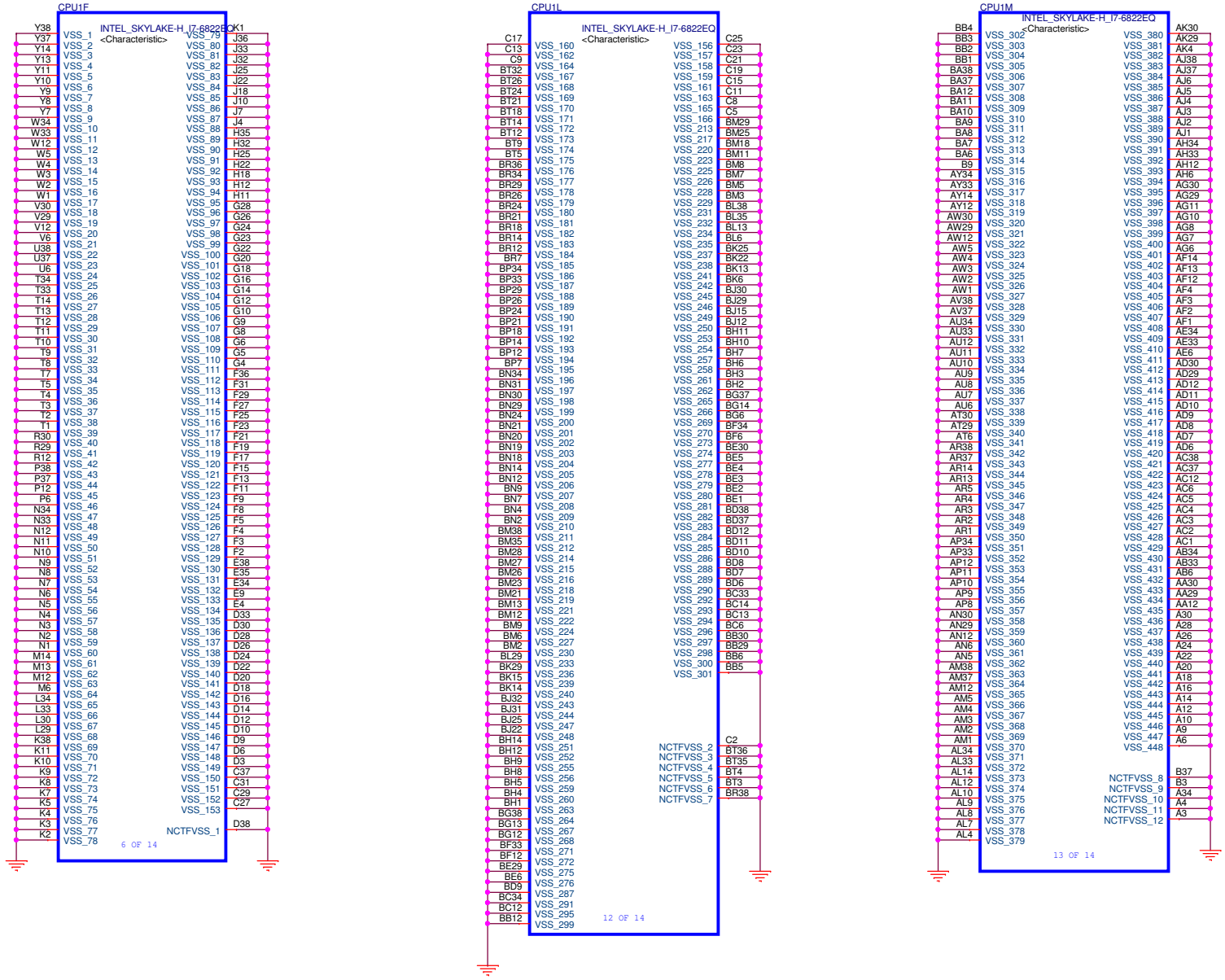
Skylake-H VCCGT





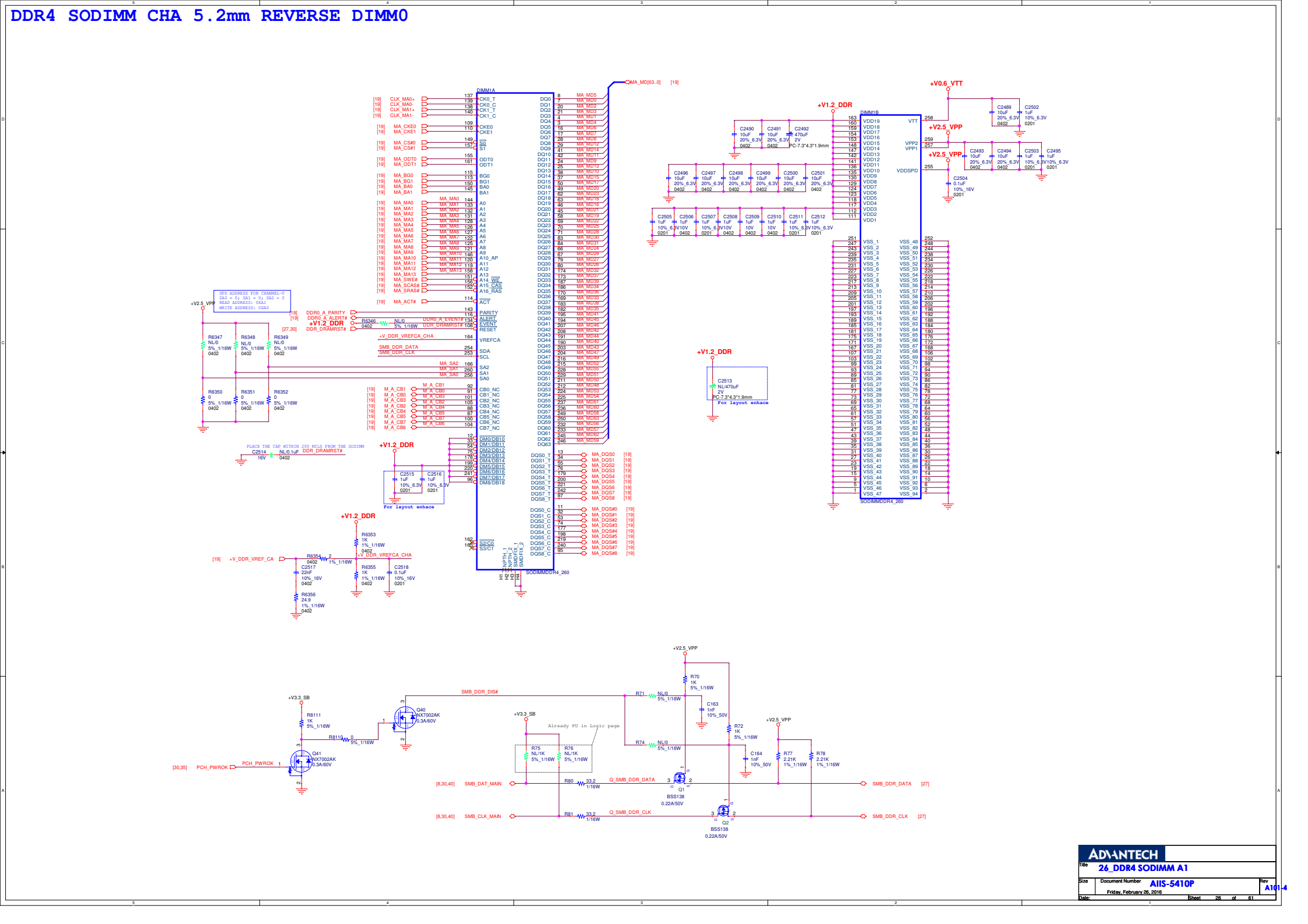
ADVANTECH			
Title	24_SKYLAKE-H VCCGT PWR		
Size	Document Number AIIS-5410P		Rev A101-4
Date: Friday, February 26, 2016	Sheet 24 of 61		

Skylake-H GND



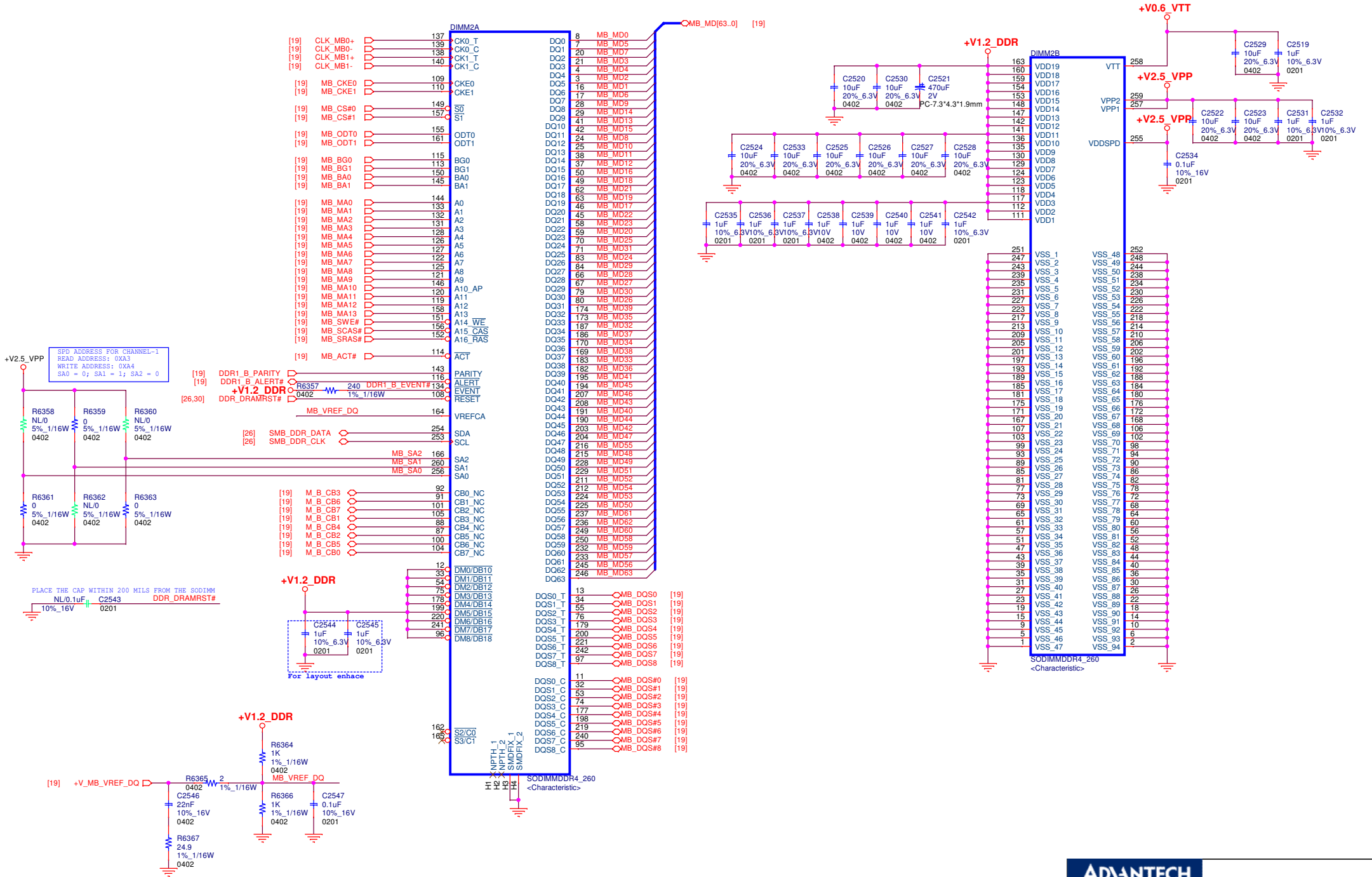
Title	25_SKYLAKE-H GND
Size	Document Number AIIS-5410P Rev A101-4
Date:	Friday, February 26, 2016 Sheet 25 of 61

DDR4 SODIMM CHA 5.2mm REVERSE DIMM0



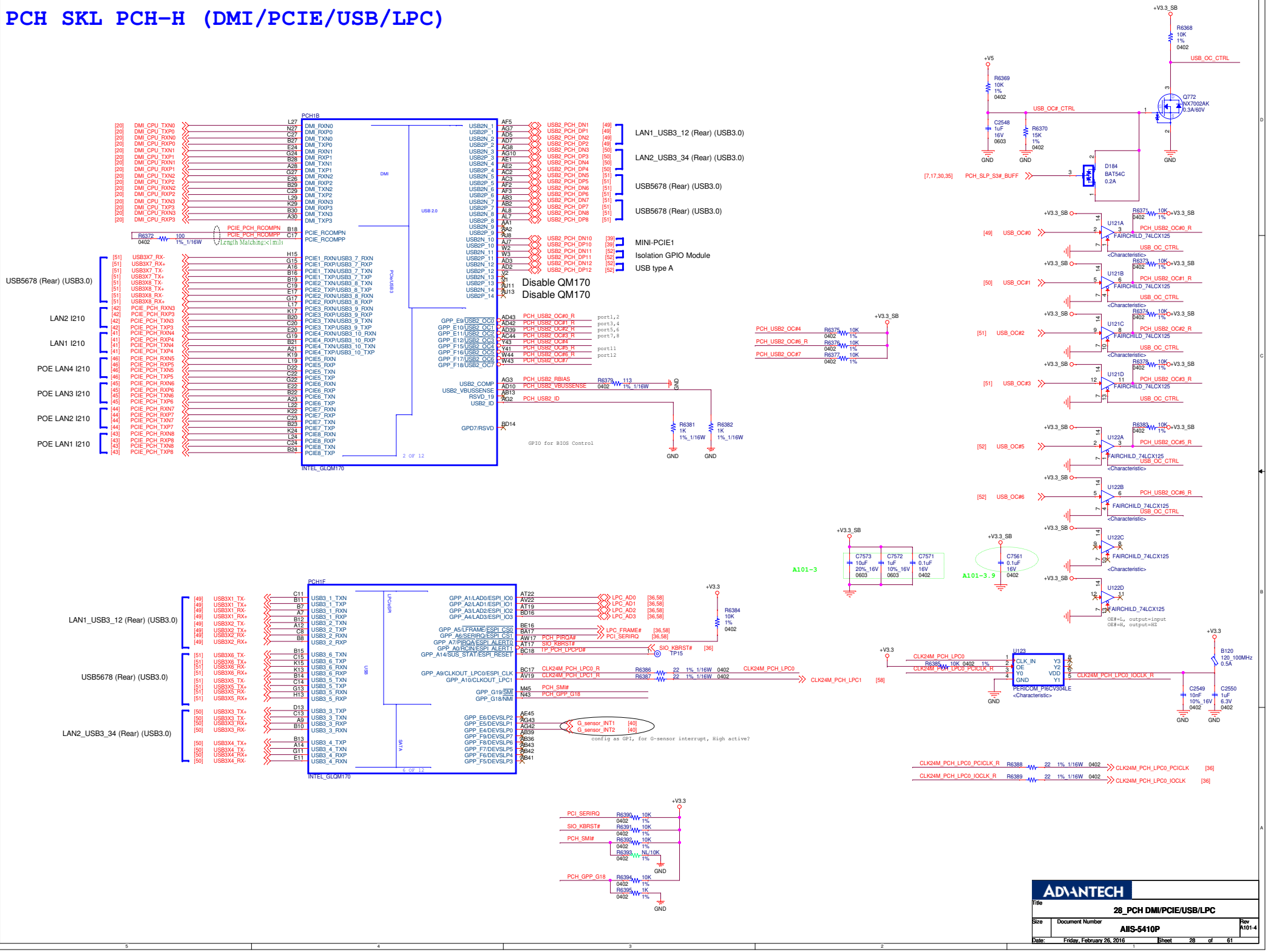
Title	26_DDR4 SODIMM A1		
Size	Document Number AIIS-5410P		Rev A101-4
Date: Friday, February 26, 2016	Sheet 26 of 61		

DDR4 SODIMM CHB 9.2mm STD DIMM0

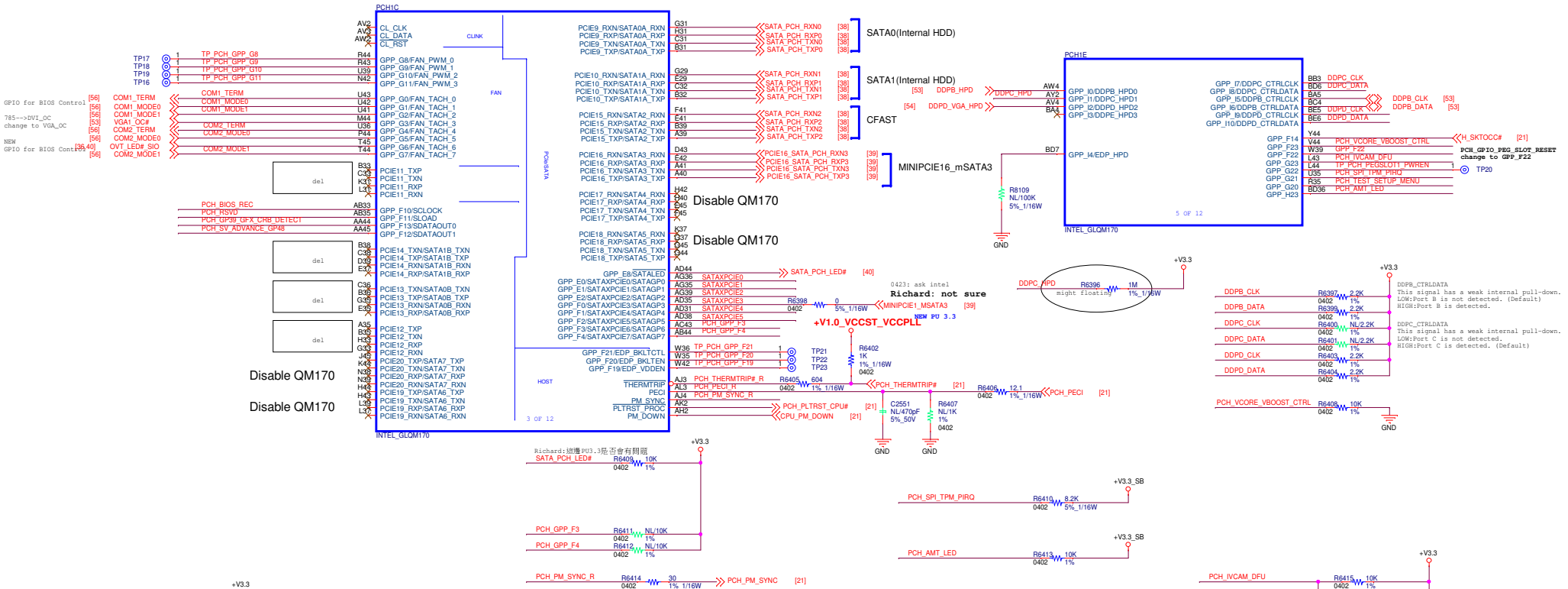


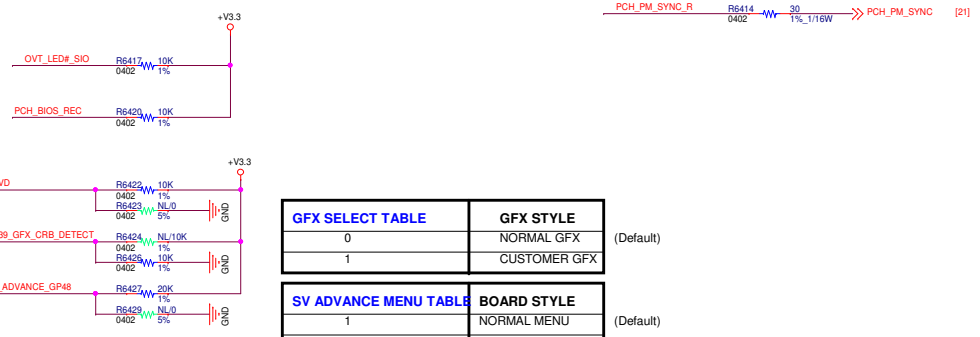
Title	27_DDR4 SODIMM B1
Size	Document Number AIIS-5410P Rev A101-4
Date:	Friday, February 26, 2016 Sheet 27 of 61

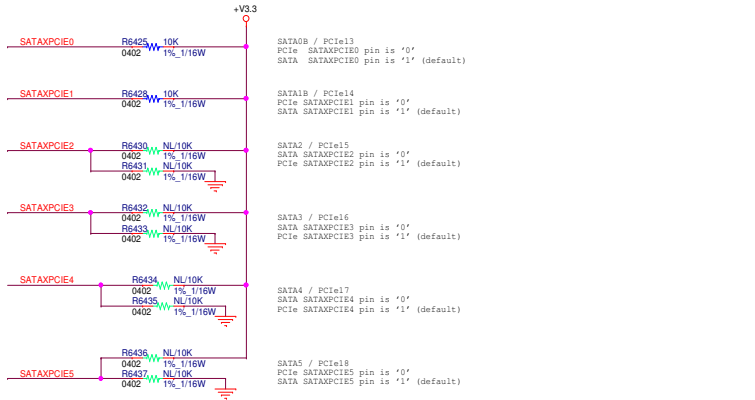
PCH SKL PCH-H (DMI/PCIE/USB/LPC)



PCH SKL PCH-H (PCIE/SATA/DDC)







TEST SETUP MENU TABLE

	BOARD STYLE
0	TEST SETUP MENU ENABLED
1	DISABLED (Default)

GFX SELECT TABLE	GFX STYLE
0	NORMAL GFX (Default)
1	CUSTOMER GFX

SV ADVANCE MENU TABLE	BOARD STYLE
1	NORMAL MENU (Default)
0	SV ADVANCE MENU

ADVANTECH

Title: 29_PCH PCIE/SATA/DDC

Size	Document Number	Rev
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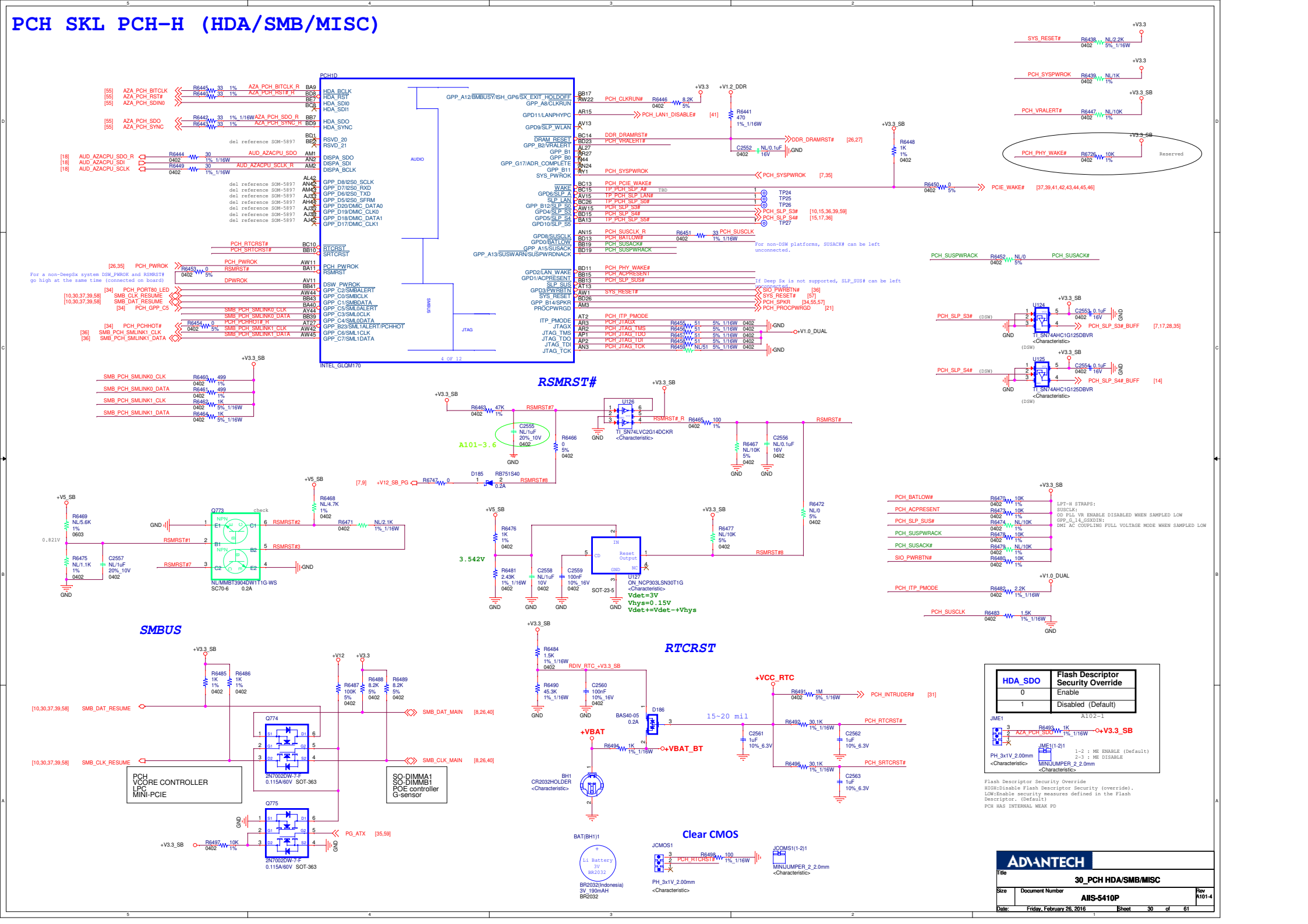
Date: Friday, February 26, 2016 Sheet 29 of 61

PCH SKL PCH-H (HDA/SMB/MISC)

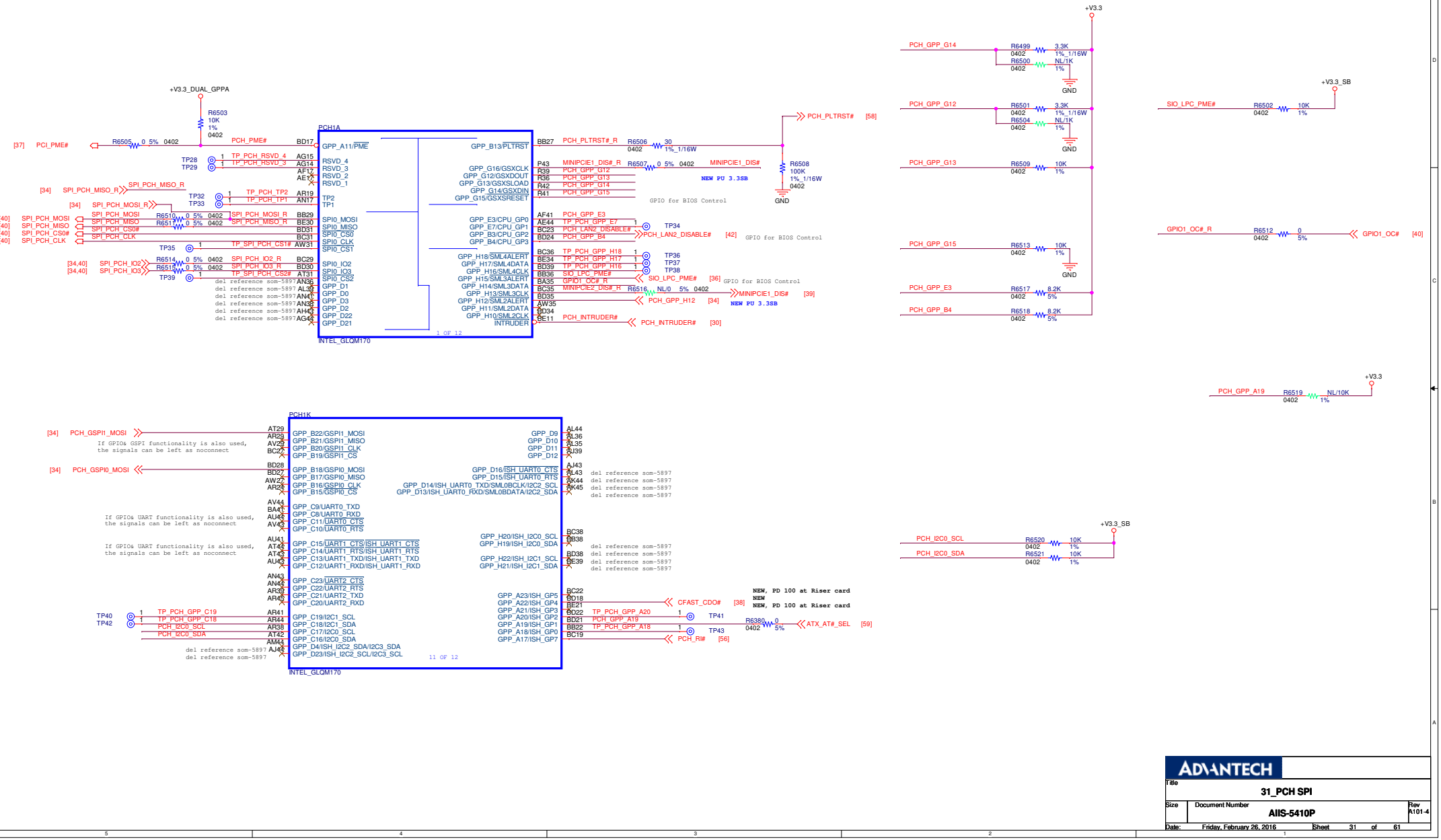


HDA_SDO	Flash Descriptor Security Override
0	Enable
1	Disabled (Default)

Flash Descriptor Security Override
HIGH:Disable Flash Descriptor Security (override).
LOW:Enable security measures defined in the Flash Descriptor. (Default)
PCH HAS INTERNAL WEAK PD

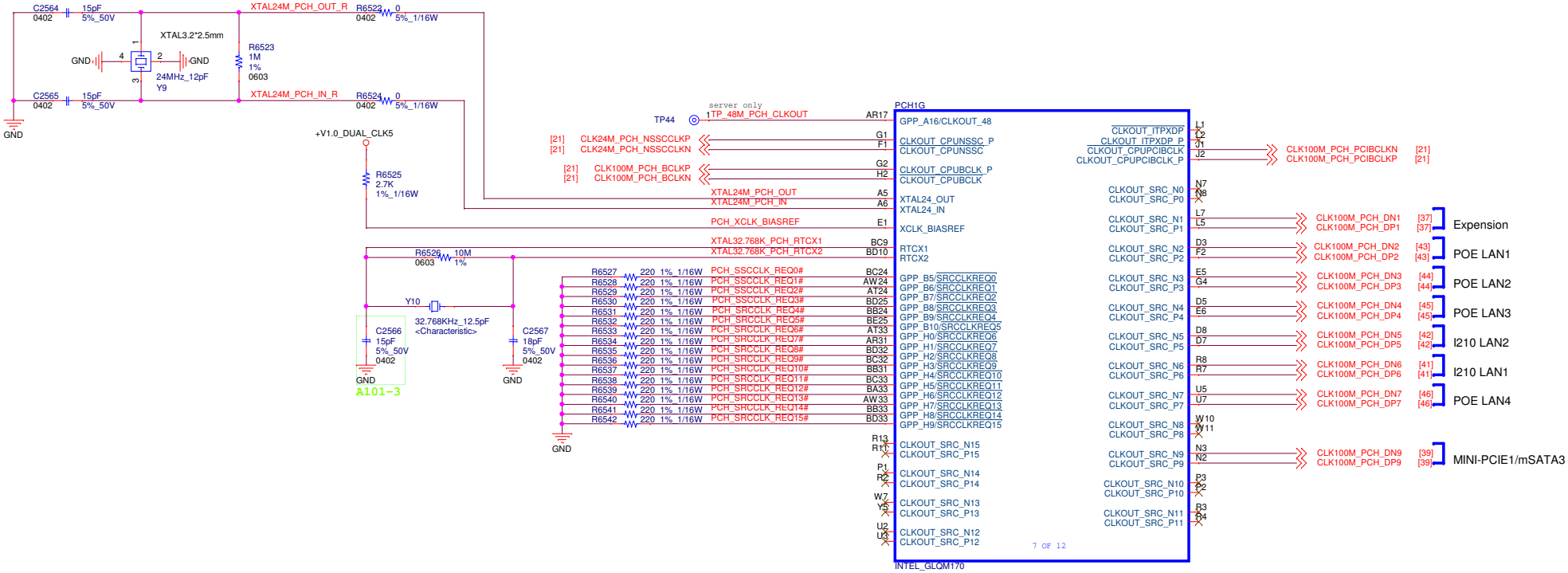
Title	30_PCH HDA/SMB/MISC		
Size	Document Number	AIIS-5410P	Rev A101-4
Date:	Friday, February 26, 2016	Sheet 30 of 61	

PCH SKL PCH-H (SPI)



Title	31_PCH SPI	
Size	Document Number AIIS-5410P	Rev A101-4
Date: Friday, February 26, 2016	Sheet 31 of 61	

PCH SKL PCH-H (CLOCK)



ADVANTECH

Title	32_PCH CLOCK	
Size	Document Number: AIIS-5410P	Rev: A101-4
Date: Friday, February 26, 2016	Sheet 32 of 61	

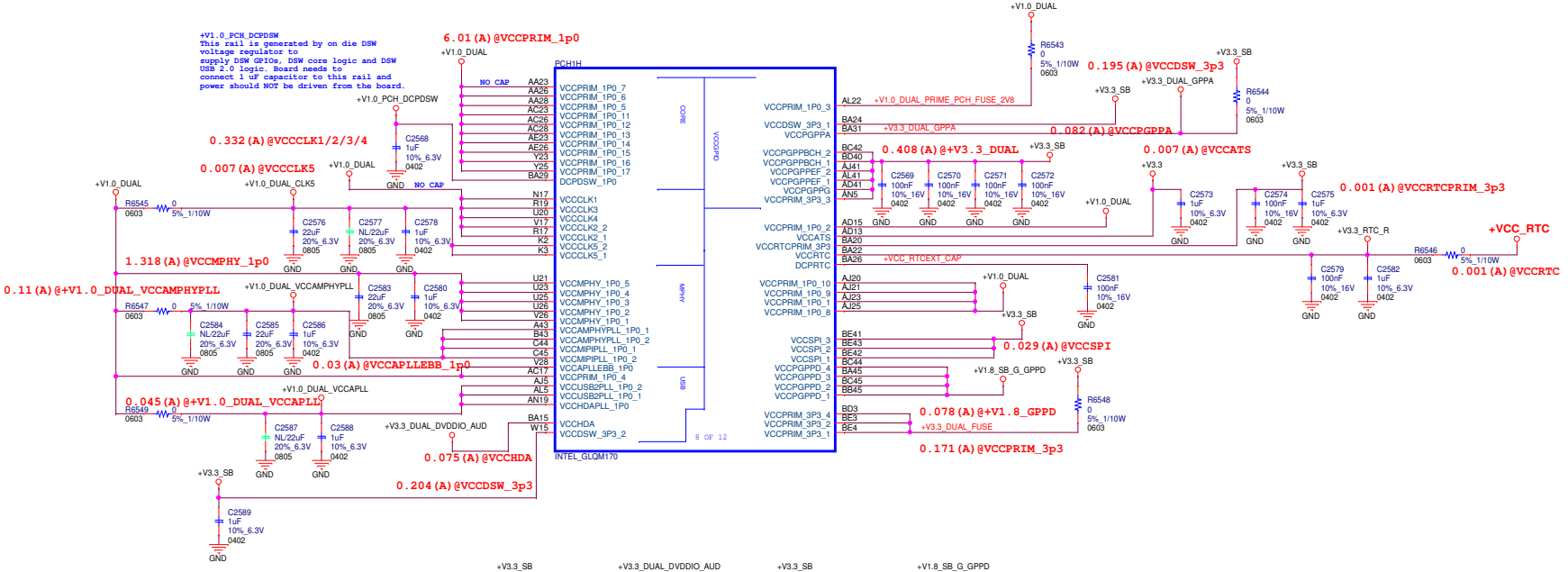
PCH SKL PCH-H (POWER)

7.858(A)@+V1.0_DUAL

0.844(A)@+V3.3_DUAL

0.205(A)@+V3.3_SB

0.007(A)@+V3.3



Title	33_PCH POWER		
Size	Document Number		Rev
	AIIS-5410P		A101-4
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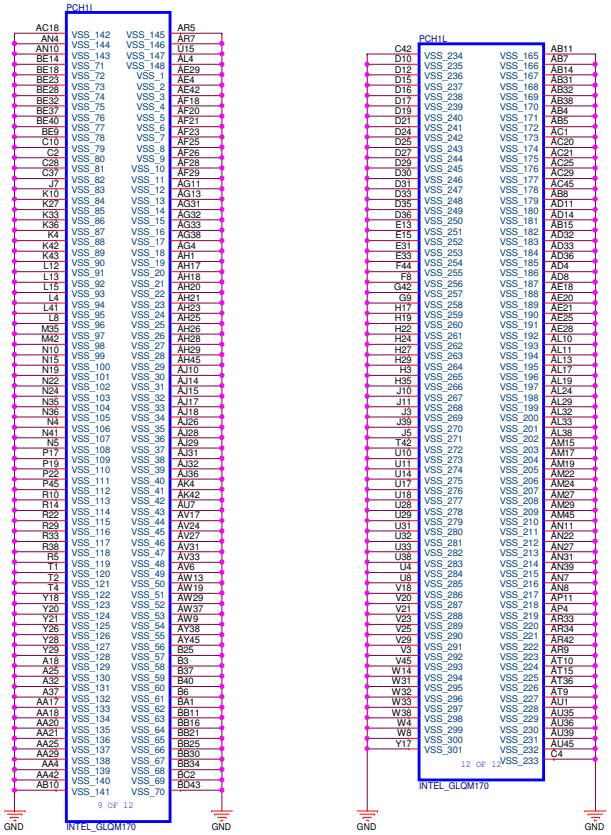
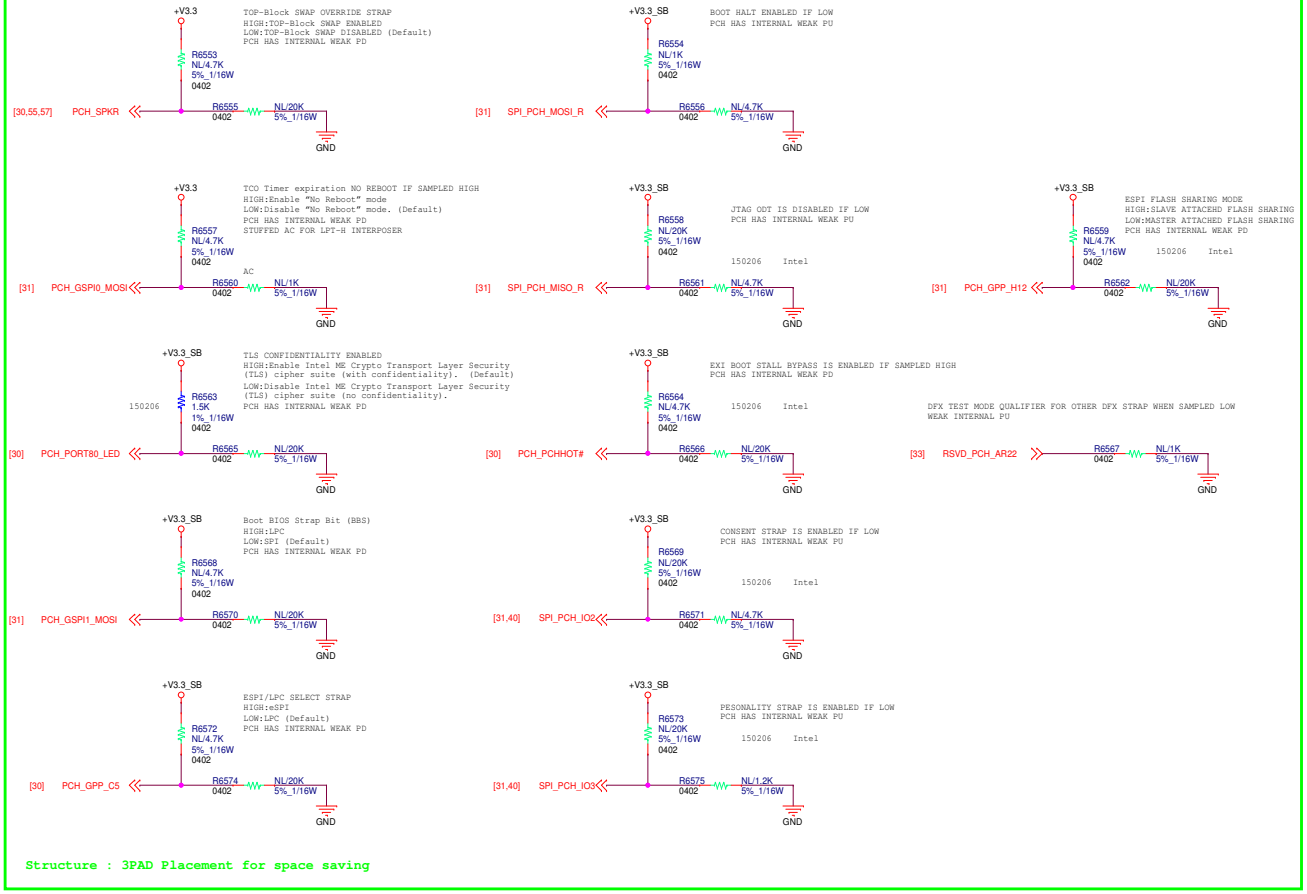
PCH SKL PCH-H (GND,PCH Strap Option)



PCH Strap Option

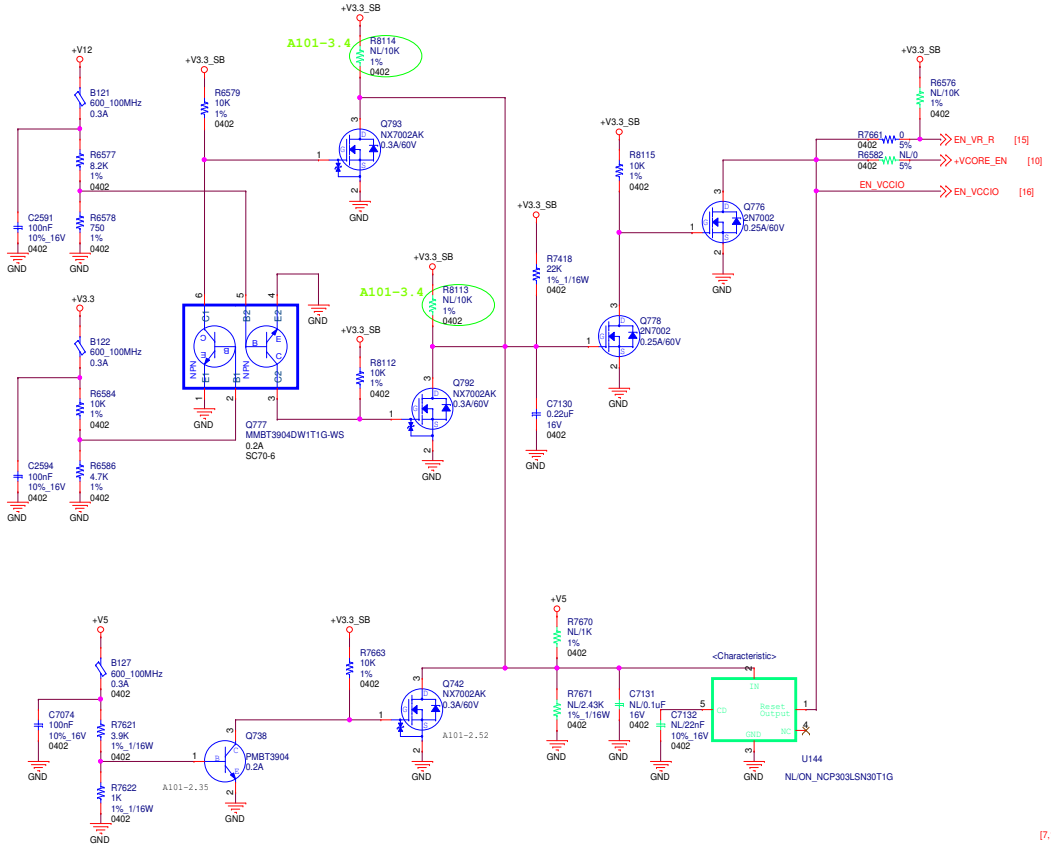


Structure : 3PAD Placement for space saving

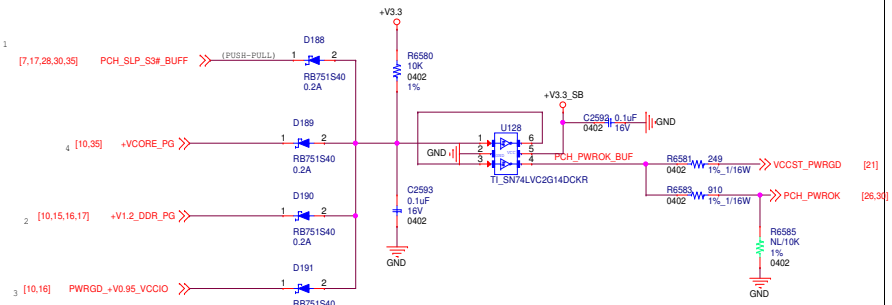
ADVANTECH

Title	34_PCH GND/PCH Strap Option	
Size	Document Number: AIIS-5410P	Rev: A101-4
Date: Friday, February 26, 2016	Sheet 34 of 61	

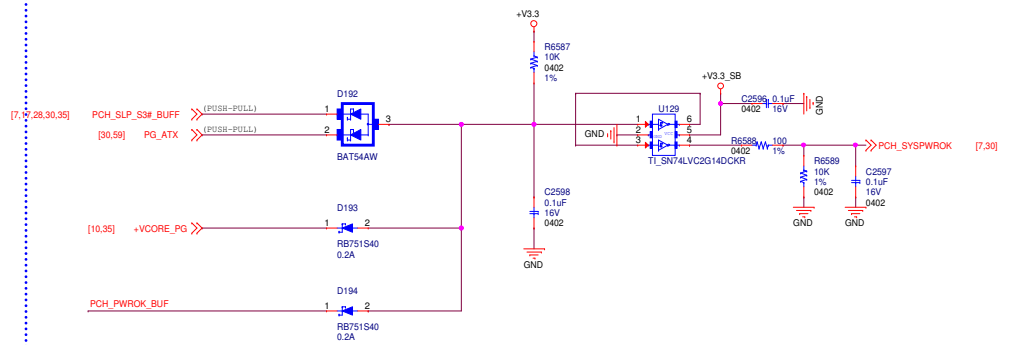
VR_EN



PWROK



SYS_PWROK



ADVANTECH			
Title	35_PWROK/SYSPWROK/VCORE_EN		
Size	Document Number AIIS-5410P		Rev A101-4
Date: Friday, February 26, 2016	Sheet 35 of 61		

SIO-NCT6106D

COM2

Fan Ctrl.

KB/MS

COM1

PORT80

LPC

SIO old version 1410022361

NCT6106D
LQFP128
NUVOTON_NCT6106D-C
<Characteristic>

thermistor 給power board 用
與SIO_AGND平行走線到GF1

Close to SuperIO thermistor

JCASE1 : caseopen pin header

POWER ON SETTING PIN

PIN	Name	0	1	Strapping Power
51	UART1_RTS#	2E	4E	3VCC
52	UART1_DTR#	24M Clock Source	48M Clock Source	3VCC
54	UART1_SOUT	GPIO to PORT80 Disable	GPIO to PORT80 Enable	3VCC
106	SUPLED	UART	DSW	3VSB
111	UART3_RTS#	SOUTC to 80port disable	SOUTC to 80port enable	3VCC
112	UART3_DTR#	SOUTE to 80port disable	SOUTE to 80port enable	3VCC

Title	36_SIO NCT6106D
Size	Custom
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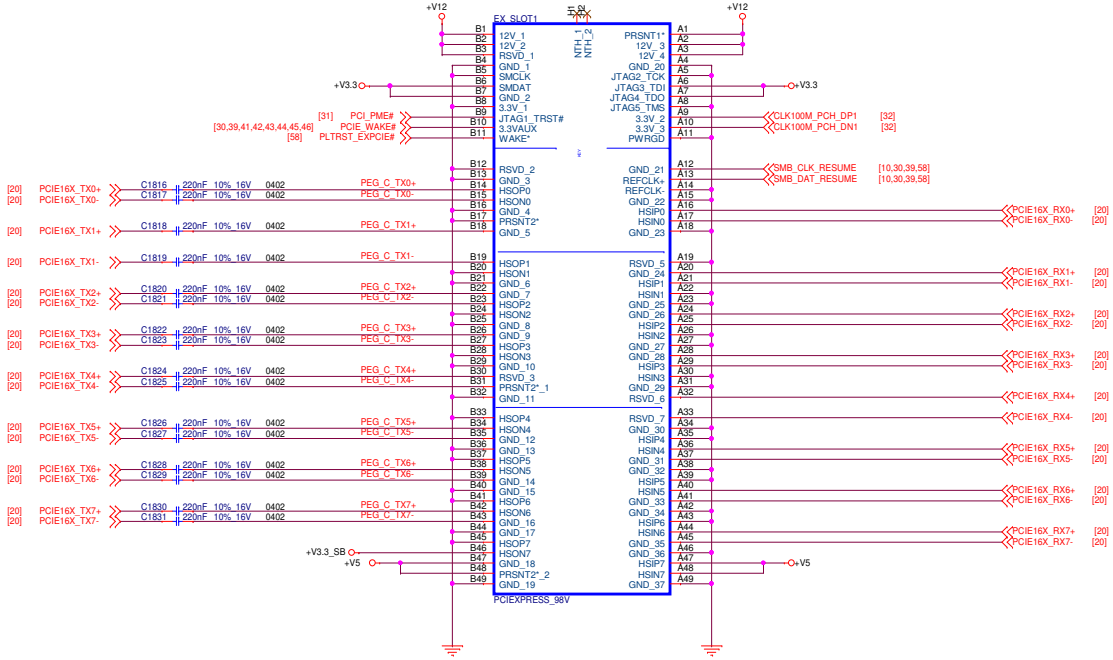
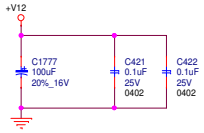
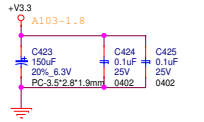
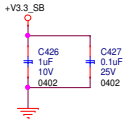
EXPCIEX8 Slot

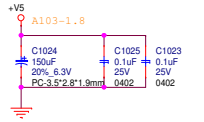


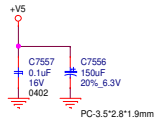
x8 PCIe Connector A			
AB01	+12V	+12V	AA01
AB02	+12V	+12V	AA02
AB03	+12V	+12V	AA03
AB04	GND	GND	AA04
AB05	GND	GND	AA05
AB06	+3.3V	+3.3V	AA06
AB07	+3.3V	+3.3V	AA07
AB08	GND	GND	AA08
AB09	PCI_PME#	REFCLK1+	AA09
AB10	WAKE#	REFCLK1-	AA10
AB11	PERST#	GND	AA11
Mechanical Key			
AB12	GND	SMCLK	AA12
AB13	GND	SMDAT	AA13
AB14	a_PETp0	GND	AA14
AB15	a_PETn0	GND	AA15
AB16	GND	a_PERp0	AA16
AB17	GND	a_PERn0	AA17
AB18	a_PETp1	GND	AA18
AB19	a_PETn1	GND	AA19
AB20	GND	a_PERp1	AA20
AB21	GND	a_PERn1	AA21
AB22	a_PETp2	GND	AA22
AB23	a_PETn2	GND	AA23
AB24	GND	a_PERp2	AA24
AB25	GND	a_PERn2	AA25
AB26	a_PETp3	GND	AA26
AB27	a_PETn3	GND	AA27
AB28	GND	a_PERp3	AA28
AB29	GND	a_PERn3	AA29
AB30	a_PETp4	GND	AA30
AB31	a_PETn4	GND	AA31
AB32	GND	a_PERp4	AA32
AB33	GND	a_PERn4	AA33
AB34	a_PETp5	GND	AA34
AB35	a_PETn5	GND	AA35
AB36	GND	a_PERp5	AA36
AB37	GND	a_PERn5	AA37
AB38	a_PETp6	GND	AA38
AB39	a_PETn6	GND	AA39
AB40	GND	a_PERp6	AA40
AB41	GND	a_PERn6	AA41
AB42	a_PETp7	GND	AA42
AB43	a_PETn7	GND	AA43
AB44	GND	a_PERp7	AA44
AB45	GND	a_PERn7	AA45
AB46	+3.3VSB	GND	AA46
AB47	+5V	+5V	AA47
AB48	+5V	+5V	AA48
AB49	GND	GND	AA49

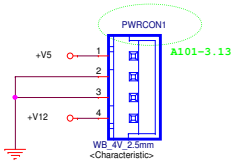












ADVANTECH

Title	37_EXPCIEX8 Slot	
Size C	Document Number AIIS-5410P	Rev A101-4
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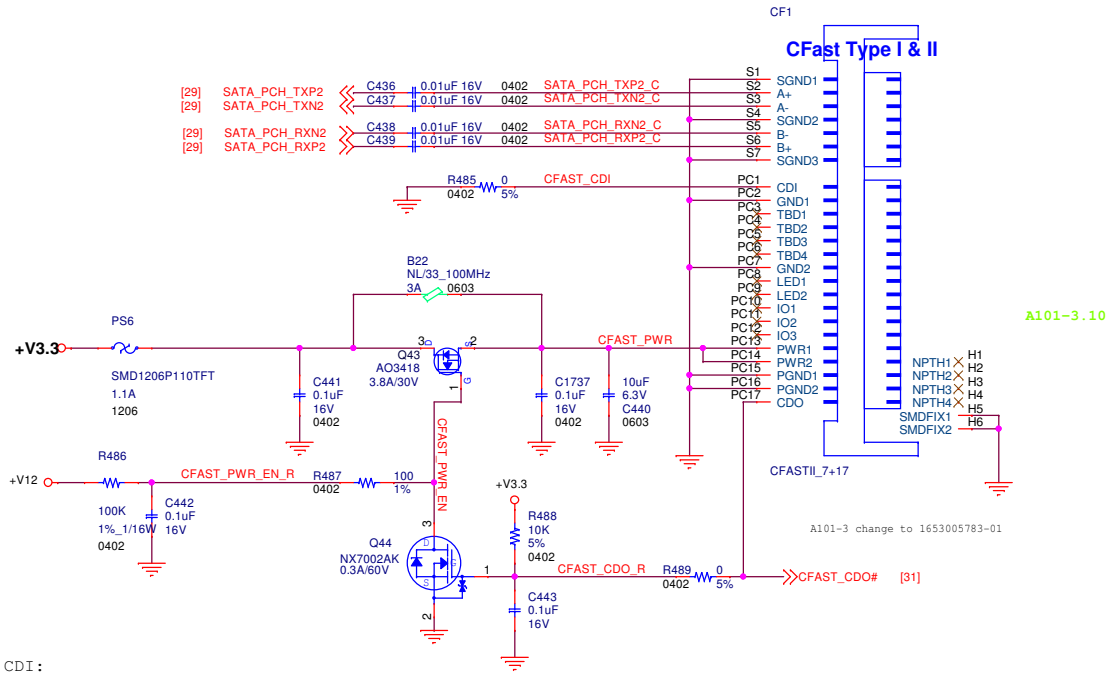
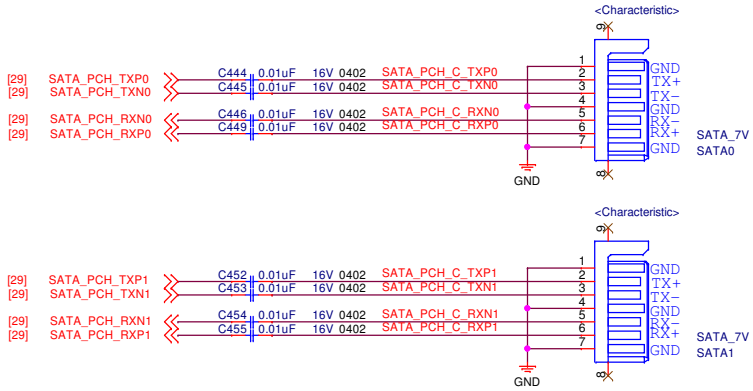
CFast

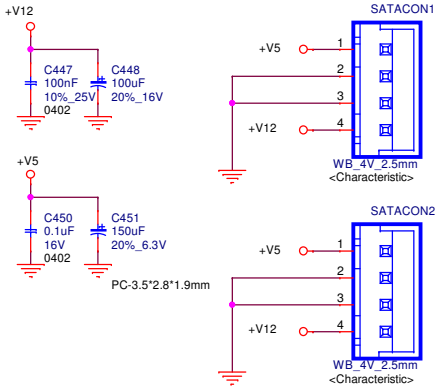


CDI:
This signal is driven by the CFast host, and shall be sampled by the CFast device
This pin shall be shorted on a CFast device to CDO.
This signal and CDO provide a mechanism for a CFast host to detect that a CFast device has been fully inserted, and so that power can be applied safely.
The host may drive, and the device may sample, this pin to provide signaling to enable CFast Power Management Sleep state.
CDO:
This pin shall be shorted on the CFast device to CDI. It is effectively driven by CDI.

SATA PORT-> 6Gbps



SATA Power Conn.



ADVANTECH		
Title	38_CONN_SATA1&2 / CFast]	
Size	Document Number AIIS-5410P	Rev A101-4
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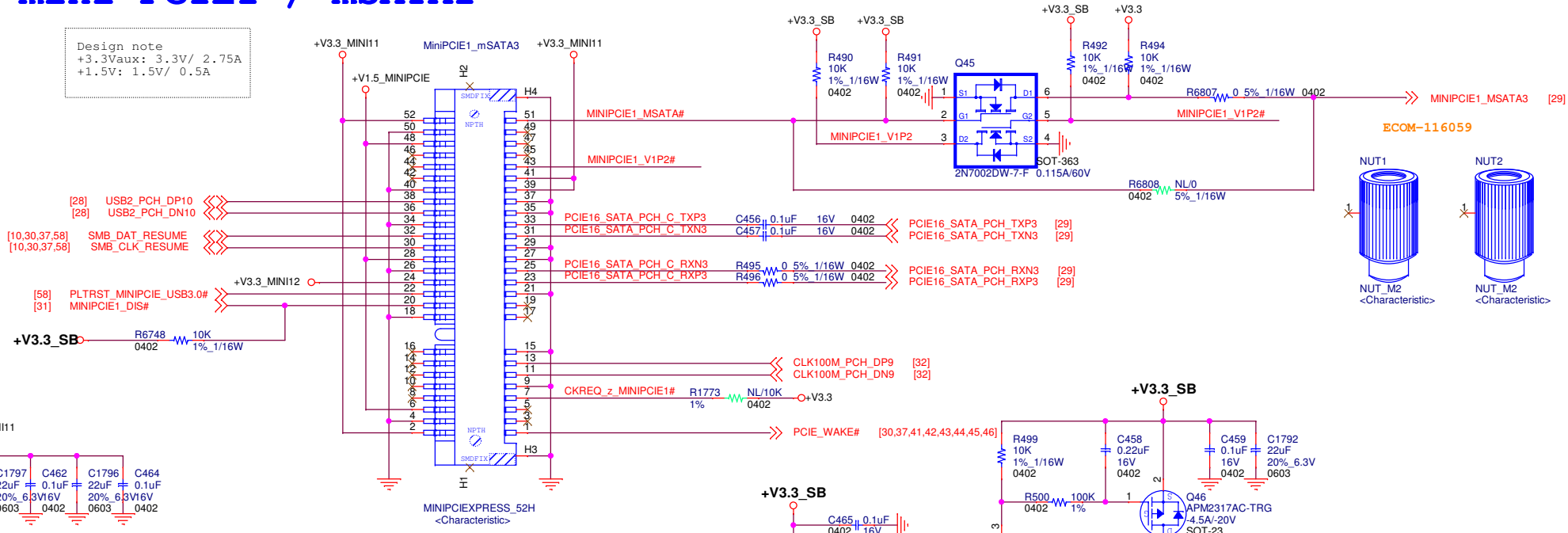
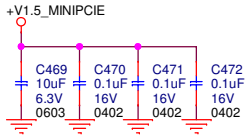
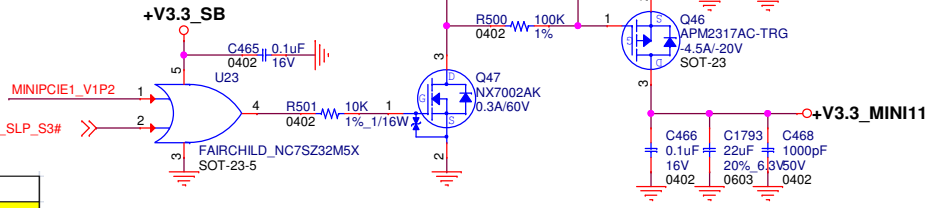
mini-PCIE1 / mSATA1

Design note
+3.3Vaux: 3.3V/ 2.75A
+1.5V: 1.5V/ 0.5A



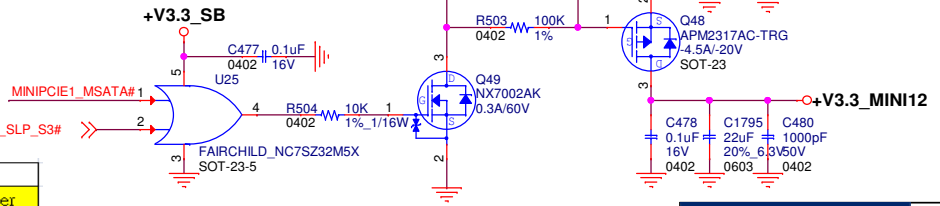


waynel014: review cap-OK



Power of Pin2, 39, 41, 52		
Pin43	SLP_S3#	Power
L	L	3.3V
L	H	3.3V
H	L	0V
H	H	3.3V

Pin43 | SLP_S3# = Power



Power of Pin24		
Pin51	SLP_S3#	Power
L	L	0V
L	H	3.3V
H	L	3.3V
H	H	3.3V

Pin51 | SLP_S3# = Power

Pin	mini-pcie 1.1	mini-pcie 1.2	mSATA	
2	3.3V	3.3Vaux	3.3V	+V3.3_MINI11
24	3.3Vaux	3.3Vaux	3.3V	+V3.3_MINI12
39	Reserved*	3.3Vaux	3.3V	+V3.3_MINI11
41	Reserved*	3.3Vaux	3.3V	+V3.3_MINI11
52	3.3V	3.3Vaux	3.3V	+V3.3_MINI11

Spec.	Mini PCIe 1.1	Mini PCIe 1.2	mSATA
Pin43	Reserved (H)	GND (L)	NC (H)
Pin51	Reserved (H)	Reserved (H)	Presences Detection (GND->L)

ADVANTECH

Title	39_MINI-PCIE1/mSATA3	
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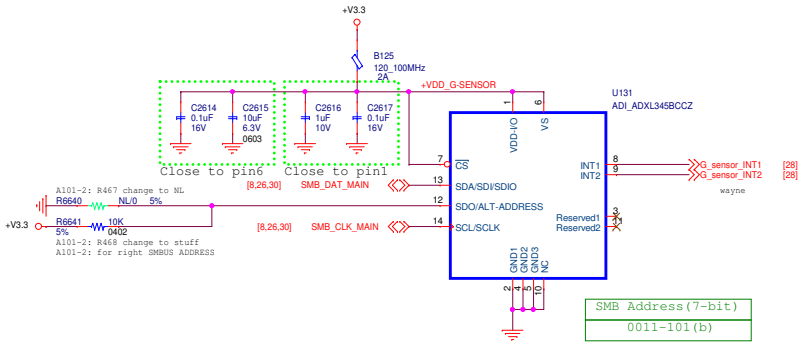
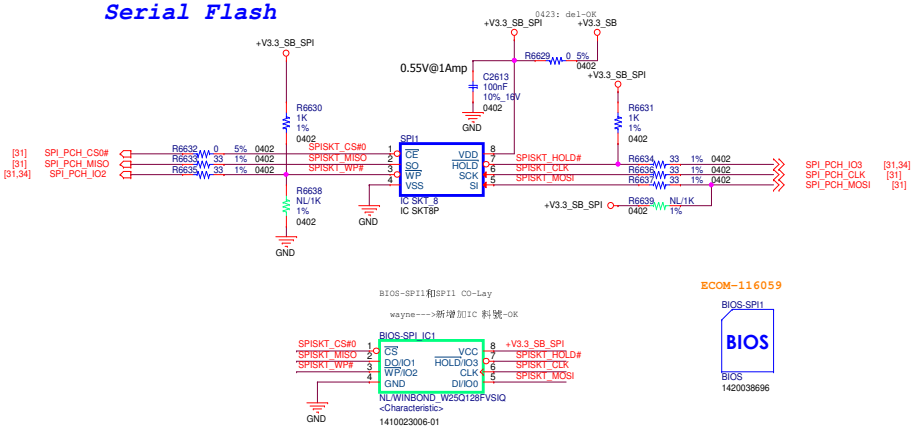
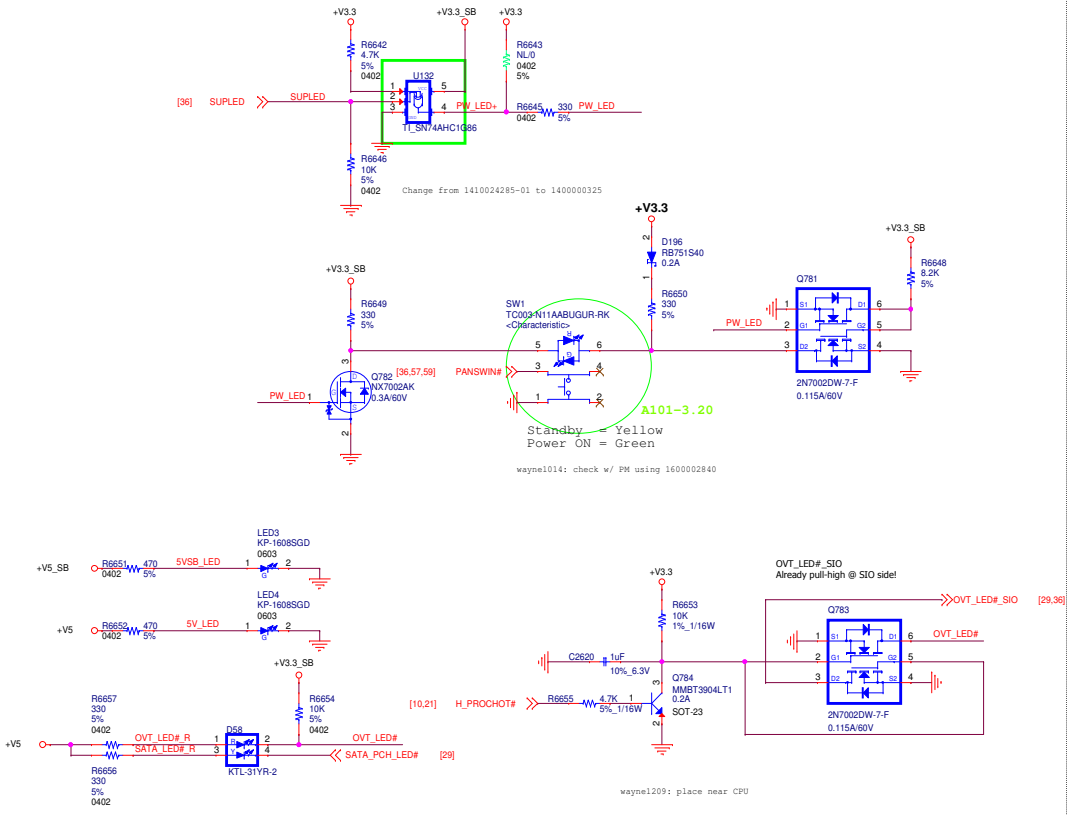
G-Senser



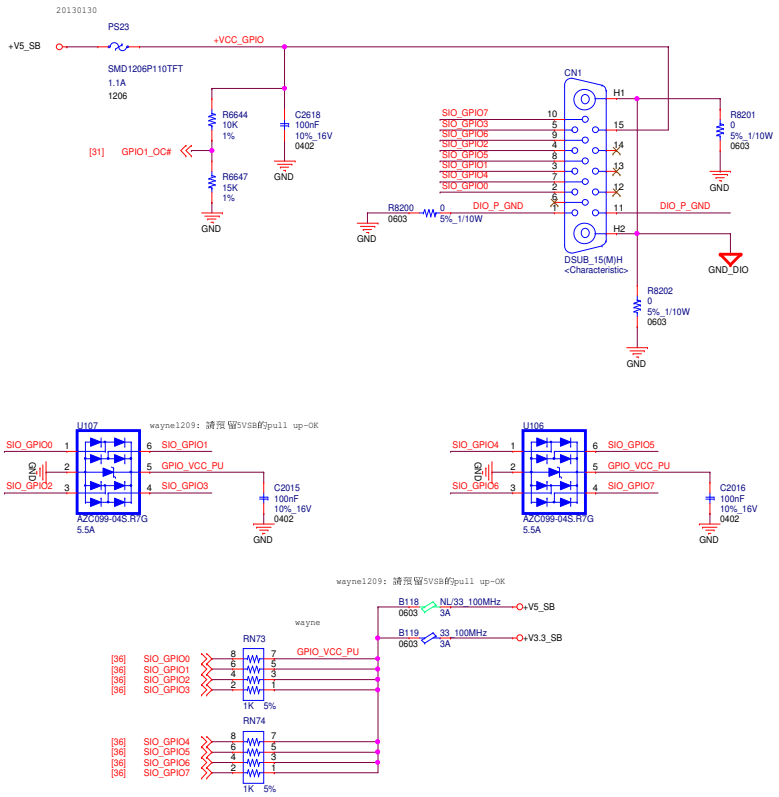
Serial Flash



PWRLED



8 bit GPIO



ADVANTECH			
Title	40_PWRLED/GPIO/SPI/G-SENSOR		
Size	Document Number	AIIS-5410P	Rev A101-4
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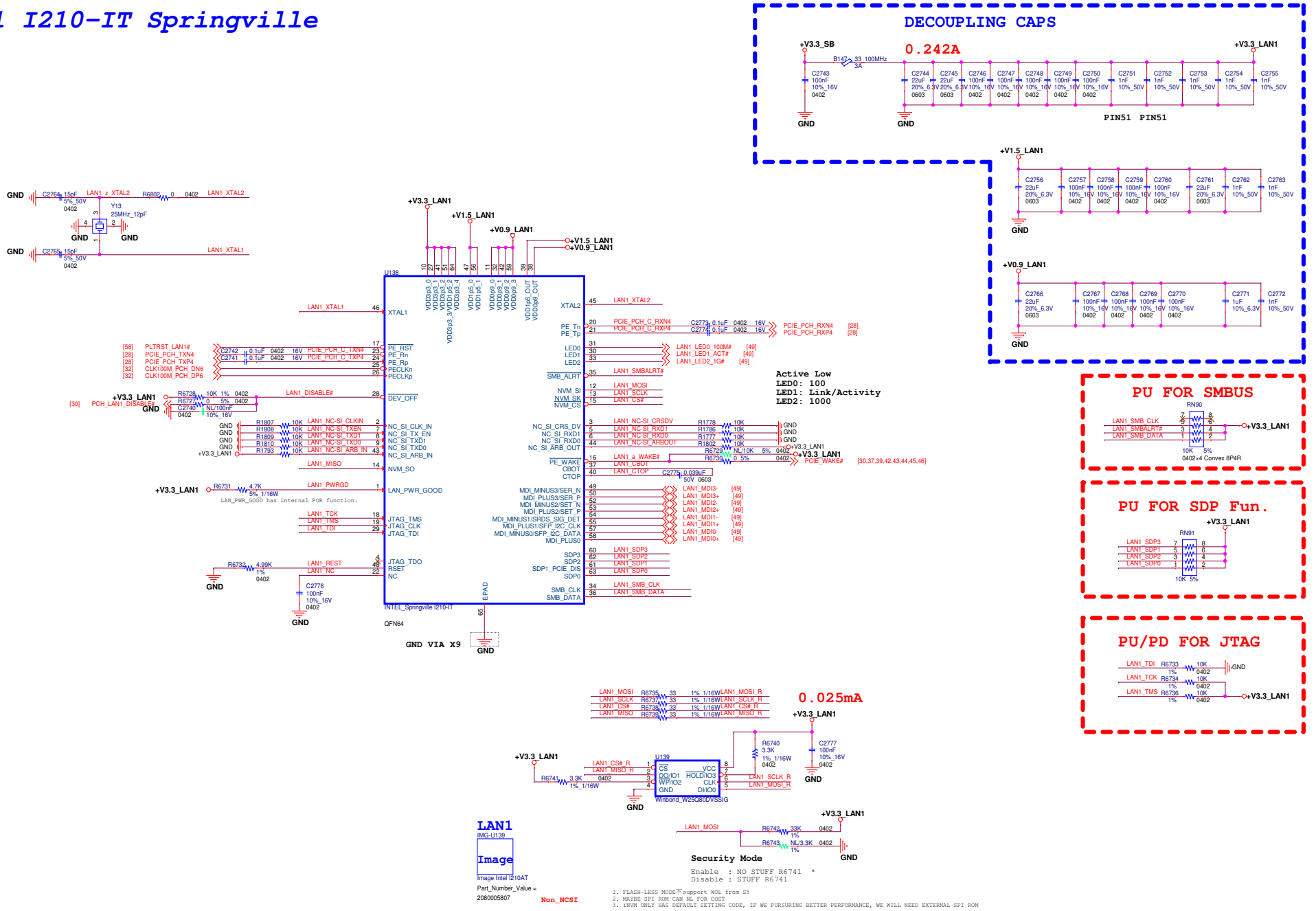
LAN1 I210-IT Springville



ADVANTECH			
Title	41_LAN1 NIC I210IT		
Size	Document Number	AIIS-5410P	Rev A101-4
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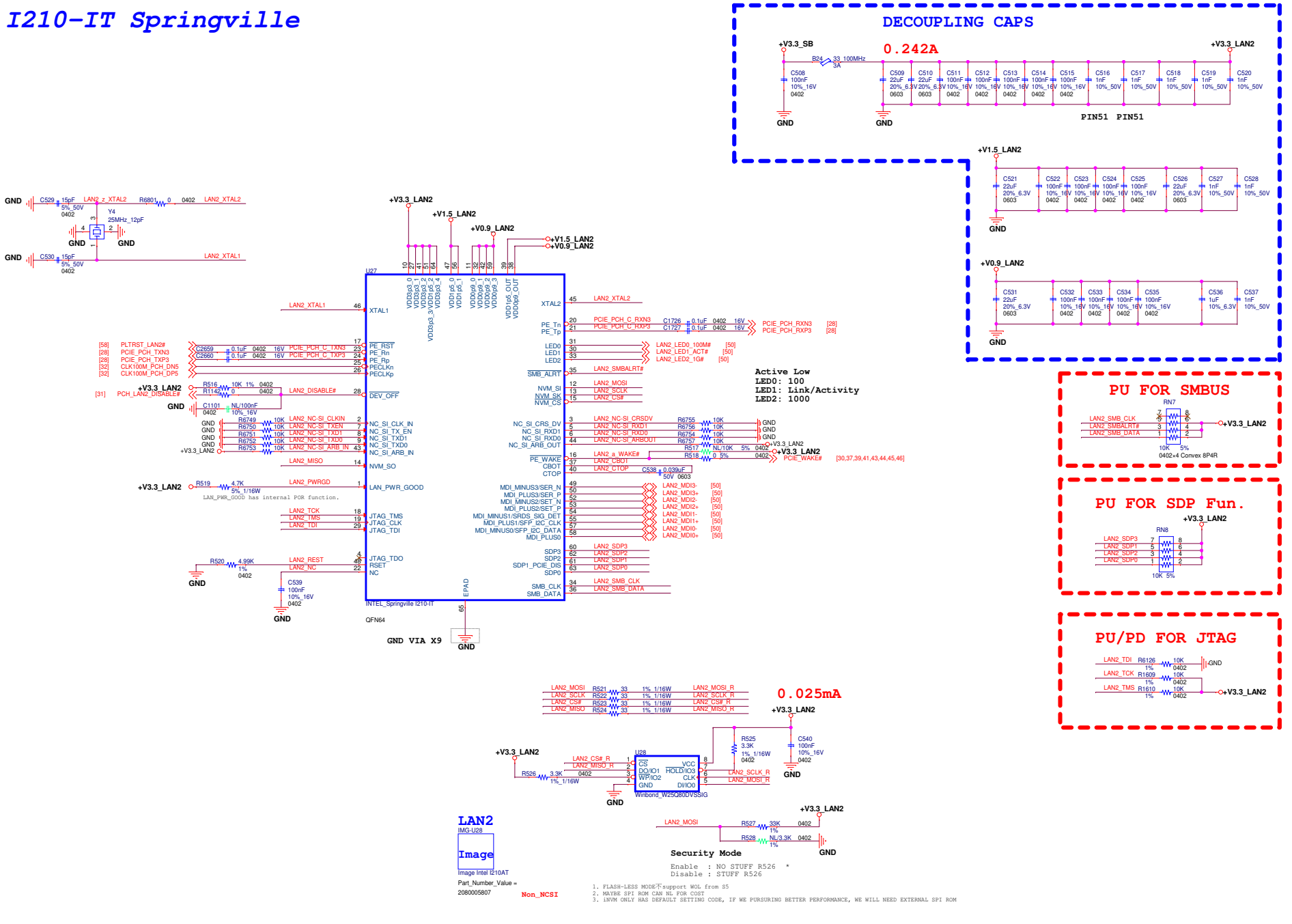
LAN2 I210-IT Springville



ADVANTECH		
Title	42_LAN2 NIC I210IT	
Size	Document Number: AIIS-5410P	Rev: A101-4
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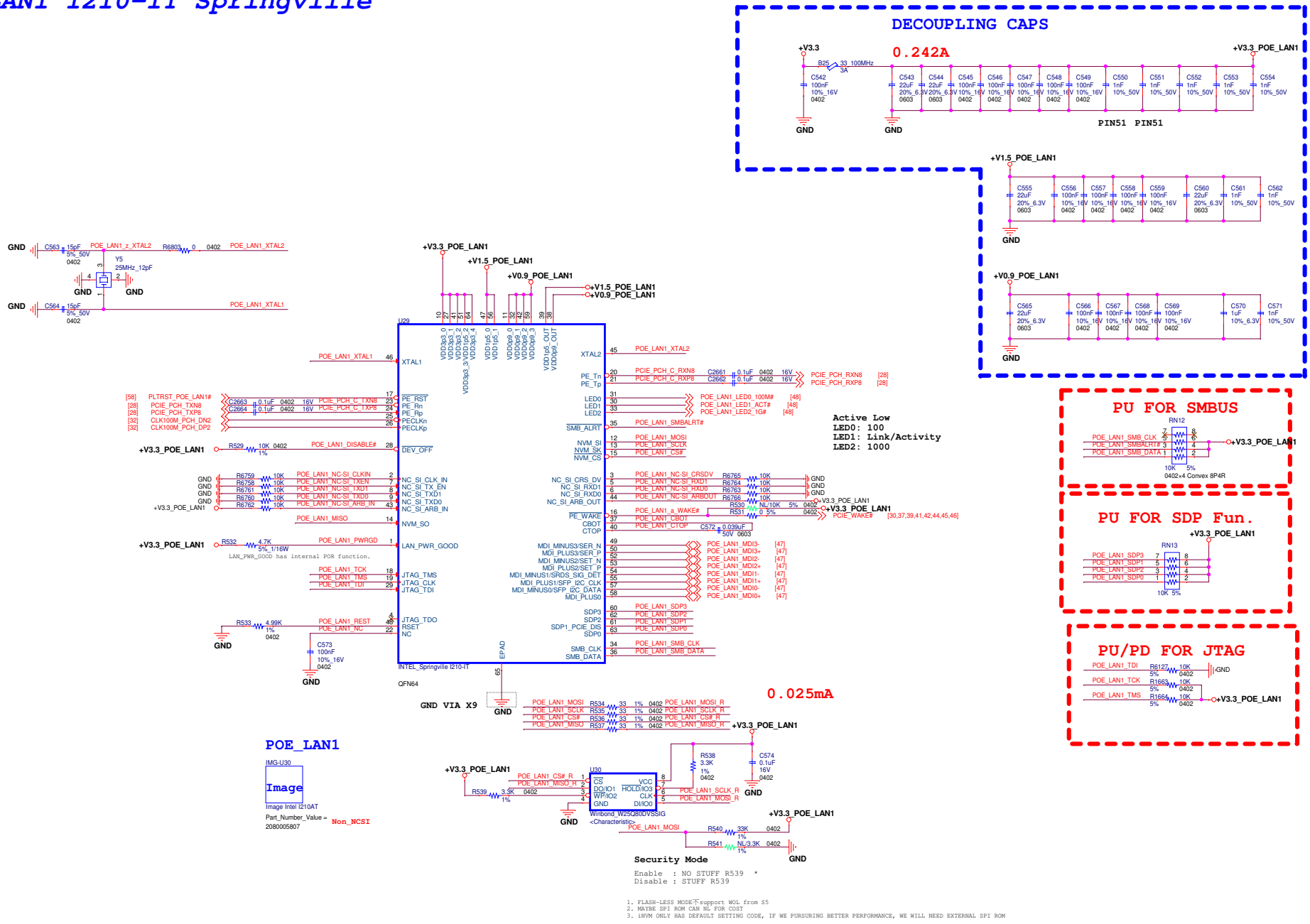
POE_LAN1 I210-IT Springville



ADVANTECH			
Title	43_POE_LAN1 NIC I210IT		
Size	Document Number	AIIS-5410P	Rev A101-4
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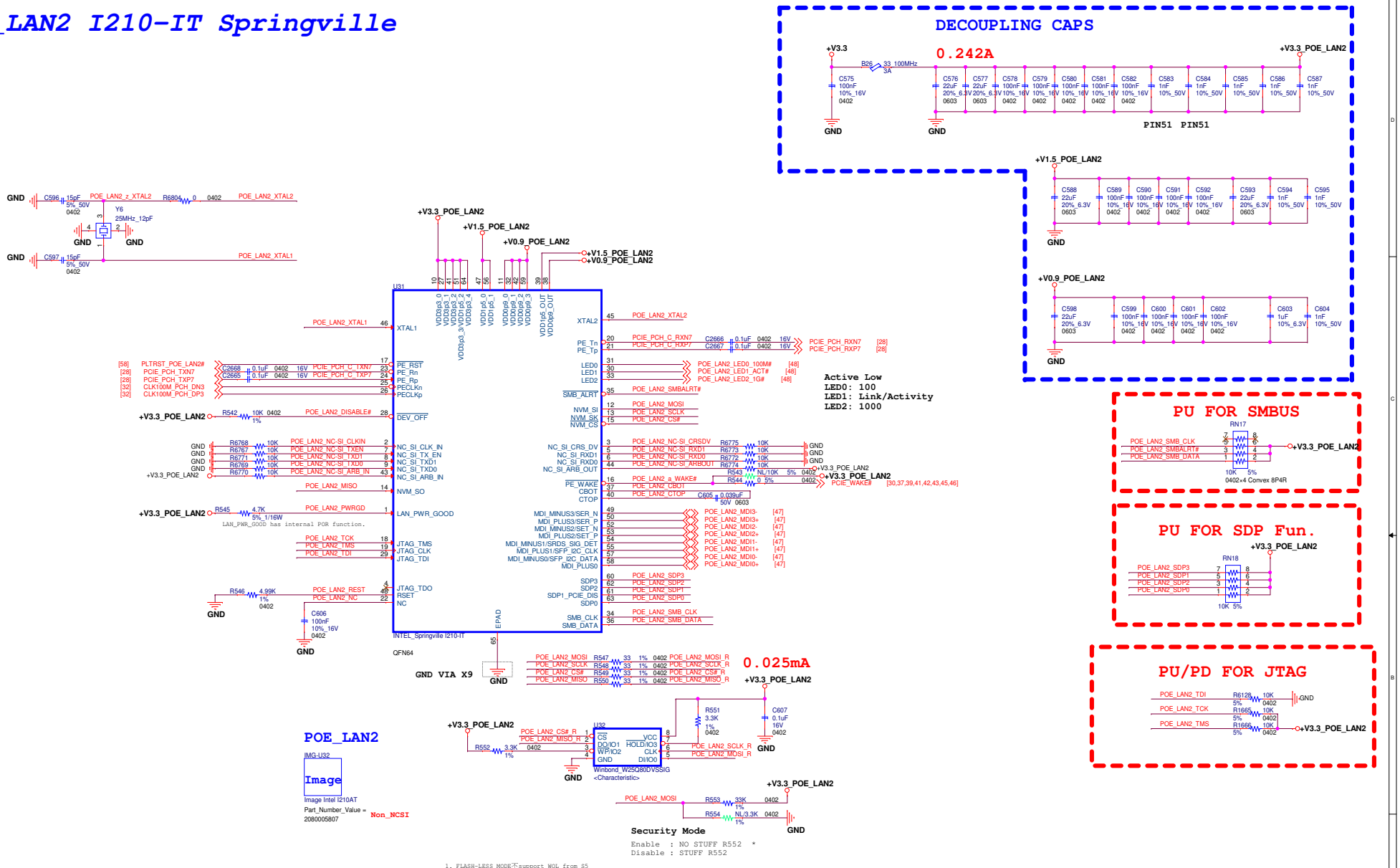
POE_LAN2 I210-IT Springville



ADVANTECH			
Title	44_POE_LAN2 NIC I210IT		
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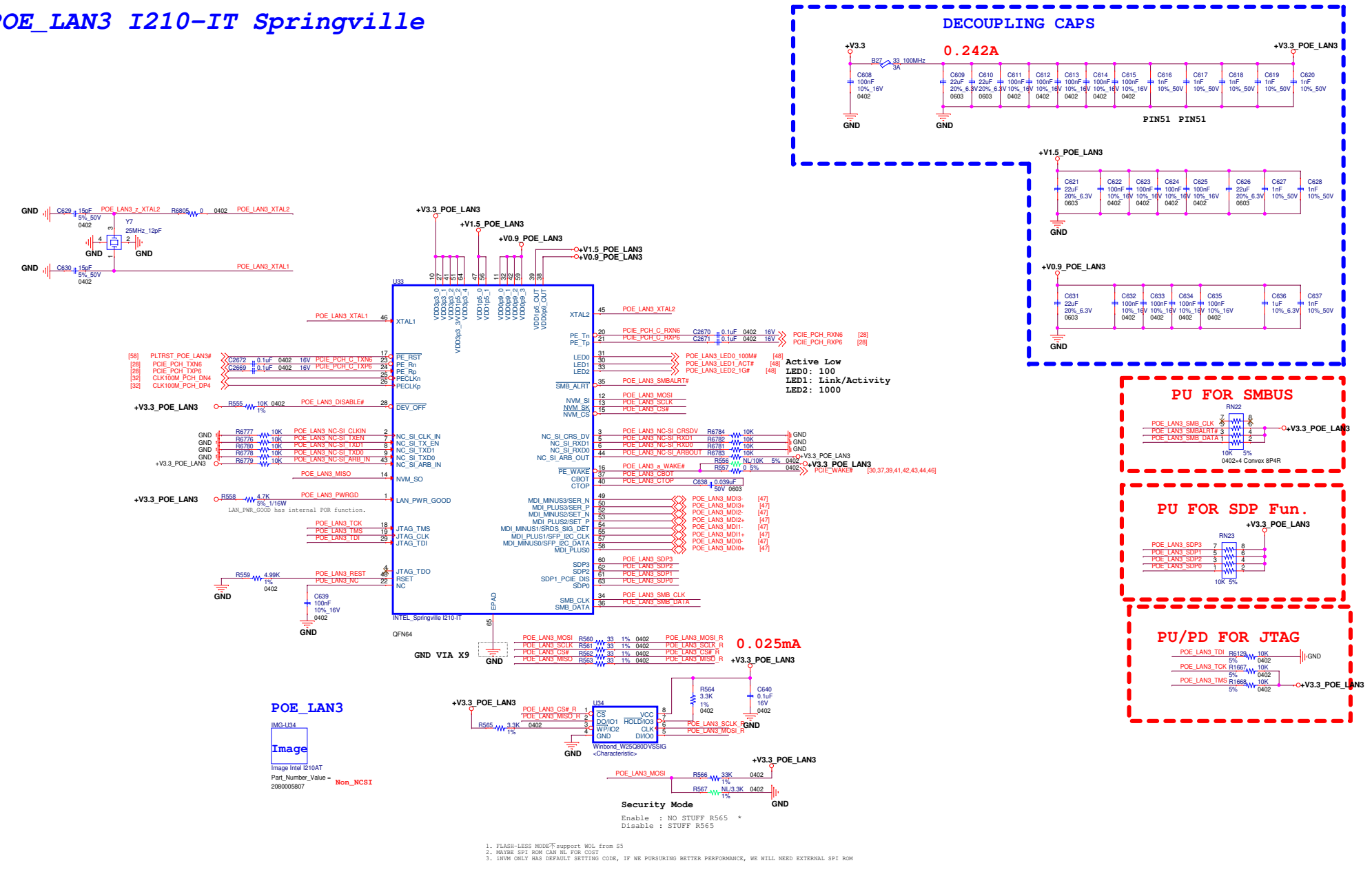
POE_LAN3 I210-IT Springville



ADVANTECH			
Title	45_POE_LAN3 NIC I210IT		
Size	Document Number		Rev
	AIIS-5410P		A101-4
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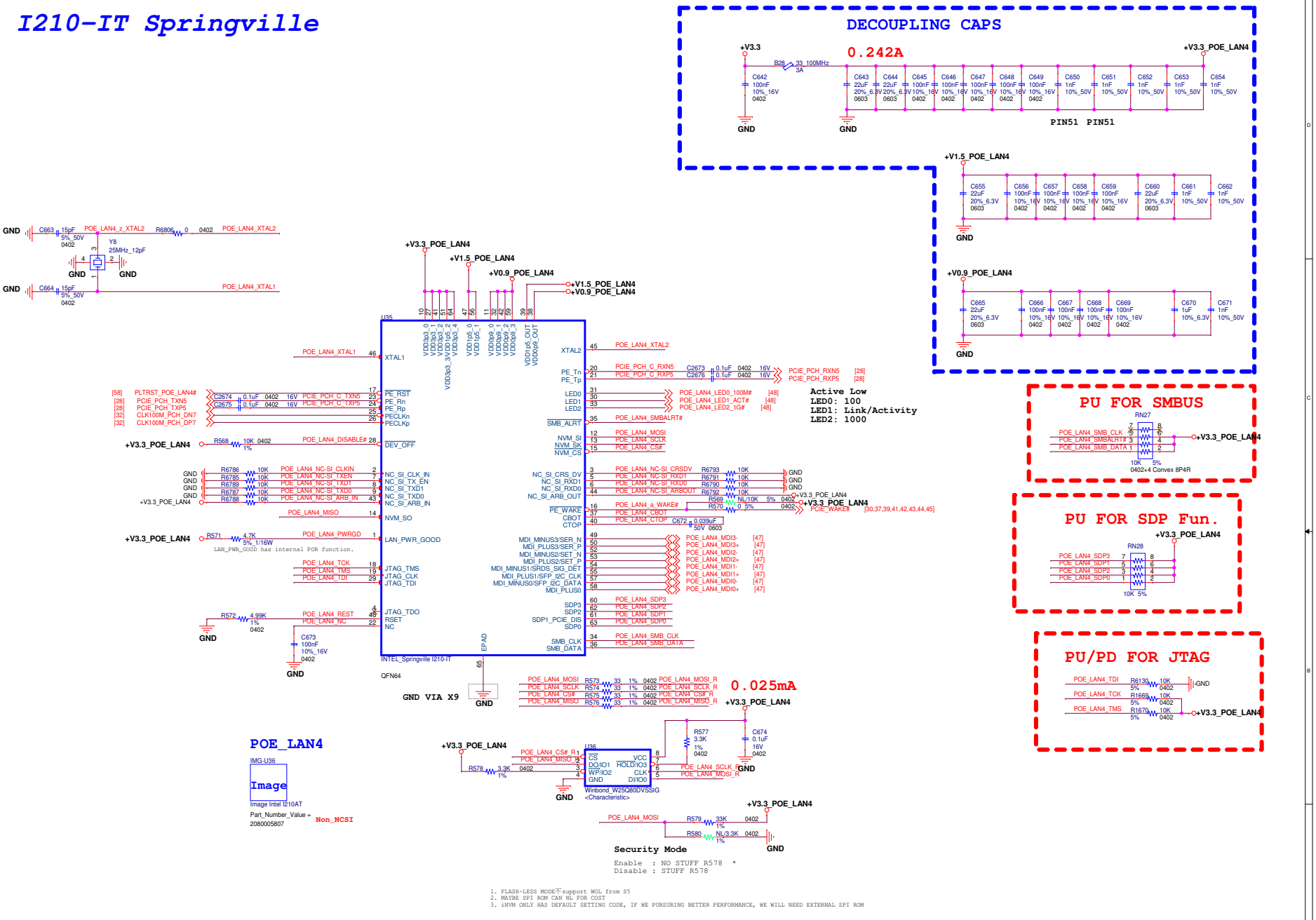
POE_LAN4 I210-IT Springville



ADVANTECH			
Title	46_POE_LAN4 NIC I210IT		
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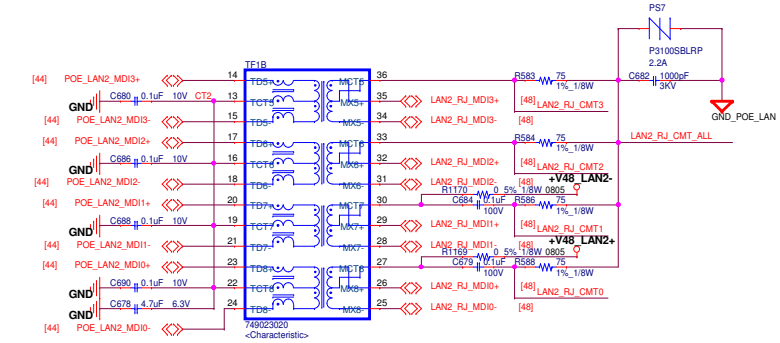
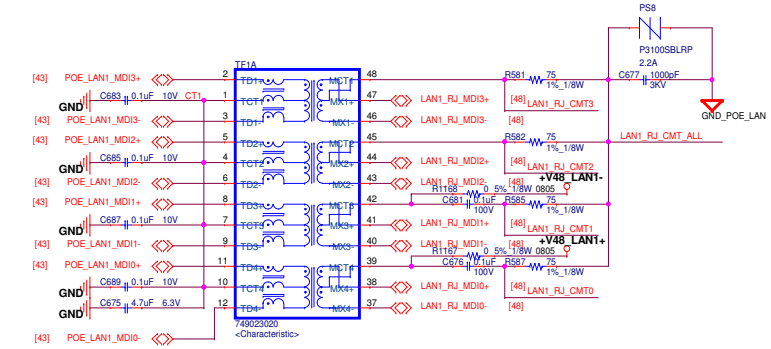
POE_LAN TRANSFORMER

wayne1001: no-isolation BOM & Text-OK

LAN2

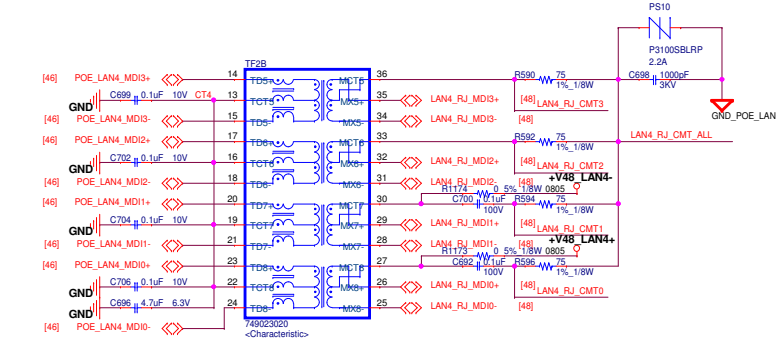


LAN1

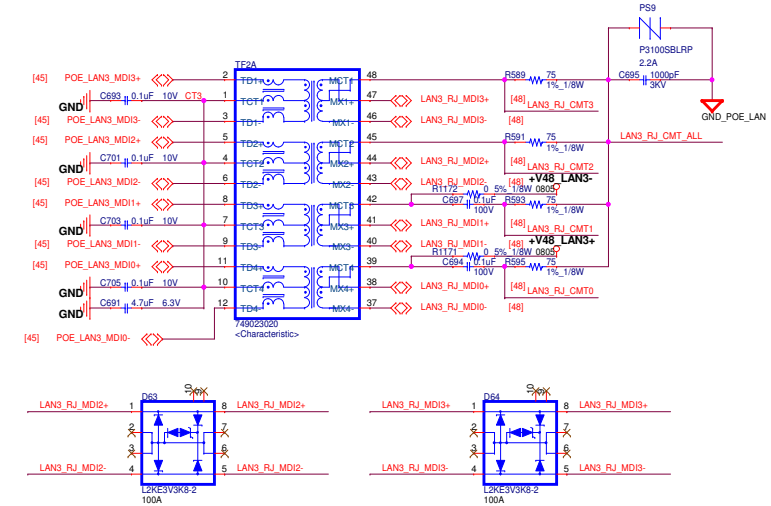


Xfrm in PLM System :
Add 1252002250-01(Wurth/749023020) to main source
Change 1252002198-01 (Pulse/H6080FNL) to Second source

LAN4



LAN3



POE SKU	Stuff	Empty
NON-POE		R1167-R1174 and C676,C681,C679,C684,C694,C697,C692,C700 change to 0 ohm
Support POE	R1167-R1174 C676,C681,C679,C684,C694,C697,C692,C700	

ADVANTECH

Title	47_POE_LAN TRANSFORMER	
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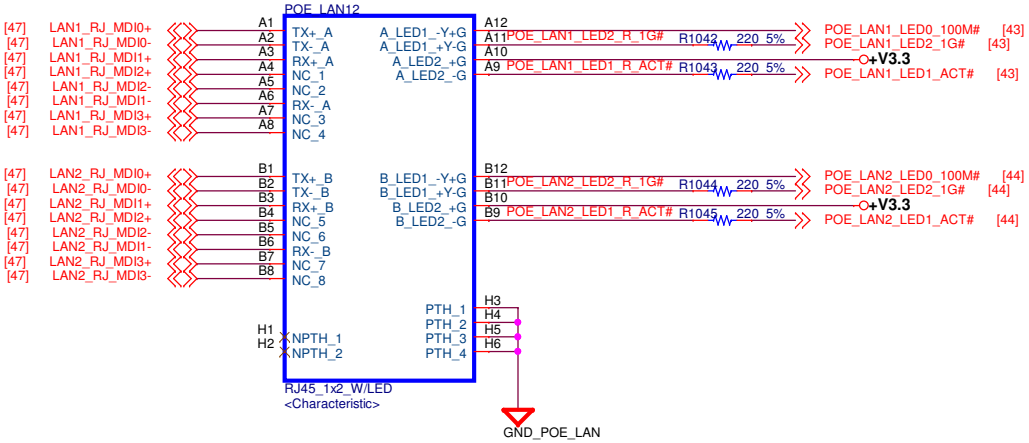
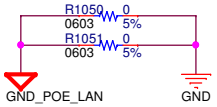
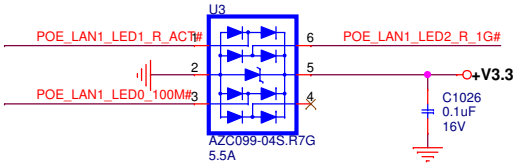
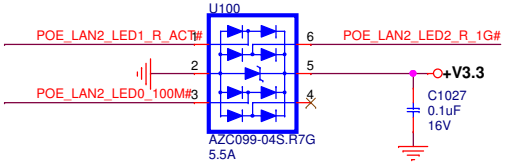
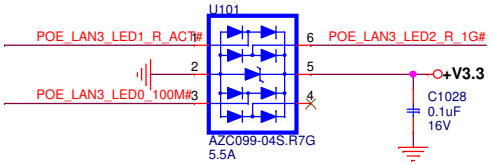
POE_LAN1234 CONN

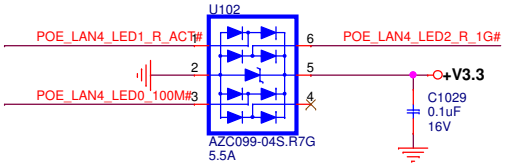


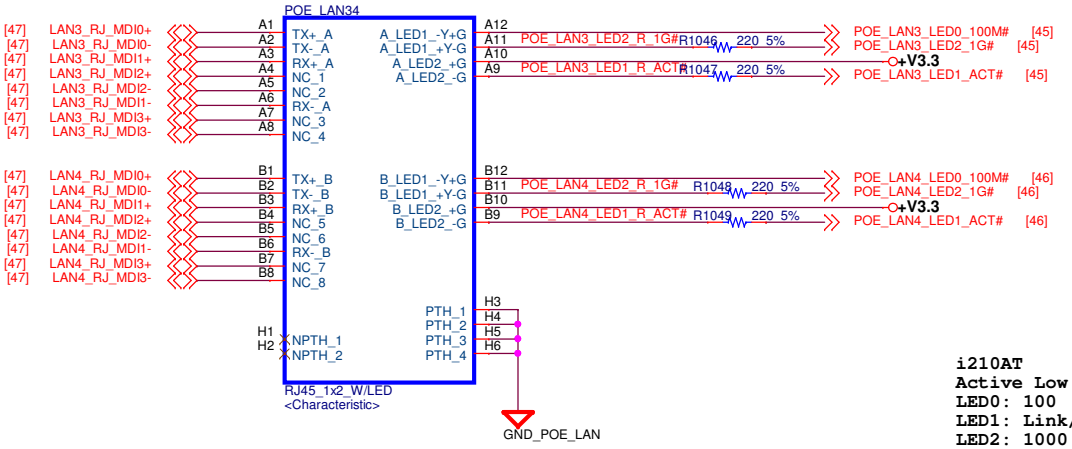












i210AT
Active Low
LED0: 100
LED1: Link/Activity
LED2: 1000

Giga LAN connector
Left Side : Green/Orange LED

Status	Display
10Mbps	Always turn off
100Mbps	Orange
1000Mbps	Green

ADVANTECH

Title	48_CONN_POE_LAN1234	
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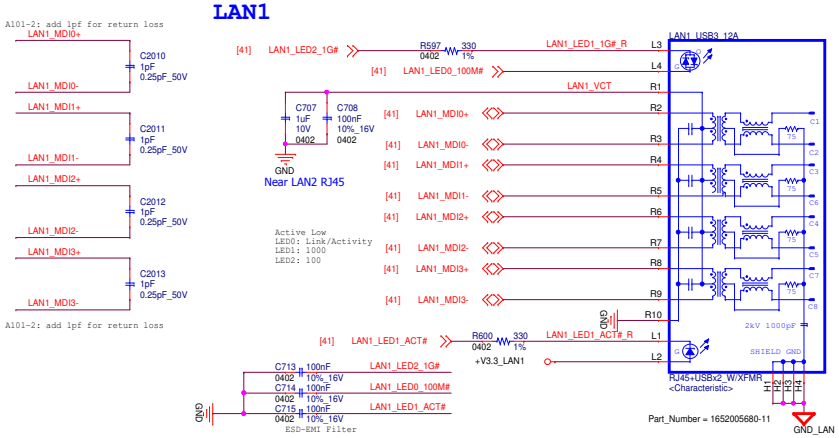
CN [LAN1/USB3.0]

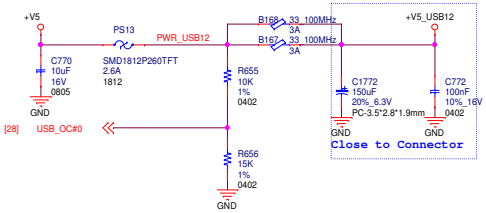
LAN1



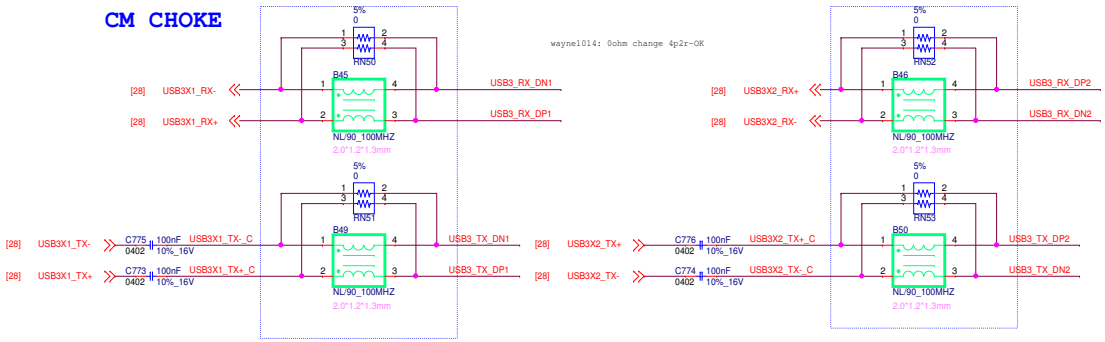
Giga LAN connector Left Side : Green/Orange LED	
Status	Display
10Mbps	Always turn off
100Mbps	Orange
1000Mbps	Green

Right Side : Green LED	
Status	Display
Link status	Always turn on without transmitting/receiving data
Activity status	Flash

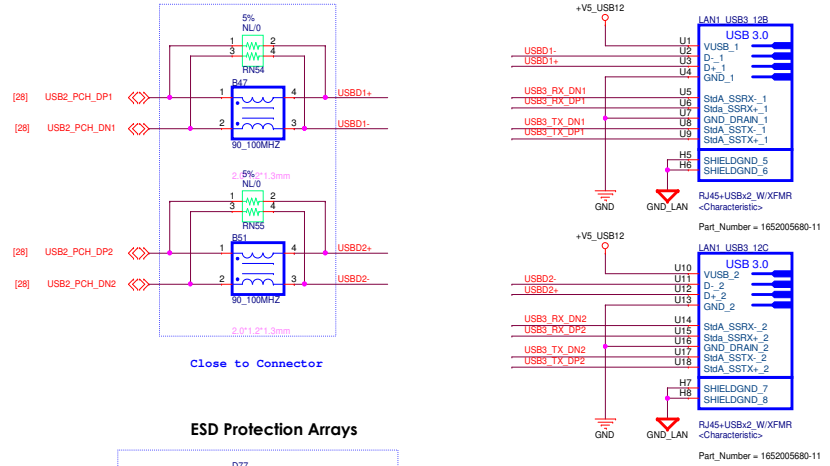
USB POWER



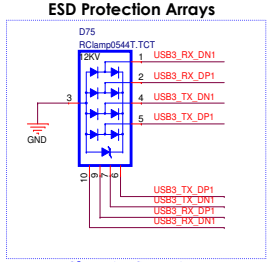
CM CHOKE



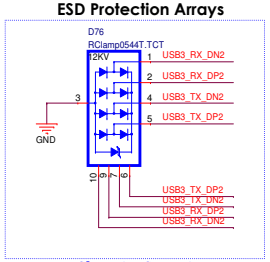
USB PORT 1/2



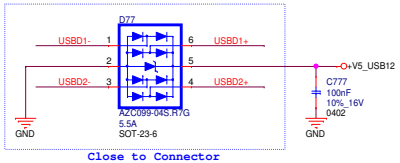
ESD Protection Arrays



ESD Protection Arrays



ESD Protection Arrays



USB2.0 Port 1-2
USB3.0 Port 1-2

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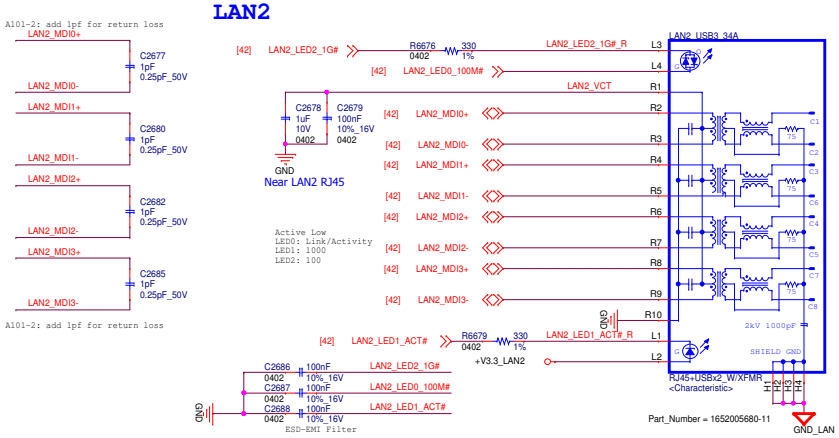
CN [LAN2/USB3.0]

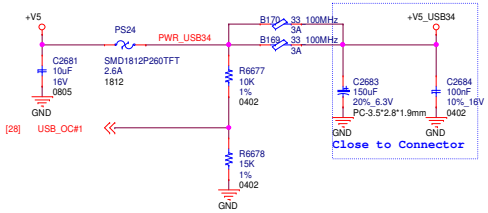
LAN2



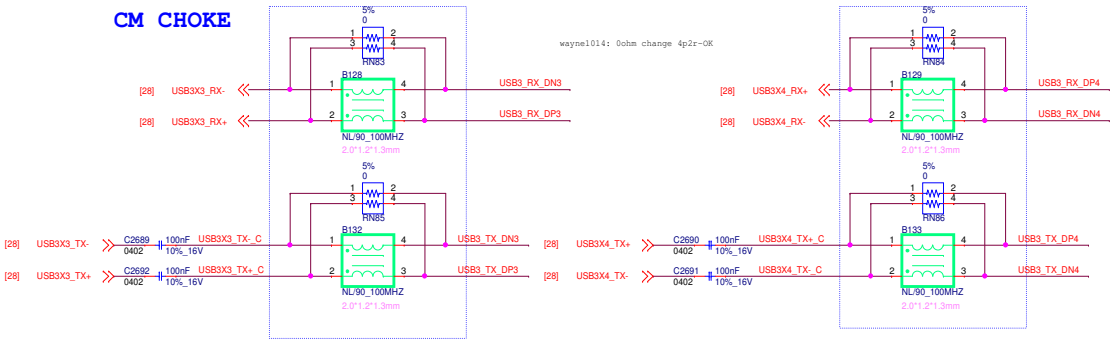
Giga LAN connector Left Side : Green/Orange LED	
Status	Display
10Mbps	Always turn off
100Mbps	Orange
1000Mbps	Green

Right Side : Green LED	
Status	Display
Link status	Always turn on without transmitting/receiving data
Activity status	Flash

USB POWER



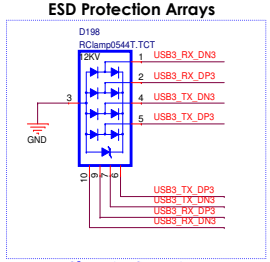
CM CHOKE



Close to Connector

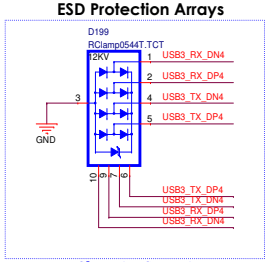
Close to Connector

ESD Protection Arrays



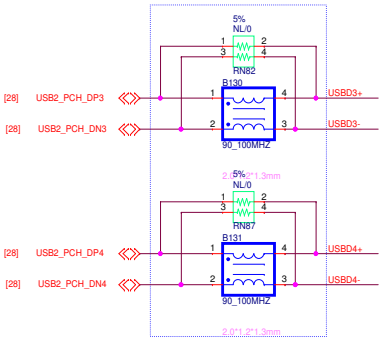
Close to Connector

ESD Protection Arrays



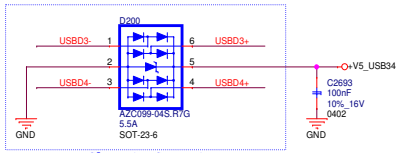
Close to Connector

USB PORT 3/4

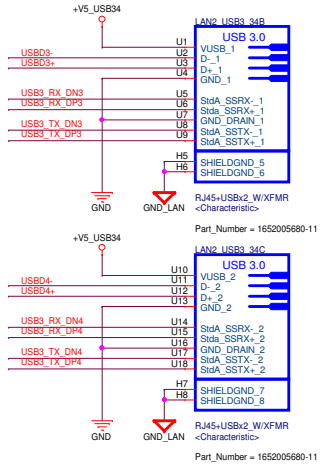


Close to Connector

ESD Protection Arrays



Close to Connector



USB2.0 Port 3-4
USB3.0 Port 3-4

ADVANTECH

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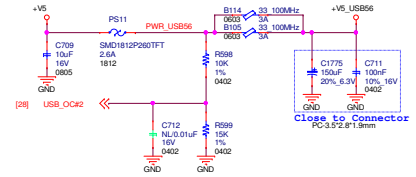
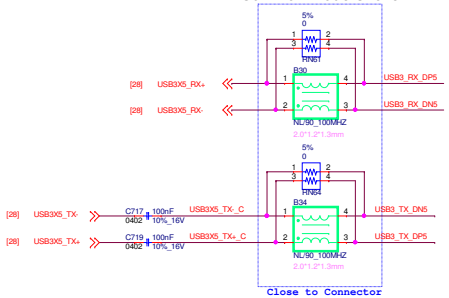
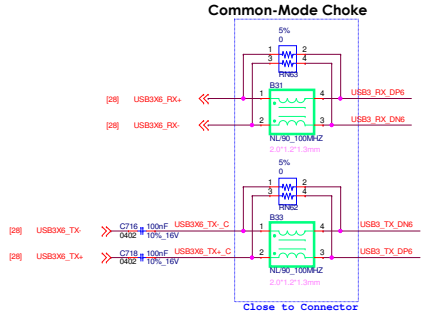
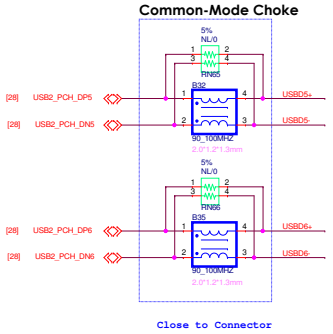
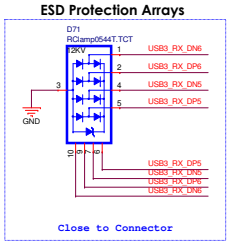
CN [Rear IO USB3.0 X4]

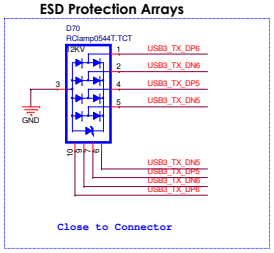


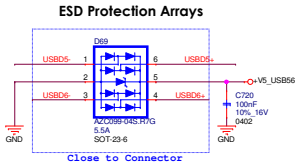


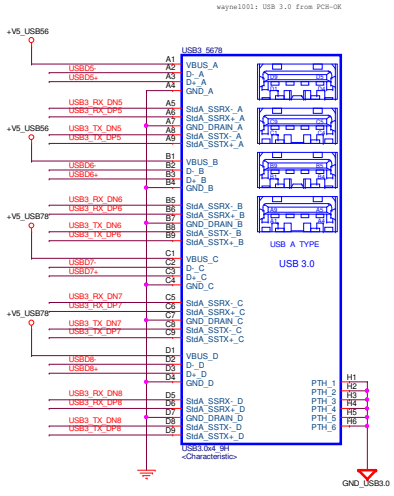


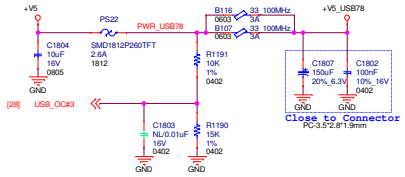


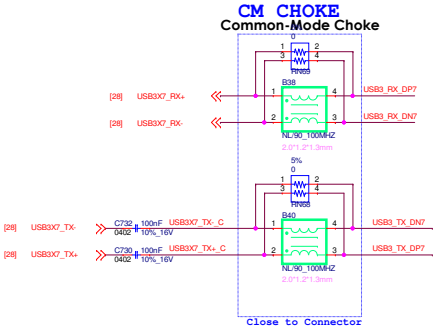


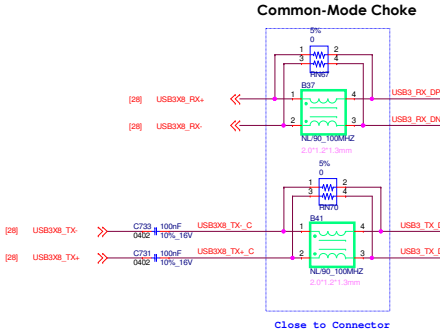


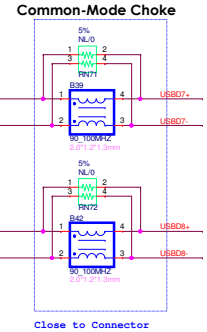


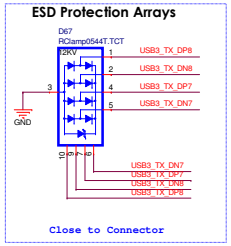


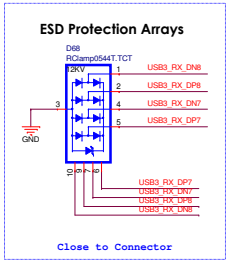


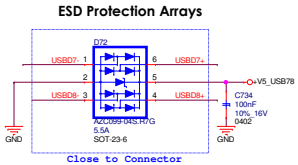












USB2.0 Port 5-6-7-8
USB3.0 Port 5-6-7-8

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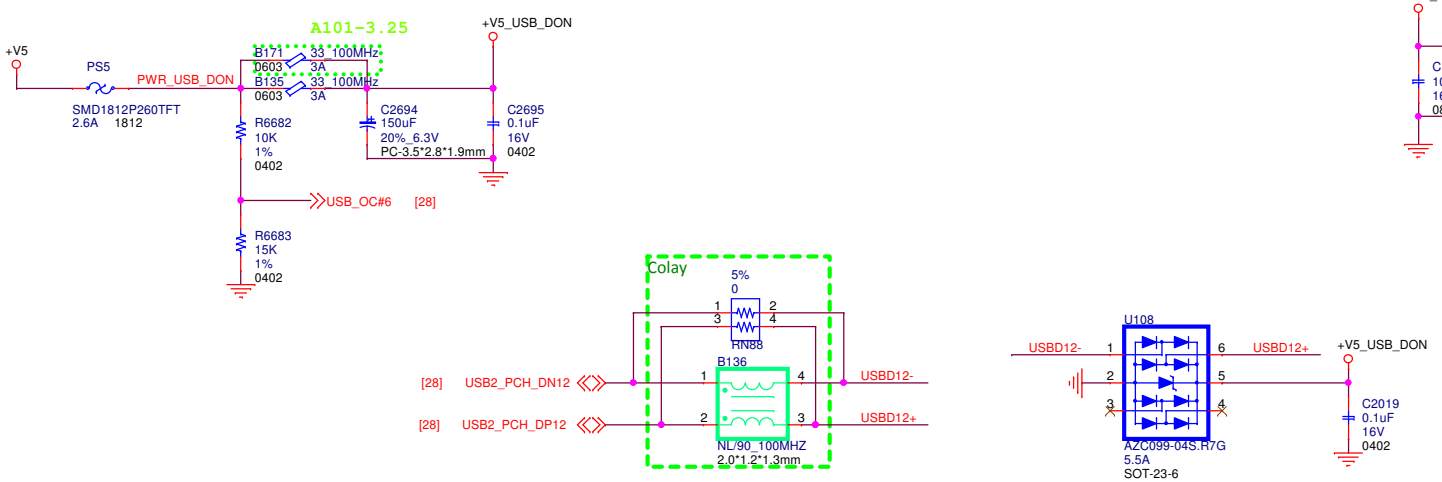
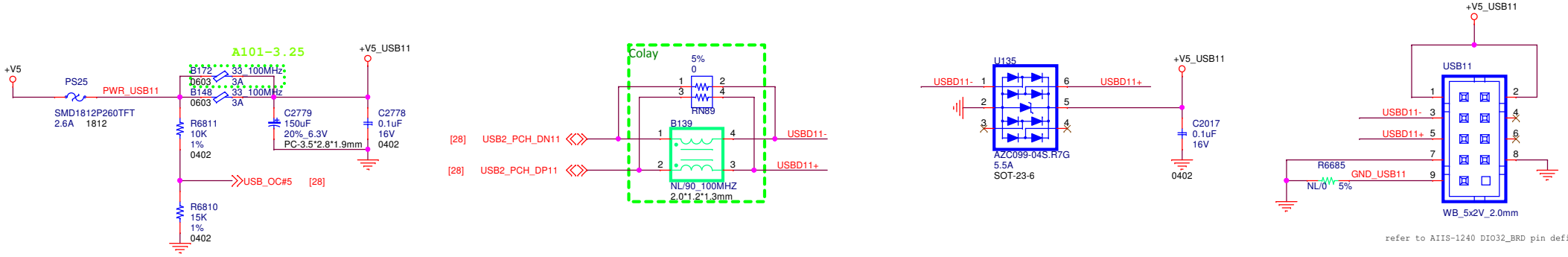
Internal USB2.0 Dongle



Pin Header for Isolation GPIO module



refer to AIIS-1240 DIO32_BRD pin define

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Title	52_CONN_USB2.0	
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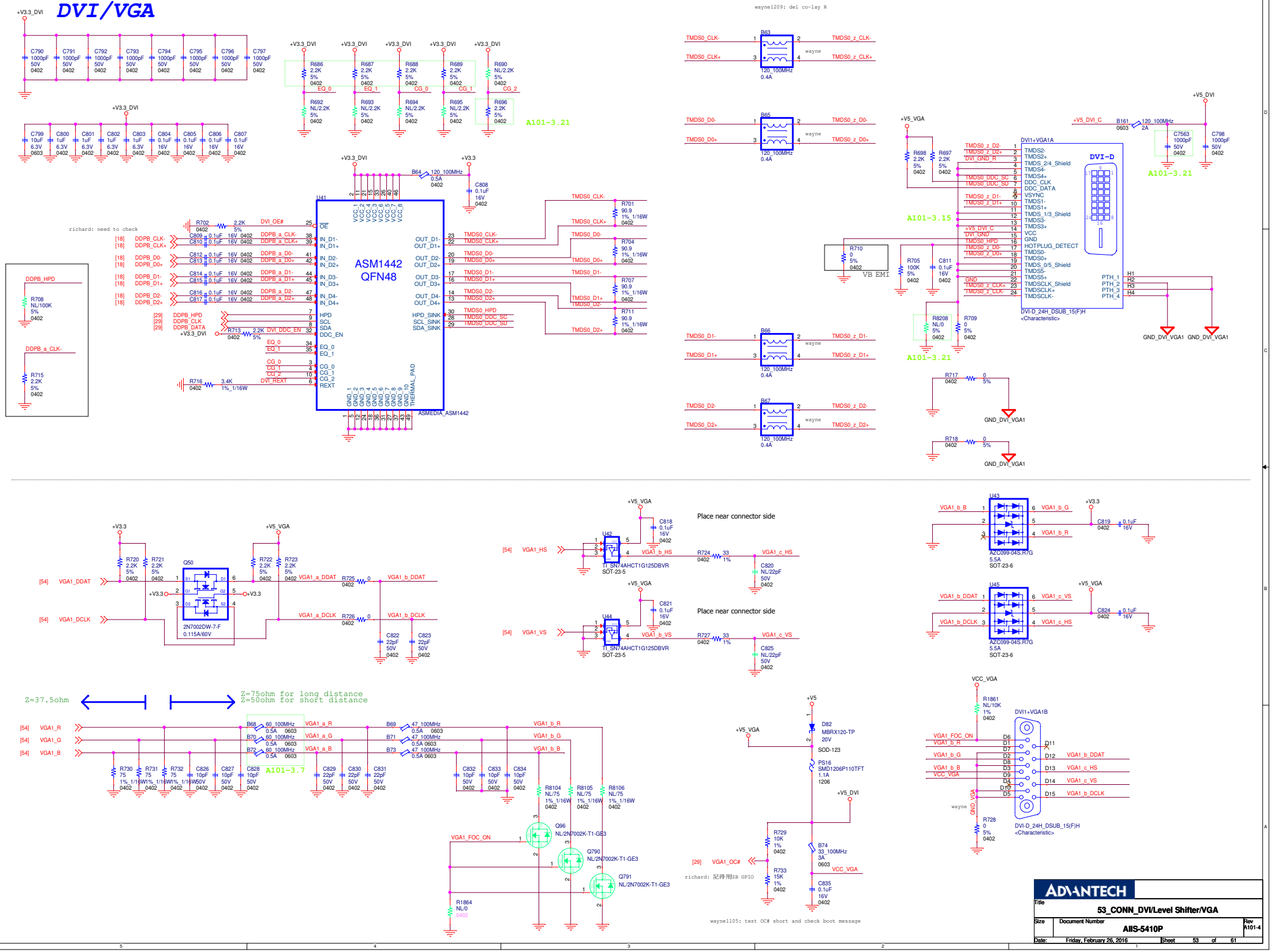
DVI/VGA


wayne1209: del co-lay R
ASM1442
QFN48
ASMEDIA_ASM1442
A101-3.21
A101-3.15
A101-3.7
DVI-D
DVI1+VGA1A
DVI1+VGA1B
DVI-D_24H_DSUB_15(F)H
<Characteristic>
VB EMI
Place near connector side
Z=37.5ohm
Z=75ohm for long distance
Z=50ohm for short distance
richard: need to check
richard: 記得用SB GPIO
wayne1105: test OC# short and check boot message
GND_DVI_VGA1
ADVANTECH
Title
53_CONN_DVI/Level Shifter/VGA
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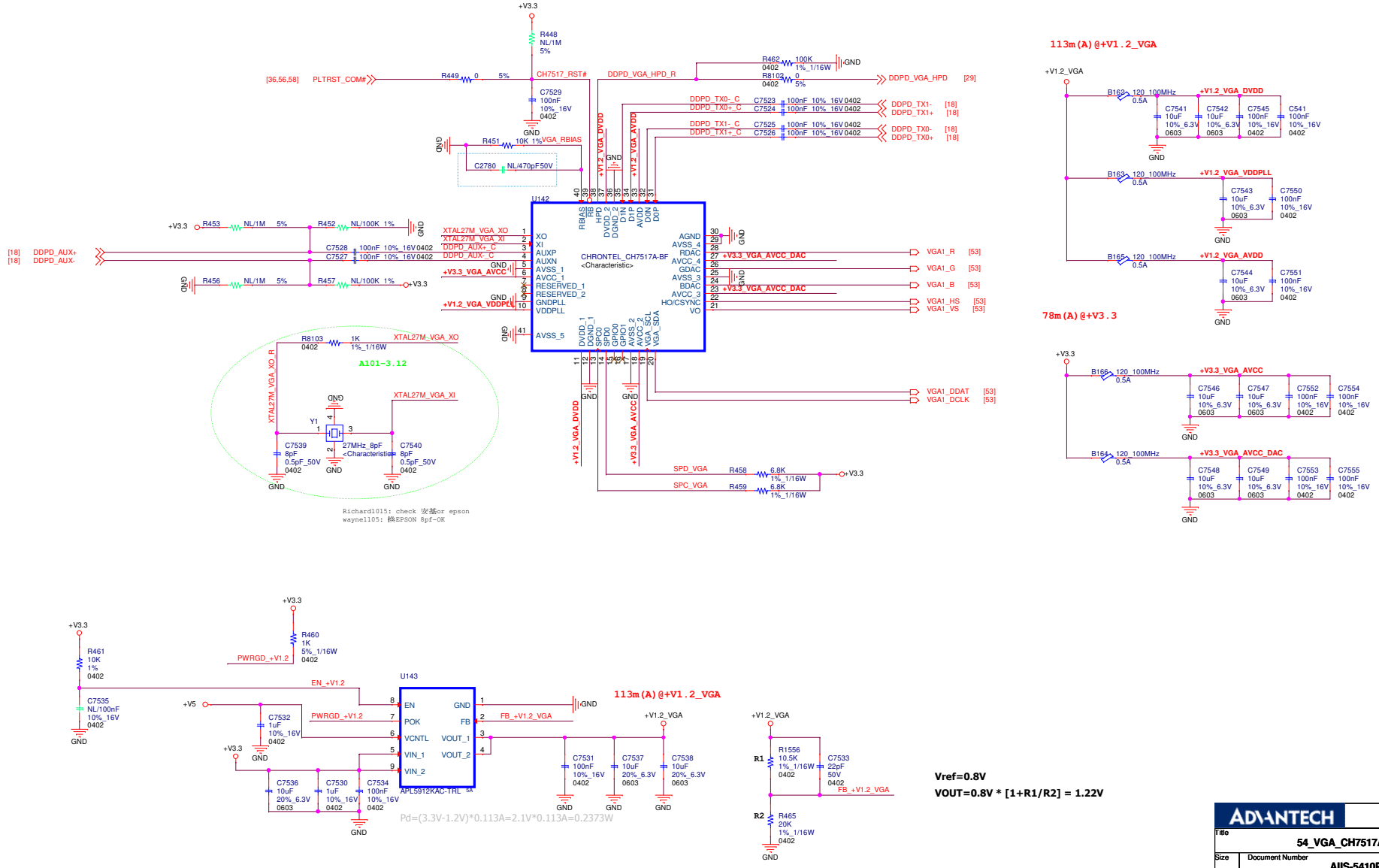
VGA_CH7517



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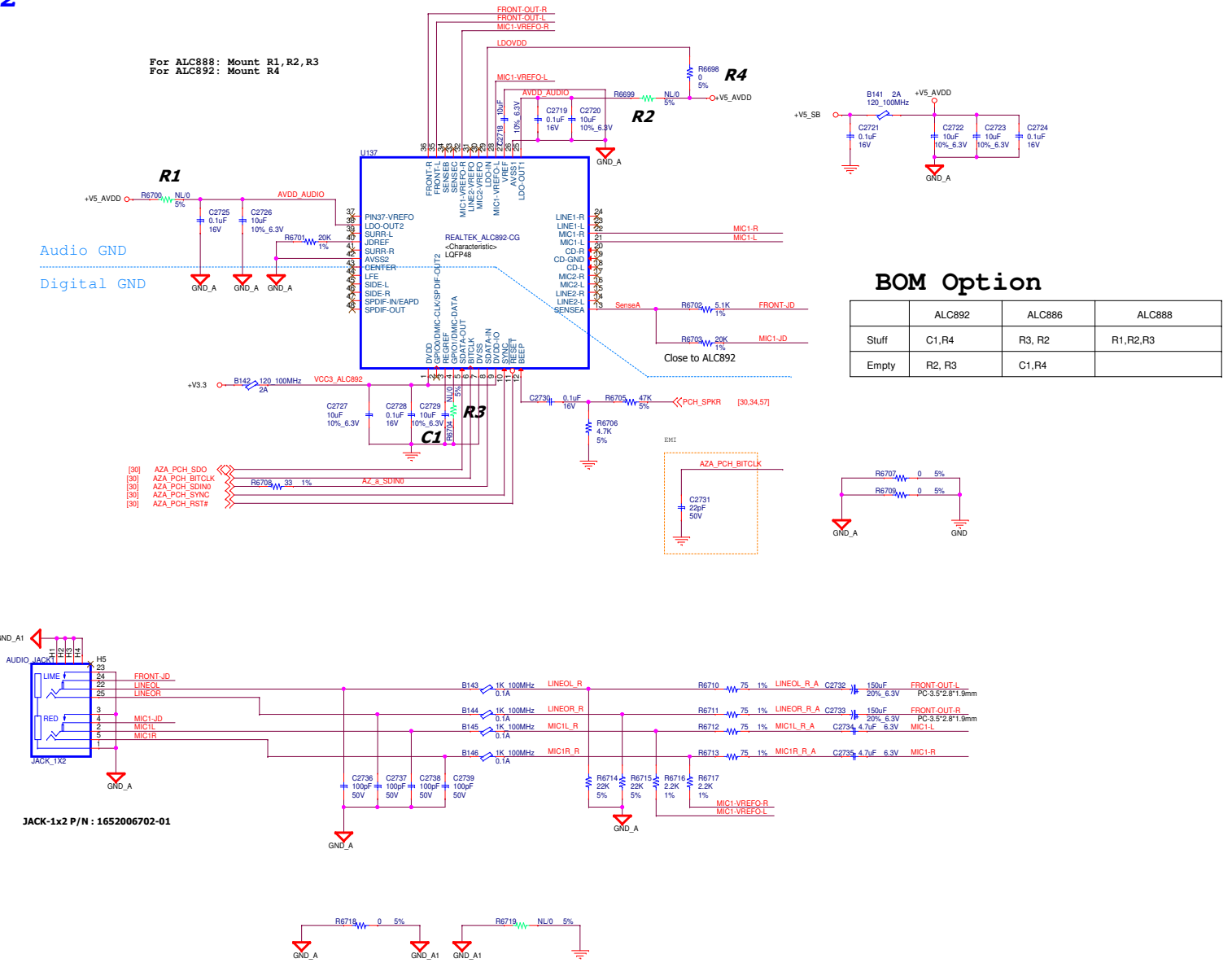
AUDIO ALC892



BOM Option

	ALC892	ALC886	ALC888
Stuff	C1,R4	R3, R2	R1,R2,R3
Empty	R2, R3	C1,R4	

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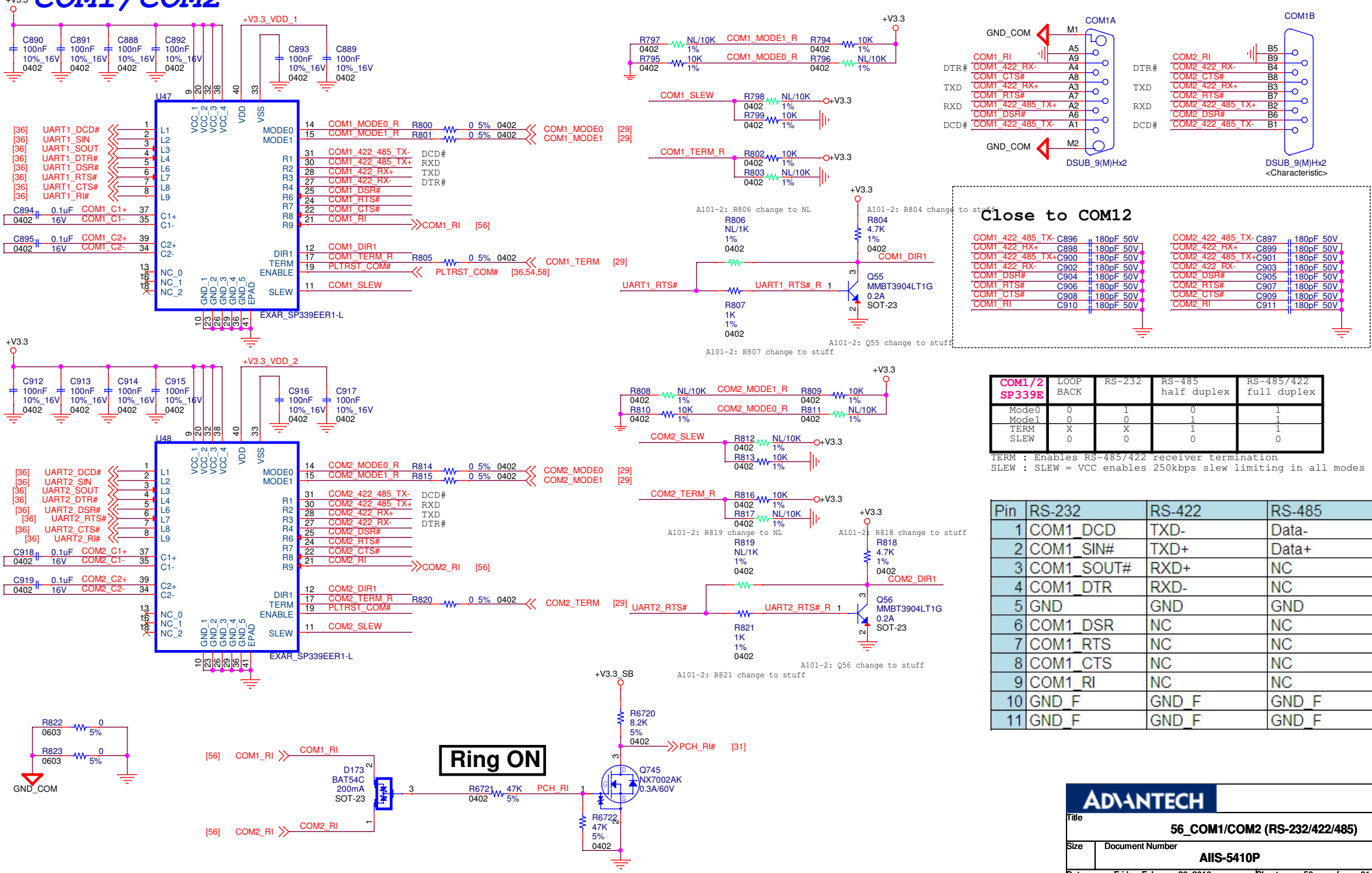
COM1 / COM2



COM1/2 SP339E	LOOP BACK	RS-232	RS-485 half duplex	RS-485/422 full duplex
Mode0	0	1	0	1
Mode1	0	0	1	1
TERM	X	X	1	1
SLEW	0	0	0	0

TERM : Enables RS-485/422 receiver termination
SLEW : SLEW = VCC enables 250kbps slew limiting in all modes

Pin	RS-232	RS-422	RS-485
1	COM1_DCD	TXD-	Data-
2	COM1_SIN#	TXD+	Data+
3	COM1_SOUT#	RXD+	NC
4	COM1_DTR	RXD-	NC
5	GND	GND	GND
6	COM1_DSR	NC	NC
7	COM1_RTS	NC	NC
8	COM1_CTS	NC	NC
9	COM1_RI	NC	NC
10	GND_F	GND_F	GND_F
11	GND_F	GND_F	GND_F

ADVANTECH

Title: 56_COM1/COM2 (RS-232/422/485)

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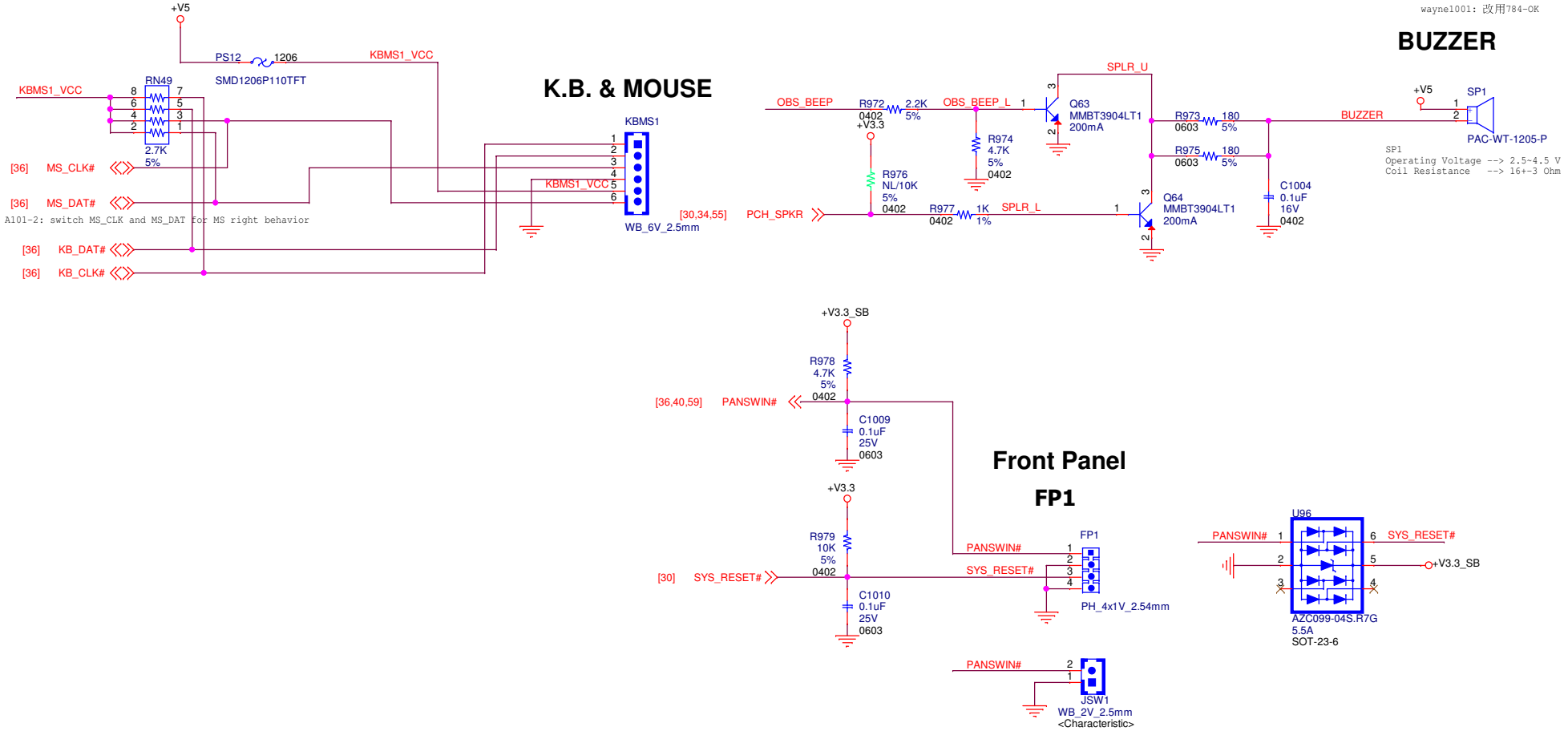
KB&MS/Buzzer/Front Panel



wayne1001: 改用784-OK

ADVANTECH		
Title	57_KB&MS/Buzzer/Front Panel	
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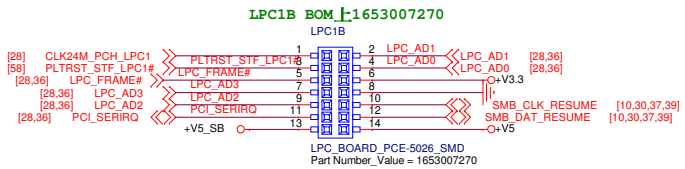
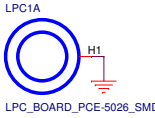
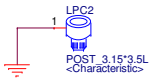
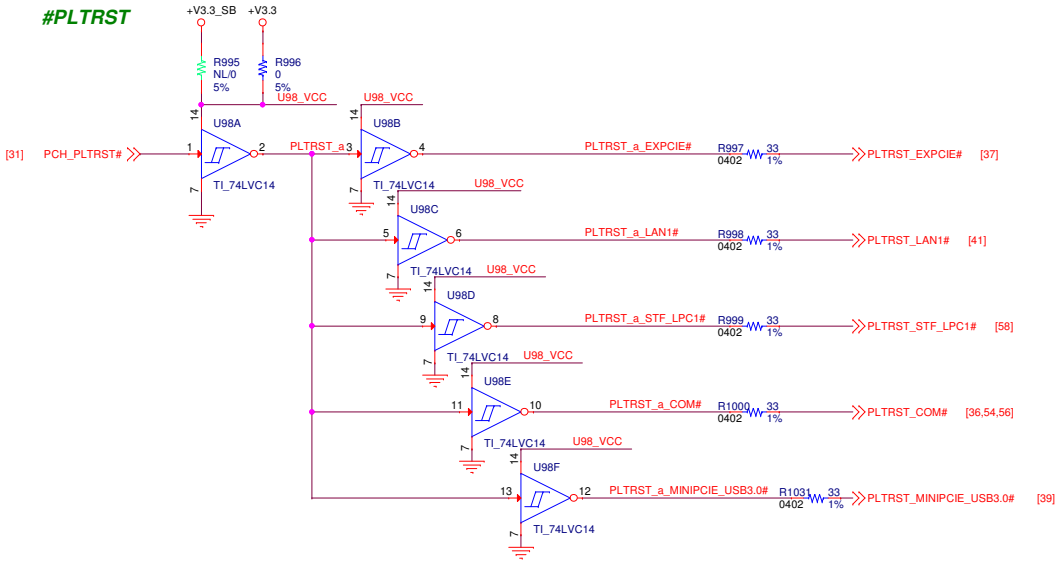
Reset Logic/LPC

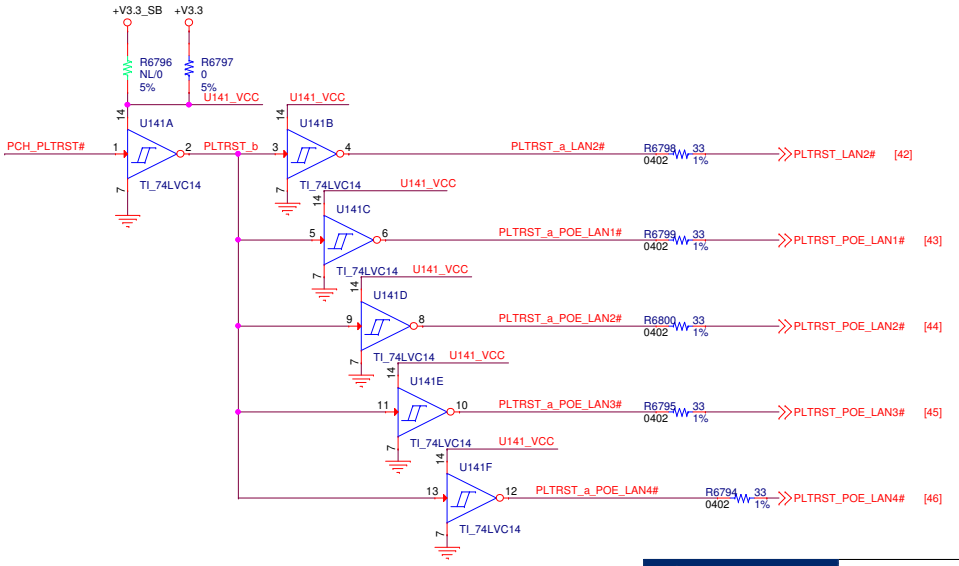






#PLTRST





ADVANTECH

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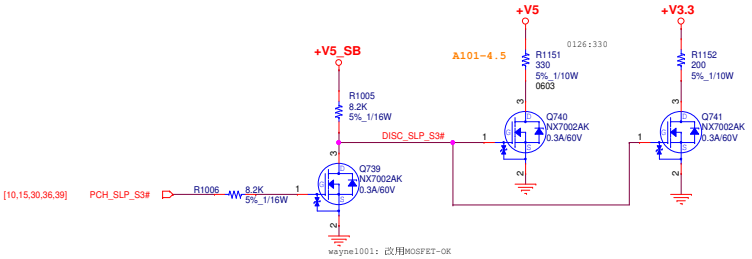
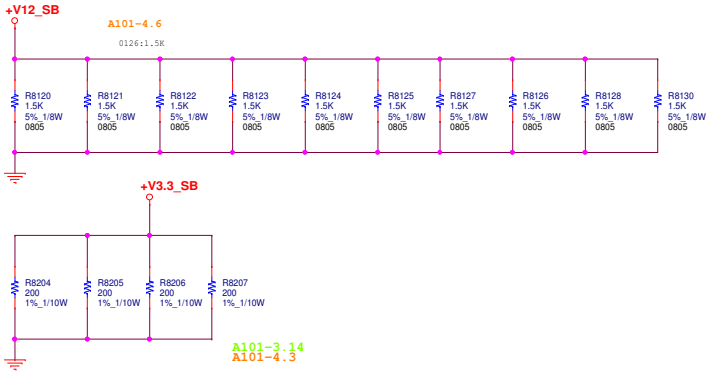
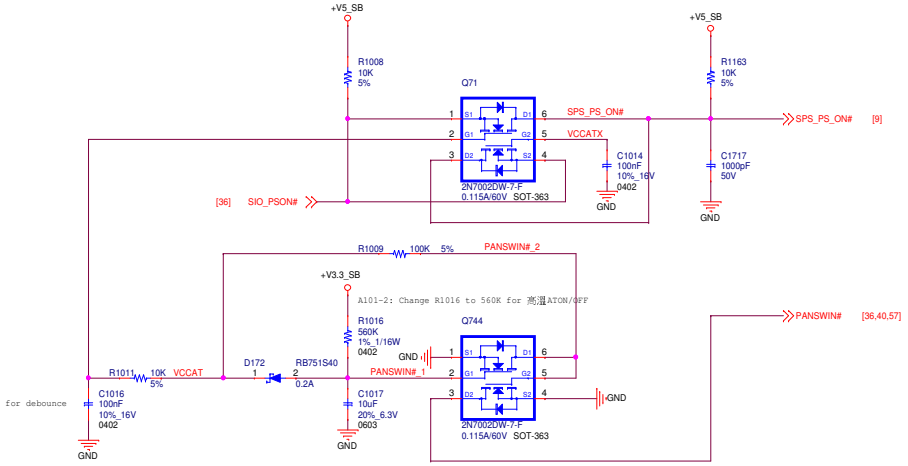
Discharge_AT/ATX Mode

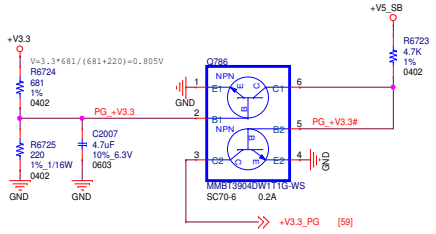
Discharge

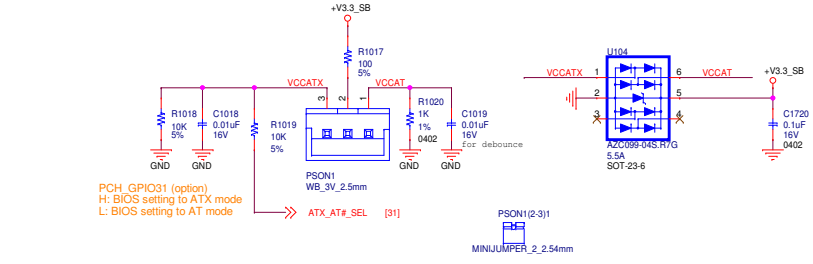


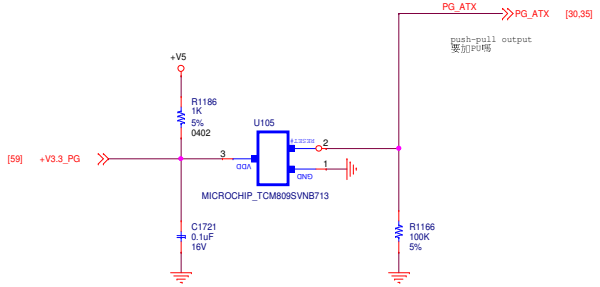


ATX/AT Mode Selection









Mode	Jumper Setting
AT	1-2 Short
ATX	2-3 Short (Default)

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Title	59_Discharge_AT/ATX Mode	
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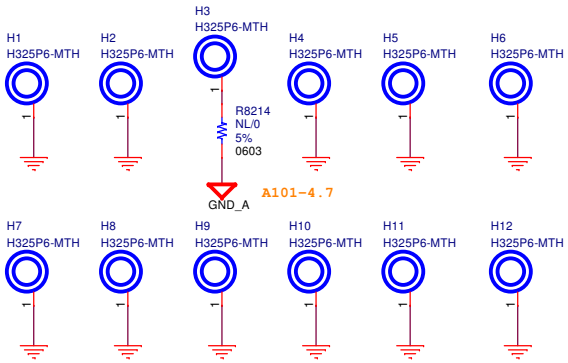

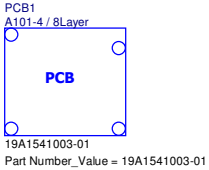

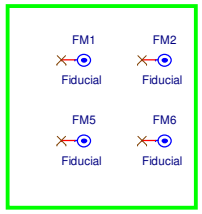

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Title	60_Other BOM	
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Revision History

AIIS-3410P ECOP-101531 A101-1 PCB: 19A13410P0-01 (8 Layer) RD: Richard.Liu 2014/11/27

AIIS-5410P ECOP-107241 A101-2 PCB: 19A1541001-01 (8 Layer) RD: Qx.Wu 2015/08/17

AIIS-5410P ECOP-xxxxxxx A101-3 PCB: 19A1541002-01 (8 Layer) RD: Qx.Wu 2015/10/08

1. POWER: U111 chagne to1410025762-11, Un-stuff C7558(chagne to 0402), R6160, R6162, R6165, R6168, R6171, R6172 change to 750 ohm, R6205, R6208, R6211 -->To update B12 version
2. POWER: C2066 change to 100nF -->To enhance power sense
3. POWER: R8108 chage to 100k, R44 chagne to 470k, Add D201, C7559 -->To decrease inrush curent
4. Sequence: Un-stuff R8113, R8114 -->Multi-pull high
5. Sequence: R6224 chagne to 330k, C2171 change to 0.22uF -->+V2.5_VPP power off delay not enough
6. Sequence: Un-stuff C2555 -->+V12_SB_PG off delay too long
7. VGA: B68, B70, B72 change to 60ohm -->To solve RGB overshoot
8. POWER: R101 change to 750k, R106 change to 1.2k, C127 change to 470pF, R104 change to 0ohm, B4接+V12_SB, Q21, Q22 change to CSD18534, Add R8203 (2 ohm), C7560(2.2 nF) -->POE thermal issue
9. OC: Add C7561, place close to U122 -->Power Surge event when PM enable
10. BOM: CF1 change to 1653005783-01, remove CF2 -->BOM change
11. POWER: Remove R6141, R6142, Add R8209~R8211 -->To solve +V3.3_SB power down at -25℃
12. OSC: R8103 change to 1k -->To optimize crystal
13. BOM: PWRCON1 change to 1655001154 -->PM request
14. POWER: Add R8204~R8207 -->+V3.3_SB dummy loard
15. DVI: DVI1+VGA1 pin4,5,12,13,20,21 link to DVI_GND_R -->DVI EMI
16. SIO: R6604 chagne to 10k ohm -->+VCCGT sense pin current limit
17. POWER: +12V switch change to PMOS -->old solution break down
18. POWER: Add C7562 (100pF) -->To eliminate TPS51125 PG abnormal waveform
19. POWER: C2068 change to 1 uF, C2141 unstuff, Add C7567 -->VRTT change list
20. BOM: SW1 chagne to 1600002840 -->cost down
21. DVI: Stuff R686/R687/R688/R689/R696, Add R8208, C7563 -->EMI
22. RTC: C2566 chagne to 15pF -->RTC timer failed
23. POWER: C2045 change to 47uF -->new spec suggestion
24. Sequence: remove R6253, Add D203 -->leakage Voltage
25. Power: Add B171, B172 -->USB power
26. sequence: Add R8213,unstuff R6190 -->+VCORE_PG have glitch while +V3.3_SB ramp up

AIIS-5410P ECOP-111566 A101-4 PCB: 19A1541003-01 (8 Layer) RD: Richard.Liu 2016/1/27

1. Power: change sunnber connection form gate to phase -->For correct circuit design
2. Sequence: change R6224 from 330k ohm to 560k ohm -->Fix power off sequence tPCH16 timming fail issue
3. Sequence: Stuff R8204,R8205,R8206,R8207 -->fix +V3.3_SB、PCH_RTCRST# and SIO_PWRBTN# waveforms leakage issue
4. Sequence: add Q798 and R8165 -->For better power on sequence
5. Power: change R1151 from 200 ohm to 330 ohm -->For better resistor watt margin
6. Power: change R8120~R8130 from 1.2k ohm to 1.5k ohm -->For better resistor watt margin
7. EMI: add R8214 -->Reserve for EMI test

AIIS-5410P ECOM-116059 A101-4 PCB: 19A1541003-01 (8 Layer) RD: Richard.Liu 2016/1/27

1. change NUT1,NUT2 to 1910002436-02-->For replace P/N
2. Update BIOS to Final version to 1420038696-->For Final BIOS version

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