Cover page

Model Name:MIC-7700 A101-2

Version:	A101-2	PCB P/N:	19A1770001-01	Update Date:	2016/6/6

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Title	01_Cover page	
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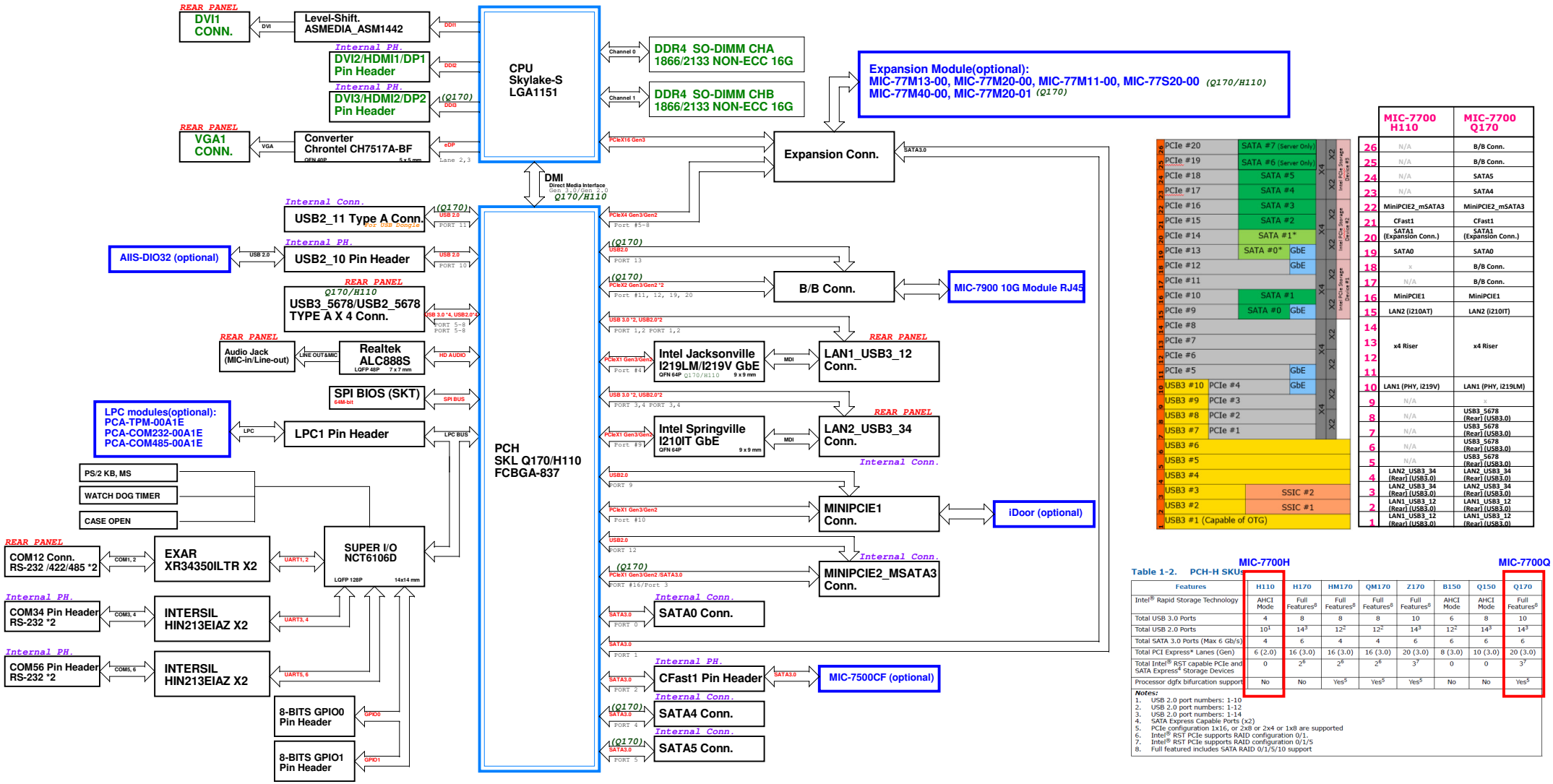
Block Diagram

MIC-7700 A101-2



	MIC-7700 H110	MIC-7700 Q170
26	N/A	B/B Conn.
25	N/A	B/B Conn.
24	N/A	SATA5
23	N/A	SATA4
22	MiniPCIE2_mSATA3	MiniPCIE2_mSATA3
21	CFast1	CFast1
20	SATA1 (Expansion Conn.)	SATA1 (Expansion Conn.)
19	SATA0	SATA0
18	x	B/B Conn.
17	N/A	B/B Conn.
16	MiniPCIE1	MiniPCIE1
15	LAN2 (i210AT)	LAN2 (i210IT)
14	x4 Riser	x4 Riser
13		
12		
11		
10	LAN1 (PHY, i219V)	LAN1 (PHY, i219LM)
9	N/A	x
8	N/A	USB3_5678 (Rear) (USB3.0)
7	N/A	USB3_5678 (Rear) (USB3.0)
6	N/A	USB3_5678 (Rear) (USB3.0)
5	N/A	USB3_5678 (Rear) (USB3.0)
4	LAN2_USB3_34 (Rear) (USB3.0)	LAN2_USB3_34 (Rear) (USB3.0)
3	LAN2_USB3_34 (Rear) (USB3.0)	LAN2_USB3_34 (Rear) (USB3.0)
2	LAN1_USB3_12 (Rear) (USB3.0)	LAN1_USB3_12 (Rear) (USB3.0)
1	LAN1_USB3_12 (Rear) (USB3.0)	LAN1_USB3_12 (Rear) (USB3.0)

Table 1-2. PCH-H SKUs

Features	MIC-7700H H110	H170	HM170	QM170	Z170	B150	Q150	MIC-7700Q Q170
Intel® Rapid Storage Technology	AHCI Mode	Full Features[8]	Full Features[8]	Full Features[8]	Full Features[8]	AHCI Mode	AHCI Mode	Full Features[8]
Total USB 3.0 Ports	4	8	8	8	10	6	8	10
Total USB 2.0 Ports	10[1]	14[3]	12[2]	12[2]	14[3]	12[2]	14[3]	14[3]
Total SATA 3.0 Ports (Max 6 Gb/s)	4	6	4	4	6	6	6	6
Total PCI Express* Lanes (Gen)	6 (2.0)	16 (3.0)	16 (3.0)	16 (3.0)	20 (3.0)	8 (3.0)	10 (3.0)	20 (3.0)
Total Intel® RST capable PCIe and SATA Express[4] Storage Devices	0	2[6]	2[6]	2[6]	3[7]	0	0	3[7]
Processor dgfx bifurcation support	No	No	Yes[5]	Yes[5]	Yes[5]	No	No	Yes[5]

Notes:
1. USB 2.0 port numbers: 1-10
2. USB 2.0 port numbers: 1-12
3. USB 2.0 port numbers: 1-14
4. SATA Express Capable Ports (x2)
5. PCIe configuration 1x16, or 2x8 or 2x4 or 1x8 are supported
6. Intel® RST PCIe supports RAID configuration 0/1.
7. Intel® RST PCIe supports RAID configuration 0/1/5
8. Full featured includes SATA RAID 0/1/5/10 support

MODEL IO LIST

Orcad BOM	CPU	PCH	MEMORY SUPPORT	VGA1	DVI1	DP1/DVI2 (Cable)	DP2/DVI3 (Cable)	LAN1	LAN2	COM (Cable)	COM	GPIO (Cable)	USB2.0 (Conn.)	USB2.0 (Conn.)	USB2.0/USB3.0	SATA3.0 (Conn.)	MINIPCIE/mSATA (Conn.)	LPC (Conn.)	Expansion Conn. (Conn.)	B/B Conn. (Conn.)	Audio	CFast (Conn.)
Part_Number_Value	Skylake-S	PCH -H	DDR4 SO-DIMM 1866/2133 NON-ECC	CH7517A-BF	ASM1442	1	1	Intel I219LM	Intel I210IT	RS-232 *4	RS-232/422/485 *2	2	1	1	0/4+2+2	3	2/0 or 1/1	1	1	1	MIC-in/ Line-out	1
Part_Number_7700Q	Skylake-S	Q170	DDR4 SO-DIMM 1866/2133 NON-ECC	CH7517A-BF	ASM1442	1	1	Intel I219LM	Intel I210IT	RS-232 *4	RS-232/422/485 *2	2	1	1	0/4+2+2	3	2/0 or 1/1	1	1	1	MIC-in/ Line-out	1
Part_Number_7700H	Skylake-S	H110	DDR4 SO-DIMM 1866/2133 NON-ECC	CH7517A-BF	ASM1442	1	NA	Intel I219V	Intel I210IT	RS-232 *4	RS-232/422/485 *2	2	NA	1	4/2+2	1	1/1	1	1	NA	MIC-in/ Line-out	1

Dongle (Type A): AIIS-DIO32

PCA-TPM-00A1E
PCA-COM232-00A1E
PCA-COM485-00A1E

MIC-7900 10G Module RJ45

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Title	02_Block Diagram		
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Outline

New Product Planning- MIC-7700 Fanless

Product picture is for concept only. MIC-7700 will has a new ID design

Target market:

MA/ Machine Vision/Equipment System

Benefit:

- Skylake-S Desktop CPU with Q170/H110
  - Excellent Graphics, Media, & Display
  - Real-time feature adds
- i-Module for flexible expansion
- iDoor for industrial communication

Specification:

- Intel Skylake-S CPU (35W/65W)
- 2x DDR4 Memory up to 32GB
- 2x GbE
- 2x Mini-PCIe
- 4xCOM max. to 6xCOM
- Optional Module (Isolation COM/32Bit DIO/LAN module/TPM/COM232/485))
- 9~36Vdc
- -20~50'C /60'C
- Dimension: MIC-7500 (H : add 4mm)

Enabling an Intelligent Planet

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Title	03_Outline	
Size	Document Number MIC-7700	Rev A101-2
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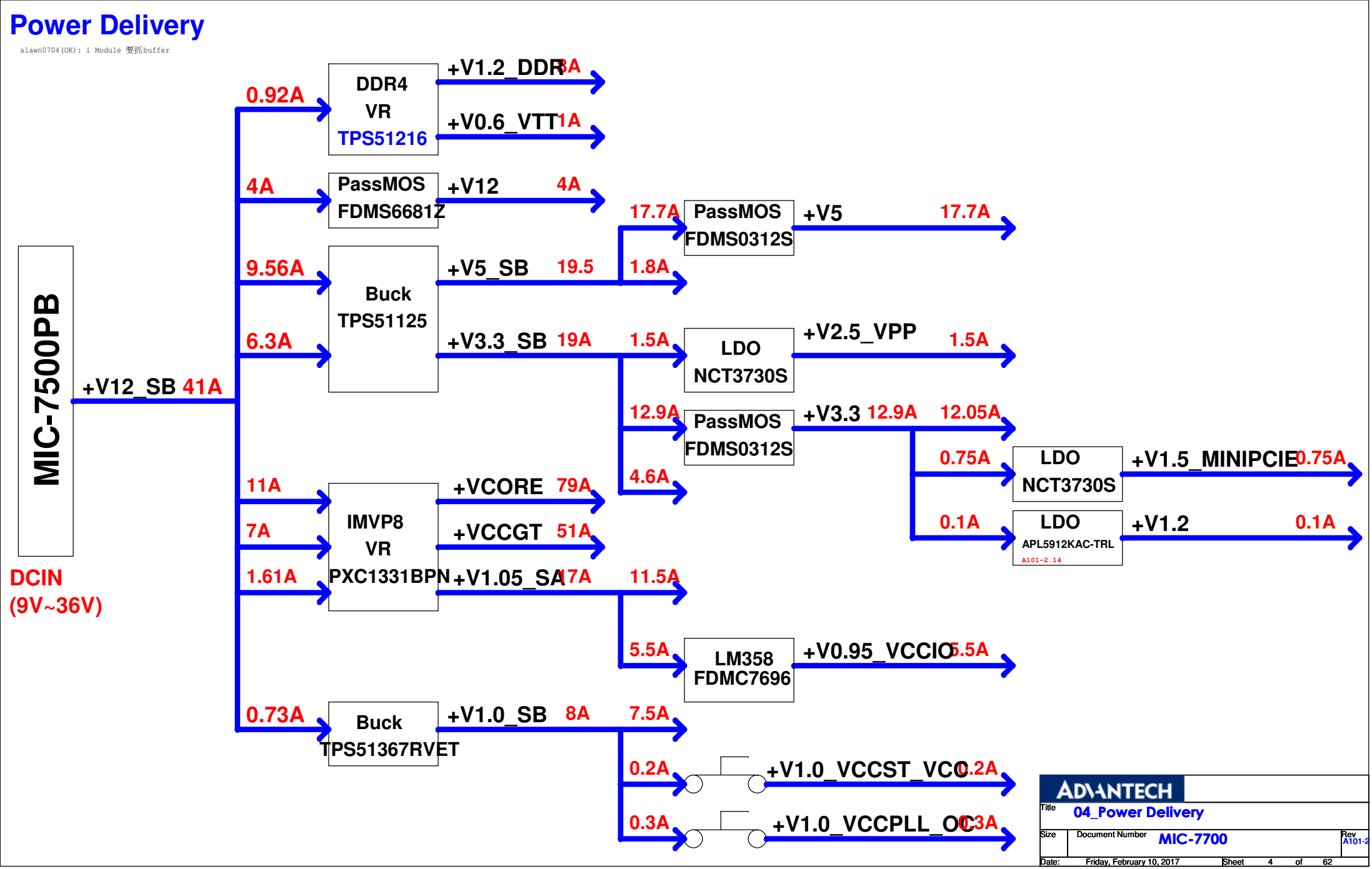
Power Delivery

alawn0704(OK): i Module 要抓buffer



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Title	04_Power Delivery		
Size	Document Number MIC-7700		Rev A101-2
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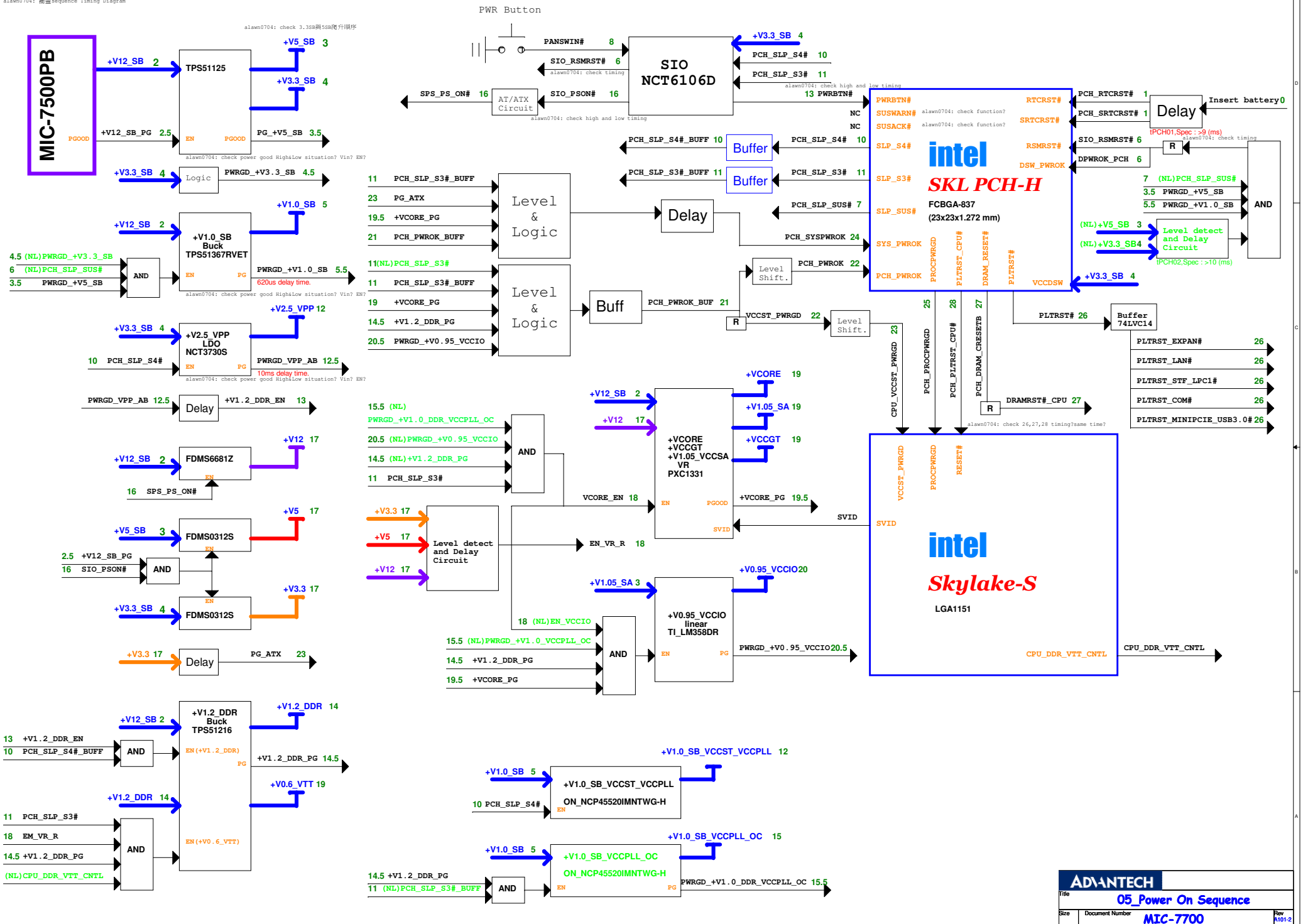
Power On Sequence

alawn0704: 補電sequence Timing Diagram



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Title	05_Power On Sequence	
Size	Document Number MIC-7700	Rev A101-2
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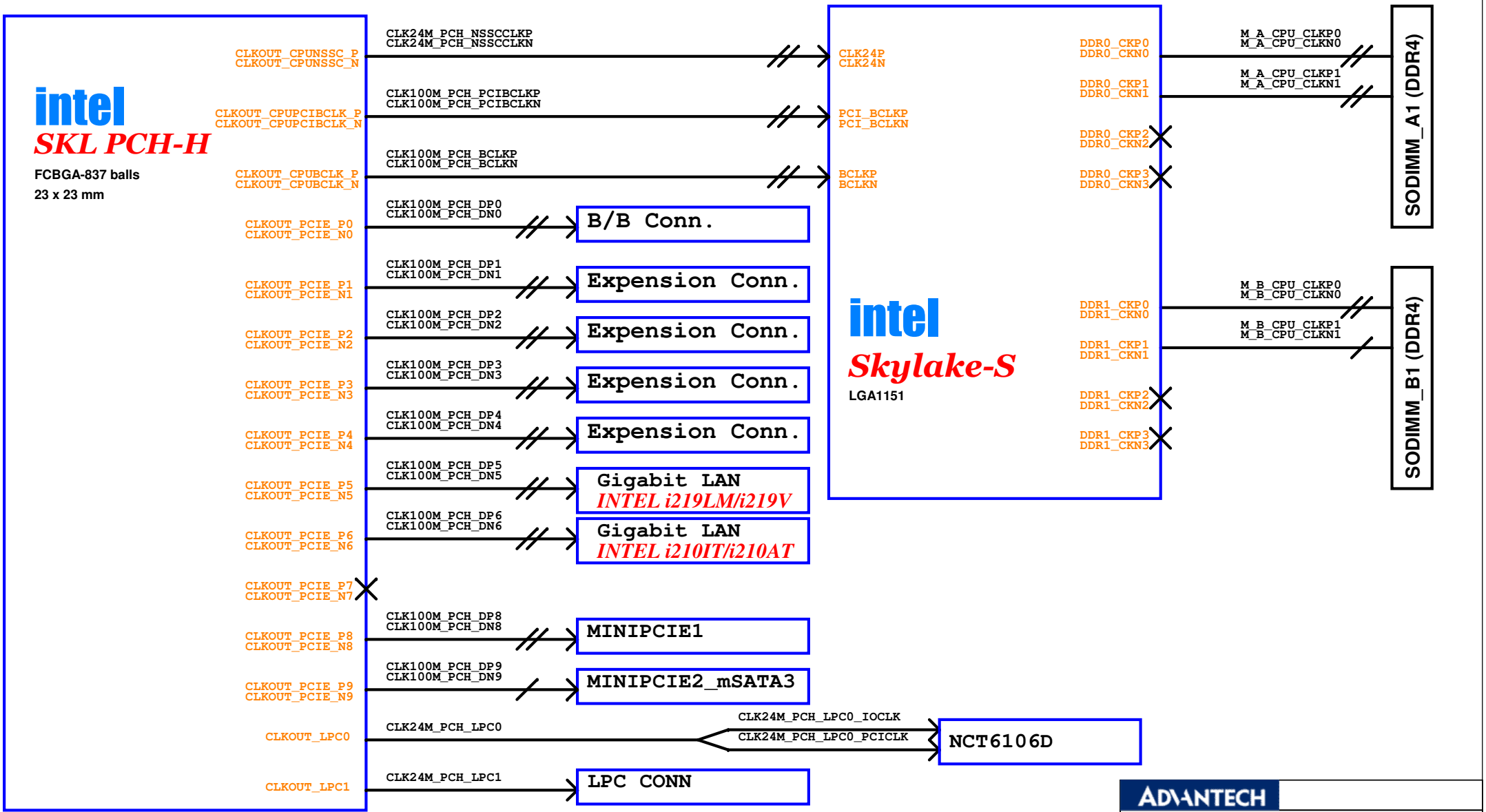
Clocks Distribution



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Title	06_Clocks Distribution	
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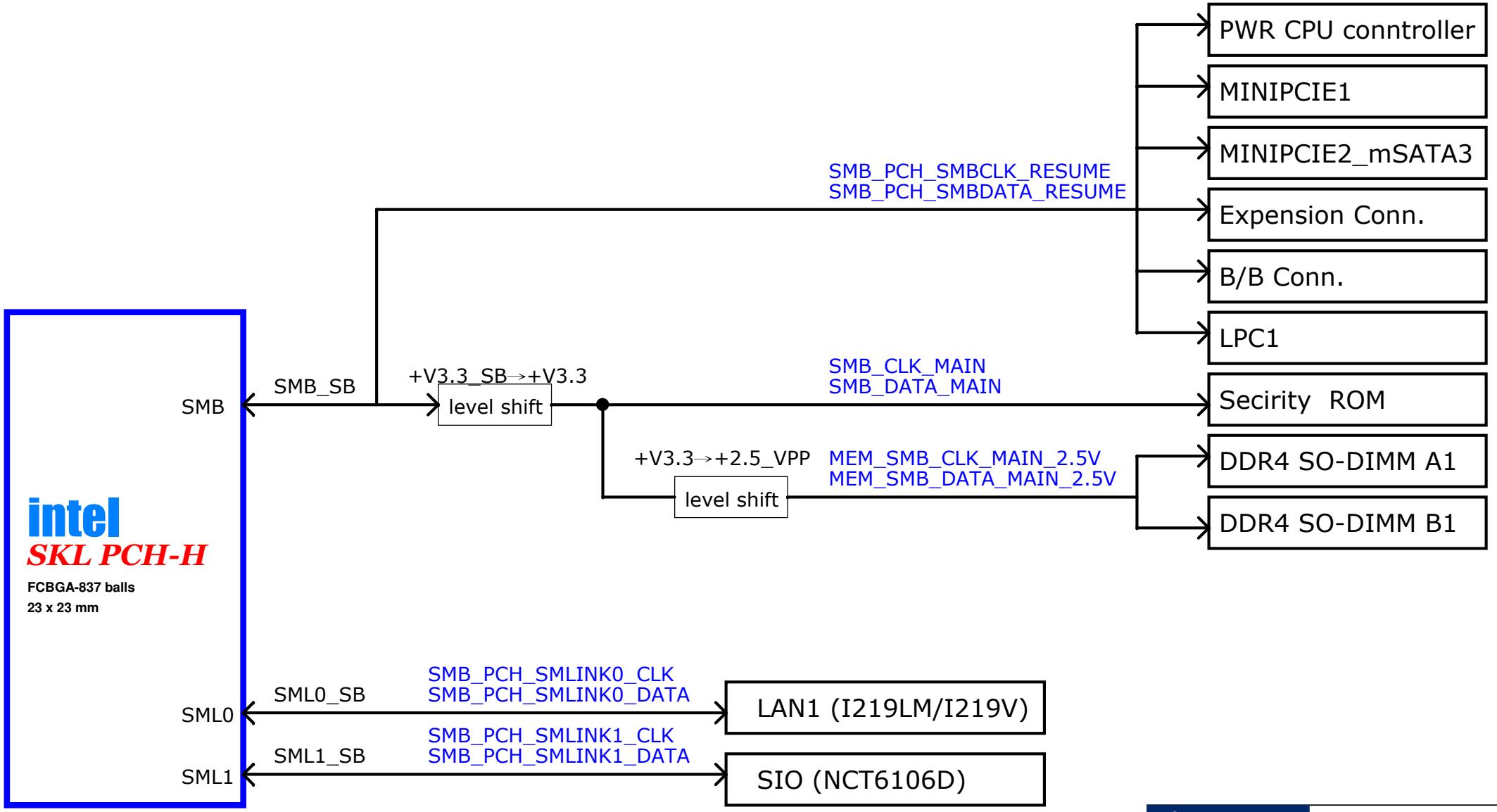
SMBUS Distribution



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Title	07_SMBUS Distribution	
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GPIO LIST

alawn0704(OA): GPIO Follow AIIS-3400

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Title	08_GPIO LIST	
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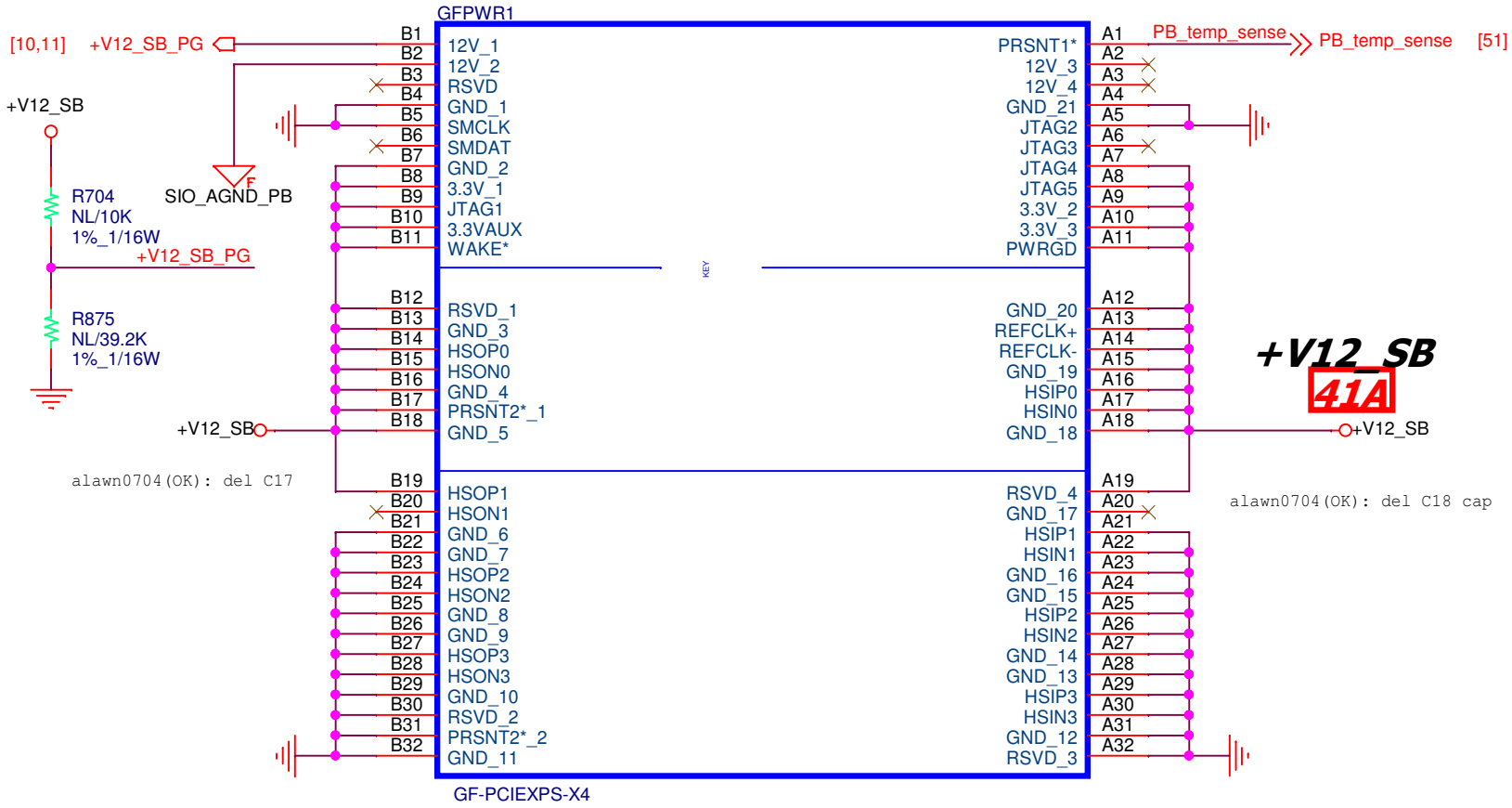
PWR +V12_SB

Power/B pull high 20k to LM5175 VCC (7.5V)

When Power/B no pull high, mount R704
When Power/B has pull high and we need 5V, mount R875



alawn0704(OK): need to update

x4 PCIe Connector B			
AB01	PWROK	Temp_Sense	AA01
AB02	SIO_AGND	RSV	AA02
AB03	RSV	RSV	AA03
AB04	GND	GND	AA04
AB05	GND	GND	AA05
AB06	RSV	RSV	AA06
AB07	+12V_SB	+12V_SB	AA07
AB08	+12V_SB	+12V_SB	AA08
AB09	+12V_SB	+12V_SB	AA09
AB10	+12V_SB	+12V_SB	AA10
AB11	+12V_SB	+12V_SB	AA11
Mechanical Key			
AB12	+12V_SB	+12V_SB	AA12
AB13	+12V_SB	+12V_SB	AA13
AB14	+12V_SB	+12V_SB	AA14
AB15	+12V_SB	+12V_SB	AA15
AB16	+12V_SB	+12V_SB	AA16
AB17	+12V_SB	+12V_SB	AA17
AB18	+12V_SB	+12V_SB	AA18
AB19	+12V_SB	+12V_SB	AA19
AB20	RSV	RSV	AA20
AB21	GND	GND	AA21
AB22	GND	GND	AA22
AB23	GND	GND	AA23
AB24	GND	GND	AA24
AB25	GND	GND	AA25
AB26	GND	GND	AA26
AB27	GND	GND	AA27
AB28	GND	GND	AA28
AB29	GND	GND	AA29
AB30	GND	GND	AA30
AB31	GND	GND	AA31
AB32	GND	GND	AA32

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Title: 09_PWR +V12_SB

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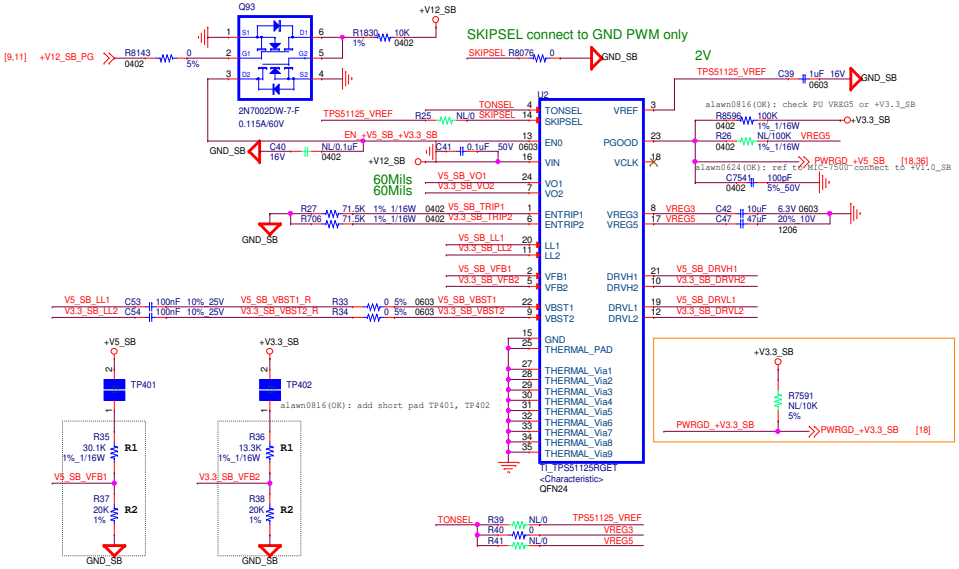
PWR +V5_SB/+V3.3_SB



Vout=2*(1+R1/R2)

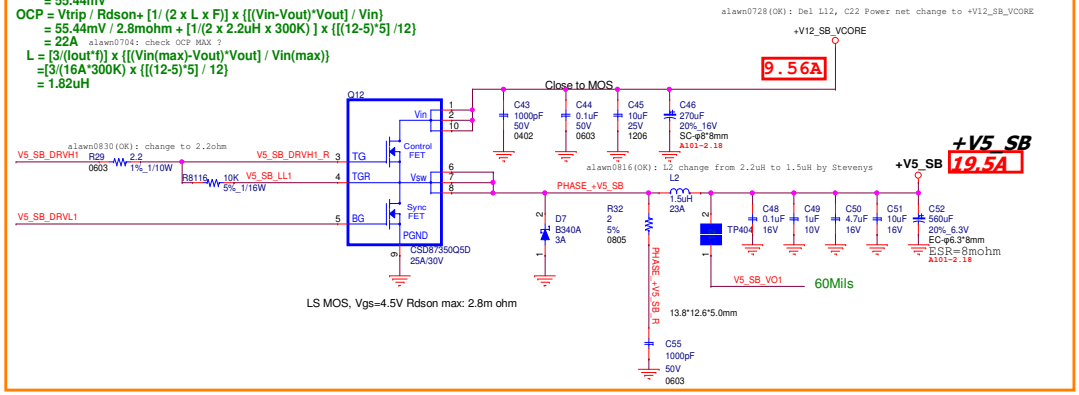
V1=2*(1+30.1/20)=5.01V V2=2*(1+13.3/20)=3.33V

TONSEL	SWITCHING FREQUENCY	
	CH1	CH2
GND	200KHz	250KHz
VREF	245KHz	305KHz
VREG3	300KHz	375KHz
VREG5	365KHz	460KHz

Default

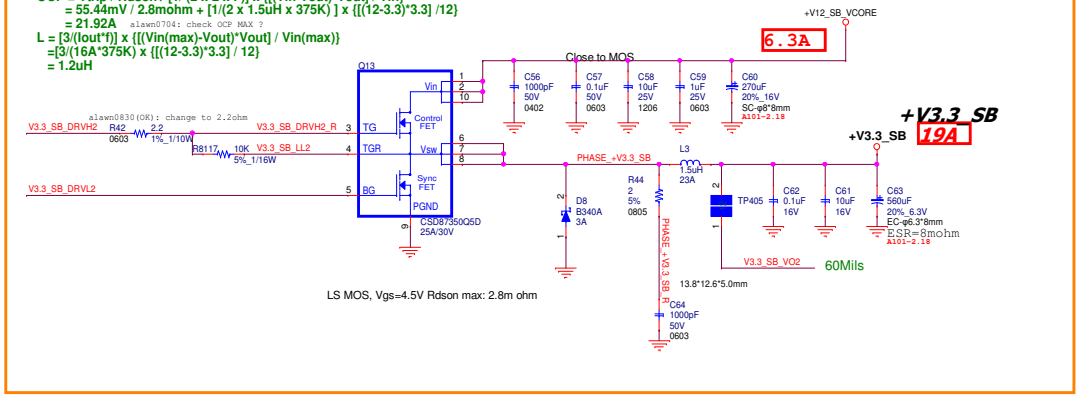
+V5_SB

Vtrip = ((Rtrip1 x 10uA)/9)-24
= ((71.5K x 10uA)/9)-24
= 55.44mV
OCP = Vtrip / Rdson+ [1/ (2 x L x F)] x {[(Vin-Vout)*Vout] / Vin}
= 55.44mV / 2.8mohm + [1/(2 x 2.2uH x 300K)] x {[(12-5)*5] /12}
= 22A alawn0704: check OCP MAX ?
L = [3/(Iout*f)] x {[(Vin(max)-Vout)*Vout] / Vin(max)}
=[3/(16A*300K) x {[(12-5)*5] / 12}
= 1.82uH



+V3.3_SB

Vtrip = ((Rtrip2 x 10uA)/9)-24
= ((72K x 10uA)/9)-24
= 55.44mV
OCP = Vtrip / Rdson+ [1/ (2 x L x F)] x {[(Vin-Vout)*Vout] / Vin}
= 55.44mV / 2.8mohm + [1/(2 x 1.5uH x 375K)] x {[(12-3.3)*3.3] /12}
= 21.92A alawn0704: check OCP MAX ?
L = [3/(Iout*f)] x {[(Vin(max)-Vout)*Vout] / Vin(max)}
=[3/(16A*375K) x {[(12-3.3)*3.3] / 12}
= 1.2uH



Title	10_PWR +V5_SB/+V3.3_SB
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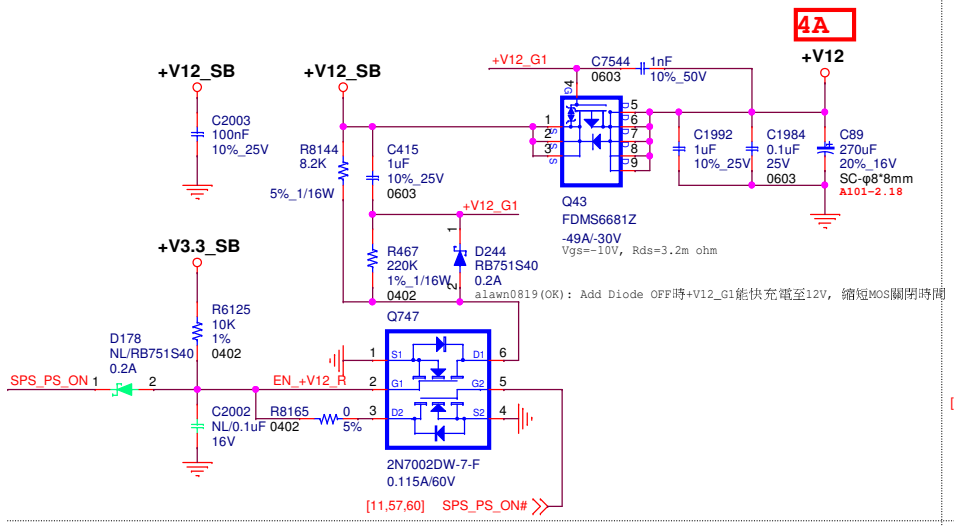
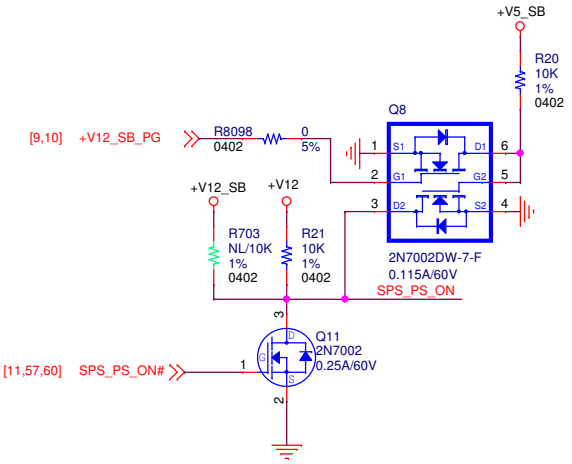
PWR_+V12/+V5/+V3.3/Discharge

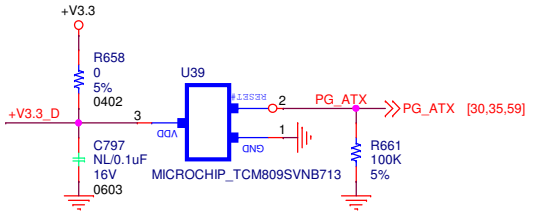
+V12



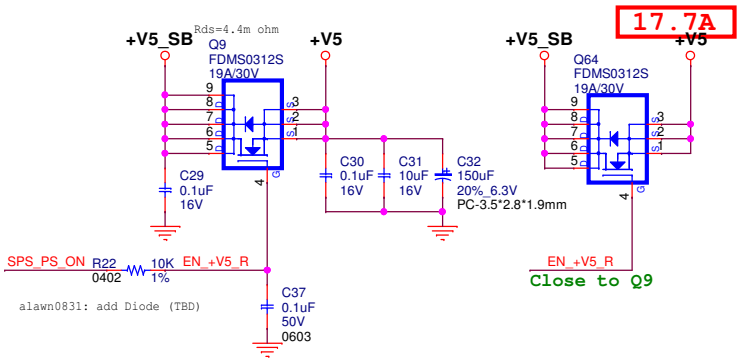
+V5, +V3.3 Enable



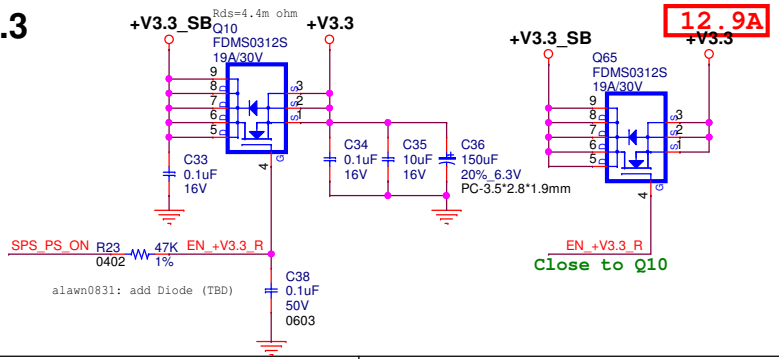
Main Power OK



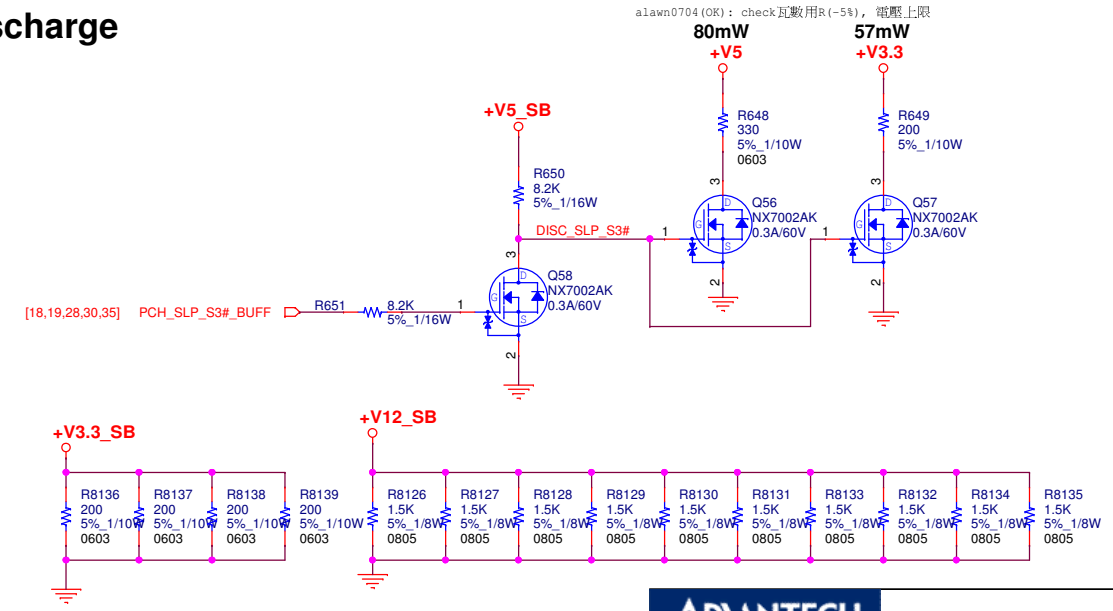
+V5



+V3.3



Discharge



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Title	11_PWR_+V12/+V5/+V3.3/Discharge	
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PWR CPU_Controller

CPU Controller

+VCORE Iomax=79A
+V1.05_SA Iomax=16.6A(VCCIO=5.5A)
+VCCGT Iomax=51A

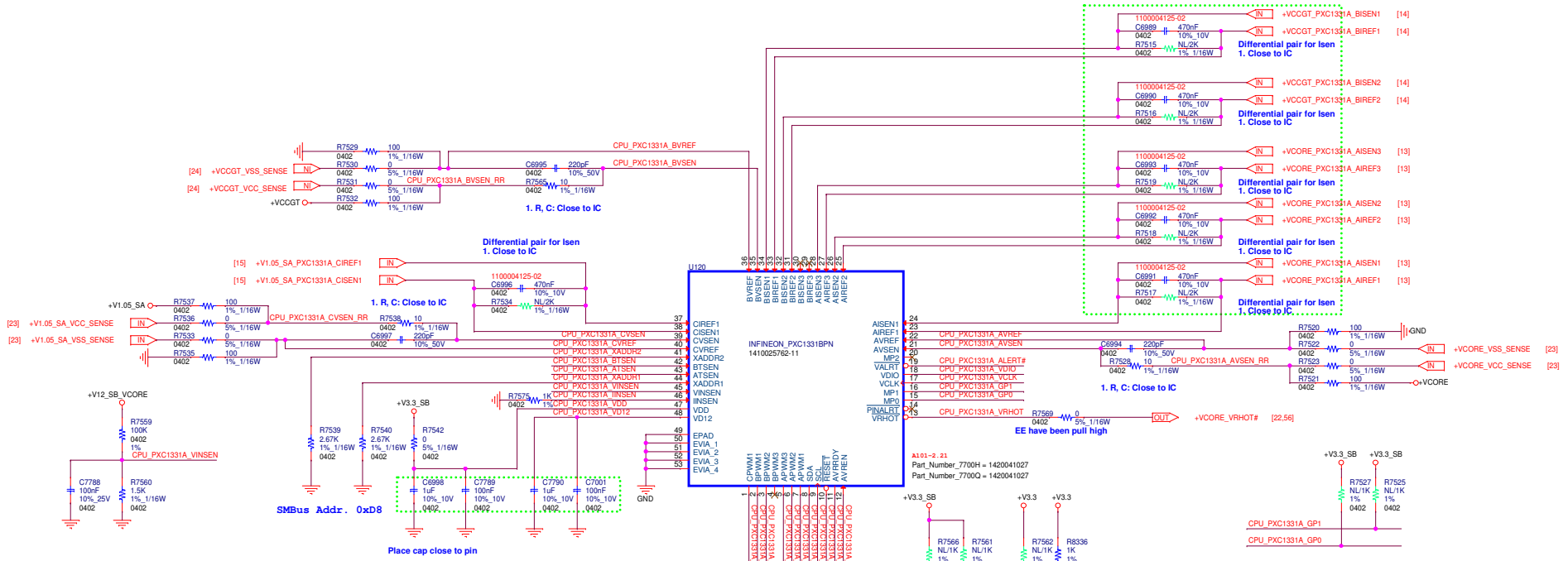
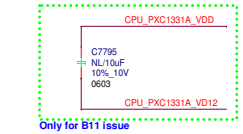
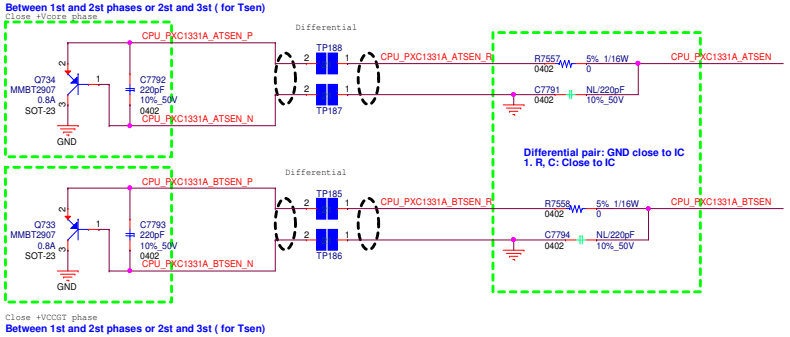


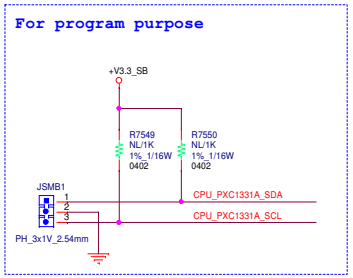
Table 6: Device I2C Slave Address

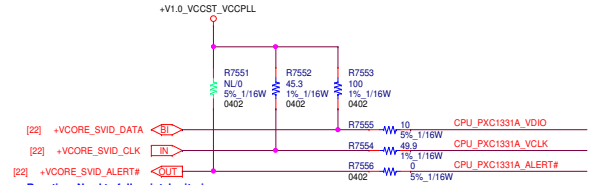
Resistor-to-GND (1%)	XADDR2							
XADDR1	2.26 kΩ	2.67 kΩ	3.16 kΩ	4.02 kΩ	5.36 kΩ	8.06 kΩ	16.0 kΩ	Open
2.26 kΩ	FC	DC	BC	9C	7C	5C	3C	1C
2.67 kΩ	F8	D8	B8	98	78	58	38	reserved
3.16 kΩ	F4	D4	B4	94	74	54	34	14
4.02 kΩ	F0	D0	B0	90	70	50	30	10
5.36 kΩ	EC	CC	AC	8C	6C	4C	2C	0C
8.06 kΩ	E8	C8	A8	88	68	48	28	08
16.0 kΩ	E4	C4	A4	84	64	44	24	04
Open	E0	C0	A0	80	60	40	20	reserved





PROGRAM JUMPER





Title	12_PWR CPU_Controller
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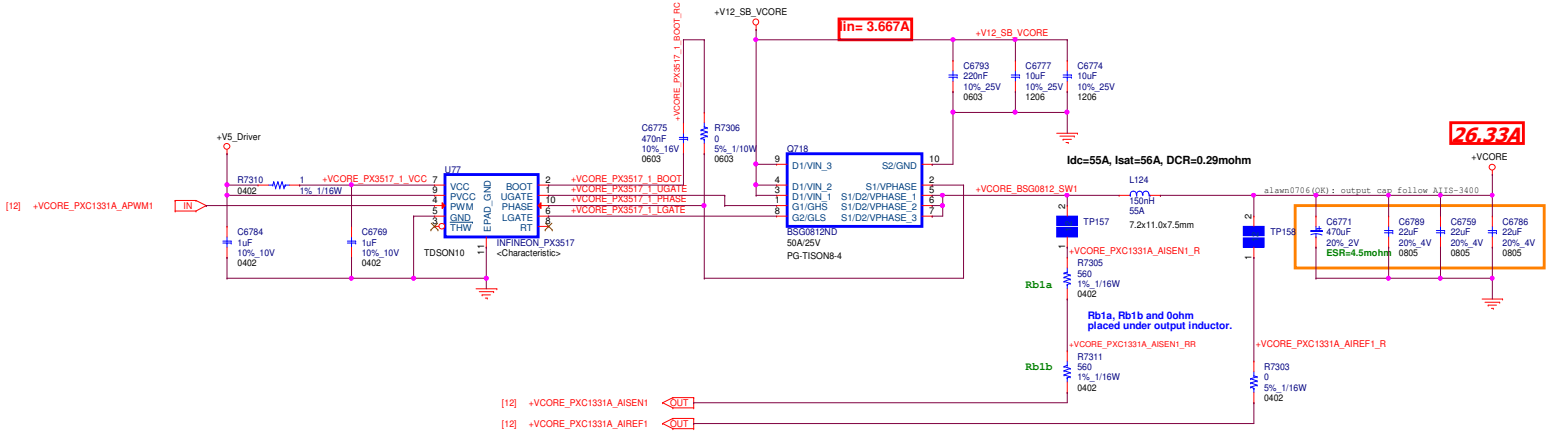
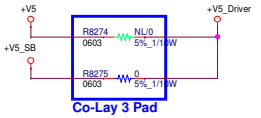
PWR +VCORE_Phase1-3

+VCORE Iomax=79A

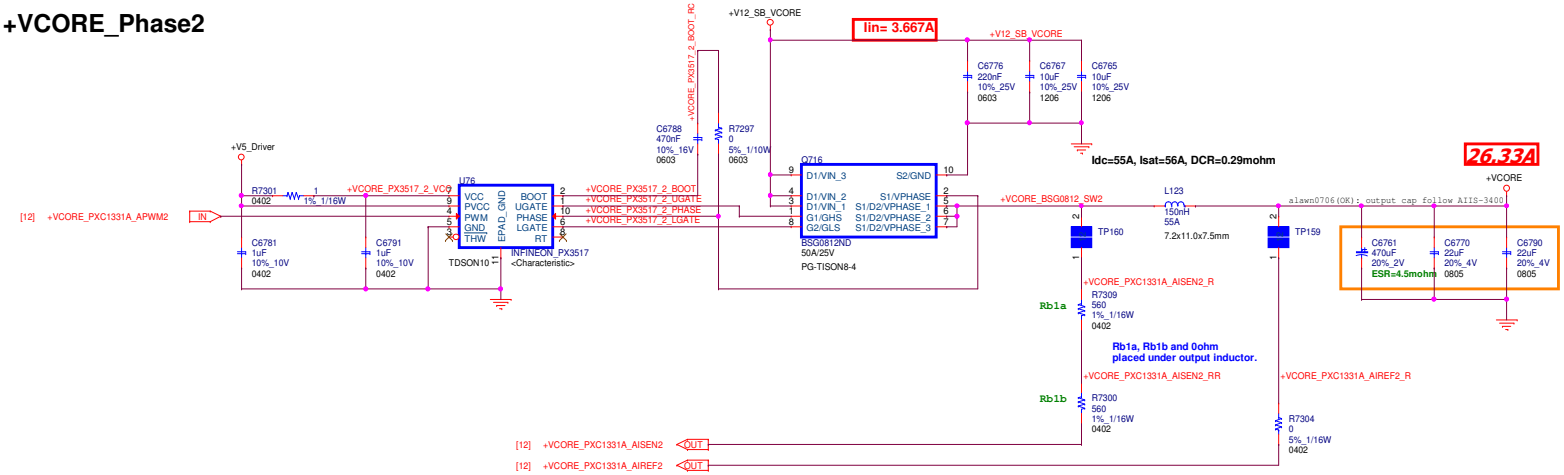
+VCORE_Phase1



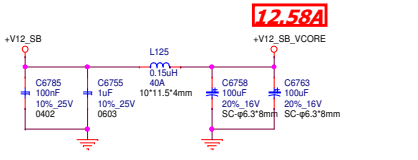
+V5_Driver



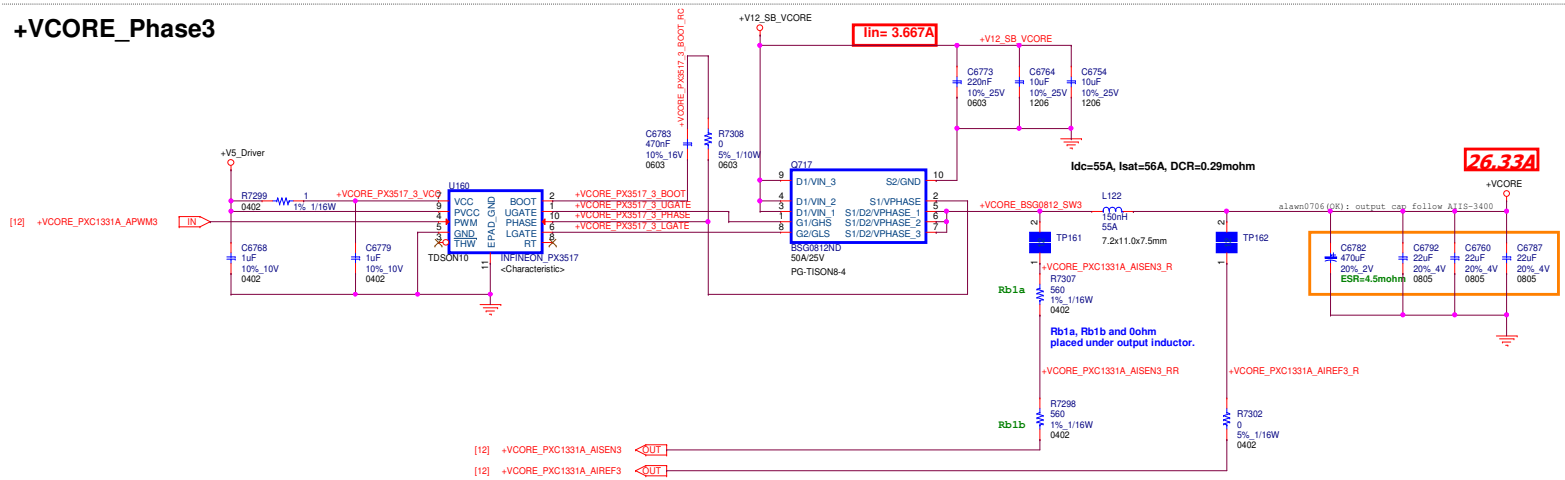
+VCORE_Phase2



+V12_SB_VCORE



+VCORE_Phase3



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Title	13_PWR +VCORE_Phase1-3	
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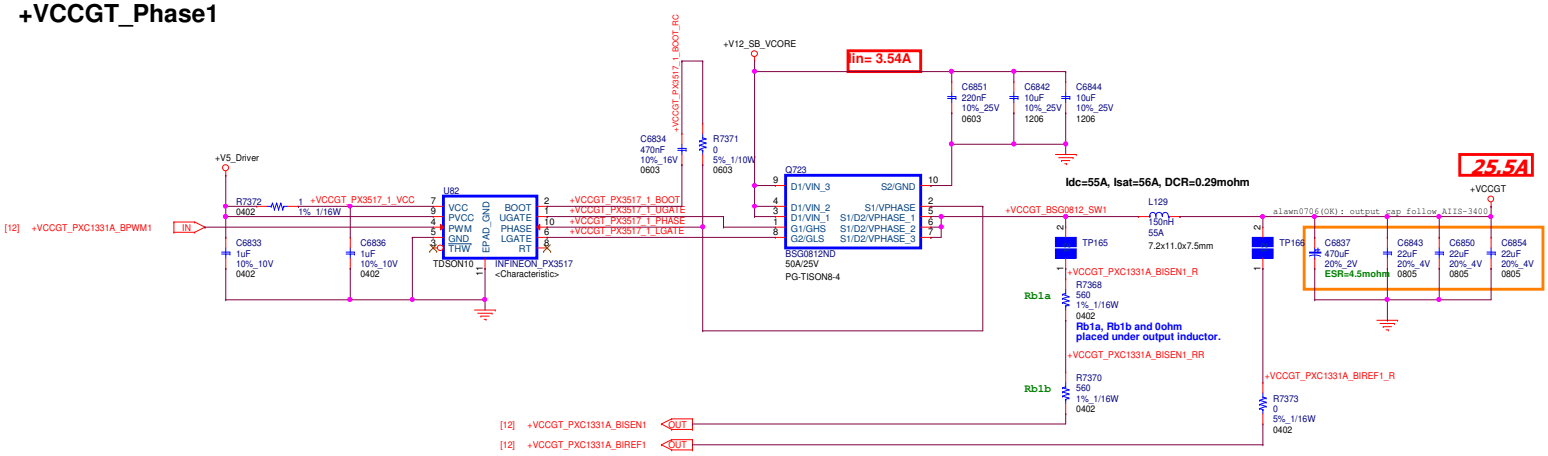
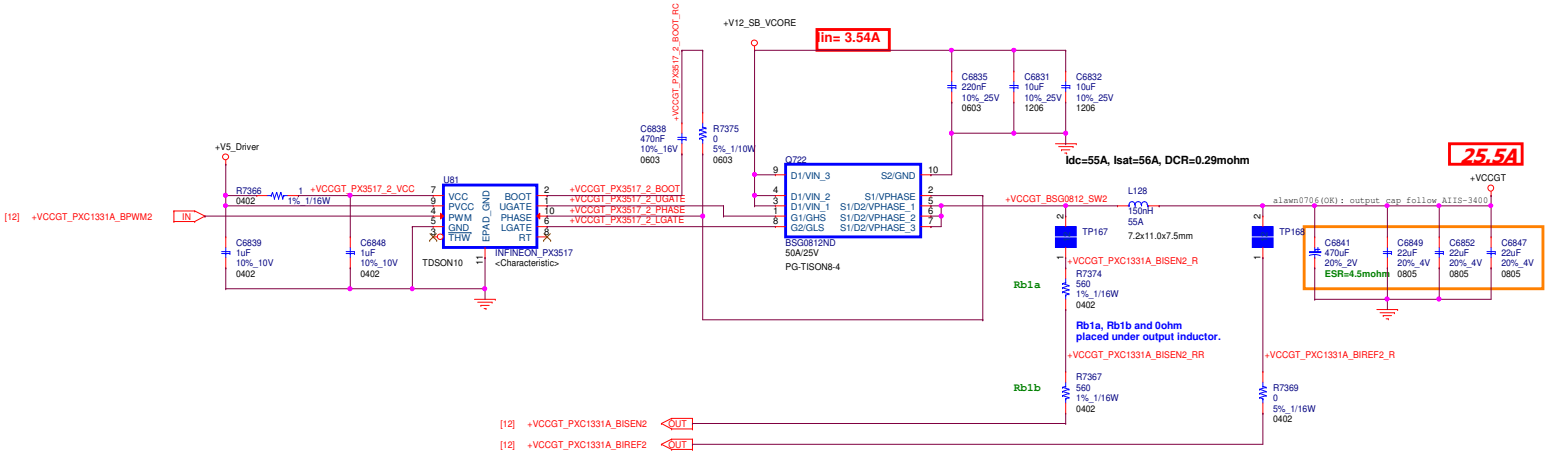
PWR +VCCGT_Phase1-2

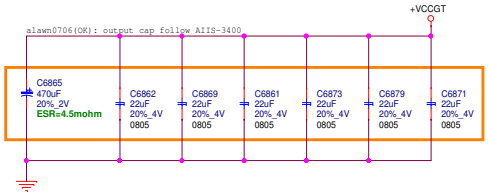
+VCCGT Iomax=51A

+VCCGT_Phase1



+VCCGT_Phase2





+V12_SB_VCORE

ADVANTECH

Title	14_PWR +VCCGT_Phase1-2	
Size	Document Number MIC-7700	Rev A101-2
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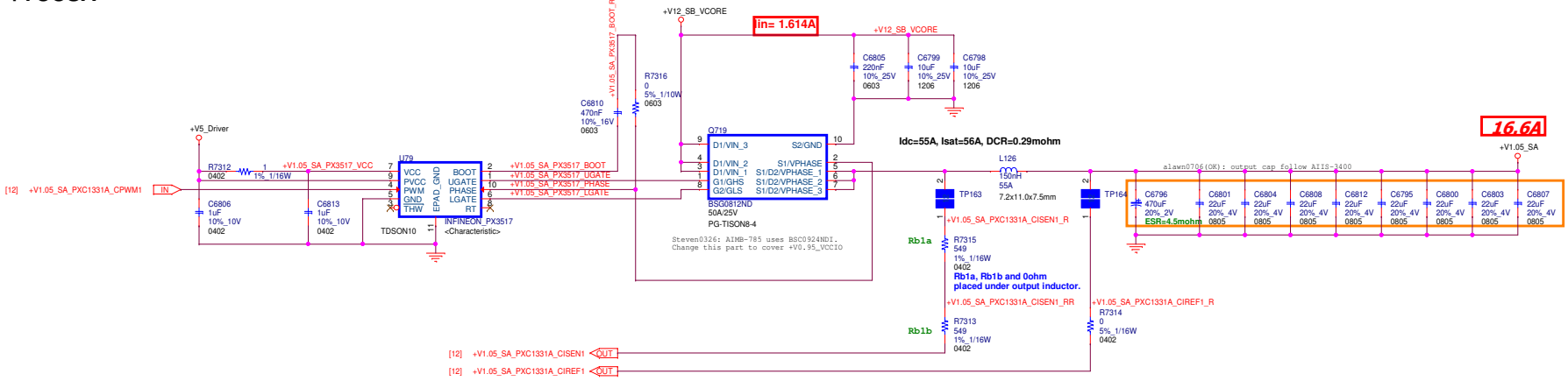
PWR +VCCSA

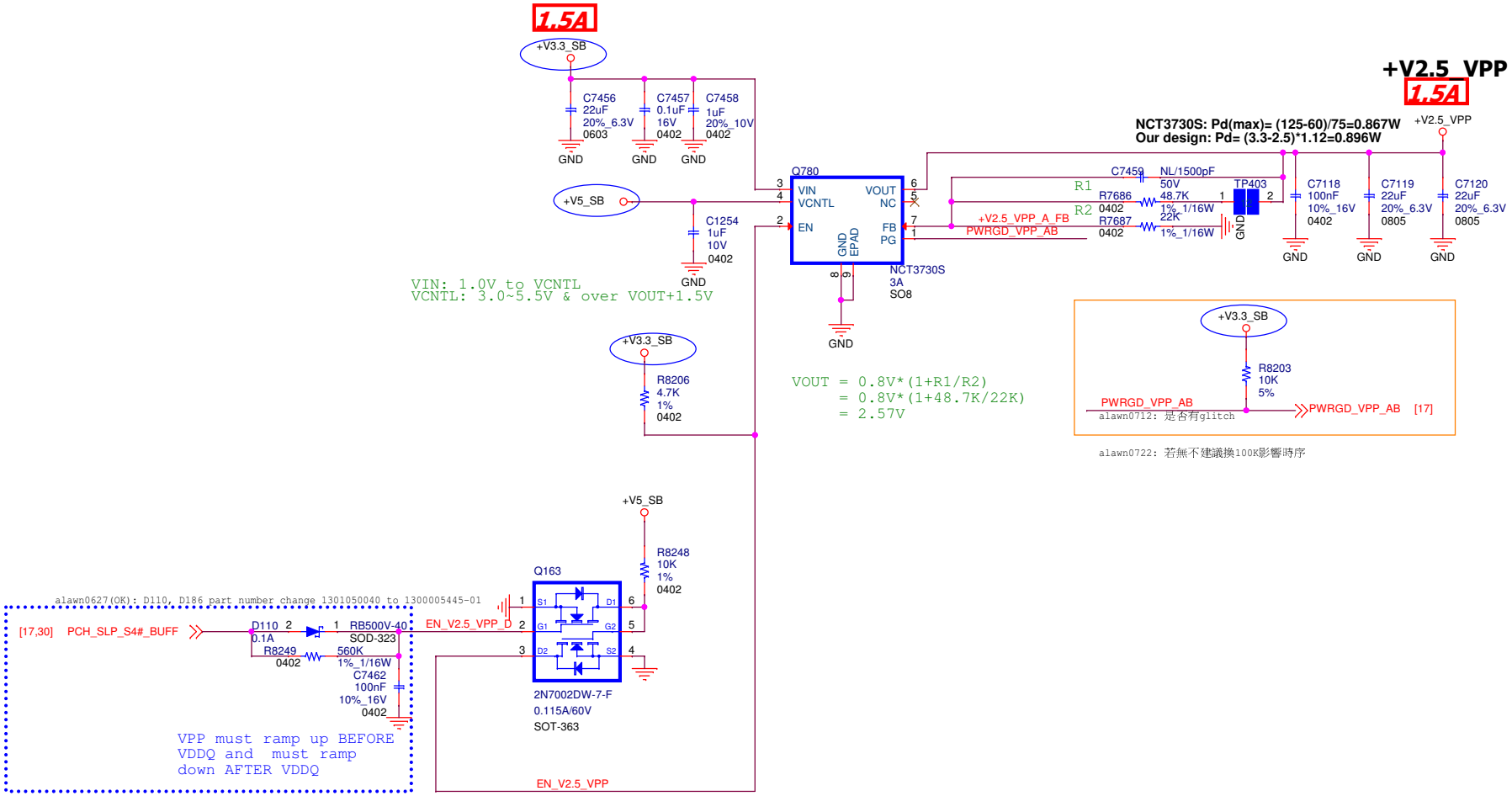
+V1.05_SA Iomax=16.6A

+VCCSA



Title	15_PWR +VCCSA		
Size	Document Number	MIC-7700	Rev A101-2
Date:	Friday, February 10, 2017	Sheet 15 of 62	

PWR DDR4 +V2.5_VPP



ADVANTECH		
Title	16_PWR DDR4 +V2.5_VPP	
Size	Document Number: MIC-7700	Rev: A101-2
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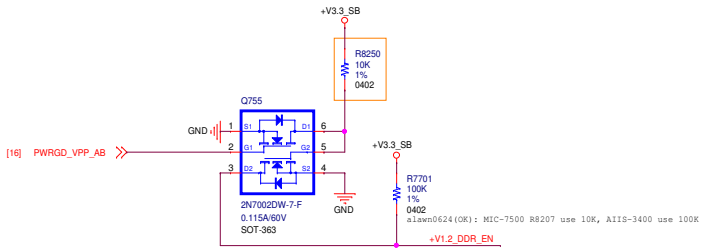
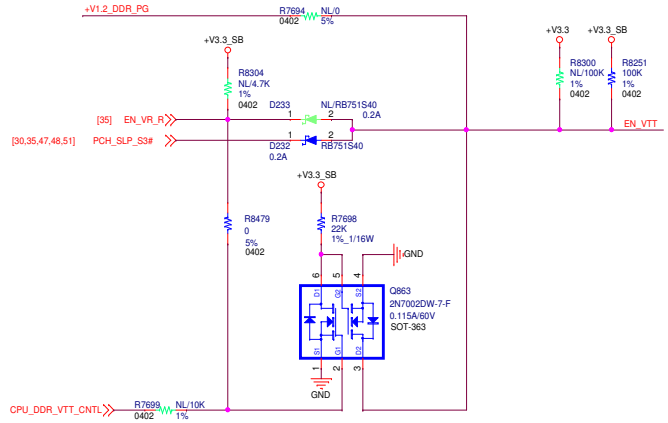
PWR DDR4 +V1.2_DDR/+V0.6_VTT

VDDQ_EN

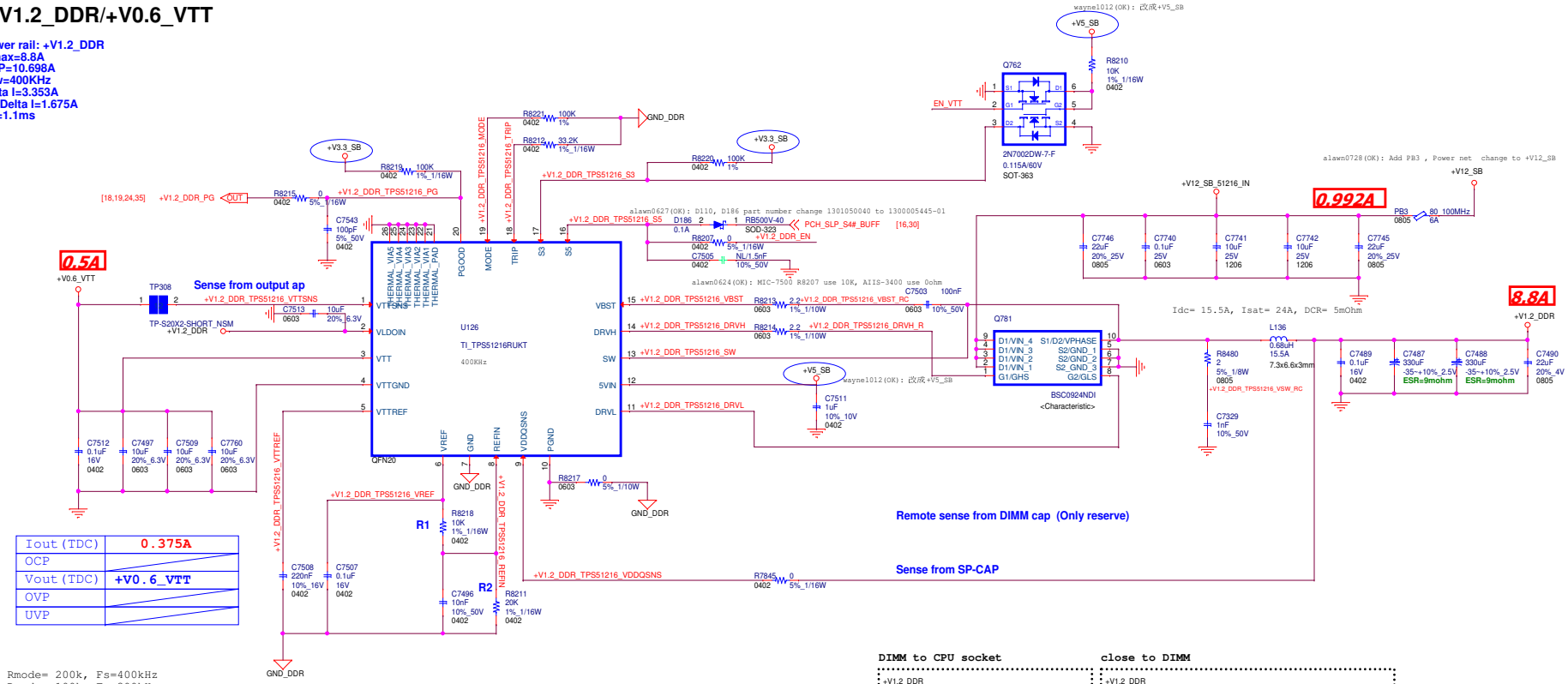


VTT_EN



+V1.2_DDR/+V0.6_VTT

Power rail: +V1.2_DDR
Iomax=8.8A
OCP=10.698A
Fsw=400KHz
Delta I=3.353A
1/2 Delta I=1.675A
SS=1.1ms



Iout(TDC)	0.375A
OCP	
Vout(TDC)	+V0.6_VTT
OVP	
UVP	

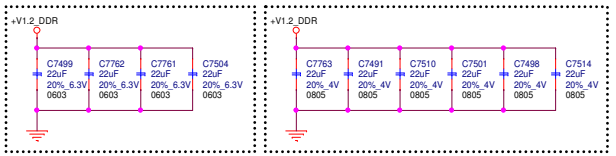
```
Rmode= 200k, Fs=400kHz
Rmode= 100k, Fs=300kHz

Vtrip(mV) = Rtrip(Kohm) x 10uA = 33.2Kx10uA = 332mV
Iocl = Vtrip /8 x Rdson + Iripple/2
     = Vtrip / 8 x Rdson + (1/ (2 x L x f)) x ((Vin-Vout)xVout)/Vin
     = 332mV / 8 x 4.6mohm +  1.676
     ~= 10.698A

R2 = R1 / [(Vref / Vout) -1]
     = 10K / [(1.8 / 1.2) - 1]
     =20K
```

Table 2. MODE Selection

MODE NO.	RESISTANCE BETWEEN MODE AND GND (kΩ)	SWITCHING FREQUENCY (kHz)	DISCHARGE MODE
3	200	400	Tracking
2	100	300	
1	68	300	Non-tracking
0	47	400	



ADVANTECH

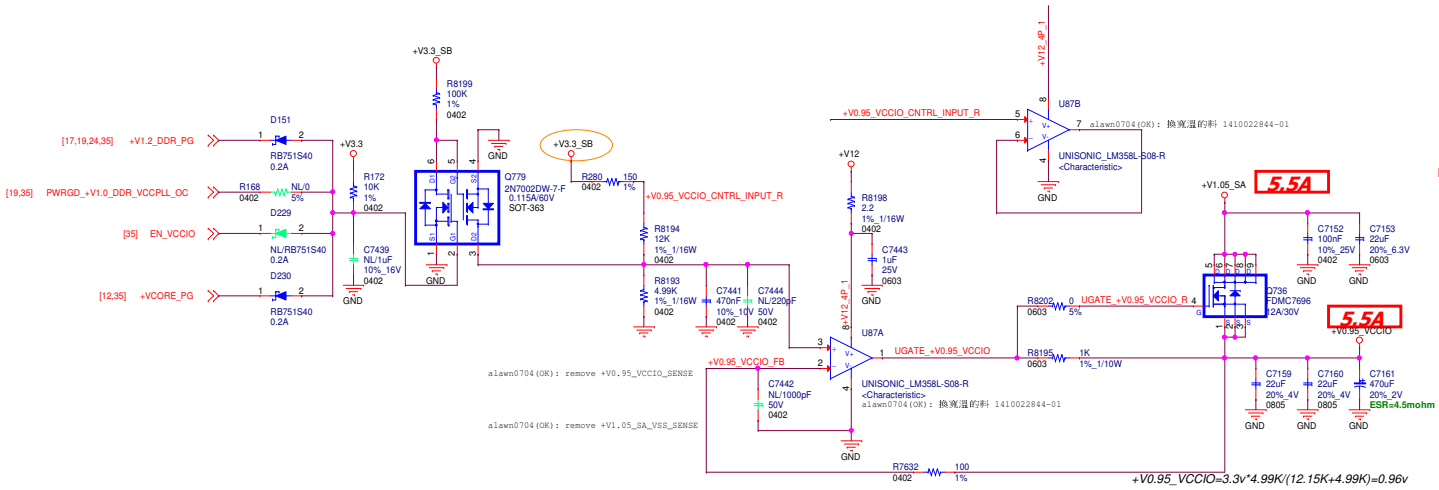
Title: 17_PWR DDR4 +V1.2_DDR/+V0.6_VTT

Size | Document Number: MIC-7700 | Rev: A101-2

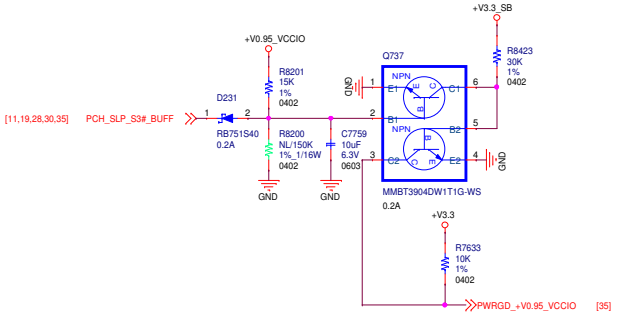
Date: Friday, February 10, 2017 | Sheet 17 of 62

PWR +V0.95_VCCIO/+V1.0_SB

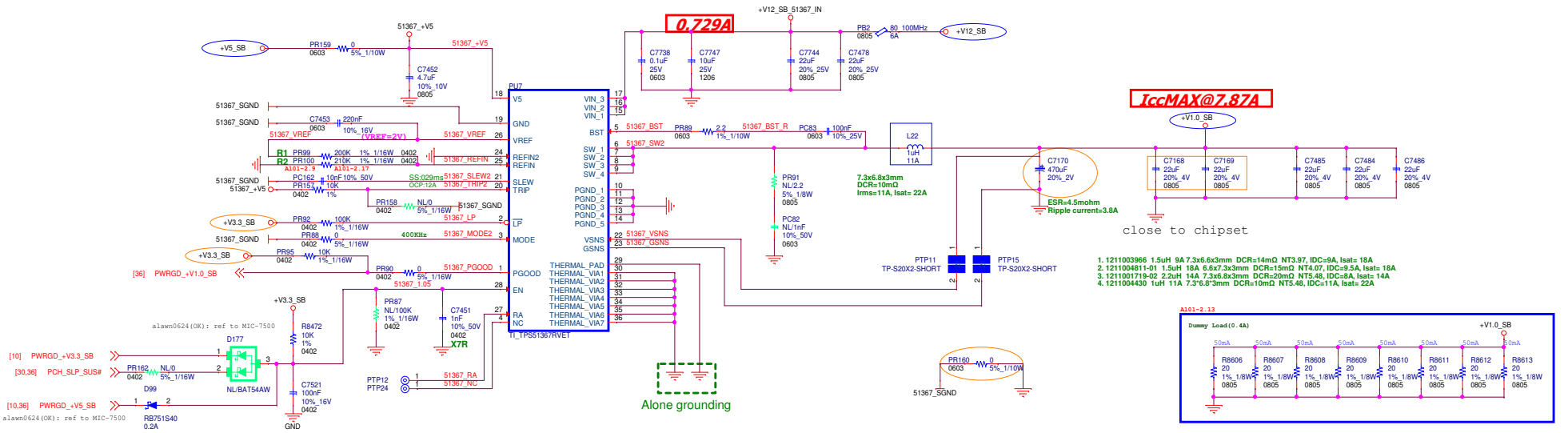
+V0.95_VCCIO



PWRGD_+V0.95_VCCIO



+V1.0_SB



Output Voltage use "TPS51367_2_3 Design Tool_0.53C.xls" to know R1 and R2

ADVANTECH

Title	18_PWR +V0.95_VCCIO/+V1.0_SB	
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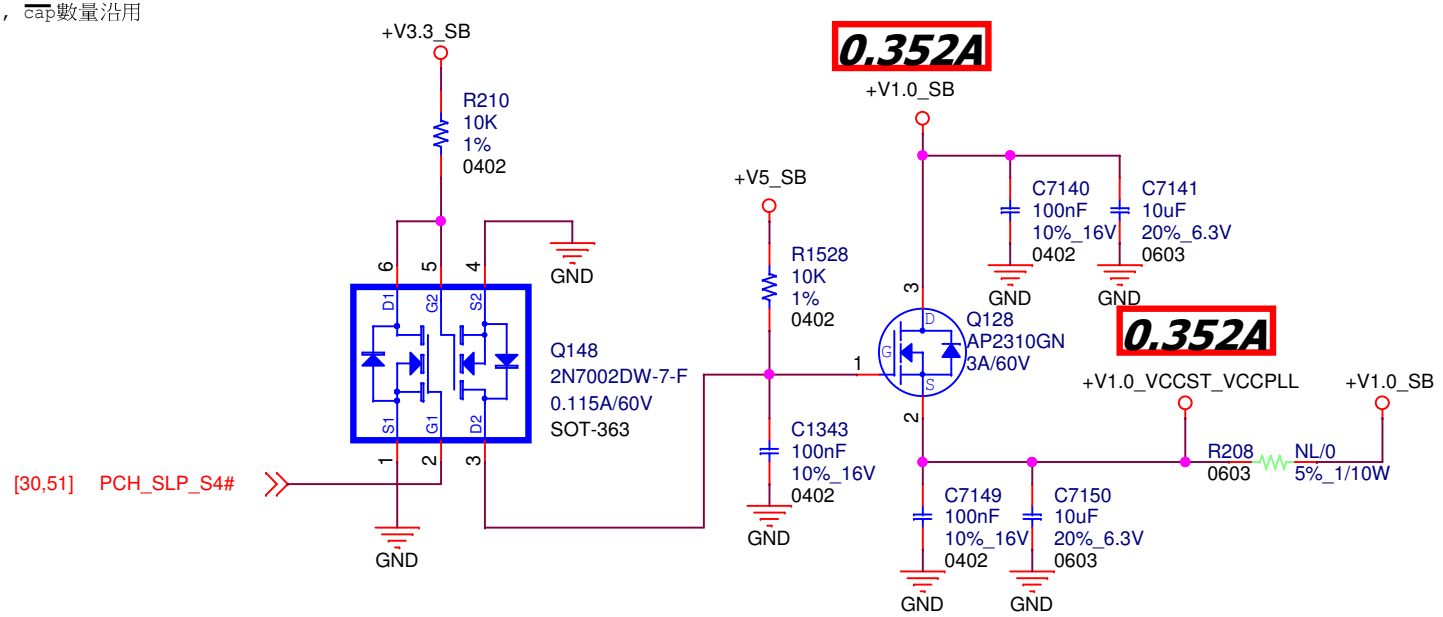
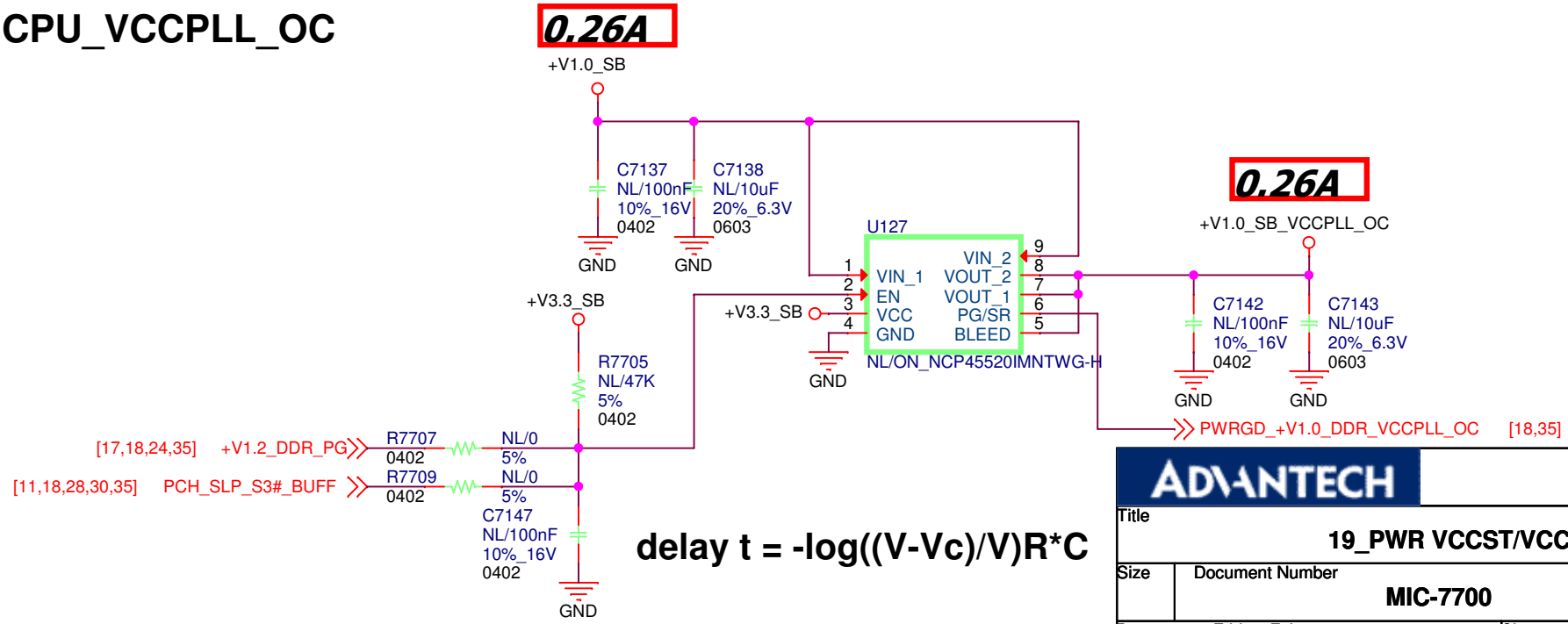
PWR VCCST/VCCPLL_OC

CPU_VCCST_VCCPLL

alawn0704(OK): ref 705, cap數量沿用



CPU_VCCPLL_OC



delay t = -log((V-Vc)/V)R*C

ADVANTECH

Title	19_PWR VCCST/VCCPLL_OC	
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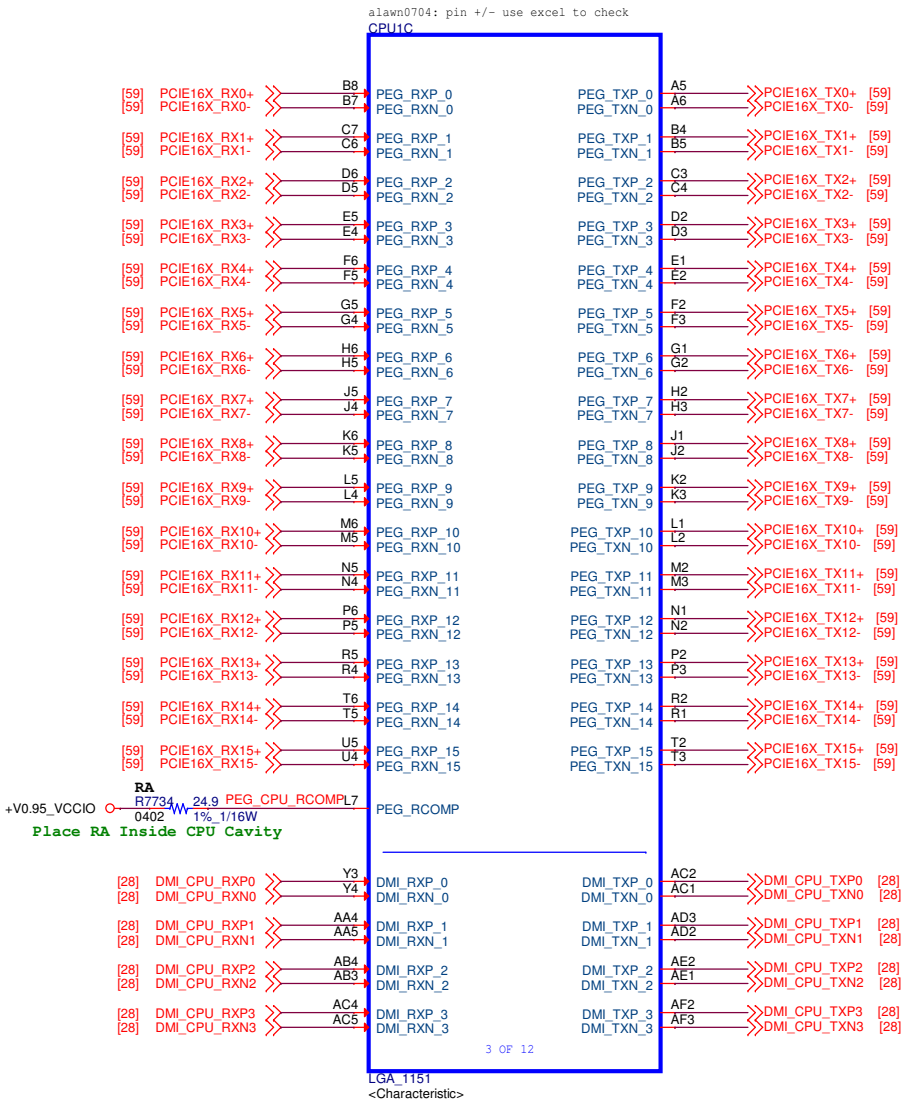
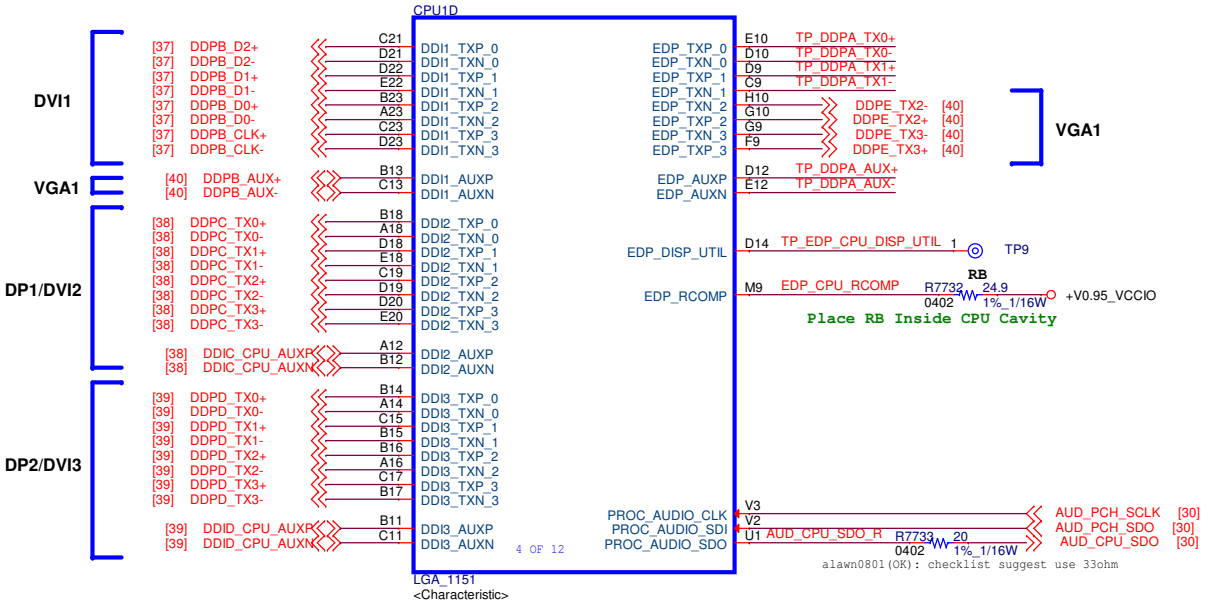
CPU PEG/DMI/DDI





Display Signal Mapping

Table 50-4. Digital Display Interface Signal Mapping

Port	DDI PROCESSOR Pin Names	Display Port Mapping	HDMI* Mapping
Port 1	DDI1_TXN[0]	DDI1_LANE0_DN	HDMIxC_TX2_DN
	DDI1_TXP[0]	DDI1_LANE0_DP	HDMIxC_TX2_DP
	DDI1_TXN[1]	DDI1_LANE1_DN	HDMIxC_TX1_DN
	DDI1_TXP[1]	DDI1_LANE1_DP	HDMIxC_TX1_DP
	DDI1_TXN[2]	DDI1_LANE2_DN	HDMIxC_TX0_DN
	DDI1_TXP[2]	DDI1_LANE2_DP	HDMIxC_TX0_DP
	DDI1_TXN[3]	DDI1_LANE3_DN	HDMIxC_CLK_DN
	DDI1_TXP[3]	DDI1_LANE3_DP	HDMIxC_CLK_DP
	DDPB_HPD	DDI1_HPD_Q	DDI1_HPD_Q
	DDPB_CTRLCLK	NA	DDI1_CTRL_CK
	DDPB_CTRLDATA	NA	DDI1_CTRL_DATA
Port 2	DDI2_TXN[0]	DDI2_LANE0_DN	HDMIxC_TX2_DN
	DDI2_TXP[0]	DDI2_LANE0_DP	HDMIxC_TX2_DP
	DDI2_TXN[1]	DDI2_LANE1_DN	HDMIxC_TX1_DN
	DDI2_TXP[1]	DDI2_LANE1_DP	HDMIxC_TX1_DP
	DDI2_TXN[2]	DDI2_LANE2_DN	HDMIxC_TX0_DN
	DDI2_TXP[2]	DDI2_LANE2_DP	HDMIxC_TX0_DP
	DDI2_TXN[3]	DDI2_LANE3_DN	HDMIxC_CLK_DN
	DD21_TXP[3]	DDI2_LANE3_DP	HDMIxC_CLK_DP
	DDPC_HPD	DDI2_HPD_Q	DDI2_HPD_Q
	DDPC_CTRLCLK	NA	DDI2_CTRL_CK
	DDPC_CTRLDATA	NA	DDI2_CTRL_DATA
Port 3	DDI3_TXP[0]	DDI3_LANE0_DP	HDMIx_TX2_DP
	DDI3_TXN[0]	DDI3_LANE0_DN	HDMIx_TX2_DN
	DDI3_TXP[1]	DDI3_LANE1_DP	HDMIx_TX1_DP
	DDI3_TXN[1]	DDI3_LANE1_DN	HDMIx_TX1_DN
	DDI3_TXP[2]	DDI3_LANE2_DP	HDMIx_TX0_DP
	DDI3_TXN[2]	DDI3_LANE2_DN	HDMIx_TX0_DN
	DDI3_TXP[3]	DDI3_LANE3_DP	HDMIx_CLK_DP
	DDI3_TXN[3]	DDI3_LANE3_DN	HDMIx_CLK_DN
	Hot plug detect used by HDMI Port 3	DDPD_HPD	DDI3_HPD_Q
	HDMI DDC lines for Port 3	DDPD_CTRLCLK	DDI3_CTRL_CK
		DDPD_CTRLDATA	DDI3_CTRL_DATA

ADVANTECH

Title	20_CPU PEG/DMI/DDI	
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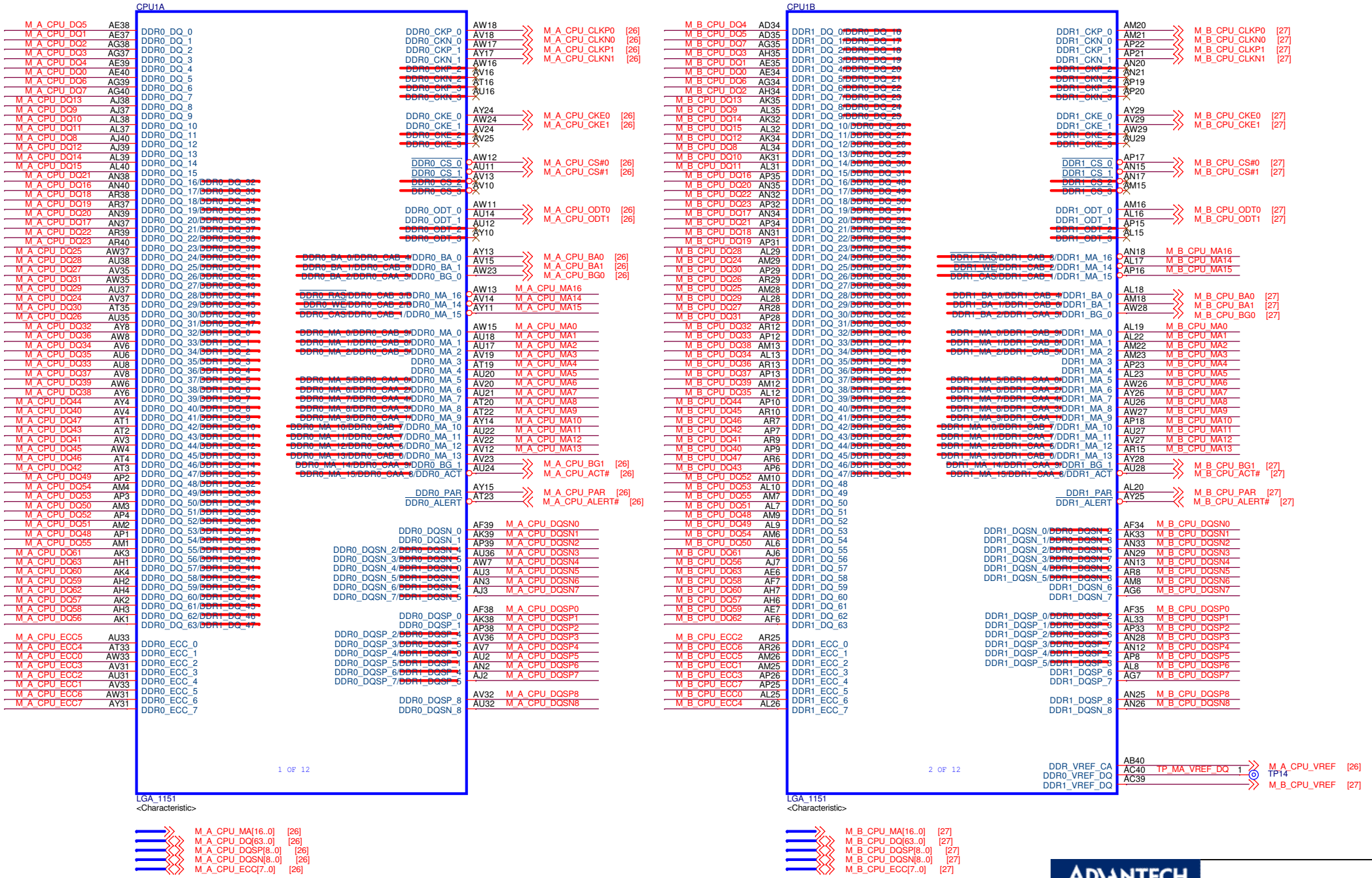
CPU DDR4 MA/MB



Title	21_CPU DDR4 MA/MB
Size	Document Number: MIC-7700
Rev	A101-2
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CPU MISC/CFG

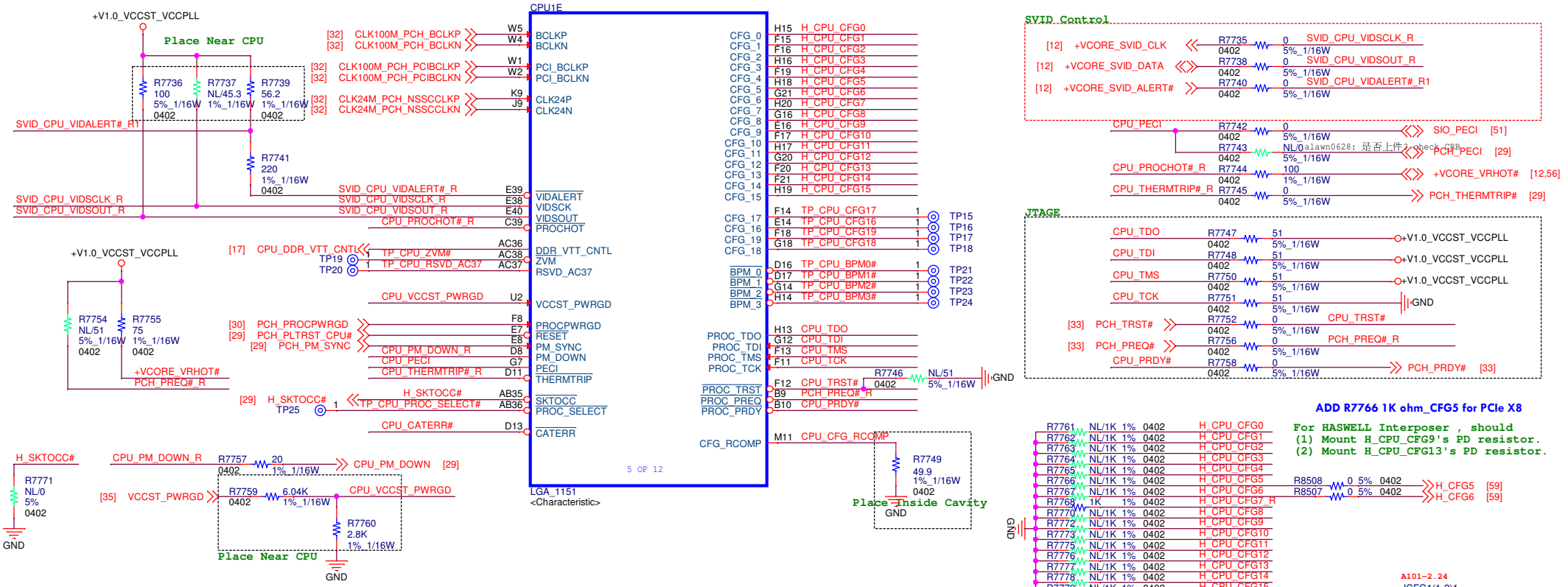

Table 2-17. PCI Express* Bifurcation and Lane Reversal Mapping

Bifurcation	Link Width			Config. Signals			Lanes													
	0:1:0	0:1:1	0:1:2	CFG [6]	CFG [5]	CFG [2]	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1x16	x16	N/A	N/A	1	1	1	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1x16 **Reversed**	x16	N/A	N/A	1	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2x8	x8	x8	N/A	1	0	1	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
2x8 **Reversed**	x8	x8	N/A	1	0	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
1x8+2x4	x8	x4	x4	0	0	1	0	1	2	3	4	5	6	7	0	1	2	3	0	1	2	3
1x8+2x4 **Reversed**	x8	x4	x4	0	0	0	3	2	1	0	3	2	1	0	7	6	5	4	3	2	1	0

Notes:

1. For CFG bus further details, refer to Section 6.4.
2. Support is also provided for narrow width and use devices with lower number of lanes (that is, usage on x4 configuration), however further bifurcation is not supported.
3. In case that more than one device is connected, the device with the highest lane count, should always be connected to the lower lanes, as follows:
   - Connect lane 0 of 1st device to lane 0.
   - Connect lane 0 of 2nd device to lane 8.
   - Connect lane 0 of 3rd device to lane 12.

   For example:
   a. When using 1x8 + 2x4, the 8 lane device must use lanes 0:7.
   b. When using 1x4 + 1x2, the 4 lane device must use lanes 0:3, and other 2 lanes device must use lanes 8:9.
   c. When using 1x4 + 1x2 + 1x1, 4 lane device must use lanes 0:3, two lane device must use lanes 8:9, one lane device must use lane 12.

Configuration Signals:

CFG[0]: Stall reset sequence after PCU PLL lock until de-asserted:
– 1 = (Default) Normal Operation;No stall.
– 0 = Stall.

CFG[2]: PCI Express* Static x16 Lane Numbering Reversal.
– 1 = (Default) Normal operation
– 0 = Lane numbers reversed.

CFG[4]: eDP enable:
– 1 = Disabled.
– 0 = (Default) Enabled.

CFG[6:5]: PCI Express* Bifurcation
– 00 = 1 x8, 2 x4 PCI Express*
– 01 = reserved
– 10 = 2 x8 PCI Express*
– 11 = (Default) 1 x16 PCI Express*

CFG[7]: PEG Training:
– 1 = (default) PEG Train immediately following RESET# de assertion.
– 0 = PEG Wait for BIOS for training.

Mode	Jumper Setting
PEG Train immediately following RESET# de-assertion.	1-2 Short (Default)
PEG Wait for BIOS for training.	2-3 Short

ADVANTECH

Title	22_CPU MISC/CFG	
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CPU VCORE/VCCSA POWER

0.55(V)~1.5(V)@+VCORE

79(A)@+VCORE

11.1(A)@+V1.05_SA

2.8(A)@+V1.2_VDDQ

5.5(A)@+V0.95_VCCIO

0.25(A)@+V1.0_VCCST_VCCPLL

0.12(A)@+V1.0_VCCST

0.13(A)@+V1.0_VCCPLL

0.26(A)@VCCPLL_OC

2.5(A)@+V1.0_OPC

2.8(A)@+V1.0_EOPIO

0.05(A)@+V1.8_SB_G_OPC

Co-Lay 3 Pad

No use if not Support CPU 4+4e

close to CPU socket

Place Caps at TOP socket edge

Place all above caps on TOP side of CPU cavity

Place all below caps on BOTTOM side near CPU socket

Place all caps inside CPU socket cavity TOP

Place all caps at TOP socket edge

Place caps in socket edge TOP

Place caps in socket cavity BOTTOM/TOP

alawn0704: check 2 type power rail defference

alawn0704(OK): remove +V0.95_VCCIO_SENSE

VccPLL_OC power rail is directly tied to VDDQ VR.

CPU1G

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LGA_1151

<Characteristic>

CPU1I

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LGA_1151

<Characteristic>

Title	23_CPU VCORE/VCCSA POWER
Size	Document Number MIC-7700 Rev A101-2
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CPU VCCGT/VCCGTX POWER

0.55(V)~1.5(V)@+VCCGT
116(A)@+VCCGT

0.55(V)~1.5(V)@+VCCGTX
No use it not Support CPU 4+4e

Place caps on TOP side socket cavity

C7217 22uF 20% 6.3V 0805 — C7218 22uF 20% 6.3V 0805 — C7219 22uF 20% 6.3V 0805 — C7220 22uF 20% 6.3V 0805 — C7221 22uF 20% 6.3V 0805 — C7222 22uF 20% 6.3V 0805

Place cap in socket edge TOP

C7223 22uF 20% 6.3V 0805 — C7224 22uF 20% 6.3V 0805 — C7216 22uF 20% 6.3V 0805

Place caps on Backside under socket cavity

C7225 22uF 20% 6.3V 0805 — C7226 22uF 20% 6.3V 0805 — C7227 22uF 20% 6.3V 0805 — C7228 22uF 20% 6.3V 0805 — C7229 22uF 20% 6.3V 0805 — C7230 22uF 20% 6.3V 0805 — C7231 22uF 20% 6.3V 0805

+VCCGT

CPU1H

AA34 VCCGT_1
AA35 VCCGT_2
AA36 VCCGT_3
AA37 VCCGT_4
AA38 VCCGT_5
AB33 VCCGT_6
AB34 VCCGT_7
G36 VCCGT_8
G37 VCCGT_9
G38 VCCGT_10
G39 VCCGT_11
G40 VCCGT_12
H36 VCCGT_13
H38 VCCGT_14
H40 VCCGT_15
J36 VCCGT_16
J37 VCCGT_17
J38 VCCGT_18
J39 VCCGT_19
J40 VCCGT_20
K36 VCCGT_21
K38 VCCGT_22
K40 VCCGT_23
L34 VCCGT_24
L35 VCCGT_25
L36 VCCGT_26
L37 VCCGT_27
L38 VCCGT_28
L39 VCCGT_29
L40 VCCGT_30
M33 VCCGT_31
M34 VCCGT_32
M36 VCCGT_33
M38 VCCGT_34
M40 VCCGT_35
N34 VCCGT_36
N35 VCCGT_37
N36 VCCGT_38
N37 VCCGT_39
N38 VCCGT_40
N39 VCCGT_41
N40 VCCGT_42
P33 VCCGT_43
P34 VCCGT_44
P36 VCCGT_45
P38 VCCGT_46
P40 VCCGT_47
R34 VCCGT_48
R35 VCCGT_49
R36 VCCGT_50
R37 VCCGT_51
R38 VCCGT_52
R39 VCCGT_53
R40 VCCGT_54
T33 VCCGT_55
T34 VCCGT_56
T36 VCCGT_57
T38 VCCGT_58
T40 VCCGT_59
U34 VCCGT_60
U35 VCCGT_61
U36 VCCGT_62
U37 VCCGT_63
U38 VCCGT_64
U39 VCCGT_65
U40 VCCGT_66
V33 VCCGT_67
V34 VCCGT_68
V36 VCCGT_69
V38 VCCGT_70
V40 VCCGT_71
W34 VCCGT_72
W35 VCCGT_73
W36 VCCGT_74
W37 VCCGT_75
W38 VCCGT_76
Y33 VCCGT_77
Y34 VCCGT_78
Y36 VCCGT_79
Y38 VCCGT_80

VCCGTX_F35 F35
VCCGTX_G34 G34
VCCGTX_G35 G35
VCCGTX_H33 H33
VCCGTX_H34 H34
VCCGTX_J33 J33
VCCGTX_J35 J35
VCCGTX_K32 K32
VCCGTX_K34 K34
VCCGTX_L31 L31
VCCGTX_L33 L33
VCCGTX_M32 M32

VCCGT_SENSE F39 → +VCCGT_VCC_SENSE [12]
VSSGT_SENSE F38 → +VCCGT_VSS_SENSE [12]
F37 TP_+VCCGTX_VCC_SENSE
F36 TP_+VCCGTX_VSS_SENSE

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LGA_1151
<Characteristic>

+VCCGTX

CPU1J

TP26 1 TP_CPU_J8 J8 RSVD_TP_J8
TP27 1 TP_CPU_J7 J7 RSVD_TP_J7
TP29 1 TP_CPU_L8 L8 RSVD_TP_L8
TP30 1 TP_CPU_K8 K8 RSVD_TP_K8
TP31 1 TP_CPU_AV1 AV1 RSVD_TP_AV1
TP32 1 TP_CPU_AW2 AW2 RSVD_TP_AW2
H8 VSS_H8
TP38 1 TP_CPU_K10 K10 RSVD_K10
TP39 1 TP_CPU_L10 L10 RSVD_L10
TP40 1 TP_CPU_J17 J17 RSVD_J17
TP41 1 TP_CPU_B39 B39 RSVD_B39
TP42 1 TP_CPU_J19 J19 RSVD_J19
TP44 1 TP_CPU_C40 C40 RSVD_C40
G8 VSS_G8
AY3 VSS_AY3
[33] PCH_2_CPU_TRIGGER → CPU_2_PCH_TRIGGER_R B3 PROC_TRIGIN
D1 PROC_TRIGOUT
TP49 1 TP_CPU_L12_R1_P_R L12 RSVD_L12
TP50 1 TP_CPU_K12_R1_N_R K12 RSVD_K12

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LGA_1151
<Characteristic>

RSVD_TP_H11 H11 TP_CPU_H11 1 TP33
RSVD_TP_H12 H12 TP_CPU_H12 1 TP28
RSVD_TP_AW38 AW38 TP_CPU_AW38 1 TP34
RSVD_TP_AV39 AV39 TP_CPU_AV39 1 TP35
RSVD_AU39 AU39 TP_CPU_AU39 1 TP36
RSVD_AU40 AU40 TP_CPU_AU40 1 TP37
VSS_AT15 AT15
VSS_AR23 AR23
VSS_AR22 AR22
RSVD_J15 J15 TP_RSVD_CPU_J15 1 TP43
RSVD_J14 J14 TP_RSVD_CPU_J14 1 TP45
RSVD_AU9 AU9 TP_RSVD_CPU_AU9 1 TP46
RSVD_AU10 AU10 TP_RSVD_CPU_AU10 1 TP47
RSVD_J13 J13 TP_RSVD_CPU_J13 1 TP48
RSVD_K13 K13 CPU_LGC_SPARE1
RSVD_J11 J11 LGC_SPARE2
RSVD_D15 D15 TP_CPU_RSVD_D15 1 TP51
RSVD_K11 K11 TP_CPU_RSVD_K11 1 TP52

GND

LGC_SPARE2 — R7795 0402 NL/0 5%_1/16W → DRAMRST#_CPU [26,27,30]
CPU_2_PCH_TRIGGER_R — R7796 0402 20 1%_1/16W → CPU_2_PCH_TRIGGER [33]
[17,18,19,35] +V1.2_DDR_PG → R7797 0402 NL/1.2K 1%_1/16W → CPU_LGC_SPARE1
R7798 NL/560 1%_1/16W 0402 GND

ADVANTECH

Title	24_CPU VCCGT/VCCGTX POWER	
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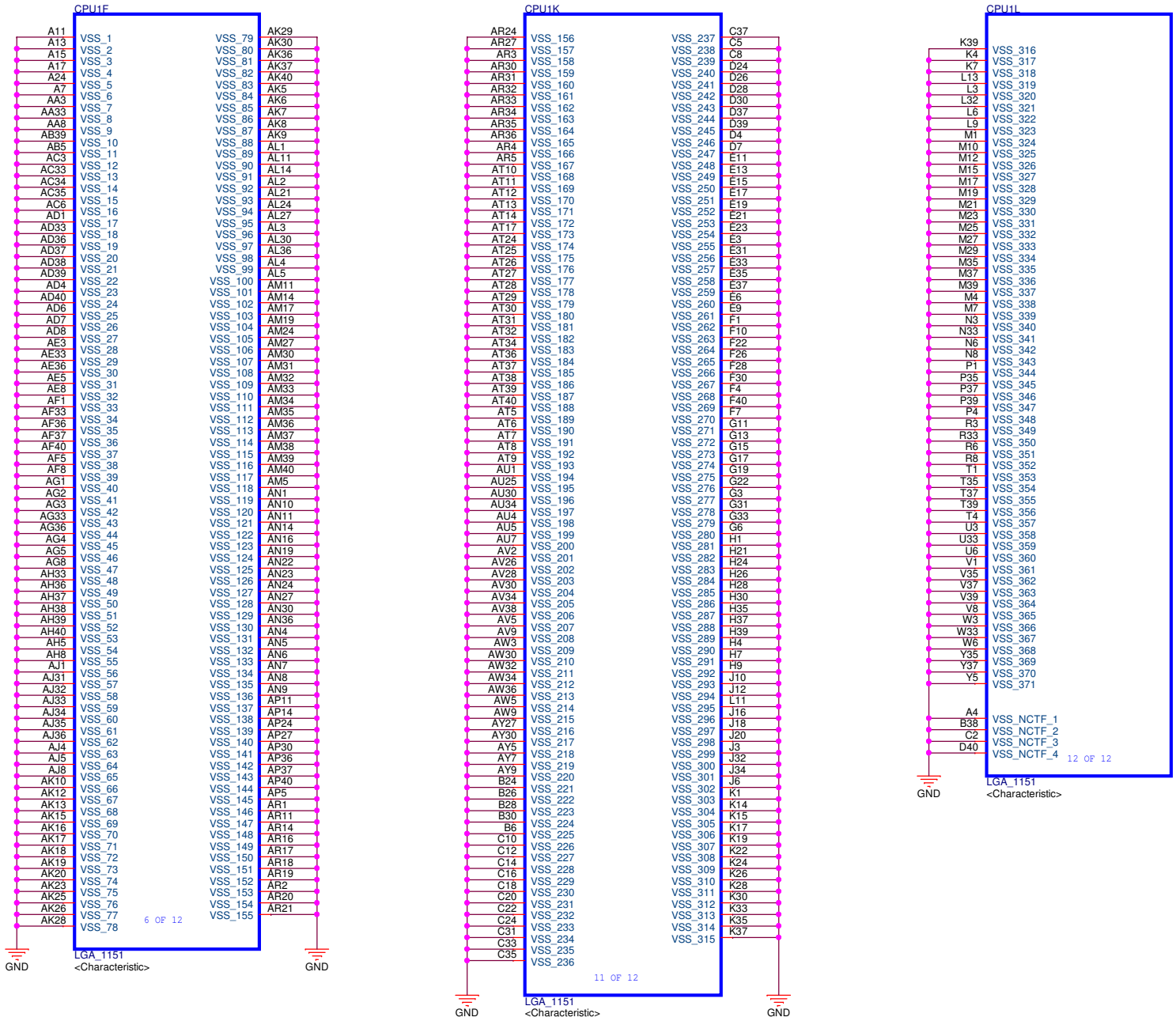
CPU GND



ADVANTECH

Title	25_CPU GND	
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DDR4 SODIMM A1

5.2mm

5.2mm

DIMMA1A

DIMMA1B

M_A_CPU_DQ[63..0] [21]

[21] M_A_CPU_CLKP0
[21] M_A_CPU_CLKN0
[21] M_A_CPU_CLKP1
[21] M_A_CPU_CLKN1
[21] M_A_CPU_CKE0
[21] M_A_CPU_CKE1
[21] M_A_CPU_CS#0
[21] M_A_CPU_CS#1
[21] M_A_CPU_ODT0
[21] M_A_CPU_ODT1
[21] M_A_CPU_BG0
[21] M_A_CPU_BG1
[21] M_A_CPU_BA0
[21] M_A_CPU_BA1
[21] M_A_CPU_MA[16..0] IN
[21] M_A_CPU_ACT#
[21] M_A_CPU_PAR
[21] M_A_CPU_ALERT#
M_A_A1_EVENT#
[24,27,30] DRAMRST#_CPU
M_A_CPU_VREFCA
[27,30] MEM_SMB_DATA_MAIN_2.5V
[27,30] MEM_SMB_CLK_MAIN_2.5V
M_A_A1_SA2
M_A_A1_SA1
M_A_A1_SA0
[21] M_A_CPU_ECC[7..0] IN

CK0_T CK0_C CK1_T CK1_C CKE0 CKE1 S0 S1 ODT0 ODT1 BG0 BG1 BA0 BA1 A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10_AP A11 A12 A13 A14_WE A15_CAS A16_RAS ACT PARITY ALERT EVENT RESET VREFCA SDA SCL SA2 SA1 SA0 CB0_NC CB1_NC CB2_NC CB3_NC CB4_NC CB5_NC CB6_NC CB7_NC DM0/DB10 DM1/DB11 DM2/DB12 DM3/DB13 DM4/DB14 DM5/DB15 DM6/DB16 DM7/DB17 DM8/DB18 S2/C0 S3/C1

DQ0 M_A_CPU_DQ0 … DQ63 M_A_CPU_DQ63

DQS0_T M_A_CPU_DQSP0 … DQS8_T M_A_CPU_DQSP8

DQS0_C M_A_CPU_DQSN0 … DQS8_C M_A_CPU_DQSN8

NPTH_1 NPTH_2 SMDPIX_1 SMDPIX_2

H1 H2 H3 H4 GND

SODIMMDDR4_260
<Characteristic>

Close to SO-DIMM
DRAMRST#_CPU
C7248 NL/100nF 10%_16V 0402 GND

+V1.2_DDR
R7809 240 1%_1/16W 0402

C7251 2.2uF 10%_16V 0603 GND
C7252 100nF 10%_16V 0402 GND

+V2.5_VPP
R8276 NL/0 5%_1/16W 0402
R7799 NL/0 5%_1/16W 0402
R7800 NL/0 5%_1/16W 0402
R8277 0 5%_1/16W 0402
R7801 0 5%_1/16W 0402
R7802 0 5%_1/16W 0402
GND
Co-Lay 3 Pad

C7236 C7237 C7238 C7239 C7240 100nF 10%_16V 0402 GND

+V1.2_DDR
4.755(A)@+V1.2_VDDQ
DDR4 DIMMx2
C7241 C7242 C7243 C7244 1uF 10%_16V 0402 GND

C6956 1uF 10%_16V 0402 GND

+V1.2_DDR
R7807 NL/51.1 1%_1/16W GND

+V1.2_DDR
R7803 0402 1K 1%_1/16W
M_A_VDDQ_VREF
C7245 0.1uF 16V 0402 GND
R7804 1K 1%_1/16W 0402 GND
C7246 0.1uF 16V 0402 GND
R7805 0 5% 0402

[21] M_A_CPU_VREF
R7806 0402 2 1% 1/16W
M_A_CPU_VREFCA
C7247 22nF 10%_50V 0402
M_A_CPU_VREF_RC
R7808 24.9 1%_1/16W 0402 GND

VDD19 VDD18 VDD17 VDD16 VDD15 VDD14 VDD13 VDD12 VDD11 VDD10 VDD9 VDD8 VDD7 VDD6 VDD5 VDD4 VDD3 VDD2 VDD1

VTT VPP2 VPP1 VDDSPD

VSS_1 … VSS_47 VSS_48 … VSS_94

SODIMMDDR4_260
<Characteristic>

0.375(A)@+V0.6_VTT
DDR4 DIMMx2
+V0.6_VTT
C7234 4.7uF 10%_6.3V 0603 GND
C7235 100nF 10%_16V 0402 GND

1.2(A)@+V2.5_VPP
DDR4 DIMMx2
+V2.5_VPP
C7233 100nF 10%_16V 0402 GND
C7232 100nF 10%_16V 0402 GND

+V2.5_VPP
C7249 2.2uF 10%_16V 0603 GND
C7250 100nF 10%_16V 0402 GND

SMB Address
1010 000x

SPD ADDRESS FOR CHANNEL-A DIMMA1 :
WRITE ADDRESS: 0XA0
READ ADDRESS: 0XA1
SA0 =0; SA1 = 0
DDR4 POR OPERATING SPEED:
2400 MT/S
STRETCH GOAL IS 2667 MT/S
'EVENT_N': INDICATES THERMAL EVENT ON DIMM.

CPU
DIMMA1
DIMMB1

M_A_CPU_DQSP[8..0] [21]
M_A_CPU_DQSN[8..0] [21]

Part_Number = 1651002908-01
鴻騰精密科技股份有限公司(Foxconn Interconnect Technology)

alawn0701(OK): change reverse part from 1651002829-01 to 1651002908-01

ADVANTECH

Title	26_DDR4 SODIMM A1	
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DDR4 SODIMM B1

9.2mm

DIMMB1A

M_B_CPU_DQ[63..0] [21]

M_B_CPU_CLKP0 [21]
M_B_CPU_CLKN0 [21]
M_B_CPU_CLKP1 [21]
M_B_CPU_CLKN1 [21]
M_B_CPU_CKE0 [21]
M_B_CPU_CKE1 [21]
M_B_CPU_CS#0 [21]
M_B_CPU_CS#1 [21]
M_B_CPU_ODT0 [21]
M_B_CPU_ODT1 [21]
M_B_CPU_BG0 [21]
M_B_CPU_BG1 [21]
M_B_CPU_BA0 [21]
M_B_CPU_BA1 [21]
M_B_CPU_MA[16..0] [21] IN

Close to SO-DIMM
DRAMRST#_CPU
C7276 NL/100nF 10%_16V 0402 GND

+V1.2_DDR
R7819 240 1%_1/16W 0402
M_B_CPU_ACT# [21]
M_B_CPU_PAR [21]
M_B_CPU_ALERT# [21]
M_B_B1_EVENT#
[24,26,30] DRAMRST#_CPU
M_B_CPU_VREFCA

C7279 2.2uF 10%_16V 0603 GND
C7280 100nF 10%_16V 0402 GND
[26,30] MEM_SMB_DATA_MAIN_2.5V
[26,30] MEM_SMB_CLK_MAIN_2.5V

M_B_B1_SA2
M_B_B1_SA1
M_B_B1_SA0

M_B_CPU_ECC[7..0] [21] IN

SMB Address

1010 010x

+V2.5_VPP +V2.5_VPP +V2.5_VPP

R8279 NL/0 5%_1/16W 0402
R7810 0 5%_1/16W 0402
R7811 NL/0 5%_1/16W 0402
R8278 0 5%_1/16W 0402
R7812 NL/0 5%_1/16W 0402
R7813 0 5%_1/16W 0402
M_B_B1_SA2
M_B_B1_SA1
M_B_B1_SA0
GND GND GND
Co-Lay 3 Pad Co-Lay 3 Pad Co-Lay 3 Pad

+V1.2_DDR

SODIMMDDR4_260
<Characteristic>

9.2mm

DIMMB1B

C7257 C7258 C7259 C7260 C7261 100nF 10%_16V 0402 GND

+V1.2_DDR
4.755(A)@+V1.2_VDDQ
DDR4 DIMMx2
C7262 C7263 C7264 C7265 1uF 10%_16V 0402 GND
C7268 C7269 C7270 C7271 C7272 22uF 6.3V 0805 GND

+V1.2_DDR
R7814 1K 1%_1/16W 0402
C7266 0.1uF 16V 0402 GND
M_B_VDDQ_VREF
R7815 1K 1%_1/16W 0402 GND
C7267 NL/0.1uF 16V 0402 GND
R7816 0 5% 0402
[21] M_B_CPU_VREF
R7817 0402 2 1%_1/16W
M_B_CPU_VREFCA
C7273 22nF 10%_50V 0402
M_B_CPU_VREF_RC
R7818 24.9 1%_1/16W 0402 GND
C7274 C7275 0.1uF 16V 0402 GND

0.375(A)@+V0.6_VTT
DDR4 DIMMx2
+V0.6_VTT
C7255 4.7uF 10%_6.3V 0603 GND
C7256 100nF 10%_16V 0402 GND

1.2(A)@+V2.5_VPP
DDR4 DIMMx2
+V2.5_VPP
C7253 C7254 100nF 10%_16V 0402 GND

+V2.5_VPP
C7277 2.2uF 10%_16V 0603 GND
C7278 100nF 10%_16V 0402 GND

SODIMMDDR4_260
<Characteristic>

SPD ADDRESS FOR CHANNEL-B DIMMB1 :
WRITE ADDRESS: 0XA4
READ ADDRESS: 0XA5
SA0 =0; SA1 = 1
DDR4 POR OPERATING SPEED:
2400 MT/S

STRETCH GOAL IS 2667 MT/S
'EVENT_N': INDICATES THERMAL
EVENT ON DIMM.

CPU

DIMMA1 DIMMB1

M_B_CPU_DQSP[8..0] [21]
M_B_CPU_DQSN[8..0] [21]

Part_Number = 1651002909-01

鴻騰精密科技股份有限公司(Foxconn Interconnect Technology)

alawn0701(OK): change reverse part from 1651002828-01 to 1651002909-01

ADVANTECH

Title	27_DDR4 SODIMM B1	
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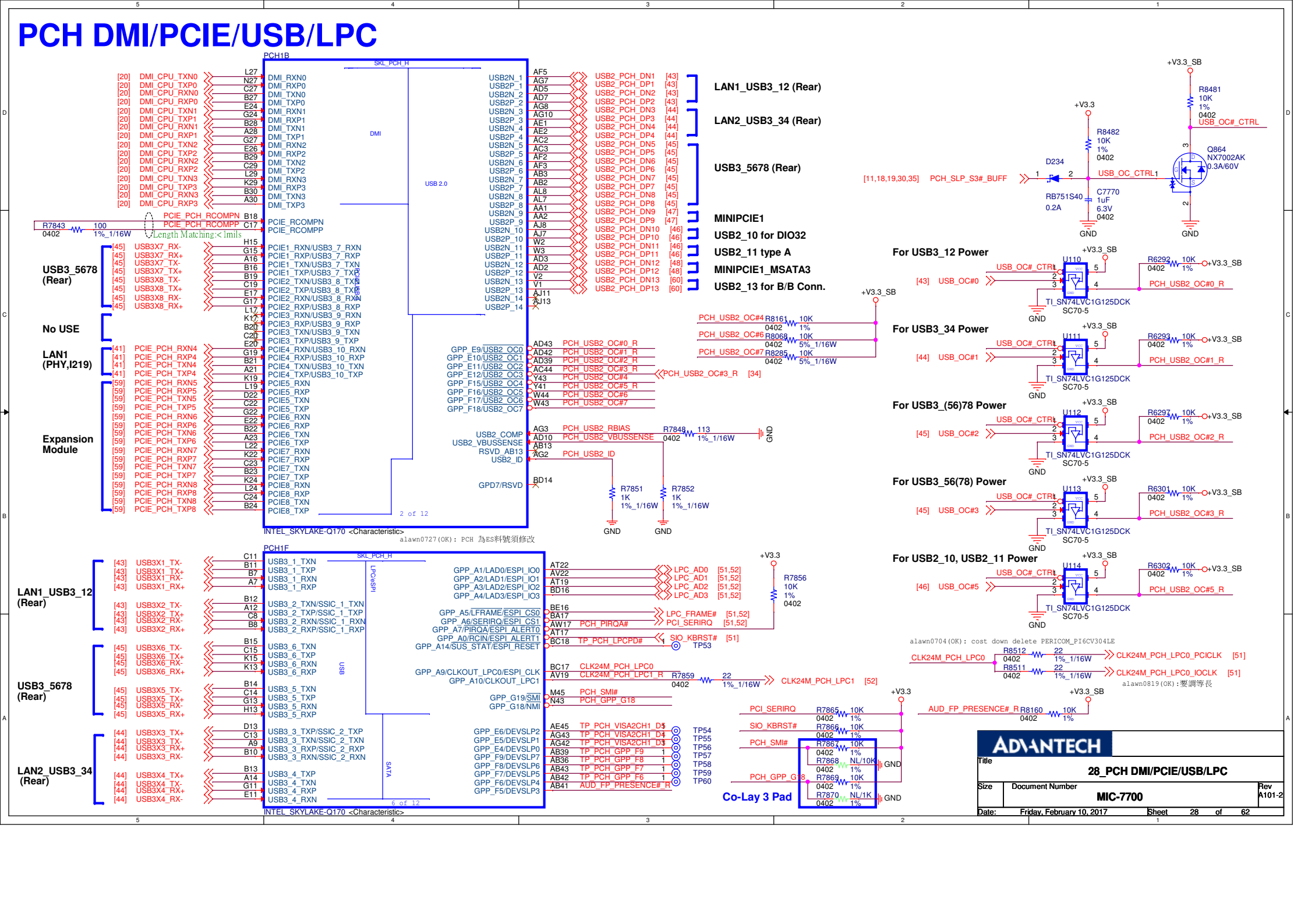
PCH DMI/PCIE/USB/LPC



PCH PCIE/SATA/DDC

PCH1C — SKL_PCH_H — INTEL_SKYLAKE-Q170 <Characteristic> — 3 of 12

CLINK: CL_CLK, CL_DATA, CL_RST

FAN: GPP_G8/FAN_PWM_0, GPP_G9/FAN_PWM_1, GPP_G10/FAN_PWM_2, GPP_G11/FAN_PWM_3, GPP_G0/FAN_TACH_0, GPP_G1/FAN_TACH_1, GPP_G2/FAN_TACH_2, GPP_G3/FAN_TACH_3, GPP_G4/FAN_TACH_4, GPP_G5/FAN_TACH_5, GPP_G6/FAN_TACH_6, GPP_G7/FAN_TACH_7

PCIe/SATA: PCIE11_TXP, PCIE11_TXN, PCIE11_RXP, PCIE11_RXN, GPP_F10/SCLOCK, GPP_F11/SLOAD, GPP_F13/SDATAOUT0, GPP_F12/SDATAOUT1, PCIE14_TXN/SATA1B_TXN, PCIE14_TXP/SATA1B_TXP, PCIE14_RXN/SATA1B_RXN, PCIE14_RXP/SATA1B_RXP, PCIE13_TXN/SATA0B_TXN, PCIE13_TXP/SATA0B_TXP, PCIE13_RXN/SATA0B_RXN, PCIE13_RXP/SATA0B_RXP, PCIE12_TXP, PCIE12_TXN, PCIE12_RXP, PCIE12_RXN, PCIE20_TXP/SATA7_TXP, PCIE20_TXN/SATA7_TXN, PCIE20_RXP/SATA7_RXP, PCIE20_RXN/SATA7_RXN, PCIE19_TXP/SATA6_TXP, PCIE19_TXN/SATA6_TXN, PCIE19_RXP/SATA6_RXP, PCIE19_RXN/SATA6_RXN

HOST: GPP_F21/EDP_BKLTCTL, GPP_F20/EDP_BKLTEN, GPP_F19/EDP_VDDEN, THERMTRIP, PECI, PM_SYNC, PLTRST_PROC, PM_DOWN

PCIE9_RXN/SATA0A_RXN [42] — PCIE9_RXP/SATA0A_RXP [42] — PCIE9_TXN/SATA0A_TXN [42] — PCIE9_TXP/SATA0A_TXP [42] → **LAN2 (I210)**

PCIE10_RXN/SATA1A_RXN [47] — PCIE10_RXP/SATA1A_RXP [47] — PCIE10_TXN/SATA1A_TXN [47] — PCIE10_TXP/SATA1A_TXP [47] → **MINIPCIE1**

PCIE15_RXN/SATA2_RXN [49] — PCIE15_RXP/SATA2_RXP [49] — PCIE15_TXN/SATA2_TXN [49] — PCIE15_TXP/SATA2_TXP [49] → **CFAST1**

PCIE16_RXN/SATA3_RXN [48] — PCIE16_RXP/SATA3_RXP [48] — PCIE16_TXN/SATA3_TXN [48] — PCIE16_TXP/SATA3_TXP [48] → **MINIPCIE1_MSATA3**

PCIE17_RXN/SATA4_RXN [49] — PCIE17_RXP/SATA4_RXP [49] — PCIE17_TXN/SATA4_TXN [49] — PCIE17_TXP/SATA4_TXP [49] → **SATA4**

PCIE18_RXN/SATA5_RXN [49] — PCIE18_RXP/SATA5_RXP [49] — PCIE18_TXN/SATA5_TXN [49] — PCIE18_TXP/SATA5_TXP [49] → **SATA5**

GPP_E8/SATALED — SATA_PCH_LED# [56]

GPP_E0/SATAXPCIE0/SATAGP0 — SATAXPCIE0
GPP_E1/SATAXPCIE1/SATAGP1 — SATAXPCIE1
GPP_E2/SATAXPCIE2/SATAGP2 — SATAXPCIE2
GPP_F0/SATAXPCIE3/SATAGP3 — SATAXPCIE3 — R8038 0 5%_1/16W — NEW_PU_3.3 — MINIPCIE2_MSATA [48]
GPP_F1/SATAXPCIE4/SATAGP4 — SATAXPCIE4 0402
GPP_F2/SATAXPCIE5/SATAGP5 — SATAXPCIE5
GPP_F3/SATAXPCIE6/SATAGP6 — PCH_GPP_F3
GPP_F4/SATAXPCIE7/SATAGP7 — PCH_GPP_F4

COM2_TERM [53] — COM2_MODE0 [53] — COM2_MODE1 [53]

PCH_THERMTRIP#_R — PCH_THERMTRIP# [22]
PCH_PECI — PECI [22]
PCH_PM_SYNC_R — PCH_PM_SYNC [22]
PCH_PLTRST_CPU# [22]
CPU_PM_DOWN [22]

C7332 NL/470pF 5%_50V — GND
R7890 NL/1K 1% 0402 — GND

alawn0711(OK): Ref CRB NL/

PCH1E — SKL_PCH_H — INTEL_SKYLAKE-Q170 <Characteristic> — 5 of 12

GPP_I0/DDPB_HPD0 — AW4 — [37] DDPB_HPD
GPP_I1/DDPC_HPD1 — AY2 — [38] DDPC_HPD
GPP_I2/DDPD_HPD2 — AV4 — [39] DDPD_HPD
GPP_I3/DDPE_HPD3 — BA4 — [40] DDPE_VGA_HPD
EDP_HPD — BD7 — GPP_I4/EDP_HPD

GPP_I7/DDPC_CTRLCLK — BB3 — DDPC_CLK [38]
GPP_I8/DDPC_CTRLDATA — BD6 — DDPC_DATA [38]
GPP_I5/DDPB_CTRLCLK — BA5 — DDPB_CLK [37]
GPP_I6/DDPB_CTRLDATA — BC4 — DDPB_DATA [37]
GPP_I9/DDPD_CTRLCLK — BE5 — DDPD_CLK [39]
GPP_I10/DDPD_CTRLDATA — BE6 — DDPD_DATA [39]

GPP_F14 — Y44 — H_SKTOCC#_R
GPP_F23 — V44 — PCH_VCORE_VBOOST_CTRL
GPP_F22 — W39 — GPP_F22
GPP_G23 — L43 — PCH_IVCAM_DFU
GPP_G22 — L44 — TP_PCH_PEGSLOT1_PWREN1 — TP65
GPP_G21 — U35 — PCH_SPI_TPM_PIRQ
GPP_G20 — R35 — PCH_TEST_SETUP_MENU
GPP_H23 — BD36 — PCH_AMT_LED

DDPC_HPD — R8550 1M 5% 0402 — +V3.3
DDPD_HPD — R8582 1M 5% 0402 — +V3.3

H_SKTOCC#_R — R7879 0 5%_1/16W 0402 — H_SKTOCC# [22]

DDPB_CLK — R7882 2.2K 1% 0402 — +V3.3
DDPB_DATA — R7883 2.2K 1% 0402 — +V3.3

DDPB_CTRLDATA
This signal has a weak internal pull-down.
LOW:Port B is not detected. (Default)
HIGH:Port B is detected.

DDPC_CLK — R7885 2.2K 1% 0402
DDPC_DATA — R7886 2.2K 1% 0402

DDPC_CTRLDATA
This signal has a weak internal pull-down.
LOW:Port C is not detected. (Default)
HIGH:Port C is detected.

DDPD_CLK — R7887 2.2K 1% 0402
DDPD_DATA — R7888 2.2K 1% 0402

DDPD_CTRLDATA
This signal has a weak internal pull-down.
LOW:Port D is not detected. (Default)
HIGH:Port D is detected.

PCH_VCORE_VBOOST_CTRL — R7889 10K 1% 0402
EDP_HPD — R7884 100K 1% 1/16W 0402 — GND

GPP_F22 — R7834 10K 1% 0402 — +V3.3
PCH_IVCAM_DFU — R7904 10K 0402 1% — GND
PCH_TEST_SETUP_MENU — R7906 NL/10K 0402 1% — GND
R7909 10K 0402 1%
R7911 NL/0 0402 5% — GND

Co-Lay 3 Pad

(Default)

TEST SETUP MENU	BOARD STYLE
0	TEST SETUP MENU ENABLED
1	DISABLED

PCH_SPI_TPM_PIRQ — R7895 8.2K 5% 1/16W 0402 — +V3.3_SB
PCH_AMT_LED — R7901 10K 1% 0402

alawn0819: 確認PCH_CONFIG_JUMPER的準位(EDS)，為何上件的表格是反的

alawn0704: what's this

RA: [30,34,50,58] PCH_SPKR — R7919 NL/2.2K 0402 1% — PCH_CONFIG_JUMPER
RB: [31,34] PCH_GSPI0_MOSI — R7920 NL/2.2K 0402 1%
R7918 1K 1% 1/16W — +V3.3
R7921 10K 1% 0402 — GND

STUFF RA FOR LPT-H
STUFF RB FOR SKL PCH H

RECOVER/CONFIGURE	MODE
Stuff RC, Not Stuff RA & RB	NORMAL
Not Stuff RA & RB & RC	CONFIGURE
Not Stuff RA & RB & RC	RECOVERY (Default)

B/B Conn: [60] PCIE_PCH_TXP11, [60] PCIE_PCH_TXN11, [60] PCIE_PCH_RXP11, [60] PCIE_PCH_RXN11

alawn0628(OK): AB33 MIC-7500 is PCH_BIOS_RE

PCH_CONFIG_JUMPER — AB33
PCH_RSVD — AB35
PCH_GP39_GFX_CRB_DETECT — AA44
PCH_SV_ADVANCE_GP48 — AA45

SATA1: [59] SATA_PCH_TXN1, [59] SATA_PCH_TXP1, [59] SATA_PCH_RXN1, [59] SATA_PCH_RXP1

SATA0: [49] SATA_PCH_TXN0, [49] SATA_PCH_TXP0, [49] SATA_PCH_RXN0, [49] SATA_PCH_RXP0

B/B Conn: [60] PCIE_PCH_TXP12, [60] PCIE_PCH_TXN12, [60] PCIE_PCH_RXP12, [60] PCIE_PCH_RXN12

B/B Conn: [60] PCIE_PCH_TXP20, [60] PCIE_PCH_TXN20, [60] PCIE_PCH_RXP20, [60] PCIE_PCH_RXN20

B/B Conn: [60] PCIE_PCH_TXP19, [60] PCIE_PCH_TXN19, [60] PCIE_PCH_RXP19, [60] PCIE_PCH_RXN19

PCB_ID0 R44 — PCB_ID1 R43 — PCB_ID2 U39 — TP63 — 1 TP_PCH_GPP_G11 N42
GPIO for BIOS Control

[53] COM1_TERM — U43
[53] COM1_MODE0 — U42
[53] COM1_MODE1 — U41
[40] VGA1_DVI1_OC# — M44
[38] DP1_OC# — U36
PCH_SV_DETECT — P44
[51,56] OVT_LED#_SIO — T45
[39] DP2_OC# — T44

GFX SELECT	
	GFX STYLE
0	NORMAL GFX (Default)
1	CUSTOMER GFX

SV ADVANCE	
	BOARD STYLE
1	NORMAL MENU (Default)
0	SV ADVANCE MENU

SATA_PCH_LED# — R7891 10K 1% 0402 — +V3.3
PCH_GPP_F3 — R8513 NL/10K 1% 0402
PCH_GPP_F4 — R7849 NL/10K 1% 0402
PCH_PM_SYNC_R — R7912 30 1% 1/16W 0402 — PCH_PM_SYNC [22]

+V1.0_VCCST_VCCPLL — R7753 75 1% 1/16W 0402 — Place Close to PCH

alawn0819(OK): PDG suggest 1K, 使用75ohm使PCH_THERMTRIP#較大較不易受到干擾
PCH_THERMTRIP#_R — R7914 560 1% 1/16W 0402 — PCH_THERMTRIP# [22]

OVT_LED#_SIO — R7915 10K 0402 1%
PCH_SV_DETECT — R7916 NL/10K 0402 1%
R7917 10K 0402 1% — GND
PCH_RSVD — R7922 10K 0402 1%
R7923 NL/0 0402 5% — GND
PCH_GP39_GFX_CRB_DETECT — R7924 NL/10K 0402 1%
R7925 10K 0402 1% — GND
PCH_SV_ADVANCE_GP48 — R7926 20K 0402 1%
R7927 NL/0 0402 5% — GND
DP2_OC# — R8533 NL/20K 0402 1%
R8534 NL/0 0402 5% — GND
A101-2.16

Co-Lay 3 Pad

alawn0819: 不用時是GPIO, default是in or out

SATAXPCIE0 — R8518 10K 0402 1%_1/16W — SATA0B / PCIe13: PCIe SATAXPCIE0 pin is '0' / SATA SATAXPCIE0 pin is '1' (default)
SATAXPCIE1 — R8519 10K 0402 1%_1/16W — SATA1B / PCIe14: PCIe SATAXPCIE1 pin is '0' / SATA SATAXPCIE1 pin is '1' (default)
SATAXPCIE2 — R8514 NL/10K 0402 1%_1/16W — R7412 NL/10K 0402 1%_1/16W — GND — SATA2 / PCIe15: SATA SATAXPCIE2 pin is '0' / PCIe SATAXPCIE2 pin is '1' (default)
SATAXPCIE3 — R8515 NL/10K 0402 1%_1/16W — R7413 NL/10K 0402 1%_1/16W — GND — SATA3 / PCIe16: SATA SATAXPCIE3 pin is '0' / PCIe SATAXPCIE3 pin is '1' (default)
SATAXPCIE4 — R8516 NL/10K 0402 1%_1/16W — R7414 NL/10K 0402 1%_1/16W — GND — SATA4 / PCIe17: SATA SATAXPCIE4 pin is '0' / PCIe SATAXPCIE4 pin is '1' (default)
SATAXPCIE5 — R8071 NL/10K 0402 1%_1/16W — R8517 NL/10K 0402 1%_1/16W — GND — SATA5 / PCIe18: PCIe SATAXPCIE5 pin is '0' / SATA SATAXPCIE5 pin is '1' (default)

alawn0704: 是否要PU, check with EDS

Co-Lay 3 Pad

alawn0819(OK): 追加一組PCB_ID2

PCB_ID0 — R8245 NL/10K 0402 1% — GND
PCB_ID1 — R8246 10K 0402 1% — GND
PCB_ID2 — R7876 NL/10K 0402 1% — GND
R8247 10K 0402 1% — GND
R8599 NL/10K 0402 1%
R8600 10K 0402 1% — GND

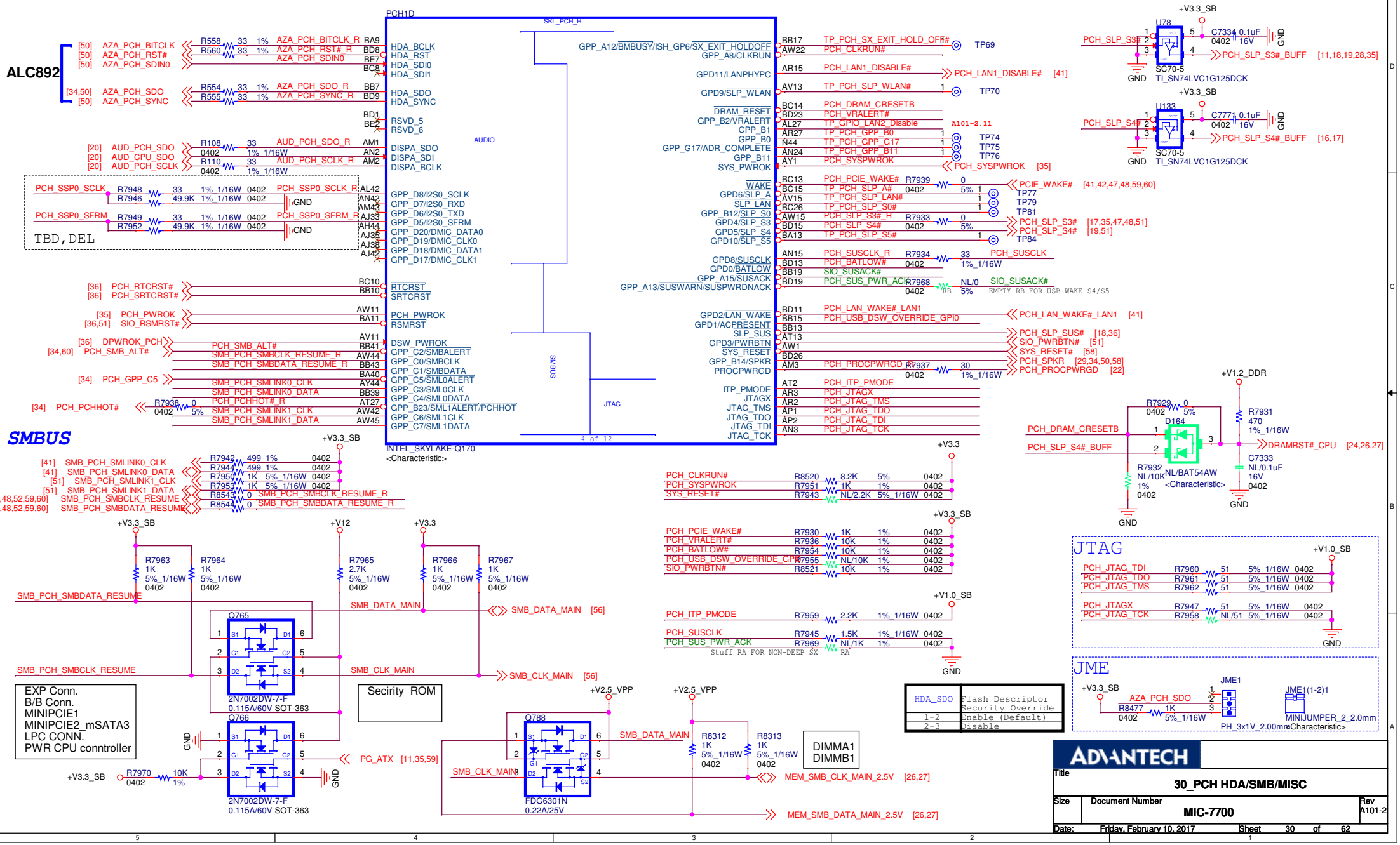
Co-Lay 3 Pad

Project	MIC-7700H	MIC-7700Q
PCB_ID0	0	1
PCB_ID1	0	0
PCB_ID2	0	0

ADVANTECH

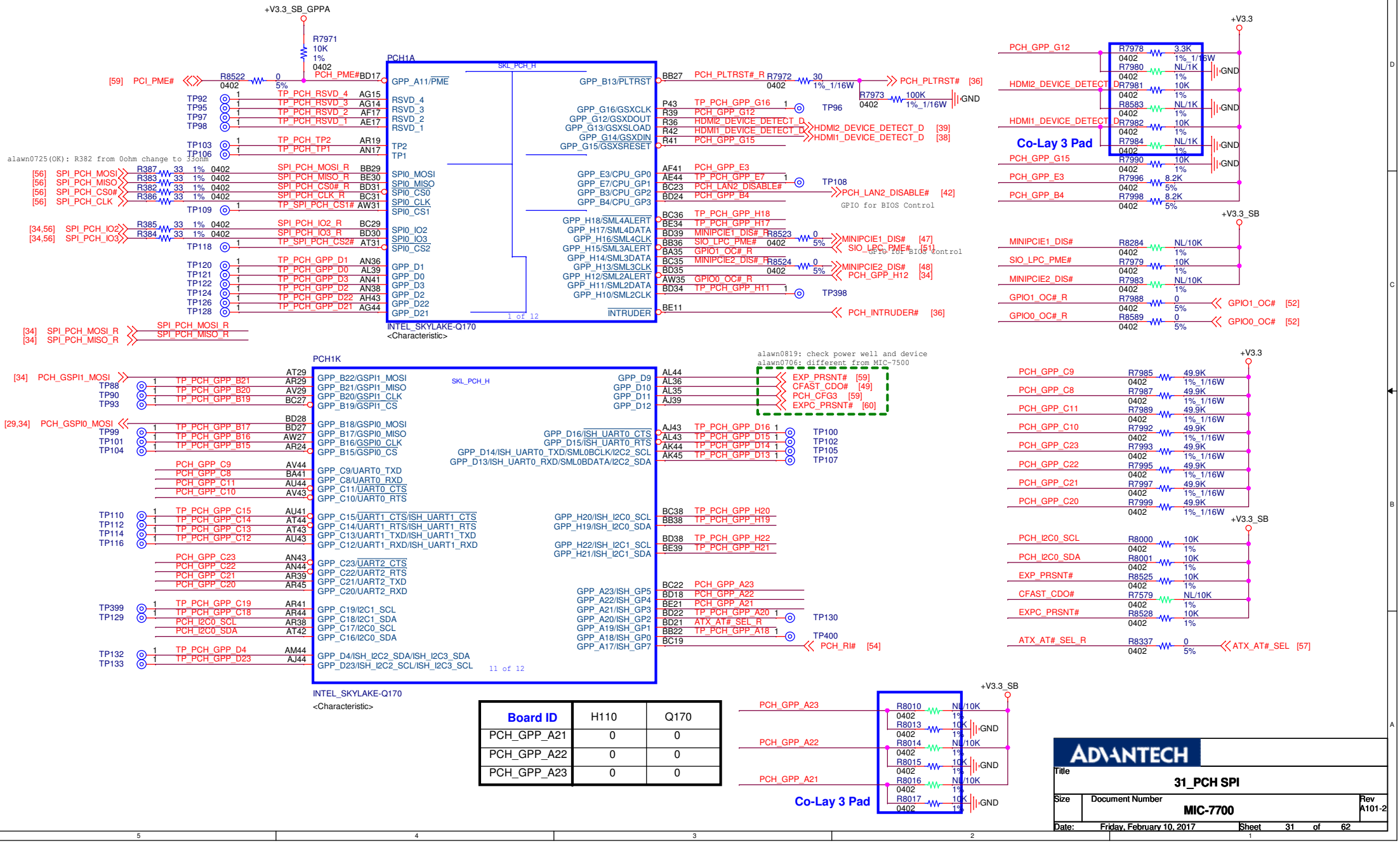
Title	29_PCH PCIE/SATA/DDC	
Size	Document Number: MIC-7700	Rev: A101-2
Date: Friday, February 10, 2017	Sheet 29 of 62	

PCH HDA/SMB/MISC



Title	30_PCH HDA/SMB/MISC
Size	Document Number: MIC-7700
Rev	A101-2
Date:	Friday, February 10, 2017
Sheet	30 of 62

PCH SPI

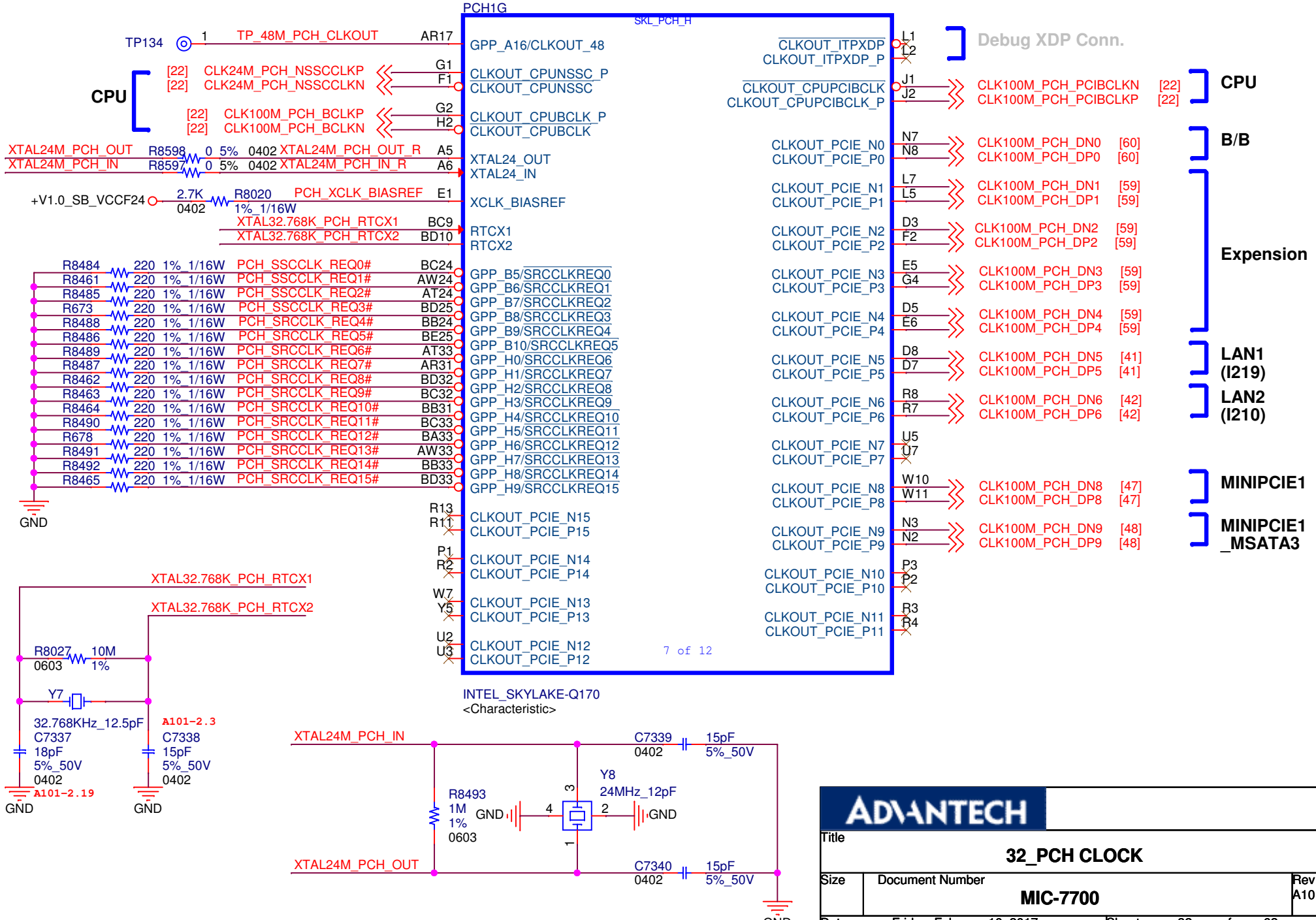


Board ID	H110	Q170
PCH_GPP_A21	0	0
PCH_GPP_A22	0	0
PCH_GPP_A23	0	0

ADVANTECH

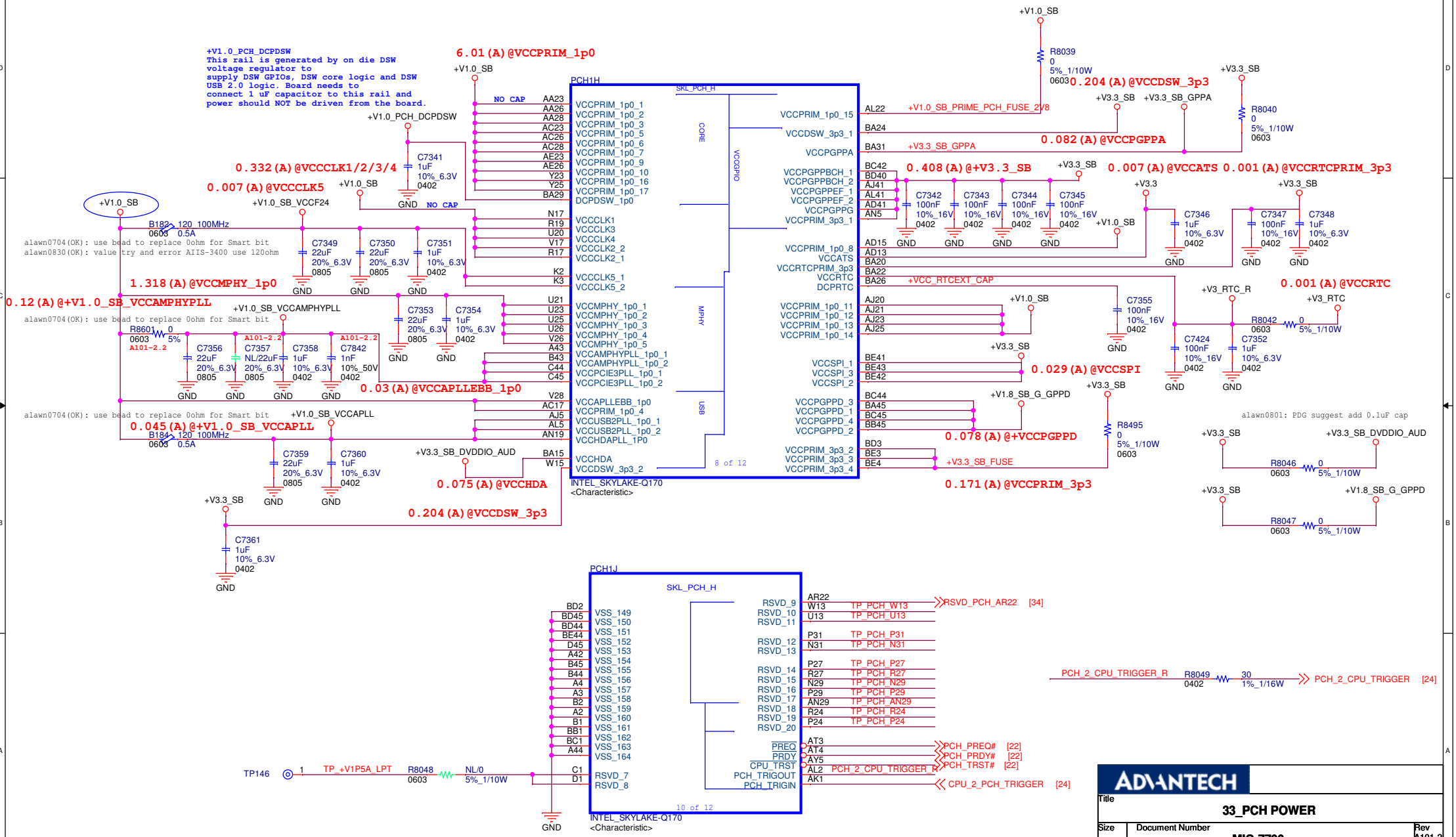
Title	31_PCH SPI	
Size	Document Number: MIC-7700	Rev: A101-2
Date: Friday, February 10, 2017	Sheet 31 of 62	

PCH CLOCK



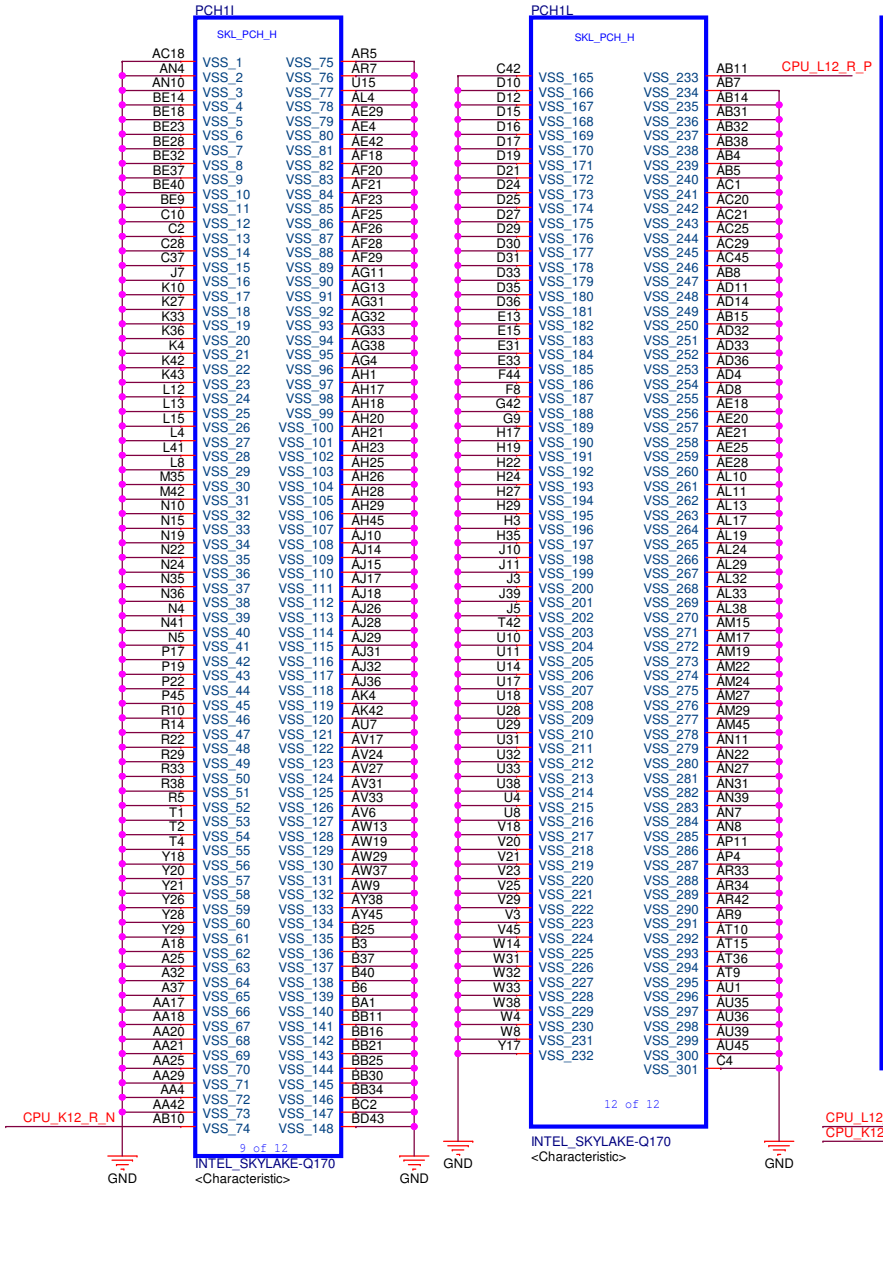
ADVANTECH		
Title	32_PCH CLOCK	
Size	Document Number MIC-7700	Rev A101-2
Date: Friday, February 10, 2017	Sheet 32 of 62	

PCH POWER



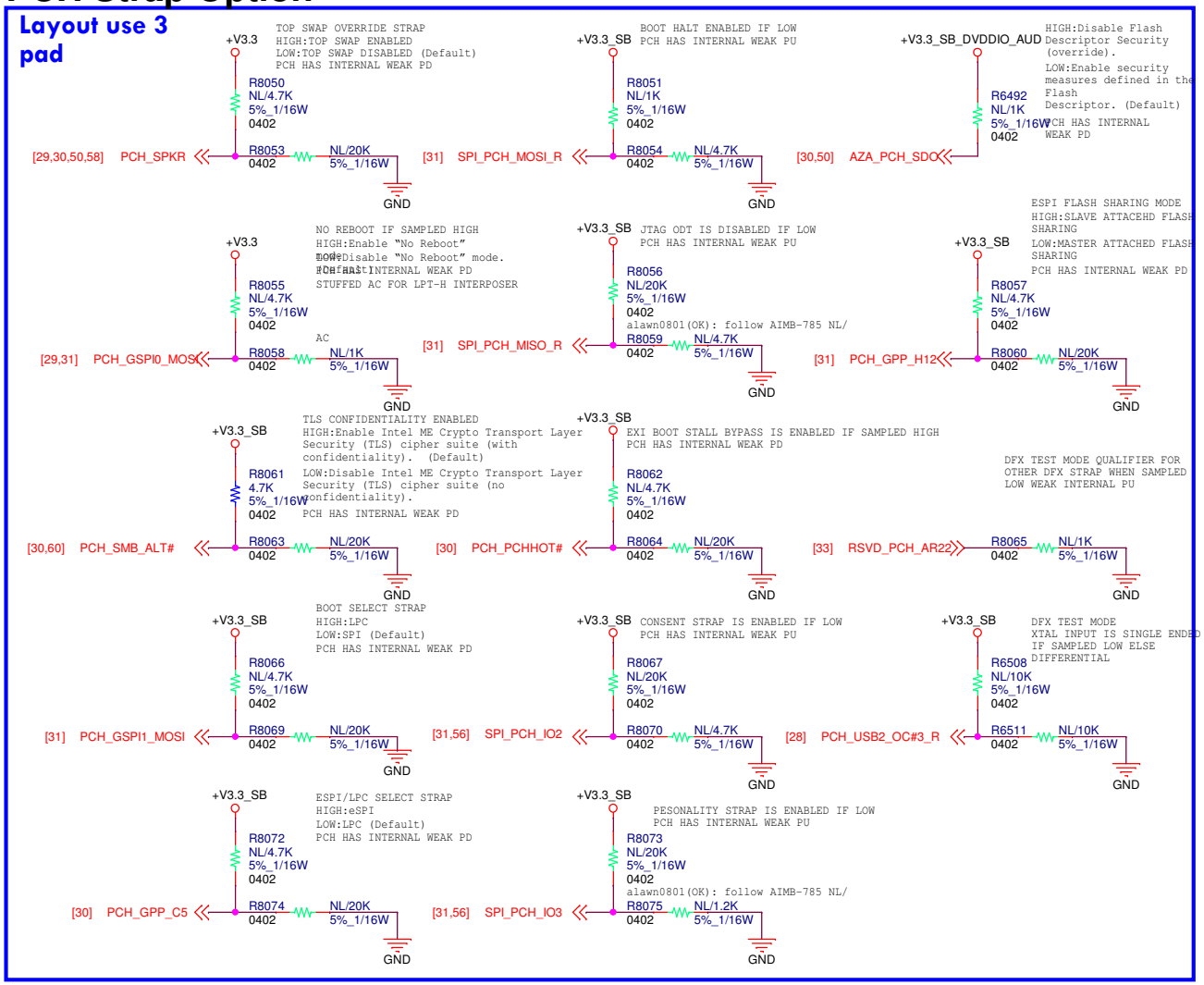
Title	33_PCH POWER		
Size	Document Number	MIC-7700	Rev A101-2
Date:	Friday, February 10, 2017	Sheet 33 of 62	

PCH GND/PCH Strap Option



PCH Strap Option

Layout use 3 pad



ADVANTECH

Title	34_PCH GND/PCH Strap Option	
Size	Document Number MIC-7700	Rev A101-2
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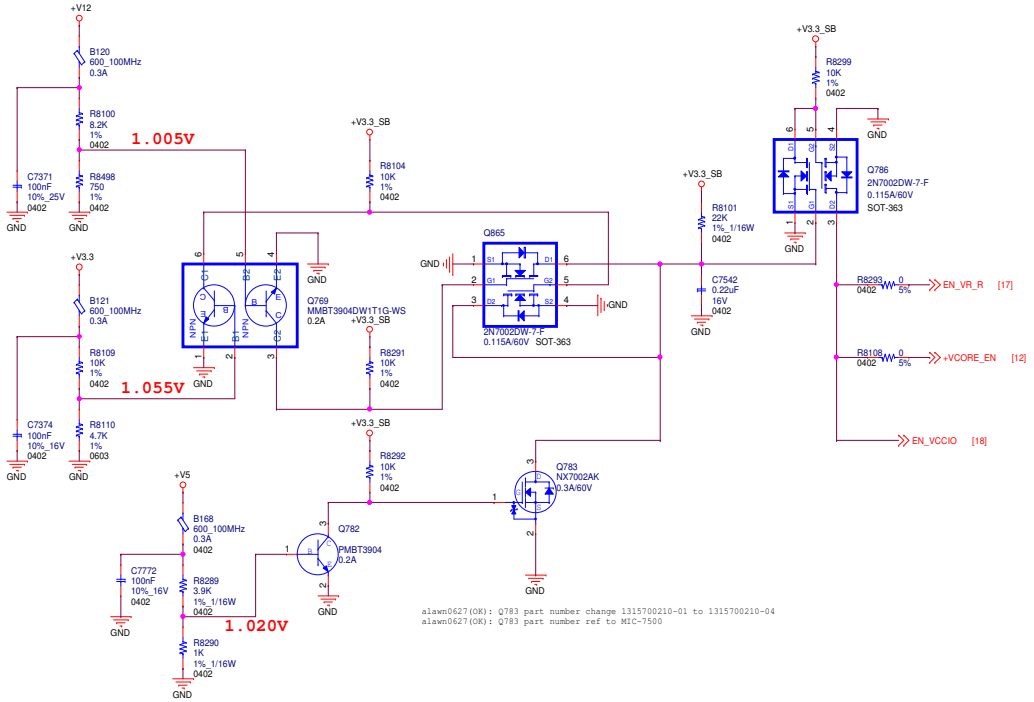
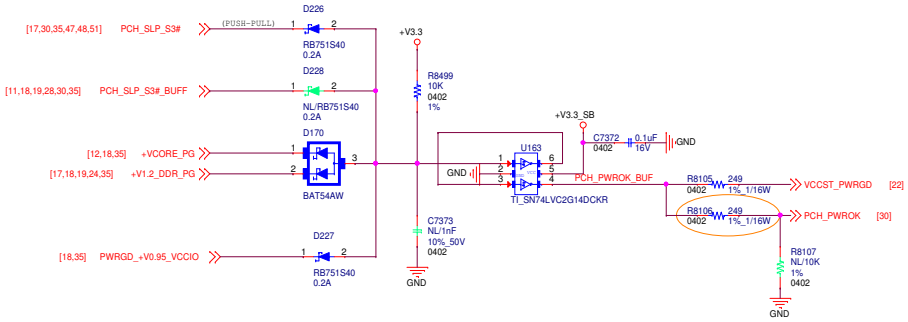
VCCIOEN/VREN/POK/SYSPOK

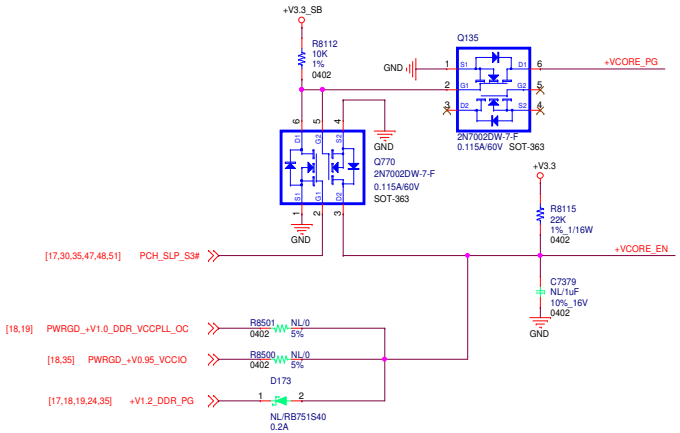
Main Power Ready



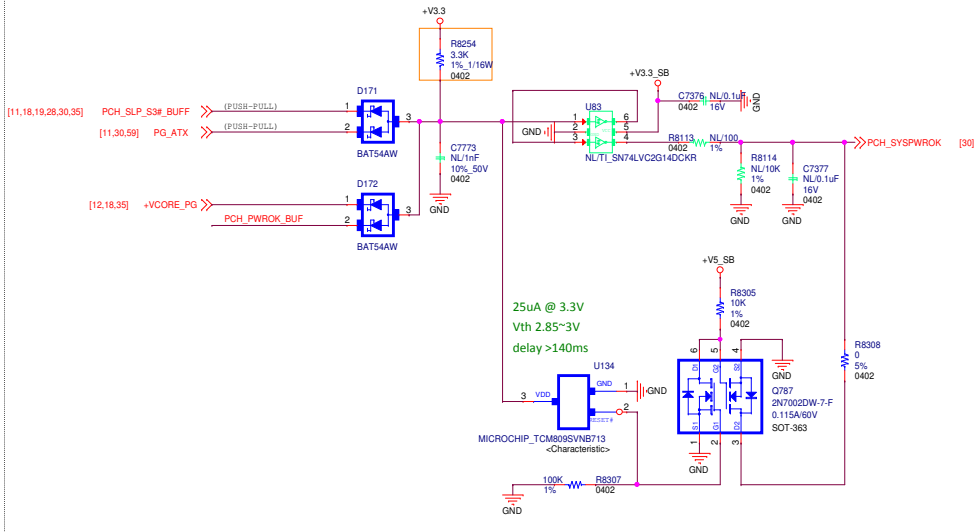
PWROK



VR_EN



SYS_PWROK



ADVANTECH

Title	35_VCCIOEN/VREN/POK/SYSPOK	
Size	Document Number: MIC-7700	Rev: A101-2
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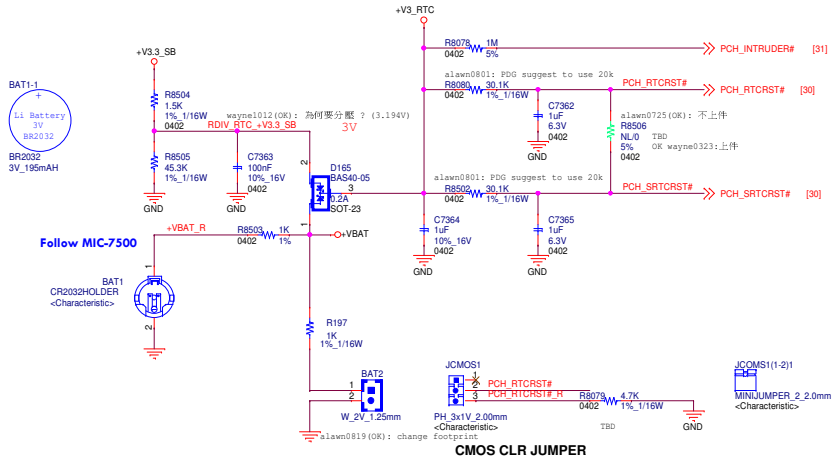
RTCRST#/RSMRST#/PLTRST#

RTCRST#

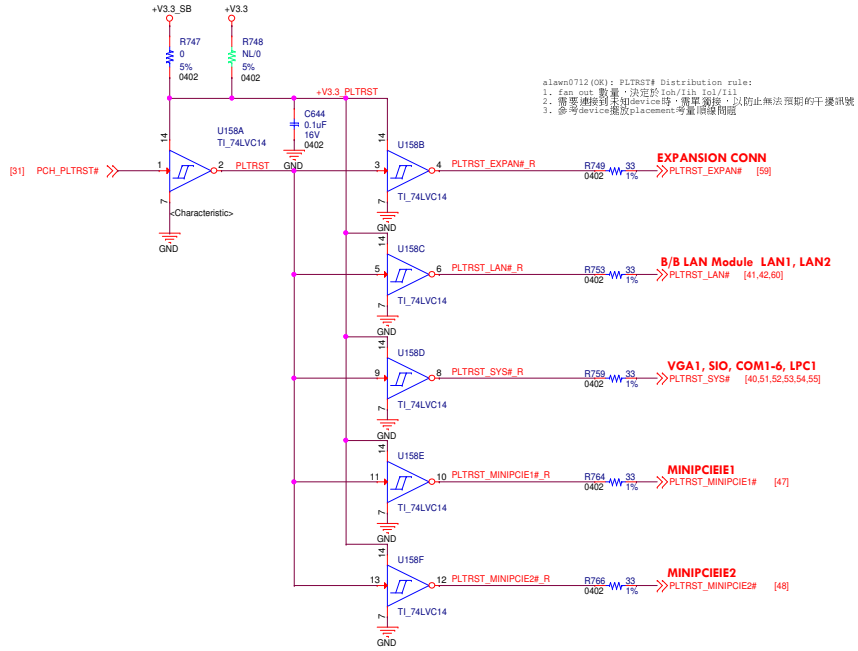


CMOS CLR JUMPER

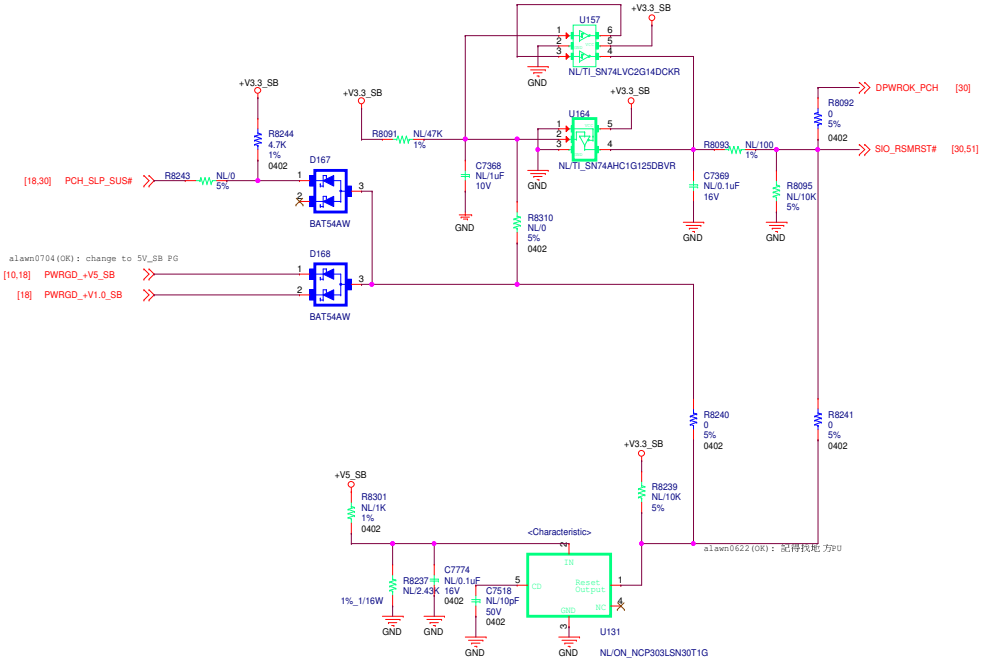
Mode	Jumper Setting
Normal (Default)	1-2
CLR CMOS	2-3

PLTRST#

alawn0819(OK): PU 3.3V可能會當3.3V陡升太緩，使得IC坐落在unknow區，有機會使IC誤動作，造成glitch
alawn0629(OK): MIC-7500 is PU +V3.3



RSMRST#



Title	36_RTCRST#/RSMRST#/PLTRST#		
Size	Document Number	MIC-7700	Rev A101-2
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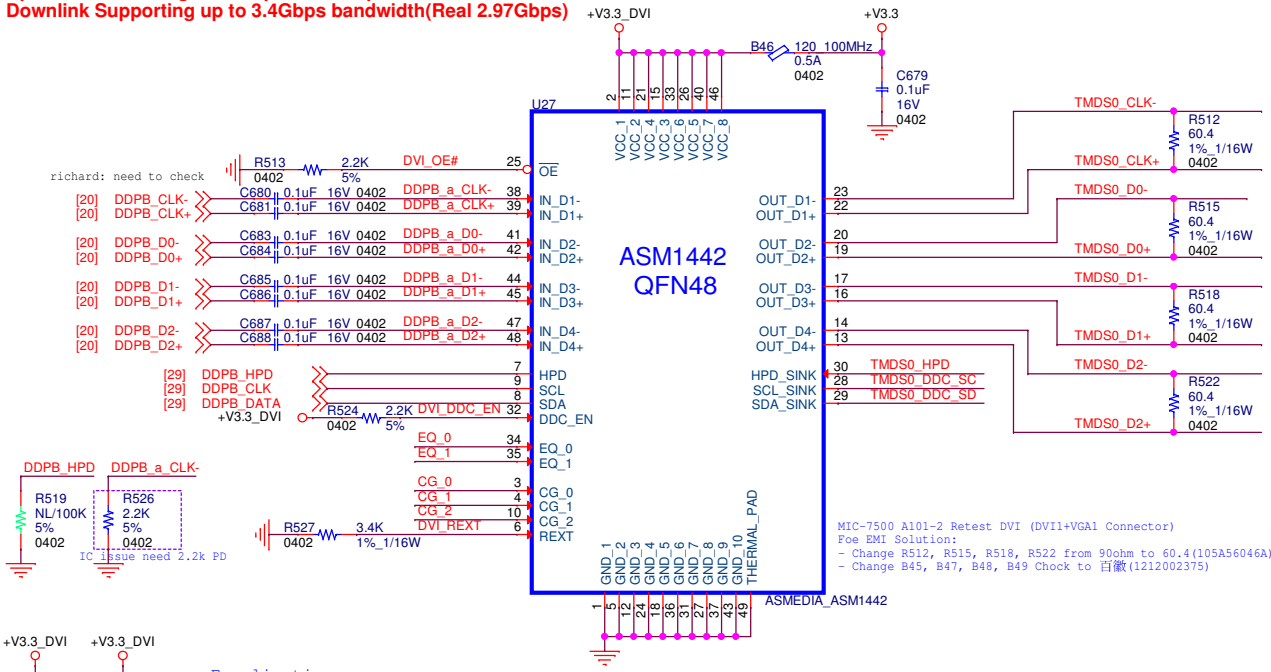
Display DVI1/Level Shifter

Uplink Nominal range 250Mbps to 2.5Gbps
Downlink Supporting up to 3.4Gbps bandwidth(Real 2.97Gbps)

0.1(A)@+V3.3_DVI



MIC-7500 A101-2 Retest DVI (DVI1+VGA1 Connector)
Foe EMI Solution:
- Change R512, R515, R518, R522 from 90ohm to 60.4(105A56046A)
- Change B45, B47, B48, B49 Chock to 百徽(1212002375)

DDPB_HPD DDPB_a_CLK-
R519 NL/100K 5% 0402
R526 2.2K 5% 0402
IC issue need 2.2k PD

+V3.3_DVI +V3.3_DVI
R497 NL/2.2K 5% 0402 EQ_0
R498 NL/2.2K 5% 0402 EQ_1
R503 NL/2.2K 5% 0402
R504 NL/2.2K 5% 0402
Co-Lay 3 Pad

Equalization

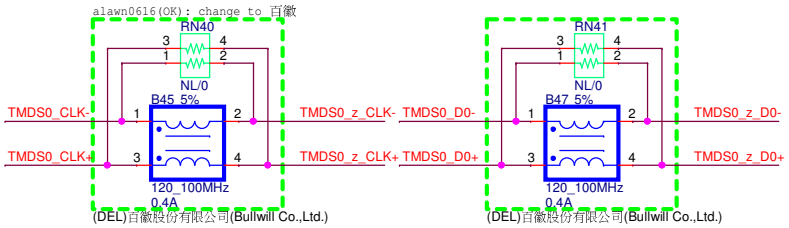
EQ_1	EQ_0	
0	0	12dB
0	1	9dB
1	0	6dB
1	1	3dB (default)

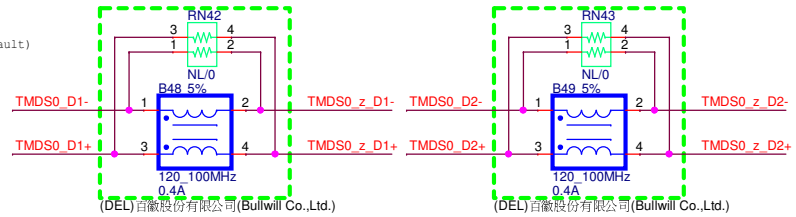
+V3.3_DVI +V3.3_DVI +V3.3_DVI
R499 NL/2.2K 5% 0402 CG_0
R500 NL/2.2K 5% 0402 CG_1
R501 NL/2.2K 5% 0402 CG_2
R505 NL/2.2K 5% 0402
R506 NL/2.2K 5% 0402
R507 NL/2.2K 5% 0402
Co-Lay 3 Pad

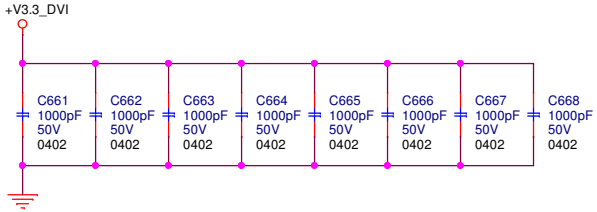
Output Integrity

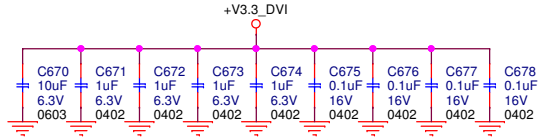
CG_2	CG_1	CG_0	Swing	Preamp	Slew-rate	Note
0	0	0	450	0	0	
0	0	1	420	0	-3dB	Shortest trace
0	1	0	450	0	-3dB	Shortest trace (default)
0	1	1	460	0	-4dB	
1	0	0	340	0	0	
1	0	1	400	2dB	0	Longtest trace
1	1	0	400	2dB	0	Longtest trace
1	1	1	420	0	0	

alawn0616(OK): change to 百徽



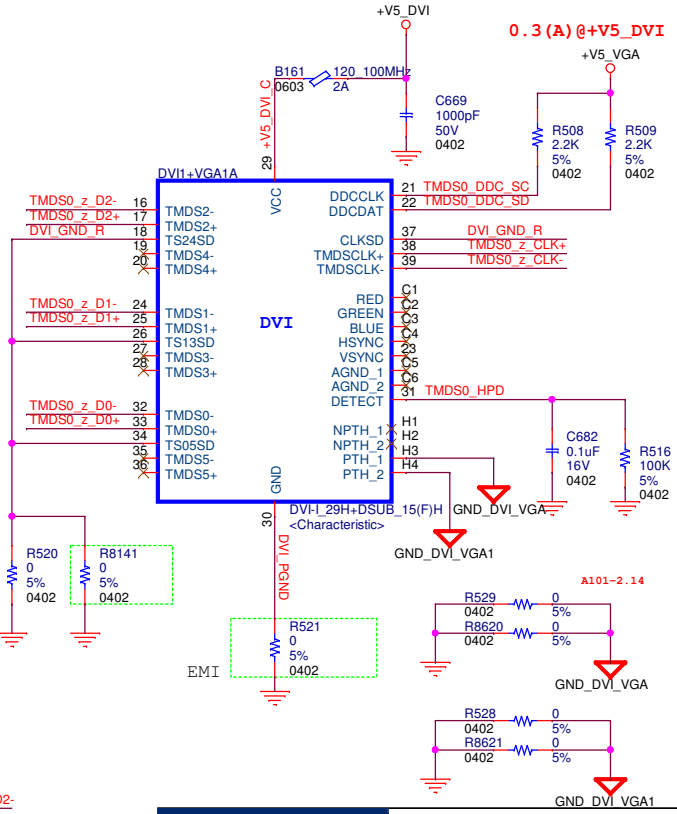






0.055(A)@+V5_DVI

0.3(A)@+V5_DVI



ADVANTECH

Title	37_Display DVI1/Level Shifter	
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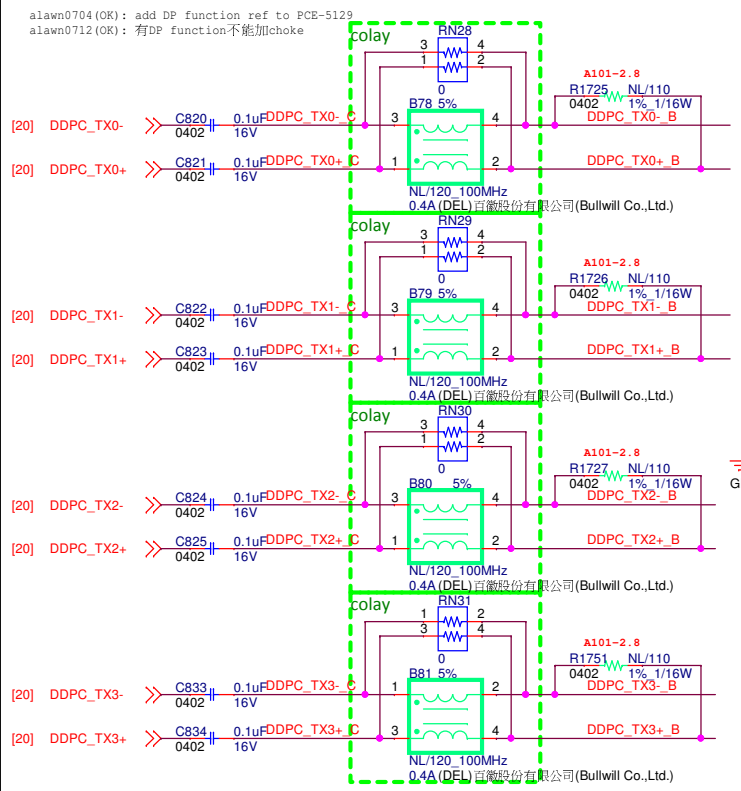
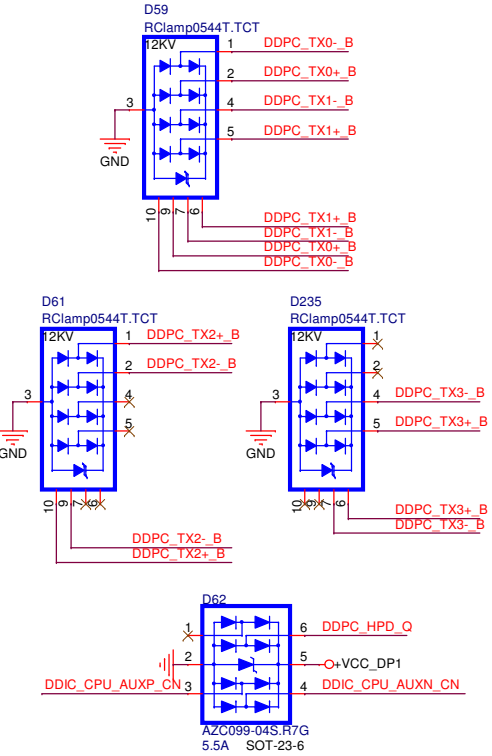
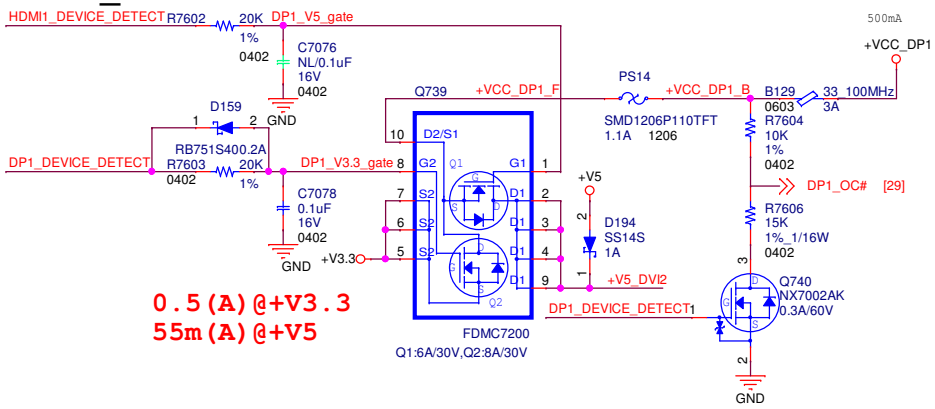
Display DVI2/HDMI1/DP1 PH

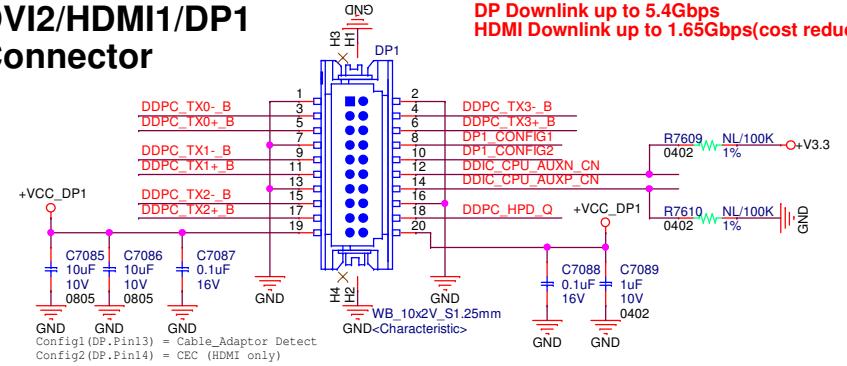


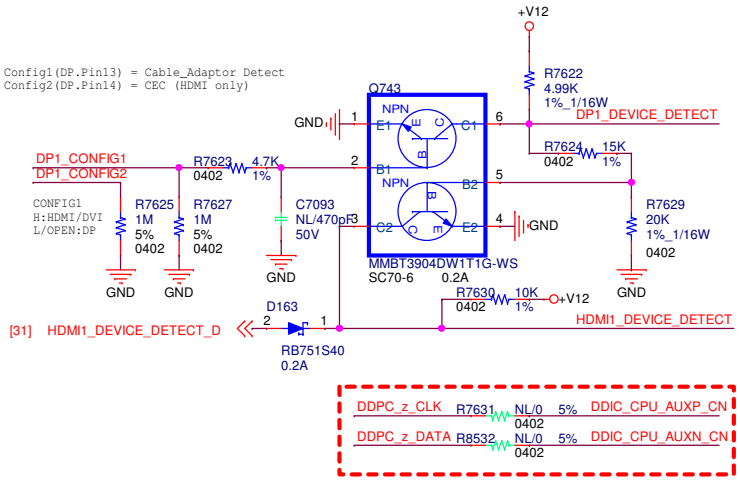


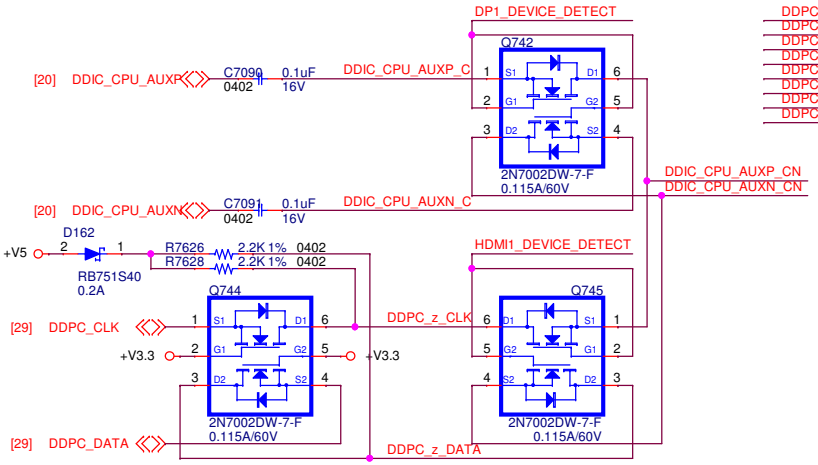


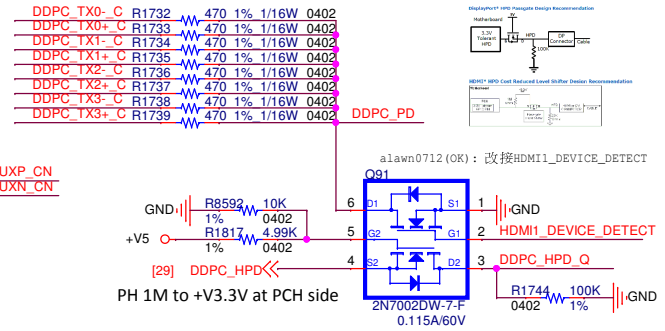
DVI2/HDMI1/DP1 Connector

DP Downlink up to 5.4Gbps
HDMI Downlink up to 1.65Gbps(cost reduce)









ADVANTECH

Title	38_Display DP1/DVI2 PIN HEADER	
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38_Display DVI3/HDMI2/DP2 PH

alawn0704(OK): add DP function ref to PCE-5129
alawn0712(OK): 有DP function不能加choke

H110 NL/

A101-2.15

[20] DDPD_TX0- — C7824 0.1uF 0402 16V — DDPD_TX0-_C — B172 5% — DDPD_TX0-_B — R8571 NL/110 0402 1%_1/16W — A101-2.8
[20] DDPD_TX0+ — C7825 0.1uF 0402 16V — DDPD_TX0+_C — DDPD_TX0+_B
RN45 colay — NL/120_100MHz 0.4A(DEL)百徽股份有限公司(Bullwill Co.,Ltd.)

[20] DDPD_TX1- — C7826 0.1uF 0402 16V — DDPD_TX1-_C — B173 5% — DDPD_TX1-_B — R8570 NL/110 0402 1%_1/16W — A101-2.8
[20] DDPD_TX1+ — C7827 0.1uF 0402 16V — DDPD_TX1+_C — DDPD_TX1+_B
RN47 colay — NL/120_100MHz 0.4A(DEL)百徽股份有限公司(Bullwill Co.,Ltd.)

[20] DDPD_TX2- — C7828 0.1uF 0402 16V — DDPD_TX2-_C — B174 5% — DDPD_TX2-_B — R8569 NL/110 0402 1%_1/16W — A101-2.8
[20] DDPD_TX2+ — C7829 0.1uF 0402 16V — DDPD_TX2+_C — DDPD_TX2+_B
RN44 colay — NL/120_100MHz 0.4A(DEL)百徽股份有限公司(Bullwill Co.,Ltd.)

[20] DDPD_TX3- — C7830 0.1uF 0402 16V — DDPD_TX3-_C — B175 5% — DDPD_TX3-_B — R8568 NL/110 0402 1%_1/16W — A101-2.8
[20] DDPD_TX3+ — C7831 0.1uF 0402 16V — DDPD_TX3+_C — DDPD_TX3+_B
RN46 colay — NL/120_100MHz 0.4A(DEL)百徽股份有限公司(Bullwill Co.,Ltd.)

D242 RClamp0544T.TCT 12KV
DDPD_TX2+_B — DDPD_TX2-_B — DDPD_TX1+_B — DDPD_TX1-_B — DDPD_TX1-_B — DDPD_TX1+_B — DDPD_TX2-_B — DDPD_TX2+_B

D239 RClamp0544T.TCT 12KV
DDPD_TX0+_B — DDPD_TX0-_B — DDPD_TX3-_B — DDPD_TX3+_B — DDPD_TX3+_B — DDPD_TX3-_B — DDPD_TX0-_B — DDPD_TX0+_B

GND

D243 AZC099-04S.R7G 5.5A SOT-23-6
DDPD_HPD_Q — +VCC_DP2 — DDID_CPU_AUXP_CN — DDID_CPU_AUXN_CN

+VCC_DP2 H110 NL/

A101-2.15

HDMI2_DEVICE_DETECT — R8560 20K 1% — DP2_V5_gate — C7816 NL/0.1uF 16V 0402 — GND
DP2_DEVICE_DETECT — D238 RB751S400.2A — R8559 20K 1% 0402 — DP2_V3.3_gate — C7815 0.1uF 16V 0402 — GND

Q870 FDMC7200 Q1:6A/30V,Q2:8A/30V
+VCC_DP2_F — +V3.3 — +V5 — +V5_DVI

PS15 SMD1206P110TFT 1.1A 1206 — 500mA
+VCC_DP2_B — B171 33_100MHz 0603 3A — +VCC_DP2

D237 SS14S 1A

R8561 10K 1% 0402 — DP2_OC# [29]
R8558 15K 1%_1/16W 0402

Q869 NX7002AK 0.3A/60V
DP2_DEVICE_DETECT1 — GND

0.5(A)@+V3.3
55m(A)@+V5

DVI3/HDMI2/DP2 Connector H110 NL/

A101-2.15

DP Downlink up to 5.4Gbps
HDMI Downlink up to 1.65Gbps(cost reduce)

DP2
DDPD_TX0-_B — DDPD_TX0+_B — DDPD_TX1-_B — DDPD_TX1+_B — DDPD_TX2-_B — DDPD_TX2+_B
DDPD_TX3-_B — DDPD_TX3+_B — DP2_CONFIG1 — DP2_CONFIG2 — DDID_CPU_AUXN_CN — DDID_CPU_AUXP_CN — DDPD_HPD_Q

R8566 NL/100K 0402 1% — +V3.3
R8567 NL/100K 0402 1% — GND

+VCC_DP2 — C7817 10uF 10V 0805 — C7818 10uF 10V 0805 — C7821 0.1uF 16V — GND
C7823 0.1uF 16V — C7822 1uF 10V 0402 — GND

WB_10x2V_S1.25mm
GND<Characteristic>

Config1(DP.Pin13) = Cable_Adaptor Detect
Config2(DP.Pin14) = CEC (HDMI only)

H110 NL/

A101-2.15

Config1(DP.Pin13) = Cable_Adaptor Detect
Config2(DP.Pin14) = CEC (HDMI only)

+V12 — R8551 4.99K 1%_1/16W — DP2_DEVICE_DETECT
Q868 MMBT3904DW1T1G-WS SC70-6 0.2A
GND — R8553 15K 0402 1%
DP2_CONFIG1 — R8555 4.7K 0402 1%
DP2_CONFIG2 — R8552 1M 5% 0402 — R8554 1M 5% 0402 — C7814 NL/470pF 50V — GND
CONFIG1 H:HDMI/DVI L/OPEN:DP
R8557 20K 1%_1/16W 0402 — GND
R8556 10K 0402 1% — +V12
[31] HDMI2_DEVICE_DETECT_D — D236 RB751S40 0.2A — HDMI2_DEVICE_DETECT

DDPD_z_CLK — R8563 NL/0 5% 0402 — DDID_CPU_AUXP_CN
DDPD_z_DATA — R8562 NL/0 5% 0402 — DDID_CPU_AUXN_CN

[20] DDID_CPU_AUXP — C7820 0.1uF 0402 16V — DDID_CPU_AUXP_C — Q871 2N7002DW-7-F 0.115A/60V — DDID_CPU_AUXP_CN
[20] DDID_CPU_AUXN — C7819 0.1uF 0402 16V — DDID_CPU_AUXN_C — DDID_CPU_AUXN_CN

D240 RB751S40 0.2A
+V5 — R8564 2.2K 1% 0402 — R8565 2.2K 1% 0402
Q872 2N7002DW-7-F 0.115A/60V
[29] DDPD_CLK — DDPD_z_CLK — +V3.3
[29] DDPD_DATA — DDPD_z_DATA

HDMI2_DEVICE_DETECT — Q873 2N7002DW-7-F 0.115A/60V

DDPD_TX0-_C — R8575 470 1% 1/16W 0402
DDPD_TX0+_C — R8581 470 1% 1/16W 0402
DDPD_TX1-_C — R8574 470 1% 1/16W 0402
DDPD_TX1+_C — R8576 470 1% 1/16W 0402
DDPD_TX2-_C — R8577 470 1% 1/16W 0402
DDPD_TX2+_C — R8578 470 1% 1/16W 0402
DDPD_TX3-_C — R8579 470 1% 1/16W 0402
DDPD_TX3+_C — R8580 470 1% 1/16W 0402
DDPD_PD

alawn0712(OK): 改接HDMI2_DEVICE_DETECT

Q874 2N7002DW-7-F 0.115A/60V
GND — R8594 10K 1% 0402 — R8573 4.99K 1% 0402 — +V5
[29] DDPD_HPD — DDPD_HPD_Q — R8573 100K 1% 0402 — GND
HDMI2_DEVICE_DETECT

PH 1M to +V3.3V at PCH side

ADVANTECH

Title	39_Display DP2/DVI3 PIN HEADER	
Size	Document Number MIC-7700	Rev A101-2
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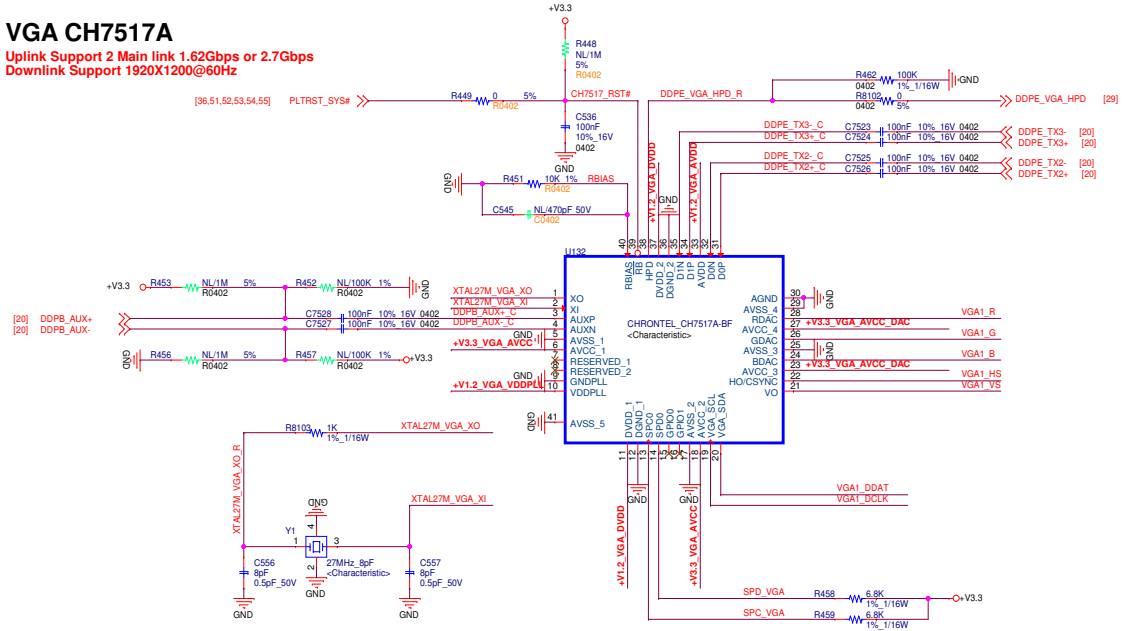
Display VGA1/CH7517

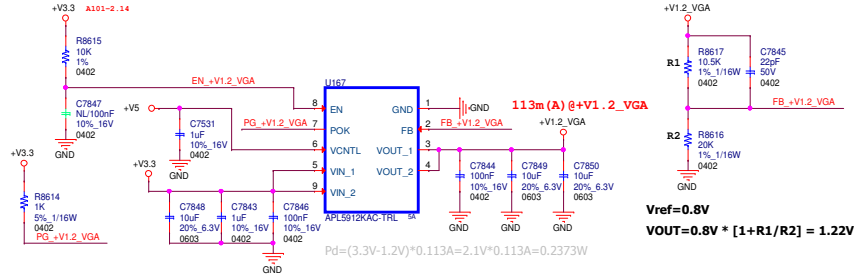
VGA CH7517A

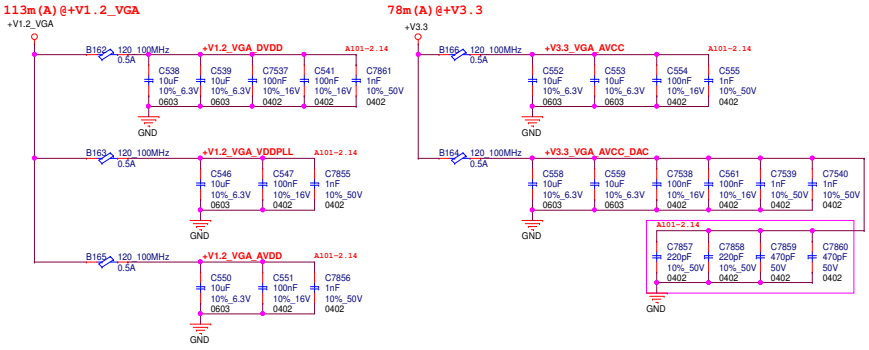
Uplink Support 2 Main link 1.62Gbps or 2.7Gbps
Downlink Support 1920X1200@60Hz



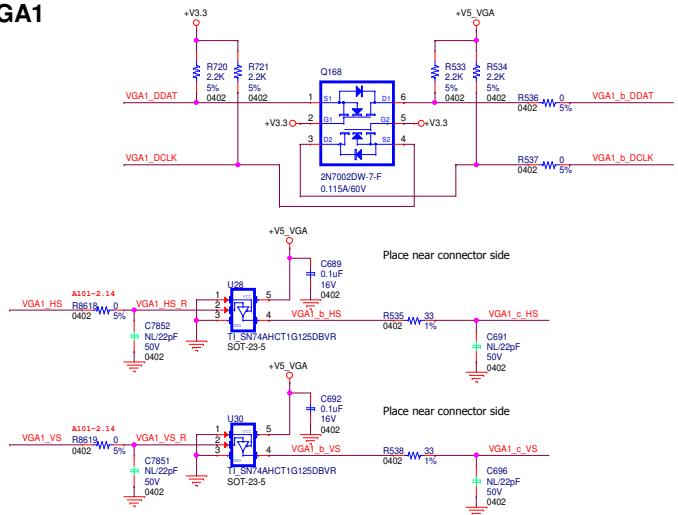
+V1.2_VGA

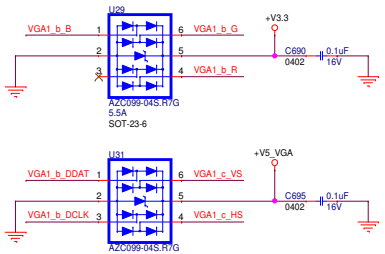
alawn0704(OK): change to NCT3730S copy from +V1.5_MINIPCIE
alawn1201(OK): 換回APL5912KAC-TRL

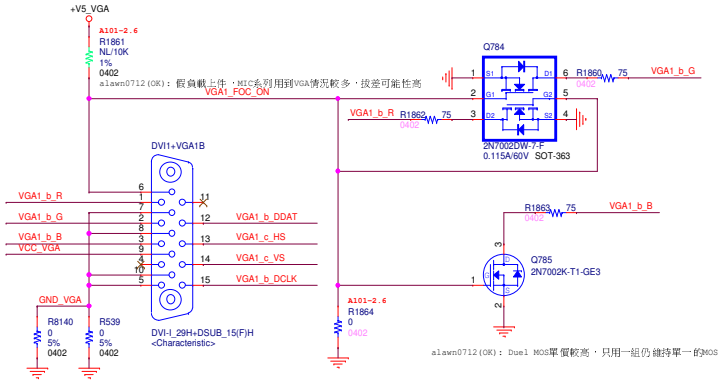


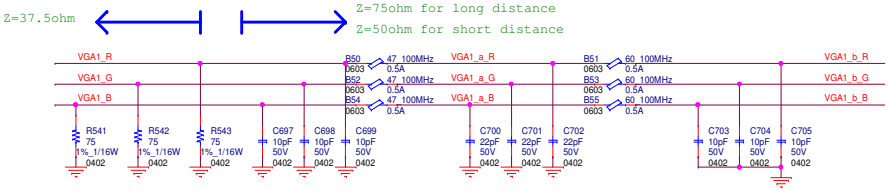


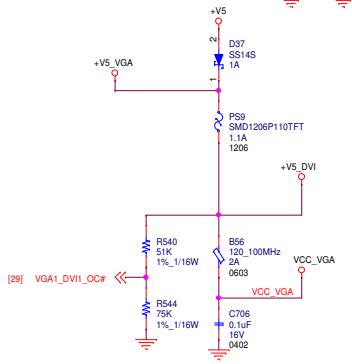
VGA1





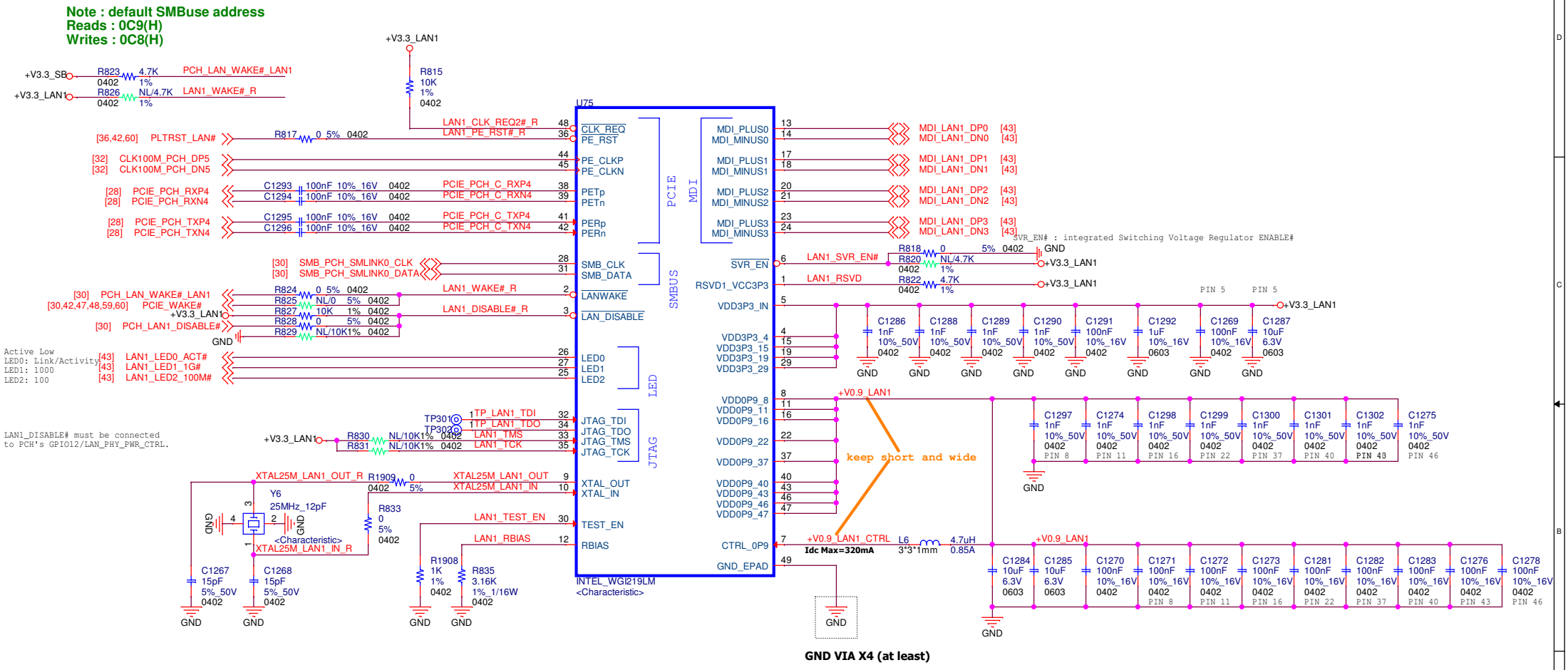






ADVANTECH			
Title	40_Display VGA1/CH7517		
Size	Document Number	MIC-7700	Rev A101-2
Date:	Friday, February 10, 2017	Sheet 40 of 62	

LAN1 INTEL I219LM/I219V



Title	41_LAN1 INTEL I219LM/I219V	
Size	Document Number MIC-7700	Rev A101-2
Date: Friday, February 10, 2017	Sheet 41 of 62	

LAN2 INTEL I210IT

A101-2.20

DECOUPLING

0.5A

LAN LED Disable

A101-2.11

Q875

2N7002DW-7-F
0.115A/60V

0.025mA

Non_NCSI A101-2.12

IMG-115

Image Intel I210IT
2080006756
A101-2.22

Security Mode

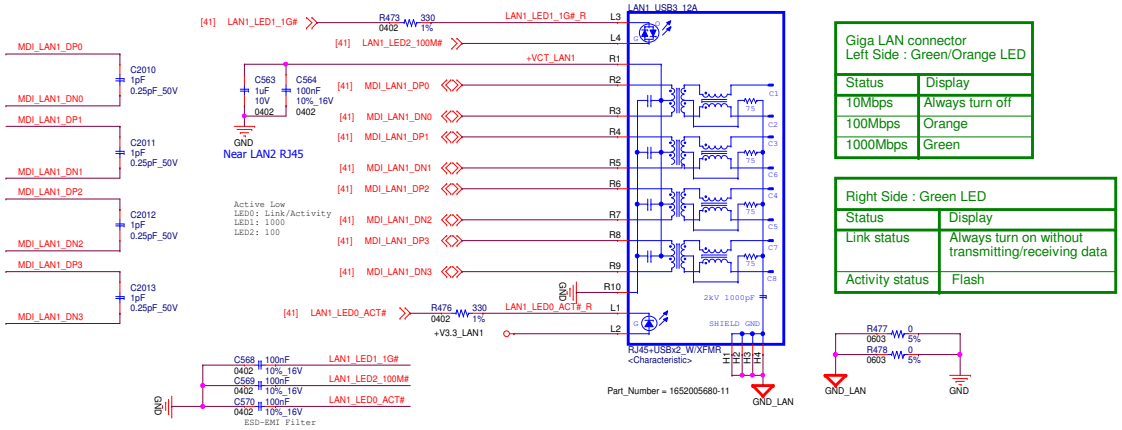
Enable : NO STUFF R450 *
Disable : STUFF R450
1. FLASH-LESS MODE, support WOL from S5
2. MAYBE SPI ROM CAN NL FOR COST
3. iNVM ONLY HAS DEFAULT SETTING CODE, IF WE PURSURING BETTER PERFORMANCE, WE WILL NEED EXTERNAL SPI ROM

KEEP SPI TRACES SHORT FOR 70MHZ SIGNALING

Title	42_LAN2 INTEL I210IT	
Size	Document Number MIC-7700	Rev A101-2
Date: Friday, February 10, 2017	Sheet 42 of 62	

CONN LAN1/USB3_12

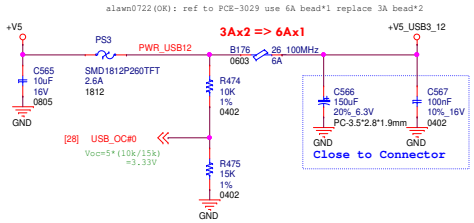
LAN1



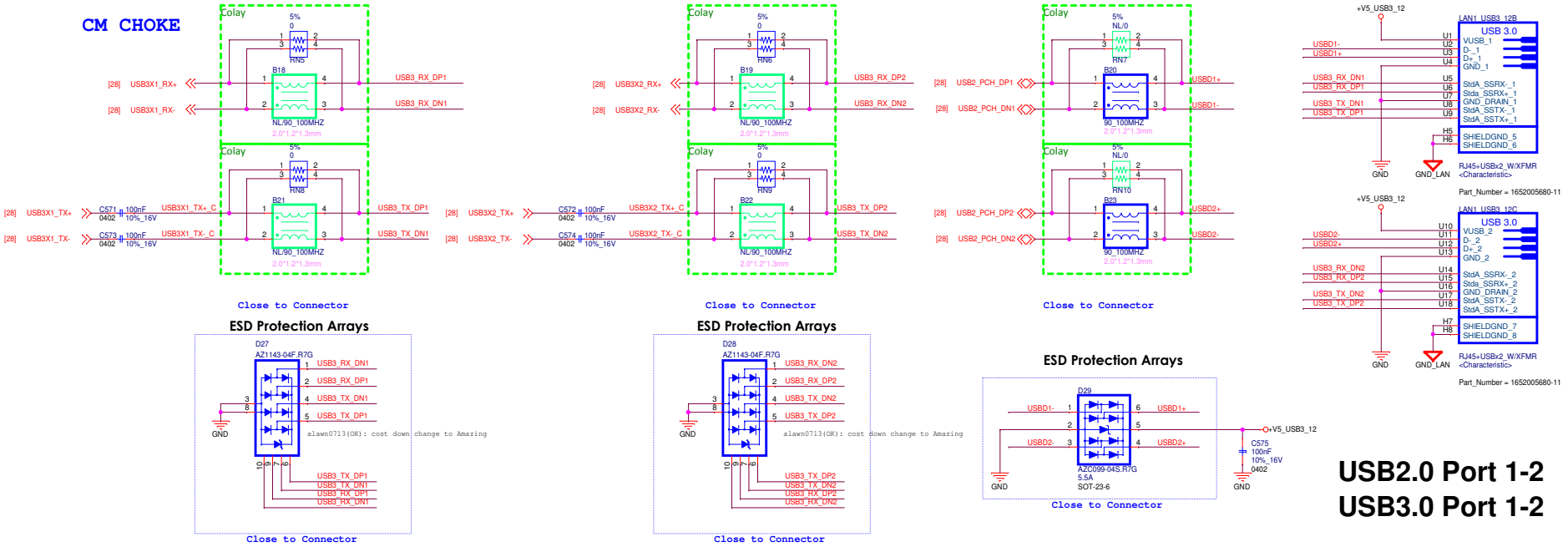
Giga LAN connector Left Side : Green/Orange LED	
Status	Display
10Mbps	Always turn off
100Mbps	Orange
1000Mbps	Green

Right Side : Green LED	
Status	Display
Link status	Always turn on without transmitting/receiving data
Activity status	Flash

Power for USB3_12



USB3_12



USB PORT 1/2

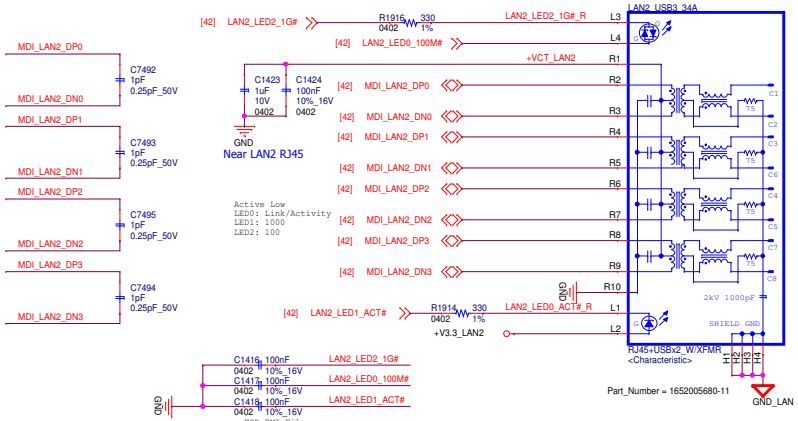
USB2.0 Port 1-2

USB3.0 Port 1-2

ADVANTECH			
Title	43_CONN LAN1/USB3_12		
Size	Document Number	MIC-7700	Rev A101-2
Date:	Friday, February 10, 2017	Sheet 43 of 62	

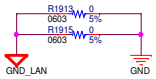
CONN LAN2/USB3_34

LAN2

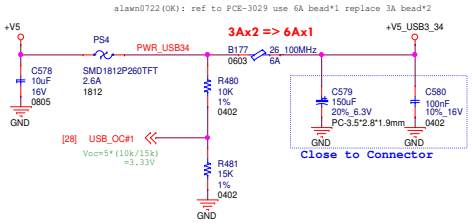


Giga LAN connector Left Side : Green/Orange LED	
Status	Display
10Mbps	Always turn off
100Mbps	Orange
1000Mbps	Green

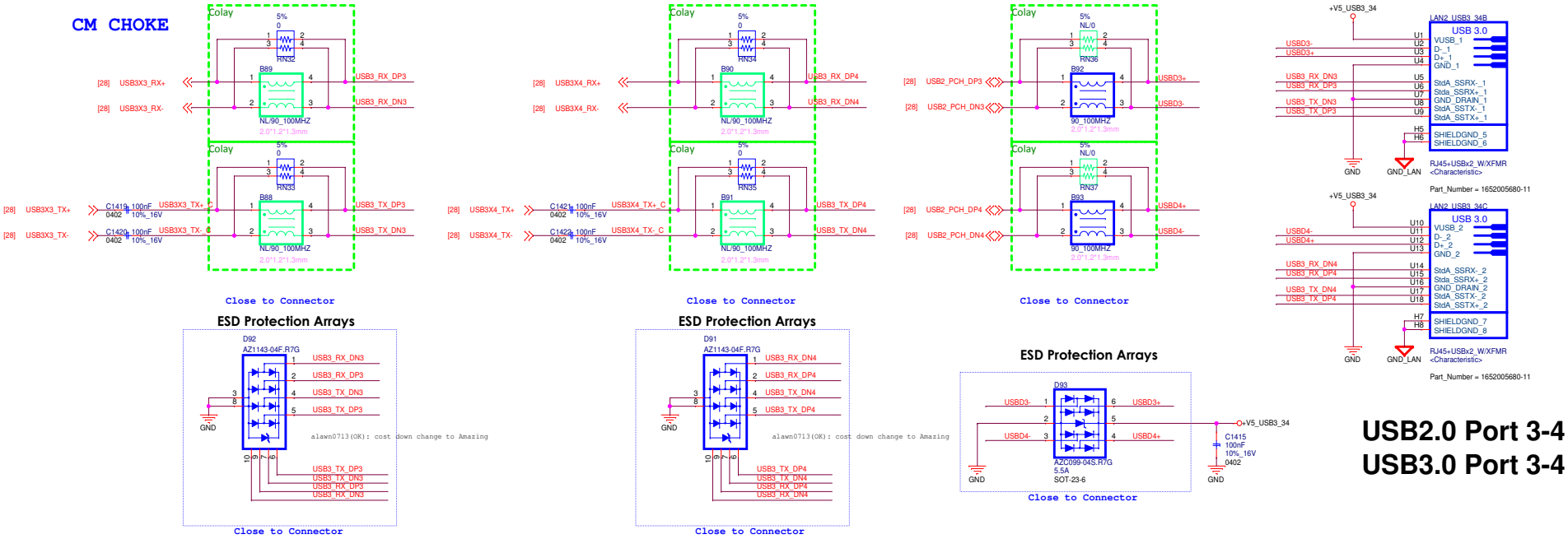
Right Side : Green LED	
Status	Display
Link status	Always turn on without transmitting/receiving data
Activity status	Flash



Power for USB3_34



USB3_34



USB2.0 Port 3-4
USB3.0 Port 3-4

ADVANTECH			
Title	44_CONN LAN2/USB3_34		
Size	Document Number	MIC-7700	Rev A101-2
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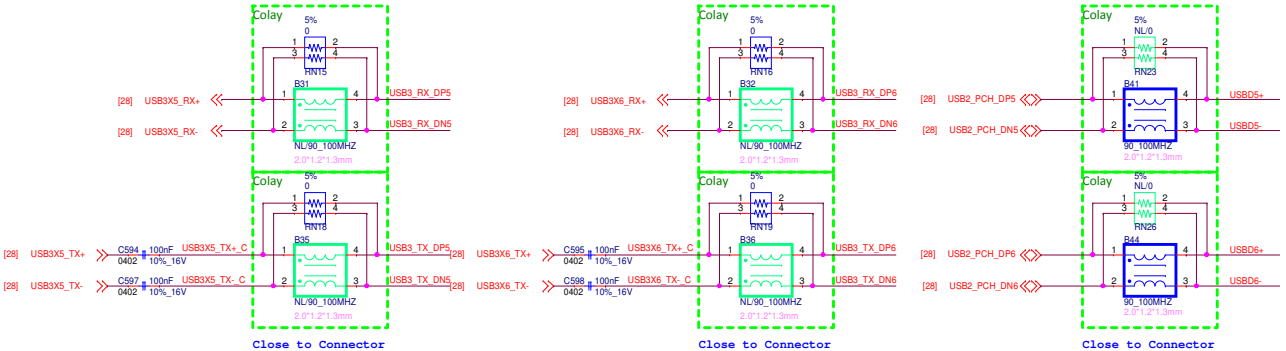
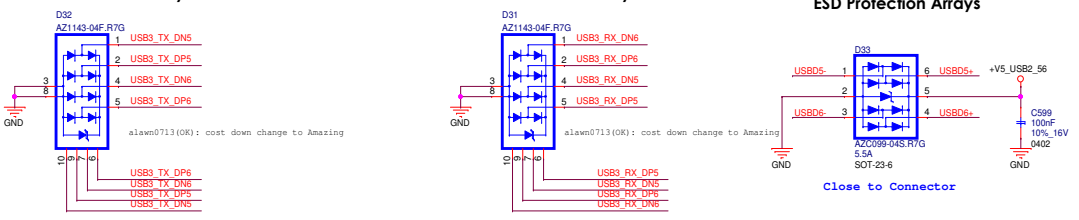
CONN USB2_5678/USB3_5678

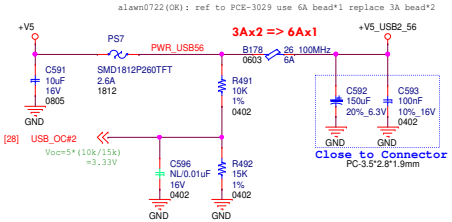
USB3_56



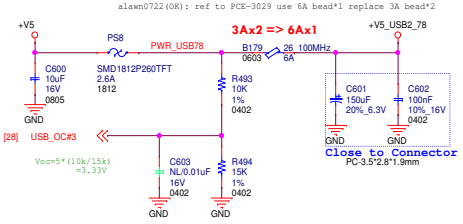
ESD Protection Arrays



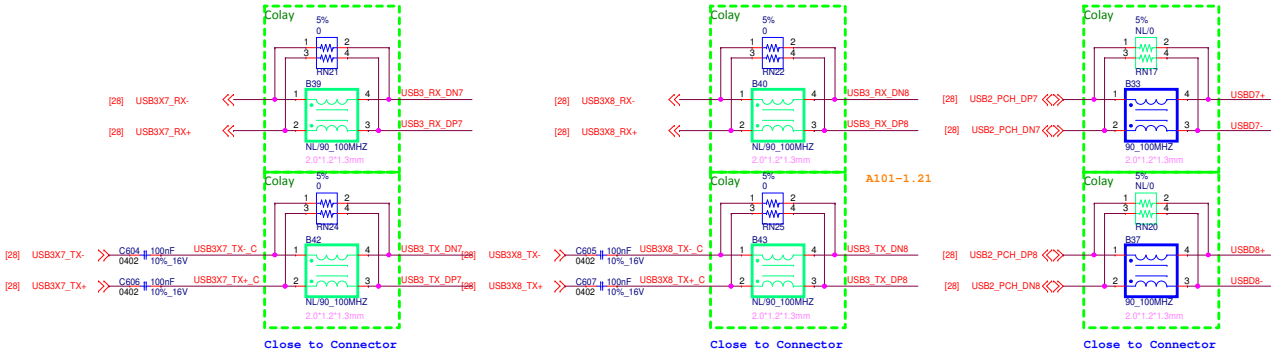
Power for USB2_56



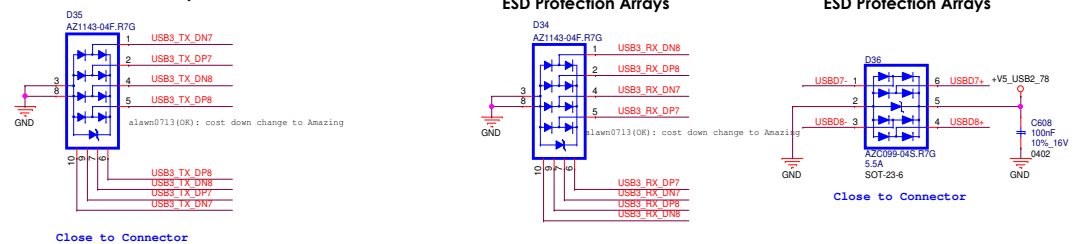
Power for USB2_78



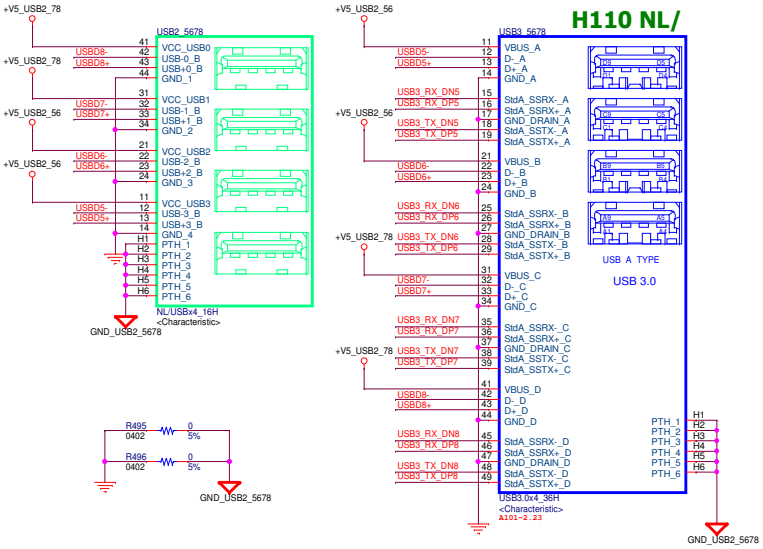
USB3_78



ESD Protection Arrays



USB2.0 Port 5,6,7,8
USB3.0 Port 5,6,7,8 Co-Lay



ADVANTECH
Title
45_CONN USB2_5678/USB3_5678
Size
Document Number
MIC-7700
Rev
A101-2
Date: Friday, February 10, 2017
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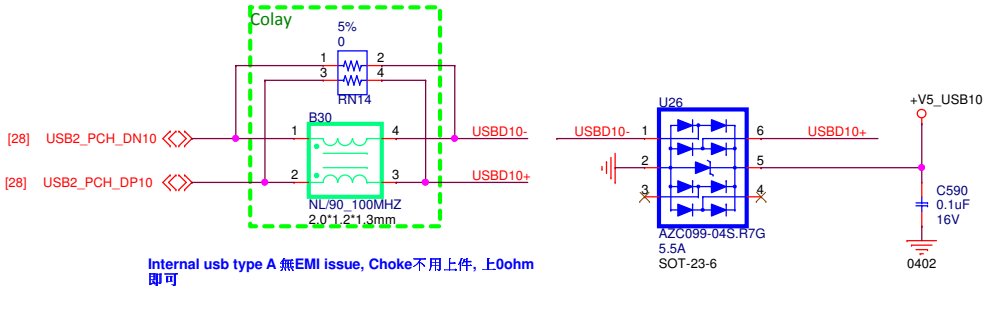
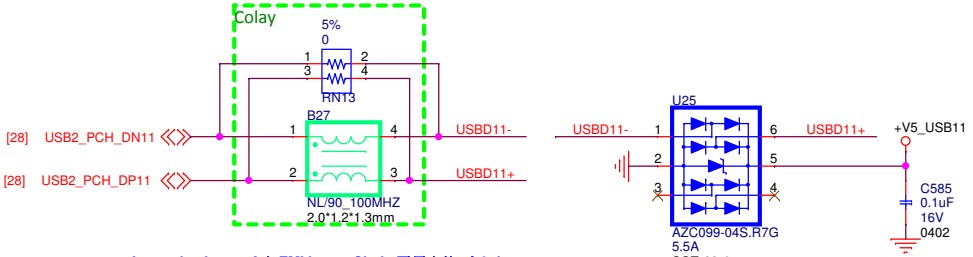
CONN USB2_10/USB2_11

USB2_10 Isolation GPIO module

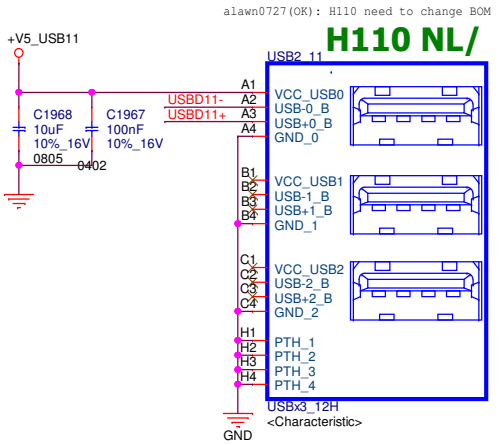


Internal usb type A 無EMI issue, Choke不用上件, 上0ohm 即可

USB2_11 Internal Dongle



Internal usb type A 無EMI issue, Choke不用上件, 上0ohm 即可



ADVANTECH		
Title	46_CONN USB2_10/USB2_11	
Size	Document Number: MIC-7700	Rev: A101-2
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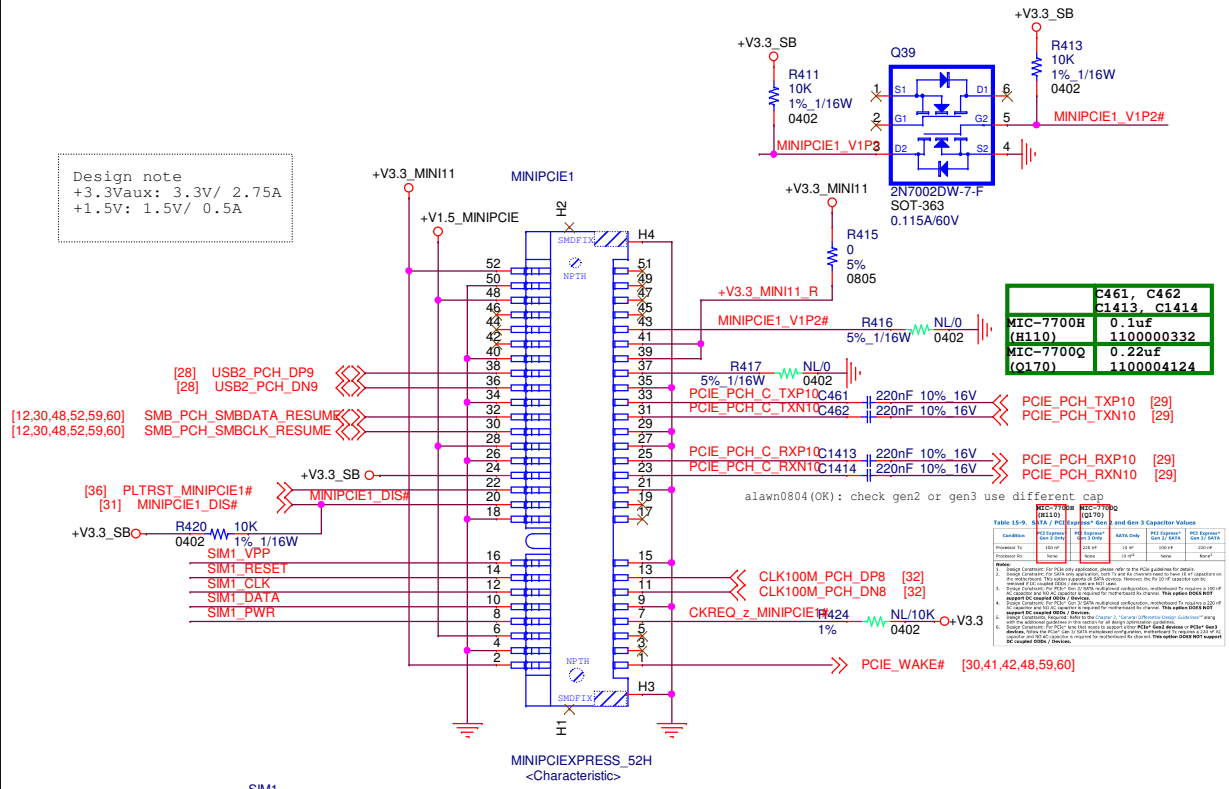
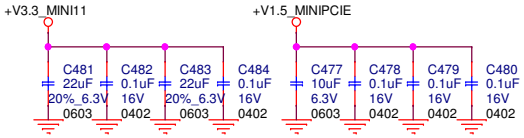
CONN MINIPCIE1(USIM)

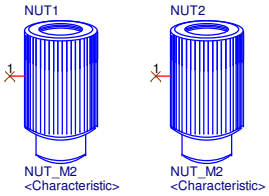
MINIPCIE1



Pin	mini-pcie 1.1	mini-pcie 1.2	mSATA	
2	3.3V	3.3Vaux	3.3V	+V3.3_MINI11
24	3.3Vaux	3.3Vaux	3.3V	+V3.3_SB
39	Reserved*	3.3Vaux	3.3V	+V3.3_MINI11
41	Reserved*	3.3Vaux	3.3V	+V3.3_MINI11
52	3.3V	3.3Vaux	3.3V	+V3.3_MINI11

Spec.	Mini PCIe 1.1	Mini PCIe 1.2	mSATA
Pin43	Reserved (H)	GND (L)	NC (H)
Pin51	Reserved (H)	Reserved (H)	Presences Detection (GND-2b)



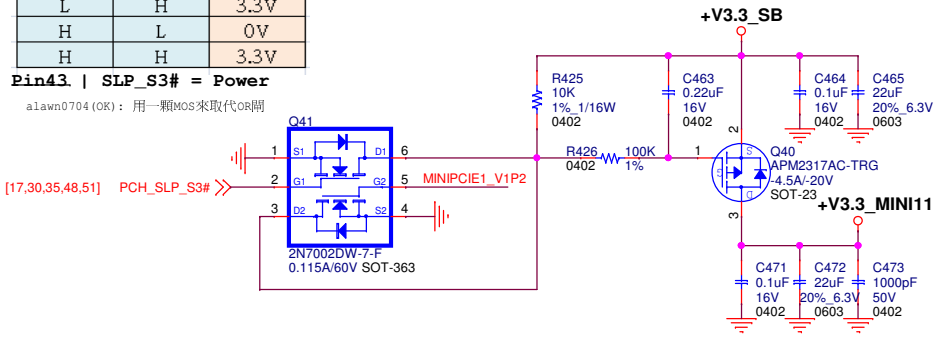


+V3.3_MINI11

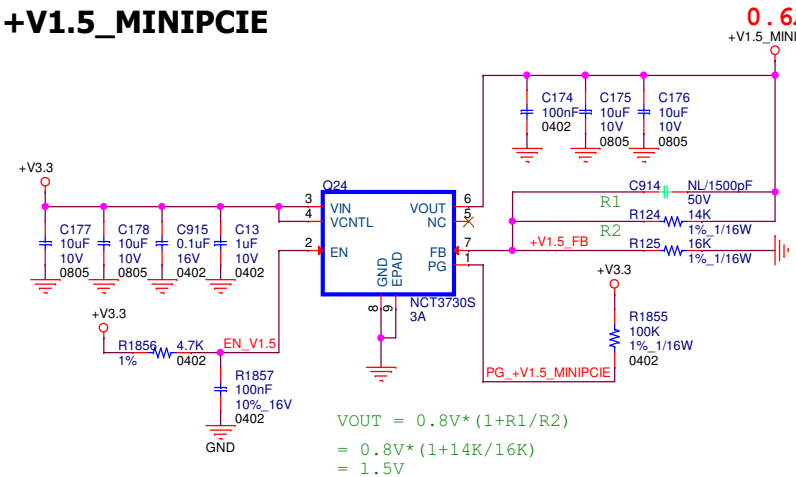
Power of Pin2, 39, 41, 52		
Pin43	SLP_S3#	Power
L	L	3.3V
L	H	3.3V
H	L	0V
H	H	3.3V

Pin43 | SLP_S3# = Power

alawn0704(OK): 用一顆MOS來取代OR閘



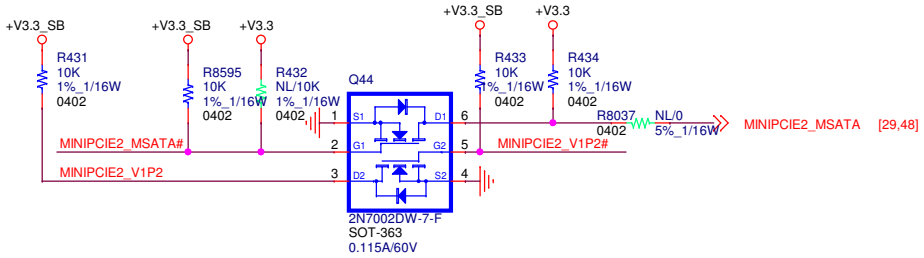
+V1.5_MINIPCIE



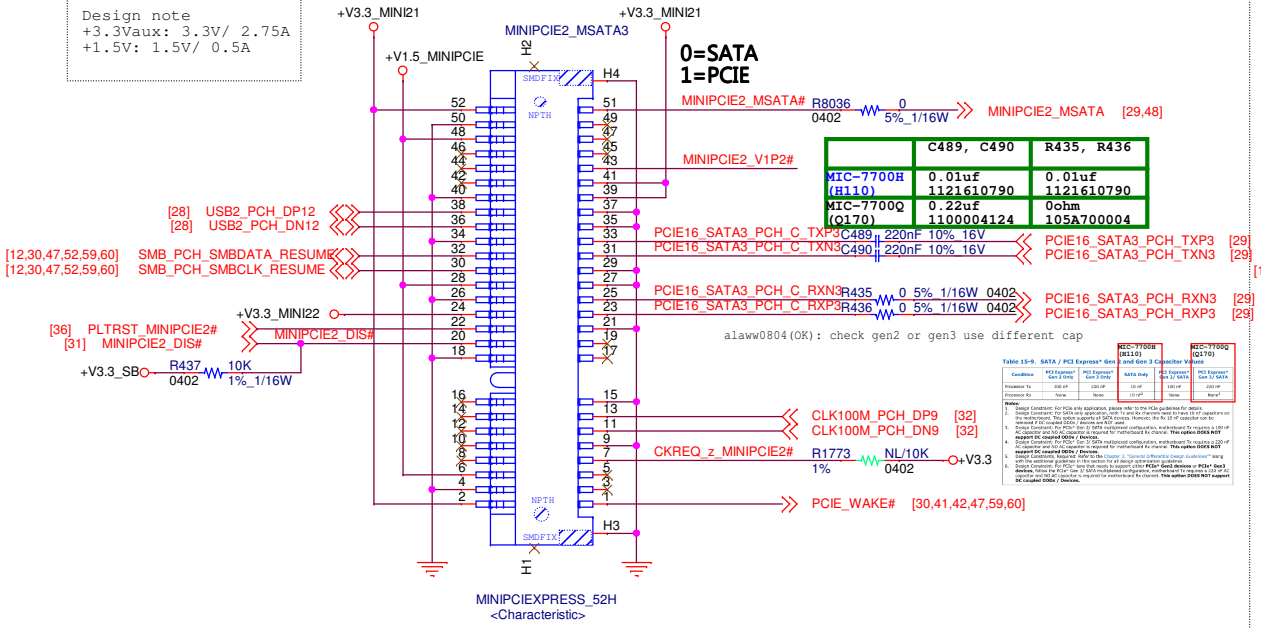
ADVANTECH			
Title	47_CONN MINIPCIE1(USIM)		
Size	Document Number MIC-7700		Rev A101-2
Date: Friday, February 10, 2017		Sheet 47 of 62	

CONN MINIPCIE2_mSATA3(iDoor)

MiniPCIE2_mSATA3

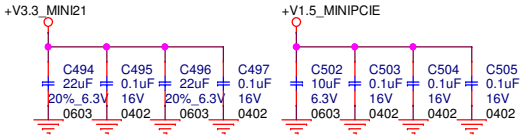


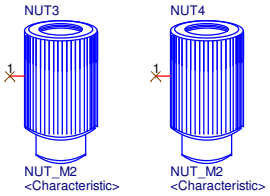
Design note
+3.3Vaux: 3.3V/ 2.75A
+1.5V: 1.5V/ 0.5A



Pin	mini-pcie 1.1	mini-pcie 1.2	mSATA	
2	3.3V	3.3Vaux	3.3V	+V3.3_MINI21
24	3.3Vaux	3.3Vaux	3.3V	+V3.3_MINI22
39	Reserved*	3.3Vaux	3.3V	+V3.3_MINI21
41	Reserved*	3.3Vaux	3.3V	+V3.3_MINI21
52	3.3V	3.3Vaux	3.3V	+V3.3_MINI21

Spec.	Mini PCIe 1.1	Mini PCIe 1.2	mSATA
Pin43	Reserved (H)	GND (L)	NC (H)
Pin51	Reserved (H)	Reserved (H)	Presences Detection (GND->L)



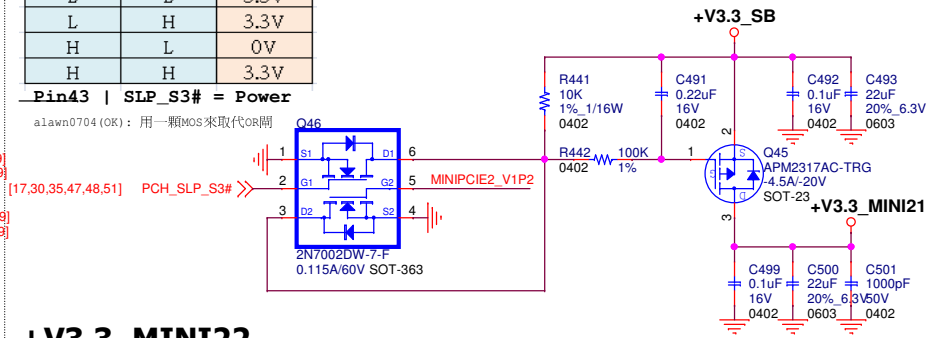


+V3.3_MINI21

Power of Pin2, 39, 41, 52		
Pin43	SLP_S3#	Power
L	L	3.3V
L	H	3.3V
H	L	0V
H	H	3.3V

Pin43 | SLP_S3# = Power

alawn0704(OK): 用一顆MOS來取代OR閘

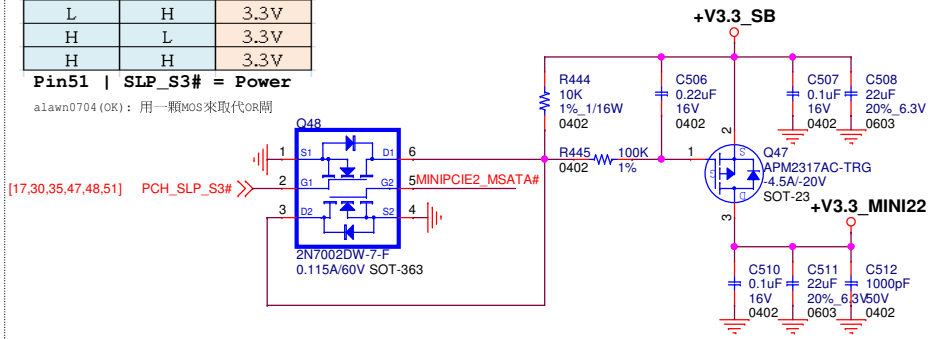


+V3.3_MINI22

Power of Pin24		
Pin51	SLP_S3#	Power
L	L	0V
L	H	3.3V
H	L	3.3V
H	H	3.3V

Pin51 | SLP_S3# = Power

alawn0704(OK): 用一顆MOS來取代OR閘



ADVANTECH

Title	48_CONN MINIPCIE2_mSATA3(iDoor)	
Size	Document Number: MIC-7700	Rev: A101-2
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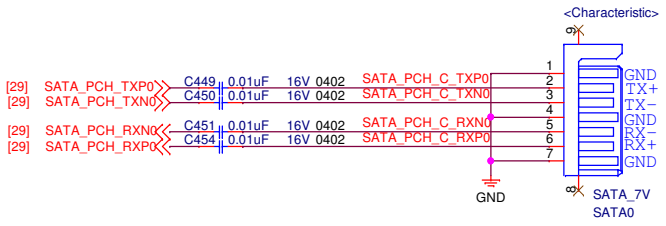
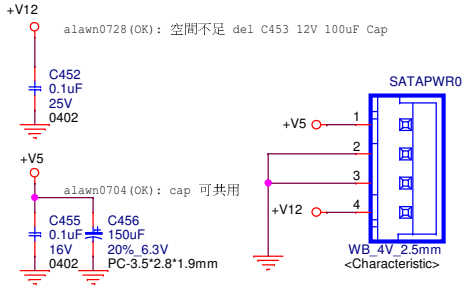
CONN SATA0, 4, 5/CFast1

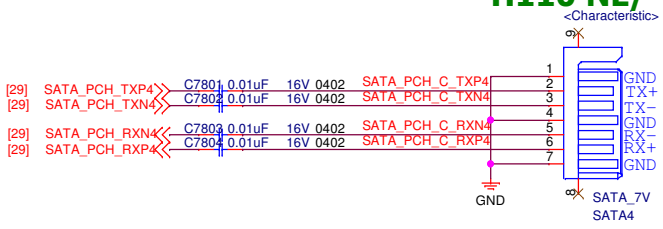
SATA0

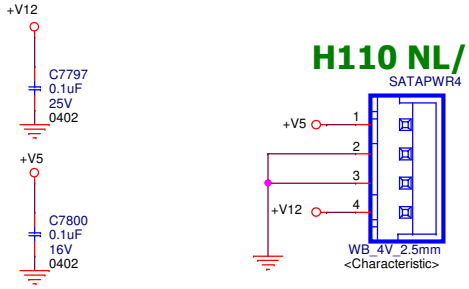




SATA4

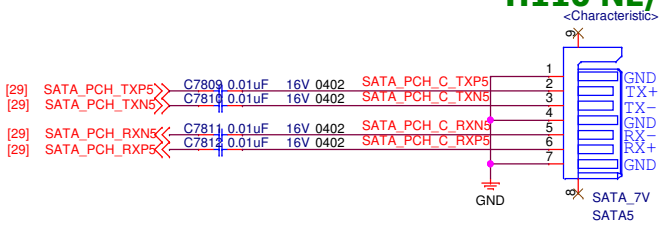
H110 NL/

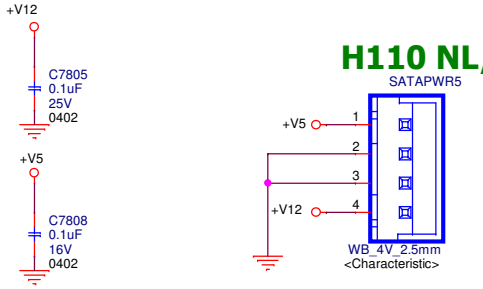




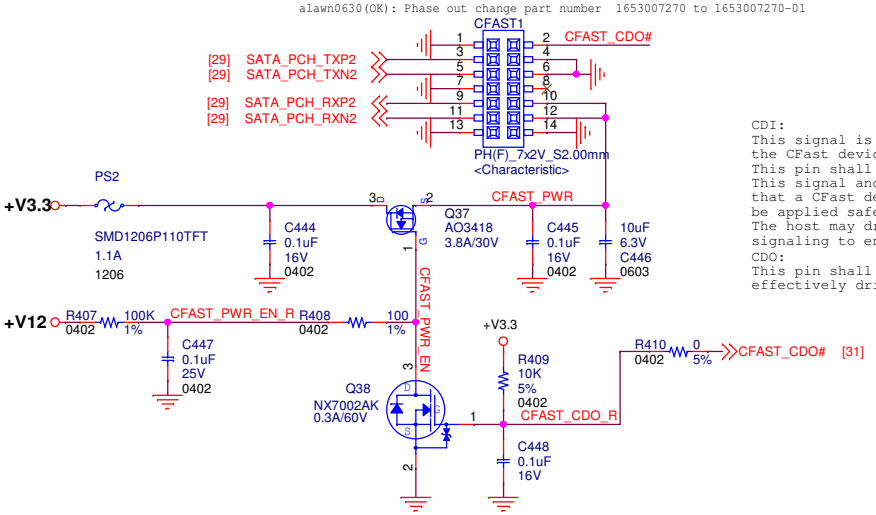
SATA5.

H110 NL/





CFast



CDI:
This signal is driven by the CFast host, and shall be sampled by the CFast device
This pin shall be shorted on a CFast device to CDO.
This signal and CDO provide a mechanism for a CFast host to detect that a CFast device has been fully inserted, and so that power can be applied safely.
The host may drive, and the device may sample, this pin to provide signaling to enable CFast Power Management Sleep state.
CDO:
This pin shall be shorted on the CFast device to CDI. It is effectively driven by CDI.

ADVANTECH

Title	49_CONN SATA0, 4, 5/CFast1	
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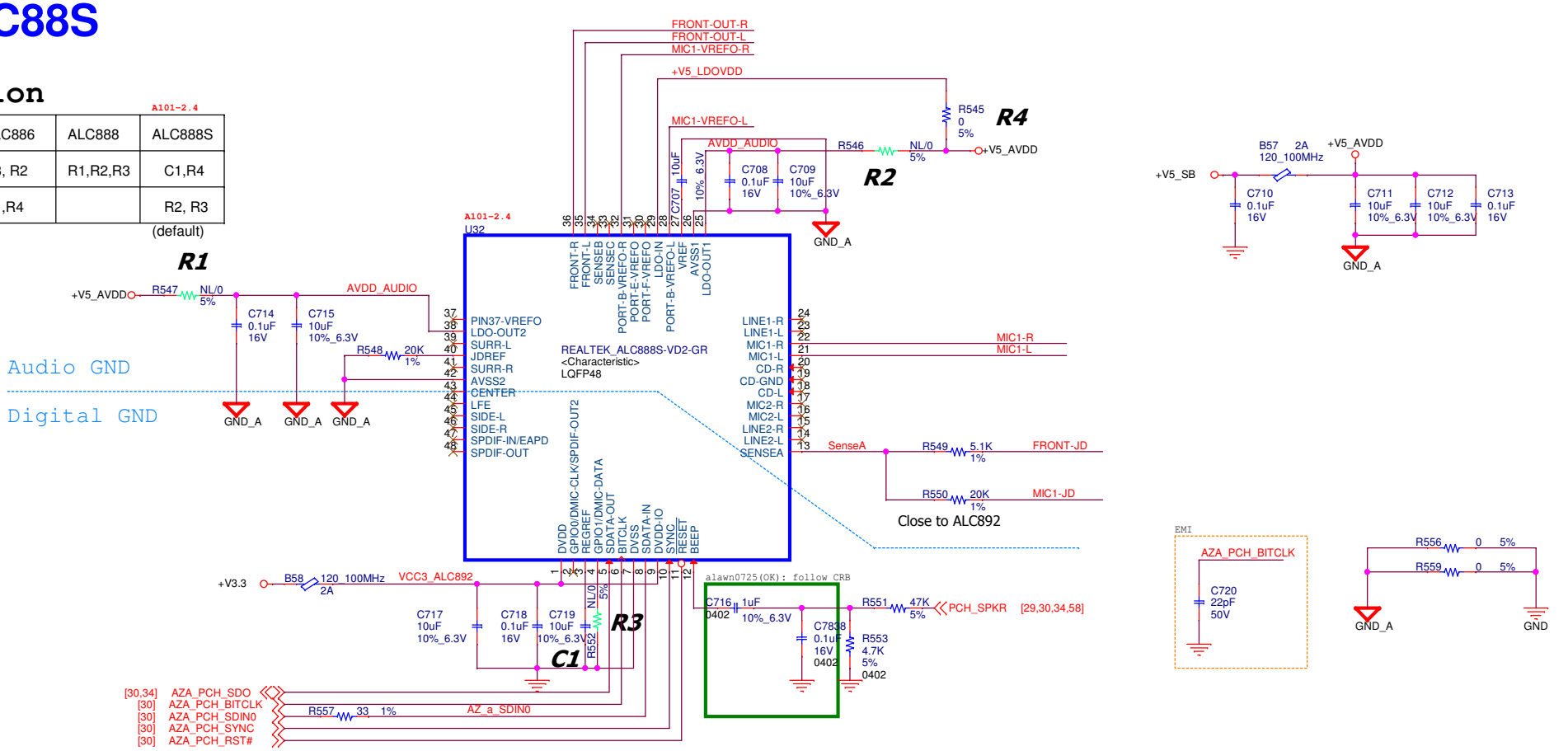
Audio ALC88S

IC BOM Option

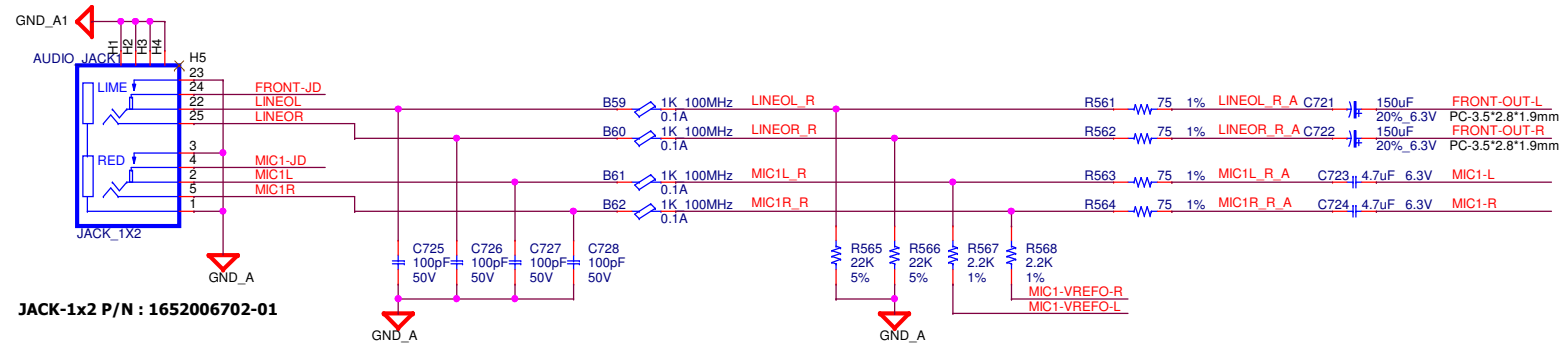
A101-2.4

	ALC892	ALC886	ALC888	ALC888S
Stuff	C1,R4	R3, R2	R1,R2,R3	C1,R4
Empty	R2, R3	C1,R4		R2, R3

(default)



AUDIO_JACK1



Title	50_Audio ALC888S	
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SIO NCT6106D

SIO old version 1410022361

Thermistor

AVREF
R687 10K 1%_1/16W
給Riser用
與SIO_AGND平行走線到EXPA1
SIO_CPUTIN
SIO_CPUTIN [59]

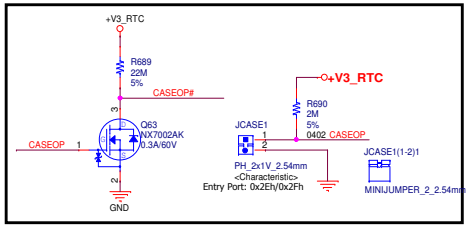
AVREF
(~2.048V)
R688 10K 1%_1/16W
C815 100nF 10%_16V 0402
SIO_SYSTIN
Close to SuperIO
RT5 10K 1%_250mW
SIO_AGND

AVREF
R8163 10K 1%_1/16W
給Power用
與SIO_AGND_PB平行走線到GF1
PB_temp_sense
PB_temp_sense [9]
B167 30_100MHz 1A 0603
SIO_AGND
SIO_AGND_PB

POWER ON SETTING PIN

PIN	Name	0	1	Strapping Power
51	UART1_RTS#	2E	4E	3VCC
52	UART1_DTR#	24M Clock Source	48M Clock Source	3VCC
54	UART1_SOUT	GPIO to PORT80 Disable	GPIO to PORT80 Enable	3VCC
106	SUPLED	UART	DSW	3VSB
111	UART3_RTS#	SOUTC to 80port disable	SOUTC to 80port enable	3VCC
112	UART3_DTR#	SOUTE to 80port disable	SOUTE to 80port enable	3VCC

JCASE1 : case open pin header



Port 80

```
alawn0705(OK): need to check
alawn0704(OK): change small package ref ASMB-975
alawn0726(OK): del Port 80 add GPIO0
```

Title	51_SIO NCT6106D
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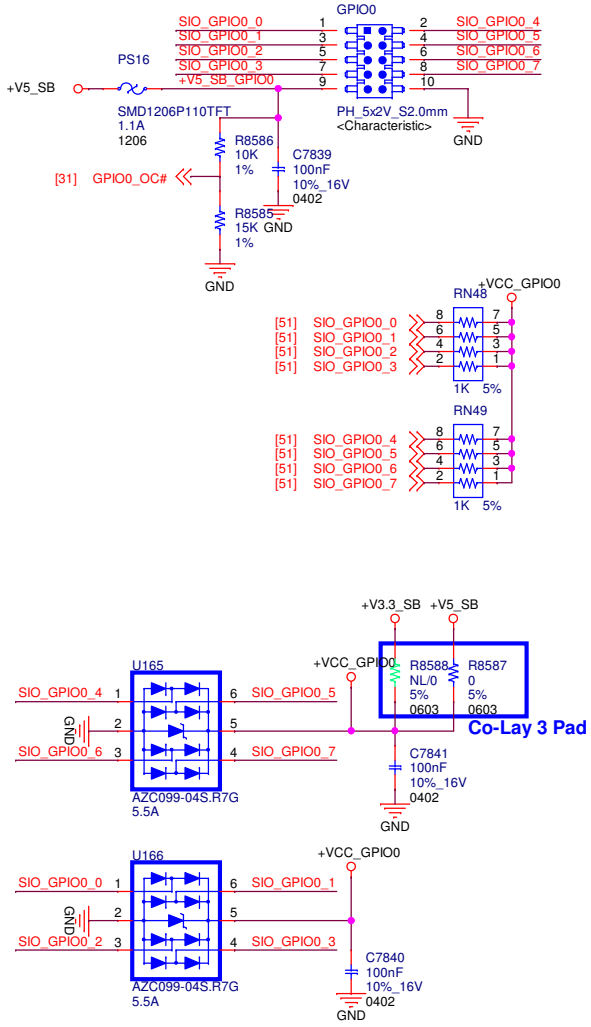
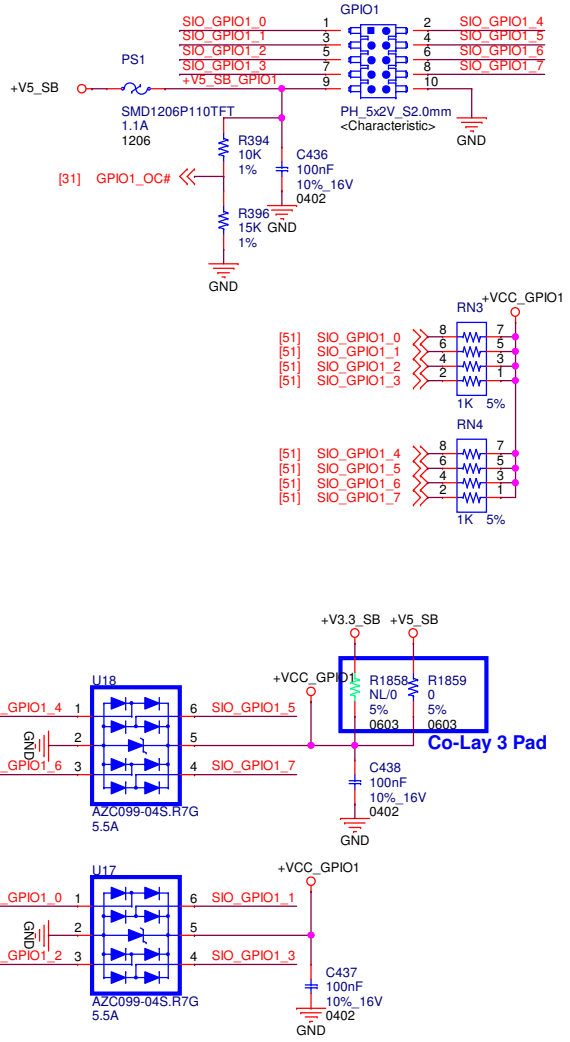
CONN GPIO0, 1/LPC1/KBMS1

8 bit GPIO0

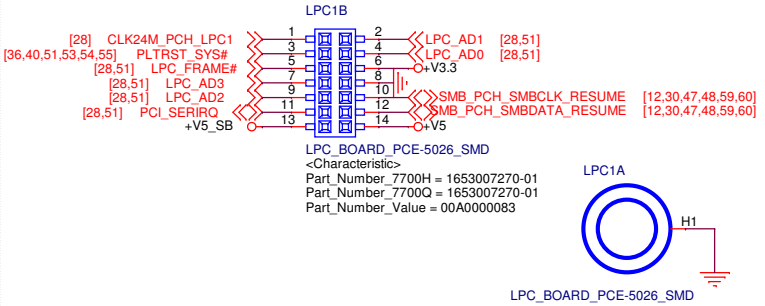


8 bit GPIO1

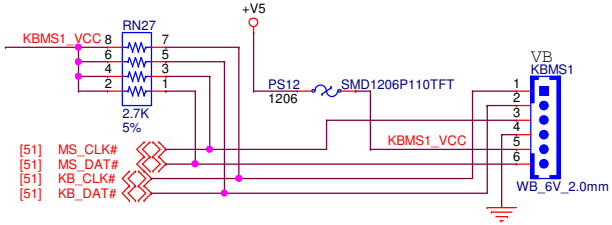


LPC1 for isolation COM module

LPC1B BOM P1653007270-01:
Part_Number 00A0000083
Part_Number_Value 1653007270-01



K.B. & MOUSE



PS2 KBMS_CABLE1 P/N -->1703060191

ADVANTECH

Title	52_CONN GPIO0, 1/LPC1/KBMS1	
Size	Document Number MIC-7700	Rev A101-2
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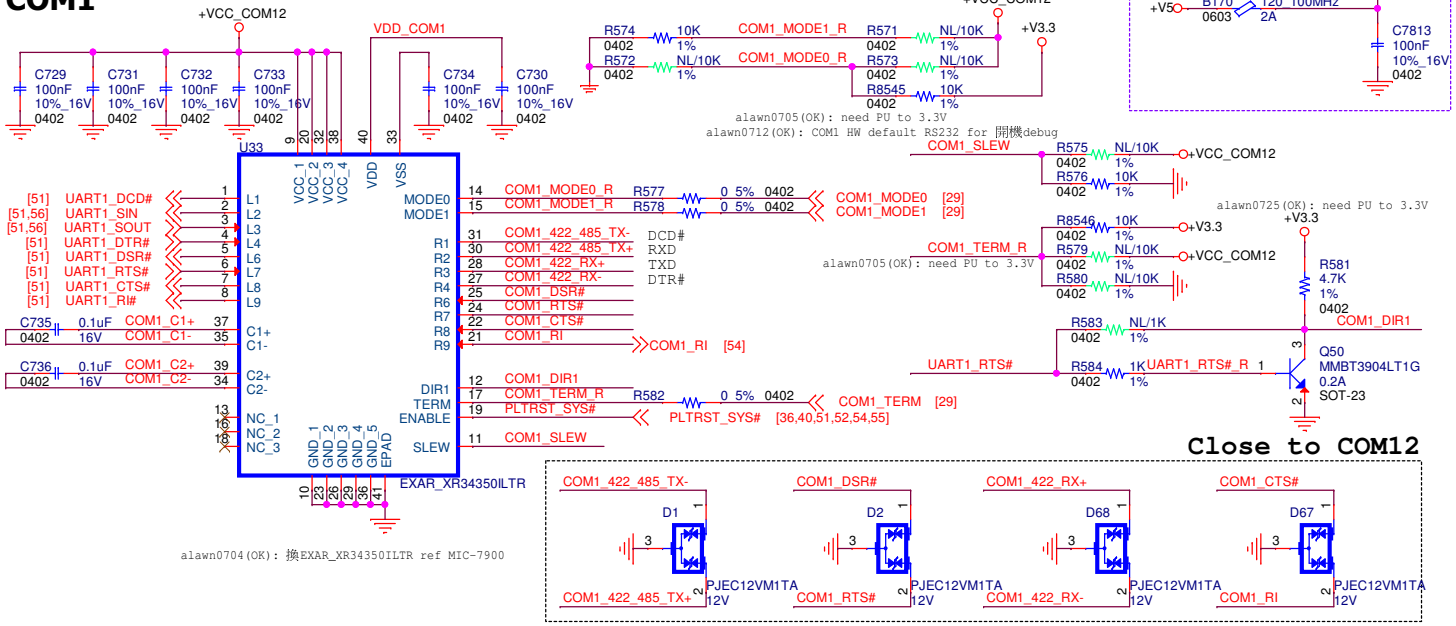
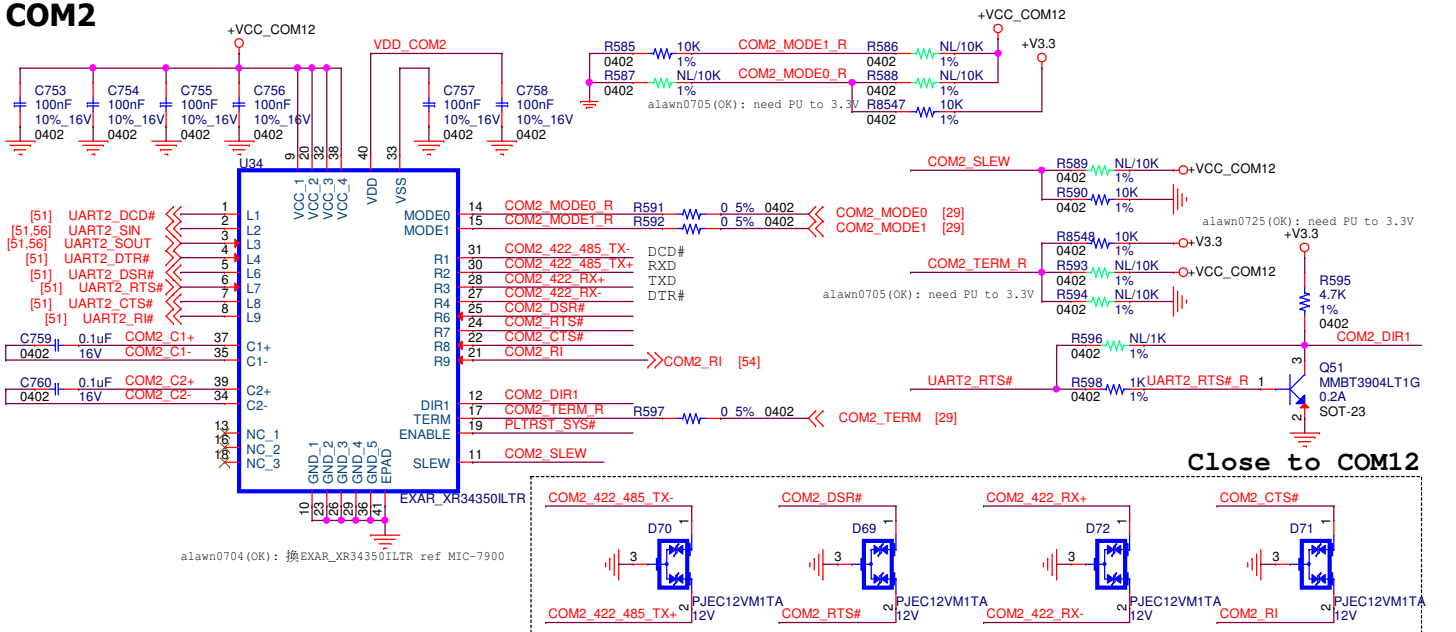
CONN COM1, 2(RS-232/422/485)

COM1

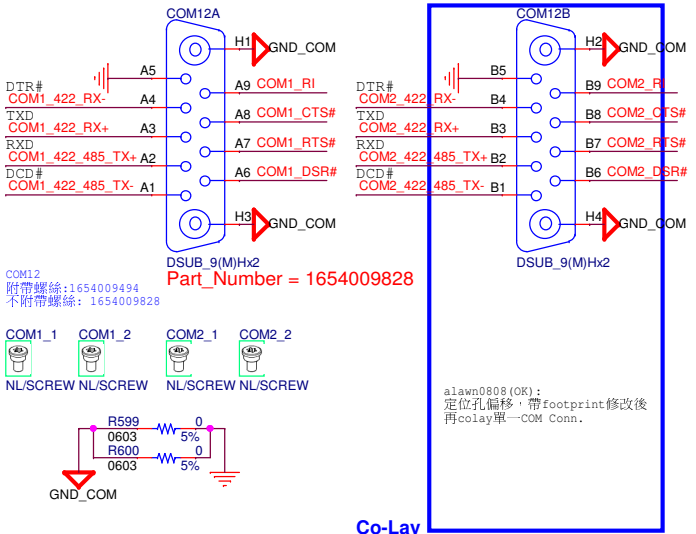


Close to COM12

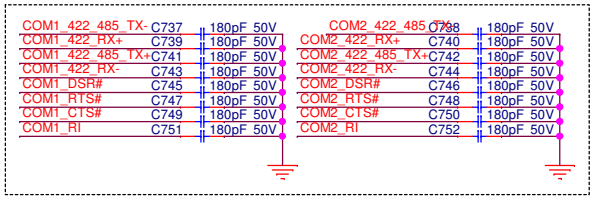
COM2



Close to COM12



Close to COM12



COM1/2 SP339E	LOOP BACK	RS-232	RS-485 half duplex	RS-485/422 full duplex
Mode0	0	1	0	1
Mode1	0	0	1	1
TERM	X	X	1	1
SLEW	0	0	0	0

TERM : Enables RS-485/422 receiver termination
SLEW : SLEW = VCC enables 250kbps slew limiting in all modes

Pin	RS-232	RS-422	RS-485
1	COM1_DCD	TXD-	Data-
2	COM1_SIN#	TXD+	Data+
3	COM1_SOUT#	RXD+	NC
4	COM1_DTR	RXD-	NC
5	GND	GND	GND
6	COM1_DSR	NC	NC
7	COM1_RTS	NC	NC
8	COM1_CTS	NC	NC
9	COM1_RI	NC	NC
10	GND_F	GND_F	GND_F
11	GND_F	GND_F	GND_F

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Title	53_CONN COM1, 2(RS-232/422/485)	
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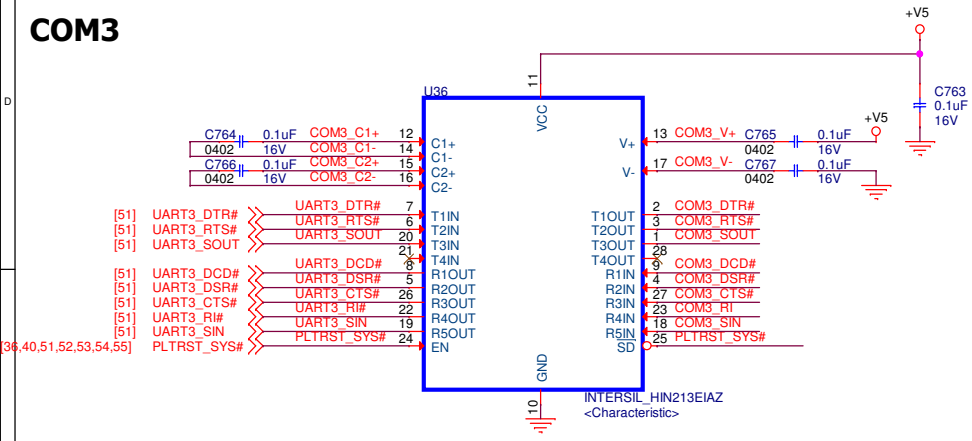
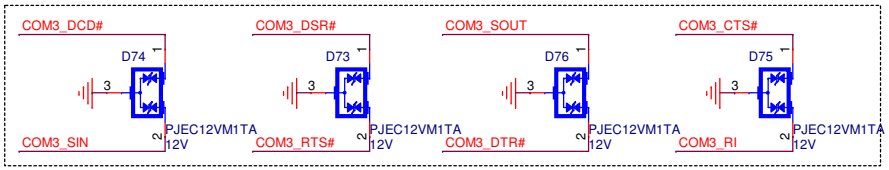
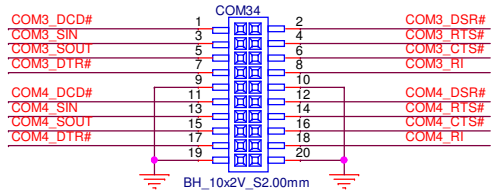
CONN COM3, 4(RS-232)/RING ON

COM3

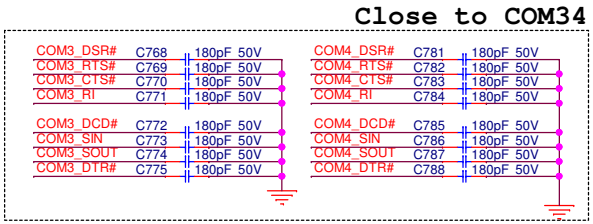


Close to COM34

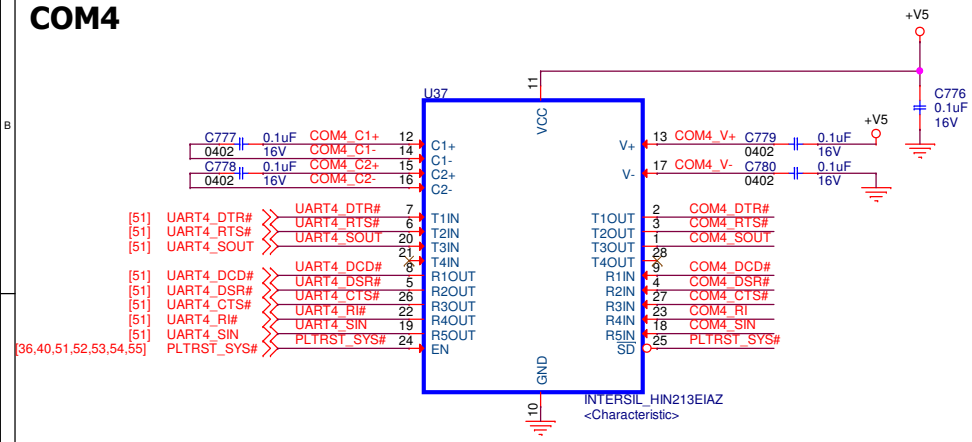




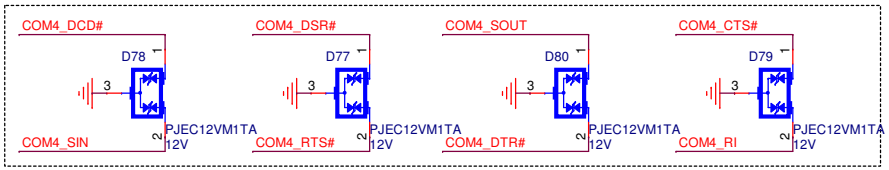
Close to COM34



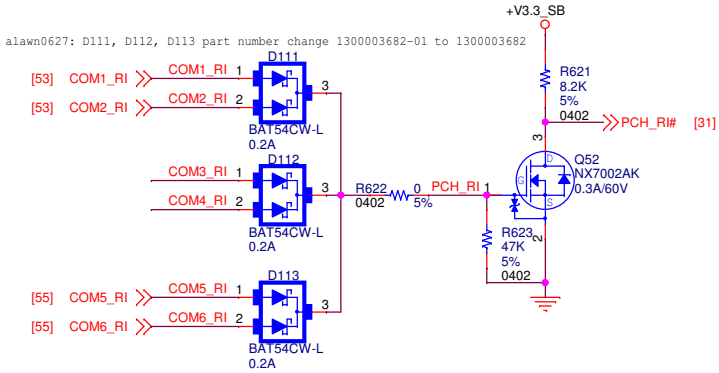
COM4



Close to COM34



Ring ON



Title	54_CONN COM3, 4(RS-232)/RING ON	
Size	Document Number: MIC-7700	Rev: A101-2
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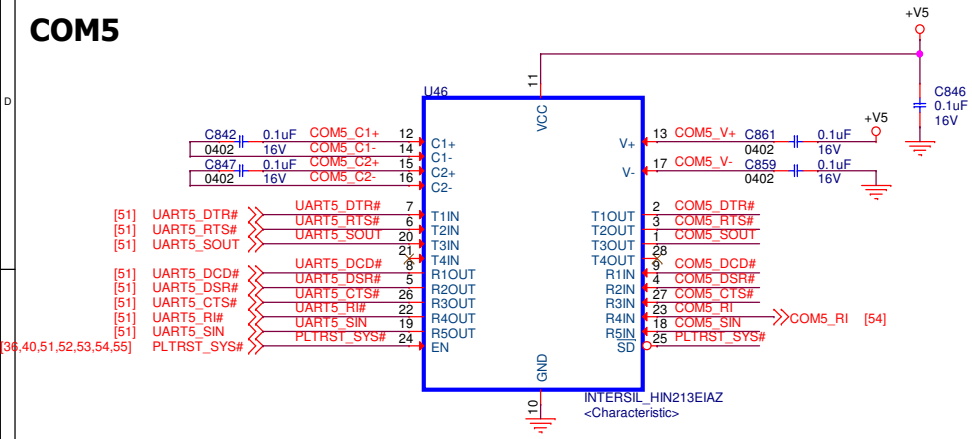
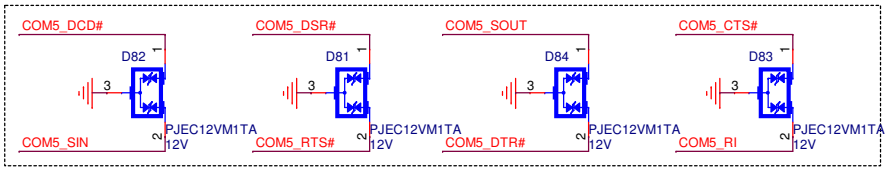
CONN COM5, 6(RS-232)

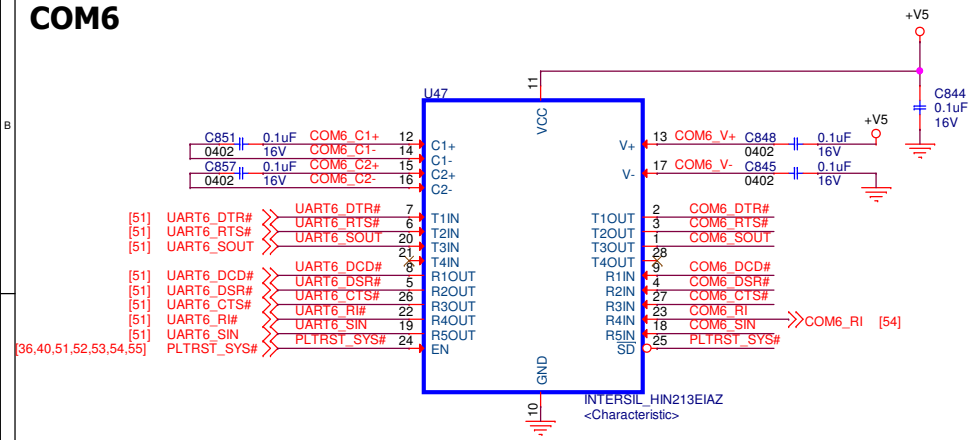
COM5



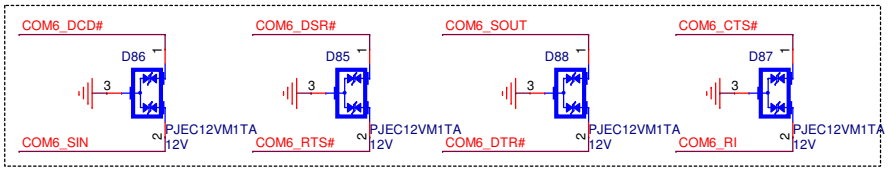
Close to COM56

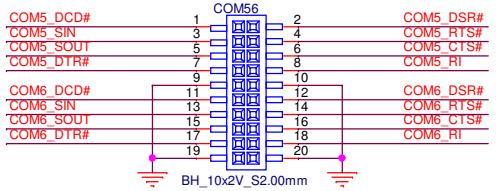


COM6

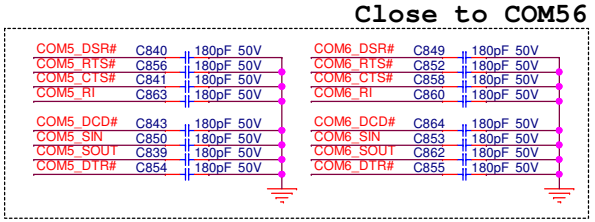


Close to COM56





Close to COM56



ADVANTECH

Title	55_CONN COM5, 6(RS-232	
Size	Document Number MIC-7700	Rev A101-2
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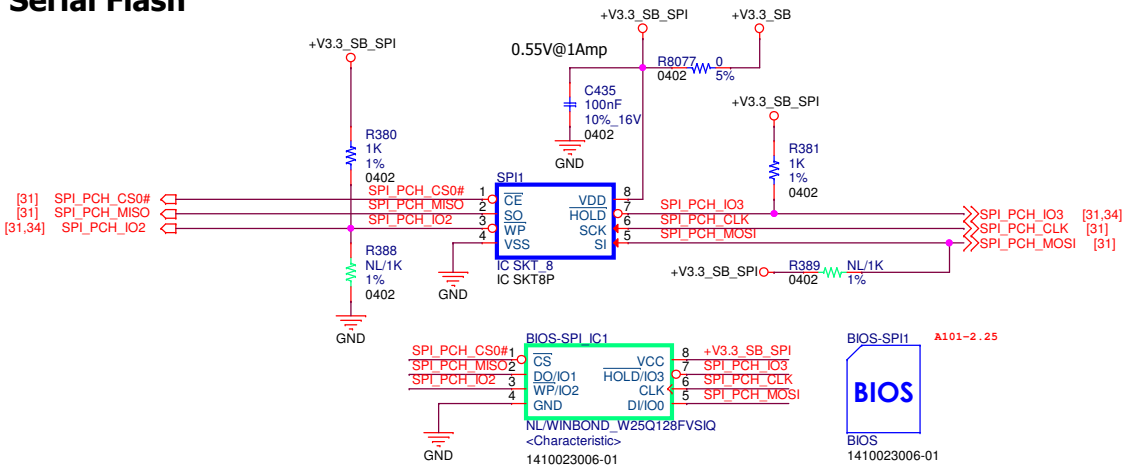
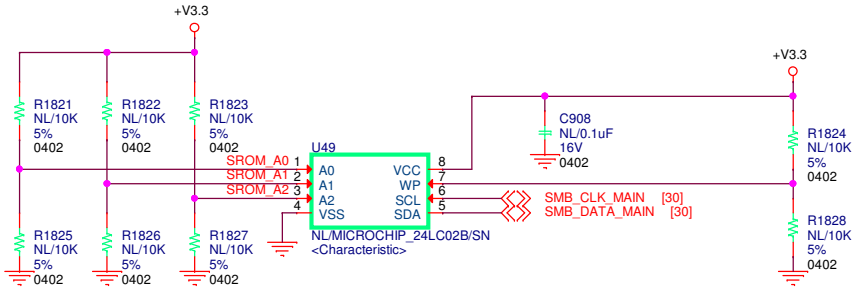
SPI/Security/LED

Serial Flash

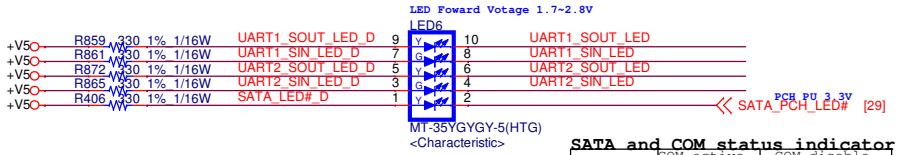


Secirity ROM 2 Kb



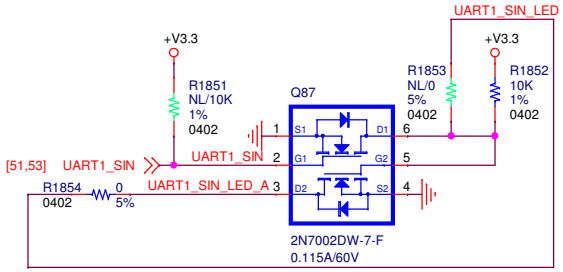
1010	A2	A1	A0	R/W#
1010	0	0	0	X

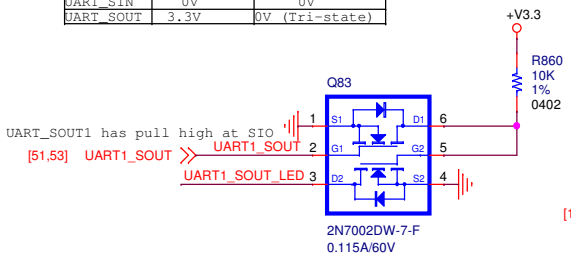
LED

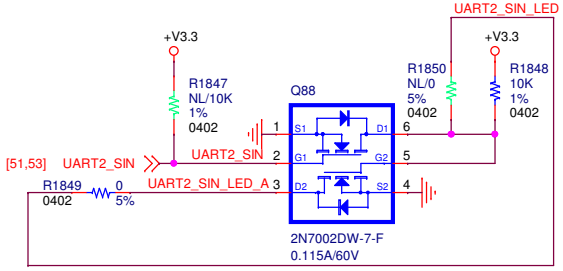


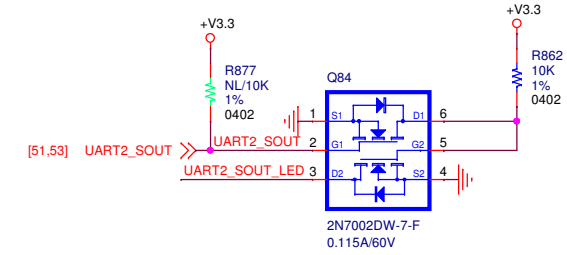
SATA and COM status indicator

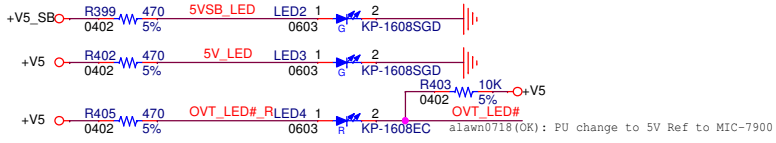
	COM active	COM disable
UART_SIN	0V	0V
UART_SOUT	3.3V	0V (Tri-state)

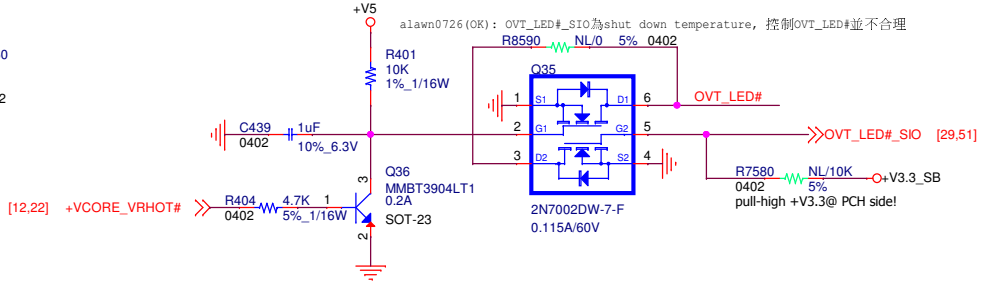










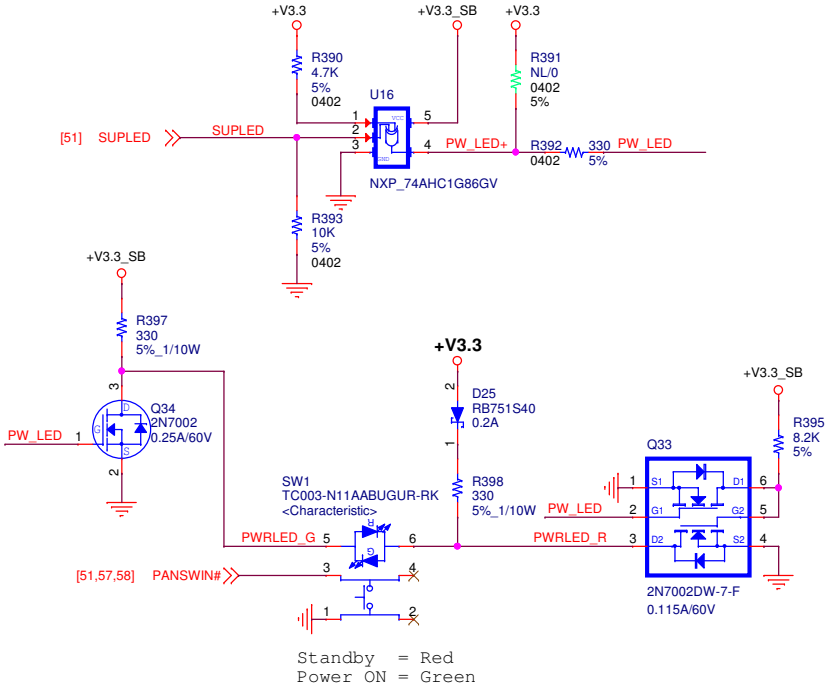


ADVANTECH

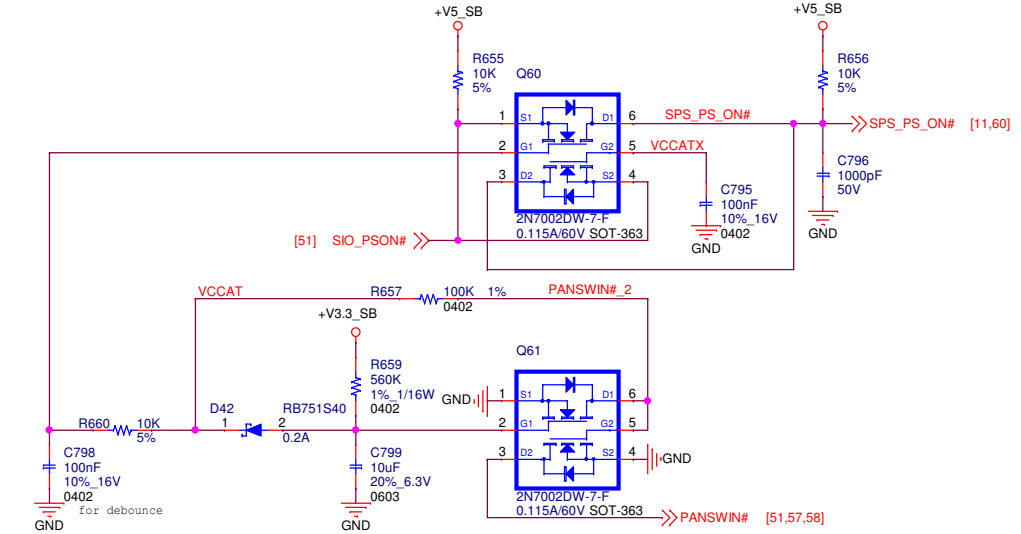
Title	56_SPI/Security/LED	
Size	Document Number MIC-7700	Rev A101-2
Date: Friday, March 03, 2017	Sheet 56 of 62	

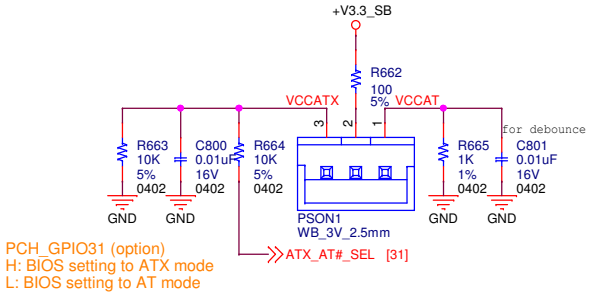
PWRBTN/AT_ATX Mode

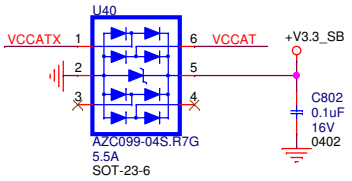
PWRBTN



ATX/AT Mode Selection







Mode	Jumper Setting
AT	1-2 Short
ATX	2-3 Short (Default)

Title	57_PWRBTN/AT_ATX Mode	
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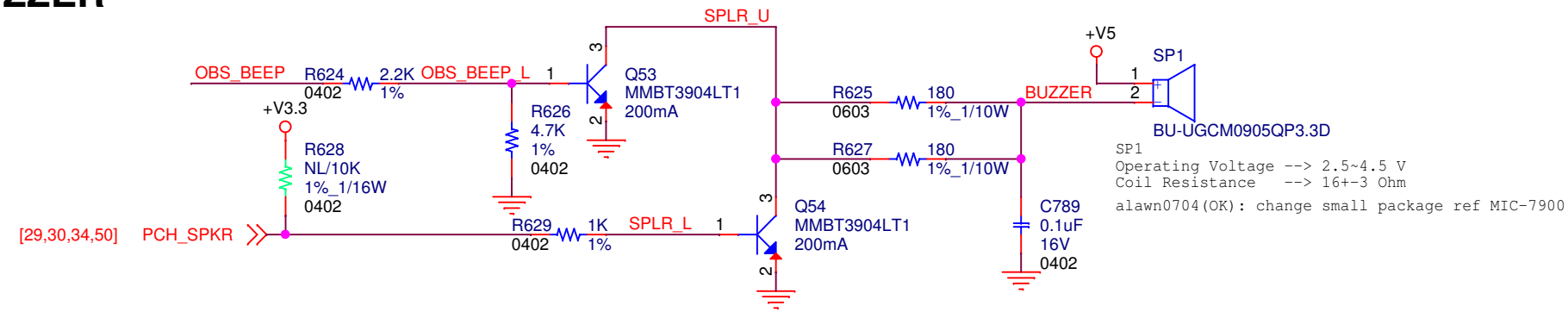
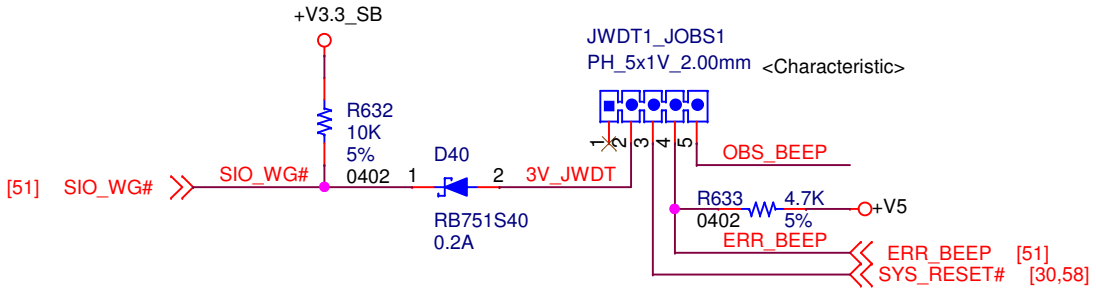
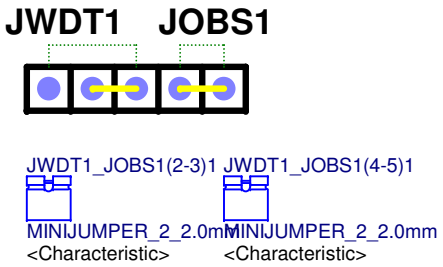
JFP1/JWDT1_JOBS1/SP1

BUZZER

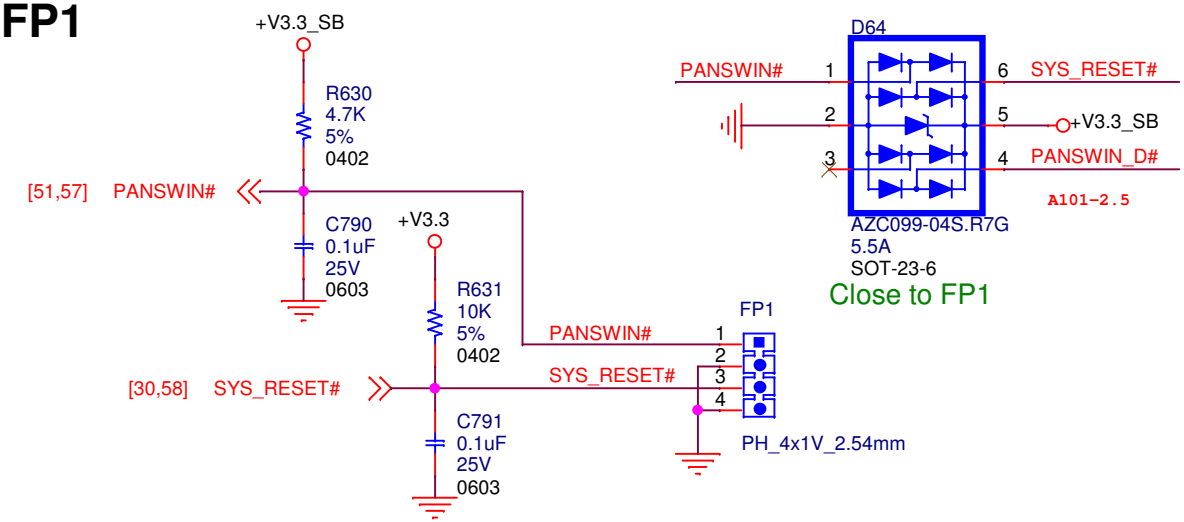


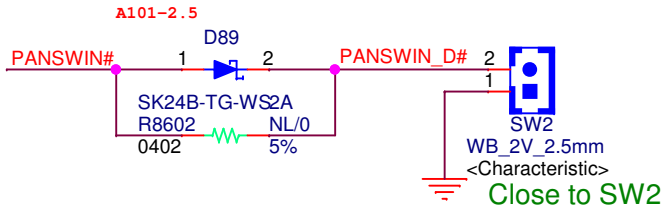
JWDT1_JOBS1





JFP1





ADVANTECH		
Title	58_JFP1/JWDT1_JOBS1/SP1	
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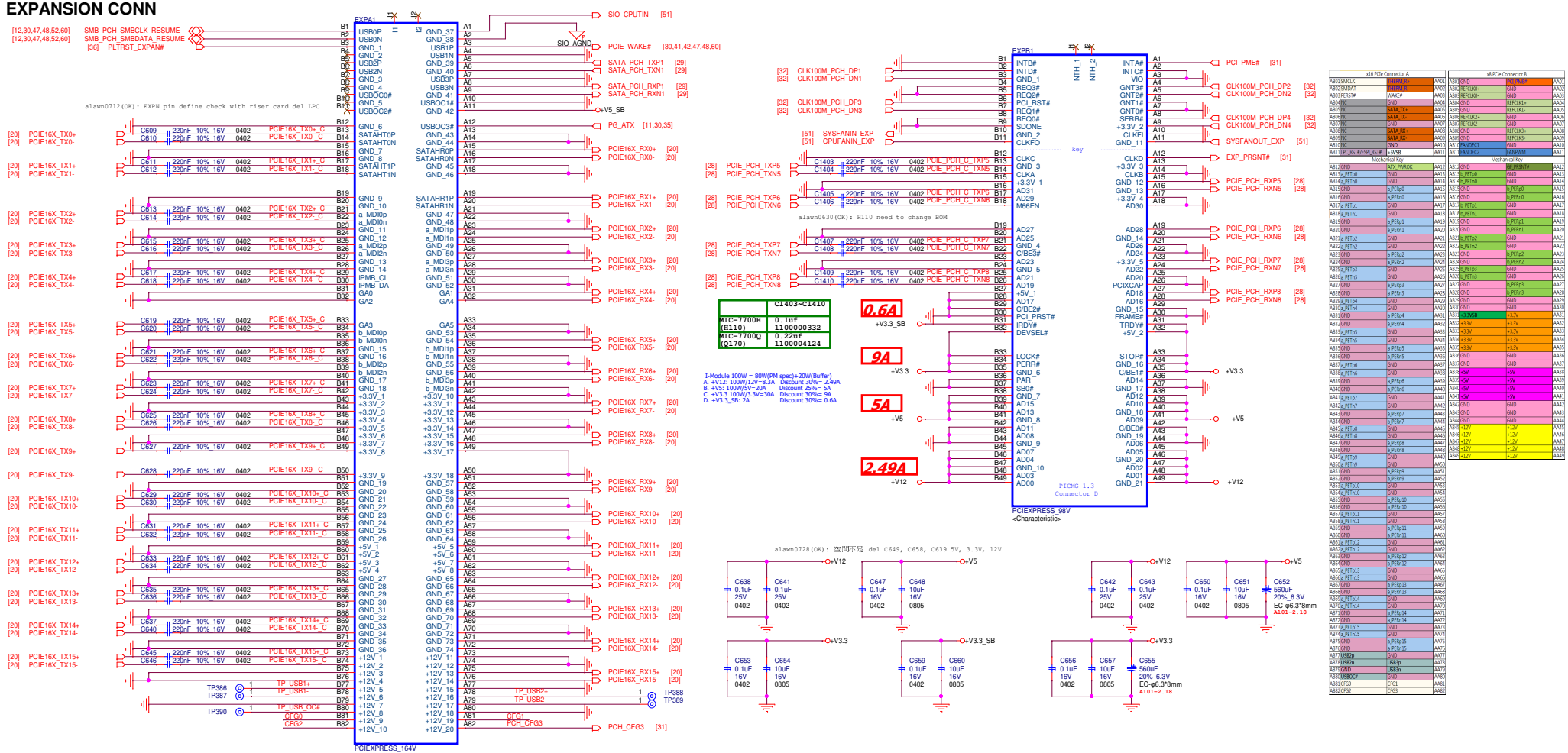
CONN EXPANSION Module

EXPANSION CONN



OTG Table

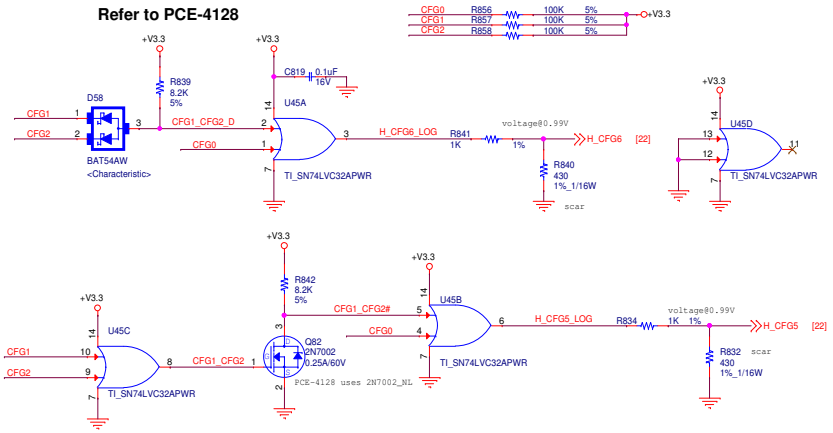
PCI-E x16 / x8 / x4 Configuration Table

From BP				To CPU1		
CFG0	CFG1	CFG2		H_CFG6	H_CFG5	PEG
1	---	---	→	1	1	1 x16
0	1	1	→	1	0	2 x8
0	1	0	→	0	0	1 x8/2 x4
0	0	0	→	0	1	4 x4(Reserved)

From BP		To PCH1
CFG3	→	PCI-E 5~8 Config
1	→	1 x4
0	→	4 x1

(Default)

Refer to PCE-4128



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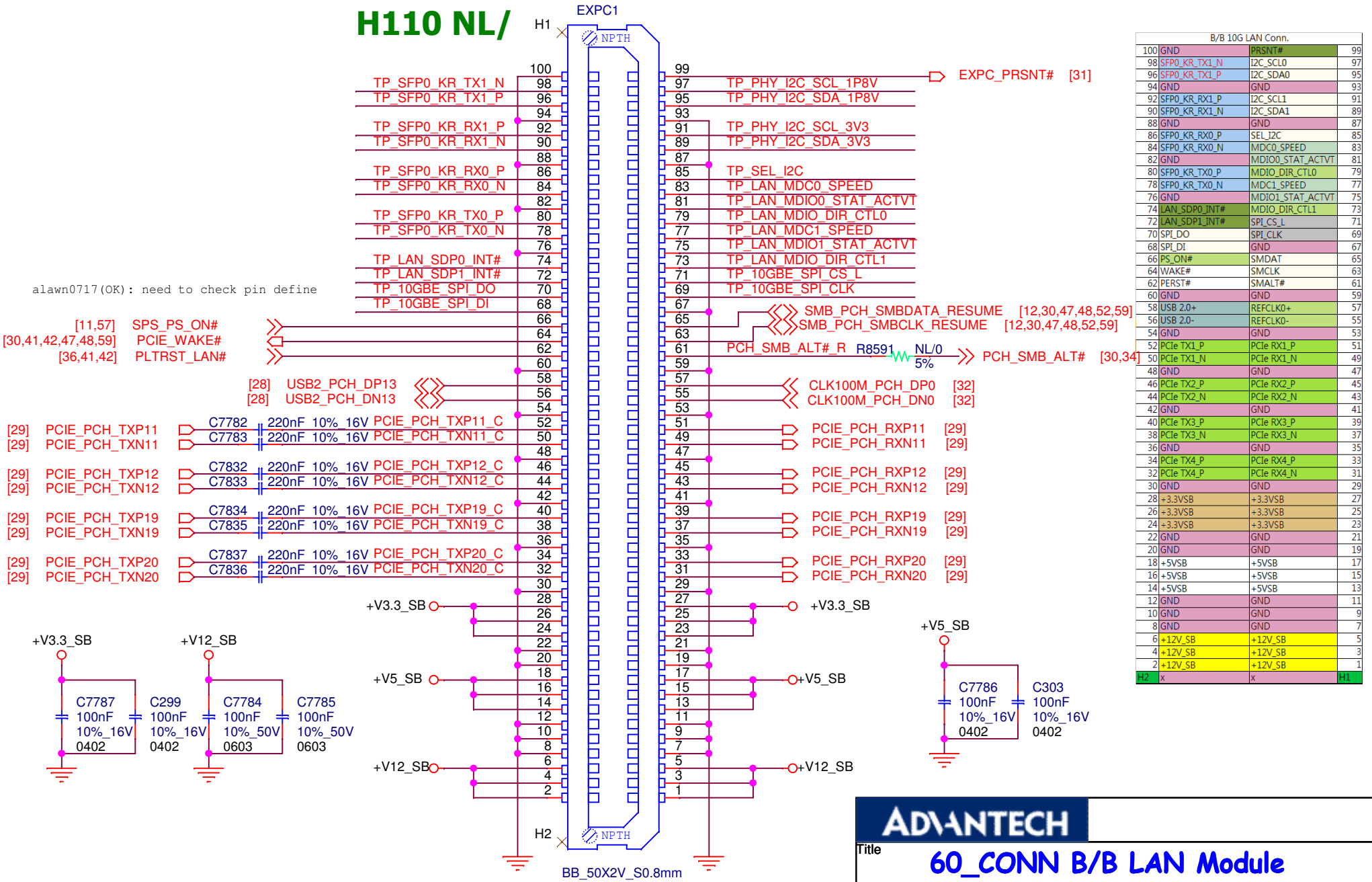
CONN B/B LAN Module

H110 NL/



B/B 10G LAN Conn.

100	GND	PRSNT#	99
98	SFP0_KR_TX1_N	I2C_SCL0	97
96	SFP0_KR_TX1_P	I2C_SDA0	95
94	GND	GND	93
92	SFP0_KR_RX1_P	I2C_SCL1	91
90	SFP0_KR_RX1_N	I2C_SDA1	89
88	GND	GND	87
86	SFP0_KR_RX0_P	SEL_I2C	85
84	SFP0_KR_RX0_N	MDC0_SPEED	83
82	GND	MDIO0_STAT_ACTVT	81
80	SFP0_KR_TX0_P	MDIO_DIR_CTL0	79
78	SFP0_KR_TX0_N	MDC1_SPEED	77
76	GND	MDIO1_STAT_ACTVT	75
74	LAN_SDP0_INT#	MDIO_DIR_CTL1	73
72	LAN_SDP1_INT#	SPI_CS_L	71
70	SPI_DO	SPI_CLK	69
68	SPI_DI	GND	67
66	PS_ON#	SMDAT	65
64	WAKE#	SMCLK	63
62	PERST#	SMALT#	61
60	GND	GND	59
58	USB 2.0+	REFCLK0+	57
56	USB 2.0-	REFCLK0-	55
54	GND	GND	53
52	PCIe TX1_P	PCIe RX1_P	51
50	PCIe TX1_N	PCIe RX1_N	49
48	GND	GND	47
46	PCIe TX2_P	PCIe RX2_P	45
44	PCIe TX2_N	PCIe RX2_N	43
42	GND	GND	41
40	PCIe TX3_P	PCIe RX3_P	39
38	PCIe TX3_N	PCIe RX3_N	37
36	GND	GND	35
34	PCIe TX4_P	PCIe RX4_P	33
32	PCIe TX4_P	PCIe RX4_N	31
30	GND	GND	29
28	+3.3VSB	+3.3VSB	27
26	+3.3VSB	+3.3VSB	25
24	+3.3VSB	+3.3VSB	23
22	GND	GND	21
20	GND	GND	19
18	+5VSB	+5VSB	17
16	+5VSB	+5VSB	15
14	+5VSB	+5VSB	13
12	GND	GND	11
10	GND	GND	9
8	GND	GND	7
6	+12V_SB	+12V_SB	5
4	+12V_SB	+12V_SB	3
2	+12V_SB	+12V_SB	1
H2	x	x	H1

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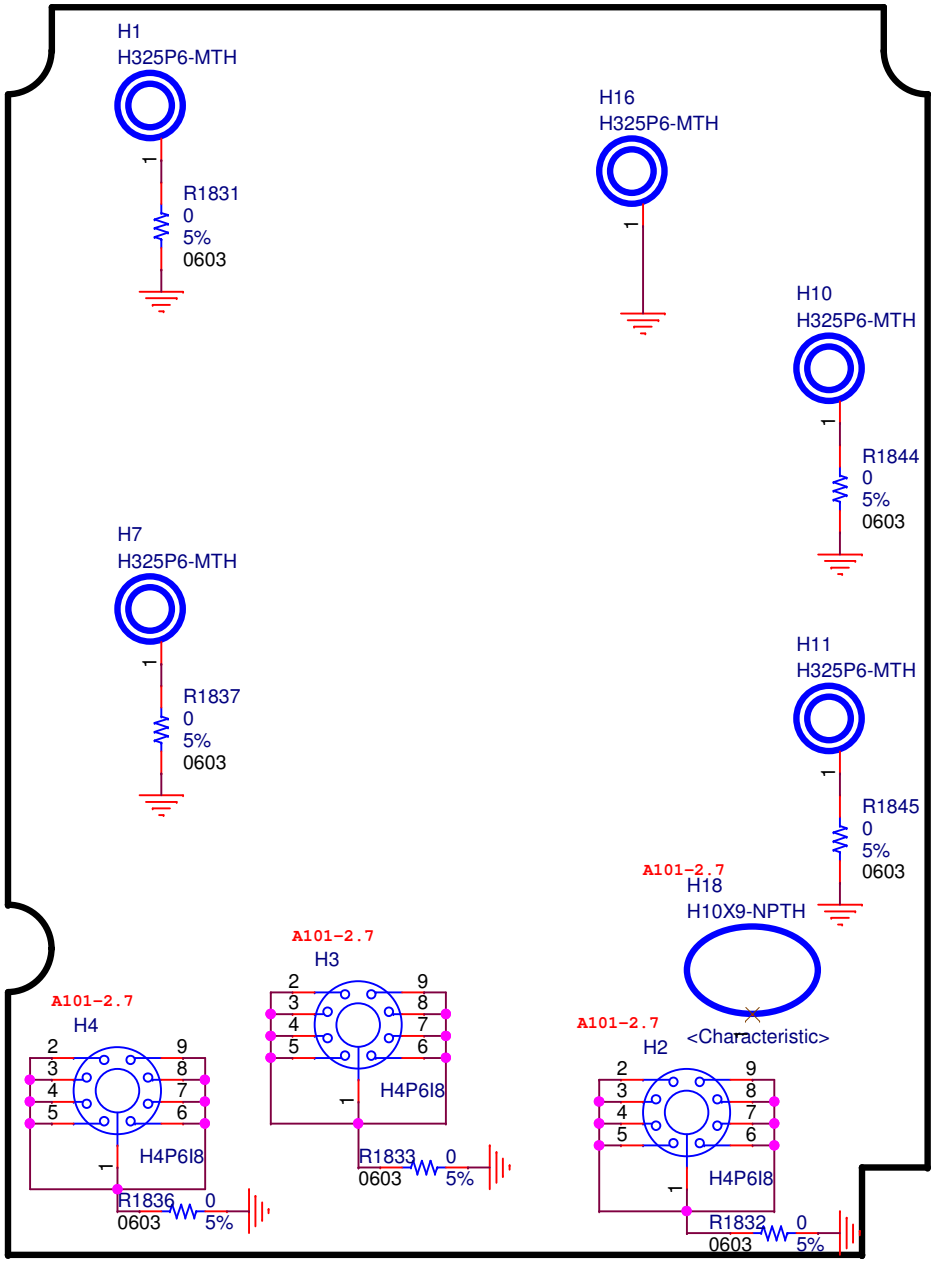
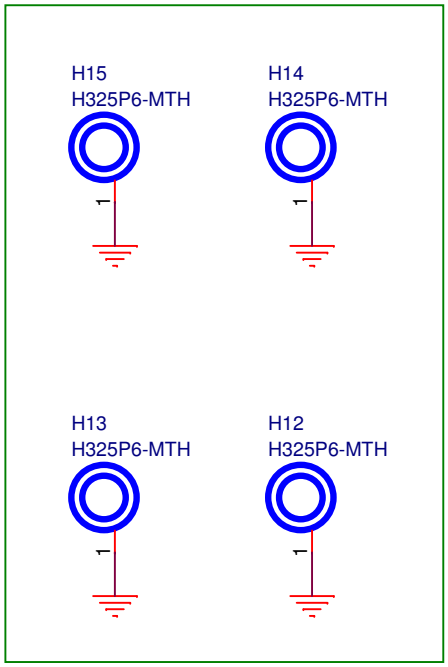
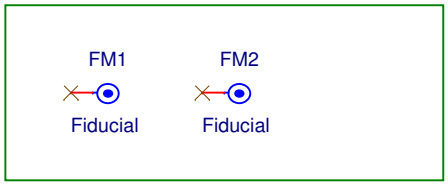
Other BOM

Board CPU Side

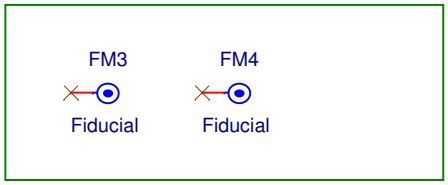


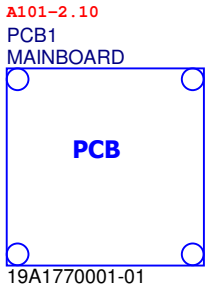
For CPU thermal module CPU side

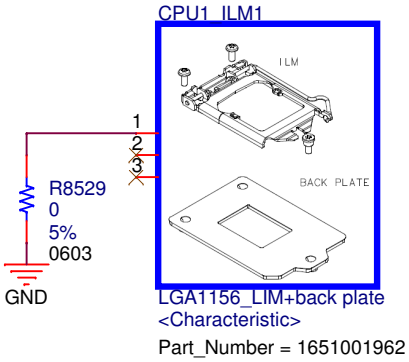




IO side







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Title	61_Other BOM	
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History

MIC-7700H MIC-7700Q

MIC-7700 ECOP-116297 ECOP-116298 A101-1 PCB: 19A1770000-01 (8 Layer) RD: Alawn.Lee 2016/6/14
MIC-7700 ECOP-117790 ECOP-117791 A101-1 PCB: 19A1770000-01 (8 Layer) RD: Alawn.Lee 2016/6/14

MIC-7700 ECOP-119755 ECOP-119756 A101-2 PCB: 19A1770001-01 (8 Layer) RD: Alawn.lee 2016/11/18
1. BOM: Remove R696, -->GPIO_PORT80_SEL floating
2. Sch: Remove B183,C7357,Add R8601, C7842 -->For On off solution
3. BOM: C7338 need to change to 15pF -->crystal matching change to 15pF
4. BOM: ALC892 change to ALC888S -->PM Spec change
5. Sch: Reserve R8602, PANSWIN_D# connect to D64 , D89 change to 1300000163 -->Protect D89 for ESD
6. BOM: Remove R1861, Stuff R1864 -->Remove VGA dummy load
7. Sch: H2, H3, H4 part number change to 0010000033, H18 part number change to 0020200094 -->ME modify screw size
8. BOM: Remove R1725, R1726, R1727, R1751, R8571, R8570, R8569, R8568 -->DVI, HDMI eye diagram fail
9. BOM: PR100 change to 215k ohm -->+V1.0_SB Ripple Fail
10. BOM: PCB Part Number change to 19A1770001-01 -->PCB Part Number update
11. Sch: LAN2 disable function follow MIC-7900 A101-4 -->LAN2 disable function
12. BOM: U115 are changed from 1410020979-11 to 1410024453-01, R8081, R8082 change to 10k -->Due to 1410020979-11 phase out.
13. Sch: Add R8606~R8613 -->For +V1.0_SB Dummy load
14. Sch: +V1.2_VGA LDO Change APL5912KAC-TRL, Add R8618~R8621, Reverse C7851, C7852, Add C7855~C7861, C555 change 1nF -->try to fix VGA ripple
15. BOM: H110 SKU do not need DP2 function -->Cost Down

MIC-7700 ECOP-120859 ECOP-120860 A101-2 PCB: 19A1770001-01 (8 Layer) RD: Alawn.lee 2017/2/6
16. BOM: H110 SKU Stuff R8533 -->H110 SKU DP2_OC# need to Pull High
17. BOM: PR100 change to 210k ohm -->+V1.0_SB Ripple Fail
18. BOM: 1100006542-01 change to 1100006542-05
, 1100006644-01 change to 1100006644-05 -->Different Package
19. BOM: C7337 change to 18pF -->XTAL32.768K_PCH_RTCX1 cannot meet the specification.
20. BOM: H110 SKU LAN2 change to i210IT -->temperature over spec
21. BOM: U120 change to 1420041027 -->add Vcore FW code
22. BOM: Add IMG-115 -->For LAN2 i210 Image
23. BOM: USB3_5678 change to 1654010908-02 -->Phase out

MIC-7700 ECOP-121317 ECOP-121318 A101-2 PCB: 19A1770001-01 (8 Layer) RD: Alawn.lee 2017/3/3
24. BOM: JCFG(1-2)1 Part Reference change to JCFG1(1-2)1 -->Follow naming rule
25. BOM: Add BIOS Part Number -->Add BIOS Part Number

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Title: 62_History		
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