Model Name: PCE-3029 / PCE-4129 A101-2

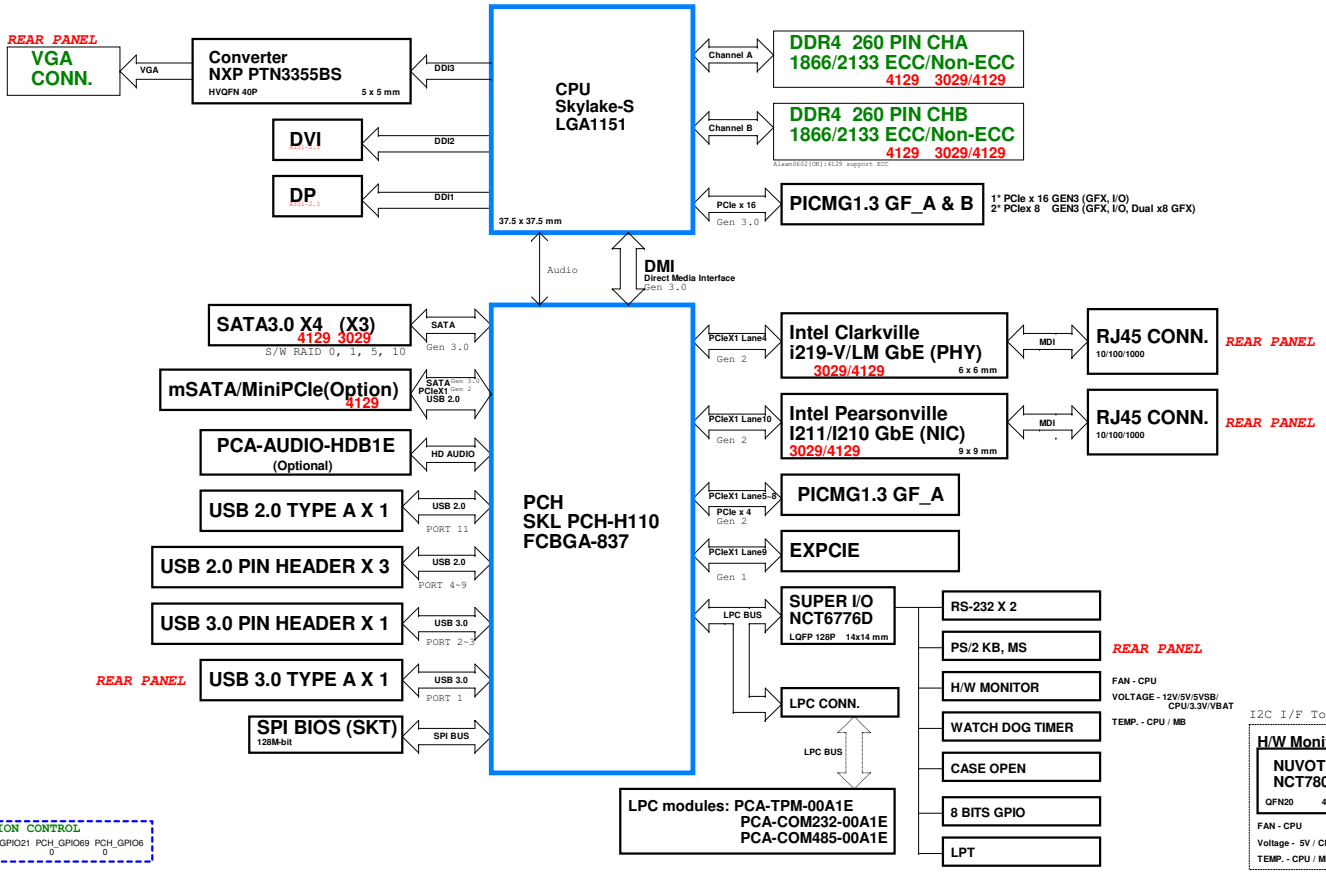
Approved by	Checked by	Prepared by

Checked MOW : WW35'12

ADVANTECH

Title: COVER PAGE		
Size	Document Number: PCE-3029/PCE-4129	Rev: A101-2
Date: Tuesday, December 01, 2015	Sheet 1 of 55	

PCE-3029 / PCE-4129 Board Diagram



PCB VERSION CONTROL

Rev. ID:	PCH_GPIO21	PCH_GPIO69	PCH_GPIO6
A101-1->	0	0	0

I2C I/F To JFP1+JFP2

H/W Monitor

NUVOTON NCT7802Y

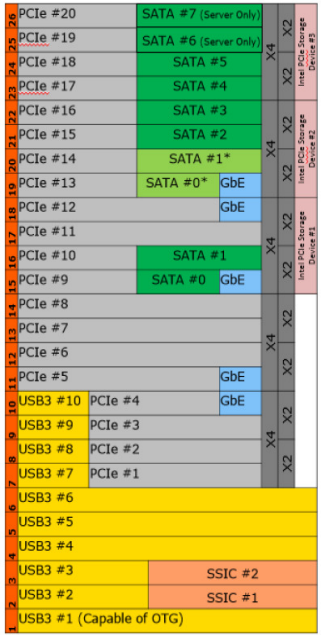
QFN20 4 x 4 mm

FAN - CPU

Voltage - 5V / CPU

TEMP. - CPU / MB

Fliexible I/O



	PCE-4129 C236	PCE-3029 H110
26	X	N/A
25	X	N/A
24	X	N/A
23	SATA4 (mSATA/miniPCIe)	N/A
22	SATA3	SATA3 (mSATA)
21	SATA2	SATA2
20	SATA1	SATA1
19	SATA0	SATA0
18	X	N/A
17	X	N/A
16	LAN2 (i210-AT)	LAN2 (i211-AT)
15	EXPCIE1	EXPCIE1
14	PICMG 1.3 x4	PICMG 1.3 x4
13		
12		
11		
10	LAN1 (PHY, i219)	LAN1 (PHY, i219)
9	X	N/A
8	X	N/A
7	X	N/A
6	X	N/A
5	X	N/A
4	X	X
3	USB 3.0 BOX Header	USB 3.0 BOX Header
2	USB 3.0 BOX Header	USB 3.0 BOX Header
1	USB 3.0 Rear IO	USB 3.0 Rear IO

Jumper List

JME1(1-2)
JCMOS1(1-2)
JWDT1_JOBS1(2-3)
JWDT1_JOBS1(4-5)

MODEL LIST

Orcad BOM	Model	PCH	LAN1	LAN2	MEMORY SUPPORT	VGA	DP/DVI	COM	USB2.0	USB 2.0 Type A	USB3.0	USB 3.0 Type A	SATA3.0	AMT 9.0	RAID	NCT7802Y	MINIPCIE/mSATA	EXPCIE1
Part_Number_Value		C236	Intel I219LM (PHY)	Intel I210AT (NIC)	ECC SO-DIMM	YES	1/1	2	6	1	2	1	4	NO	YES	YES	(Option)/Yes	YES
Part_Number_3029	PCE-3029WG2-00A1E	H110	Intel I219V (PHY)	Intel I211AT (NIC)	Non-ECC SO-DIMM	YES	1/1	2	6	1	2	1	3	NO	NO	YES	NO/Yes	YES
Part_Number_4129	PCE-4129G2-00A1E	C236	Intel I219LM (PHY)	Intel I210AT (NIC)	ECC/Non-ECC SO-DIMM	YES	1/1	2	6	1	2	1	4	NO	YES	YES	(Option)/Yes	YES

Table 1-3. PCH-H HSIO Detail (Lane 1-14)

SKU	1	2	3	4	5	6	7	8	9	10	11	12	13	14
H110	USB 3.0/ OTG	USB 3.0	USB 3.0	USB 3.0	N/A	N/A	N/A	N/A	N/A	LAN Only	PCIe/ LAN	PCIe	PCIe	PCIe

Table 1-4. PCH-H HSIO Detail (Lane 15-26)

SKU	15	16	17	18	19	20	21	22	23	24	25	26
H110	PCIe/ LAN	PCIe	N/A	LAN Only	SATA/ LAN	SATA*	SATA	SATA	N/A	N/A	N/A	N/A

Table 1-6. Server/Workstation PCH HSIO Detail (Lane 1-13)

SKU	1	2	3	4	5	6	7	8	9	10	11	12	13
C236	USB 3.0/ OTG	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0	USB 3.0/ PCIe	USB 3.0/ PCIe	USB 3.0/ PCIe	USB 3.0/ PCIE/ LAN	PCIe/ LAN	PCIe	PCIe

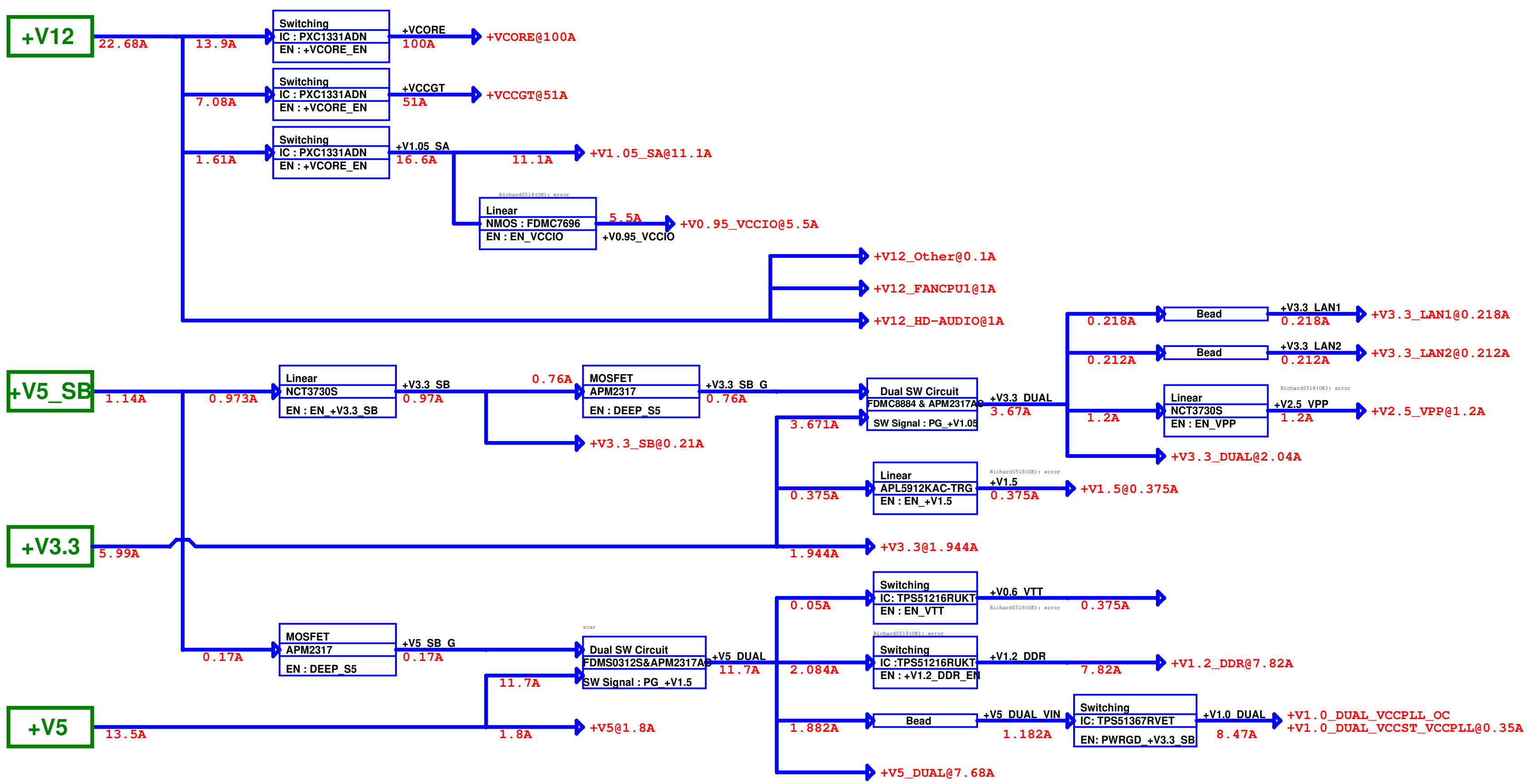
Table 1-7. Server/Workstation PCH HSIO Detail (Lane 14-26)

SKU	14	15	16	17	18	19	20	21	22	23	24	25	26
C236	PCIe	SATA/ PCIe/ LAN	SATA/ PCIe	PCIe	PCIE/ LAN	SATA/ PCIE/ LAN	SATA/ PCIe	SATA/ PCIe	SATA/ PCIe	SATA/ PCIe	SATA/ PCIe	SATA/ PCIe	SATA/ PCIe

ADVANTECH

Title	BOARD DIAGRAM	
Size	Document Number: PCE-3029/PCE-4129	Rev: A101-2
Date: Tuesday, December 01, 2015	Sheet 2 of 55	

PCE-3029 / PCE-4129 POWER DELIVERY

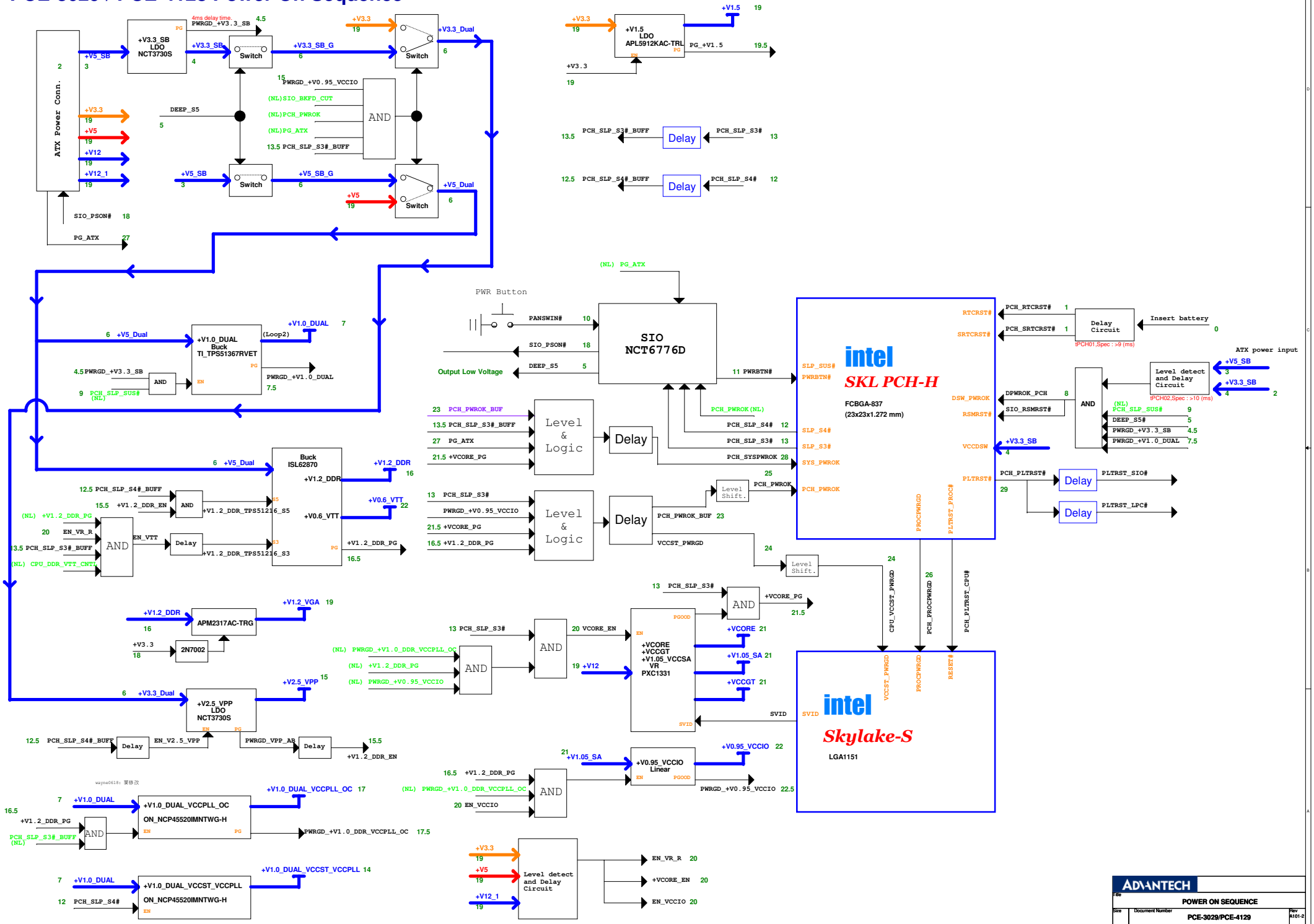


(Step 1) Source Power Input		Discount 電流及Watt		
OrCAD Net name	Voltage	Max Current (A)	P = I x V	Max Power (W)
+V12	12 V	22.69 A	→	272.23 W
+V12_1	12 V	2.00 A	→	24.00 W
+V5	5 V	20.13 A	→	100.65 W
+V3.3	3.3 V	5.99 A	→	19.76 W
+V5_SB	5 V	0.21 A	→	1.07 W
-V12	-12 V	0.00 A	→	0.00 W
-V5	-5 V	0.00 A	→	0.00 W
			Total (Watt)	417.71 W

Richard0518(OK): error

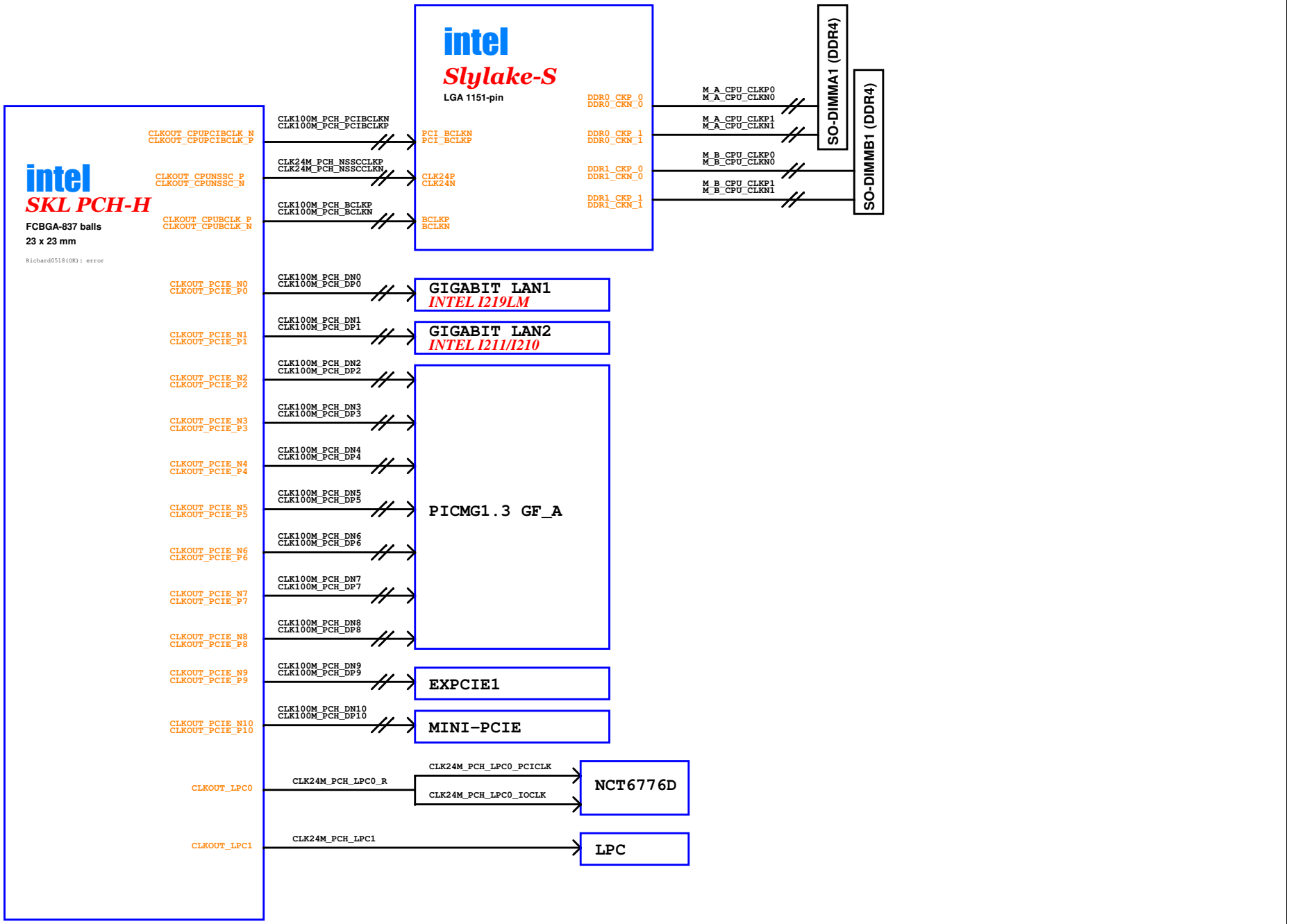
Source	+V12	12 V			Total: 23A																						
	+V12	12 V	90%	7.08A	→	+VCCGT	1.5 V		51 A	Total: 51A	Buck	PXC1410A +															
	+V12	12 V	90%	13.9A	→	+VCORE	1.5 V		100 A	Total: 100A	Buck	PXC1410A															
	+V12	12 V	90%	1.61A	→	+V1.05_SA	1.05 V		11 A	Total: 17A	Buck	PXC1410A															
						+V1.05_SA	1.05 V	Linear	5.5A	→	+V0.95_VCCIO	0.95 V		5.5 A	Total: 5.5A	LDO	TI_LM358 +										
Source	+V12_1	12 V		0 A	Total: 2A																						
Source	+V3.3	3.3 V			Total: 6A																						
	+V3.3	3.3 V	Linear	0.38A	→	+V1.5	1.5 V		0.4 A	Total: 0.4A	LDO	APL5912															
	+V3.3	3.3 V	100%	0.08A	→	+V1.8_SB_GGPPD	3.3V		0.1 A	Total: 0.1A	PassMOS	0 Ohm															
	+V3.3	3.3 V	100%	0.08A	→	+V3.3_VGA	3.3 V		0.1 A	Total: 0.1A	PassMOS	Bead															
	+V3.3	3.3 V	100%	3.67A	→	+V3.3_DUAL	3.3 V		0 A	Total: 3.7A	PassMOS	FDMC8884															
						+V3.3_DUAL	3.3 V	100%	0.08A	→	+V3.3_DUAL DVDDIO_A	3.3 V		0.1 A	Total: 0.1A	PassMOS	Bead										
						+V3.3_DUAL	3.3 V	100%	0.08A	→	+V3.3_DUAL GPPA	3.3 V		0.1 A	Total: 0.1A	PassMOS	0 Ohm										
						+V3.3_DUAL	3.3 V	100%	0.22A	→	+V3.3_LAN1	3.3 V		0.2 A	Total: 0.2A	PassMOS	Bead										
						+V3.3_DUAL	3.3 V	100%	0.21A	→	+V3.3_LAN2	3.3 V		0.2 A	Total: 0.2A	PassMOS	Bead										
						+V3.3_DUAL	3.3 V	Linear	1.2A	→	+V2.5_VPP	2.5 V		1.2 A	Total: 1.2A	LDO	APL5912										
Source	+V5	5 V		0 A	Total: 14A																						
	+V5	5 V	100%	0.06A	→	+V5_VGA	5 V		0.1 A	Total: 0.1A	PassMOS	Bead															
	+V5	5 V	100%	11.7A	→	+V5_DUAL	5 V		0.5 A	Total: 12A	PassMOS	FDMC7696															
						+V5_DUAL	5 V	90%	2.08A	→	+V1.2_DDR	1.2 V		2.8 A	Total: 7.8A	Buck	TPS51216(1)										
						+V5_DUAL	5 V	90%	0.05A	→	+V0.6_VTT	0.6 V		0.4 A	Total: 0.4A	Buck	TPS51216(2)										
						+V5_DUAL	5 V	90%	1.88A	→	+V1.0_DUAL	1 V		6 A	Total: 8.5A	Buck	TI_LM358 +										
											+V1.0_DUAL	1 V	100%	0.12A	→	+V1.0_DUAL VCCAMPH	1 V		0 A	Total: 0.1A	PassMOS	0 Ohm					
											+V1.0_DUAL	1 V	100%	0.05A	→	+V1.0_DUAL VCCAPLL	1 V		0 A	Total: 0A	PassMOS	0 Ohm					
											+V1.0_DUAL	1 V	100%	0.01A	→	+V1.0_DUAL VCCF24	1 V		0 A	Total: 0A	PassMOS	0 Ohm					
											+V1.0_DUAL	1 V	100%	0.26A	→	+V1.0_DUAL VCCPLL_O	1 V		0.3 A	Total: 0.3A	PassMOS	AP2306GN(131					
											+V1.0_DUAL	1 V	100%	0.35A	→	+V1.0_DUAL VCCST_VC	1 V		0 A	Total: 0.4A	PassMOS	AP2306GN(131					
Source	+V5_SB	5 V			Total: 1.1A											+V1.0_DUAL VCCST_VC	1 V	100%	0.1A	→	+V1.0_DUAL	1 V		0.1 A	#####	PassMOS	0 Ohm
	+V5_SB	5 V	100%	0.17A	→	+V5_SB_G	5V		0.2 A	Total: 0.2A	PassMOS																
	+V5_SB	5 V	Linear	0.97A	→	+V3.3_SB	3.3 V		0 A	Total: 1A	LDO	APL5912															
						+V3.3_SB	3.3 V	100%	0.76A	→	+V3.3_SB_G	3.3V		0.8 A	Total: 0.8A	PassMOS											

PCE-3029 / PCE-4128 Power On Sequence



ADVANTECH			
Title	POWER ON SEQUENCE		
Size	Document Number	PCE-3029/PCE-4129	Rev A101-2
Date: Tuesday, December 01, 2015	Sheet 4 of 55		

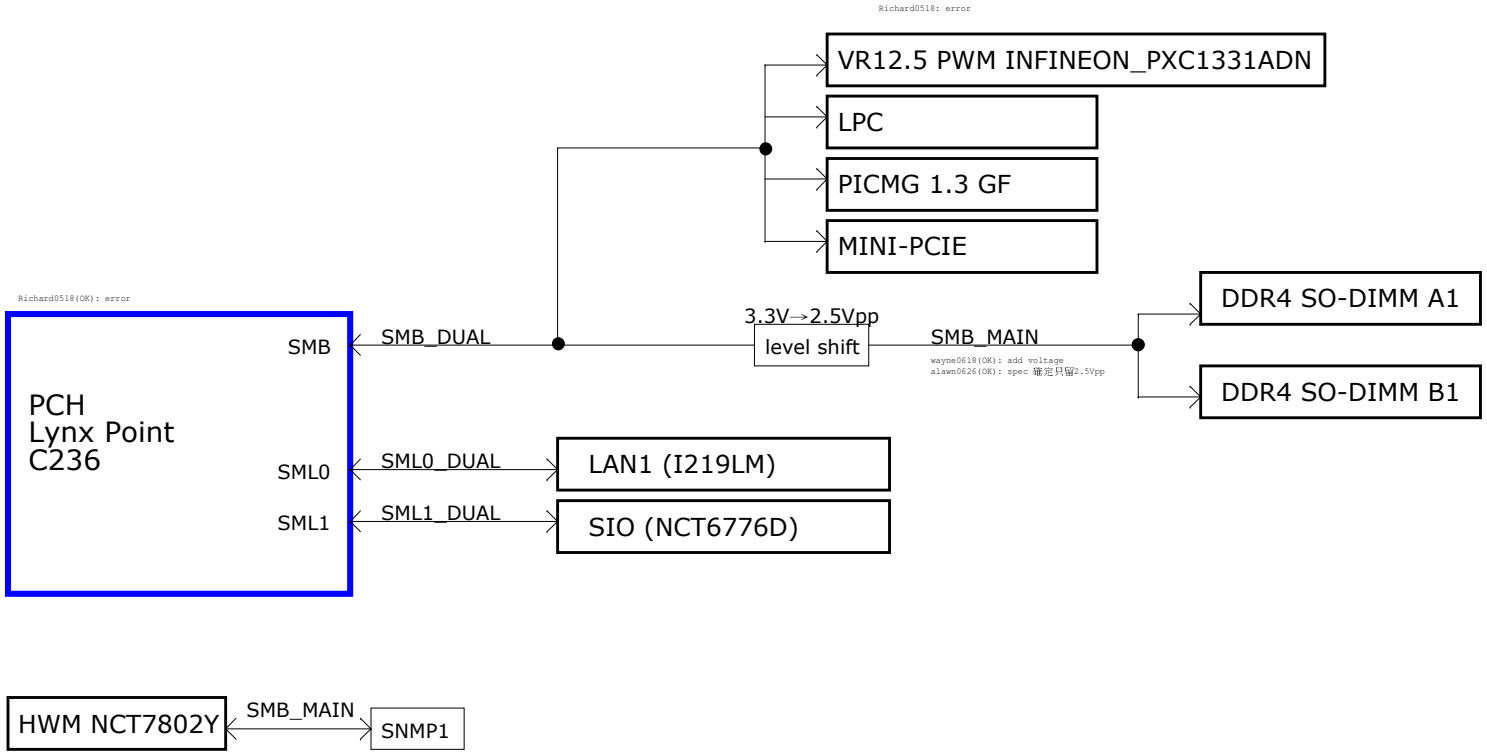
CLOCKS DISTRIBUTION



ADVANTECH

Title	CLOCKS DISTRIBUTION	
Size	Document Number PCE-3029/PCE-4129	Rev A101-2
Date: Tuesday, December 01, 2015	Sheet 5 of 55	

SMBUS DISTRIBUTION



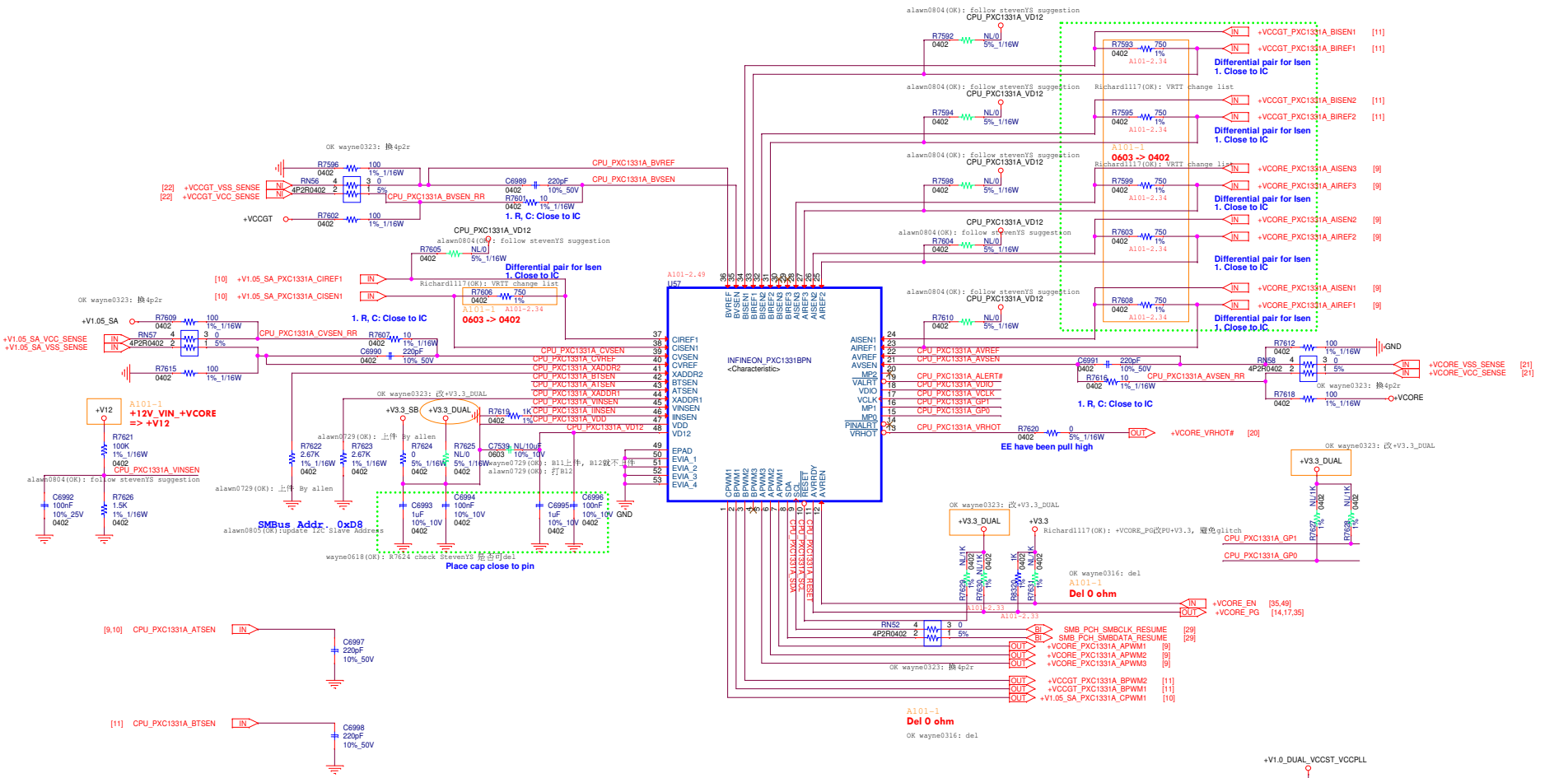
Title	SMBUS DISTRIBUTION	
Size	Document Number PCE-3029/PCE-4129	Rev A101-2
Date: Tuesday, December 01, 2015	Sheet 6 of 55	

Richard0518(OK):check with PM，没support可以删掉
wayne0618(OK): del

ADVANTECH		
Title	JTAG DISTRIBUTION	
Size	Document Number PCE-3029/PCE-4129	Rev A101-2
Date: Tuesday, December 01, 2015	Sheet 7 of 55	

PWR [VCORE+VSA PWM IC]

+VCORE Iomax=79A
+V1.05_SA Iomax=12.3A
+VCCGT Iomax=51A



alawn0805(OK):update I2C Slave Address

Table 6: Device I2C Slave Address

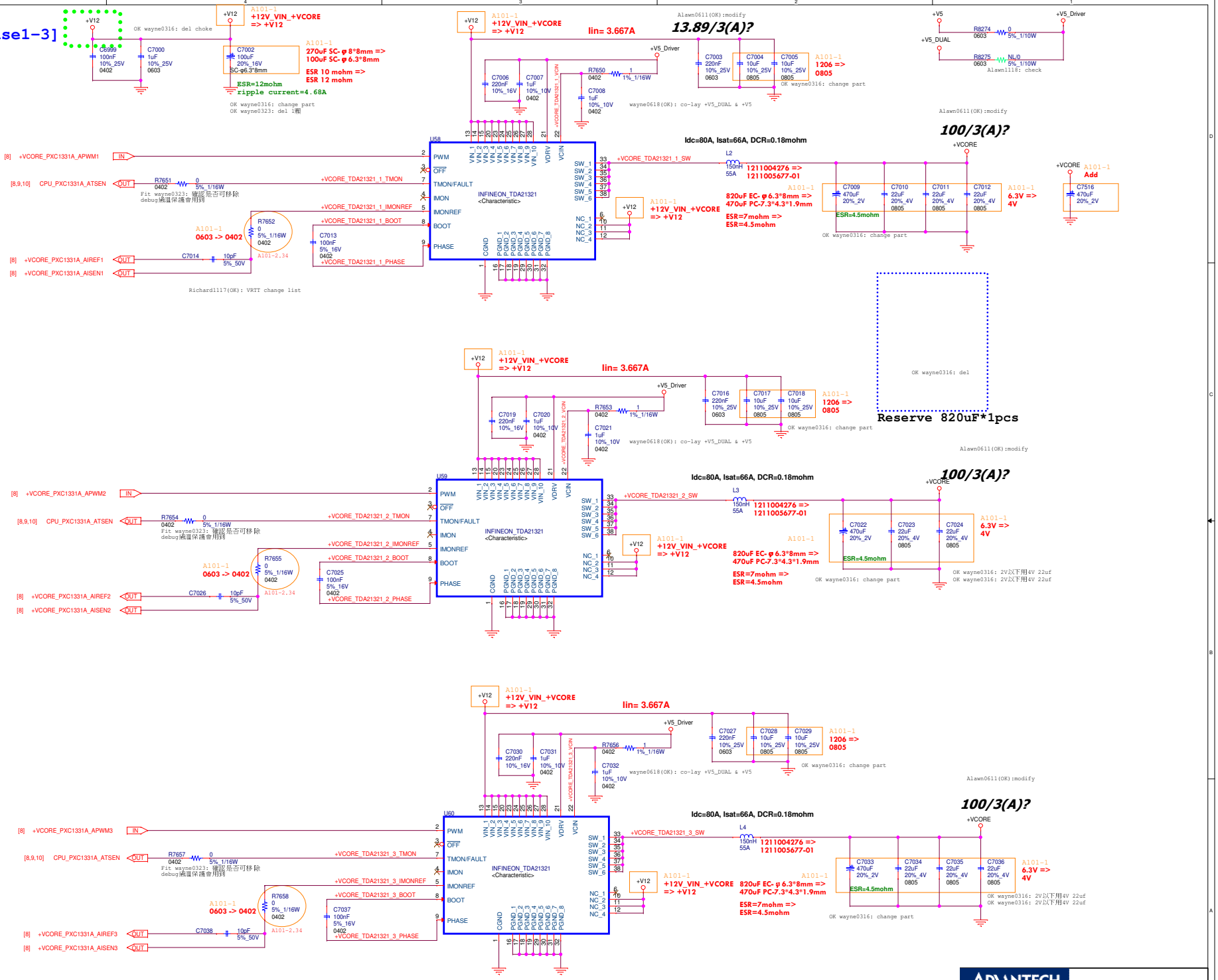
Resistor-to-GND (1%)		XADDR2							
		2.26 kΩ	2.67 kΩ	3.16 kΩ	4.02 kΩ	5.36 kΩ	8.06 kΩ	16.0 kΩ	Open
XADDR1	2.26 kΩ	FC	DC	BC	9C	7C	5C	3C	1C
	2.67 kΩ	F8	D8	B8	98	78	58	38	reserved
	3.16 kΩ	F4	D4	B4	94	74	54	34	14
	4.02 kΩ	F0	D0	B0	90	70	50	30	10
	5.36 kΩ	EC	CC	AC	8C	6C	4C	2C	0C
	8.06 kΩ	E8	C8	A8	88	68	48	28	08
	16.0 kΩ	E4	C4	A4	84	64	44	24	04
	Open	E0	C0	A0	80	60	40	20	reserved

Richard0518(OK):目前有空間，建議加回pin header，不然繞線很麻煩，2.54mm follow PCE-5129

Title	PWR CPU_Controller
Size	Document Number: PCE-3029/PCE-4129
Rev	A101-2
Date:	Monday, December 07, 2015
Sheet	8 of 55

PWR [VCORE_Phase1-3]

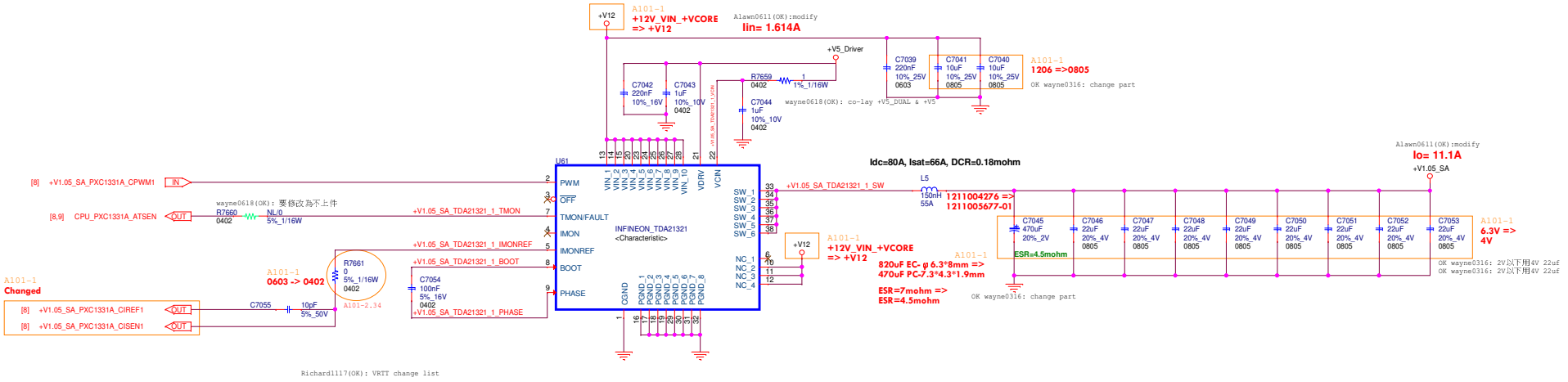
+VCORE Iomax=79A



Title	PWR +VCORE_Phase1-3	
Size	Document Number: PCE-3029/PCE-4129	Rev: A101-2
Date: Monday, December 07, 2015	Sheet 9 of 55	

PWR [VSA_Phase1]

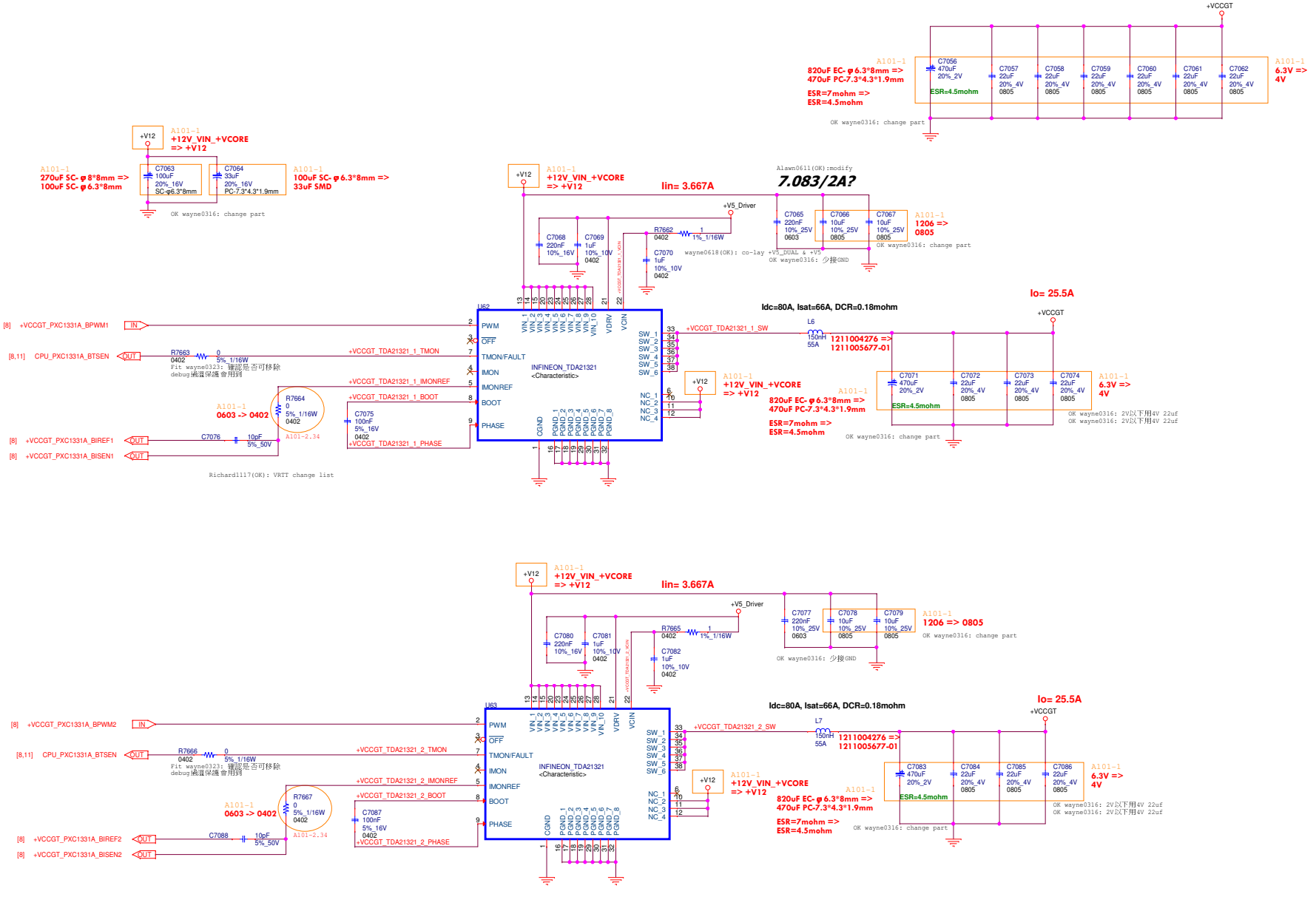
+V1.05_SA Iomax=12.3A



Title	PWR +V1.05_SA		
Size	Document Number	PCE-3029/PCE-4129	Rev A101-2
Date:	Monday, December 07, 2015	Sheet 10 of 55	

PWR [+VCCGT_Phase1-2]

+VCCGT Iomax=51A

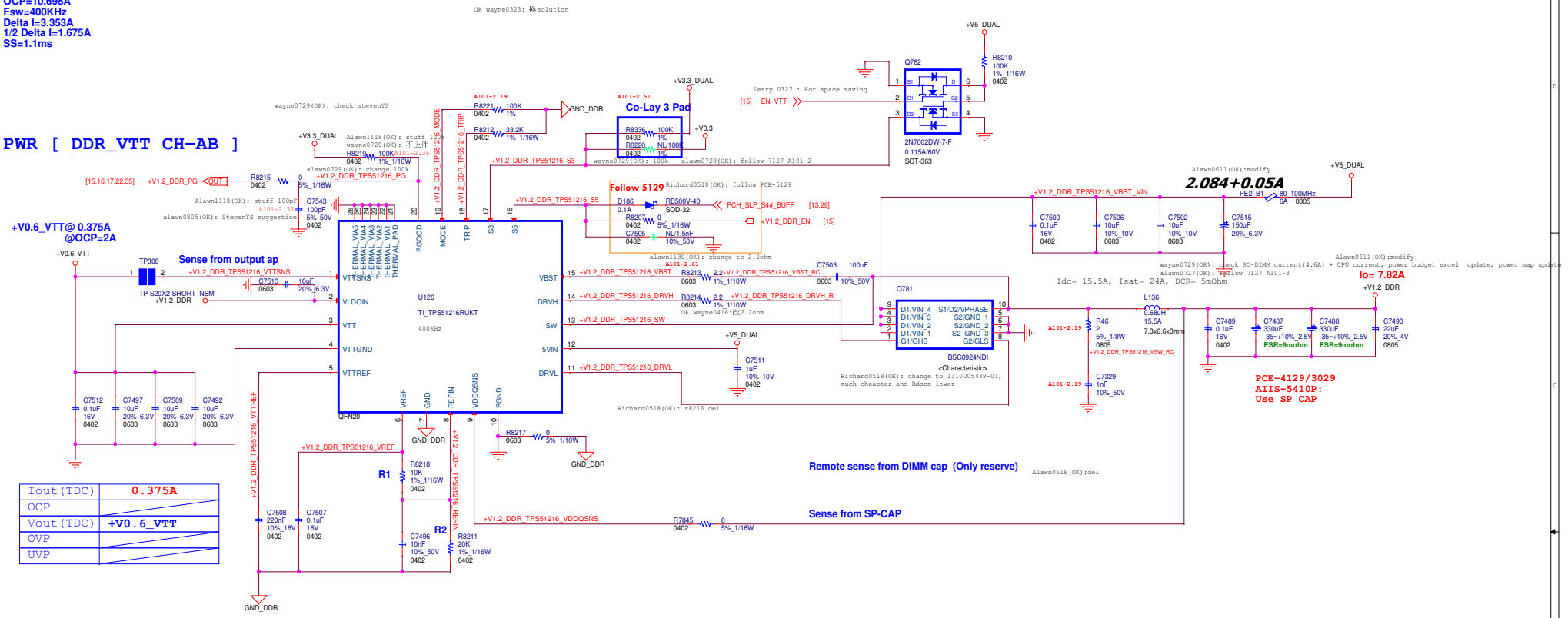


ADVANTECH			
Title	PWR +VCCGT_Phase1-2		
Size	Document Number	PCE-3029/PCE-4129	Rev A101-2
Date:	Monday, December 07, 2015	Sheet 11 of 55	

PWR [+V1.2_DDR PWM IC]

Power rail: +V1.2_DDR
Iomax=8.19A
OCP=10.698A
Fsw=400KHz
Delta I=3.353A
1/2 Delta I=1.675A
SS=1.1ms

PWR [DDR_VTT CH-AB]



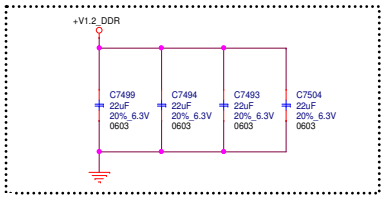
Rmode= 200k, Fs=400kHz
Rmode= 100k, Fs=300kHz

Vtrip(mV) = Rtrip(Kohm) x 10uA = 33.2Kx10uA = 332mV
Iocl = Vtrip /8 x Rdson + Iripple/2
= Vtrip / 8 x Rdson + (1/ (2 x L x f)) x ((Vin-Vout)xVout)/Vin
= 332mV / 8 x 4.6mohm + 1.676
~= 10.698A

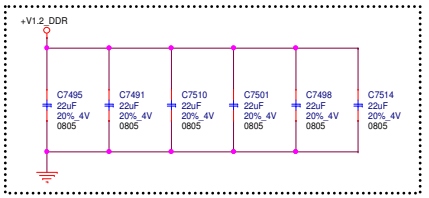
R2 = R1 / [(Vref / Vout) -1]
= 10K / [(1.8 / 1.2) - 1]
=20K

Table 2. MODE Selection

MODE NO.	RESISTANCE BETWEEN MODE AND GND (kΩ)	SWITCHING FREQUENCY (kHz)	DISCHARGE MODE
3	200	400	Tracking
2	100	300	
1	68	300	Non-tracking
0	47	400	



DIMM to CPU socket



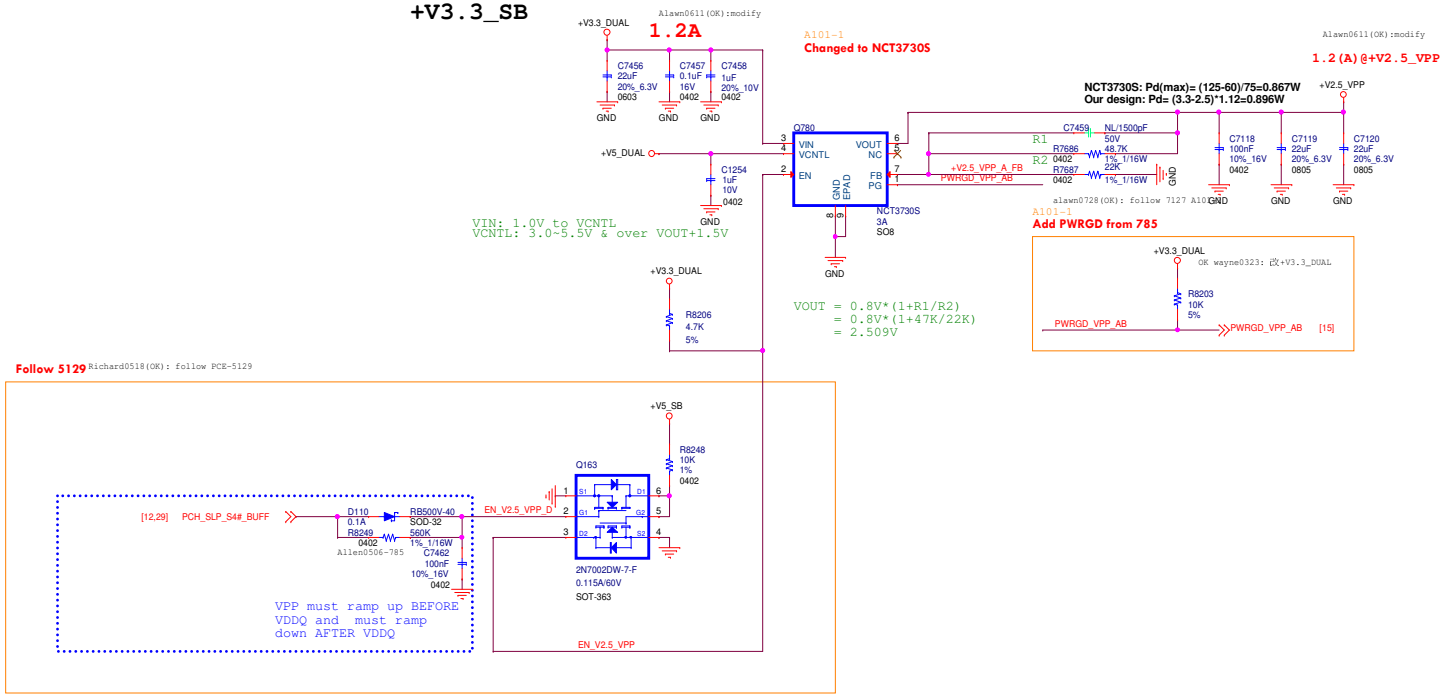
close to DIMM

ADVANTECH

Title	PWR +V1.2_DDR/VTT	
Size	Document Number PCE-3029/PCE-4129	Rev A101-2
Date: Monday, December 07, 2015	Sheet 12 of 55	

PWR [DDR_VPP CH-AB]

+V3.3_SB



Iout(TDC)	1.12A
OCP	
Vout(TDC)	+V2.5_VPP
OVP	
UVP	

A101-1
Del +V2.5_VPP_B

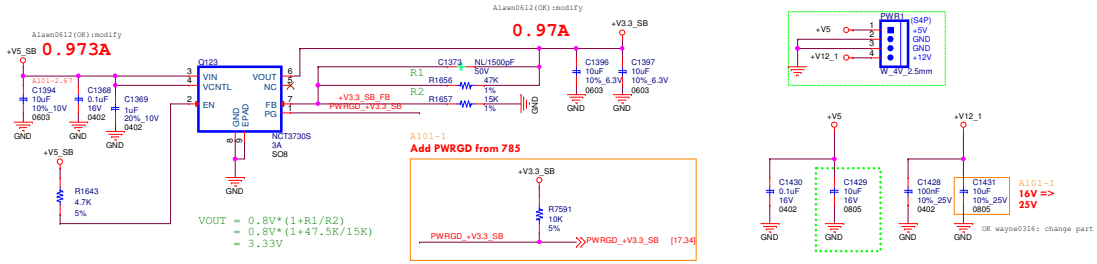
PWR [DDR_VTT CH-AB]

A101-1
Changed solution

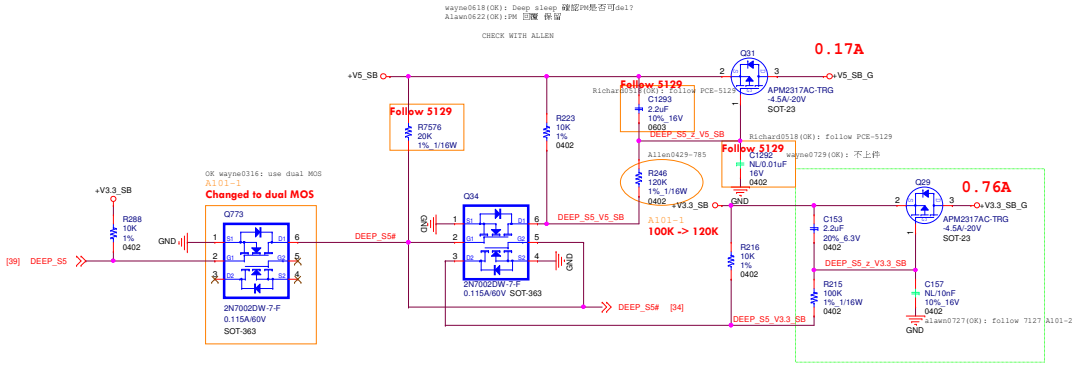
ADVANTECH			
Title	PWR VPP		
Size	Document Number	PCE-3029/PCE-4129	Rev A101-2
Date: Friday, December 04, 2015	Sheet 13 of 55		

+V3.3_SB

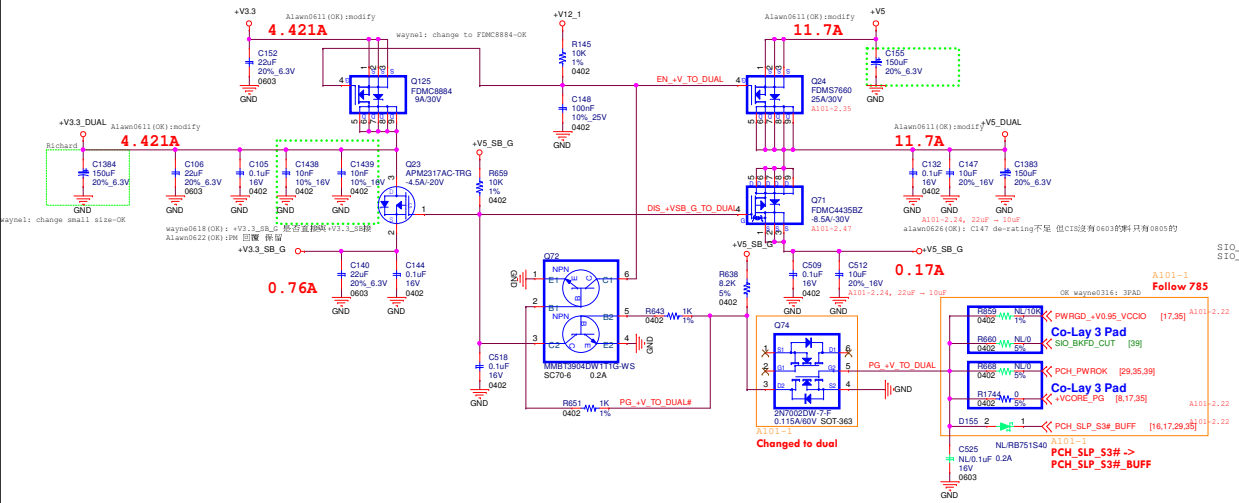
APL1084 change to NCT3730s



Deep Sleep Power Rail Switching



Dual Power Rail Switching



SIO_BKFD_CUT:When high,switches dual rails to standby power,In S3,S5
SIO_LATCHED_BKFD_CUT:When high,switches dual rails to standby power,In S3

ADVANTECH

Title	PWR +V3.3_SB/DEEP/DUAL POWER	
Size	Document Number PCE-3029/PCE-4129	Rev A101-2
Date: Monday, December 07, 2015	Sheet 14 of 55	

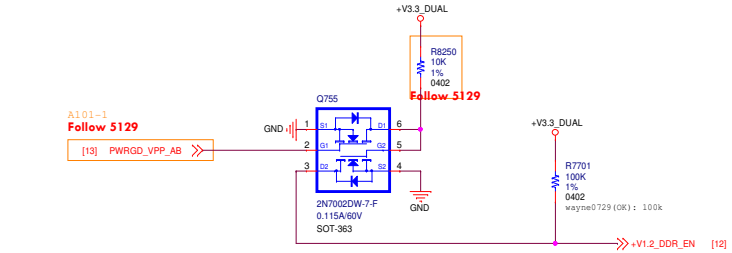
PWR DDR4 Power Sequence

VPP_EN

Richard0518(OK): del

PCH_SLP_S3#	PCH_SLP_S4#	EN_VR_R	EN_VPP
Low	Low	Low	Low
High	High	High	High
Low	High	Low	High

VDDQ_EN

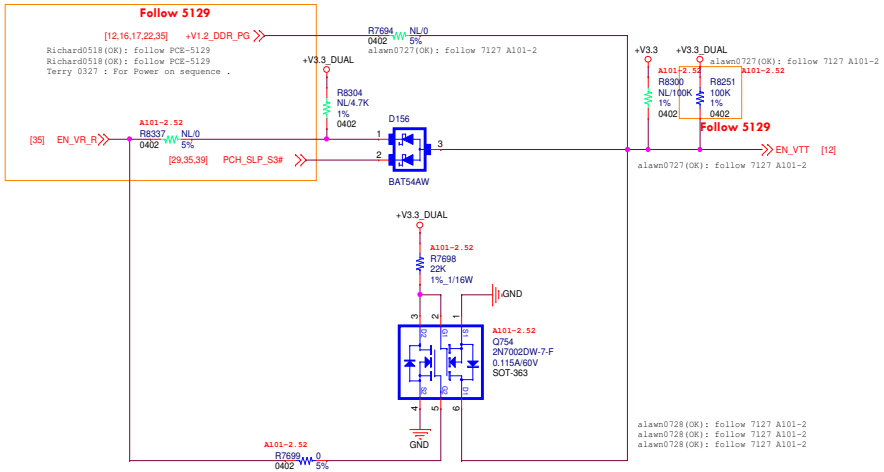


A101-1
Follow 5129

Terry 0327 : For can't enter S3 issue

Richard0518(OK): follow PCE-5129

VTT_EN



ADVANTECH

Title	PWR DDR4 Power Sequence	
Size	Document Number: PCE-3029/PCE-4129	Rev: A101-2
Date: Friday, December 04, 2015	Sheet 15 of 55	

PWR [CPU_VCCOPC / CPU_VCCEOPIO]

Table 7-7. VCC_{OPC} Voltage levels

ZVM# state	VCC_{OPC}	Units
0	0	V
1	1.0/1.05 (Based on SKU)	V

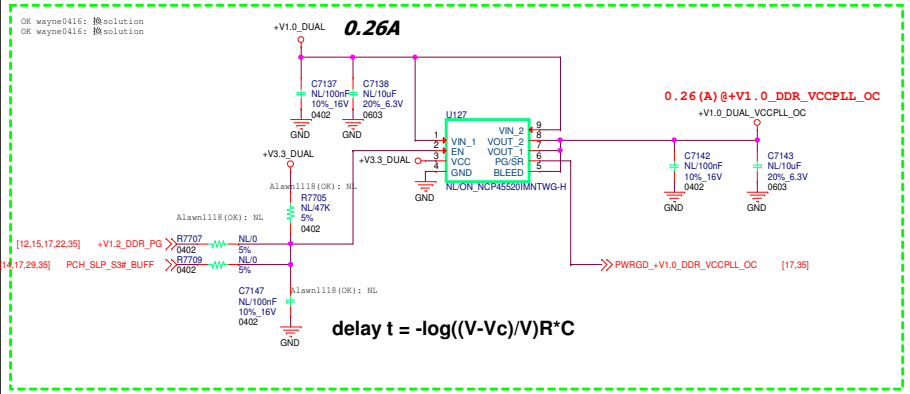
Table 7-9. VCC_{EOPIO} Voltage levels (separate VR)

ZVM# state	MSM# state	VCC_{EOPIO}	Units
0	X	0	V
1	0	0.8/0.85 (Based on SKU)	V
1	1	1.0/1.1 (Based on SKU)	V

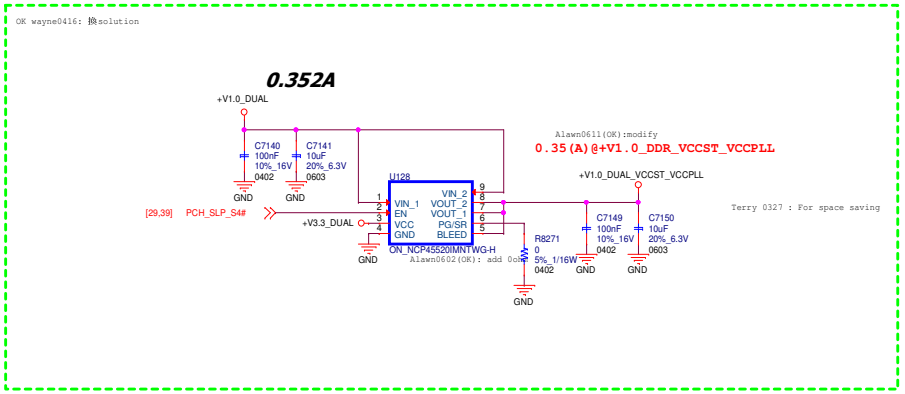
Notes:
1. S-processor line doesn't support MSM# signal.

PWR [CPU_VCCPLL_OC]

Alawn1118(OK): NL
A101-2.37



PWR [CPU_VCCST_VCCPLL]

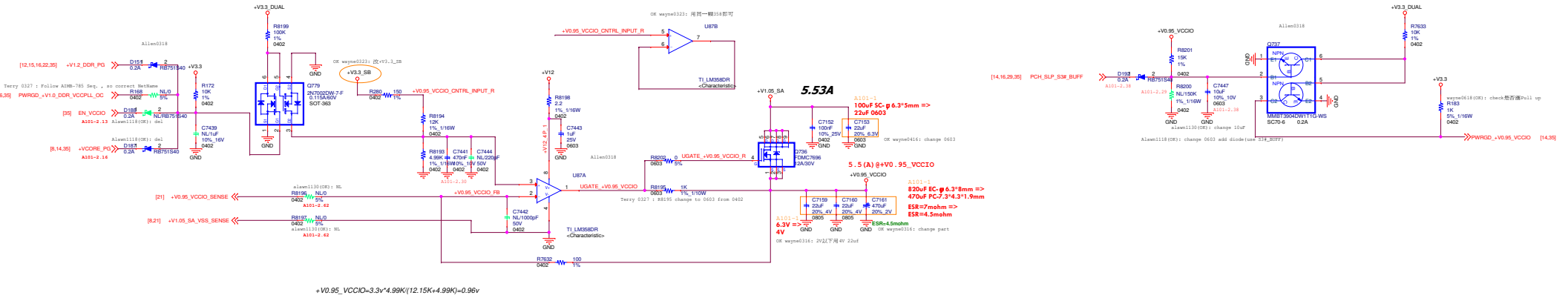


PWR [CPU_VCC_OPC_1P8]

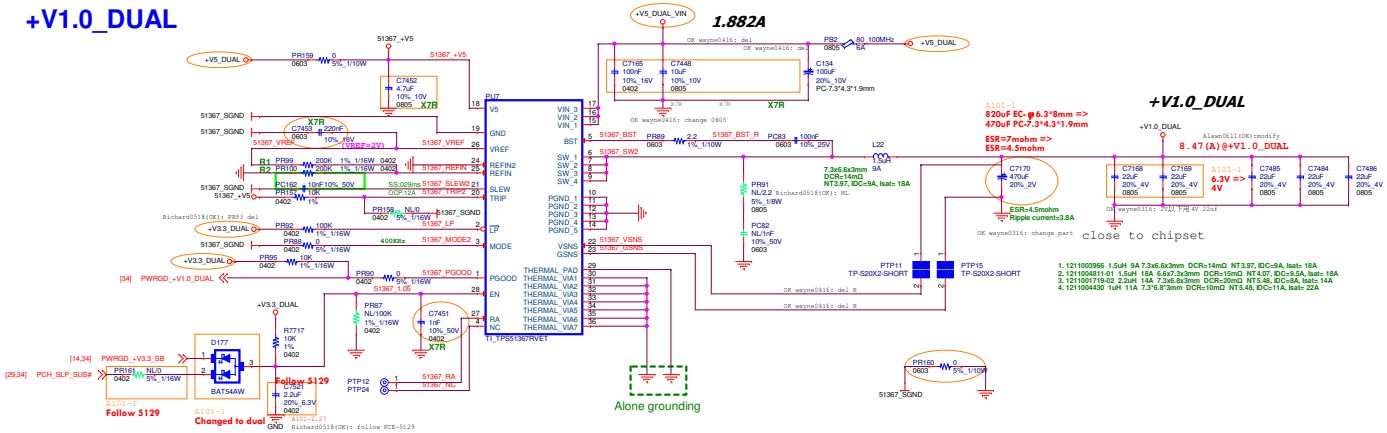
ADVANTECH

Title	PWR VCCOPC_EOPIO/VCCPLL_OC	
Size	Document Number: PCE-3029/PCE-4129	Rev: A101-2
Date: Friday, December 04, 2015	Sheet 16 of 55	

PWR [+V1.0_DUAL / +V0.95_VCCIO]



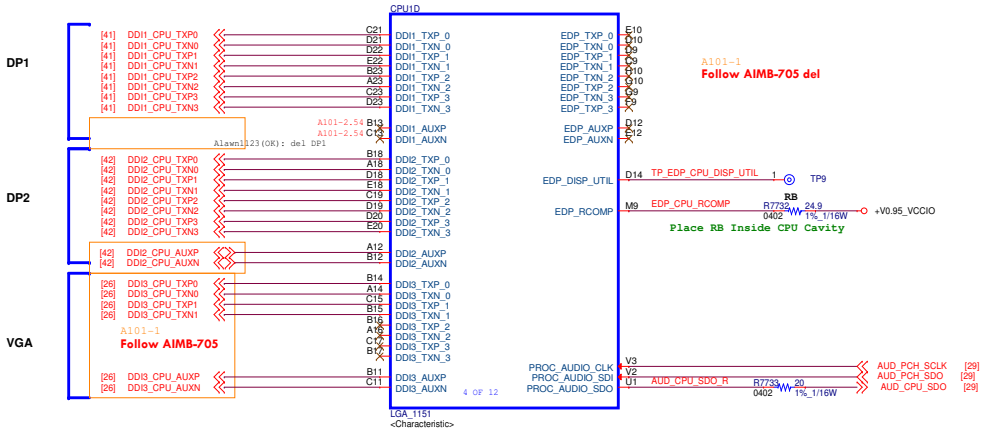
+V1.0_DUAL



Output Voltage use "TPS51367_2_3 Design Tool_0.53C.xls" to know R1 and R2

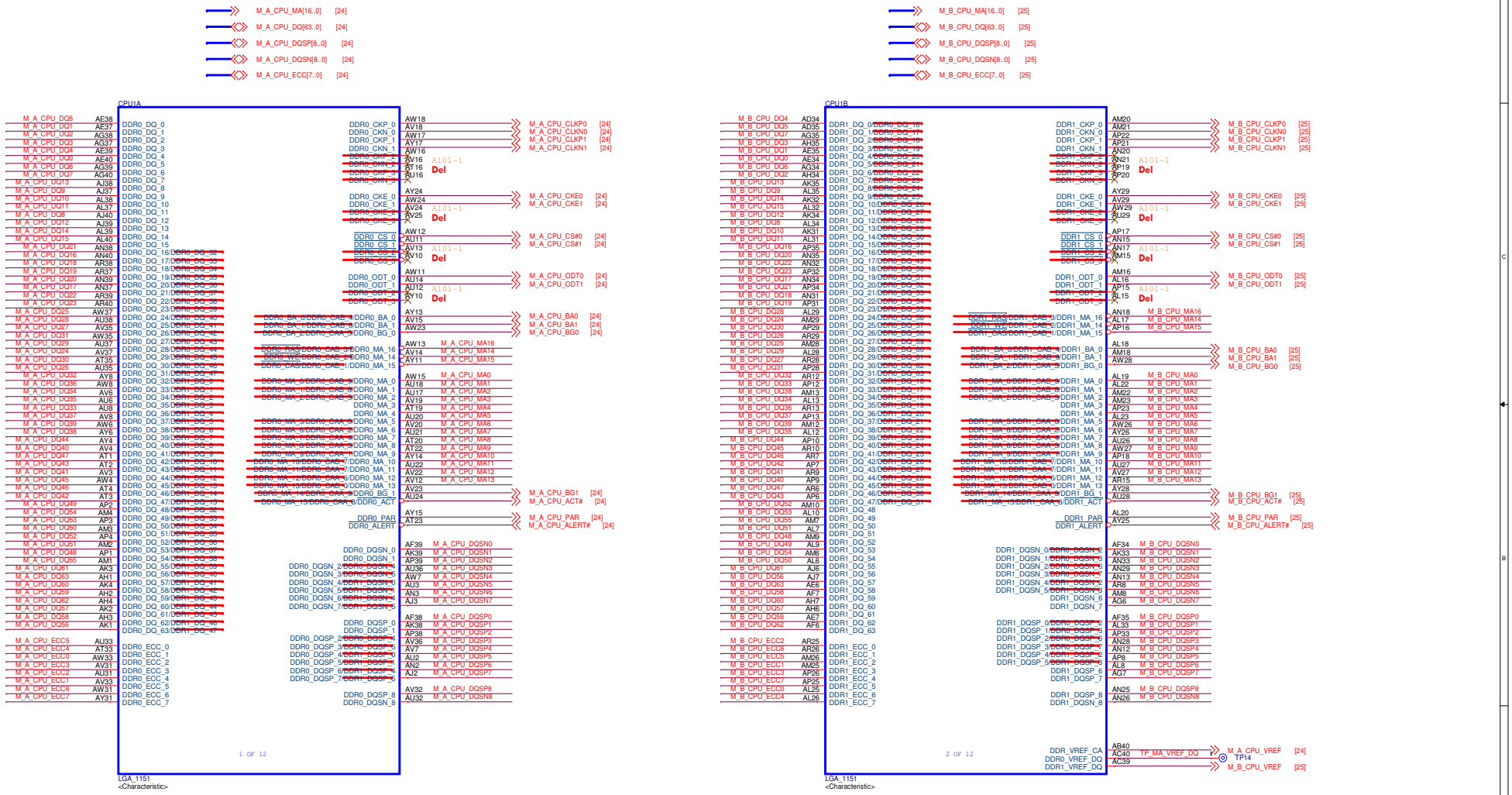
Title	PWR +V1.0_DUAL/+V0.95_VCCIO		
Size	Document Number		Rev
	PCE-3029		A101-2
Date:	Monday, December 07, 2015	Sheet	17 of 55

CPU Skylake – DT (PEG/DMI/DDI)



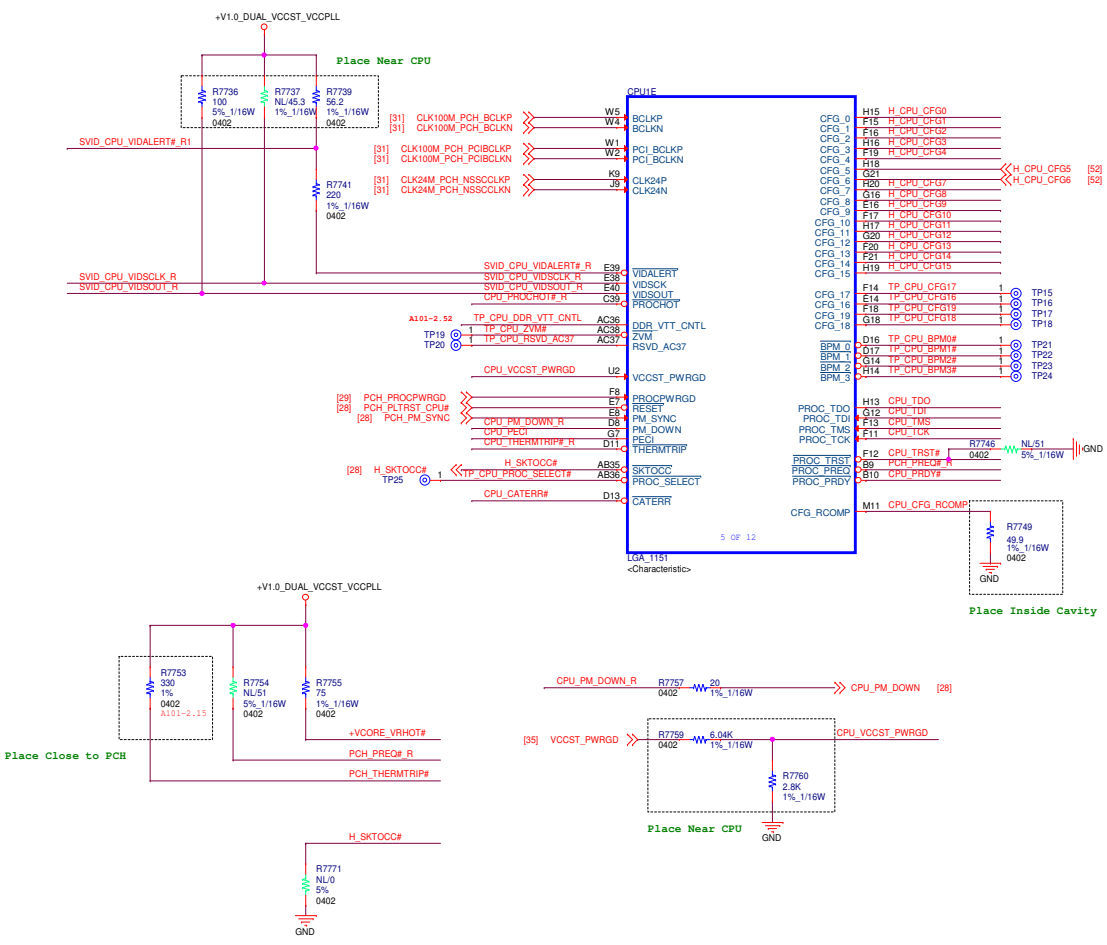
ADVANTECH			
Title	CPU PEG/DMI/DDI		
Size	Document Number	PCE-3029/PCE-4129	Rev A101-2
Date: Monday, December 07, 2015	Sheet 18 of 55		

CPU Skylake - DT (DDR4 MEMORY)

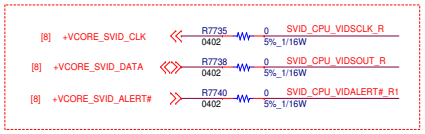


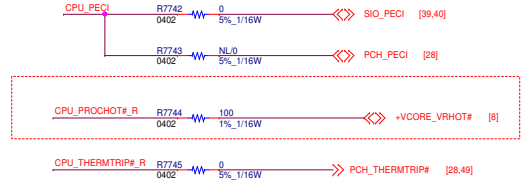
Title	CPU DDR4 MA/MB
Size	Document Number: PCE-3029/PCE-4129
Rev	A101-2
Date:	Monday, December 07, 2015
Sheet	19 of 55

CPU Skylake – DT (MISC/CFG)

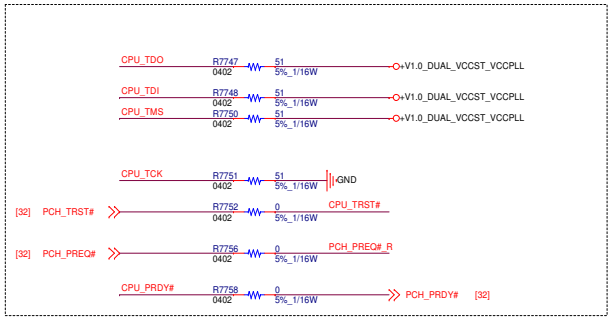


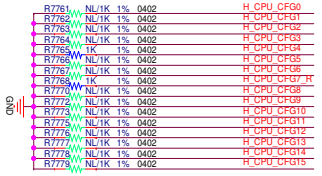
SVID Control





JTAG





A101-1
Del PCIEX16_CFG 0 ohm

For HASWELL Interposer , should
(1) Mount H_CPU_CFG9's PD resistor.
(2) Mount H_CPU_CFG13's PD resistor.

Error Signal

Configuration Signals:

CFG[0]: Stall reset sequence after PCU PLL lock until de-asserted:
– 1 = (Default) Normal Operation;No stall.
– 0 = Stall.

CFG[2]: PCI Express* Static x16 Lane Numbering Reversal.
– 1 = (Default) Normal operation
– 0 = Lane numbers reversed.

CFG[4]: eDP enable:
– 1 = Disabled.
– 0 = (Default) Enabled.

CFG[6:5]: PCI Express* Bifurcation
– 00 = 1 x8, 2 x4 PCI Express*
– 01 = reserved
– 10 = 2 x8 PCI Express*
– 11 = (Default) 1 x16 PCI Express*

CFG[7]: PEG Training:
– 1 = (default) PEG Train immediately following RESET# de assertion.
– 0 = PEG Wait for BIOS for training.

150206

A101-1
Del pin header

H_CPU_CFG7
H_CPU_CFG7_R
R7780 NL/0 0402 5%

wayne0226(OK): add 0ohm for remove JCFG1

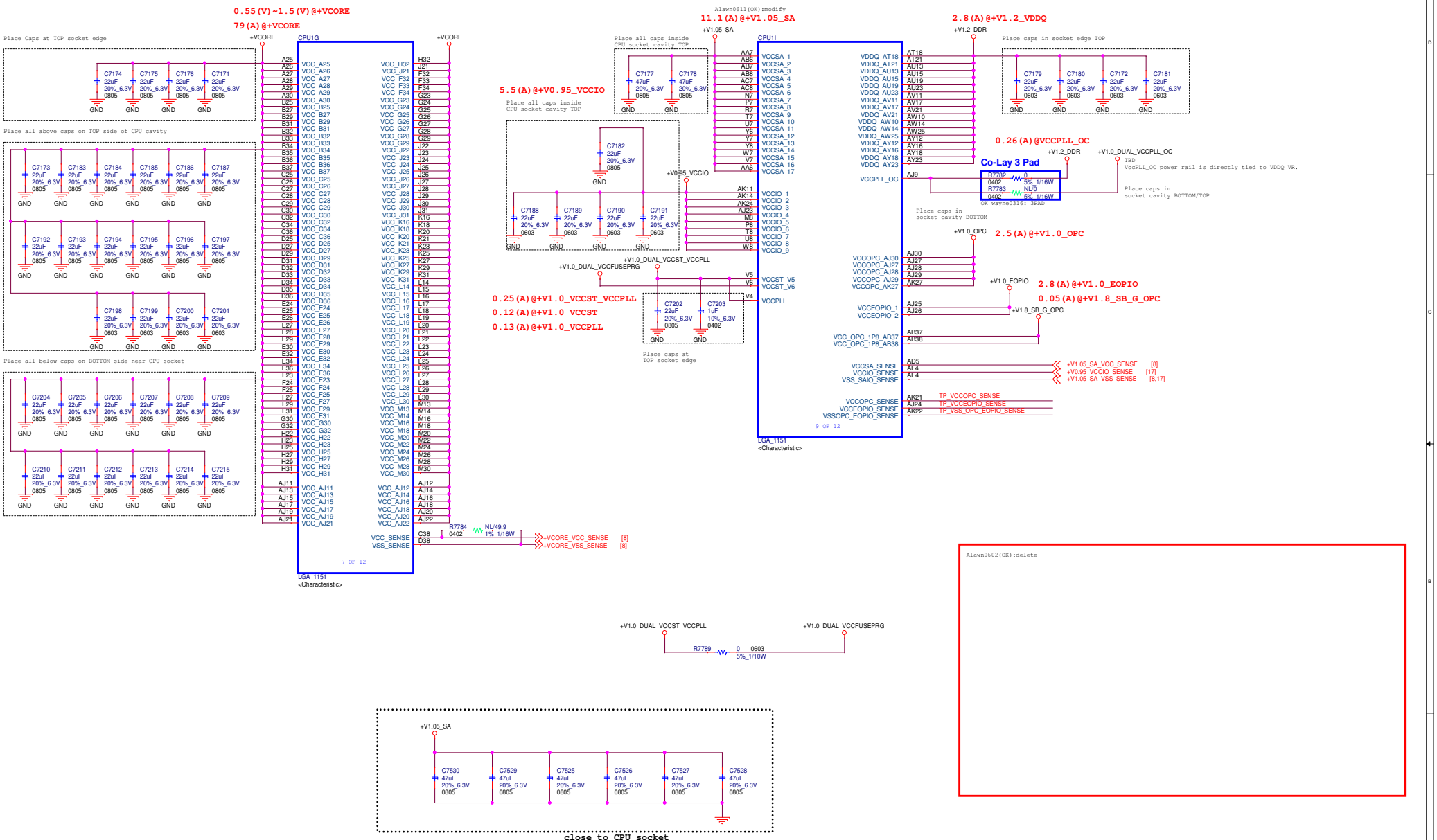
OK wayne0416: del PH, 留電阻即可

Mode	Jumper Setting
PEG Train immediately following RESET# de assertion.	1-2 Short (Default)
PEG Wait for BIOS for training.	2-3 Short

ADVANTECH

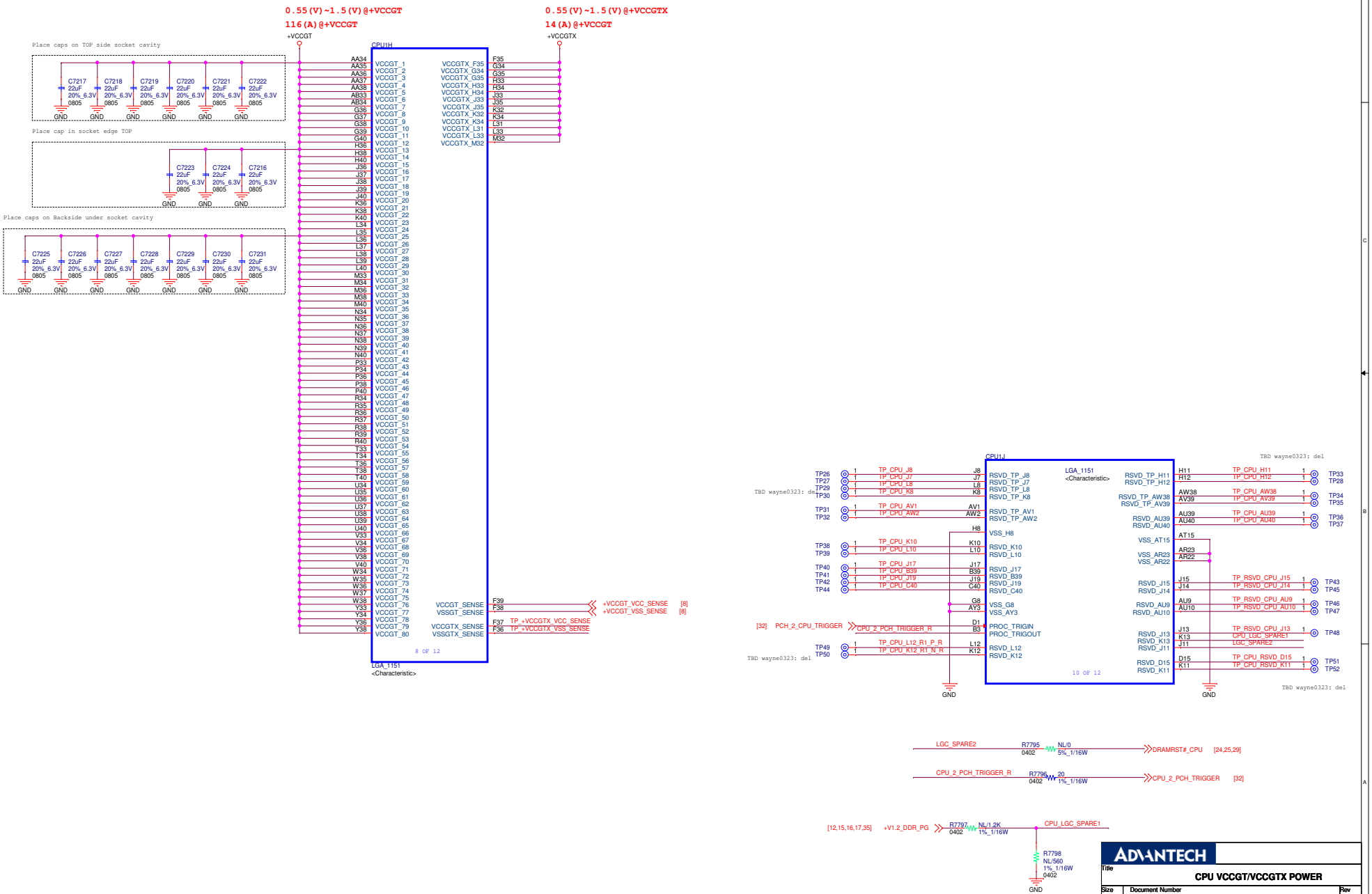
Title	CPU MISC/CFG	
Size	Document Number PCE-3029/PCE-4129	Rev A101-2
Date: Monday, December 07, 2015	Sheet 20 of 55	

CPU Skylake – DT (VCORE/VCCSA POWER)



Title	CPU VCORE/VCCSA POWER
Size	Document Number: PCE-3029/PCE-4129
Rev	A101-2
Date:	Monday, December 07, 2015
Sheet	21 of 55

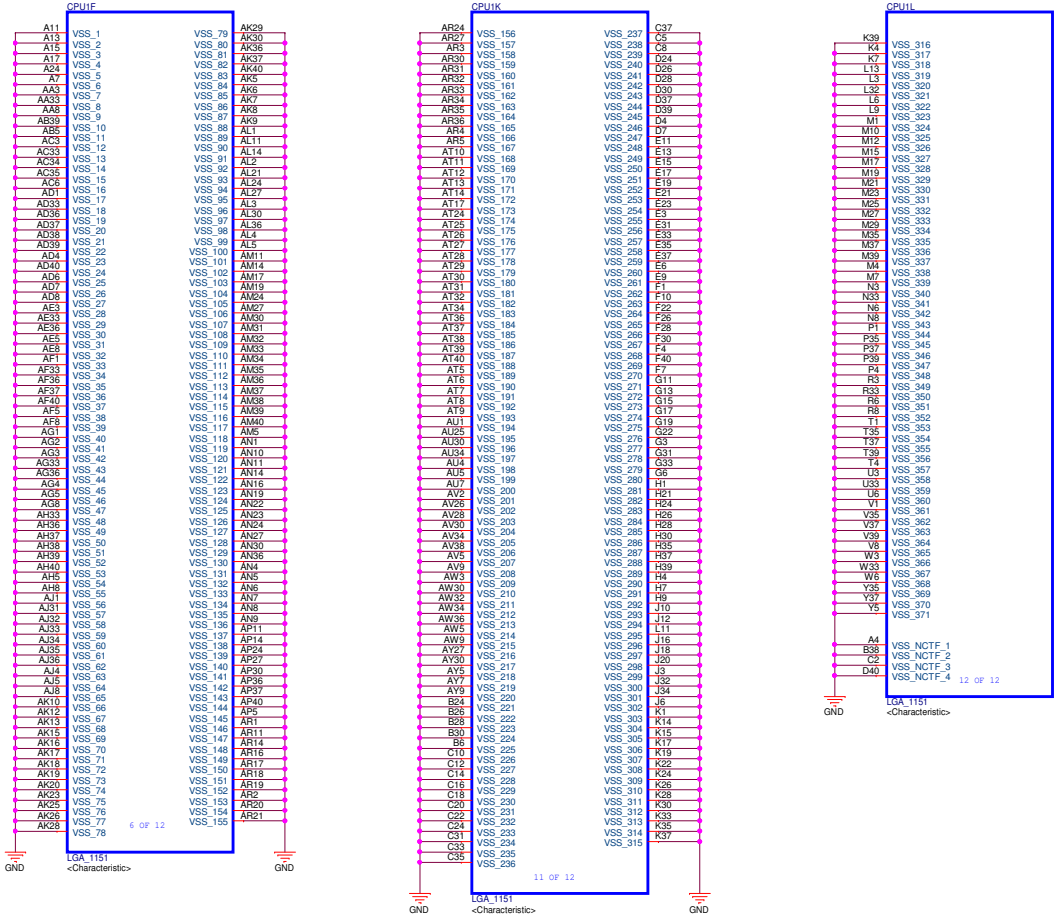
CPU Skylake – DT (VCCGT/VCCGTX POWER)



ADVANTECH

Title	CPU VCCGT/VCCGTX POWER	
Size	Document Number: PCE-3029/PCE-4129	Rev: A101-2
Date: Monday, December 07, 2015	Sheet 22 of 55	

CPU Skylake – DT (GND)

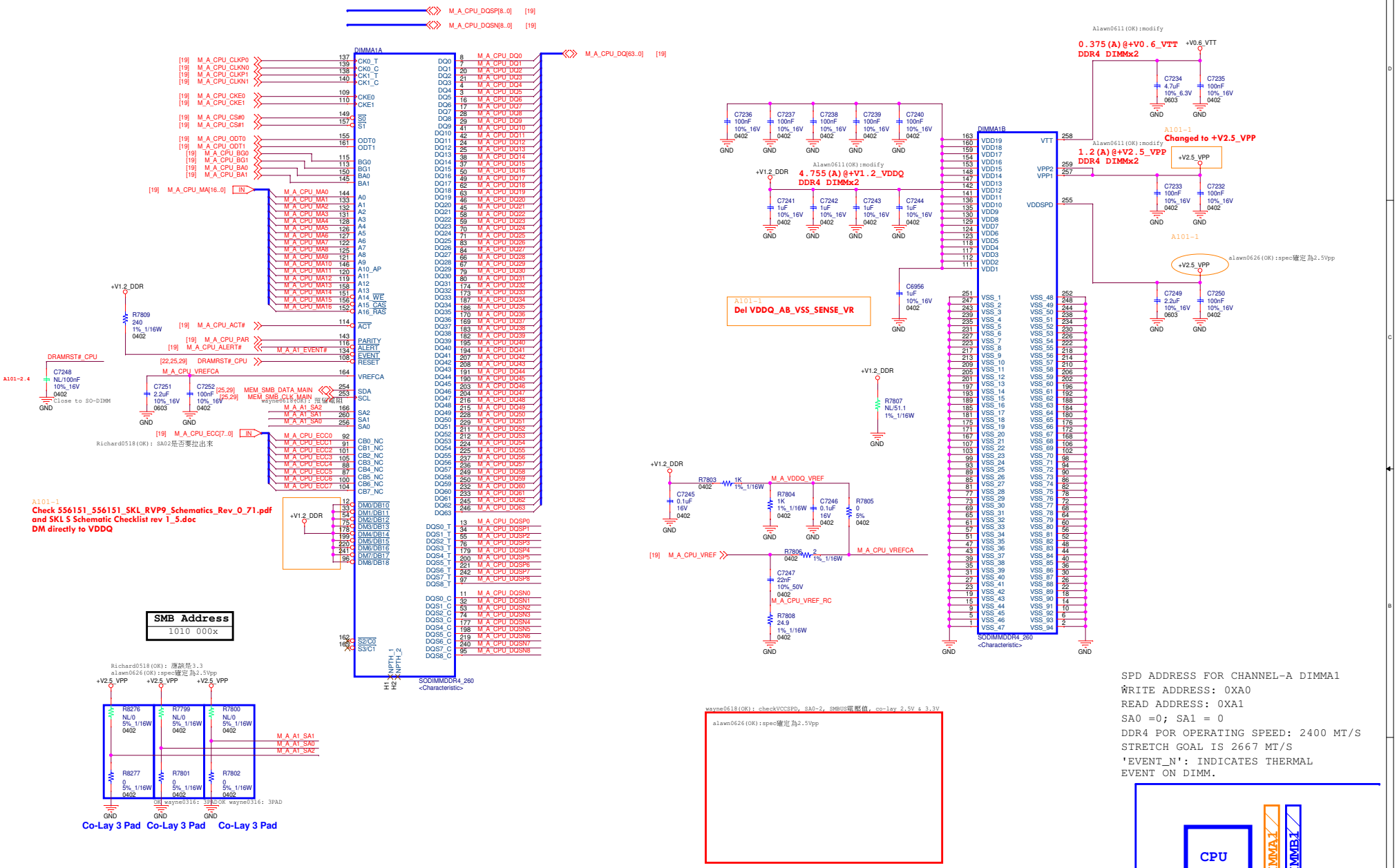


ADVANTECH

Title	CPU GND	
Size	Document Number PCE-3029/PCE-4129	Rev A101-2
Date: Monday, December 07, 2015	Sheet 23 of 55	

DDR4 SKT [CH-A1] / DIP TYPE

Attend : 1651002910-01



SPD ADDRESS FOR CHANNEL-A DIMMA1
WRITE ADDRESS: 0XA0
READ ADDRESS: 0XA1
SA0 =0; SA1 = 0
DDR4 POR OPERATING SPEED: 2400 MT/S
STRETCH GOAL IS 2667 MT/S
'EVENT_N': INDICATES THERMAL EVENT ON DIMM.

CPU

DIMMA1

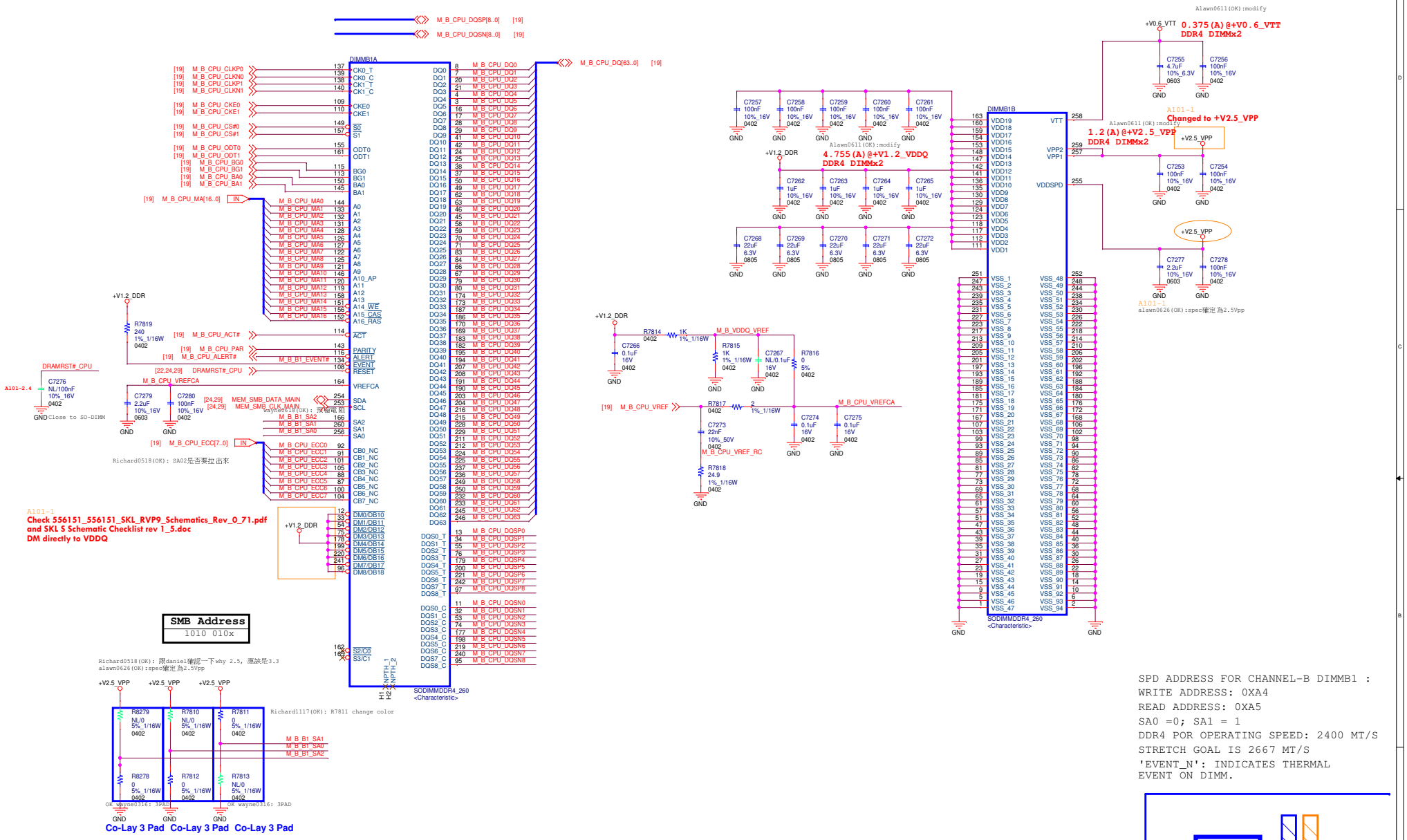
DIMMB1

ADVANTECH

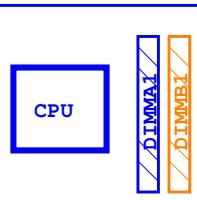
Title	DDR4 SKT CH-A1	
Size	Document Number PCE-3029/PCE-4129	Rev A101-2
Date: Monday, December 07, 2015	Sheet 24 of 55	

DDR4 SKT [CH-B1] / DIP TYPE

Attend : 1651002910-01



SPD ADDRESS FOR CHANNEL-B DIMMB1 :
WRITE ADDRESS: 0XA4
READ ADDRESS: 0XA5
SA0 =0; SA1 = 1
DDR4 POR OPERATING SPEED: 2400 MT/S
STRETCH GOAL IS 2667 MT/S
'EVENT_N': INDICATES THERMAL
EVENT ON DIMM.



Title	DDR4 SKT CH-B1	
Size	Document Number PCE-3029/PCE-4129	Rev A101-2
Date: Monday, December 07, 2015	Sheet 25 of 55	

VGA

A101-1
Follow 5129

Alawn0611(OK):modify
+V3.3_VGA @ 78mA

Place 100 nF capacitor as close as possible to pin 38 and pin 40 without vias at same side as PTN3355

TESTMODE open: I2C address = C0h

Mount LC for buck mode: active 210mW, standby 0.4mW
Unmount LC for LDO mode: active 400mW, standby 40mW

Pin 36 Pin 35

pin 1 pin 5

CFG3 open: not used

DOCK_IN=0: VGA active output is ch#1

CFG 1/2=10

CFG5 open: 27 MHz XTAL is used

Table 8. CFG1_SCL/CFG2_SDA pin definitions

Pin value	System behavior
00	Compliant HPD behavior
01	Most interoperable (non-compliant) HPD behavior
10	Most interoperable (non-compliant) HPD behavior
11	(Default) Compliant behavior (but configurable via I²C-bus)

A101-1
Follow AIMB-705

A101-2.5

A101-1
Follow 5129 del SDA/SCL level shifter

A101-1
Follow 4128

0.055A

alawn0630(OK):VGA座負載

Z=37.5ohm
Z=75ohm for long distance
Z=50ohm for short distance

Title	CONN VGA
Size	Document Number: PCE-3029/PCE-4129
Rev	A101-2
Date:	Monday, December 07, 2015
Sheet	26 of 55

ADVANTECH

PCH SKL PCH-H (DMI/PCIE/USB/LPC)

OK wayne0316: USB 使用DUAL 電源，可不須要buffer

A101-1
Del USB_OC_CTRL

OK wayne0316: USB 使用DUAL 電源，可不須要buffer

A101-1
Del USB_OC buffer

A101-1
Del OC buffer

PCH1B

SKL_PCH_H

DMI_RXN0 L27
DMI_RXP0 N27
DMI_TXN0 C27
DMI_TXP0 B27
DMI_RXN1 E24
DMI_RXP1 G24
DMI_TXN1 B28
DMI_TXP1 A28
DMI_RXN2 G27
DMI_RXP2 E26
DMI_TXN2 B29
DMI_TXP2 C29
DMI_RXN3 L29
DMI_RXP3 K29
DMI_TXN3 B30
DMI_TXP3 A30

[18] DMI_CPU_TXN0
[18] DMI_CPU_TXP0
[18] DMI_CPU_RXN0
[18] DMI_CPU_RXP0
[18] DMI_CPU_TXN1
[18] DMI_CPU_TXP1
[18] DMI_CPU_RXN1
[18] DMI_CPU_RXP1
[18] DMI_CPU_TXN2
[18] DMI_CPU_TXP2
[18] DMI_CPU_RXN2
[18] DMI_CPU_RXP2
[18] DMI_CPU_TXN3
[18] DMI_CPU_TXP3
[18] DMI_CPU_RXN3
[18] DMI_CPU_RXP3

DMI

USB 2.0

R7843 0402 100 1%_1/16W
PCIE_PCH_RCOMPN B18
PCIE_PCH_RCOMPP C17
Length Matching:<1mil

PCIE_RCOMPN
PCIE_RCOMPP

A101-1 Del
PCIE1_RXN/USB3_7_RXN G19
PCIE1_RXP/USB3_7_RXP A19
PCIE1_TXN/USB3_7_TXN B19
PCIE1_TXP/USB3_7_TXP B18
A101-1 Del
PCIE2_TXN/USB3_8_TXN C19
PCIE2_TXP/USB3_8_TXP E19
PCIE2_RXN/USB3_8_RXN G19
PCIE2_RXP/USB3_8_RXP L19
A101-1 Del
PCIE3_RXN/USB3_9_RXN K19
PCIE3_RXP/USB3_9_RXP B20
PCIE3_TXN/USB3_9_TXN C20
PCIE3_TXP/USB3_9_TXP E20

LAN1 (PHY, I219)

PCIE4_RXN/USB3_10_RXN G19
PCIE4_RXP/USB3_10_RXP B21
PCIE4_TXN/USB3_10_TXN A21
PCIE4_TXP/USB3_10_TXP K19

[37] PCIE_PCH_RXN4
[37] PCIE_PCH_RXP4
[37] PCIE_PCH_TXN4
[37] PCIE_PCH_TXP4

PICMG 1.3 x4

PCIE5_RXN L19
PCIE5_RXP D22
PCIE5_TXN C22
PCIE5_TXP G22
PCIE6_RXN E22
PCIE6_RXP B22
PCIE6_TXN A23
PCIE6_TXP L22
PCIE7_RXN C23
PCIE7_RXP B23
PCIE7_TXN K24
PCIE7_TXP L24
PCIE8_RXN C24
PCIE8_RXP B24
PCIE8_TXN
PCIE8_TXP

[52] PCIE_PCH_RXN5
[52] PCIE_PCH_RXP5
[52] PCIE_PCH_TXN5
[52] PCIE_PCH_TXP5
[52] PCIE_PCH_RXN6
[52] PCIE_PCH_RXP6
[52] PCIE_PCH_TXN6
[52] PCIE_PCH_TXP6
[52] PCIE_PCH_RXN7
[52] PCIE_PCH_RXP7
[52] PCIE_PCH_TXN7
[52] PCIE_PCH_TXP7
[52] PCIE_PCH_RXN8
[52] PCIE_PCH_RXP8
[52] PCIE_PCH_TXN8
[52] PCIE_PCH_TXP8

2 of 12

INTEL_SKYLAKE-Q170
<Characteristic>

USB2N_1 AF5
USB2P_1 AG7
USB2N_2 AD5
USB2P_2 AD7
USB2N_3 AG8
USB2P_3 AG10
USB2N_4 AE1
USB2P_4 AE2
USB2N_5 AC2
USB2P_5 AC3
USB2N_6 AF2
USB2P_6 AF3
USB2N_7 AB3
USB2P_7 AB2
USB2N_8 AL8
USB2P_8 AL7
USB2N_9 AA1
USB2P_9 AA2
USB2N_10 AJ8
USB2P_10 AJ7
USB2N_11 W2
USB2P_11 W3
USB2N_12 AD3
USB2P_12 AD2
USB2N_13 Y2
USB2P_13 Y1
USB2N_14 AU11
USB2P_14 AU13

USB2_PCH_DN1 [46]
USB2_PCH_DP1 [46]
USB2_PCH_DN2 [46]
USB2_PCH_DP2 [46]
USB2_PCH_DN3 [46]
USB2_PCH_DP3 [46]
USB2_PCH_DN4 [47]
USB2_PCH_DP4 [47]
USB2_PCH_DN5 [47]
USB2_PCH_DP5 [47]
USB2_PCH_DN6 [47]
USB2_PCH_DP6 [47]
USB2_PCH_DN7 [47]
USB2_PCH_DP7 [47]
USB2_PCH_DN8 [47]
USB2_PCH_DP8 [47]
USB2_PCH_DN9 [47]
USB2_PCH_DP9 [47]
USB2_PCH_DN10 [46,47]
USB2_PCH_DP10 [46,47]
USB2_PCH_DN11 [43]
USB2_PCH_DP11 [43]

USB1 (Rear) (USB3.0)
USB23 (Box Header) (USB3.0)
USB45 (Pin Header)
USB67 (Pin Header)
USB89 (Pin Header)
USB11 (Type A)
PCE-4129(C236) for Mini-PCIe

A101-1 Del

A101-1 Del

GPP_E9/USB2_OC0 AD43
GPP_E10/USB2_OC1 AD42
GPP_E11/USB2_OC2 AD39
GPP_E12/USB2_OC3 AC44
GPP_F15/USB2_OC4 Y43
GPP_F16/USB2_OC5 Y41
GPP_F17/USB2_OC6 W44
GPP_F18/USB2_OC7 W43

USB_OC#12 [46]
USB_OC#34 [47]
USB_OC#56 [47]
USB_OC#3
USB_OC#4
USB_OC#5
USB_OC#6
USB_OC#7

A101-1
USB_OC#5611
=> USB_OC#56

A101-1
Add

+V3.3_DUAL

USB_OC#3 R8158 0402 10K 1%
USB_OC#4 R8159 0402 10K 1%
USB_OC#5 R8161 0402 10K 1%
USB_OC#6 R8068 0402 10K 5%_1/16W
USB_OC#7 R8285 0402 10K 5%_1/16W

A101-1
PCH_USB2_OC#6
=> DVI2_OC#
MINIPCIE1_DIS# =>
GPIO_PCH_PCIESLOT_RST_R

Richard0518(OK): 這張根不要用這裡的GPIO
Richard0518(OK): 這張根不要用這裡的GPIO

USB2_COMP AG3
USB2_VBUSSENSE AD10
RSVD_AB13 AB13
USB2_ID AG2
GPD7/RSVD BD14

PCH_USB2_RBIAS
PCH_USB2_VBUSSENSE
PCH_USB2_ID

R7848 0402 113 1%_1/16W
GND

A101-1
Del ATX_AT#_SEL for BIOS

GPIO for BIOS Control

R7851 1K 1%_1/16W GND
R7852 1K 1%_1/16W GND

PCH1F

SKL_PCH_H

USB3_1_TXN C11
USB3_1_TXP B11
USB3_1_RXN B7
USB3_1_RXP A7
USB3_2_TXN/SSIC_1_TXN B12
USB3_2_TXP/SSIC_1_TXP A12
USB3_2_RXN/SSIC_1_RXN C8
USB3_2_RXP/SSIC_1_RXP B8
USB3_6_TXN B15
USB3_6_TXP C15
USB3_6_RXN K15
USB3_6_RXP K14
USB3_5_TXN B14
USB3_5_TXP C14
USB3_5_RXN G14
USB3_5_RXP H14
USB3_3_TXP/SSIC_2_TXP D13
USB3_3_TXN/SSIC_2_TXN C13
USB3_3_RXP/SSIC_2_RXP A9
USB3_3_RXN/SSIC_2_RXN B10
USB3_4_TXP B13
USB3_4_TXN A13
USB3_4_RXP G13
USB3_4_RXN E13

USB3 (Rear) (USB3.0)
USB12 (Box header) (USB3.0)
USB12 (Box header) (USB3.0)

[46] USB3_PCH_TXN1
[46] USB3_PCH_TXP1
[46] USB3_PCH_RXN1
[46] USB3_PCH_RXP1
[46] USB3_PCH_TXN2
[46] USB3_PCH_TXP2
[46] USB3_PCH_RXN2
[46] USB3_PCH_RXP2
[46] USB3_PCH_TXP3
[46] USB3_PCH_TXN3
[46] USB3_PCH_RXP3
[46] USB3_PCH_RXN3

A101-1 Del
A101-1 Del

USB

SATA

6 of 12

INTEL_SKYLAKE-Q170
<Characteristic>

GPP_A1/LAD0/ESPI_IO0 AT22
GPP_A2/LAD1/ESPI_IO1 AV22
GPP_A3/LAD2/ESPI_IO2 AT19
GPP_A4/LAD3/ESPI_IO3 BD16
GPP_A5/LFRAME/ESPI_CS0 BE16
GPP_A6/SERIRQ/ESPI_CS1 BA17
GPP_A7/PIRQA/ESPI_ALERT0 AW17
GPP_A0/RCIN/ESPI_ALERT1 AT17
GPP_A14/SUS_STAT/ESPI_RESET BC18

LPC_AD0 [39,51]
LPC_AD1 [39,51]
LPC_AD2 [39,51]
LPC_AD3 [39,51]
LPC_FRAME# [39,51]

A101-1
Follow 4128

+V3.3_DUAL
R7856 10K 1% 0402

PCH_SERIRQ [39,51]
PCH_PIRQA#
TP_PCH_LPCPD#
KBRST# [39]
TP53

A101-1
SIO_KBRST#
=> KBRST#

GPP_A9/CLKOUT_LPC0/ESPI_CLK BC17
GPP_A10/CLKOUT_LPC1 AV19

CLK24M_PCH_LPC0_R
CLK24M_PCH_LPC1_R
R7859 22 1% 1/16W 0402
CLK24M_PCH_LPC1 [51]

GPP_G19/SMI M45
GPP_G18/NMI N43

PCH_SMI#
PCH_GPP_G18

GPP_E6/DEVSLP2 AE45
GPP_E5/DEVSLP1 AG43
GPP_E4/DEVSLP0 AG42
GPP_F9/DEVSLP7 AB39
GPP_F8/DEVSLP6 AB36
GPP_F7/DEVSLP5 AB43
GPP_F6/DEVSLP4 AB42
GPP_F5/DEVSLP3 AB41

TP_PCH_VISA2CH1_D5
TP_PCH_VISA2CH1_D4
TP_PCH_VISA2CH1_D3
TP_PCH_GPP_F9
TP_PCH_GPP_F8
TP_PCH_GPP_F7
TP_PCH_GPP_F6
AUD_FP_PRESENCE#_R

TP54
TP55
TP56
TP57
TP58
TP59
TP60

A101-1
Del AUD_FP_PRESENCE#

A101-1
Del clock buffer

CLK24M_PCH_LPC0_R
R7861 22 1% 1/16W 0402 CLK24M_PCH_LPC0_PCICLK [39]
R7862 22 1% 1/16W 0402 CLK24M_PCH_LPC0_IOCLK [39]

+V3.3

PCH_SERIRQ R7865 0402 10K 1%
KBRST# R7866 0402 10K 1%

PCH_SMI#
Co-Lay 3 Pad
OK wayne0316: 3PAD
R7867 0402 10K 1%
R7868 0402 NL/10K 1%
GND

PCH_GPP_G18
Co-Lay 3 Pad
OK wayne0316: 3PAD
R7869 0402 10K 1%
R7870 0402 NL/1K 1%
GND

A101-2.1

A101-1
Add

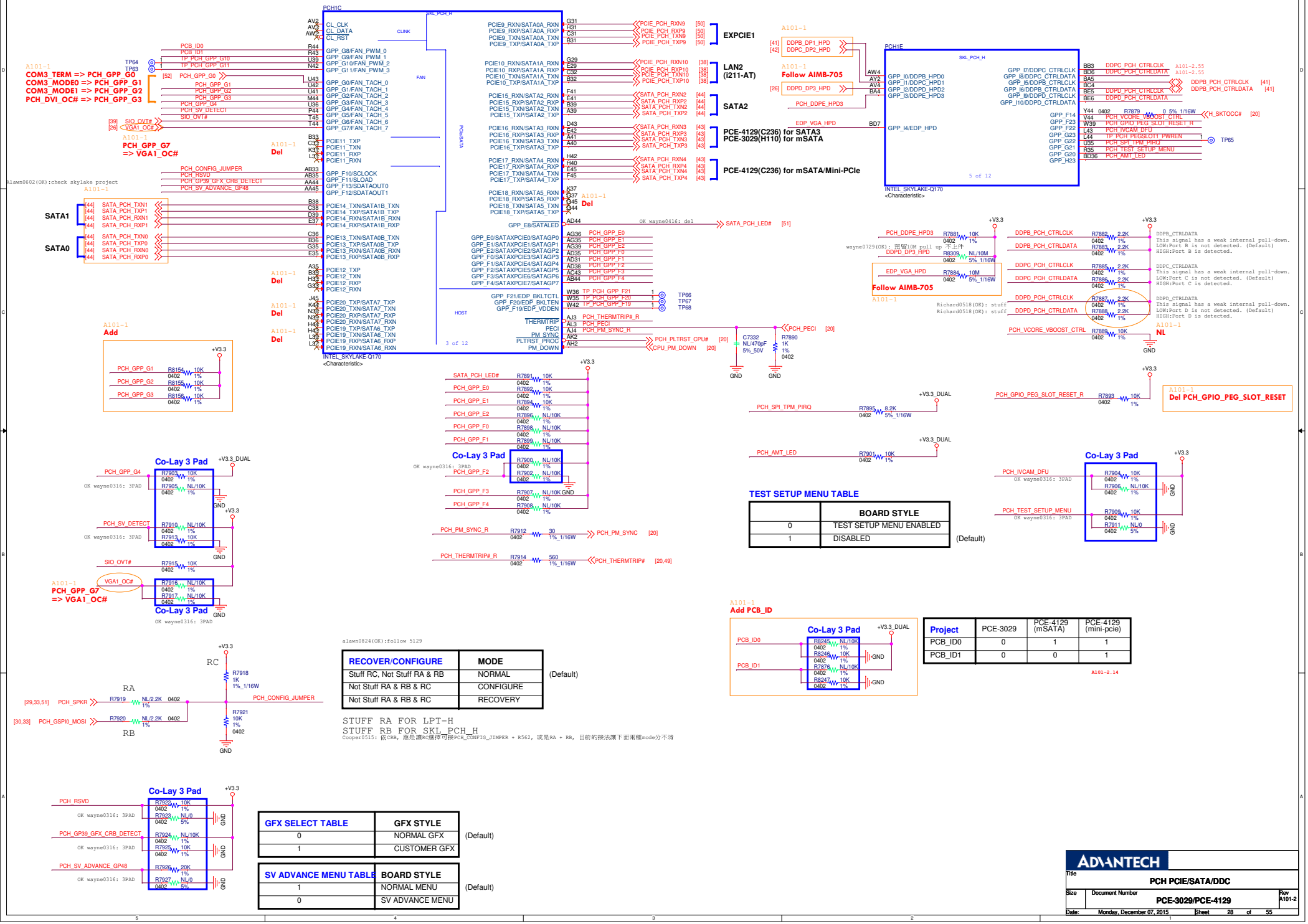
+V3.3_DUAL

AUD_FP_PRESENCE#_R R8160 0402 10K 1%

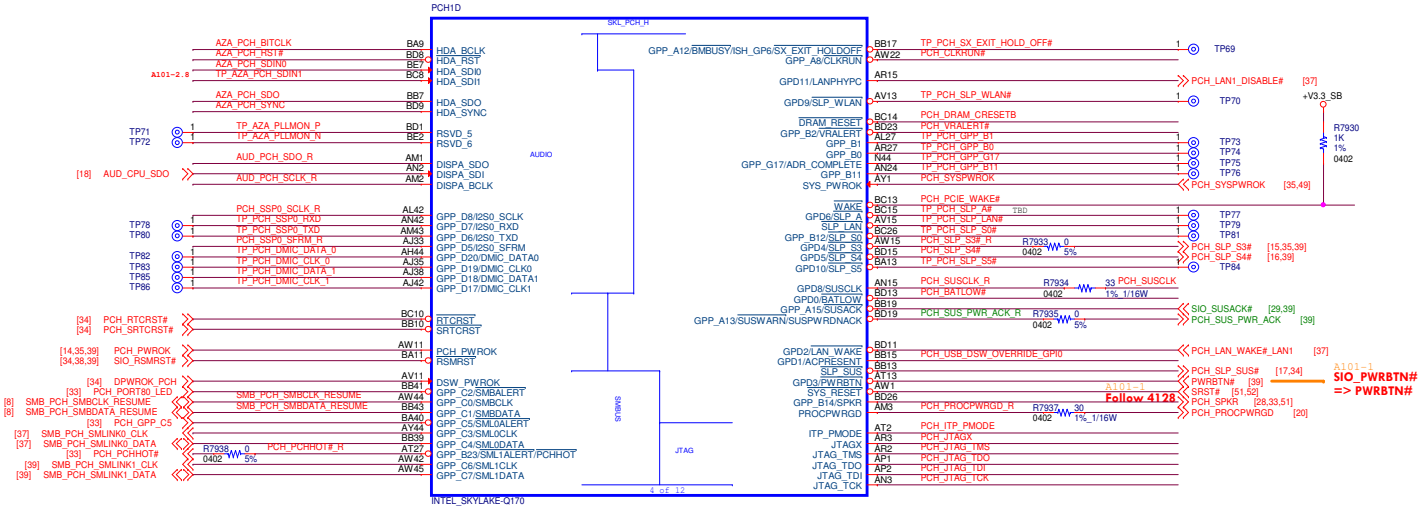
ADVANTECH

Title	PCH DMI/PCIE/USB/LPC	
Size	Document Number PCE-3029/PCE-4129	Rev A101-2
Date: Monday, December 07, 2015	Sheet 27 of 55	

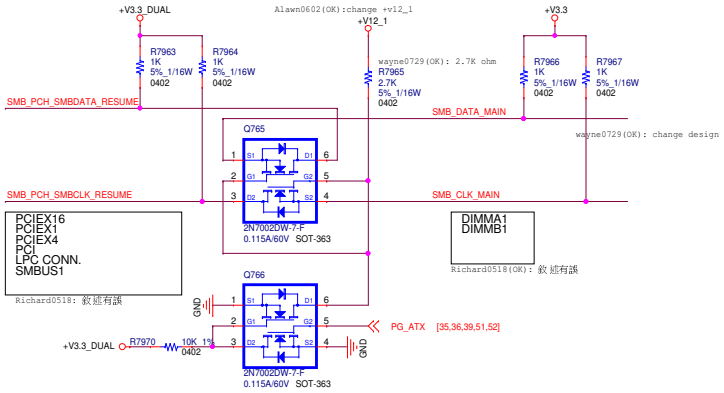
PCH SKL PCH-H (PCIE/SATA/DDC)

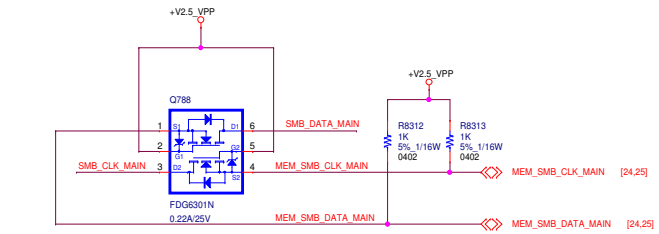


PCH SKL PCH-H (HDA/SMB/MISC)

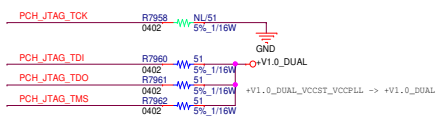


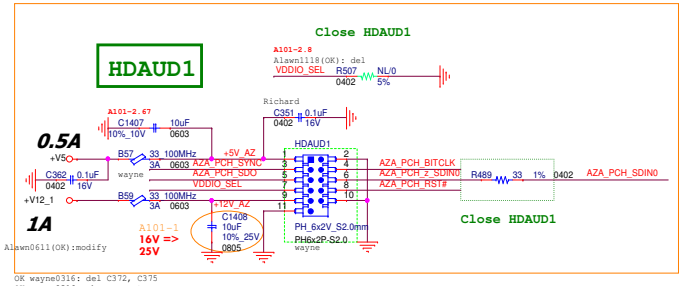
SMBUS

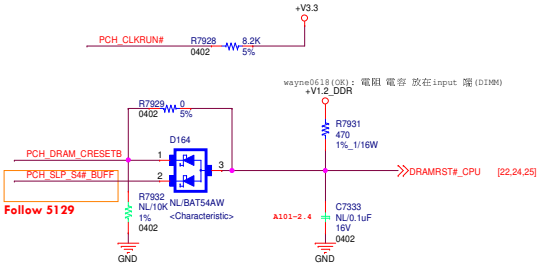


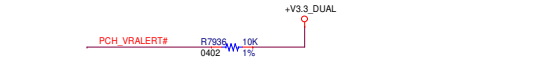


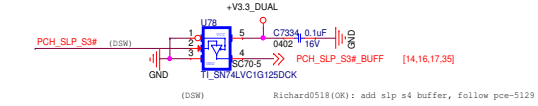
JTAG

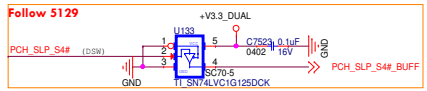


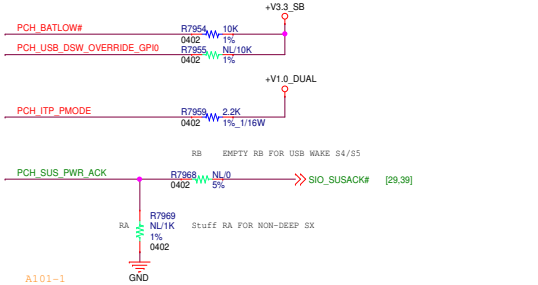


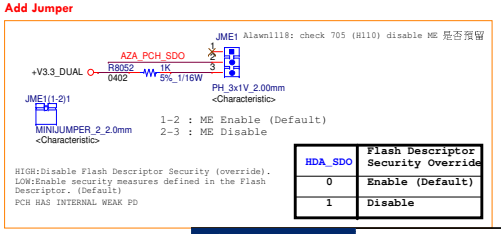


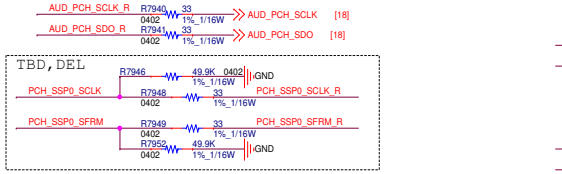


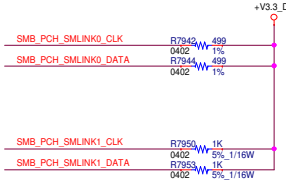


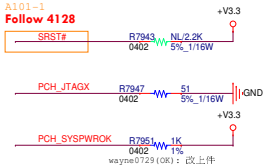




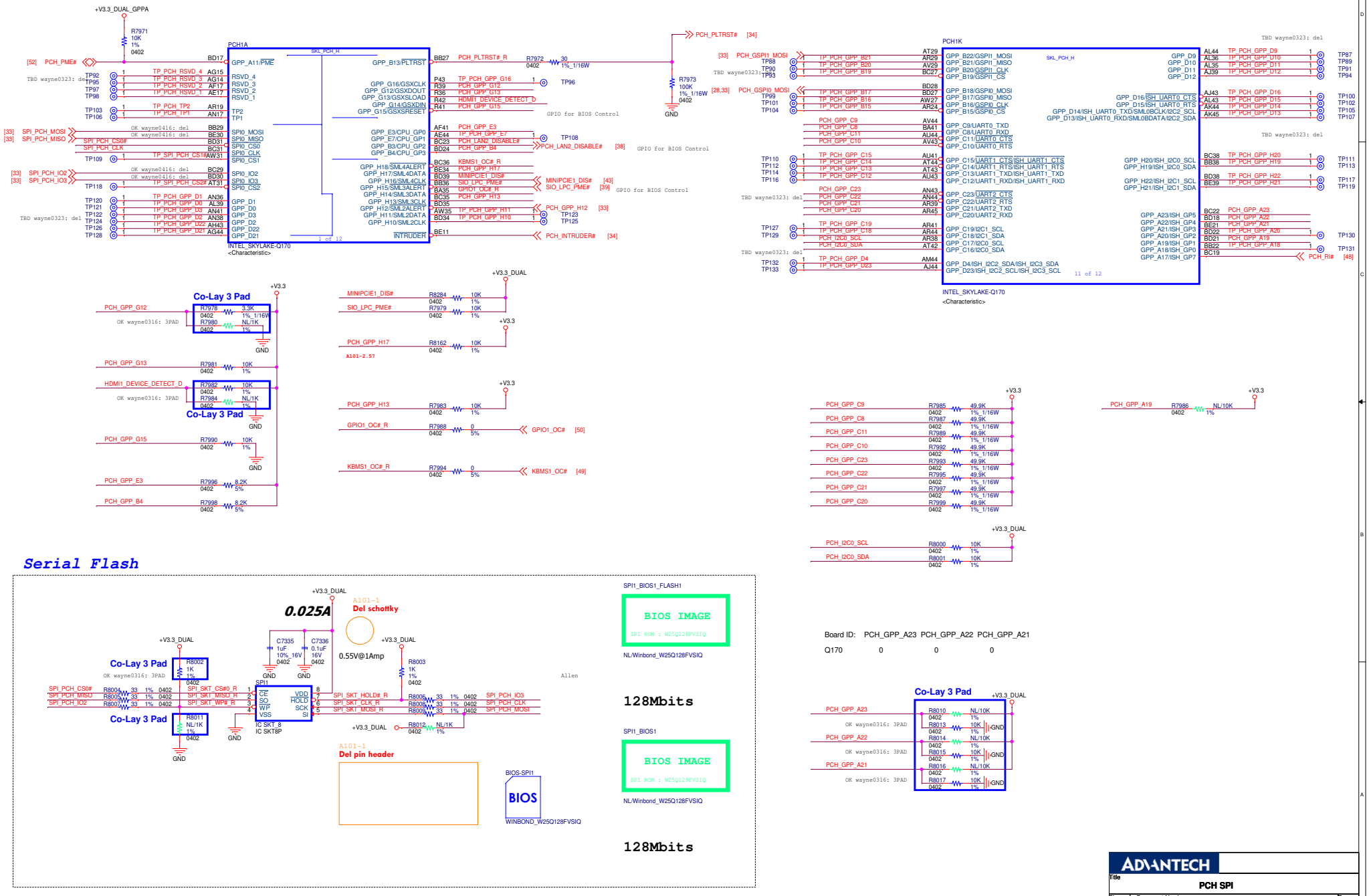






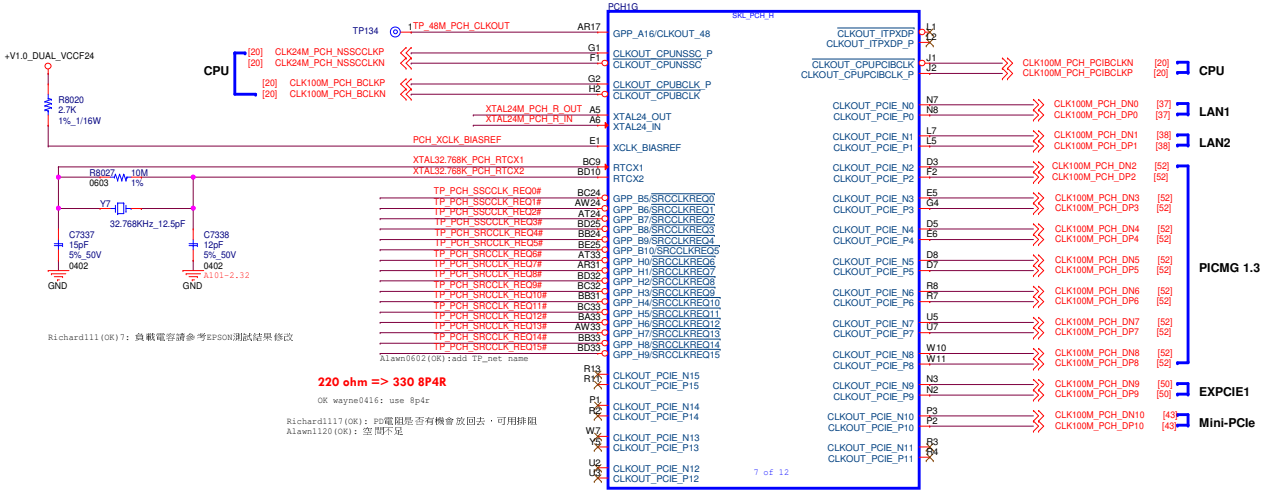


PCH SKL PCH-H (SPI)



Title	PCH SPI		
Size	Document Number	PCE-3029/PCE-4129	Rev A101-2
Date:	Monday, December 07, 2015	Sheet 30 of 55	

PCH SKL PCH-H (CLOCK)



Richard111(OK)7: 負載電容請參考EPSON測試結果修改

Alawn0602(OK):add TP_net name

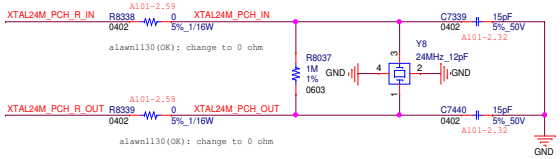
220 ohm => 330 8P4R

OK wayne0416: use 8p4r

Richard1117(OK): PD電阻是否有機會放回去，可用排阻
Alawnl120(OK): 空間不足

alawn0828(OK): 15p → 12p
alawn0727(OK): follow 7127 A101-2

Richard1117(OK): 負載電容請參考EPSON測試結果修改



alawn0727(OK): follow 7127 A101-2

alawn0727(OK): follow 7127 A101-2
alawn0828(OK): 15p → 12p

A101-1
Del PD R 220 of REQ11 ~ 15

ADVANTECH

Title	PCH CLOCK	
Size	Document Number PCE-3029/PCE-4129	Rev A101-2
Date: Monday, December 07, 2015	Sheet 31 of 55	

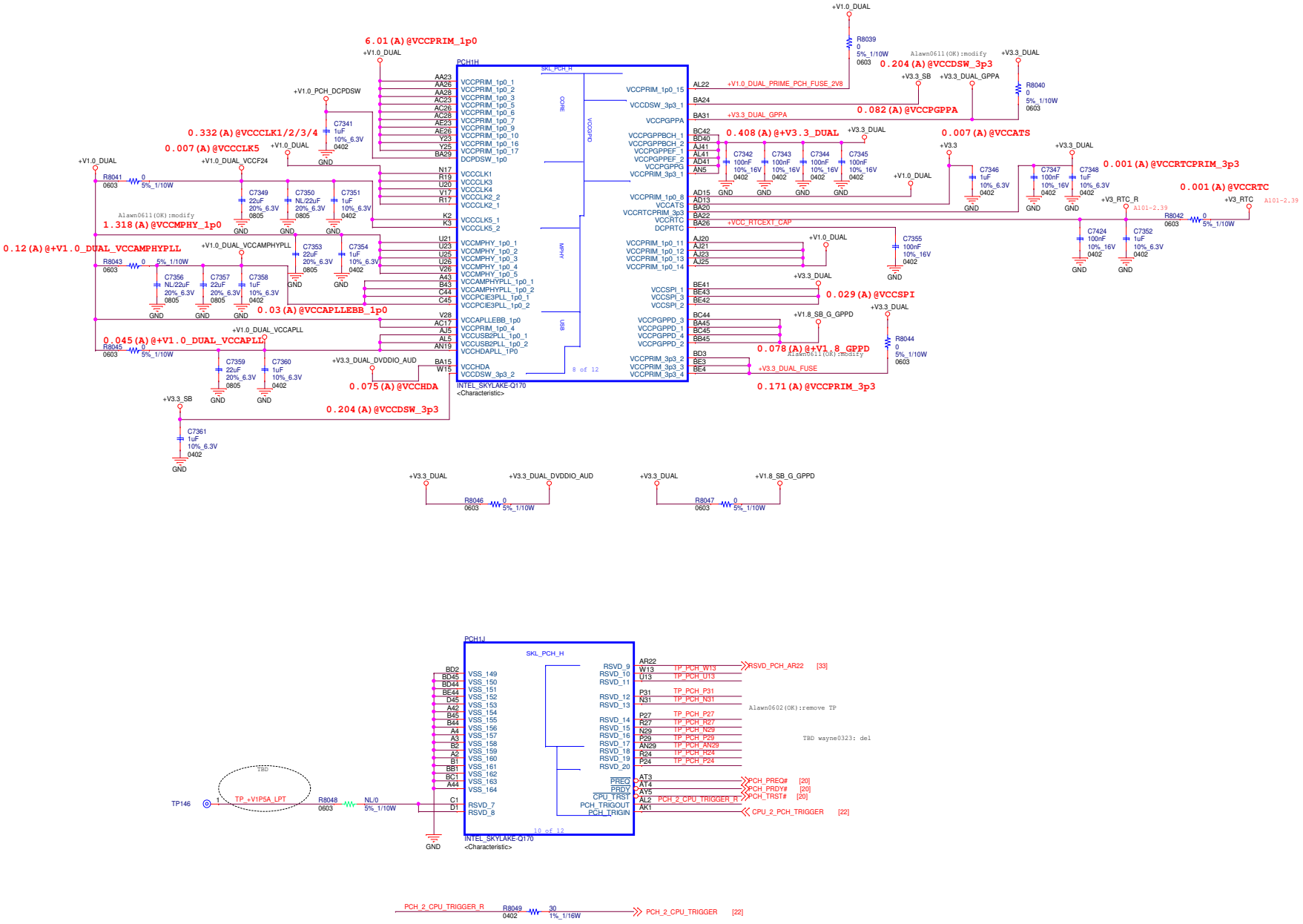
PCH SKL PCH-H (POWER)

7.234(A)@+V1.0_DUAL

0.766(A)@+V3.3_DUAL

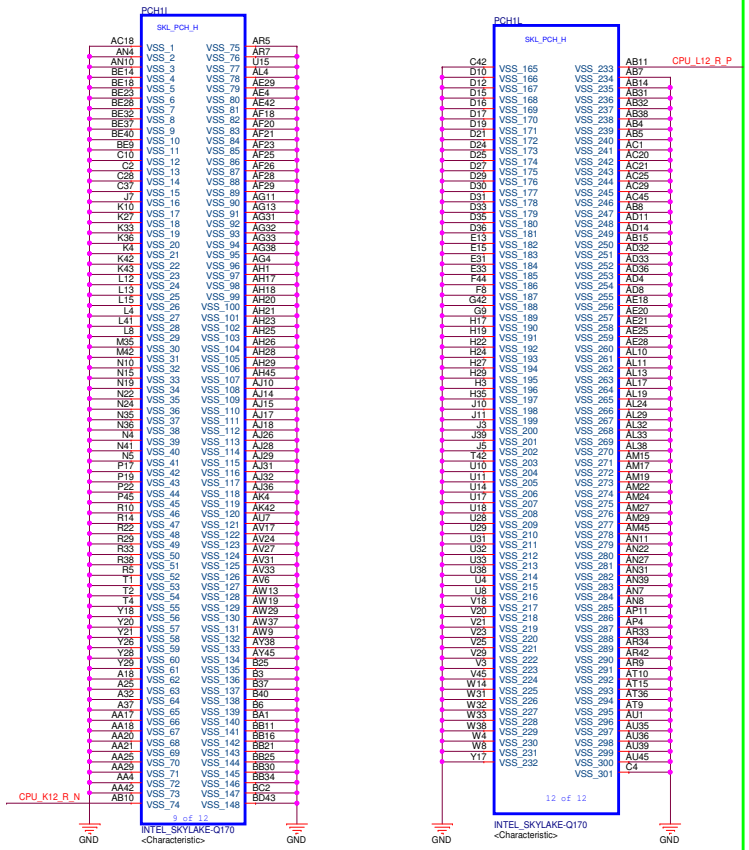
0.205(A)@+V3.3_SB

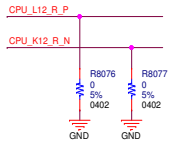
0.036(A)@+V1.8_DUAL



Title	PCH POWER		
Size	Document Number	PCE-3029/PCE-4129	Rev A101-2
Date:	Monday, December 07, 2015	Sheet 32 of 55	

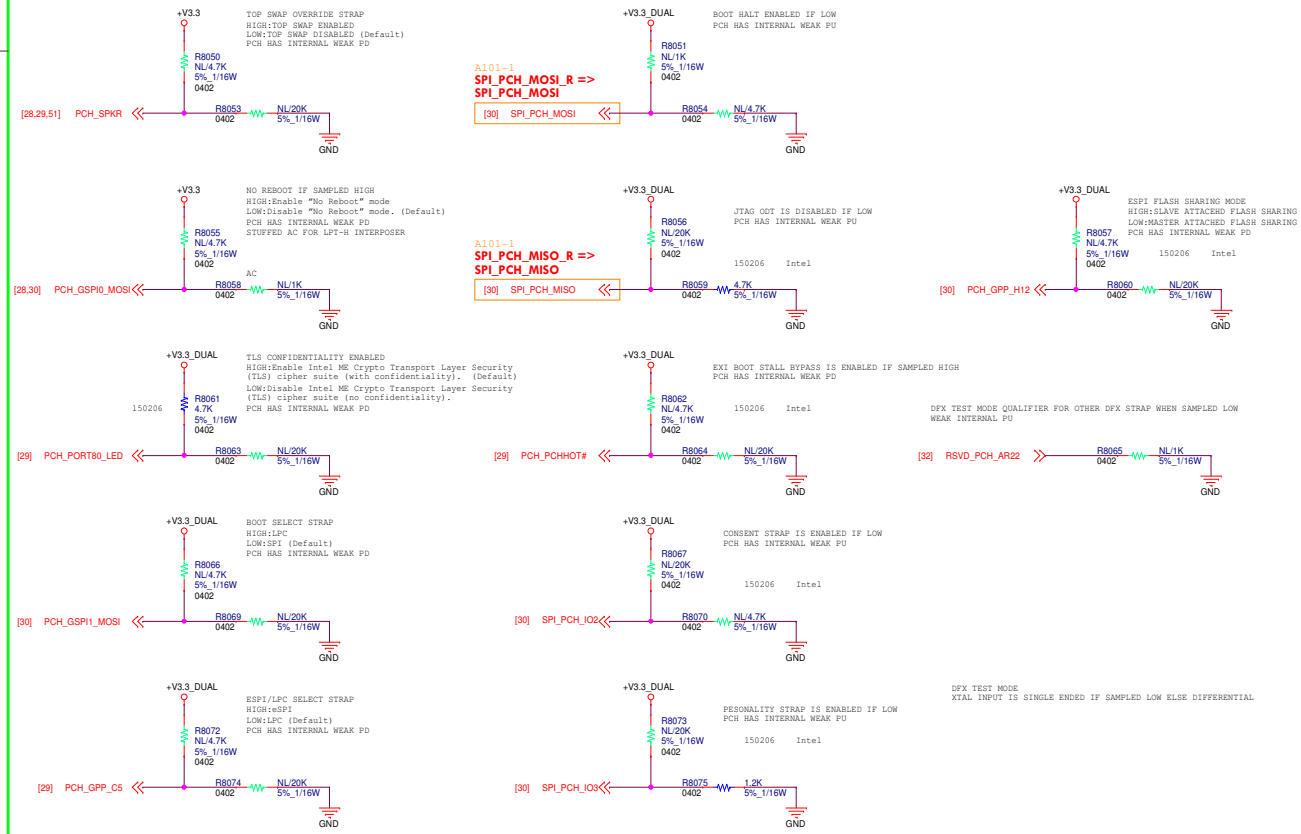
PCH SKL PCH-H (GND,PCH Strap Option)





Layout use 3 pad

PCH Strap Option

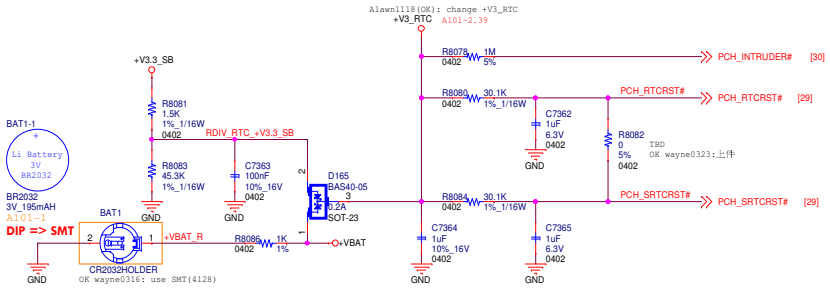


Structure : 3PAD Placement for space saving

ADVANTECH

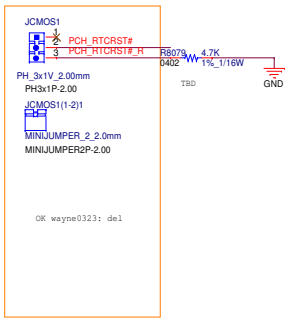
Title	PCH GND/PCH Strap Option	
Size	Document Number: PCE-3029/PCE-4129	Rev: A101-2
Date: Monday, December 07, 2015	Sheet 33 of 55	

RTCRST#



A101-1
Del Box pin header

A101-1
2.54 => 2.00



CMOS CLR JUMPER

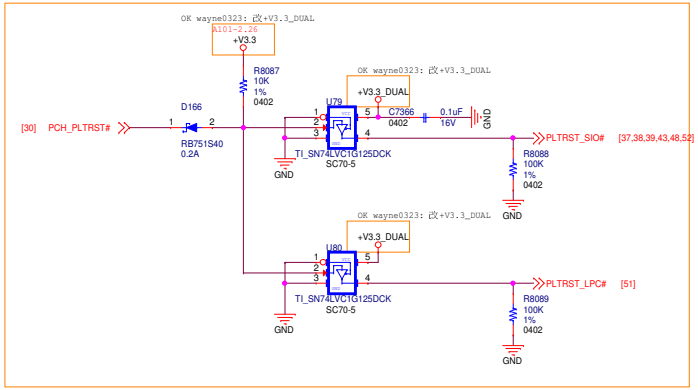
Mode	Jumper Setting
Normal (Default)	1-2
CLR CMOS	2-3

DPWROK

A101-1
Del logic circuit of DPWROK

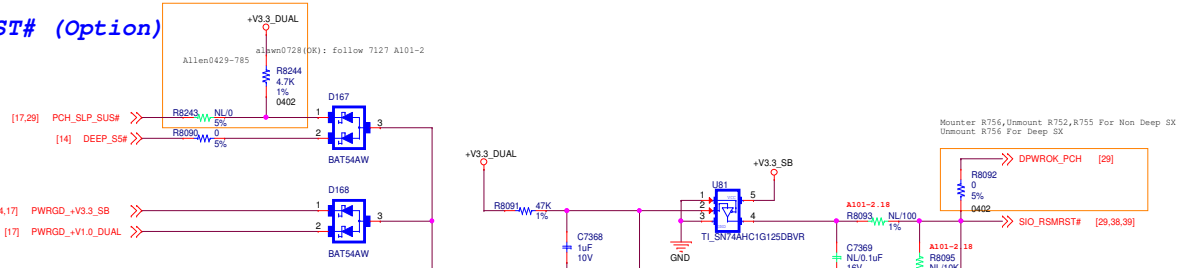
PLTRST#

A101-1
Changed to use buffer

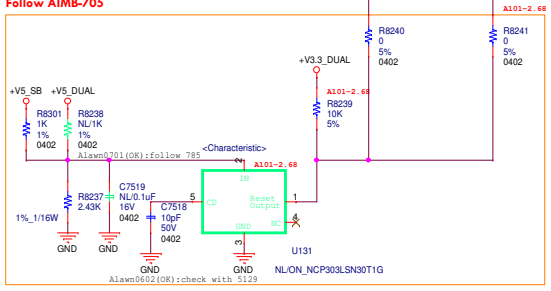


RSMRST# (Option)

A101-1
Follow AIMB-705

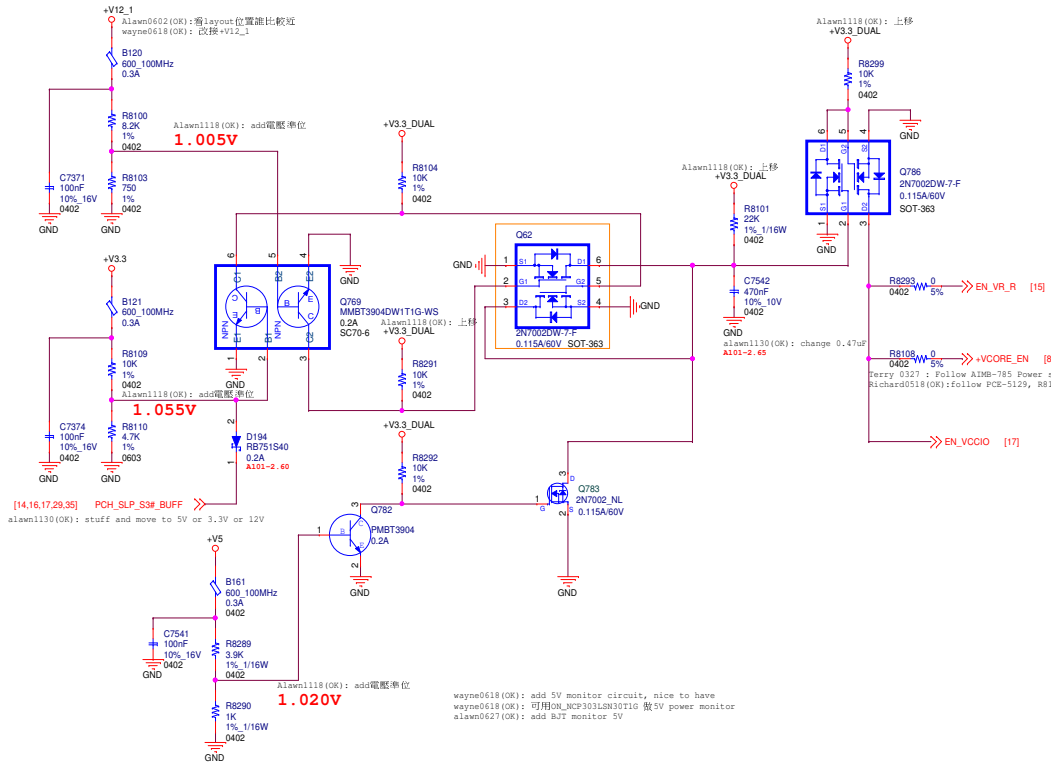


A101-1
Follow AIMB-705

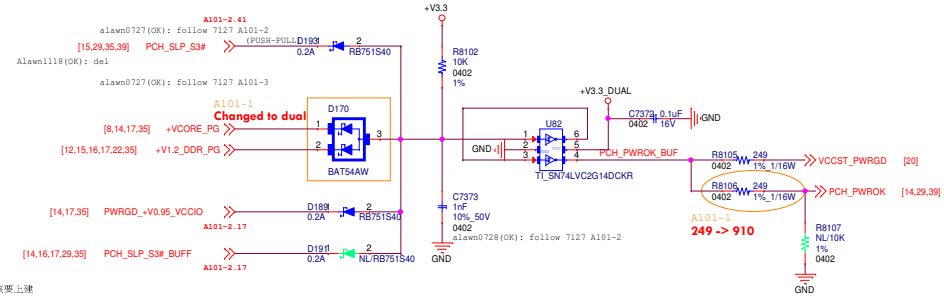


A101-1
Del buffer

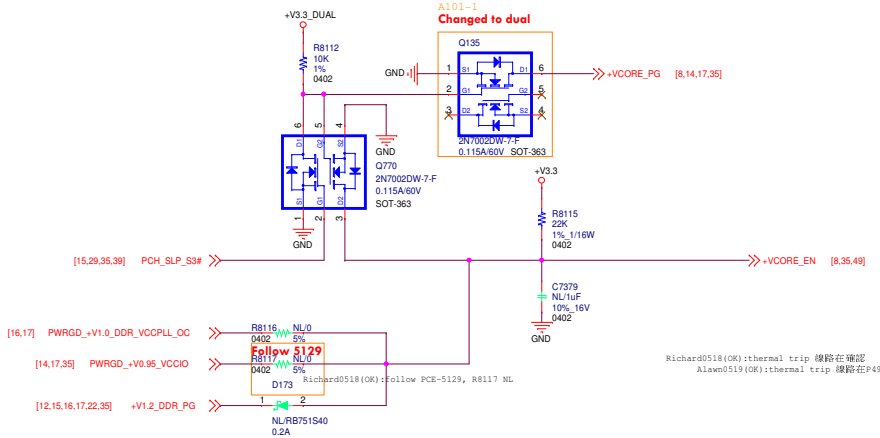
VCCIO_EN



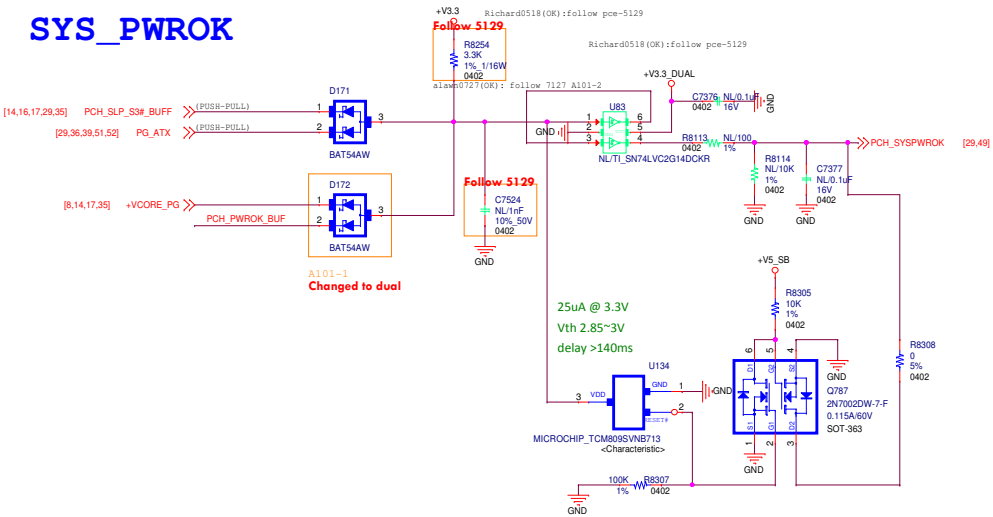
PWROK



VR_ENABLE

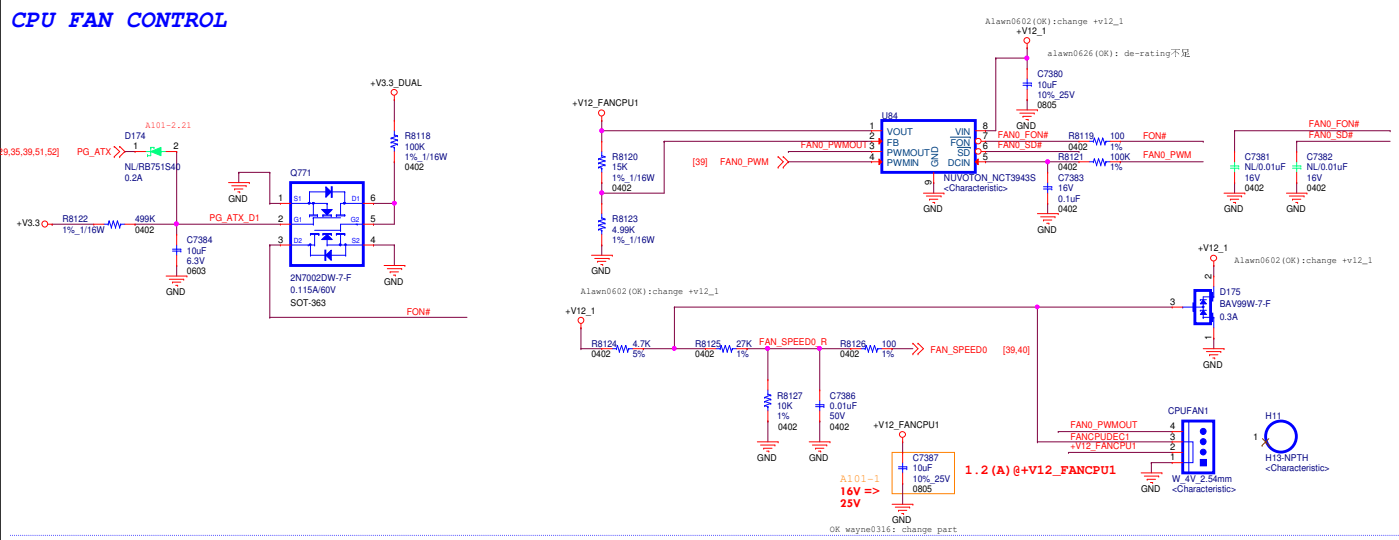


SYS_PWROK



ADVANTECH			
Title	PWROK/SYSPWROK/VCORE_EN		
Size	Document Number	PCE-3029/PCE-4129	Rev A101-2
Date:	Monday, December 07, 2015	Sheet 35 of 55	

CPU FAN CONTROL



SYSFAN1 CONTROL

A101-1

Del SYSFAN1

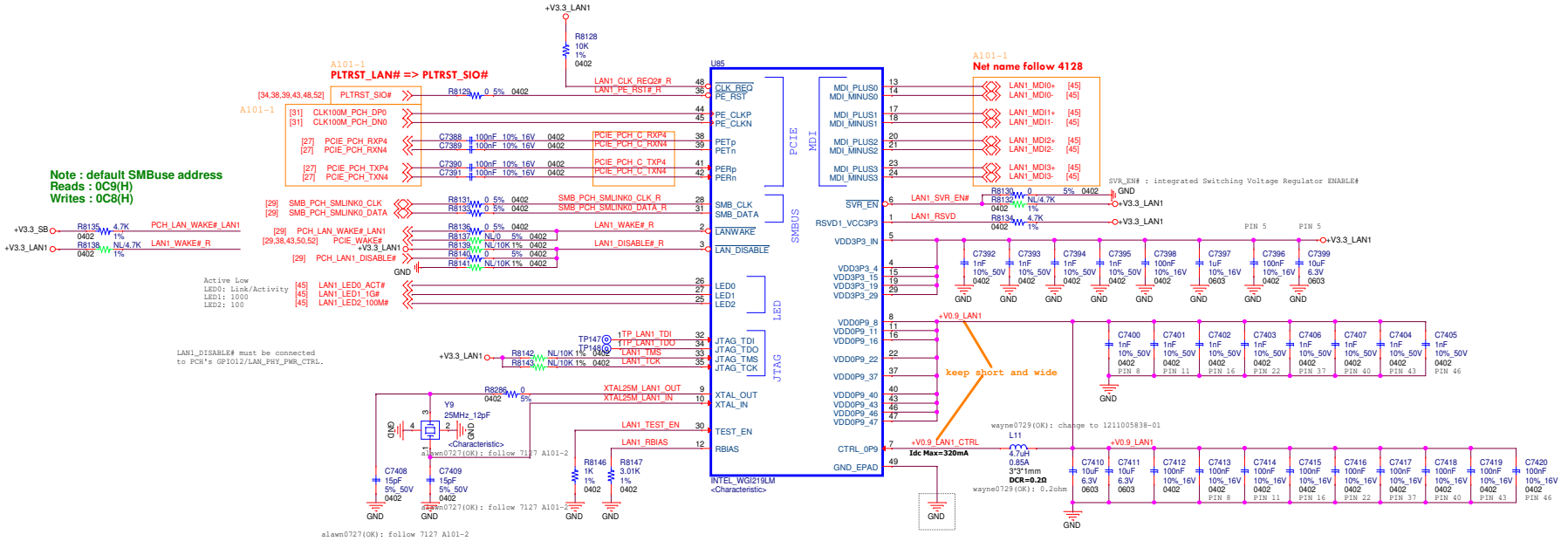
SYSFAN2 CONTROL

A101-1

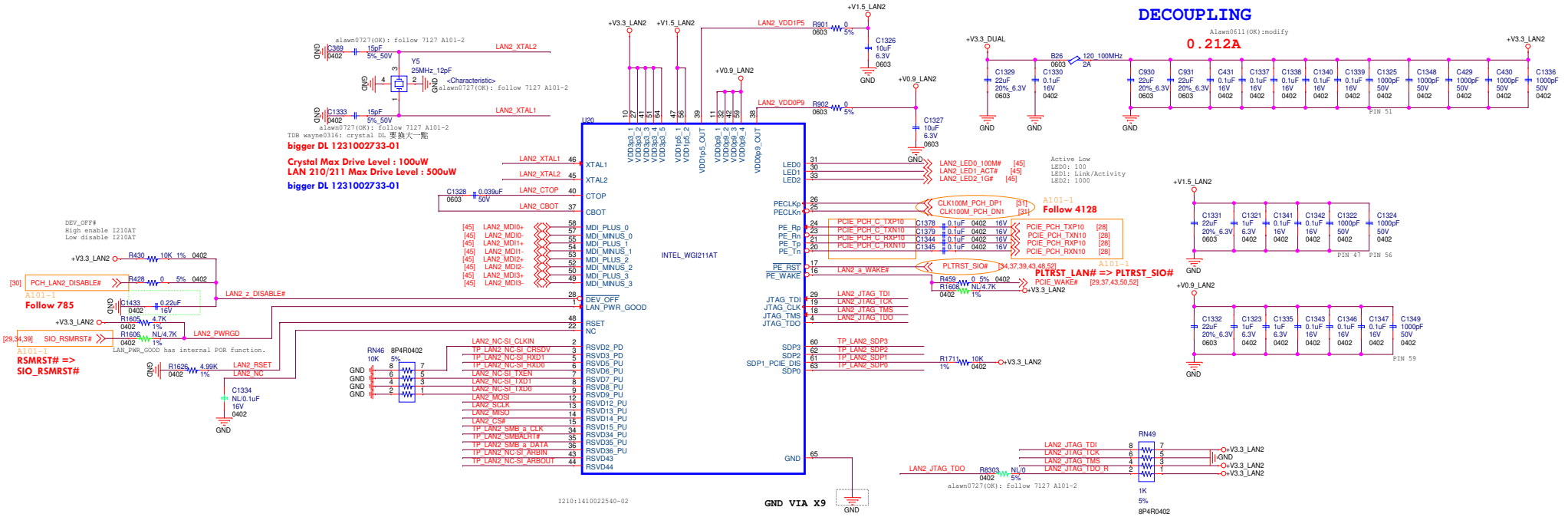
Del SYSFAN2

ADVANTECH			
Title: CONN FAN			
Size	Document Number: PCE-3029/PCE-4129		Rev: A101-2
Date: Monday, December 07, 2015	Sheet 36 of 55		

LAN1 PHY I219LM



LAN2 I211A(H110) / I210(C236)



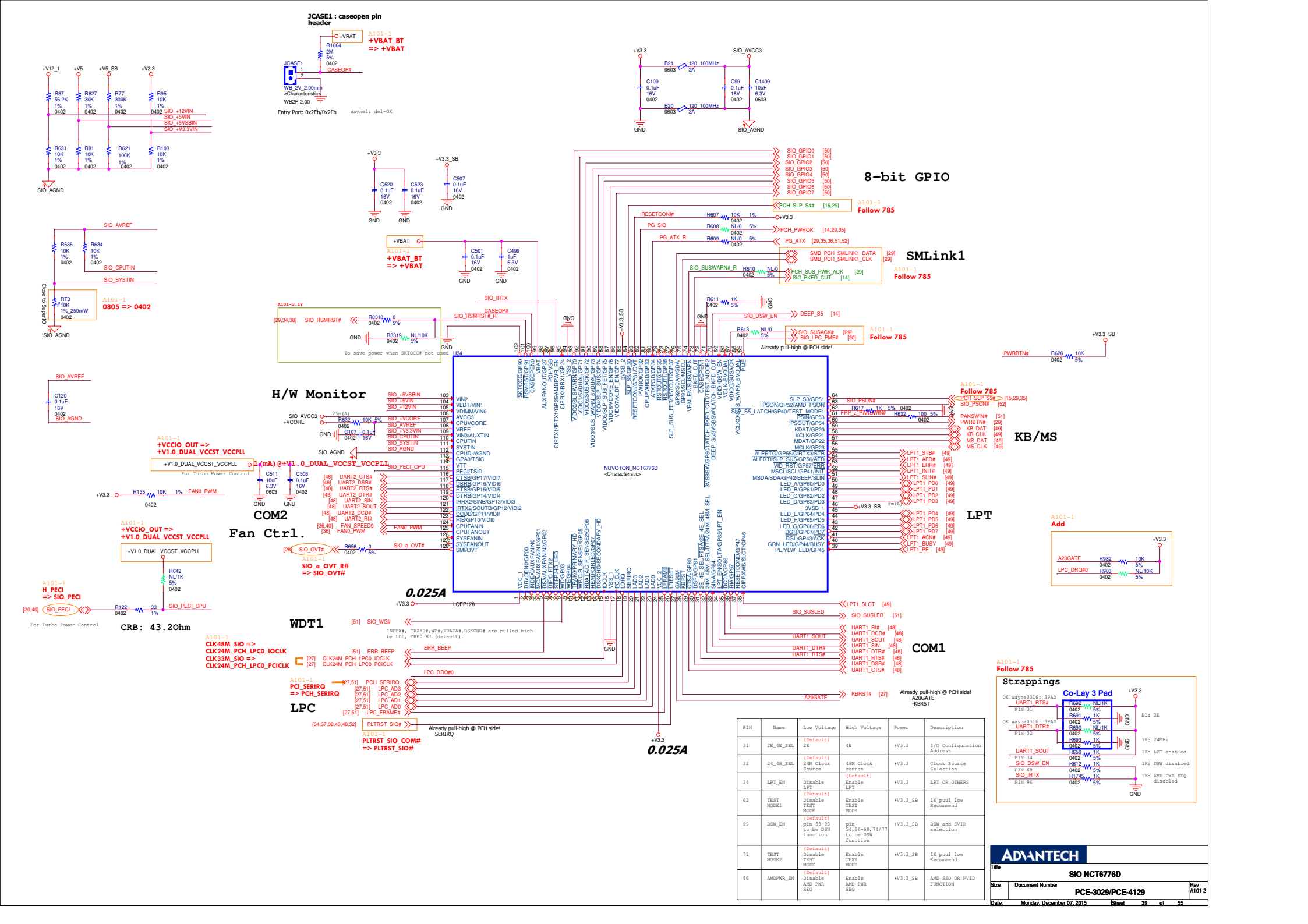
Revision Number: 1.7.2

Table 11-1. TAP Controller Pins

Signal	I/O	Description
TCK	In	Test clock input for the test logic defined by IEEE1149.1. **Note:** Signal should be connected to ground through a 1 KΩ pull-down resistor.
TDI	In	Test Data Input. Serial test instructions and data are received by the test logic at this pin. **Note:** Signal should be connected to VCC33 through a 1 KΩ pull-up resistor.
TDO	O/D	Test Data Output. The serial output for the test instructions and data from the test logic defined in IEEE1149.1. **Note:** Signal should be connected to VCC33 through a 1 KΩ pull-up resistor.
TMS	In	Test Mode Select input. The signal received at TMS is decoded by the TAP controller to control test operations. **Note:** Signal should be connected to VCC33 through a 1 KΩ pull-up resistor.

ADVANTECH

Title	LAN2 NIC I210AT/I210	
Size	Document Number: PCE-3029/PCE-4129	Rev: A101-2
Date: Monday, December 07, 2015	Sheet 38 of 55	



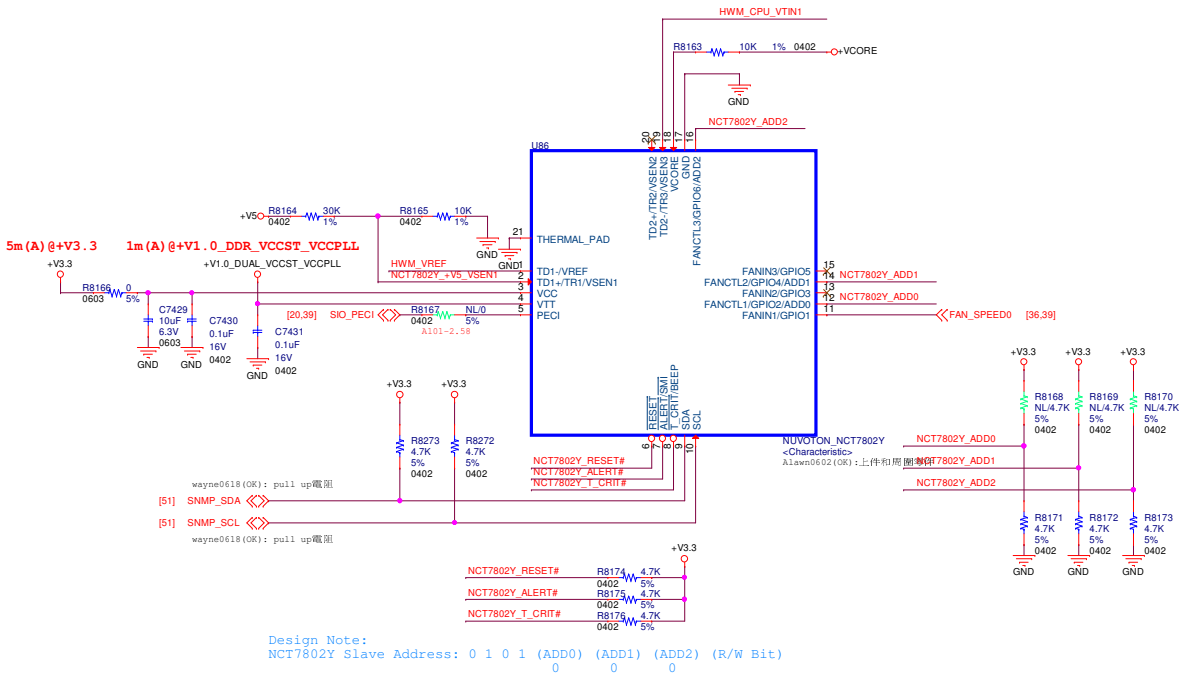
PIN	Name	Low Voltage	High Voltage	Power	Description
31	2E_4E_SEL	(Default) 2E	4E	+V3.3	I/O Configuration Address
32	24_48_SEL	(Default) 24M Clock Source	48M Clock source	+V3.3	Clock Source Selection
34	LPT_EN	Disable LPT	(Default) Enable LPT	+V3.3	LPT OR OTHERS
62	TEST MODE1	(Default) Disable TEST MODE	Enable TEST MODE	+V3.3_SB	1K puul low Recommend
69	DSW_EN	(Default) pin 88-93 to be DSW function	pin 54,66-68,74/77 to be DSW function	+V3.3_SB	DSW and SVID selection
71	TEST MODE2	(Default) Disable TEST MODE	Enable TEST MODE	+V3.3_SB	1K puul low Recommend
96	AMDPWR_EN	(Default) Disable AMD PWR SEQ	Enable AMD PWR SEQ	+V3.3_SB	AMD SEQ OR PVID FUNCTION

OK wayne0316: del
OK wayne0316: 改用NCT7802

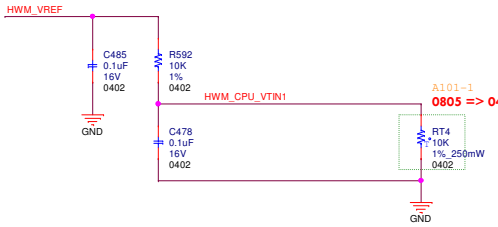
A101-1
Del W83782G
Add NCT7802Y from 785

alawn0619(OK):ref 5129 NA
wayne0618(OK): check
Input是否要處理

A101-1
Add HWM_MB_VTIN3
wayne0618(OK): del



Design Note:
NCT7802Y Slave Address: 0 1 0 1 (ADD0) (ADD1) (ADD2) (R/W Bit)
0 0 0



Layout Note:
RT4 Place inner CPU Socket.
R1071,C814,C993 Close to U55
HWM_MB_VTIN1 Spacing 20 mil

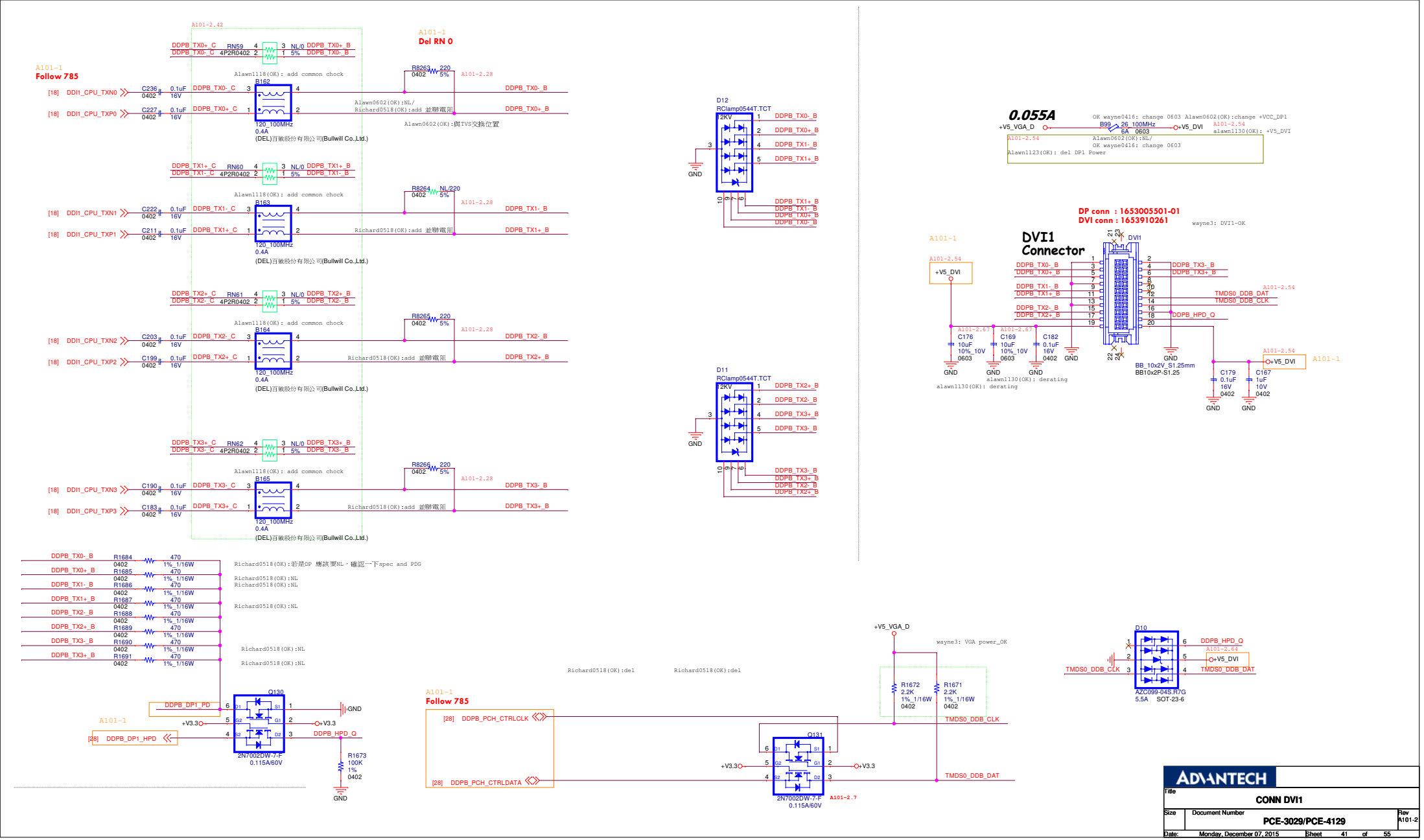
wayne0618(OK): del

Layout Note:
RT1 Place far away hot area.
R1070,C813,C807 Close to U55
HWM_MB_VTIN3 Spacing 20 mil

Design Note:
VREF:3.6(V),Temperature is 25 Deg.
HWM_CPU_VTIN1 = 3.6 x [10K /(10K+10K)] = 1.8(V)
HWM_MB_VTIN3 = 3.6 x [10K /(10K+10K)] = 1.8(V)

ADVANTECH

Title	HWM NCT7802Y	
Size	Document Number PCE-3029/PCE-4129	Rev A101-2
Date: Monday, December 07, 2015	Sheet 40 of 55	



ADVANTECH			
Title	CONN DVI1		
Size	Document Number	PCE-3029/PCE-4129	Rev A101-2
Date: Monday, December 07, 2015	Sheet 41 of 55		

Richard0518(OK):修改地方同DP1

A101-1
Del RN 0

A101-1
Follow 785

[18] DDI2_CPU_TXN0 — C379 0.1uF 16V 0402 — DDPC_TX0-_B
[18] DDI2_CPU_TXP0 — C377 0.1uF 16V 0402 — DDPC_TX0+_B
R8267 NL/169 1% 1/16W

[18] DDI2_CPU_TXN1 — C373 0.1uF 16V 0402 — DDPC_TX1-_B
[18] DDI2_CPU_TXP1 — C370 0.1uF 16V 0402 — DDPC_TX1+_B
R8268 NL/169 1% 1/16W

[18] DDI2_CPU_TXN2 — C366 0.1uF 16V 0402 — DDPC_TX2-_B
[18] DDI2_CPU_TXP2 — C361 0.1uF 16V 0402 — DDPC_TX2+_B
R8269 NL/169 1% 1/16W

[18] DDI2_CPU_TXN3 — C358 0.1uF 16V 0402 — DDPC_TX3-_B
[18] DDI2_CPU_TXP3 — C357 0.1uF 16V 0402 — DDPC_TX3+_B
R8270 NL/169 1% 1/16W

D31
RClamp0544T.TCT
12KV
1 DDPC_TX0-_B
2 DDPC_TX0+_B
3 GND
4 DDPC_TX1+_B
5 DDPC_TX1-_B
10 9 7 6 DDPC_TX1-_B DDPC_TX1+_B DDPC_TX0+_B DDPC_TX0-_B

D29
RClamp0544T.TCT
12KV
1 DDPC_TX2-_B
2 DDPC_TX2+_B
3 GND
4 DDPC_TX3-_B
5 DDPC_TX3+_B
10 9 7 6 DDPC_TX3+_B DDPC_TX3-_B DDPC_TX2+_B DDPC_TX2-_B

Alawn1118(OK): change to FDMC8884
Alawn1118(OK): add 2.7k at gate
Alawn1118(OK): 12_1V or 12V check layout
Richard1117(OK): 怪怪的

Alawn1118(OK): add net name
OK wayne0416: 3 pad

+V12 A101-2.31 — R8329 2.7K 1% 1/16W 0402 — Q790 FDMC8884 9A/30V
+VCC_DP2_B — B103 26_100MHz 6A 0603 — +V3.3_DP1 A101-2.63
alawn1130(OK): +V3.3_DP1
Alawn1118(OK): change 0603(ref usb)
A101-2.43
A101-2.55
Alawn1123(OK): del DVI2 power
+V3.3

DP conn : 1653005501-01
DVI conn : 1653910261
alawn1130(OK): DP1
wayne3: DVI2-OK

DP1 Connector

A101-1
A101-2.63 +V3.3_DP1
H2 DP1 A101-2.63
H1 DPH(F)_10x2V_S1.27mm <Characteristic>

DDPC_TX0-_B DDPC_TX0+_B DDPC_TX1-_B DDPC_TX1+_B DDPC_TX2-_B DDPC_TX2+_B
DDPC_TX3-_B DDPC_TX3+_B
A101-2.55 DDI2_CPU_C_AUXN DDI2_CPU_C_AUXP
DDPC_HPD_Q

C673 22uF 20% 6.3V 0603 GND
C674 22uF 20% 6.3V 0603 GND
C672 0.1uF 16V 0402 GND
GND
C676 0.1uF 16V 0402 GND
C675 1uF 10V 0402 GND
A101-2.63 +V3.3_DP1 A101-1

R1719 100K 1% 0402 +V3.3
C1420 0.1uF 16V 0402 DDI2_CPU_AUXN [18]
C1421 0.1uF 16V 0402 DDI2_CPU_AUXP [18]
R1720 100K 1% 0402 GND

A101-1
Follow 785
A101-2.55
Alawn1123(OK): del DDPC_PCH_CTRLCLK/DATA

Alawn1123(OK): del DDPC_DP2_PD
A101-2.55
A101-1
+V3.3
[28] DDPC_DP2_HPD
Q55 2N7002DW-7-F 0.115A/60V
DDPC_HPD_Q
R1692 100K 1% 0402 GND

D48
DDI2_CPU_C_AUXP A101-2.55
DDPC_HPD_Q A101-2.63
+V3.3_DP1
DDI2_CPU_C_AUXN A101-2.55
AZC099-04S.R7G 5.5A SOT-23-6

ADVANTECH

Title	CONN DVI2	
Size	Document Number: PCE-3029/PCE-4129	Rev: A101-2
Date: Monday, December 07, 2015	Sheet 42 of 55	

mini-PCIE1 / mSATA1

waynel: 1.5 & 3.3V power use bead 切換BOM change-OK

Design note
+3.3Vaux: 3.3V/ 2.75A
+1.5V: 1.5V/ 0.5A

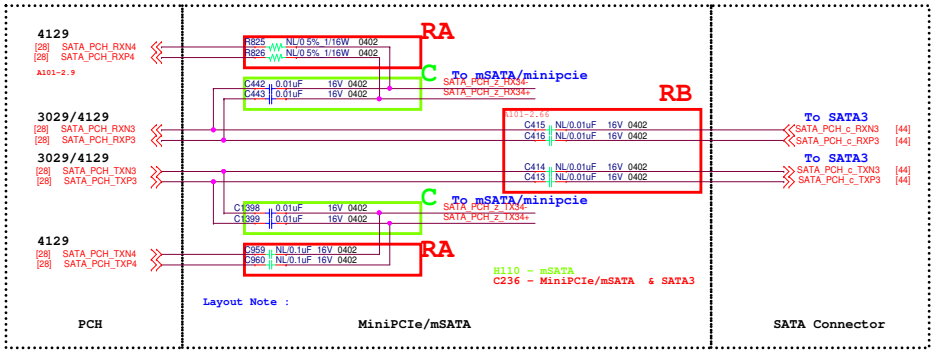
H110

	stuff	empty
mSATA	C442,C443,C1398,C1399,B96,B97,R1716	C959,C960,R825,R826,B94,B95 R7871#7873

C236

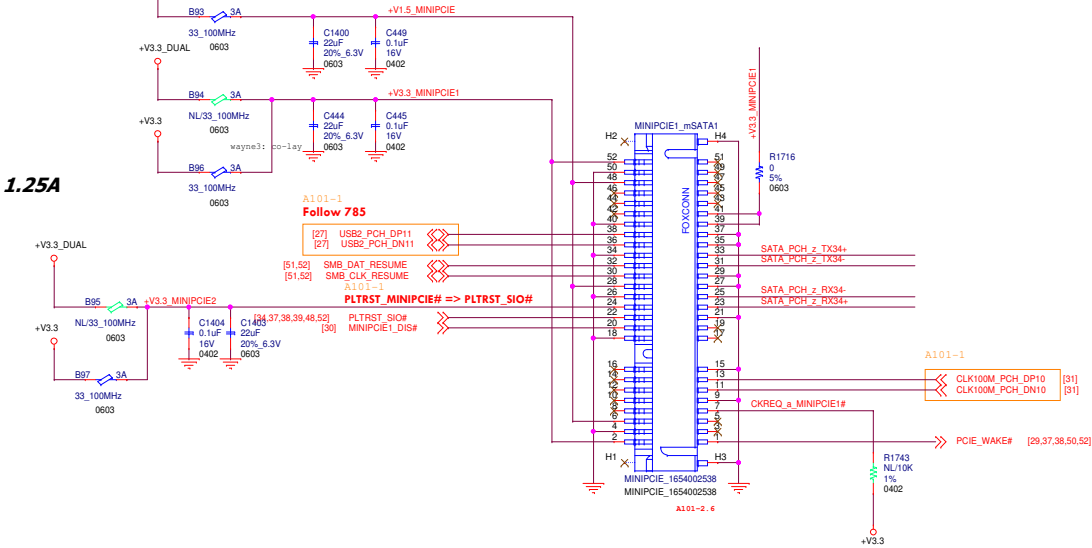
	stuff	empty	
mSATA	C959,C960,R825,R826,B96,B97,R1716 R7871#7873	C442,C443,C1398,C1399,B94,B95	default
MINIPCIE 1.2	C959,C960,R825,R826,B94,B95,R1716 R7871#7873	C442,C443,C1398,C1399,B97,B96	
MINIPCIE 1.1	C959,C960,R825,R826,B96,B95 R7871#7873	C442,C443,C1398,C1399,B94,B97,R1716	

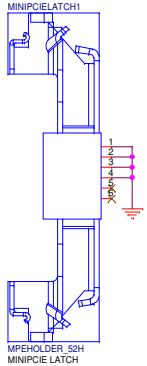
Co-Lay



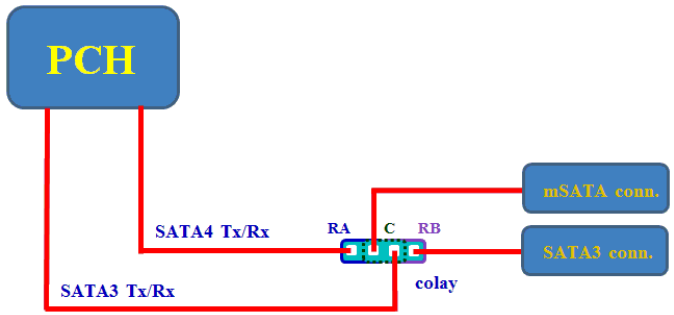
0.375A

A101-1
+V1.5_PCH
=> +V1.5

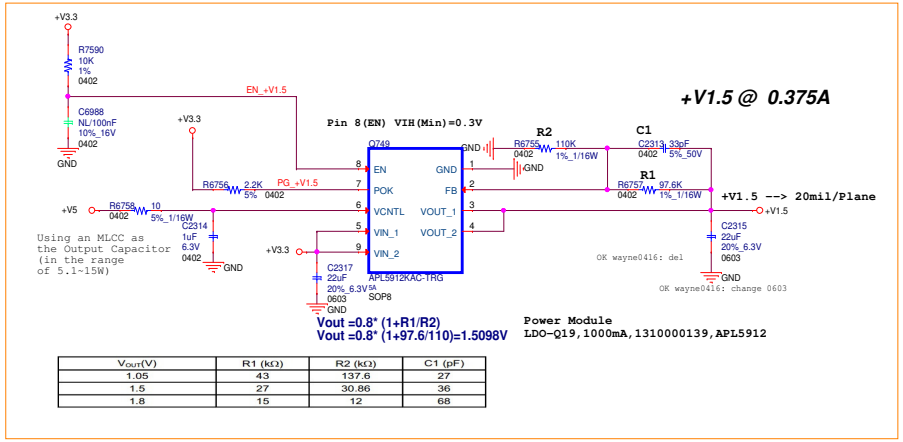




alawn1130(OK): colay picture



A101-1
Add +V1.5 for Mini-PCIe



+V1.5 @ 0.375A

V_{OUT}(V)	R1 (kΩ)	R2 (kΩ)	C1 (pF)
1.05	43	137.6	27
1.5	27	30.86	36
1.8	15	12	68

Pin51 | SLP_S3# = Power

Power of Pin2, 39, 41, 52		
Pin43	SLP_S3#	Power
L	L	3.3V
L	H	3.3V
H	L	0V
H	H	3.3V

Pin43 | SLP_S3# = Power

Power of Pin24		
Pin51	SLP_S3#	Power
L	L	0V
L	H	3.3V
H	L	3.3V
H	H	3.3V

Pin	mini-pcie 1.1	mini-pcie 1.2	mSATA	
2	3.3V	3.3Vaux	3.3V	+V3.3_MINI11
24	3.3Vaux	3.3Vaux	3.3V	+V3.3_MINI12
39	Reserved*	3.3Vaux	3.3V	+V3.3_MINI11
41	Reserved*	3.3Vaux	3.3V	+V3.3_MINI11
52	3.3V	3.3Vaux	3.3V	+V3.3_MINI11

Spec.	Mini PCIe 1.1	Mini PCIe 1.2	mSATA
Pin43	Reserved (H)	GND (L)	NC (H)
Pin51	Reserved (H)	Reserved (H)	Presences Detection (GND->L)

3.3. Connector Pin-out Definitions

The following sections illustrate signal pin-outs for the system connector. Table 3-6 lists the pin-out for the system connector.

Table 3-6: System Connector Pin-out

Pin #	Name	Pin #	Name
51	Reserved	52	+3.3Vaux
49	Reserved	50	GND
47	Reserved	48	+1.5V
45	Reserved	46	LED_WPAN#
43	GND	44	LED_WLAN#
41	+3.3Vaux	42	LED_WWAN#
39	+3.3Vaux	40	GND
37	GND	38	USB_D+
35	GND	36	USB_D-
33	PETp0	34	GND
31	PETn0	32	SMB_DATA
29	GND	30	SMB_CLK
27	GND	28	+1.5V
25	PERp0	26	GND
23	PERn0	24	+3.3Vaux
21	GND	22	PERST#
19	Reserved* (UIM_C4)	20	W_DISABLE#
17	Reserved* (UIM_C8)	18	GND

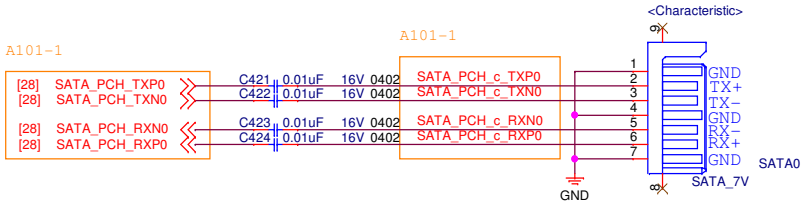
Pin #	Name	Pin #	Name
9	GND	10	UIM_DATA
7	CLKREQ#	8	UIM_PWR
5	COEX2	6	1.5V
3	COEX1	4	GND
1	WAKE#	2	3.3Vaux

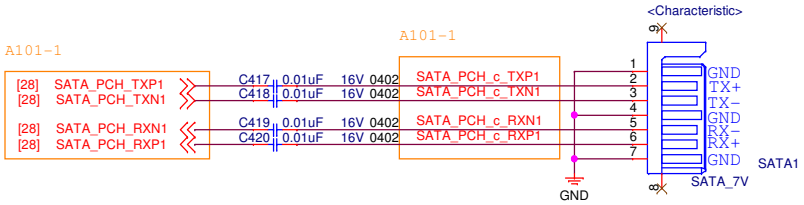
* Reserved for future UIM interface (if needed)

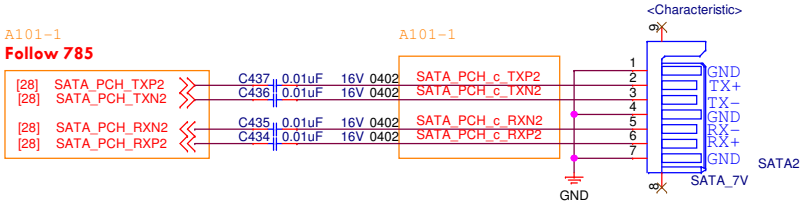
ADVANTECH

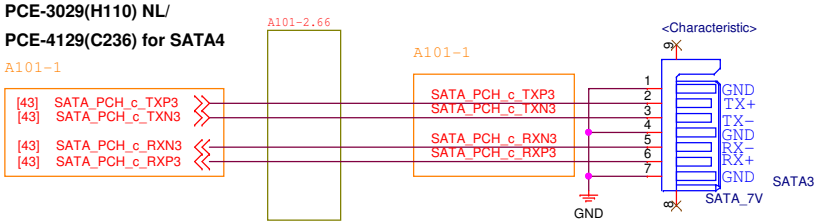
Title	MIN PCIE/mSATA	
Size	Document Number PCE-3029/PCE-4129	Rev A101-2
Date: Monday, December 07, 2015	Sheet 43 of 55	

SATA PORT-> 6Gbps





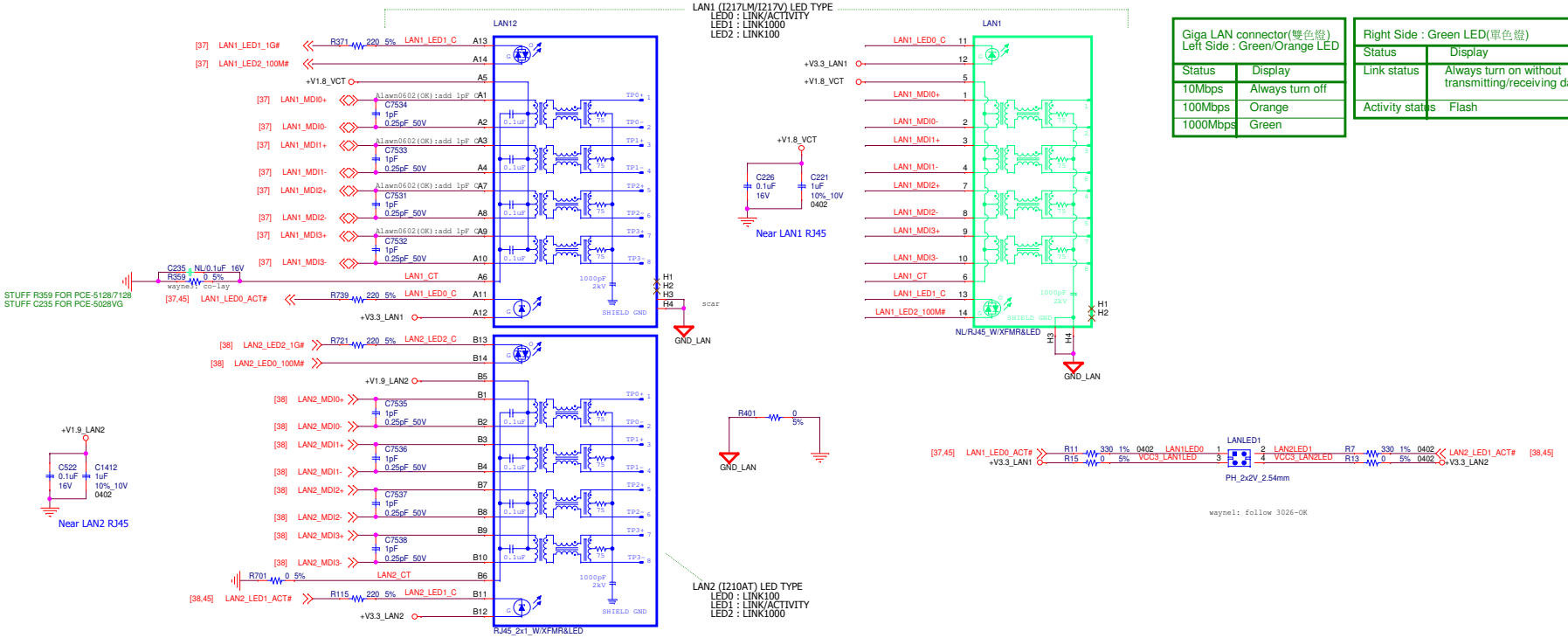




wayne0618(OK): Part_Number_Value是上件, value不應NL/

waynel: 分開寫-OK

Title	CONN SATA	
Size	Document Number: PCE-3029/PCE-4129	Rev: A101-2
Date: Monday, December 07, 2015	Sheet 44 of 55	

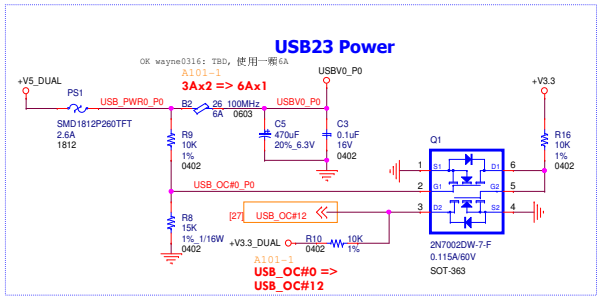


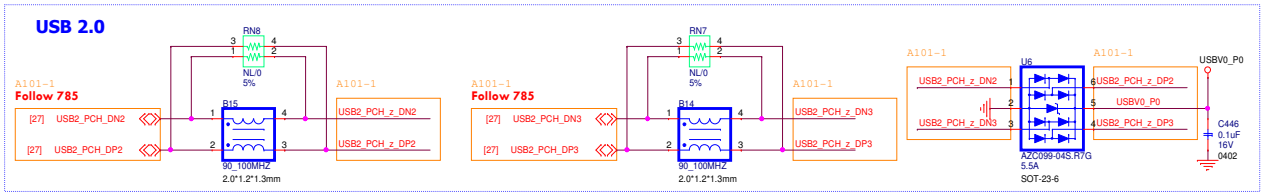
Giga LAN connector(雙色燈) Left Side : Green/Orange LED	
Status	Display
10Mbps	Always turn off
100Mbps	Orange
1000Mbps	Green

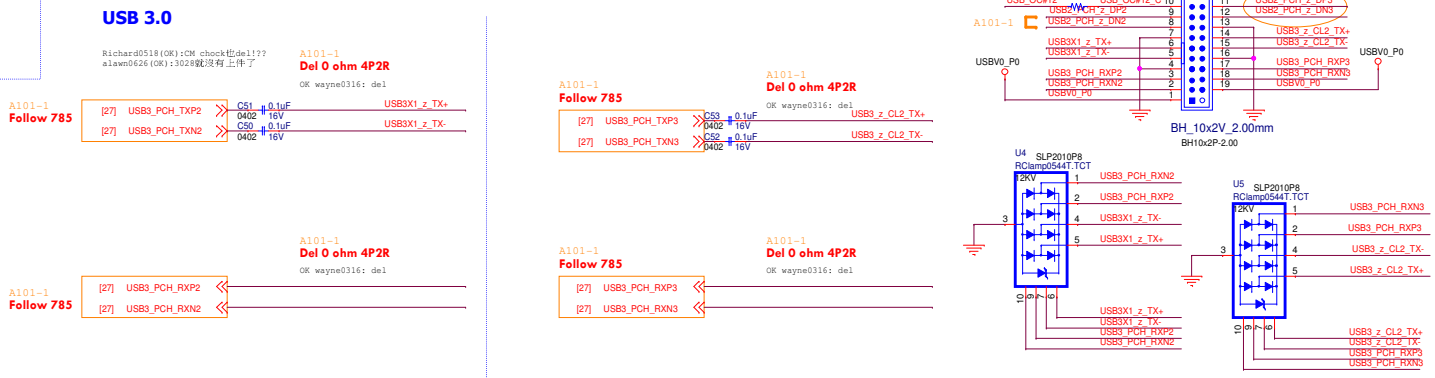
Right Side : Green LED(單色燈)	
Status	Display
Link status	Always turn on without transmitting/receiving data
Activity status	Flash

ADVANTECH

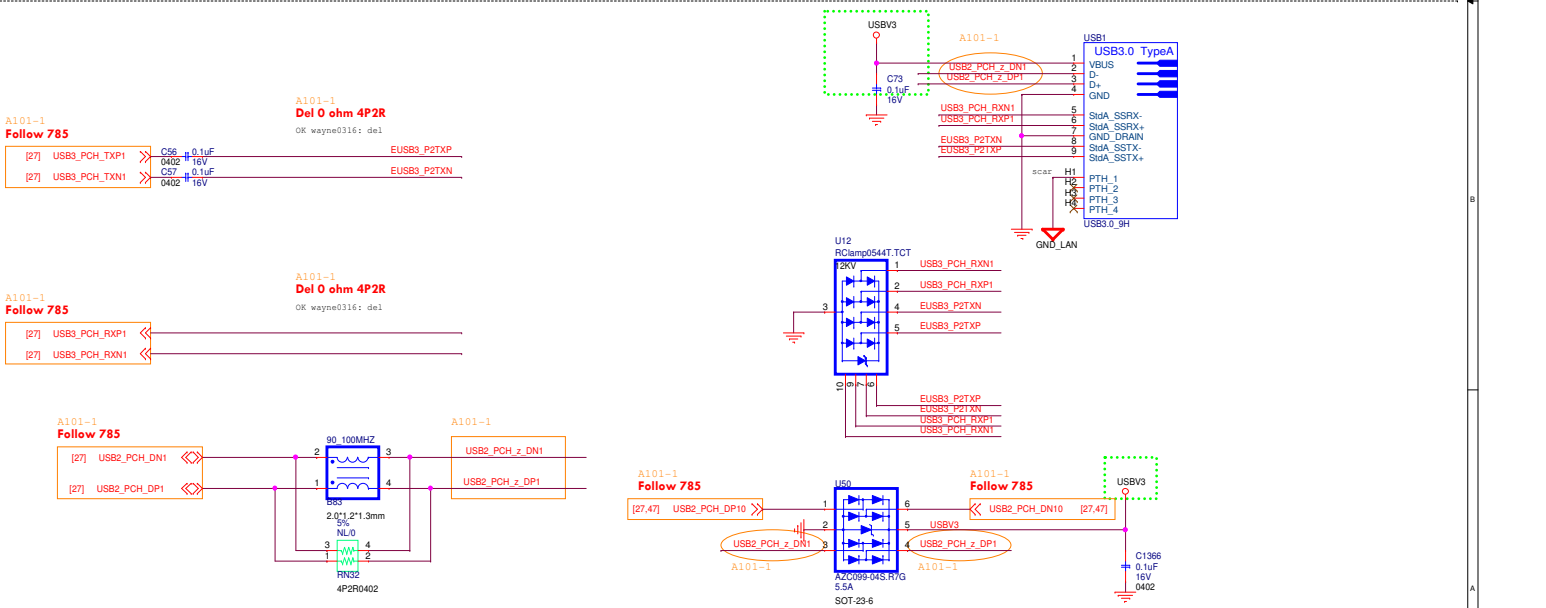
Title	CONN LAN12	
Size	Document Number: PCE-3029/PCE-4129	Rev: A101-2
Date: Monday, December 07, 2015	Sheet 45 of 55	





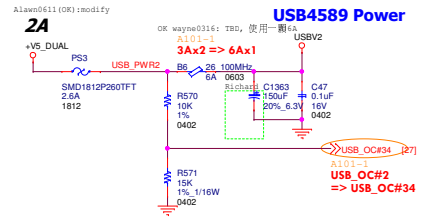


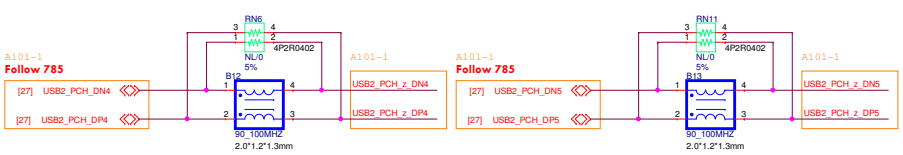
USB3 3.0 REAR I/O TYPE A

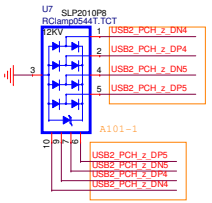


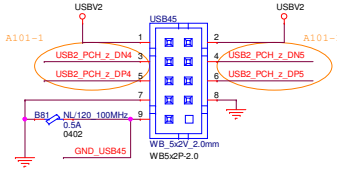
ADVANTECH		
Title	CONN USB3.0	
Size	Document Number PCE-3029/PCE-4129	Rev A101-2
Date: Monday, December 07, 2015	Sheet 46 of 55	

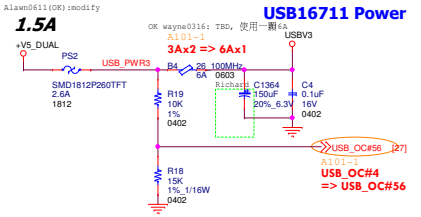
USB456789 2.0 PIN HEADER

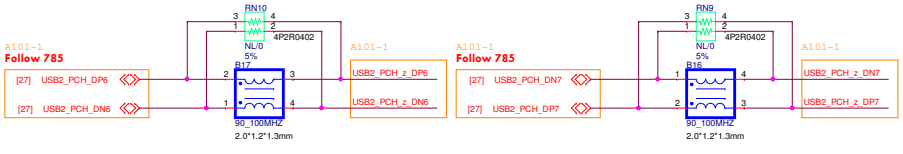


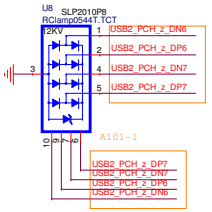


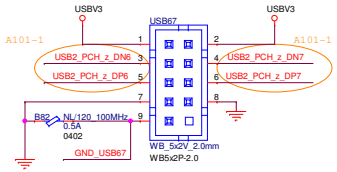


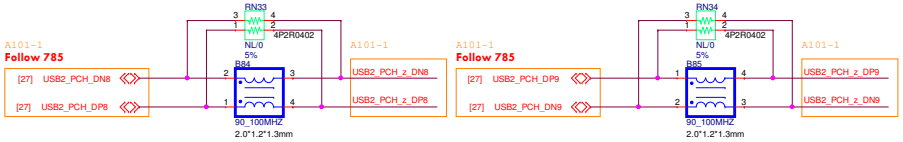


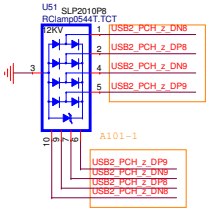


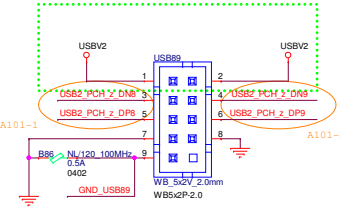




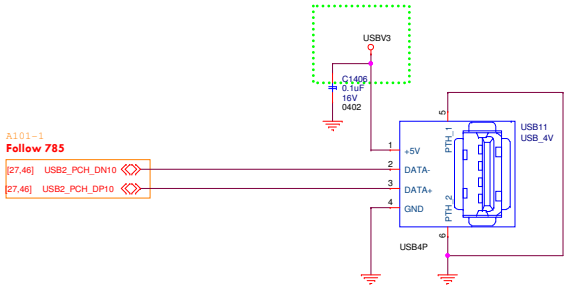






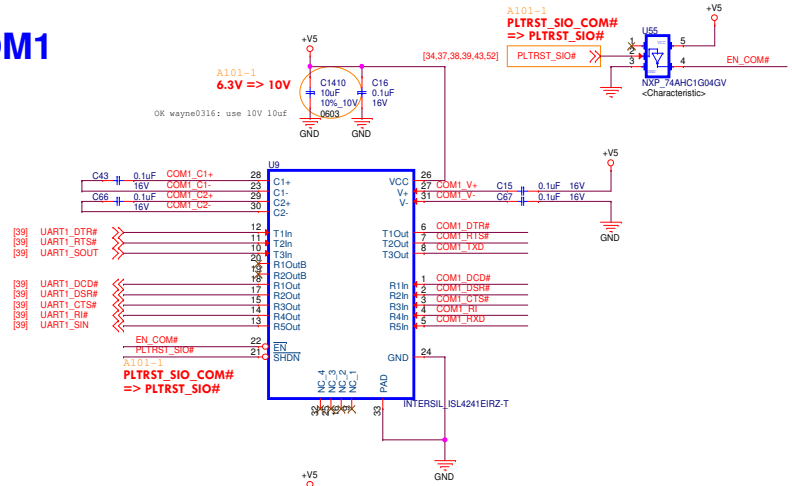


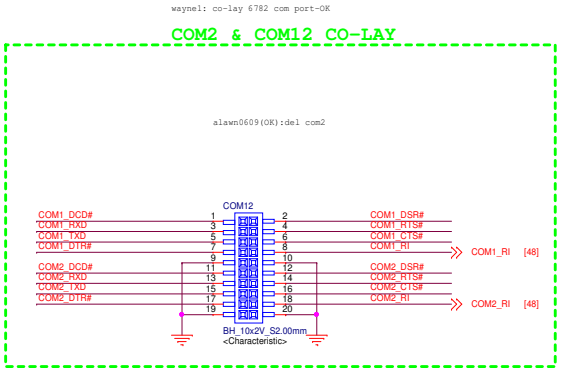
USB11 2.0 INNER TYPE A



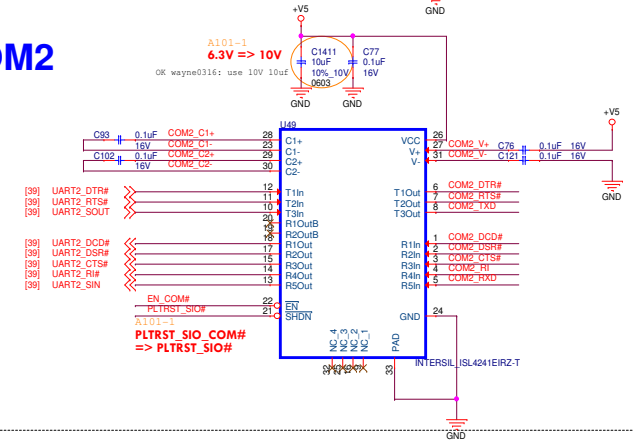
ADVANTECH		
Title	CONN USB2.0	
Size	Document Number	Rev
	PCE-3029/PCE-4129	A101-2
Date: Monday, December 07, 2015	Sheet 47 of 55	

COM1

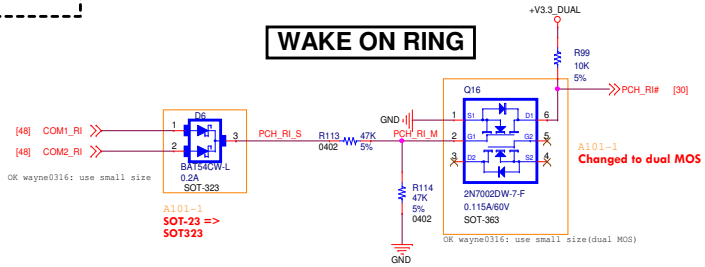




COM2



WAKE ON RING

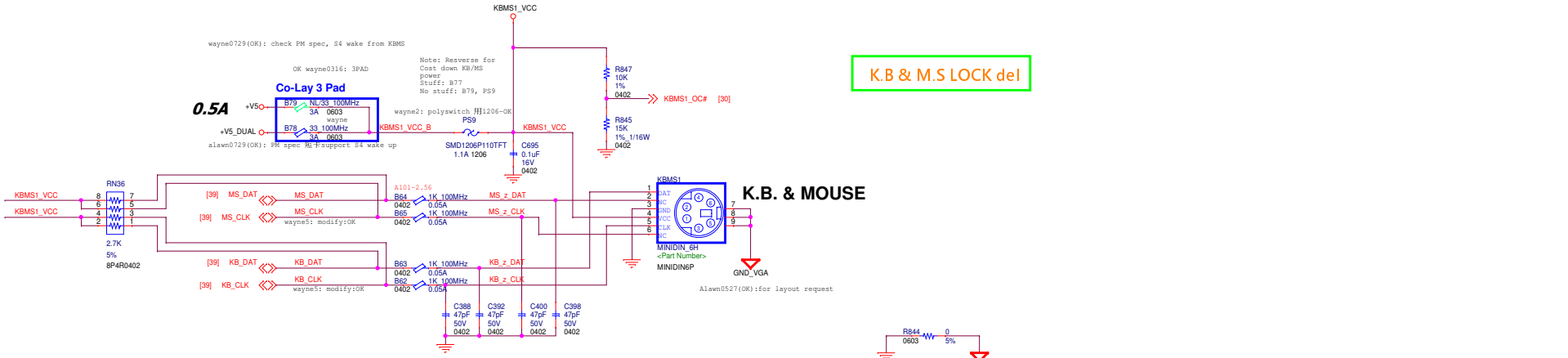


VGA from PCH

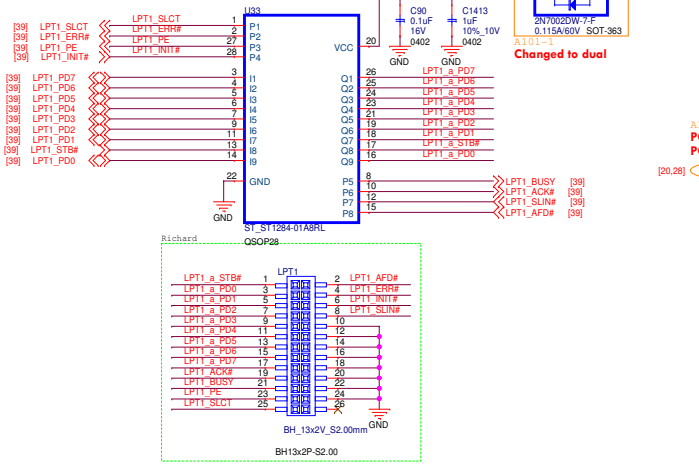
A101-1
Del 4128 VGA

ADVANTECH			
Title: CONN COM 1-2			
Size	Document Number: PCE-3029/PCE-4129		Rev: A101-2
Date: Monday, December 07, 2015	Sheet 48 of 55		

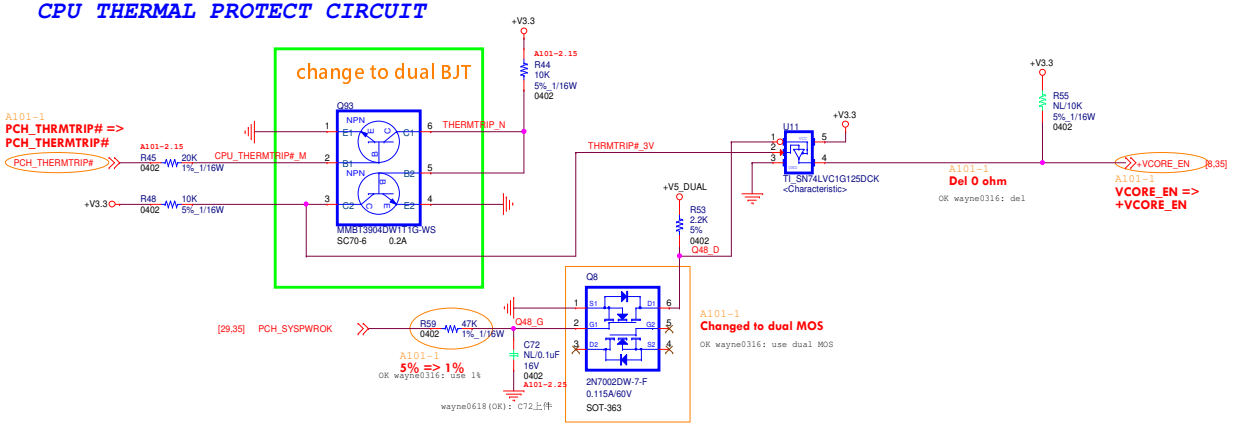
K.B. & M.S.



Printer Port

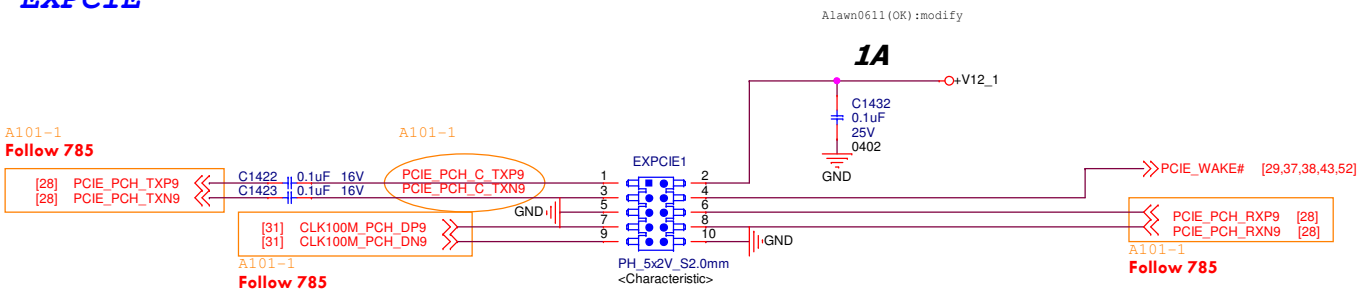


CPU THERMAL PROTECT CIRCUIT

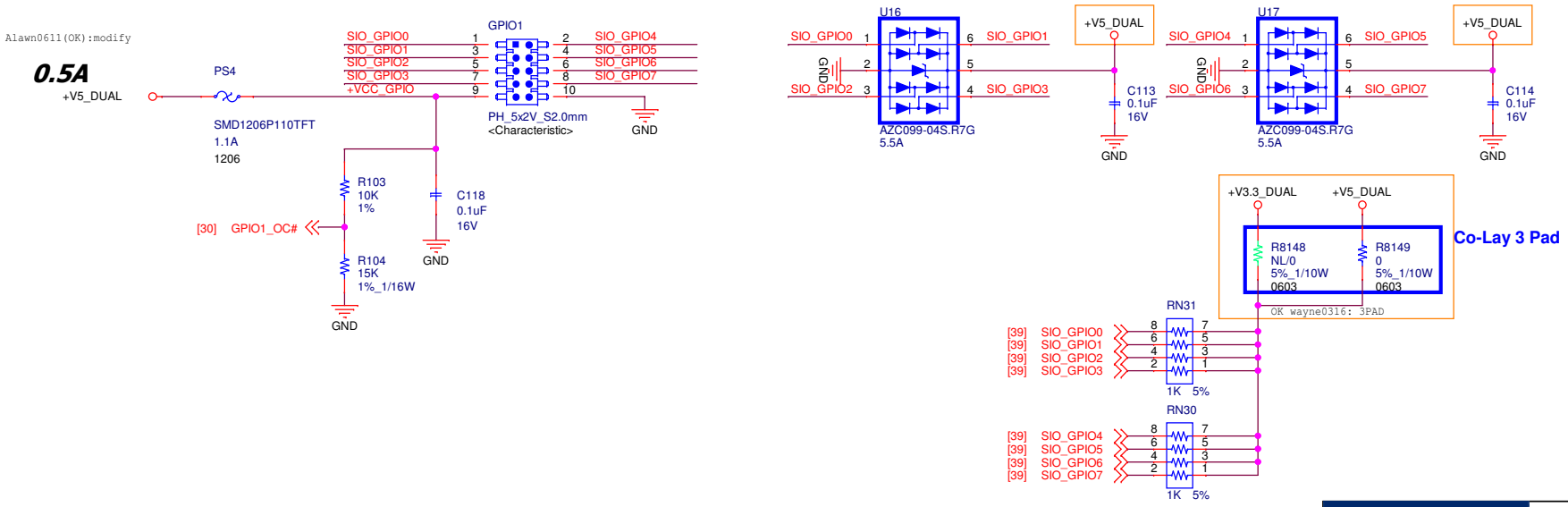


ADVANTECH			
Title	CONN KB&MS/LPT/THERMALTRIP		
Size	Document Number	PCE-3029/PCE-4129	Rev A101-2
Date: Monday, December 07, 2015	Sheet 49 of 55		

EXPCIE

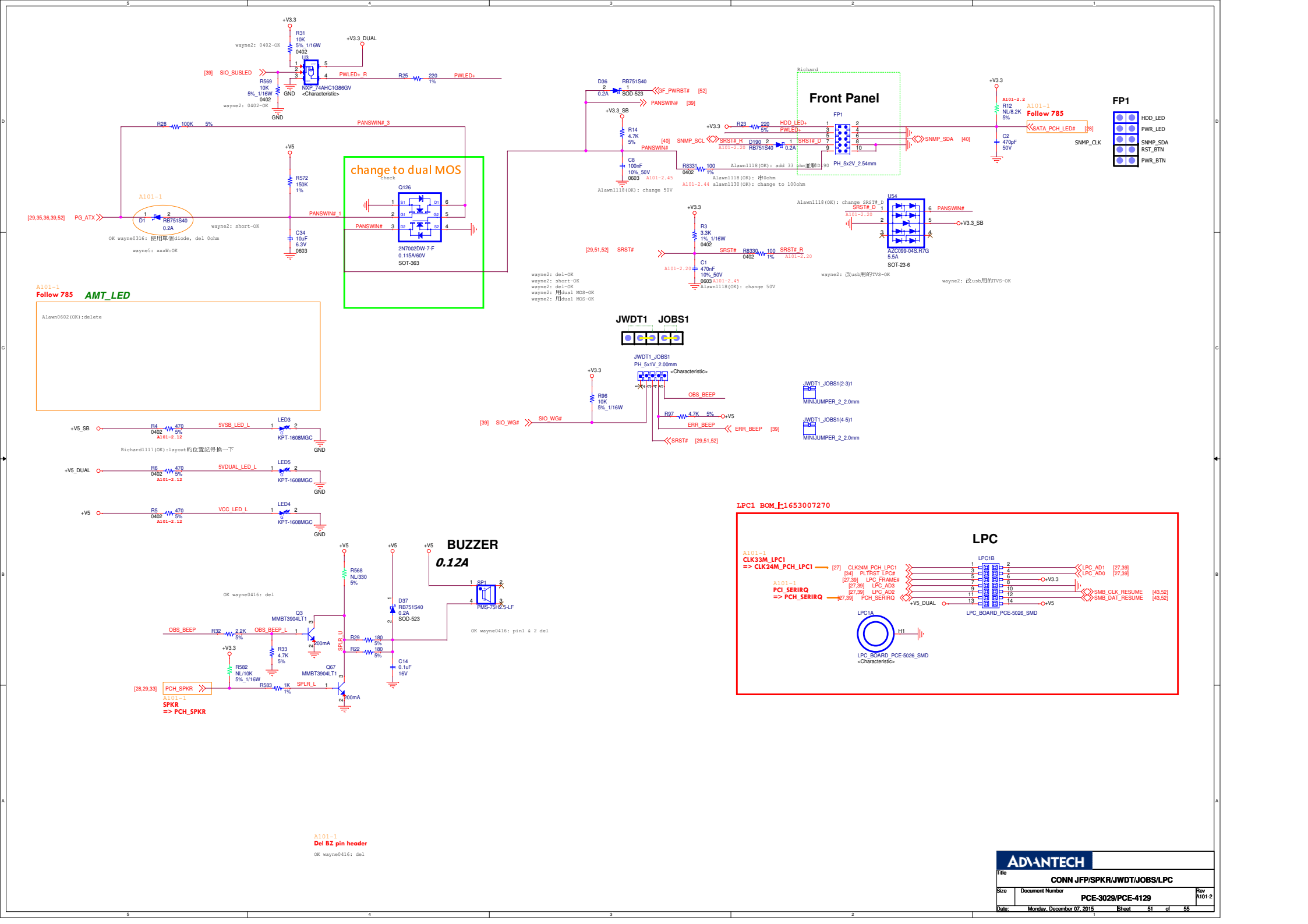


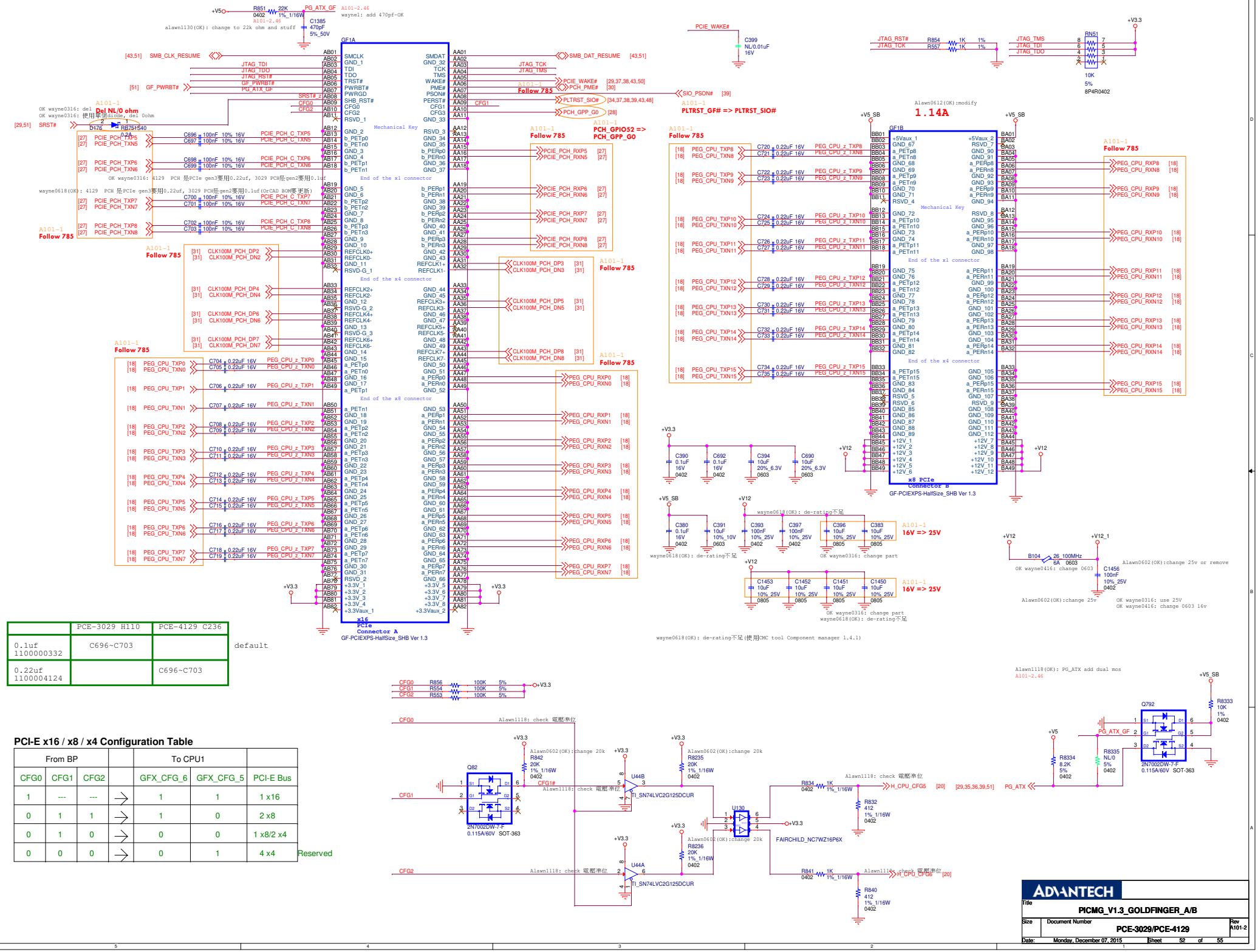
GPIO



ADVANTECH

Title	GPIO/EXPCIE1	
Size	Document Number: PCE-3029/PCE-4129	Rev: A101-2
Date: Monday, December 07, 2015	Sheet 50 of 55	


Front Panel
FP1
change to dual MOS
AMT_LED
JWDT1 JOBS1
BUZZER
0.12A
LPC
LPC1 BOM P:1653007270
Del BZ pin header
CONN JFP/SPKR/JWDT/JOBS/LPC
PCE-3029/PCE-4129
Monday, December 07, 2015



	PCE-3029 H110	PCE-4129 C236	
0.1uf 1100000332	C696~C703		default
0.22uf 1100004124		C696~C703	

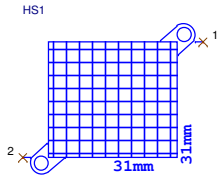
PCI-E x16 / x8 / x4 Configuration Table

From BP				To CPU1		
CFG0	CFG1	CFG2		GFX_CFG_6	GFX_CFG_5	PCI-E Bus
1	---	---	→	1	1	1 x16
0	1	1	→	1	0	2 x8
0	1	0	→	0	0	1 x8/2 x4
0	0	0	→	0	1	4 x4

Reserved

Title	PICMG_V1.3_GOLDFINGER_A/B	
Size	Document Number	Rev
	PCE-3029/PCE-4129	A101-2
Date: Monday, December 07, 2015	Sheet 52 of 55	

PCH Heatsink

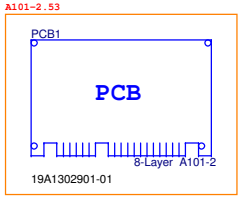


HEATSINK FWA-5285TS

PCB

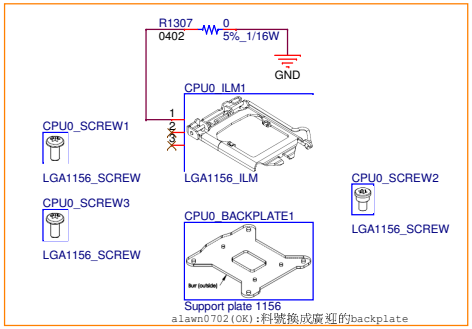
A101-1
Updated

A101-2.53

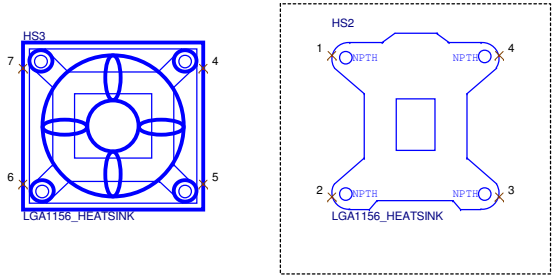


ILM + BP

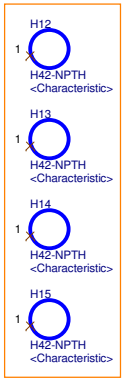
A101-1
Follow 785



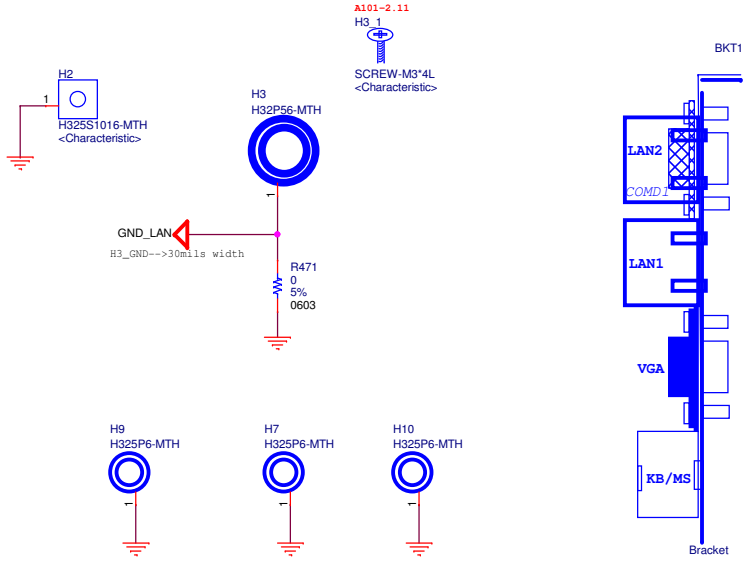
ILM + BP KEEP OUT ZONE



A101-1
Add



BKT & SCREW HOLE

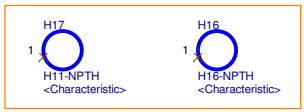


FM

A101-1
Add

Alawn0604(OK):delete FM5~8

A101-1
Add



For DIMMA1

For DIMMB1

ADVANTECH

Title	OTHER BOM	
Size	Document Number: PCE-3029/PCE-4129	Rev: A101-2
Date: Monday, December 07, 2015	Sheet 53 of 55	

PCH GPIO LIST

ADVANTECH

Title	PCH GPIO LIST	
Size	Document Number: PCE-3029/PCE-4129	Rev: A101-2
Date: Tuesday, December 01, 2015	Sheet 54 of 55	

Revision History

ECOP-107468 REV: A101-1 PCB:19A1302900-01(8 Layer) RD: Alawn.Lee 2015/3/18

ECOP-XXX A101-2 PCB: 19A1302901-01 (8 Layer) RD: Alawn.lee 2015/11/15

1. BOM: remove R7870 -->R7870重複上件
2. BOM: remove R12 -->R12重複PU
3. Sch: 修改文字面 -->修改文字面
4. BOM: Remove C7276, C7248, C7333 -->開幾卡55
5. Sch: add R8316, and C556, C557 change to 8pF, Y1 change to 1231003137-01 -->VGA Cristal change to Epson
6. BOM: Add P/N:1654002538 -->mini-pcie forget to stuff
7. BOM: Add Q131 -->DVI: Q131 forget to stuff
8. BOM: reserve R507 -->Audio: change net name to VDDIO_SEL and connect to gnd
9. Sch: SATA_PCH_RXN4/SATA_PCH_RXP4 change -->signal 正負反接
10. FUNC: Remove R8294, Add R8295 -->NXP IC內部已有假負載設計
11. DFM: Ref name RO1 change to H3_1 -->DFM check
12. BOM: R4, R5, R6 change to 330ohm ~470ohm -->Reduce LED current
13. Sequence: del R810, Reserve D188 -->AT power on: +VCORE_EN has two stage
14. Sch: add new Board ID -->區分PCE-4129 mini-pcie SKU
15. Sequence: R44~10k, R45~20k, R7753~330 -->THERMAL PROTECT 分壓異常
16. Sequence: +V0.95_VCCIO Enable add D187 Vcore_PG -->Make VCCIO start to work after VR ready
17. Sequence: PCH_PWROK enable add +V0.95_VCCIO_PG(add D189), and reserve PCH_SLP_S3#_BUFF(Reserve D191) -->To delay PCH_PWROK
18. Sch: add SIO_RSMRST# From SIO add R8318, Reserve R8319 (Remove R8093, R8095) -->modify SIO_RSMRST# circuit
19. Power: R8221 change to 100k, and stuff R46, C7329 -->Power DDR_VTT finetune
20. FUNC: add D190, R8330, U54 net change to SRST#_D, Change R3 to 3.3k, and C8 change to 470n -->阻擋治具 On/off glitch 干擾 reset pin
21. Sch: Remove D174 -->Fan: no need
22. Sequence: Remove R859, D155, and R1744 change to Vcore_PG -->Dual Power Rail Switching power on切換太晚
23. Sch: Cancel -->Cancel
24. BOM: C147, C512 change from 22uF to 10uF -->22uF 0603 Package de-rating不足
25. Sequence: Remove C72 -->Power off: +VCORE_EN has two stage
26. Sequence: R8087 PU change to +V3.3 -->PCH_PLTRST# has glitch
27. Sequence: C7521 change to 2.2uF -->delay +V1.0_dual Enable
28. Signal: add R8263, R8265, R8266: 220ohm -->Fine tune DVI eye diagram
29. Sequence: remove R8200 -->PWRGD_+V0.95_VCCIO enable不須做分壓
30. Sequence: C7441 change to 0.47uF -->+V0.95_VCCIO Rising time縮短為5ms
31. Sch: Add Q790, R8329 -->Monitor 漏電到DP2
32. BOM: crystal: C7339, c7440~15p , C7338~12p -->參考EPSON測試結果修改
33. BOM: Add R8320, Remove R7630 -->+VCORE_PG改PU+V3.3, 避免glitch
34. Power: R7599, R7603, R7608, R7593, R7595, R7606~750, R7652, R7655, R7658, R7664, R7667, R7661~0 -->VRTT change list
35. Sch: Q24 change to 1310003822 -->Rdson較小, 3.5 mΩ at VGS = 4.5 V, ID = 19 A
36. BOM: Stuff R8219, C7543 -->+V1.2_DDR_PG Pull High (Remove PWR [CPU_VCCPLL_OC])
37. BOM: Remove C7137, C7138, C7142, C7143, C7147, R7705, R7707, U127 -->PWR [CPU_VCCPLL_OC] no use
38. Sch: C7447 change to 10uF , add D192 -->Reserve PWRGD_+V0.95_VCCIO delay circuit
39. Sch: net name +V3.3_RTC~+V3_RTC -->modify net name
40. Sch: Del Q48, R8097, R8099, C7370, R8096, R8098 -->RSMRST# Remove no need circuit
41. Sch: del D169, add D193 -->del EN_VCCIO, so change to single diode
42. Sch: Add B162~B165, RN59~62 -->DVI: Add common mode choke
43. Sch: B100, B103 change package to 0603 -->change small package
44. Sch: Add R8331 -->Reserve PANSWIN# delay circuit
45. Sch: C1, C8 package change to 0603 -->increase derating to 50V
46. Sch: Add Q792, R8333, R8334, Reserve R8335, stuff R851 -->Add dual mos to separate Power Supply PG
47. Sch: Q71 from 1310003892 change to 1310003353 -->Drain Current is larger than 1310003892
48. BOM: Cancel -->Cancel
49. BOM: U57 from 1410025762-01 change to 1410025762-11 -->INFINEON_PXC1331ADN change version from B11 change to B12
50. Sch: Cancel -->Cancel
51. Sch: add R8336, Remove R8220 -->+V1.2_DDR_TPS51216_S3 PU change to 3.3_dual
52. Sch: Reserve R8337, Remove R8300, stuff R7698, R8251, and R7699 change to 0ohm, Q754 change to MOS -->Remove CPU_DDR_VTT_CNTL and change to EN_VR_R
53. BOM: PCB Part number 19A1302901-01 -->PCB version
54. Sch: Del DP1, R1717, R1718, R1721, R1722, C1418, C1419, B102 -->Del DP1 Connector
55. Sch: Del DVI2, R1693~R1700, Q132, R1678, R1679, R1723, R1724, PS12, B100, R1676, R1677 -->Del DVI2 Connector
56. Sch: B62~B64 package change to 0402 -->change small package
57. Sch: R8162 Change PU to +V3.3 -->Del DVI2 so no need DVI2_OC#
58. Sch: Remove R8167 -->PECI no use in HWM
59. Sch: add R8338, R8339 -->XTAL24M_PCH reserve 0 ohm resistor
60. Sch: add D194 -->+VCORE_EN, EN_VCCIO reserve discharge circuit
61. Sch: change to 2.2ohm -->降低1.2DDR MOS切換速度,
62. Sch: Remove R8196, R8197 -->Remove +V0.95_VCCIO_SENSE to CPU
63. Sch: net name +VCC_DP2~+V3.3_DP1, DP2~DP1 -->change net name
64. Sch: net name +VCC_DP1~+V5_DVI -->change net name
65. Sch: C7542 from 0.22uF change to 0.47uF -->Delay +Vcore_EN
66. Sch: Del R7871~R7874 and move C413~C416 to replace -->功能重複
67. BOM: C176, C169, C1407, C1394 change to 10uF -->22uF 0603 Package de-rating不足
68. BOM: Stuff R8241, R8239, Remove U131, R8310 -->SIO_RSMRST# need to Pull High

ADVANTECH

Title	HISTORY RECORDS	
Size	Document Number	Rev
	PCE-3029/PCE-4129	A101-2
Date: Monday, December 07, 2015	Sheet 55 of 55	