Performance Monitoring

Chris Dahnken

Intel SSG EMEA HPCTC

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Optimization Notice

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Notice revision #20101101

Performance Monitoring

The Performance Monitoring Unit (PMU)

Ways to measure performance

- time – the ultimate measure!
- gprof – break down execution time on a functional level. Careful, changes execution time!
- counter monitoring – hardware supported measurement that allows to determine which hardware component or functional unit is under stress or starves. Doesn't change exec time!

Performance Counter Monitoring

- Performance counter monitoring is a HW supported method count events appearing in the hardware
- Events are situations the HW designers allow us to see. E.g. the CPU could experience “I tried to load data, but it was not in the last level cache” (aka a LLC cache miss). This is an event that can be measured.

Command line perf monitoring

Architectural perf events

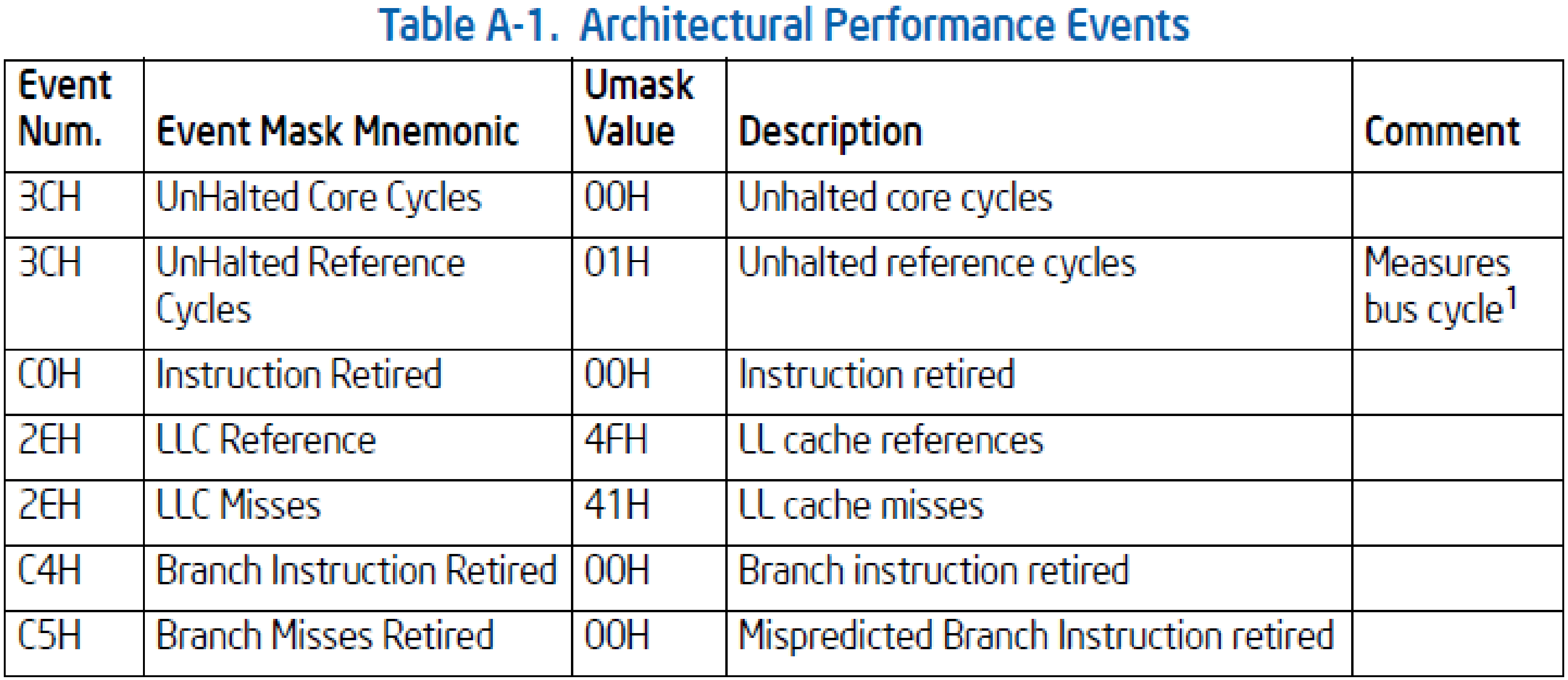


Table A-1. Architectural Performance Events

Event Num.	Event Mask Mnemonic	Umask Value	Description	Comment
3CH	UnHalted Core Cycles	00H	Unhalted core cycles	
3CH	UnHalted Reference Cycles	01H	Unhalted reference cycles	Measures bus cycle[1]
C0H	Instruction Retired	00H	Instruction retired	
2EH	LLC Reference	4FH	LL cache references	
2EH	LLC Misses	41H	LL cache misses	
C4H	Branch Instruction Retired	00H	Branch instruction retired	
C5H	Branch Misses Retired	00H	Mispredicted Branch Instruction retired	

There are another ~1000 non-architectural performance events!

Performance Counter Monitoring

- There are
  - 4 freely programmable
  - 3 fix function

  performance counter registers on current Intel CPUs
- There are 4 configuration registers, that let us specify which events are counted in the programmable counters
- There is 1 configuration register that lets us enable and disable performance monitoring.

Performance Counter Monitoring

Just in case: What is a register?

- A register is a series of latches (HW bits) with 64 bit width (some might differ, e.g. SSE) the CPU can access very quickly

- A Model Specific Register (MSR) is a register that is not guaranteed to be there in the next CPU!

Performance Counter Monitoring

How can I influence/change/write/read MSRs?

- MSRs can only be written in Ring 0 (supervisor mode). You can read MSRs as user.

You need to be

- root/sudoer to write

or

- a driver that does the access for you

Performance Counter Monitoring

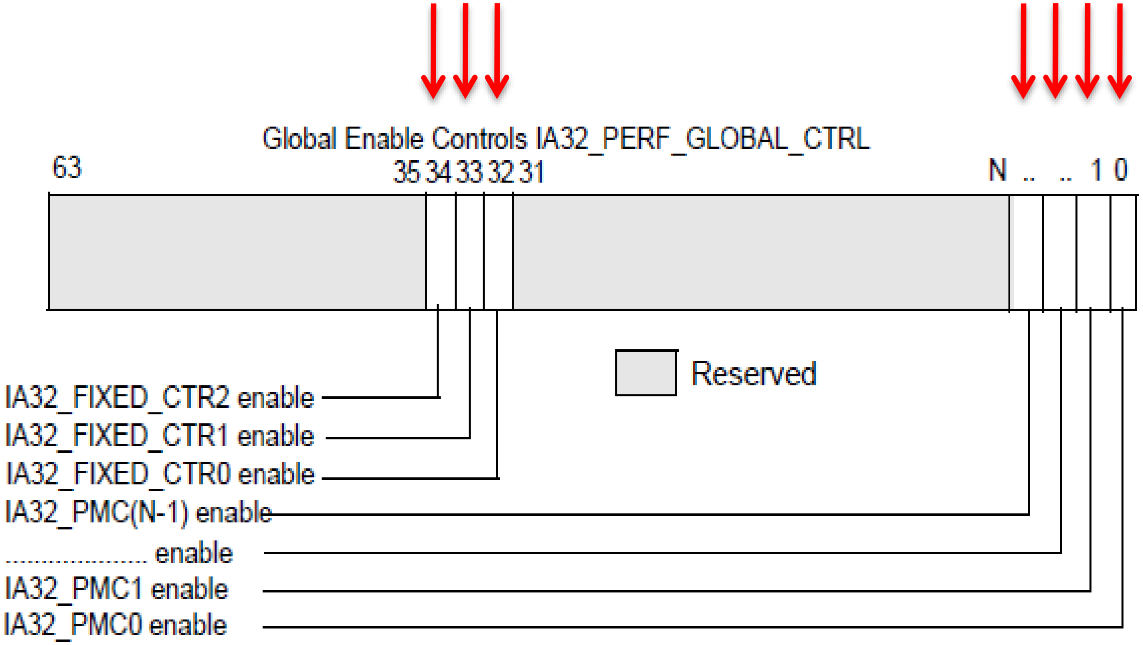
Software to read and write MSRs (linux)

- msr-tools package: rdmsr, wrmsr, msr.ko
- perf (linux system tool)
- Intel Vtune, Amplifier XE, PTU (http://software.intel.com/en-us/articles/intel-vtune-amplifier-xe/)
- Oprofile (http://oprofile.sourceforge.net/news/)
- Likwid (http://code.google.com/p/likwid/)

PMU MSRs

Control Registers

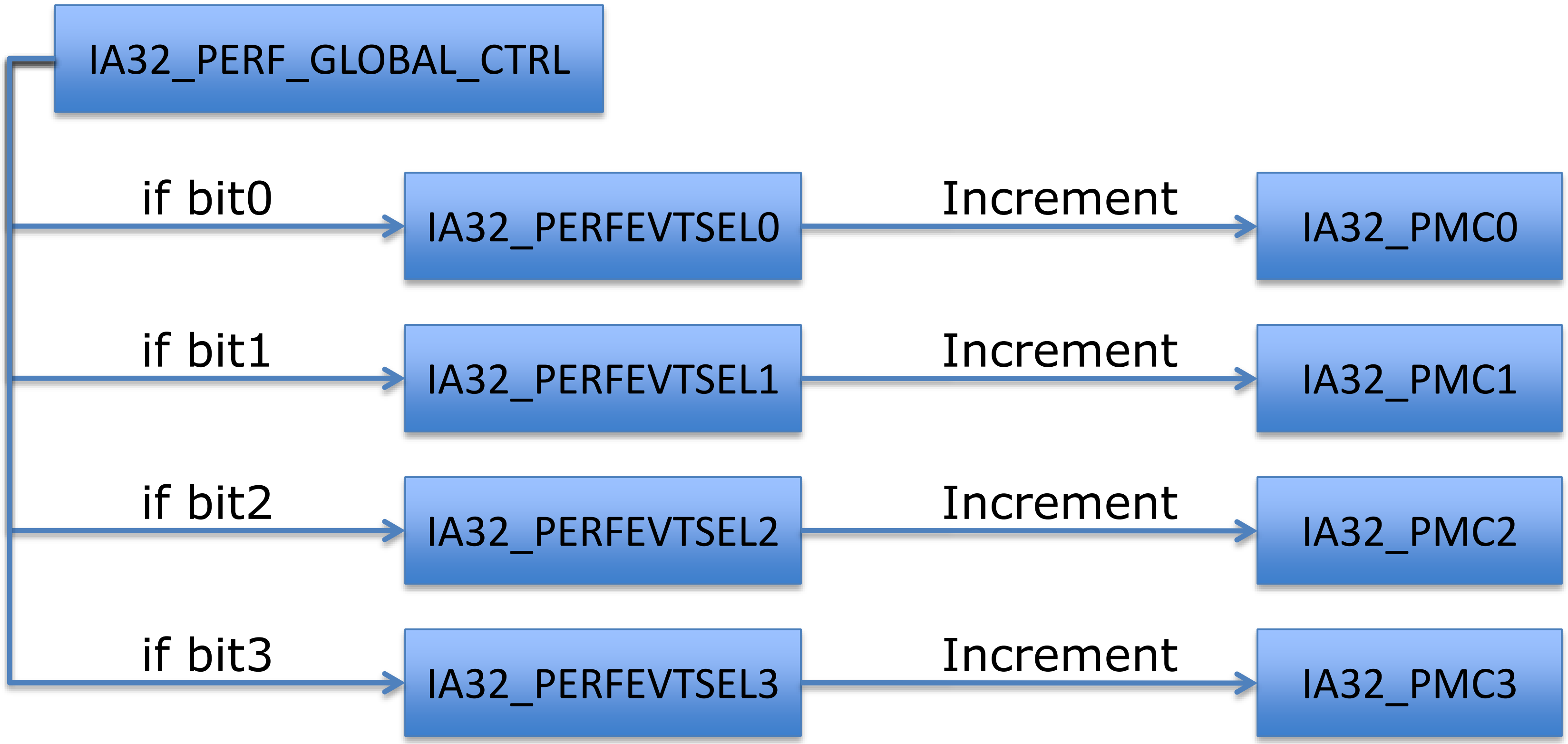
- IA32_PERF_GLOBAL_CTRL (0x38F/911)



```
wrmsr 911 –d 30064771087
```

PMU MSRs

General purpose performance counters



IA32_PERF_GLOBAL_CTRL

if bit0 → IA32_PERFEVTSEL0 → Increment → IA32_PMC0

if bit1 → IA32_PERFEVTSEL1 → Increment → IA32_PMC1

if bit2 → IA32_PERFEVTSEL2 → Increment → IA32_PMC2

if bit3 → IA32_PERFEVTSEL3 → Increment → IA32_PMC3

IA32_PERFEVTSELx specifies the number of the event to be obeserved (and a number of modifiers)

PMU MSRs

Selecting events

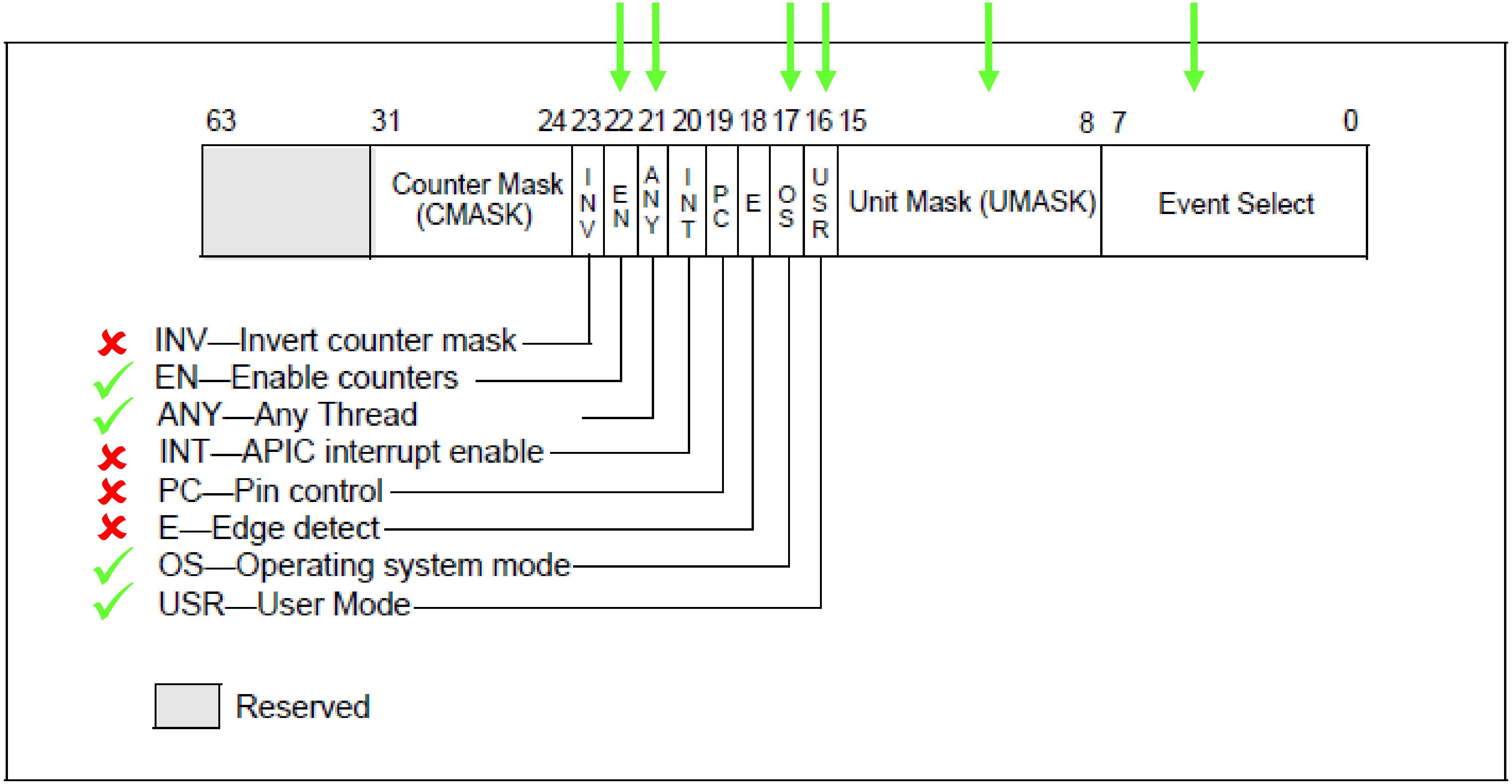


Figure 30-6. Layout of IA32_PERFEVTSELx MSRs Supporting Architectural Performance Monitoring Version 3

PMU MSRs

Selecting general purpose events

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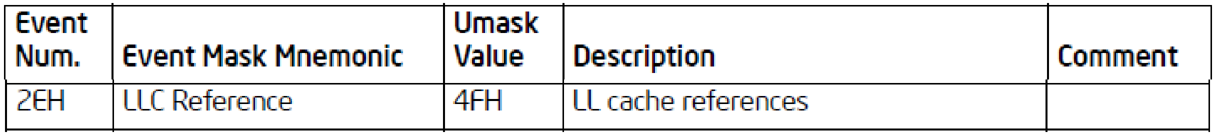
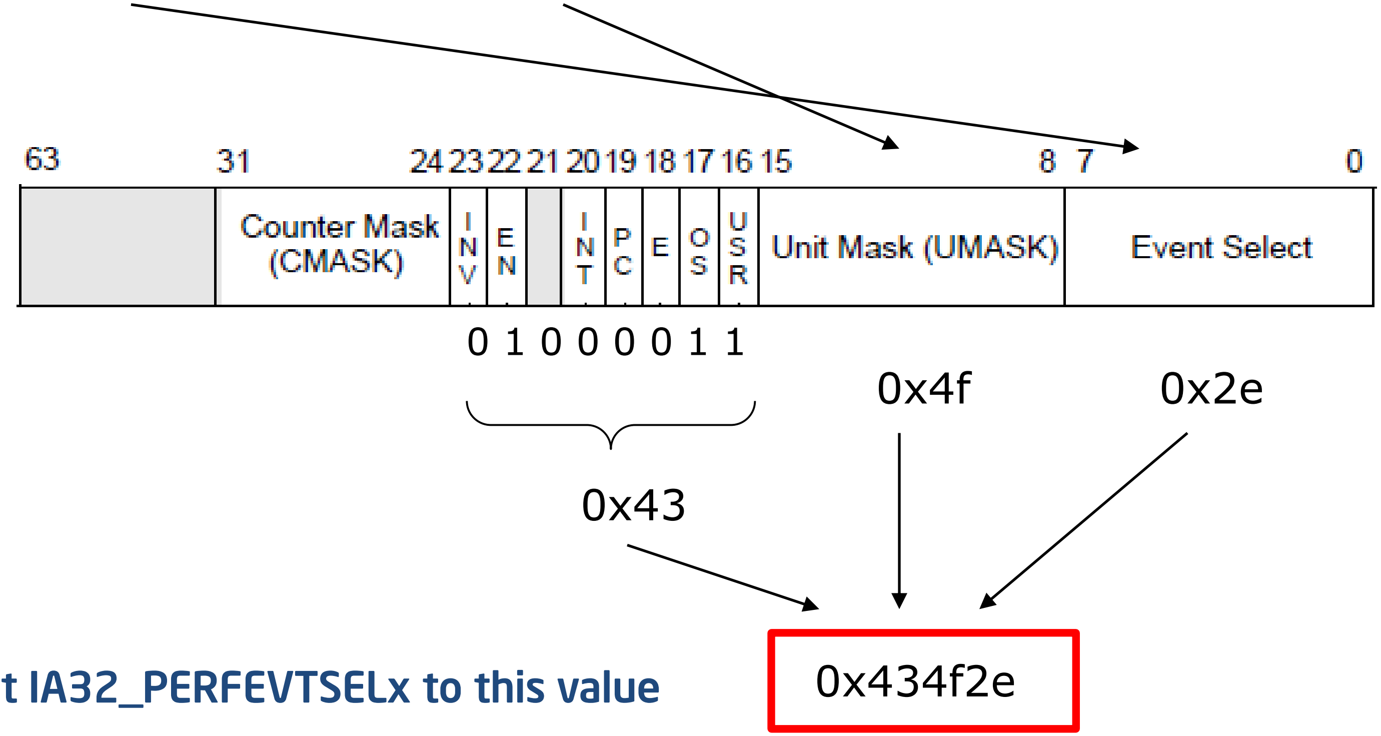
Volume 3B: System Programming Guide, Part 2



Event Num.	Event Mask Mnemonic	Umask Value	Description	Comment
2EH	LLC Reference	4FH	LL cache references	



Set IA32_PERFEVTSELx to this value

PMU MSRs

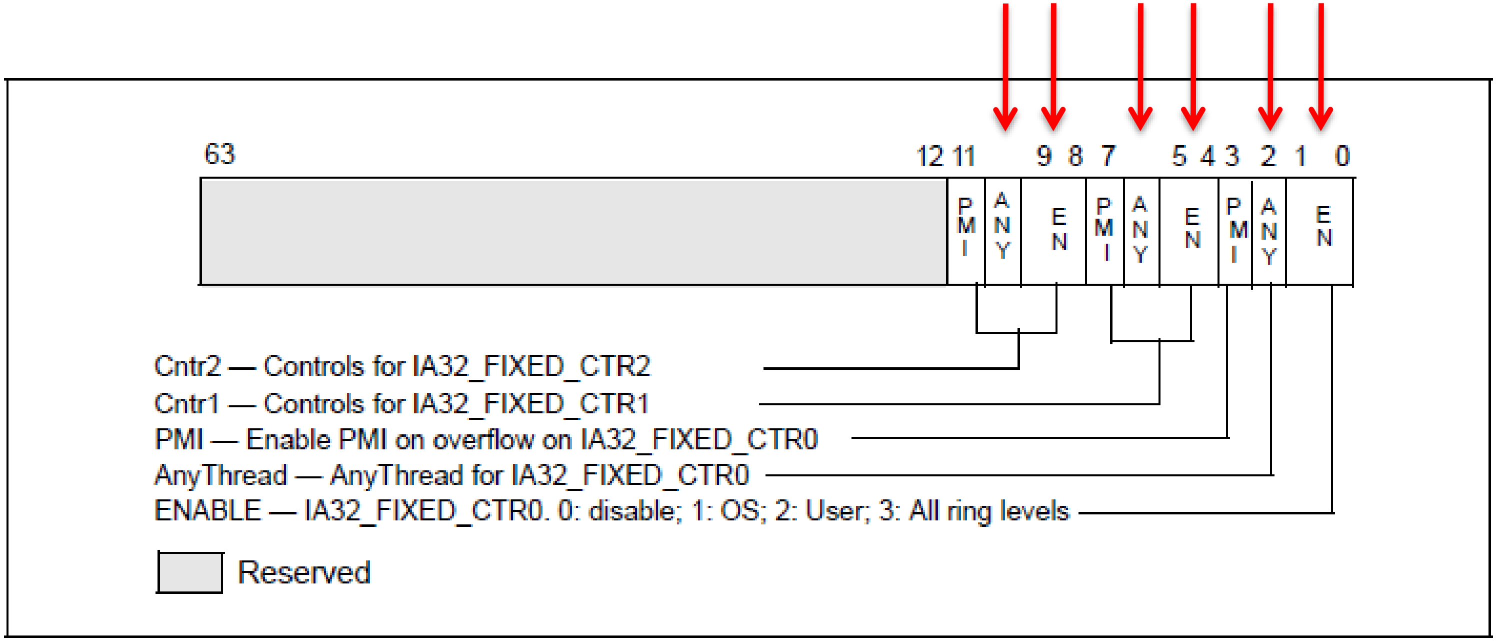
Fixed function performance counters

Additionally to the 4 freely programmable performance counters Nehalem (and later CPUs) offer three fixed function performance counters that will observe

- Instructions Retired
- CPU Cycles
- Reference CPU Cycles

PMU MSRs

Fixed function performance counters



Cntr2 — Controls for IA32_FIXED_CTR2

Cntr1 — Controls for IA32_FIXED_CTR1

PMI — Enable PMI on overflow on IA32_FIXED_CTR0

AnyThread — AnyThread for IA32_FIXED_CTR0

ENABLE — IA32_FIXED_CTR0. 0: disable; 1: OS; 2: User; 3: All ring levels

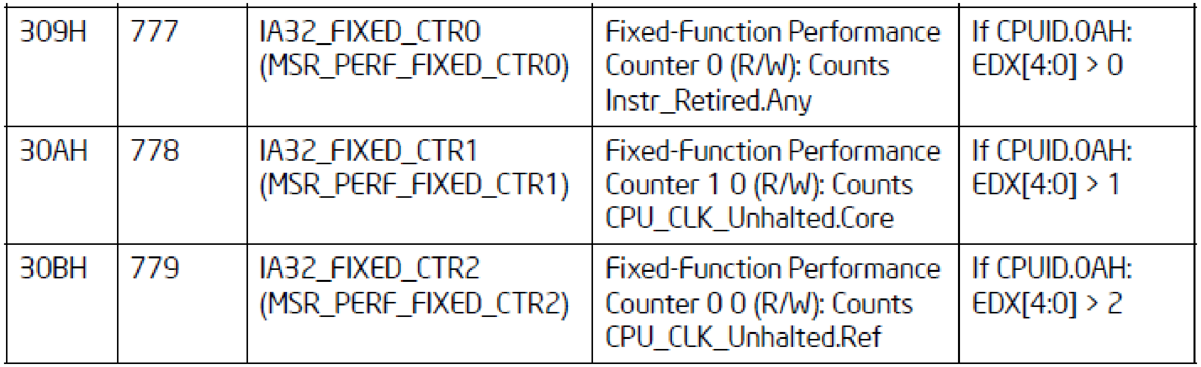
▢ Reserved

Figure 30-7. Layout of IA32_FIXED_CTR_CTRL MSR Supporting Architectural Performance Monitoring Version 3

PMU MSRs

Fixed function performance counters

- Event counts can now be seen in
- IA32_FIXED_CTR0: Instructions Retired
- IA32_FIXED_CTR1: Unhalted CPU Cycles
- IA32_FIXED_CTR2: Reference CPU Cycles



309H	777	IA32_FIXED_CTR0 (MSR_PERF_FIXED_CTR0)	Fixed-Function Performance Counter 0 (R/W): Counts Instr_Retired.Any	If CPUID.0AH: EDX[4:0] > 0
30AH	778	IA32_FIXED_CTR1 (MSR_PERF_FIXED_CTR1)	Fixed-Function Performance Counter 1 0 (R/W): Counts CPU_CLK_Unhalted.Core	If CPUID.0AH: EDX[4:0] > 1
30BH	779	IA32_FIXED_CTR2 (MSR_PERF_FIXED_CTR2)	Fixed-Function Performance Counter 0 0 (R/W): Counts CPU_CLK_Unhalted.Ref	If CPUID.0AH: EDX[4:0] > 2

PMU MSRs

Summary

- Intel CPUs can monitor particular events during execution
- 4 freely programmable counters and 3 fixed function counters measure the occurrence of the given events at the same time
- In order observe event counts
  - Enable event monitoring in the control register
  - Program the event into the event select register
  - Reset/Read the count from the counter register
- READ: 253669 - Intel 64 and IA-32 Architectures Software Developers Manual Volume 3B System Programming Guide Part 2

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Software

Appendix

Command line performance monitoring

Command line perf monitoring

- With rdmsr and wrmsr we can now easily do performance monitoring in a lightweight way.
- Before going on to feature burden apps like Vtune, let’s now do a quick performance analysis directly from the command line

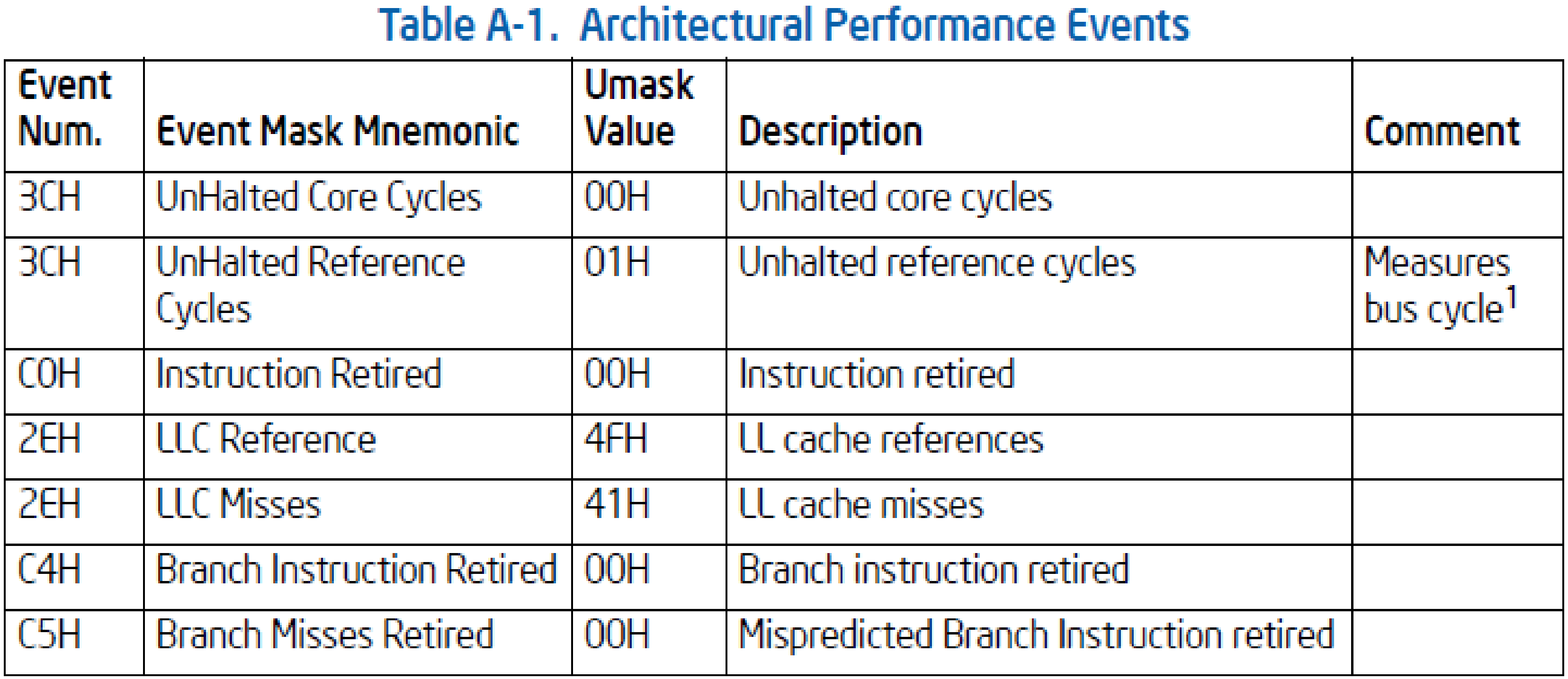
Command line perf monitoring

Architectural perf events

- Intel doesn’t guarantee the consistency of the performance monitoring unit
- Events can change with each model
- There are a number of events that Intel guarantees always to be present
- These are called Architectural performance events

Command line perf monitoring

Architectural perf events



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Command line perf monitoring

Architectural perf events

```
for c in 0 1 2 3; do
#Enable perf mon in IA32_PERF_GLOBAL_CTRL
 wrmsr -p $c 911 30064771087
#Enable fixed perf m. in IA32_FIXED_CTR_CTRL
 wrmsr -p $c 909 819
#IA32_PERFEVTSEL0(390 dec) for total branches
 wrmsr -p $c 390  0x4700c4
 #IA32_PERFEVTSEL1 (391 dec) for branch miss.
 wrmsr -p $c 391  0x4700c5
done
```

Command line perf monitoring

Architectural perf events

```
while[ 1 ]; do
  for c in 0 1 2 3; do
    wrmsr -p $c  193 0  #reset counter 0
    wrmsr -p $c  194 0  #reset counter 1
  done
  sleep 5
  for c in 0 1 2 3; do
   BRREF=`rdmsr -p $c  193` #read counter 0
   BRMISS=`rdmsr -p $c  194` #read counter 1
   echo $c `echo $BRMISS/$BRREF | bc -l`
  done
done
```

Command line perf monitoring

Advanced Example

```
proc   CPI        LLC misses    Branch misspred
----------------------------------------------------
0      1.35079      .30312        .00057
1      1.36037      .29671        .00082
2      1.35890      .30145        .00090
3      1.36869      .29146        .00049
4      1.36068      .29906        .00107
5      1.36653      .29260        .00047
6      1.35879      .30083        .00096
7      1.37438      .29364        .00044
```

app with cache blocking

```
proc   CPI        LLC misses    Branch misspred
----------------------------------------------------
0      .49865     .99099        .01582
1      .46621     .99247        .01260
2      .49805     .99210        .01281
3      .46907     .98990        .01363
4      .49935     .99038        .01508
5      .46850     .99154        .01374
6      .49610     .99049        .01602
7      .46863     .99231        .01207
```

app without cache blocking

Command line perf monitoring

Summary

- You can do this for all kind of events you are interested in
- Provides immediate feedback
- Ideal for first view assessments
- Ideal for command line work