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| Tool Version : Vivado v.2024.2 (win64) Build 5239630 Fri Nov 08 22:35:27 MST 2024
| Date         : Mon Jun  9 21:56:12 2025
| Host         : MACMINI running 64-bit major release  (build 9200)
| Command      : report_utilization -file SH2CPU_utilization_placed.rpt -pb SH2CPU_utilization_placed.pb
| Design       : SH2CPU
| Device       : xc7s25csga225-2
| Speed File   : -2
| Design State : Fully Placed
```

Utilization Design Information

Table of Contents

1. Slice Logic

Site Type	Used	Fixed	Prohibited	Available	Util%
Slice LUTs	2150	0	0	14600	14.73
LUT as Logic	2150	0	0	14600	14.73
LUT as Memory	0	0	0	5000	0.00
Slice Registers	975	0	0	29200	3.34
Register as Flip Flop	787	0	0	29200	2.70
Register as Latch	188	0	0	29200	0.64
F7 Muxes	257	0	0	7300	3.52
F8 Muxes	128	0	0	3650	3.51

* Warning! LUT value is adjusted to account for LUT combining.

1.1 Summary of Registers by Type

Total	Clock Enable	Synchronous	Asynchronous
0	_	-	-
0	_	-	Set
0	_	-	Reset
0	_	Set	-
0	_	Reset	-
0	Yes	-	-
3	Yes	-	Set
908	Yes	-	Reset
0	Yes	Set	-
64	Yes	Reset	-

2. Slice Logic Distribution

Site Type	Used	Fixed	Prohibited	Available	Util%
Slice	731	0	0	3650	20.03
SLICEL	483	0			
SLICEM	248	0			
LUT as Logic	2150	0	0	14600	14.73
using O5 output only	0				
using O6 output only	1641				
using O5 and O6	509				
LUT as Memory	0	0	0	5000	0.00
LUT as Distributed RAM	0	0			
using O5 output only	0				
using O6 output only	0				
using O5 and O6	0				
LUT as Shift Register	0	0			
using O5 output only	0				
using O6 output only	0				
using O5 and O6	0				
Slice Registers	975	0	0	29200	3.34
Register driven from within the Slice	401				
Register driven from outside the Slice	574				
LUT in front of the register is unused	147				
LUT in front of the register is used	427				
Unique Control Sets	47		0	3650	1.29

* * Note: Available Control Sets calculated as Slice * 1, Review the Control Sets Report for more information regarding control sets.

3. Memory

Site Type	Used	Fixed	Prohibited	Available	Util%
Block RAM Tile	0	0	0	45	0.00
RAMB36/FIFO*	0	0	0	45	0.00
RAMB18	0	0	0	90	0.00

* Note: Each Block RAM Tile only has one FIFO logic available and therefore can accommodate only one FIFO36E1 or one FIFO18E1. However, if a FIFO18E1 occupies a Block RAM Tile, that tile can still accommodate a RAMB18E1

4. DSP

Site Type	Used	Fixed	Prohibited	Available	Util%
DSPs	0	0	0	80	0.00

5. IO and GT Specific

Site Type	Used	Fixed	Prohibited	Available	Util%
Bonded IOB	75	0	0	150	50.00
IOB Master Pads	36				
IOB Slave Pads	37				
Bonded IPADs	0	0	0	2	0.00
PHY_CONTROL	0	0	0	3	0.00

PHASER_REF	0	0	0	3	0.00
OUT_FIFO	0	0	0	12	0.00
IN_FIFO	0	0	0	12	0.00
IDELAYCTRL	0	0	0	3	0.00
IBUFDS	0	0	0	144	0.00
PHASER_OUT/PHASER_OUT_PHY	0	0	0	12	0.00
PHASER_IN/PHASER_IN_PHY	0	0	0	12	0.00
IDELAYE2/IDELAYE2_FINEDELAY	0	0	0	150	0.00
ILOGIC	0	0	0	150	0.00
OLOGIC	0	0	0	150	0.00

6. Clocking

Site Type	Used	Fixed	Prohibited	Available	Util%
BUFGCTRL	4	0	0	32	12.50
BUFIO	0	0	0	12	0.00
MMCME2_ADV	0	0	0	3	0.00
PLLE2_ADV	0	0	0	3	0.00
BUFMRCE	0	0	0	6	0.00
BUFHCE	0	0	0	48	0.00
BUFR	0	0	0	12	0.00

7. Specific Feature

Site Type	Used	Fixed	Prohibited	Available	Util%
BSCANE2	0	0	0	4	0.00
CAPTUREE2	0	0	0	1	0.00
DNA_PORT	0	0	0	1	0.00
EFUSE_USR	0	0	0	1	0.00
FRAME_ECCE2	0	0	0	1	0.00
ICAPE2	0	0	0	2	0.00
STARTUPE2	0	0	0	1	0.00
XADC	0	0	0	1	0.00

8. Primitives

Ref Name	Used	Functional Category
LUT6	1229	LUT
FDCE	720	Flop & Latch
LUT3	580	LUT
LUT5	470	LUT
MUXF7	257	MuxFx
LUT4	217	LUT
LDCE	188	Flop & Latch
LUT2	155	LUT
MUXF8	128	MuxFx
FDRE	64	Flop & Latch
OBUF	41	IO
IBUF	34	IO
OBUFT	32	IO
CARRY4	28	CarryLogic

```
| LUT1     |    8 |                 LUT |
| BUFG     |    4 |               Clock |
| FDPE     |    3 |        Flop & Latch |
+----------+------+---------------------+


9. Black Boxes
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+----------+------+
| Ref Name | Used |
+----------+------+


10. Instantiated Netlists
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+----------+------+
| Ref Name | Used |
+----------+------+
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| Tool Version : Vivado v.2024.2 (win64) Build 5239630 Fri Nov 08 22:35:27 MST 2024
| Date : Mon Jun 9 21:56:31 2025
| Host : MACMINI running 64-bit major release (build 9200)
| Command : report_timing_summary -max_paths 10 -report_unconstrained -file SH2CPU_timing_summary_routed.rpt -pb SH2CPU_timing_summary_routed.pb -rpx SH2CPU_timing_summary_routed.rpx -warn_on_violation
| Design : SH2CPU
| Device : 7s25-csga225
| Speed File : -2 PRODUCTION 1.23 2018-06-13
| Design State : Routed

Timing Summary Report

| Timer Settings
| --------------

  Enable Multi Corner Analysis : Yes
  Enable Pessimism Removal : Yes
  Pessimism Removal Resolution : Nearest Common Node
  Enable Input Delay Default Clock : No
  Enable Preset / Clear Arcs : No
  Disable Flight Delays : No
  Ignore I/O Paths : No
  Timing Early Launch at Borrowing Latches : No
  Borrow Time for Max Delay Exceptions : Yes
  Merge Timing Exceptions : Yes
  Inter-SLR Compensation : Conservative

  Corner Analyze Analyze
  Name Max Paths Min Paths
  ------ --------- ---------
  Slow Yes Yes
  Fast Yes Yes

| Report Methodology
| ------------------

Rule	Severity	Description	Violations
TIMING-17	Critical Warning	Non-clocked sequential cell	787
TIMING-20	Warning	Non-clocked latch	188
LATCH-1	Advisory	Existing latches in the design	1

Note: This report is based on the most recent report_methodology run and may not be up-to-date. Run report_methodology on the current design for the latest report.

| Timing Details
| --------------

Path Group: (none)
From Clock:
  To Clock:

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Max Delay          2490 Endpoints
Min Delay          2490 Endpoints
--------------------------------------------------------------------------------


Max Delay Paths
--------------------------------------------------------------------------------
Slack:                    inf
  Source:                 Reset
                            (input port)
  Destination:            AB[30]
                            (output port)
  Path Group:             (none)
  Path Type:              Max at Slow Process Corner
  Data Path Delay:        34.814ns  (logic 8.859ns (25.446%)  route 25.955ns (74.554%))
  Logic Levels:           29  (CARRY4=1 IBUF=1 LUT3=5 LUT4=1 LUT5=16 LUT6=4 OBUF=1)

    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
  -------------------------------------------------------------------    -------------------
    K14                                               0.000     0.000 r  Reset (IN)
                         net (fo=0)                   0.000     0.000    Reset
    K14                  IBUF (Prop_ibuf_I_O)         0.886     0.886 r  Reset_IBUF_inst/O
                         net (fo=143, routed)         4.714     5.599    control_unit/Reset_IBUF
    SLICE_X5Y20          LUT5 (Prop_lut5_I0_O)        0.105     5.704 r  control_unit/PCReg[1]_i_5/O
                         net (fo=8, routed)           1.072     6.777    control_unit/PCReg[1]_i_5_n_2
    SLICE_X3Y22          LUT6 (Prop_lut6_I0_O)        0.105     6.882 r  control_unit/PCReg[1]_i_3/O
                         net (fo=2, routed)           0.671     7.553    control_unit/PCReg[1]_i_3_n_2
    SLICE_X3Y23          LUT3 (Prop_lut3_I0_O)        0.105     7.658 r  control_unit/PCReg[2]_i_6/O
                         net (fo=2, routed)           0.480     8.138    control_unit/pmau/SH2Pmau_Instance/acarry_2
    SLICE_X2Y24          LUT3 (Prop_lut3_I2_O)        0.125     8.263 r  control_unit/PCReg[3]_i_6/O
                         net (fo=2, routed)           0.379     8.642    control_unit/pmau/SH2Pmau_Instance/acarry_3
    SLICE_X2Y24          LUT3 (Prop_lut3_I2_O)        0.265     8.907 r  control_unit/PCReg[4]_i_6/O
                         net (fo=3, routed)           0.668     9.575    control_unit/pmau/SH2Pmau_Instance/acarry_4
    SLICE_X1Y24          LUT5 (Prop_lut5_I4_O)        0.297     9.872 r  control_unit/PCReg[6]_i_6/O
                         net (fo=3, routed)           0.683    10.555    control_unit/pmau/SH2Pmau_Instance/acarry_6
    SLICE_X2Y26          LUT5 (Prop_lut5_I4_O)        0.287    10.842 r  control_unit/PCReg[8]_i_6/O
                         net (fo=3, routed)           1.005    11.847    control_unit/pmau/SH2Pmau_Instance/acarry_8
    SLICE_X1Y28          LUT5 (Prop_lut5_I4_O)        0.264    12.111 r  control_unit/PCReg[10]_i_6/O
                         net (fo=3, routed)           0.515    12.626    control_unit/pmau/SH2Pmau_Instance/acarry_10
    SLICE_X1Y29          LUT5 (Prop_lut5_I4_O)        0.124    12.750 r  control_unit/PCReg[12]_i_6/O
                         net (fo=3, routed)           1.064    13.815    control_unit/pmau/SH2Pmau_Instance/acarry_12
    SLICE_X4Y30          LUT5 (Prop_lut5_I4_O)        0.277    14.092 r  control_unit/PCReg[14]_i_6/O
                         net (fo=3, routed)           0.891    14.982    control_unit/pmau/SH2Pmau_Instance/acarry_14
    SLICE_X4Y34          LUT5 (Prop_lut5_I4_O)        0.277    15.259 r  control_unit/PCReg[16]_i_6/O
                         net (fo=3, routed)           0.632    15.891    control_unit/pmau/SH2Pmau_Instance/acarry_16
    SLICE_X4Y36          LUT5 (Prop_lut5_I4_O)        0.286    16.177 r  control_unit/PCReg[18]_i_6/O
                         net (fo=3, routed)           0.785    16.962    control_unit/pmau/SH2Pmau_Instance/acarry_18
    SLICE_X0Y39          LUT5 (Prop_lut5_I4_O)        0.288    17.250 r  control_unit/PCReg[20]_i_6/O
                         net (fo=3, routed)           0.706    17.956    control_unit/pmau/SH2Pmau_Instance/acarry_20
    SLICE_X1Y39          LUT5 (Prop_lut5_I4_O)        0.281    18.237 r  control_unit/PCReg[22]_i_6/O
                         net (fo=3, routed)           0.947    19.185    control_unit/pmau/SH2Pmau_Instance/acarry_22
    SLICE_X4Y40          LUT5 (Prop_lut5_I4_O)        0.289    19.474 r  control_unit/PCReg[24]_i_6/O
                         net (fo=3, routed)           0.540    20.014    control_unit/pmau/SH2Pmau_Instance/acarry_24
    SLICE_X3Y41          LUT5 (Prop_lut5_I4_O)        0.294    20.308 r  control_unit/PCReg[26]_i_6/O
                         net (fo=3, routed)           0.771    21.079    control_unit/pmau/SH2Pmau_Instance/acarry_26
    SLICE_X1Y40          LUT5 (Prop_lut5_I4_O)        0.287    21.366 r  control_unit/PCReg[28]_i_6/O
                         net (fo=3, routed)           0.904    22.270    control_unit/pmau/SH2Pmau_Instance/acarry_28
    SLICE_X0Y42          LUT6 (Prop_lut6_I4_O)        0.275    22.545 r  control_unit/PCReg[28]_i_4/O
                         net (fo=1, routed)           0.575    23.121    control_unit/PCReg[28]_i_4_n_2
    SLICE_X1Y42          LUT6 (Prop_lut6_I5_O)        0.105    23.226 r  control_unit/PCReg[28]_i_1/O
                         net (fo=3, routed)           1.008    24.233    control_unit/PCMux[28]
    SLICE_X5Y37          LUT4 (Prop_lut4_I2_O)        0.105    24.338 r  control_unit/AB_OBUF[27]_inst_i_28/O
                         net (fo=1, routed)           0.000    24.338    control_unit/AB_OBUF[27]_inst_i_28_n_2
    SLICE_X5Y37          CARRY4 (Prop_carry4_S[3]_O[3])
                                                      0.206    24.544 r  control_unit/AB_OBUF[27]_inst_i_16/O[3]
                         net (fo=1, routed)           1.067    25.612    control_unit/dmau/plusOp[28]
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131     SLICE_X9Y44          LUT5 (Prop_lut5_I0_O)        0.257    25.869 r  control_unit/Registers[15][30]_i_8/O
132                          net (fo=7, routed)           0.937    26.805    control_unit/Registers[15][30]_i_8_n_2
133     SLICE_X12Y45         LUT5 (Prop_lut5_I2_O)        0.105    26.910 r  control_unit/AB_OBUF[28]_inst_i_4/O
134                          net (fo=2, routed)           0.452    27.362    control_unit/AB_OBUF[28]_inst_i_4_n_2
135     SLICE_X13Y44         LUT5 (Prop_lut5_I1_O)        0.126    27.488 r  control_unit/AB_OBUF[29]_inst_i_5/O
136                          net (fo=3, routed)           0.791    28.279    control_unit/dmau/SH2Dmau_Instance/acarry_29
137     SLICE_X13Y43         LUT3 (Prop_lut3_I2_O)        0.267    28.546 r  control_unit/AB_OBUF[31]_inst_i_8/O
138                          net (fo=2, routed)           0.720    29.266    control_unit/dmau/SH2Dmau_Instance/acarry_30
139     SLICE_X12Y43         LUT3 (Prop_lut3_I2_O)        0.105    29.371 r  control_unit/AB_OBUF[30]_inst_i_2/O
140                          net (fo=17, routed)          1.413    30.784    control_unit/DataAddress[30]
141     SLICE_X4Y38          LUT6 (Prop_lut6_I0_O)        0.105    30.889 r  control_unit/AB_OBUF[30]_inst_i_1/O
142                          net (fo=1, routed)           1.564    32.453    AB_OBUF[30]
143     M15                  OBUF (Prop_obuf_I_O)         2.361    34.814 r  AB_OBUF[30]_inst/O
144                          net (fo=0)                   0.000    34.814    AB[30]
145     M15                                                             r  AB[30] (OUT)
146   ---------------------------------------------------------------------    -------------------
147
148
```