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| Tool Version : Vivado v.2024.2 (win64) Build 5239630 Fri Nov 08 22:35:27 MST 2024
| Date         : Mon Jun  9 21:24:22 2025
| Host         : MACMINI running 64-bit major release  (build 9200)
| Command      : report_utilization -file SH2CPU_utilization_placed.rpt -pb SH2CPU_utilization_placed.pb
| Design       : SH2CPU
| Device       : xc7s25csga225-2
| Speed File   : -2
| Design State : Fully Placed
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Utilization Design Information

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1. Slice Logic

Site Type	Used	Fixed	Prohibited	Available	Util%
Slice LUTs	2329	0	0	14600	15.95
LUT as Logic	2329	0	0	14600	15.95
LUT as Memory	0	0	0	5000	0.00
Slice Registers	1232	0	0	29200	4.22
Register as Flip Flop	1067	0	0	29200	3.65
Register as Latch	165	0	0	29200	0.57
F7 Muxes	257	0	0	7300	3.52
F8 Muxes	128	0	0	3650	3.51

* Warning! LUT value is adjusted to account for LUT combining.

1.1 Summary of Registers by Type

Total	Clock Enable	Synchronous	Asynchronous
5	_	-	-
0	_	-	Set
0	_	-	Reset
0	_	Set	-
0	_	Reset	-
0	Yes	-	-
8	Yes	-	Set
1159	Yes	-	Reset
0	Yes	Set	-
60	Yes	Reset	-

2. Slice Logic Distribution

Site Type	Used	Fixed	Prohibited	Available	Util%
Slice	772	0	0	3650	21.15
SLICEL	519	0			
SLICEM	253	0			
LUT as Logic	2329	0	0	14600	15.95
using O5 output only	0				
using O6 output only	1822				
using O5 and O6	507				
LUT as Memory	0	0	0	5000	0.00
LUT as Distributed RAM	0	0			
using O5 output only	0				
using O6 output only	0				
using O5 and O6	0				
LUT as Shift Register	0	0			
using O5 output only	0				
using O6 output only	0				
using O5 and O6	0				
Slice Registers	1232	0	0	29200	4.22
Register driven from within the Slice	505				
Register driven from outside the Slice	727				
LUT in front of the register is unused	247				
LUT in front of the register is used	480				
Unique Control Sets	55		0	3650	1.51

* * Note: Available Control Sets calculated as Slice * 1, Review the Control Sets Report for more information regarding control sets.

3. Memory

Site Type	Used	Fixed	Prohibited	Available	Util%
Block RAM Tile	0	0	0	45	0.00
RAMB36/FIFO*	0	0	0	45	0.00
RAMB18	0	0	0	90	0.00

* Note: Each Block RAM Tile only has one FIFO logic available and therefore can accommodate only one FIFO36E1 or one FIFO18E1. However, if a FIFO18E1 occupies a Block RAM Tile, that tile can still accommodate a RAMB18E1

4. DSP

Site Type	Used	Fixed	Prohibited	Available	Util%
DSPs	0	0	0	80	0.00

5. IO and GT Specific

Site Type	Used	Fixed	Prohibited	Available	Util%
Bonded IOB	75	0	0	150	50.00
IOB Master Pads	36				
IOB Slave Pads	37				
Bonded IPADs	0	0	0	2	0.00
PHY_CONTROL	0	0	0	3	0.00

PHASER_REF	0	0	0	3	0.00
OUT_FIFO	0	0	0	12	0.00
IN_FIFO	0	0	0	12	0.00
IDELAYCTRL	0	0	0	3	0.00
IBUFDS	0	0	0	144	0.00
PHASER_OUT/PHASER_OUT_PHY	0	0	0	12	0.00
PHASER_IN/PHASER_IN_PHY	0	0	0	12	0.00
IDELAYE2/IDELAYE2_FINEDELAY	0	0	0	150	0.00
ILOGIC	0	0	0	150	0.00
OLOGIC	0	0	0	150	0.00

6. Clocking

Site Type	Used	Fixed	Prohibited	Available	Util%
BUFGCTRL	2	0	0	32	6.25
BUFIO	0	0	0	12	0.00
MMCME2_ADV	0	0	0	3	0.00
PLLE2_ADV	0	0	0	3	0.00
BUFMRCE	0	0	0	6	0.00
BUFHCE	0	0	0	48	0.00
BUFR	0	0	0	12	0.00

7. Specific Feature

Site Type	Used	Fixed	Prohibited	Available	Util%
BSCANE2	0	0	0	4	0.00
CAPTUREE2	0	0	0	1	0.00
DNA_PORT	0	0	0	1	0.00
EFUSE_USR	0	0	0	1	0.00
FRAME_ECCE2	0	0	0	1	0.00
ICAPE2	0	0	0	2	0.00
STARTUPE2	0	0	0	1	0.00
XADC	0	0	0	1	0.00

8. Primitives

Ref Name	Used	Functional Category
LUT6	1473	LUT
FDCE	1001	Flop & Latch
LUT3	645	LUT
LUT5	339	LUT
MUXF7	257	MuxFx
LUT2	189	LUT
LDCE	163	Flop & Latch
LUT4	154	LUT
MUXF8	128	MuxFx
FDRE	60	Flop & Latch
OBUF	41	IO
LUT1	36	LUT
IBUF	34	IO
OBUFT	32	IO

CARRY4	20	CarryLogic
FDPE	6	Flop & Latch
LDPE	2	Flop & Latch
BUFG	2	Clock

9. Black Boxes

| Ref Name | Used |

10. Instantiated Netlists

| Ref Name | Used |

| Tool Version : Vivado v.2024.2 (win64) Build 5239630 Fri Nov 08 22:35:27 MST 2024
| Date : Mon Jun 9 21:24:40 2025
| Host : MACMINI running 64-bit major release (build 9200)
| Command : report_timing_summary -max_paths 10 -report_unconstrained -file SH2CPU_timing_summary_routed.rpt -pb SH2CPU_timing_summary_routed.pb -rpx SH2CPU_timing_summary_routed.rpx -warn_on_violation
| Design : SH2CPU
| Device : 7s25-csga225
| Speed File : -2 PRODUCTION 1.23 2018-06-13
| Design State : Routed

Timing Summary Report

| Timer Settings
| --------------

  Enable Multi Corner Analysis : Yes
  Enable Pessimism Removal : Yes
  Pessimism Removal Resolution : Nearest Common Node
  Enable Input Delay Default Clock : No
  Enable Preset / Clear Arcs : No
  Disable Flight Delays : No
  Ignore I/O Paths : No
  Timing Early Launch at Borrowing Latches : No
  Borrow Time for Max Delay Exceptions : Yes
  Merge Timing Exceptions : Yes
  Inter-SLR Compensation : Conservative

  Corner Analyze Analyze
  Name Max Paths Min Paths
  ------ --------- ---------
  Slow Yes Yes
  Fast Yes Yes

| Report Methodology
| ------------------

Rule	Severity	Description	Violations
TIMING-17	Critical Warning	Non-clocked sequential cell	1000
LUTAR-1	Warning	LUT drives async reset alert	11
TIMING-20	Warning	Non-clocked latch	165
LATCH-1	Advisory	Existing latches in the design	1

Note: This report is based on the most recent report_methodology run and may not be up-to-date. Run report_methodology on the current design for the latest report.

| Timing Details
| --------------

Path Group: (none)
From Clock:
  To Clock:

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Max Delay          3293 Endpoints
Min Delay          3293 Endpoints
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Max Delay Paths
--------------------------------------------------------------------------------
Slack:                    inf
  Source:                 control_unit/pipeline_stages[2].pipeline_reg[2][MemCtrl][Enable]/C
                            (rising edge-triggered cell FDCE)
  Destination:            pmau/PCReg_reg[31]/D
  Path Group:             (none)
  Path Type:              Max at Slow Process Corner
  Data Path Delay:        41.748ns  (logic 7.365ns (17.642%)  route 34.383ns (82.358%))
  Logic Levels:           42  (CARRY4=1 FDCE=1 LUT2=2 LUT3=1 LUT4=2 LUT5=19 LUT6=15 MUXF8=1)

    Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
    -------------------------------------------------------------------    -------------------
     SLICE_X3Y27           FDCE                         0.000     0.000 r  control_unit/pipeline_stages[2].pipeline_reg[2][MemCtrl][Enable]/C
     SLICE_X3Y27           FDCE (Prop_fdce_C_Q)         0.379     0.379 f  control_unit/pipeline_stages[2].pipeline_reg[2][MemCtrl][Enable]/Q
                           net (fo=1, routed)           0.691     1.070    control_unit/pipeline_stages[2].pipeline_reg[2][MemCtrl][Enab
    SLICE_X3Y27          LUT2 (Prop_lut2_I1_O)        0.105     1.175 r  control_unit/IR[15]_i_1/O
                           net (fo=553, routed)         4.135     5.310    control_unit/p_6_in
    SLICE_X8Y42          LUT4 (Prop_lut4_I2_O)        0.105     5.415 r  control_unit/DB_reg[31]_i_9/O
                           net (fo=40, routed)          3.997     9.412    registers/Registers/RegCtrl[ASel][3]
    SLICE_X21Y32         MUXF8 (Prop_muxf8_S_O)       0.224     9.636 r  registers/Registers/DB_reg[29]_i_4/O
                           net (fo=7, routed)           1.108    10.744    control_unit/OperandA[5]
    SLICE_X21Y39         LUT2 (Prop_lut2_I1_O)        0.278    11.022 r  control_unit/Registers[15][7]_i_17/O
                           net (fo=8, routed)           0.688    11.710    control_unit/Registers[15][7]_i_17_n_1
    SLICE_X25Y39         LUT4 (Prop_lut4_I3_O)        0.275    11.985 f  control_unit/Registers[15][12]_i_30/O
                           net (fo=1, routed)           0.655    12.640    control_unit/Registers[15][12]_i_30_n_1
    SLICE_X25Y38         LUT6 (Prop_lut6_I0_O)        0.105    12.745 f  control_unit/Registers[15][12]_i_29/O
                           net (fo=1, routed)           0.510    13.255    control_unit/Registers[15][12]_i_29_n_1
    SLICE_X24Y39         LUT6 (Prop_lut6_I1_O)        0.105    13.360 r  control_unit/Registers[15][12]_i_26/O
                           net (fo=2, routed)           0.741    14.101    control_unit/Registers[15][12]_i_26_n_1
    SLICE_X22Y40         LUT6 (Prop_lut6_I5_O)        0.105    14.206 f  control_unit/Registers[15][17]_i_23/O
                           net (fo=1, routed)           0.674    14.880    control_unit/Registers[15][17]_i_23_n_1
    SLICE_X22Y41         LUT6 (Prop_lut6_I1_O)        0.105    14.985 r  control_unit/Registers[15][17]_i_19/O
                           net (fo=2, routed)           0.630    15.615    control_unit/Registers[15][17]_i_19_n_1
    SLICE_X21Y43         LUT6 (Prop_lut6_I5_O)        0.105    15.720 f  control_unit/Registers[15][22]_i_26/O
                           net (fo=1, routed)           0.573    16.293    control_unit/Registers[15][22]_i_26_n_1
    SLICE_X20Y43         LUT6 (Prop_lut6_I1_O)        0.105    16.398 r  control_unit/Registers[15][22]_i_22/O
                           net (fo=2, routed)           0.671    17.070    control_unit/Registers[15][22]_i_22_n_1
    SLICE_X21Y45         LUT5 (Prop_lut5_I0_O)        0.105    17.175 r  control_unit/Registers[15][22]_i_18/O
                           net (fo=2, routed)           0.827    18.001    control_unit/Registers[15][22]_i_18_n_1
    SLICE_X23Y45         LUT5 (Prop_lut5_I0_O)        0.105    18.106 r  control_unit/Registers[15][22]_i_16/O
                           net (fo=3, routed)           0.764    18.871    control_unit/Registers[15][22]_i_16_n_1
    SLICE_X24Y45         LUT5 (Prop_lut5_I0_O)        0.105    18.976 r  control_unit/Registers[15][24]_i_21/O
                           net (fo=2, routed)           0.787    19.762    control_unit/Registers[15][24]_i_21_n_1
    SLICE_X24Y44         LUT6 (Prop_lut6_I2_O)        0.105    19.867 r  control_unit/Registers[15][24]_i_13/O
                           net (fo=2, routed)           0.448    20.315    control_unit/Registers[15][24]_i_13_n_1
    SLICE_X22Y43         LUT5 (Prop_lut5_I0_O)        0.105    20.420 r  control_unit/pipeline_in_en_i_35/O
                           net (fo=1, routed)           0.540    20.960    control_unit/pipeline_in_en_i_35_n_1
    SLICE_X23Y43         LUT5 (Prop_lut5_I3_O)        0.105    21.065 r  control_unit/pipeline_in_en_i_16/O
                           net (fo=1, routed)           0.448    21.513    control_unit/pipeline_in_en_i_16_n_1
    SLICE_X24Y41         LUT6 (Prop_lut6_I1_O)        0.105    21.618 f  control_unit/pipeline_in_en_i_7/O
                           net (fo=5, routed)           0.976    22.594    control_unit/Zero
    SLICE_X24Y33         LUT6 (Prop_lut6_I2_O)        0.105    22.699 r  control_unit/pipeline_in_en_i_4/O
                           net (fo=1, routed)           0.814    23.514    control_unit/pipeline_in_en_i_4_n_1
    SLICE_X24Y32         LUT6 (Prop_lut6_I3_O)        0.105    23.619 f  control_unit/pipeline_in_en_i_1/O
                           net (fo=10, routed)          1.442    25.061    control_unit/pipeline_in_en_i_1_n_1
    SLICE_X10Y26         LUT3 (Prop_lut3_I2_O)        0.105    25.166 r  control_unit/PCReg[31]_i_12/O
                           net (fo=30, routed)          0.765    25.931    control_unit/PCReg[31]_i_12_n_1
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129     SLICE_X9Y25          LUT6 (Prop_lut6_I1_O)        0.105    26.036 r  control_unit/PCReg[4]_i_15/O
130                          net (fo=1, routed)           0.000    26.036    control_unit/PMAUCtrl[Off12][0]
131     SLICE_X9Y25          CARRY4 (Prop_carry4_S[0]_O[0])
132                                                       0.207    26.243 r  control_unit/PCReg_reg[4]_i_8/O[0]
133                          net (fo=1, routed)           0.555    26.798    control_unit/pmau/PMAUAddrOff[2]0[1]
134     SLICE_X8Y25          LUT6 (Prop_lut6_I1_O)        0.249    27.047 r  control_unit/PCReg[2]_i_9/O
135                          net (fo=4, routed)           0.623    27.670    control_unit/PCReg[2]_i_9_n_1
136     SLICE_X4Y29          LUT6 (Prop_lut6_I0_O)        0.105    27.775 r  control_unit/PCReg[4]_i_10/O
137                          net (fo=1, routed)           0.689    28.465    control_unit/pmau/SH2Pmau_Instance/acarry_2
138     SLICE_X5Y29          LUT5 (Prop_lut5_I4_O)        0.119    28.584 r  control_unit/PCReg[4]_i_6/O
139                          net (fo=2, routed)           0.361    28.945    control_unit/pmau/SH2Pmau_Instance/acarry_4
140     SLICE_X5Y29          LUT5 (Prop_lut5_I4_O)        0.267    29.212 r  control_unit/PCReg[6]_i_6/O
141                          net (fo=3, routed)           0.341    29.552    control_unit/pmau/SH2Pmau_Instance/acarry_6
142     SLICE_X3Y30          LUT5 (Prop_lut5_I4_O)        0.108    29.660 r  control_unit/PCReg[8]_i_6/O
143                          net (fo=3, routed)           0.492    30.152    control_unit/pmau/SH2Pmau_Instance/acarry_8
144     SLICE_X2Y32          LUT5 (Prop_lut5_I4_O)        0.267    30.419 r  control_unit/PCReg[10]_i_6/O
145                          net (fo=3, routed)           0.533    30.952    control_unit/pmau/SH2Pmau_Instance/acarry_10
146     SLICE_X2Y31          LUT5 (Prop_lut5_I4_O)        0.105    31.057 r  control_unit/PCReg[12]_i_6/O
147                          net (fo=3, routed)           0.788    31.845    control_unit/pmau/SH2Pmau_Instance/acarry_12
148     SLICE_X0Y39          LUT5 (Prop_lut5_I4_O)        0.128    31.973 r  control_unit/PCReg[14]_i_6/O
149                          net (fo=3, routed)           0.910    32.883    control_unit/pmau/SH2Pmau_Instance/acarry_14
150     SLICE_X1Y43          LUT5 (Prop_lut5_I4_O)        0.282    33.165 r  control_unit/PCReg[16]_i_6/O
151                          net (fo=3, routed)           0.544    33.709    control_unit/pmau/SH2Pmau_Instance/acarry_16
152     SLICE_X2Y44          LUT5 (Prop_lut5_I4_O)        0.295    34.004 r  control_unit/PCReg[18]_i_6/O
153                          net (fo=3, routed)           0.772    34.776    control_unit/pmau/SH2Pmau_Instance/acarry_18
154     SLICE_X3Y46          LUT5 (Prop_lut5_I4_O)        0.284    35.060 r  control_unit/PCReg[20]_i_6/O
155                          net (fo=3, routed)           0.661    35.721    control_unit/pmau/SH2Pmau_Instance/acarry_20
156     SLICE_X3Y47          LUT5 (Prop_lut5_I4_O)        0.285    36.006 r  control_unit/PCReg[22]_i_6/O
157                          net (fo=3, routed)           0.823    36.829    control_unit/pmau/SH2Pmau_Instance/acarry_22
158     SLICE_X5Y47          LUT5 (Prop_lut5_I4_O)        0.277    37.106 r  control_unit/PCReg[24]_i_6/O
159                          net (fo=3, routed)           0.821    37.927    control_unit/pmau/SH2Pmau_Instance/acarry_24
160     SLICE_X6Y50          LUT5 (Prop_lut5_I4_O)        0.288    38.215 r  control_unit/PCReg[26]_i_6/O
161                          net (fo=3, routed)           0.660    38.875    control_unit/pmau/SH2Pmau_Instance/acarry_26
162     SLICE_X5Y50          LUT5 (Prop_lut5_I4_O)        0.286    39.161 r  control_unit/PCReg[28]_i_6/O
163                          net (fo=3, routed)           0.707    39.868    control_unit/pmau/SH2Pmau_Instance/acarry_28
164     SLICE_X4Y49          LUT5 (Prop_lut5_I4_O)        0.282    40.150 r  control_unit/PCReg[31]_i_10/O
165                          net (fo=2, routed)           0.487    40.637    control_unit/pmau/SH2Pmau_Instance/acarry_30
166     SLICE_X6Y49          LUT6 (Prop_lut6_I2_O)        0.275    40.912 r  control_unit/PCReg[31]_i_4/O
167                          net (fo=1, routed)           0.731    41.643    control_unit/PCReg[31]_i_4_n_1
168     SLICE_X6Y49          LUT6 (Prop_lut6_I3_O)        0.105    41.748 r  control_unit/PCReg[31]_i_1/O
169                          net (fo=1, routed)           0.000    41.748    pmau/PCMux[31]
170     SLICE_X6Y49          FDCE                                          r  pmau/PCReg_reg[31]/D
171   -------------------------------------------------------------------    -------------------
172
173
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