EE 188 Homework #3 - util.report Zachary Huang & Chris Miranda

```
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1
   2
   | Tool Version : Vivado v.2024.2 (win64) Build 5239630 Fri Nov 08 22:35:27 MST 2024
3
  | Date
            : Mon Jun 9 21:56:12 2025
  | Host
            : MACMINI running 64-bit major release (build 9200)
            : report_utilization -file SH2CPU_utilization_placed.rpt -pb SH2CPU_utilization_placed.pb
7
            : SH2CPU
   | Design
8
  | Device
            : xc7s25csga225-2
9
   | Speed File : -2
10
  | Design State : Fully Placed
  ______
11
12
13 Utilization Design Information
14
15 Table of Contents
16 -----
17 1. Slice Logic
18 1.1 Summary of Registers by Type
19 2. Slice Logic Distribution
20 3. Memory
21 4. DSP
22 5. IO and GT Specific
23 6. Clocking
24 7. Specific Feature
25 8. Primitives
26 9. Black Boxes
27 10. Instantiated Netlists
28
29 1. Slice Logic
30
  -----
31
32 +-----
33 |
       Site Type
                  | Used | Fixed | Prohibited | Available | Util% |
34 +-----
                  | 2150 | 0 |
                                   0 | 14600 | 14.73 |
35 | Slice LUTs
                                  0 | 14600 | 14.73 |
                   | 2150 |
36 | LUT as Logic
                            0 |
37 | LUT as Memory
                  | 0 |
                            0 |
                                   0 |
                                         5000 | 0.00 |
                   | 975 | 0 |
38 | Slice Registers
                                   0 | 29200 | 3.34 |
39 | Register as Flip Flop | 787 | 0 |
                                    0 | 29200 | 2.70 |
40 | Register as Latch | 188 | 0 |
                                     0 | 29200 | 0.64 |
41 | F7 Muxes
                  | 257 |
                            0 |
                                     0 | 7300 | 3.52 |
42 | F8 Muxes
                   | 128 |
                            0 |
                                     0 |
                                          3650 | 3.51 |
43 +-----
44 * Warning! LUT value is adjusted to account for LUT combining.
45
46
47 1.1 Summary of Registers by Type
48
49
50 +-----+
   | Total | Clock Enable | Synchronous | Asynchronous |
52 +-----+
                _ 1
53 | 0
       - |
54 | 0
        _ 1
                         - |
                                  Set I
                      - |
Set |
               _ 1
  | 0
55
        Reset I
              _ 1
56 | 0
        - 1
57 I 0
                       Reset |
                                   - 1
        - 1
                _ |
                       - |
58 | 0
        - 1
              Yes |
                                  - |
59 | 3
              Yes I
                        - |
                                 Set |
        1
60 | 908 |
                        - |
               Yes |
                                 Reset |
61 | 0
               Yes |
                        Set |
                                  - |
        62 | 64
               Yes |
63 +-----+
64
```

66 2. Slice Logic Distribution

EE 188 Homework #3 - util.report Zachary Huang & Chris Miranda

	67 68								
72 Slice		·	+	+	+	+	++		
731 0						•			
SLICEL									
248			•		•	1 3030	1 20.05		
15						1			
15					•	14600	14.73		
	76				I	i	i i		
10	77	using 06 output only	1641	1	Ī	İ	i i		
	78	using 05 and 06	509	I	I	1	1 1		
	79	LUT as Memory	0	0	Θ	5000	0.00		
	80	LUT as Distributed RAM	0	0	I	1	1		
	81	using 05 output only	0	I	I	1	1 1		
Author	82		0	I	I	1	1 1		
88 using 05 output only				•	1	1			
				•	1	1	1 1		
87				•	I I	1	1 1		
Silice Registers 975 6 8 29288 3.34 99 Register driven from within the Slice 401 99 Register driven from outside the Slice 574 1 LUT in front of the register is unused 147 2 LUT in front of the register is unused 147 3 Unique Control Sets 47 0 3650 1.29 4				•	I I	1	1 1		
Register driven from within the Slice 401			•		ا ا	1 20200			
Register driven from outside the Slice 574				•	,	23200			
LUT in front of the register is unused 147			•		I	I			
1						İ	i i		
94 * * Note: Available Control Sets calculated as Slice * 1, Review the Control Sets Report for more information regarding control 6 97 98 3. Memory 99 * * Note: Available Control Sets calculated as Slice * 1, Review the Control Sets Report for more information regarding control 6 98 3. Memory 99 * * Note: Available Control Sets calculated as Slice * 1, Review the Control Sets Report for more information regarding control 6 99 * * Note: Available Control Sets Report for more information regarding control 6 90 * * Note: Available Control Sets Report for more information regarding control 6 90 * * Note: Available Control Sets Report for more information regarding control 6 90 * * Note: Available Control Sets Report for more information regarding control 6 91 * * Note: Available Control Sets Report for more information regarding control 6 91 * Note: Available Control Sets Report for more information regarding control 6 91 * Note: Available Control Sets Report for more information regarding control 6 92 * Note: Available Control Sets Report for more information regarding control 6 93 * Nemory 94 * Note: Available Control Sets Report for more information regarding control 6 94 * Note: Available Control Sets Report for more information regarding control 6 95 * Note: Available Control Sets Report for More Control Sets Report for more information regarding control 6 96 * Note: Available Control Sets Report for More Control Sets Report for	92	LUT in front of the register is used	427	I	1	1	1 1		
** Note: Available Control Sets calculated as Slice * 1, Review the Control Sets Report for more information regarding cont 96 78	93	Unique Control Sets	47	I	0	3650	1.29		
103	100 101	·							
104 Block RAM Tile 0 0 0 45 0.00					· ·				
105									
107					· ·				
* Note: Each Block RAM Tile only has one FIFO logic available and therefore can accommodate only one FIFO36E1 or one FIFO18E1 if a FIFO18E1 occupies a Block RAM Tile, that tile can still accommodate a RAMB18E1 109 110 111 11.	106	RAMB18 0 0 0	1	90	0.00				
114 ++ 115 Site Type Used Fixed Prohibited Available Util% 116 +	108 109 110 111 112	* Note: Each Block RAM Tile only has one FIFO if a FIFO18E1 occupies a Block RAM Tile, that	logic a	vailable	and therefo		modate only	one FIF036E1 or one	FIF018E1.
115 Site Type Used Fixed Prohibited Available Util% 116 ++++									
116 ++ ++ ++ ++ +									
117 DSPS					-				
118 ++ + + + + + + + + + + + + + + +									
120 121 5. IO and GT Specific 122 123 124 125 126 126 127 128	118				•				
121 5. IO and GT Specific 122	119								
122	120								
123 124		•							
124 ++ ++ +									
125 Site Type Used Fixed Prohibited Available Util% 126 +					-				
126 ++ ++ ++ ++ 127 Bonded IOB									
127 Bonded IOB 75 0 0 150 50.00 128 IOB Master Pads 36 129 IOB Slave Pads 37 130 Bonded IPADs 0 0 0 2 0.00			-	-	-	-			
128 IOB Master Pads 36									
129 IOB Slave Pads 37		• •			1				
130 Bonded IPADs 0 0 2 0.00			1	i	i	i			
131 PHY_CONTROL 0 0 3 0.00			1	0	2	0.00			
	131	PHY_CONTROL	1	0	3	0.00			

```
132 | PHASER REF
                          0 |
                                        0 |
                      0 |
                                               3 | 0.00 |
                               0 |
133 | OUT FIFO
                          0 |
                                         0 |
                                                12 | 0.00 |
                       - 1
                                               12 | 0.00 |
134 | IN FIFO
                          0 |
                               0 |
                                        0 |
                      - 1
135 | IDELAYCTRL
                       - 1
                          0 |
                               0 |
                                        0 |
                                                3 | 0.00 |
136 | IBUFDS
                       0 |
                               0 |
                                        0 |
                                               144 | 0.00 |
                          0 |
                               0 |
                                        0 |
137 | PHASER_OUT/PHASER_OUT_PHY |
                                               12 | 0.00 |
                                               12 | 0.00 |
138 | PHASER_IN/PHASER_IN_PHY |
                          0 |
                               0 |
                                        0 |
139 | IDELAYE2/IDELAYE2_FINEDELAY |
                          0 |
                               0 |
                                        0 |
                                               150 | 0.00 |
140 | ILOGIC
                  0 |
                               0 |
                                        0 |
                                              150 | 0.00 |
                                    0 |
                                             150 | 0.00 |
                               0 |
141 | OLOGIC
                       0 |
142 +-----
143
144
145 6. Clocking
146 -----
147
148 +-----
149 | Site Type | Used | Fixed | Prohibited | Available | Util% |
150 +-----
151 | BUFGCTRL | 4 | 0 | 0 | 32 | 12.50 |
152 | BUFIO | 0 | 0 | 0 |
153 | MMCME2_ADV | 0 | 0 | 0 |
154 | PLLE2_ADV | 0 | 0 | 0 |
155 | BUFMRCE | 0 | 0 | 0 |
                                   12 | 0.00 |
                                   3 | 0.00 |
                                    3 | 0.00 |
                                    6 | 0.00 |
156 | BUFHCE | 0 | 0 |
                             0 |
                                    48 | 0.00 |
                                   12 | 0.00 |
          | 0 | 0 |
                             0 |
157 | BUFR
158 +-----
159
160
161 7. Specific Feature
162 -----
163
164 +-----
165 | Site Type | Used | Fixed | Prohibited | Available | Util% |
166 +-----
167 | BSCANE2 | 0 |
                   0 | 0 |
                                    4 | 0.00 |
168 | CAPTUREE2 | 0 |
                   0 |
                            0 |
                                    1 | 0.00 |
169 | DNA_PORT | 0 | 0 |
170 | EFUSE_USR | 0 | 0 |
                            0 |
                                    1 | 0.00 |
                            0 |
                                     1 | 0.00 |
171 | FRAME_ECCE2 | 0 | 0 |
                            0 |
                                     1 | 0.00 |
172 | ICAPE2 | 0 | 0 |
                            0 |
                                     2 | 0.00 |
173 | STARTUPE2 | 0 | 0 |
                            0 |
                                     1 | 0.00 |
174 | XADC | 0 | 0 |
                            0 |
                                     1 | 0.00 |
175 +-----
176
177
178 8. Primitives
179 -----
180
181 +-----+
182 | Ref Name | Used | Functional Category |
183 +-----
                    LUT |
        | 1229 |
184 | LUT6
          | 720 |
185 | FDCE
                     Flop & Latch |
         | 580 |
186 | LUT3
                     L IIIT I
187 | LUT5
         | 470 |
                          LUT I
188 | MUXF7
         | 257 |
                          MuxFx I
189 | LUT4
         | 217 |
                         LUT |
190 | LDCE
         | 188 |
                    Flop & Latch |
191 | LUT2
         | 155 |
                         LUT |
192 | MUXF8
         | 128 |
                        MuxFx |
193 | FDRE
         | 64 |
                     Flop & Latch |
194 | OBUF
         | 41 |
                     IO |
195 | IBUF
                           IO |
         | 34 |
196 | OBUFT | 32 |
                          IO |
                    CarryLogic |
197 | CARRY4 | 28 |
```

```
LUT |
198 | LUT1 | 8 |
199 | BUFG | 4 | Clock | 200 | FDPE | 3 | Flop & Latch |
202
203
204 9. Black Boxes
205 -----
206
207 +-----+
208 | Ref Name | Used |
209 +-----+
210
211
212 10. Instantiated Netlists
213 -----
214
215 +----+
216 | Ref Name | Used |
217 +----+
218
219
220
```

```
Copyright 1986-2022 Xilinx, Inc. All Rights Reserved. Copyright 2022-2024 Advanced Micro Devices, Inc. All Rights Reserved.
1
2
   | Tool Version : Vivado v.2024.2 (win64) Build 5239630 Fri Nov 08 22:35:27 MST 2024
3
   | Date
          : Mon Jun 9 21:56:31 2025
5
   | Host
              : MACMINI running 64-bit major release (build 9200)
               : report_timing_summary -max_paths 10 -report_unconstrained -file SH2CPU_timing_summary_routed.rpt -pb
6
   SH2CPU_timing_summary_routed.pb -rpx SH2CPU_timing_summary_routed.rpx -warn_on_violation
7
   | Design
             : SH2CPU
8
  | Device
              : 7s25-csga225
   | Speed File : -2 PRODUCTION 1.23 2018-06-13
10 | Design State : Routed
11
12
13 Timing Summary Report
14
15
16
   | Timer Settings
17
18
   ------
19
20
    Enable Multi Corner Analysis
                                      : Yes
21
    Enable Pessimism Removal
                                      : Yes
22
    Pessimism Removal Resolution
                                     : Nearest Common Node
23
    Enable Input Delay Default Clock
                                     : No
    Enable Preset / Clear Arcs
24
                                     : No
    Disable Flight Delays
25
26
    Ignore I/O Paths
27
     Timing Early Launch at Borrowing Latches : No
28
     Borrow Time for Max Delay Exceptions
                                     : Yes
29
     Merge Timing Exceptions
30
    Inter-SLR Compensation
31
32
     Corner Analyze
                  Analyze
33
    Name Max Paths Min Paths
34
    -----
35
    Slow Yes
                   Yes
36
    Fast
         Yes
                   Yes
37
38
39
40
   | Report Methodology
41
42
   ______
43
44
   Rule
            Severity
                         Description
                                                  Violations
   45
   TIMING-17 Critical Warning Non-clocked sequential cell
47
   TIMING-20 Warning
                     Non-clocked latch
48 LATCH-1 Advisory
                       Existing latches in the design 1
49
   Note: This report is based on the most recent report_methodology run and may not be up-to-date. Run report_methodology on the current
50
   design for the latest report.
51
52
53
54
55
   | Timing Details
56
57
58
59
60
61 Path Group: (none)
62 From Clock:
63
   To Clock:
64
```

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```
2490 Endpoints
65
   Max Delav
66
    Min Delav
                      2490 Endpoints
67
    ______
68
69
70
    Max Delay Paths
71
72
    Slack:
73
      Source:
                             Reset
74
                               (input port)
75
      Destination:
                             AB[30]
76
                               (output port)
77
      Path Group:
                             (none)
78
      Path Type:
                            Max at Slow Process Corner
79
      Data Path Delay:
                            34.814ns (logic 8.859ns (25.446%) route 25.955ns (74.554%))
80
      Logic Levels:
                            29 (CARRY4=1 IBUF=1 LUT3=5 LUT4=1 LUT5=16 LUT6=4 OBUF=1)
81
82
                            Delay type
                                                   Incr(ns) Path(ns)
                                                                         Netlist Resource(s)
83
      ______
84
                                                       0.000
                                                              0.000 r Reset (IN)
       K14
85
                            net (fo=0)
                                                       0.000
                                                                0.000
                                                                         Reset
86
        K14
                            IBUF (Prop_ibuf_I_0)
                                                       0.886
                                                                0.886 r Reset_IBUF_inst/0
87
                            net (fo=143, routed)
                                                       4.714
                                                                5.599
                                                                         control_unit/Reset_IBUF
88
        SLICE X5Y20
                            LUT5 (Prop_lut5_I0_0)
                                                       0.105
                                                                5.704 r control_unit/PCReg[1]_i_5/0
89
                            net (fo=8, routed)
                                                       1.072
                                                                 6.777
                                                                         control_unit/PCReg[1]_i_5_n_2
90
        SLICE X3Y22
                            LUT6 (Prop lut6 I0 0)
                                                       0.105
                                                                 6.882 r control unit/PCReg[1] i 3/0
91
                            net (fo=2, routed)
                                                       0.671
                                                                 7.553
                                                                         control_unit/PCReg[1]_i_3_n_2
92
        SLICE_X3Y23
                            LUT3 (Prop_lut3_I0_0)
                                                       0.105
                                                                 7.658 r control_unit/PCReg[2]_i_6/0
93
                            net (fo=2, routed)
                                                       0.480
                                                                 8.138
                                                                         control_unit/pmau/SH2Pmau_Instance/acarry_2
                                                                 8.263 r control_unit/PCReg[3]_i_6/0
94
        SLICE_X2Y24
                            LUT3 (Prop_lut3_I2_0)
                                                       0.125
95
                            net (fo=2, routed)
                                                       0.379
                                                                 8.642
                                                                         control_unit/pmau/SH2Pmau_Instance/acarry_3
96
        SLICE_X2Y24
                            LUT3 (Prop_lut3_I2_0)
                                                       0.265
                                                                 8.907 r control_unit/PCReg[4]_i_6/0
97
                            net (fo=3, routed)
                                                       0.668
                                                                 9.575
                                                                         control unit/pmau/SH2Pmau Instance/acarry 4
                                                                 9.872 r control_unit/PCReg[6]_i_6/0
98
        SLICE X1Y24
                            LUT5 (Prop_lut5_I4_0)
                                                       0.297
99
                            net (fo=3, routed)
                                                       0.683
                                                                10.555
                                                                         control unit/pmau/SH2Pmau Instance/acarry 6
                                                                10.842 r control_unit/PCReg[8]_i_6/0
100
        SLICE X2Y26
                            LUT5 (Prop lut5 I4 0)
                                                       0.287
101
                            net (fo=3, routed)
                                                       1.005
                                                                11.847
                                                                         control_unit/pmau/SH2Pmau_Instance/acarry_8
102
        SLICE_X1Y28
                            LUT5 (Prop_lut5_I4_0)
                                                       0.264
                                                                12.111 r control_unit/PCReg[10]_i_6/0
103
                            net (fo=3, routed)
                                                       0.515
                                                                12.626 control_unit/pmau/SH2Pmau_Instance/acarry_10
        SLICE_X1Y29
                            LUT5 (Prop_lut5_I4_0)
104
                                                       0.124
                                                                12.750 r control_unit/PCReg[12]_i_6/0
105
                            net (fo=3, routed)
                                                       1.064
                                                                13.815
                                                                         control_unit/pmau/SH2Pmau_Instance/acarry_12
106
        SLICE_X4Y30
                            LUT5 (Prop_lut5_I4_0)
                                                       0.277
                                                                14.092 r control_unit/PCReg[14]_i_6/0
107
                            net (fo=3, routed)
                                                       0.891
                                                                14.982
                                                                         control_unit/pmau/SH2Pmau_Instance/acarry_14
108
        SLICE X4Y34
                            LUT5 (Prop_lut5_I4_0)
                                                       0.277
                                                                15.259 r control_unit/PCReg[16]_i_6/0
                                                                15.891 control_unit/pmau/SH2Pmau_Instance/acarry_16
109
                            net (fo=3, routed)
                                                       0.632
110
        SLICE_X4Y36
                            LUT5 (Prop lut5 I4 0)
                                                       0.286
                                                                16.177 r control_unit/PCReg[18]_i_6/0
111
                            net (fo=3, routed)
                                                       0.785
                                                                16.962
                                                                         control unit/pmau/SH2Pmau Instance/acarry 18
112
        SLICE_X0Y39
                            LUT5 (Prop_lut5_I4_0)
                                                       0.288
                                                                17.250 r control_unit/PCReg[20]_i_6/0
113
                            net (fo=3, routed)
                                                       0.706
                                                                17.956
                                                                         control_unit/pmau/SH2Pmau_Instance/acarry_20
114
        SLICE_X1Y39
                            LUT5 (Prop_lut5_I4_0)
                                                       0.281
                                                                18.237 r control_unit/PCReg[22]_i_6/0
115
                            net (fo=3, routed)
                                                       0.947
                                                                19.185
                                                                         control_unit/pmau/SH2Pmau_Instance/acarry_22
116
        SLICE_X4Y40
                            LUT5 (Prop_lut5_I4_0)
                                                       0.289
                                                                19.474 r control_unit/PCReg[24]_i_6/0
117
                            net (fo=3, routed)
                                                       0.540
                                                                20.014
                                                                         control_unit/pmau/SH2Pmau_Instance/acarry_24
118
        SLICE X3Y41
                            LUT5 (Prop_lut5_I4_0)
                                                       0.294
                                                                20.308 r control_unit/PCReg[26]_i_6/0
119
                            net (fo=3, routed)
                                                       0.771
                                                                21.079
                                                                         control_unit/pmau/SH2Pmau_Instance/acarry_26
                                                                21.366 r control_unit/PCReg[28]_i_6/0
120
        SLICE X1Y40
                            LUT5 (Prop_lut5_I4_0)
                                                       0.287
                            net (fo=3, routed)
121
                                                       0.904
                                                                22.270
                                                                         control unit/pmau/SH2Pmau Instance/acarry 28
122
        SLICE X0Y42
                            LUT6 (Prop lut6 I4 0)
                                                       0.275
                                                                22.545 r control unit/PCReg[28] i 4/0
123
                            net (fo=1, routed)
                                                       0.575
                                                                23.121
                                                                         control unit/PCReg[28] i 4 n 2
124
        SLICE_X1Y42
                            LUT6 (Prop_lut6_I5_0)
                                                       0.105
                                                                23.226 r control_unit/PCReg[28]_i_1/0
125
                            net (fo=3, routed)
                                                       1.008
                                                                24.233
                                                                         control_unit/PCMux[28]
126
        SLICE_X5Y37
                            LUT4 (Prop_lut4_I2_0)
                                                       0.105
                                                                24.338 r control_unit/AB_OBUF[27]_inst_i_28/0
127
                            net (fo=1, routed)
                                                       0.000
                                                                24.338
                                                                         control_unit/AB_OBUF[27]_inst_i_28_n_2
128
        SLICE_X5Y37
                            CARRY4 (Prop_carry4_S[3]_0[3])
129
                                                       0.206
                                                                24.544 r control_unit/AB_OBUF[27]_inst_i_16/0[3]
130
                            net (fo=1, routed)
                                                       1.067
                                                                25.612
                                                                         control unit/dmau/plus0p[28]
```

131	SLICE_X9Y44	LUT5 (Prop_lut5_I0_0)	0.257	25.869 r	control_unit/Registers[15][30]_i_8/0
132		net (fo=7, routed)	0.937	26.805	control_unit/Registers[15][30]_i_8_n_2
133	SLICE_X12Y45	LUT5 (Prop_lut5_I2_0)	0.105	26.910 r	control_unit/AB_OBUF[28]_inst_i_4/0
134		net (fo=2, routed)	0.452	27.362	control_unit/AB_OBUF[28]_inst_i_4_n_2
135	SLICE_X13Y44	LUT5 (Prop_lut5_I1_0)	0.126	27.488 r	control_unit/AB_OBUF[29]_inst_i_5/0
136		net (fo=3, routed)	0.791	28.279	<pre>control_unit/dmau/SH2Dmau_Instance/acarry_29</pre>
137	SLICE_X13Y43	LUT3 (Prop_lut3_I2_0)	0.267	28.546 r	control_unit/AB_OBUF[31]_inst_i_8/0
138		net (fo=2, routed)	0.720	29.266	<pre>control_unit/dmau/SH2Dmau_Instance/acarry_30</pre>
139	SLICE_X12Y43	LUT3 (Prop_lut3_I2_0)	0.105	29.371 r	control_unit/AB_OBUF[30]_inst_i_2/0
140		net (fo=17, routed)	1.413	30.784	<pre>control_unit/DataAddress[30]</pre>
141	SLICE_X4Y38	LUT6 (Prop_lut6_I0_0)	0.105	30.889 r	control_unit/AB_OBUF[30]_inst_i_1/0
142		net (fo=1, routed)	1.564	32.453	AB_OBUF[30]
143	M15	OBUF (Prop_obuf_I_O)	2.361	34.814 r	AB_OBUF[30]_inst/0
144		net (fo=0)	0.000	34.814	AB[30]
145	M15			r	AB[30] (OUT)
146					
147					
148					

3