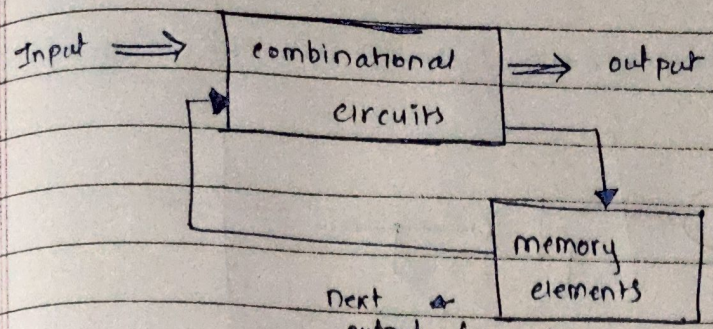
Mod-3 – Sequential circuits.

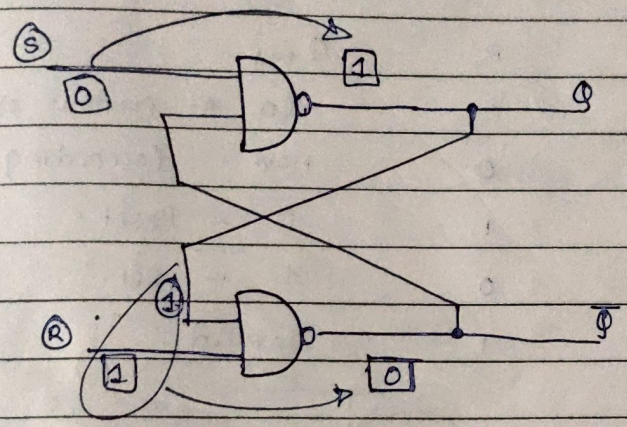


* output based on 2 things
  → based on previous output

* Flipflop stores 1 bit memory.

*

SR – Latch (using nand Gate)



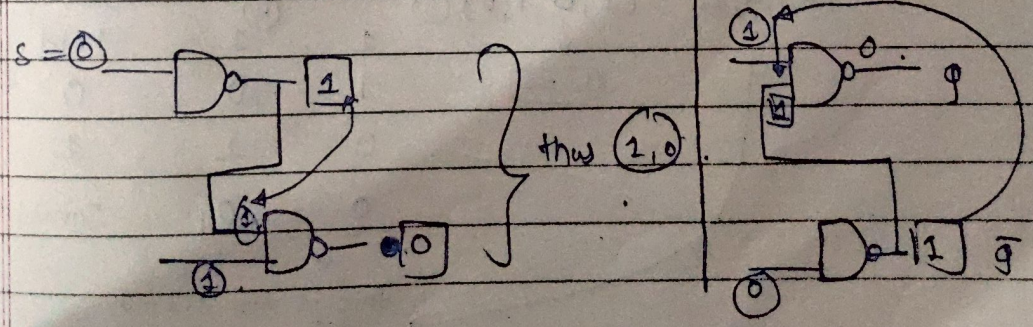
Nand

0	0	1
0	1	1
1	0	1
1	1	0

S	R	Q (n+1)
0	0	Invalid state ($Q=1$, $\bar{Q}=1$)
0	1	1
1	0	0
1	1	Hold state (Q)

* * *

$\overline{1 \cdot Q} = \bar{1} + \bar{Q}$ | $\overline{1 \cdot Q} = 0 + \bar{Q}$ | $= \bar{Q}$



* Latch is beginning block of Flip Flop.

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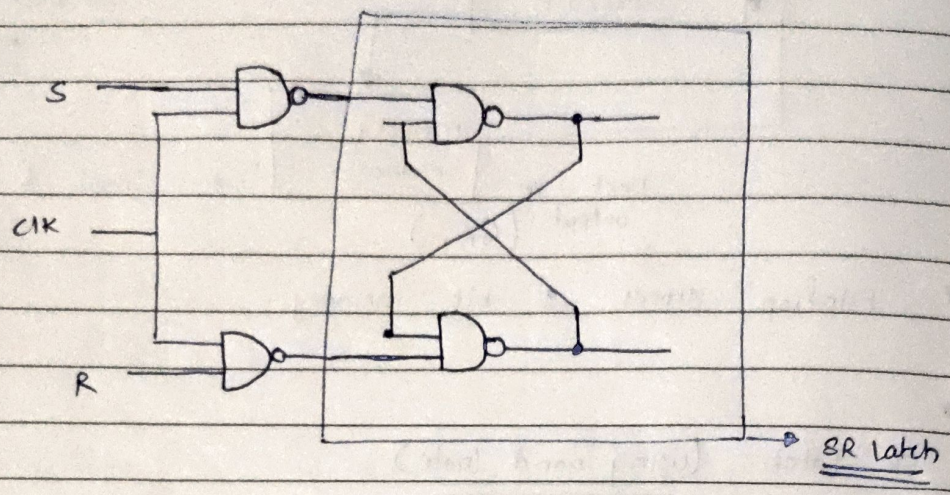
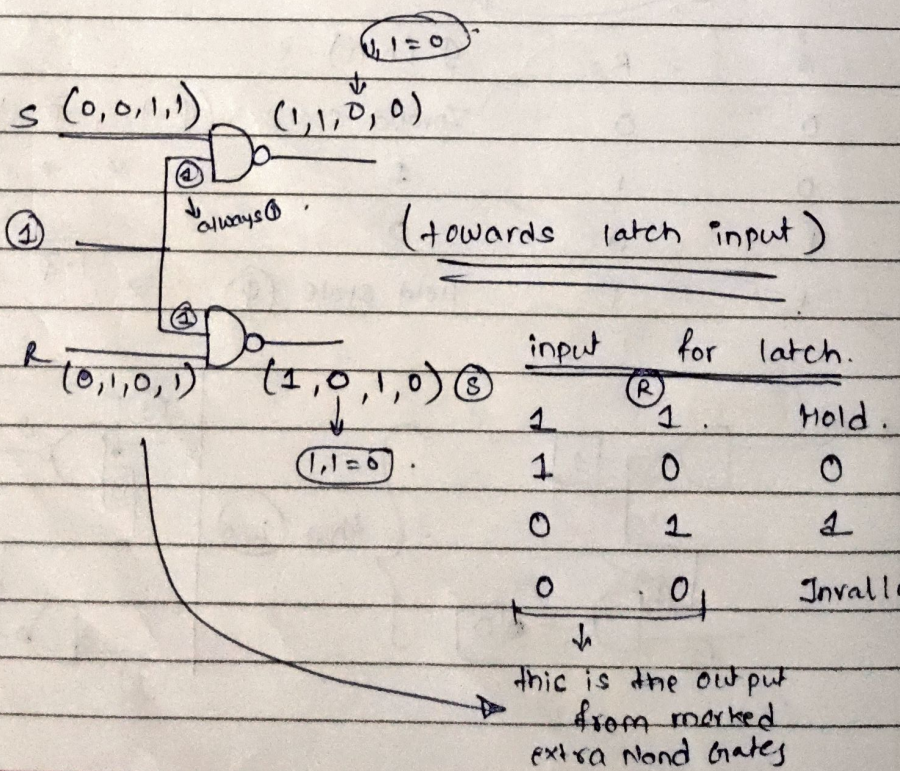
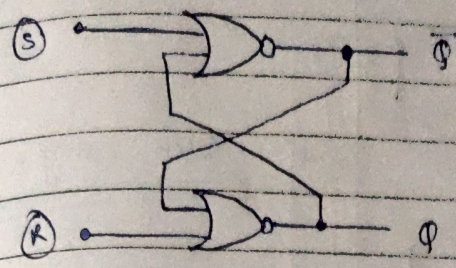
SR Flip Flop using NAND Gate :



Clock	S	R	Q_{n+1}
NOT	–	–	Q_n ← Previous state output.
Triggered	0	0	Hold. (according to latch)
	0	1	0 – Reset.
	1	0	1 – Set
	1	1	Invalid.



SR Latch using NOR Gate :



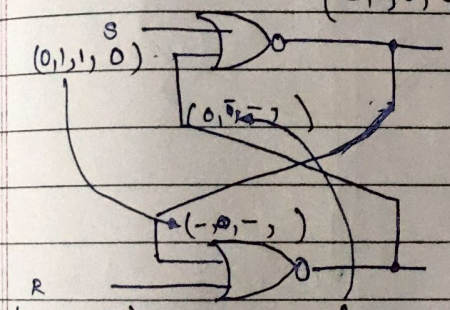
NOR		
0	0	1
0	1	0
1	0	0
1	1	0

$1+0 = 0$

$1+1 = 0$

S	R	$Q(n+1)$
0	0	Hold state $(Q + \bar{Q})$
0	1	0
1	0	1
1	1	Invalid

$(1,0,0, \overline{0+Q}) = \bar{Q}$



$(0,1,0, \overline{0+\bar{Q}}) = Q$

4th (0,0).

$(0+\bar{Q}) = \bar{Q}$

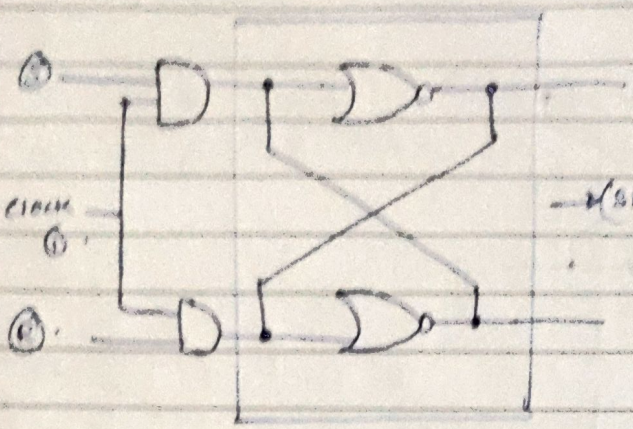
$(\overline{0+\bar{Q}}) = 1-\bar{Q}$

$= Q$.

AND

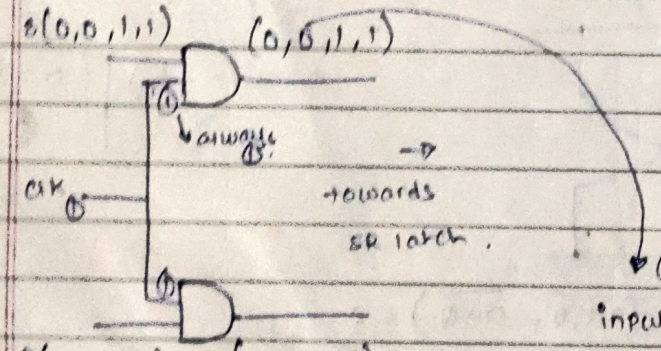
0	0	0
0	1	0
1	0	0
1	1	1

* SR flip flop using NOR gate.



(SR latch using NOR)

Clock	S	R	$Q_{(next)}$
OFF	—	—	Q_n → same output as previous.
ON	0	0	Hold
	0	1	0
	1	0	1
	1	1	Invalid.



input for latch. → we get this data from extra AND gates of SR FF

S	R	
0	0	hold
0	1	0
1	0	1
1	1	Invalid.

↑ output of latch

(SR)

0 0 → hold
0 1 → 0
1 0 → 1
1 1 → Invalid

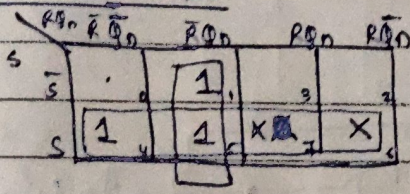
Characteristics Table

* expression last column is also based on SR values only, based on ep 7.7.

S	R	Q_n	$Q_{(n+1)}$	
0	0	0	0	hold same value
0	0	1	1	
0	1	0	0	reset
0	1	1	0	
1	0	0	1	set
1	0	1	1	
1	1	0	X	Invalid
1	1	1	X	

* 0 0 → hold same value.
* 0 1 → 0 (reset).
* 10 → 1 (set).

Characteristics eqn.



Based on above T.T, 1 mark points where we get 1 in column (4) i.e. Q_{n+1}.

* also mark don't care.

⇒ $S + \bar{R}Q_n$ ⇒ characteristic eqn of SR

Excitation Table.

(reverse characteristics table), place value of S & R according to charac. table of values of Q_n & Q_{n+1}

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

∴ at (00 & 01) SR, Q_n & Q_{n+1} is (00). thus for S=0, R=X.

∴ at (01) SR Q_n & Q_{n+1} = (10)

∴ at (00, 10) SR Q_n & Q_{n+1} = (11) ∴ S = X, R = 0.

∴ at (10) SR Q_n & Q_{n+1} is (01)

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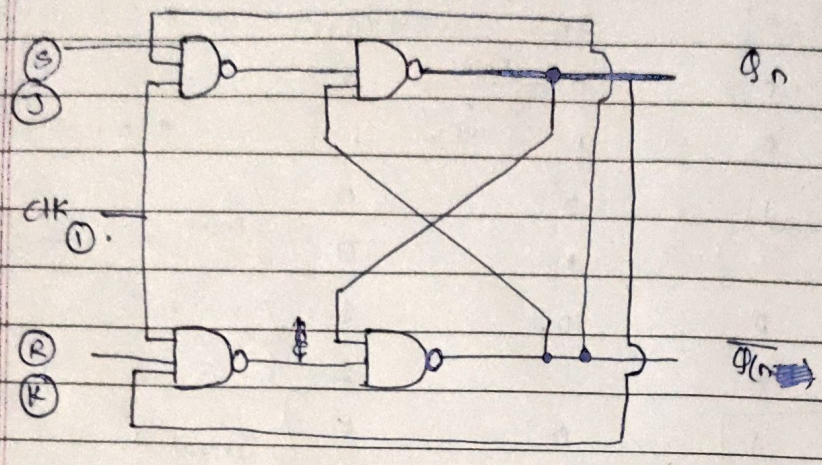
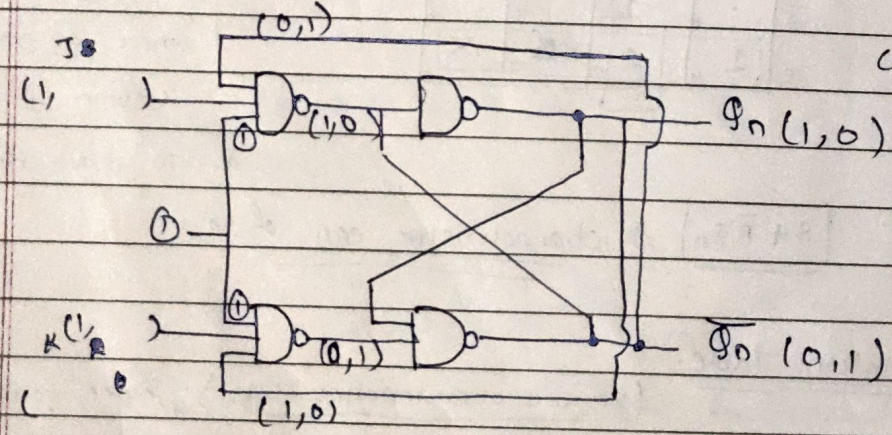
JK - Flip Flop → 75% SR Flip Flop (to correct 'Invalid' issue in SR)



JK Flip flop.

* take Q_n and input it to extra Nand (R)
* take $\overline{Q_n}$ and input it to extra Nand (S).



Case 1 $Q_n = 1$

latch → SR.

$Q_n = 1$	1	0	→ $Q_{n+1} = 0$.
$Q_n = 0$.	0	1	→ $Q_{n+1} = 1$.

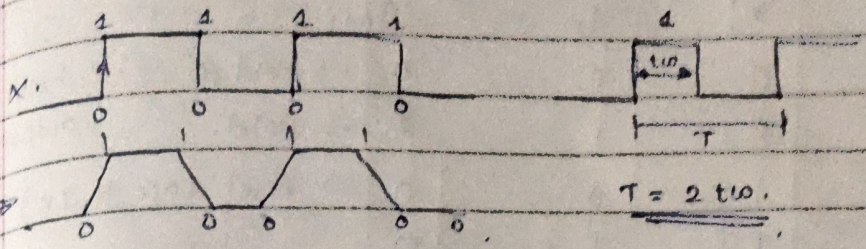
J	K	Q_{n+1}
0	0	Hold
0	1	0
1	0	1
1	1	$\overline{Q_n}$

→ same as SR ~~latch~~.

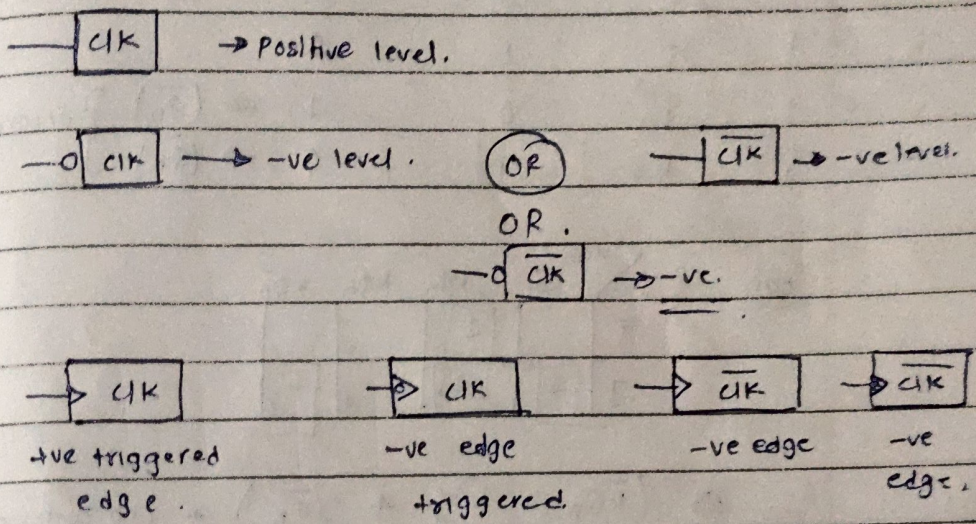
Types of triggering

① Edge → -ve & +ve

② level → low & high.



$T = 2\,t_{ON}$.



JK		
0	0	Hold
0	1	0
1	0	1
1	1	$\bar{Q}_n$

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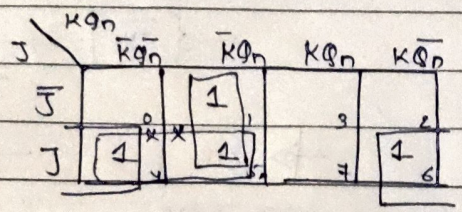
* Characteristics table of JK flipflop.
  ↳ based on T.T of JK flipflop only!

based on JK T.T

	J	K	Q_n	Q_{n+1}	
	0	0	0	0 → Hold 0 ; i.e. hold previous output	
1 ✓	0	0	1	1 → Hold.	
	0	1	0	0 → Reset (acc to JK)	
	0	1	1	0	
4 ✓	1	0	0	1 → set (acc to JK)	
5 ✓	1	0	1	1	
6 ✓	1	1	0	1 → $(\bar{Q}_n)$	according to JK T.T
	1	1	1	0 → $(\bar{Q}_n)$	

eqn



⇒ $(\bar{K}Q_n + J\bar{Q}_n)$ ← characteristics eqn.

* Excitation Table.

Q_n	Q_{n+1}	J	K	
0	0	0	x	--- (00, 01) at Q_n & Q_{n+1} = 00
0	1	1	x	(10, 11) at Q_n & Q_{n+1} = 01
1	0	x	1	(01, 11) at Q_n & Q_{n+1} = 10
1	1	x	0	(10, 00) at Q_n & Q_{n+1} = 11

→ Check for Q_n & Q_{n+1} value in charac. tables & accordingly fill J & K values.
→ If we have more than 1 value for J & K at some Q_n & Q_{n+1} -- put (x).

t_d = delay

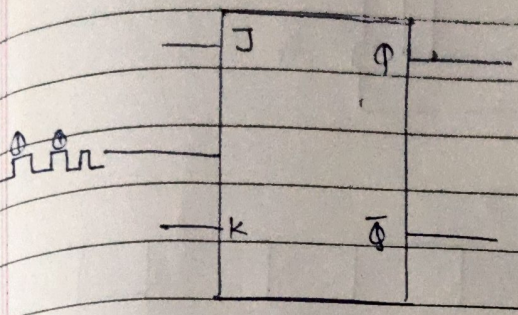
T_w = time of clock.

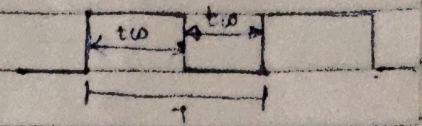
Race Around condition

① level triggered J-K flip flop.

② when J = K = 1 (Toggle) ($\bar{Q}_n$)

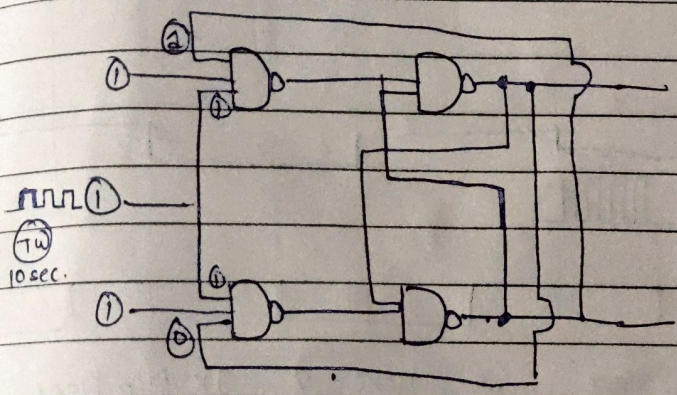
③ $T_w >> T_d$.





($T = 2t_w$)

* delay taken by FF to process input = T_d.



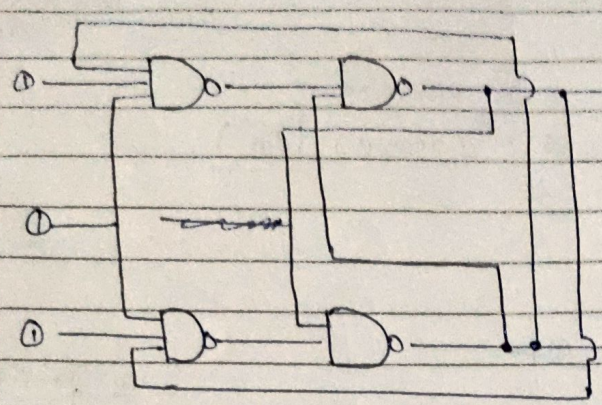
2 sec

$T_w >>> T_D$

as T_w is greater, again circuit will run considering the output 1 for Q & 0 for $\bar{Q}_n$ that is new outputs & again change value for Q_n & $\bar{Q}_n$

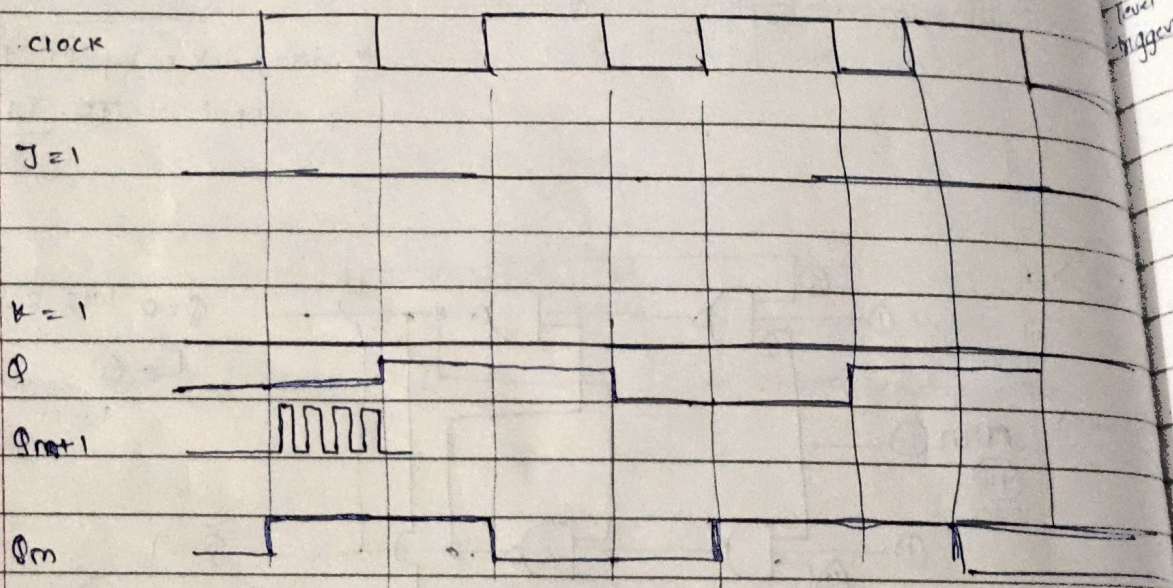
* Race around.

* Master slave → (To solve Race around condition.)



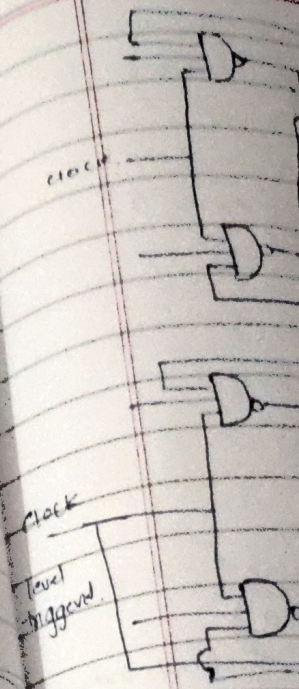
① J & K = 1
② level triggered
③ $T_{LO} >> T_d$.

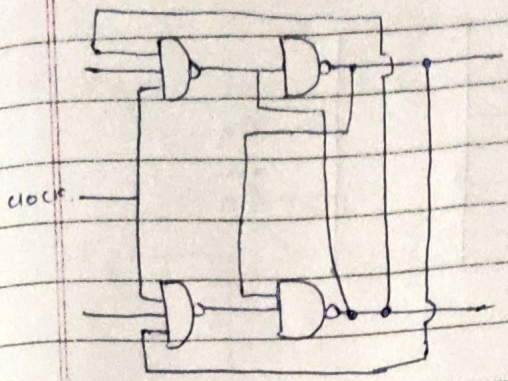
Logic 1, 0, 1 and changes.



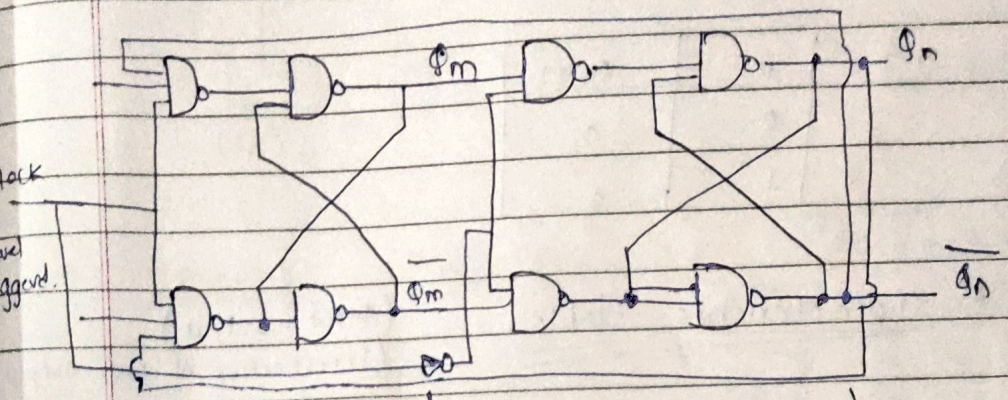
* Master & slave we have 2 JK flip flops, & now the slaves Q_n & $\bar{Q}_n$ goes to Masters extra Nand Input. as shown in diagram

* And for clock of slaved JKFF, we put a not gate to clock.





Basic JK FF.



Not to clock.

slave connected to master.

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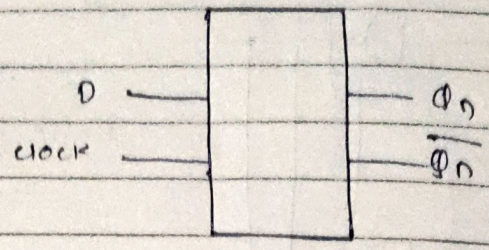
* D FlipFlop

(storage device)



(input == output)

7-1

D	Q_{n+1}
0	0
1	1

* Characteristics table. (input = output) (irrespective of prev. output)

D	Q_n	Q_{n+1}	
0	0	0	same as D.
0	1	0	
1	0	1	
1	1	1	

$\therefore$ $Q_{n+1} = D$ ← characteristic eqn.

* Excitation table

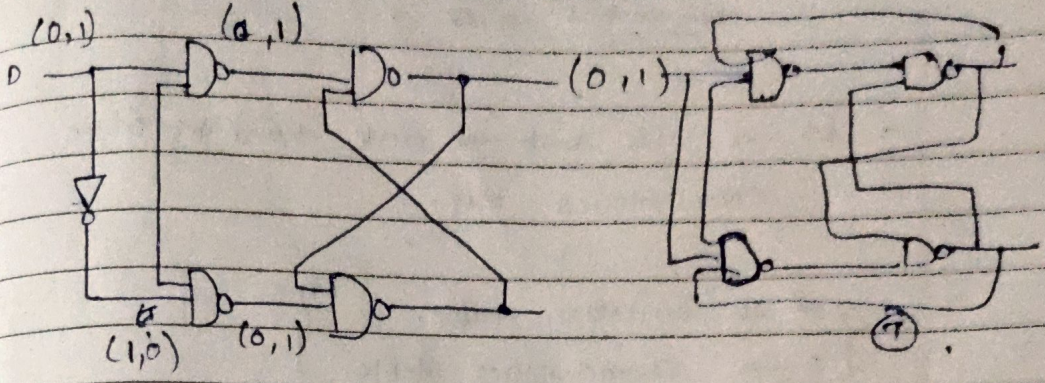
Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

(based on charc. table)

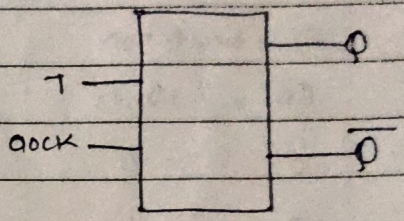
because, ($Q_{n+1} = D$)
output = input)

we consider latest Output.

Diagram from (SR).



T Flipflop (Toggle FF)



T	Q_{n+1}	
0	Q_n	← same as previous output.
1	$\overline{Q_n}$	← comp. of previous output

Characteristic table

T	Q_n	Q_{n+1}	
0	0	0	T=0, $Q_{n+1} = Q_n$
0	1	1	T=1, $Q_{n+1} = \overline{Q_n}$
1	0	1	XOR
1	1	0	

Characteristic eqn ⇒ XOR gate truth table.

$$T \oplus Q_n$$

excitation table

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

based on charc. table take values of Q_n & Q_{n+1} & compare it to T values.

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Given ↓ required ↓

SR to D conversion

↓

characteristics of SR

* SR ko kis tarah se excite karu ki D ke characteristics mile.

{ SR → excitation table.
D → characteristics table. }

SR - excitation

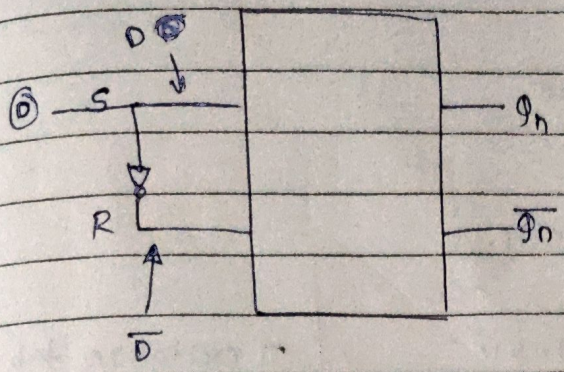
Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

D - characteristics table.

D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

(according to Q_n & Q_{n+1} write the SR execution table.)

D	Q_n	Q_{n+1}	S	R
0	0	0	0	X
0	1	0	0	1
1	0	1	1	0
1	1	1	X	0



D & Q_n → input , S, R Output.

SR eqn

(S)

	$\bar{Q}_n$	Q
$\bar{D}$		
D	1	X

⇒ D eqn.

S is 1 at 10 & 11

,

(R)

	$\bar{Q}_n$	Q
$\bar{D}$	X	1
D		

R is 1 at 01 & 00

$= \bar{D}$ eqn

given → excite.

JK → characteristics.

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T Flip Flop to JK :

given → required

✓ T excitation table.

✓ JK characteristic table.

based on Q_n & Q_{n+1} JK charac. table.

values of JK	J	K	Q_n	Q_{n+1}
0 ←	0	0	0	0
0	0	0	1	1
0	0	1	0	0
1	0	1	1	0
1	1	0	0	1
0	1	0	1	1
1	1	1	0	1
1	1	1	1	0

T excitation table

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

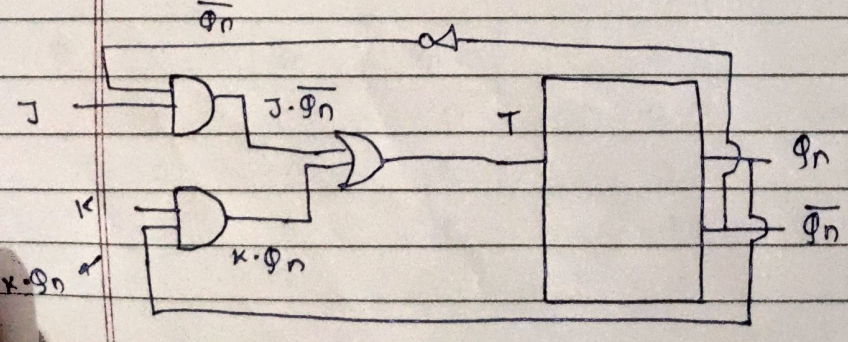
XOR

eqn

characteristic eqn of JK. for T. so T is 1 at (3, 4, 6, 7)

	$\bar{K}Q_n$	$\bar{K}\bar{Q}_n$	KQ_n	$K\bar{Q}_n$
$\bar{J}$	0	1	1 (3)	2
J	1 (4)	5	1 (7)	1 (6)

$(K Q_n + J \bar{Q}_n)$ ← T is high for JK



according to eqn.

* Clear & Preset are asynchronous.

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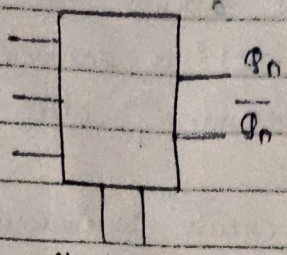
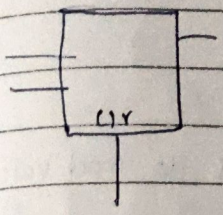
Clear & Preset pin



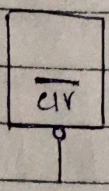
Clear → make output = 0.

Preset → make output = 1.

high enabled



low enabled.



similar for Preset.

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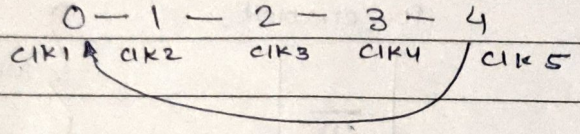
Counters :

- counter is a device that stores & displays the no. of times a particular event or process has occurred, often in relationship to clock.
- A counter circuit is usually constructed of a number of flipflops connected cascadely.

* How to find the MOD value of counter?

⇒



* Mod – number of different states is mod value.

∴ here MOD = 5.

* After applying 21 clock pulse, what is output.

∴ according to Mod, after 5, it gets into starting state again.

∴ 21th position is 1.

* How to find no. of flip flops required to design Mod – n counter?

⇒

2^n > Mod value.

n = no. of flip flops required.

∴ for Mod – 5

∴ $2^3 = 8$ > 5

∴ 3 flipflops required.

Mod – 272 given

∴ $\log_2(272)$

= 8.. – –

(∴ take upper value)

∴ = 9.

eg: 0-1-4-8-5

if we had value lower than 8 then 8 ff. but 8 has 4 bits hence here we need 4 FF.

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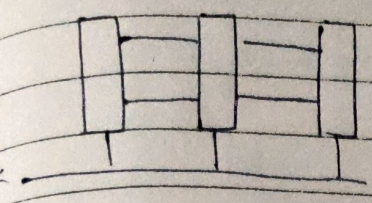
edge triggered

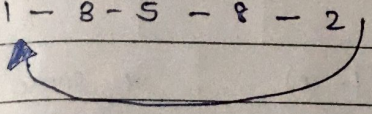
synchronous vs Asynchronous

synchronous



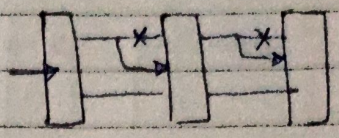
* same clock pulse for all.
* either all +ve clock or -ve.
* we can skip some stages & move.

eg: 1 - 8 - 5 - 8 - 2



* faster
* complex design
* high cost
* Ring, Twisted ring, Jhonson counter
* less delay

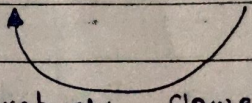
Asynchronous.



* Output goes in as a clock rather than input to next.
* further ~~counter~~ FF will get high based on prev. output.
* sequence up or sequence down.

We traverse sequentially only

eg ⇒ 1-2-3-4-5

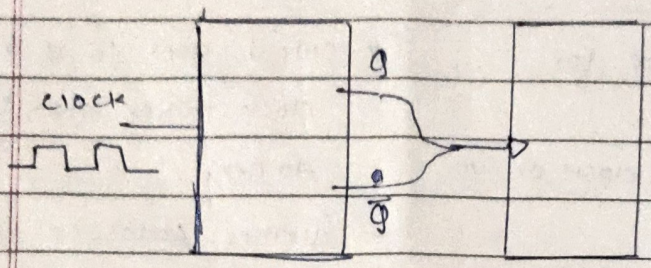


* comparatively slower.
* easier design
* low cost
* Ripple counter.
* more delay.

* Asynchronous → up & down counter

up → 0 → 1 → 2 → 3.

down → 3 → 2 → 1 → 0.



either of
Q or $\bar{Q}$.

* edge triggered is only used.

	Q (+ve)	$\bar{Q}$ (-ve)
———		
——▷	down	up
———		
——▷	up	down

* some nature = down

* opp. nature = up.

0 0

MSB → ← LSB

Designing synchronous counter (eg: 0 - 1 - 3 - 2)

→ 4 states, & max no → 2 bits

2 flip flops required $2^n = 4$.

$n = 2$

input is
D_1 & D_0 only

using D Flip Flops

2 FF (PS)		Next state.		of (b). excitation table	
Q_1	Q_0	Q_1^+	Q_0^+		
0	0	0	1	0 0	0
0	1	1	1	0 1	1
1	0	0	0	1 0	0
1	1	1	0	1 1	1

now next state number comes from (PS).

1st case we had 00 i.e. 0, then according to example after 0 we have 1, so next state of 0 is 1 ie. 01,

similarly, 2nd case we have 01 i.e. 1 to which next state should be 3 according to example

∴ we have 11 i.e. 3 in next state.

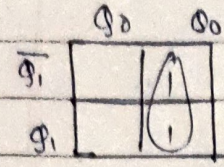
FF_1 (D_1)	FF_2 (D_0)	Q_1	Q_0	Q_1^+	Q_0^+
0	1	0	0	0	1
1	1	0	1	1	1
0	0	1	0	0	0
1	0	1	1	1	0

∴ according to excitation table, plot D_1 on Q_1 & Q_1^+

D_2 on Q_2 & Q_2^+

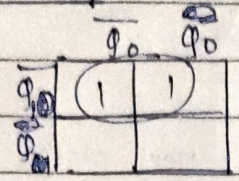
eqn

D_1 = input Q_1 & Q_0

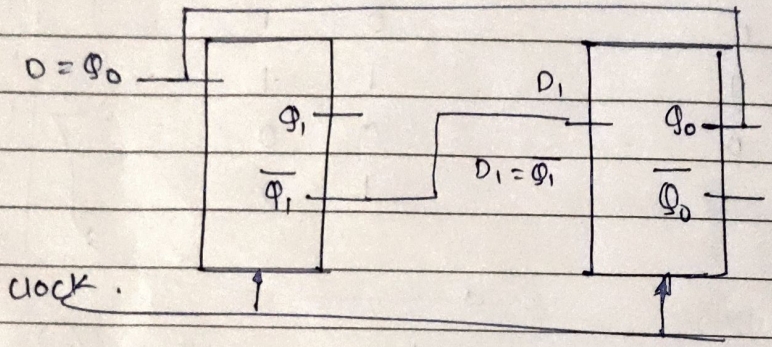


$\Rightarrow Q_0 \cdot D_1$

D_0 =



$= \bar{Q}_1 = D_0$



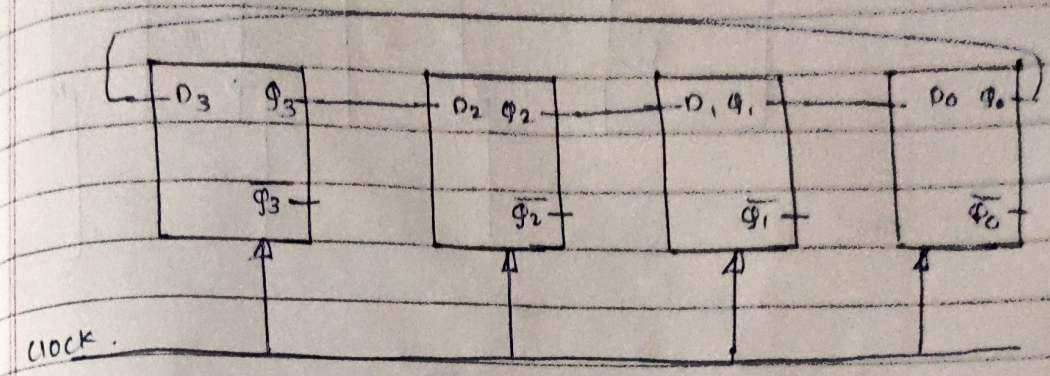
1-3-5-2 → 3 FF.

			D_2	D_1	D_0
0	0	0	x.		
0	0	1	0	1	1
0	1	0	0	0	1
0	1	1	1	0	1
1	0	0	x		
1	0	1	0	1	0
1	1	0	x		
1	1	1	x		

Ring Counter → Synchronous Counter.

→ D FF used

→ 4 bit ring counter.



$$Q_3^+ (n+1) = D_3 = Q_0 (n).$$

$$Q_2^+ (n+1) = D_2 = Q_3 (n)$$

$$Q_1^+ (n+1) = D_1 = Q_2 (n).$$

* If you start with 0, it will continue always as zero.

Q_3	Q_2	Q_1	Q_0.
0	0	0	0
0	0	0	0
1	0	0	0
0	1	0	0

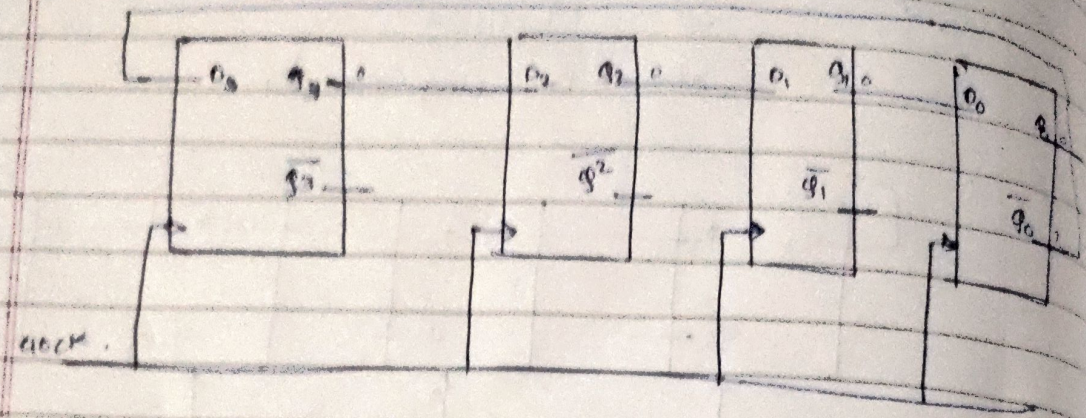
n bit ring counter = Mod-n.

no. of states = n.

4 bits has 16 combination 2^n possible states.

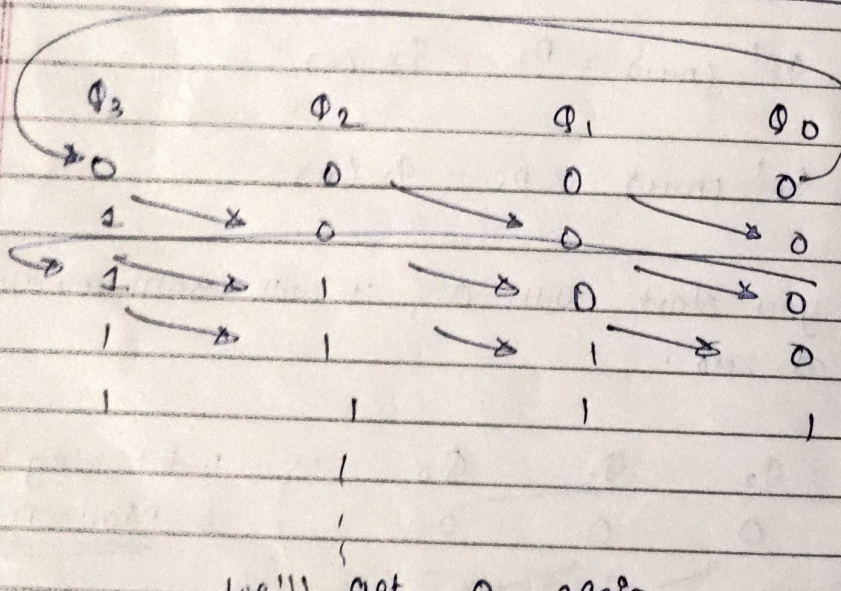
($2^n - n$ → un usable states)

* Twisted ring / Jhonson counter



Here we connect $\overline{Q_0}$ to D_3

In Ring we connected Q_0 to D_3



∴ 4 bit Jhonson counter → 8 states

Mod – 2n → different states

Total 2^n possible states.

Shift Registers

- S.R. are used in arithmetic operations
- eg: left shift, Right shift.
- Basic F.F. used is D FF

* left shift = x by 2.
* Right shift = ÷ by 2.

Mode	clocks need for n bit shift register		
	loading	Reading	Total.
SISO	n	n-1	2n-1
SIPO	n	0	n
PISO	1	n-1	n
PIPO	1	0	1

S = serial. P = parallel
I = input O = output

* SISO → n bit to n clock correspondance.
  → values to load n clocks (to n values)
  → values to read n-1 clocks.

* SIPO → values to load n clock
  → to read we have parallel output, each output can be accessed easily thru 0 clocks
* PISO → parallel input only one clock can do input
  → n-1 to read

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* PIPO → on one clock all will get loaded.
→ 0 for output.
+ 1 clock for loading all.

---

① SR → D.
E ↓ C ↓

Q_n	Q_{n+1}	S	R	D
0	0	0	X	0
0	1	1	0	0
1	0	0	1	1
1	1	X	0	1

② JK → D
E ↓ C ↓

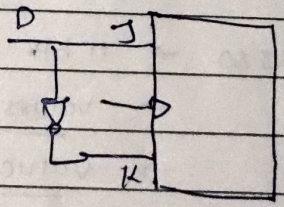
Q_n	D	Q_{n+1}
0	0	0
0	1	1
1	0	0
1	1	1

$D = Q_{n+1}$

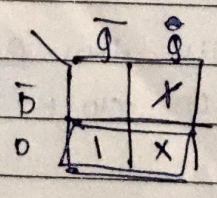
JK → E.

D	Q_n	Q_{n+1}	J	K
0	0	0	0	X
1	0	1	1	X
0	1	0	X	1
1	1	1	X	0

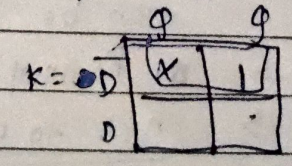
← based on chart table of JK



~~J=K=D~~ J is high at (10, 01, 11)
K is high at (00, 10, 01)
x x



J = D



K = $\bar{D}$

③ D to JK

q_n	q_{n+1}	D	$q_{n+1} = D$
0	0	0	
0	1	1	
1	0	0	
1	1	1	

J	K	q_n	q_{n+1}	D
0	0	0	0	0 (hold 0)
0	0	1	1	1
0	1	0	0	0
0	1	1	0	0
1	0	0	1	1
1	0	1	1	1
1	1	0	1	1
1	1	1	0	0

q_n	q_{n+1}	J	K	D
0	0	0	X	0
0	1	1	X	1
1	0	X	1	0
1	1	X	0	1

D is high at (01, 11) of q J K.

D is high for (01x, 10x)

011, 010, 110, 100

	$\bar{J}\bar{K}$	$\bar{J}K$	JK	$J\bar{K}$
$\bar{q}$			1	1
q	1			1

$\bar{q}J\bar{K} + qJ\bar{K}$

$J\bar{K}$ ($\bar{q} + q$)

$J\bar{K}$

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(4)* SR-T

(E) (C)

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

(T) →

T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

$T=0,\ Q_{n+1} = Q_n$

$T=1\ \ Q_{n+1} = \bar{Q}_n$

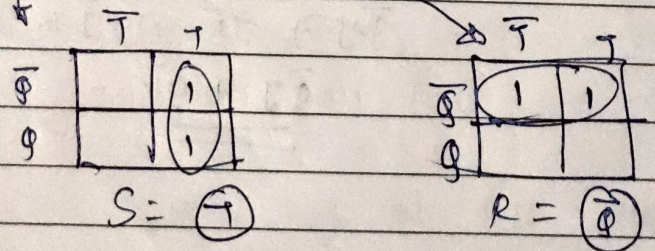
↳ XOR ⇒ $T \oplus Q_n$

⇒

Q_n	Q_{n+1}	T	S	R
0	0	0	0	X
1	1	0	1	0
0	1	1	0	1
1	0	1	X	0.

S is high at (01, 10) (TQ_n)

R is high at (00, 01)



S = $\bar{T}$ R = $\bar{Q}$.

eqn. according T.

(5) JK → T (4) (6)

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

T-C

T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

JK can Job SR high.

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* JK → SR
E C.

JK

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

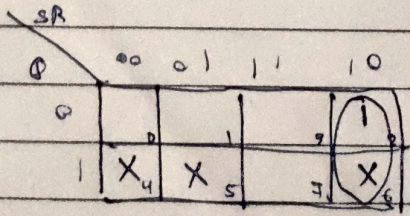
SR

S	R	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	6	1	1
1	1	0	X
1	1	1	X

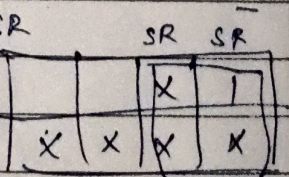
Q_n	Q_{n+1}	S	R	J	K
0	0	0	X	0	X
0	1	1	0	1	X
1	0	0	1	X	1
1	1	X	0	X	0

highal 010, 101, 110, 100)

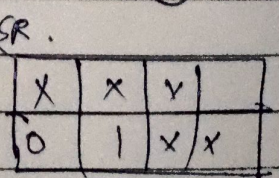
J → (~~000~~, ~~011~~, ~~0X01~~)



SR



= S.



{ Reset → 0
{ Set → 1

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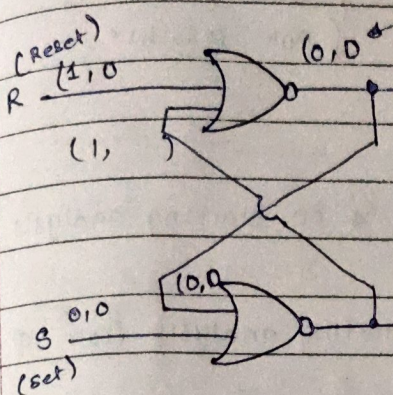
Module - 3

SR latch (NOR)

- the basic storeage element is called latch.
  It latches 0 & 1.



← because (0,1).

Q = 0,0

output of one goes as input to other

case 1 S=0 & R=1

∴ according to NOR TT. if any input is 1, output is 0.

∴ Q=0 & $\bar{Q}$ = 1.

NOR		
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

memory condition { S=0 & R=0. thus Q=0 & $\bar{Q}$ = 1.

case 2 : S=1 & R=0.

∴ If any input is 1, output to that gate is 0.

∴ $\bar{Q}$ = 0.

at R, we now have (0,0) = 1 = Q

now, S=0 & R=0 ∴ Q = ? & $\bar{Q}$ = ?

& Q in last cond^n = 1

$\bar{Q}$ = 0.

∴ at S, we have (0,1) = 0 ∴ $\bar{Q}$ = 0 } memory condition.
& at R, we have (0,0) = 1 ∴ Q = 1 }

inputs (S, Q).
(R, $\bar{Q}$)

not used

case 3 $S=1$ & $R=1$, $Q=?$ & $\bar{Q}=?$

∴ If any input is 1, output = 0.

∴ at $S=1 \rightarrow \bar{Q}=0$
at $R=0 \rightarrow Q=0$.
} same output is not possible.

~~on starting~~, $S=0$, $R=0$

∴ $Q=0$, $\bar{Q}=1$ ← on starting analysis with $\bar{Q}$

∴ $Q=1$, $\bar{Q}=0$ ← on starting analysis from Q.

S	R	Q	$\bar{Q}$
0	0	memory (same as before)	
0	1	0	1
1	0	1	0
1	1	Not used.	

---

① use 3 cases

② (0,0) = memory & (1,1) = invalid.

③ * if any input = 1, output = 0.

Nand → if any input is zero, output is 1.

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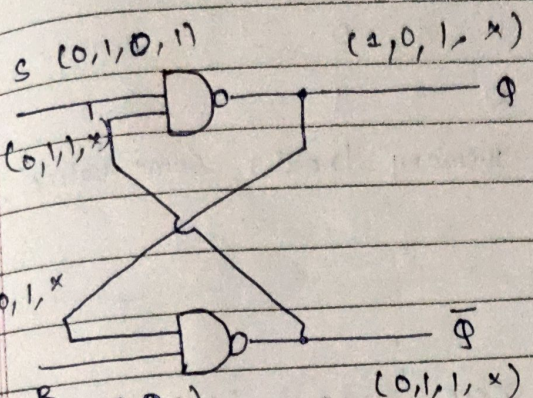
SR latch (Nand Gate)



Nand.		
A	B	Y.
0	0	1
0	1	1
1	0	1
1	1	0.

case 1 S=0, R=1

∴ if any input is 0, output is 1.

∴ at S, $Q = 1$.

∴ for R, input is (1, 1),

thus $\bar{Q} = 0$.

$Q = 1$ & $\bar{Q} = 0$.

case 2 S=1, R=0.

∴ if any input is 0, output is 1.

∴ at R, $\bar{Q} = 1$

∴ for S, input is (1, 1) i.e. $(S, \bar{Q})$ →

thus $Q = 0$

∴ $\bar{Q} = 1$, $Q = 0$.

case 3 at S=0, R=0.

∴ at S, $Q = 1$; at R=0, $\bar{Q} = 1$

∴ both outputs can't be same.

(Invalid state).

at S=1 & R=1

this is Hold. state.

at S → $(1, \bar{Q})$ R = $(1, Q)$.

⇒ $1 \cdot \bar{Q} = \bar{1} + \bar{Q}$ } S

$= 0 + Q = Q$

$1 \cdot Q = 0 + \bar{Q}$ } R

$= \bar{Q}$

Hold

S	R	Q	$\bar{Q}$
0	0	Invalid / not used.	
0	1	1	0
1	0	0	1
1	1	memory holds same value.	

① If any input is zero, output is 1.

② (1, 1) memory state

→ S ⇒ 1, $\bar{Q}$ = input.

applying nand.

$\overline{1 \cdot \bar{Q}} = \bar{1} + \bar{\bar{Q}}$

$= 0 + Q = Q$ } same output.

R ⇒ 1, Q = input

applying nand.

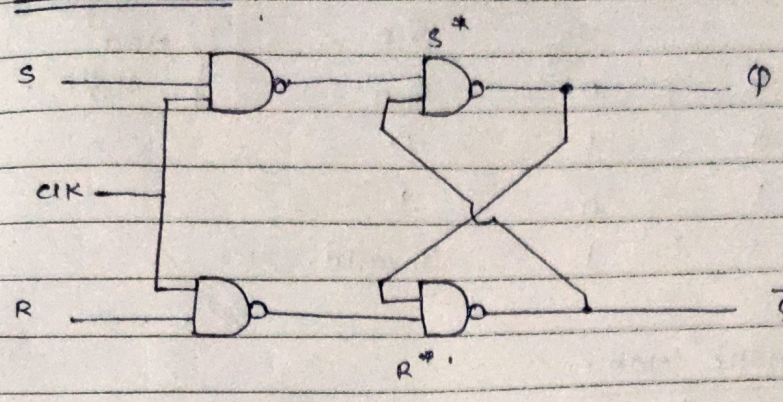
$\overline{1 \cdot Q} = \bar{1} + \bar{Q}$

$= \bar{Q}$ → same output.

③ To find T.T.

using 3 cases.

SR Flipflop



S*	R*	Q	Q̄
0	0	Invalid	
0	1	1	0
1	0	0	1
1	1	Memory	

∴ at S* → input is $(\overline{S \cdot CLK})$ according to Nand Gate.

$$S^* = (\overline{S \cdot CLK})$$
$$= \overline{S} + \overline{CLK}$$

at R* → input is $(\overline{R \cdot CLK})$ according to Nand Gate.

$$R^* = (\overline{R \cdot CLK})$$
$$= \overline{R} + \overline{CLK}$$

Truth table

CLK	S	S*	R	R*	Q	Q̄
Low	–	–	–	–	Memory	
High	0	(1)	0	(1)	Memory state.	(comes according to SR latch)
	0	(1)	1	(0)	0	1
	1	(0)	0	(1)	1	0
	1	(0)	1	(0)	Invalid state.	

∴ when clock is 1.

$S^* = \overline{S}$ & $R^* = \overline{R}$.

when S = 0 $S^* = 1$ $R = 0$, $R^* = 1$

S = 1 $S^* = 0$ $R = 1$, $R^* = 0$.

* SR F.F. truthtable comes from T.T.
* ① find eqn for S^* w.r.t S & R^* w.r.t R.
② $S^* = \bar{S}$ & $R^* = \bar{R}$.
③ T.T. according to SR latch.

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* Truthtable

clk	S	R	Q_{n+1}
0	–	–	Q_n
1	0	0	Q_n
1	0	1	0
1	1	0	1
1	1	1	Invalid.

} Hold state.

* Characteristic table.

Inputs.			Output.	
Q_n	S	R	Q_{n+1}	
0	0	0	0	} Hold state.
0	0	1	0	} reset
0	1	0	1	} set
0	1	1	X	} Invalid.
1	0	0	1	} Hold $Q_{n+1} = Q_n$
1	0	1	0	
1	1	0	1	
1	1	1	X	

* charac. table consider (SR) only for output.
* the output column is based on SR FF T.T.

* Charac. eqn: Based on above T.T., mark points where we get (1 in Q_{n+1})
* consider dont care also.

Q_n \ SR	$\bar{S}\bar{R}$	$\bar{S}R$	SR	$S\bar{R}$
$\bar{Q}_n$	0	1	X 3	1 2
Q_n	1 4	5	X 7	1 6

$\Rightarrow S + \bar{R}Q_n$

charc. eqn. for SR.

Q_{n+1} is high at $\Rightarrow$ 2, 3, 4, 6, 7.
(3, 7 are X)

Excitation Table : (determined by charac. table)

Inputs		outputs		
q_n	q_{n+1}	S	R	SR
0	0	0	X	... (00, 01)
0	1	1	0	(10, x).
1	0	0	1	(01, x)
1	1	X	0	(00, 10)

* place value of S & R according to charac. table values of (q_n & q_{n+1})

* If value contradicts put a (X).

① create latch
→ create T.T. according to gate (cases).

② create F.F.
→ create T.T. according to latch inputs & gates used.

③ charac. table based on T.T. of F.F.

④ Excitation table based on char. table.

① stores the same ... input.

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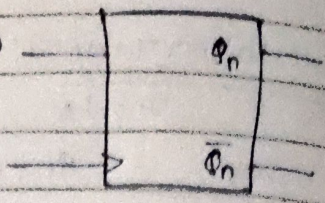
D flip flop (storeage F.F).

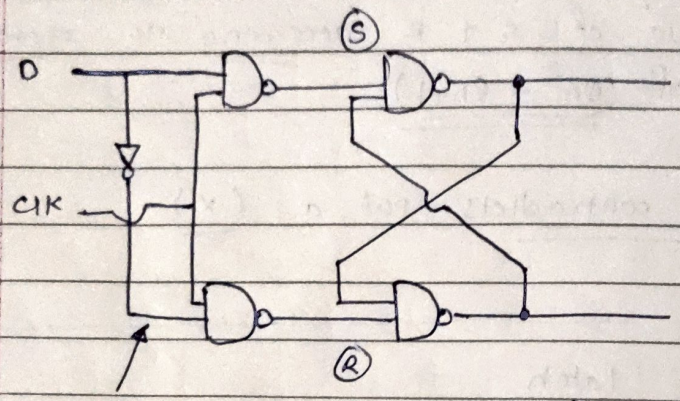
Input = output



→ SR to D.

① similar to SR flip flop.

② we consider only one input, other input is its compliment.



Truth table of D FF.

CLK	D	Φ_{n+1}.	
0	x	Φ_n	
1	0	0	same input & output
1	1	1	

$D = \Phi_{n+1}$

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Characteristic table

D	q_n	q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

Input = Output

∴ characteristic eqn = $q_{n+1} = D$.

Excitation table

q_n	q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

∴ according to charact. table,

SR	CLK	S	R	Q_{n+1}	Q_n
	1	0	0		Q_n
	1	0	1		0
	1	1	0		1
	1	1	1		Invalid.

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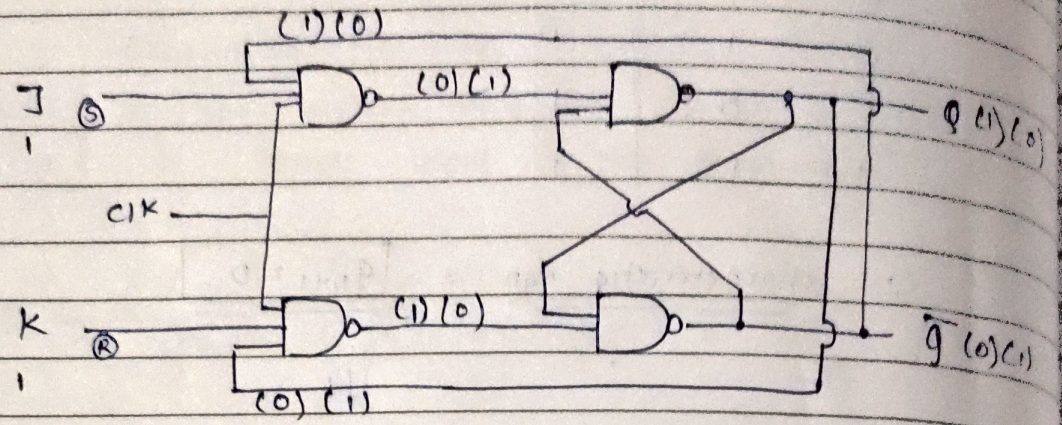
JK FF

① Adv ⇒ we don't have Invalid state at (1,1) position like SR F.F.



* Similar to SR F.F.

① take Q as input in R(K) (3 inputs now in R (K))

+

$\bar{Q}$ as input in S(J) (3 inputs in S) (J)

(S = J , R = K)

case 1) CLK = 0 → Memory state.

at CLK = 1

case 2) J = 1 & K = 0

For nand, any input = 0, output = 1.

$Q = 1$, $\bar{Q} = 0$. ∴ according to SR FF TT.

case 3) J = 0 , K = 1 , $Q = 0$, $\bar{Q} = 1$

↳ according to SR FF TT.

∴ In J·K F.F) First three cases are same as SR FF.

charac table based on T-T.

Excitation table based on char table.

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* case 4) J=1 & K=1.

assume Q=0 & $\bar{Q}$=1.

The output we get is 1,0

= (Q=1 & $\bar{Q}$=0)

now, the Q=1 & $\bar{Q}$=0.

∴ J=1, K=1 Q=1 & $\bar{Q}$=0.

∴ according to this. Q & $\bar{Q}$ becomes.

Q=0 & $\bar{Q}$=1.

∴ we get complement of previous state.

i.e. toggle.

∴ Truth table → 1st 3 cases same as SR.

CLK	J	K	Q_{n+1}	
0	x	x	Q_n	memory
1	0	0	Q_n	
1	0	1	0	
1	1	0	1	
1	1	1	$\overline{Q_n}$	toggle state.

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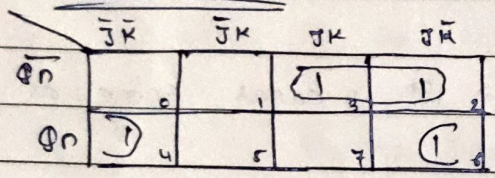
* characteristic table → based on T.T. of JK

Q_n	J	K	Q_{n+1}	
0	0	0	0	hold state
0	0	1	0	
0	1	0	1	
0	1	1	1	toggle state
1	0	0	1	
1	0	1	0	
1	1	0	1	
1	1	1	0	

J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

charac. eqn → mark when $Q_{n+1} = 1$.



$\Rightarrow J\bar{Q}_n + \bar{K}Q_n$

Q_{n+1} high at ⇒ 2, 3, 4, 6.

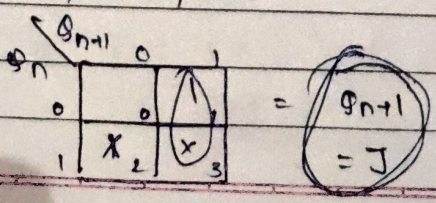
* Excitation table → (based on charac. table) (multiple value = x)

Q_n	Q_{n+1}	J	K
0	0	0	x (00, 01)
0	1	1	x (10, 11)
1	0	x	1 (01, 11)
1	1	x	0 (00, 10)

according to excitation table

eqn for J

J → 1, 2(x), 3(x)

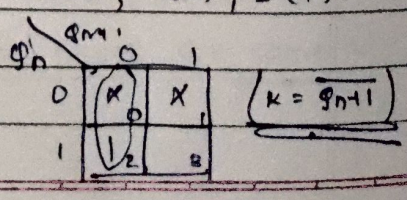


$= Q_{n+1} = J$

$J = Q_{n+1}$

eqn for K

K → 0(x), 1(x), 2(1).



$K = \bar{Q}_{n+1}$

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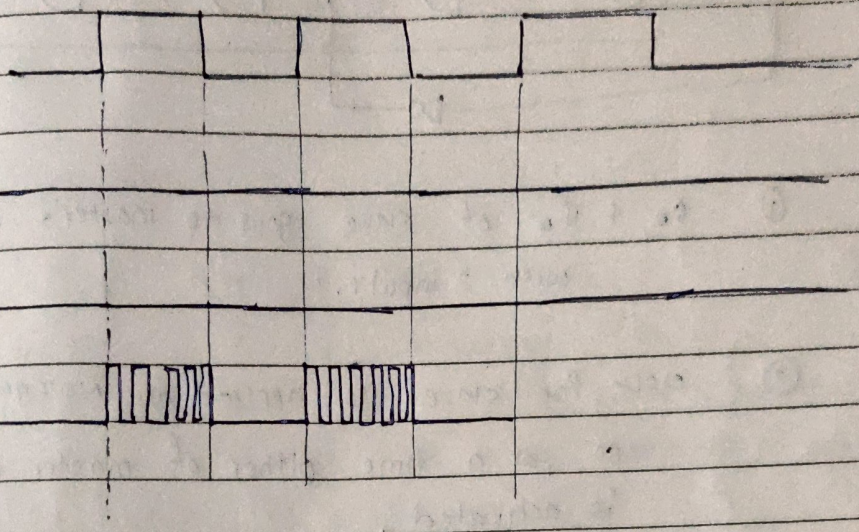
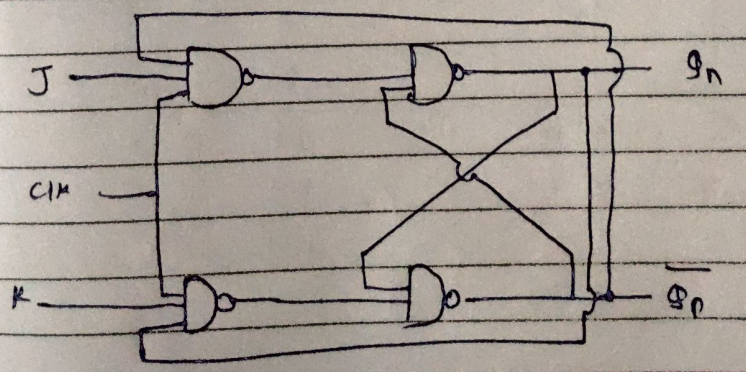
Race around condition

we need ① level triggered J·K. ~~/edge triggered~~.
② J=1 & K=1 [toggle state i.e. $\bar{Q}_n$].
③ clock T/2 > delay



Master slave → To overcome race around condition

① use 2 J·K. F·F.
② now, slaves Q_n & $\bar{Q}_n$ goes to masters Nand Gate with 3 inputs.
③ and for clock of slaves J·K, put a not gate to the clock of masters JK.



basic JK.

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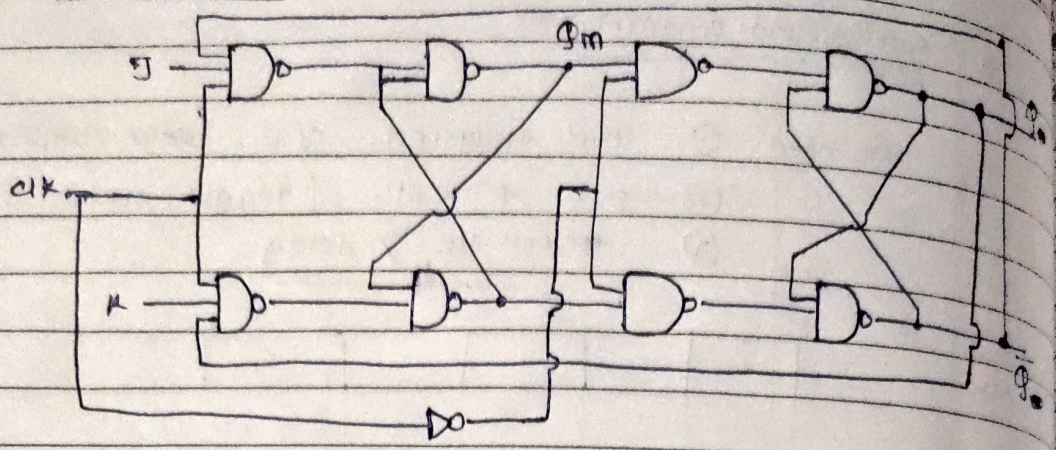
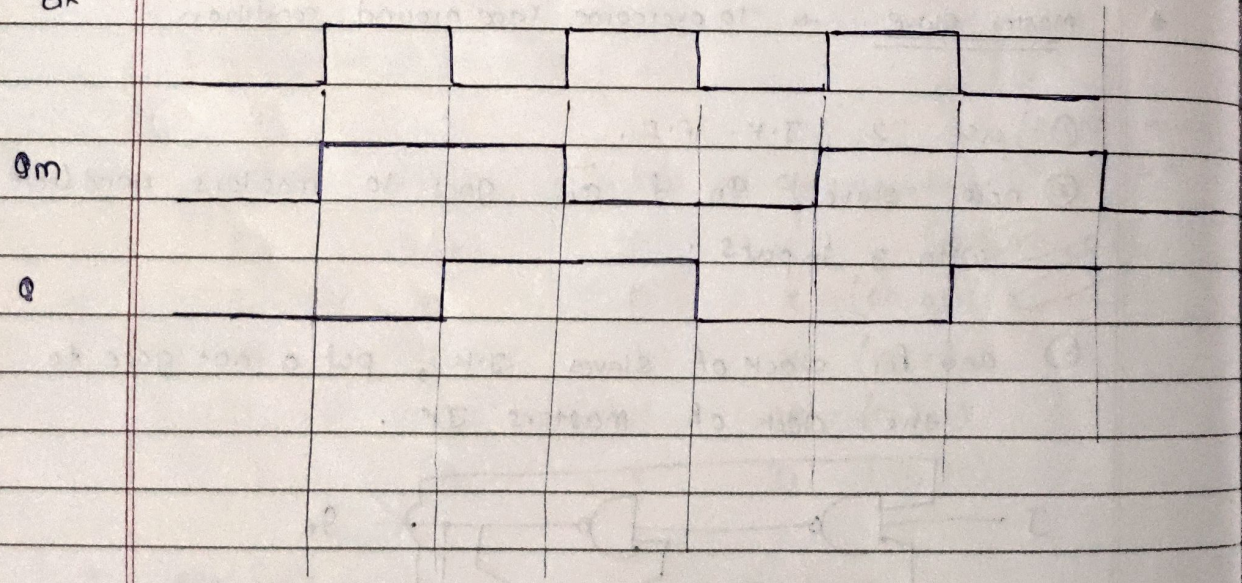
master slave JK

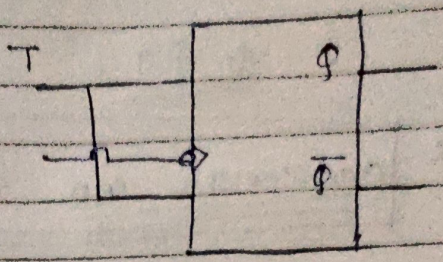


① Q & $\bar{Q}$ of slave goes to master's Nand Gate with 3 inputs.

② clock for slave is applied an NOT gate.
so, at a time either of master or slave is activated.



T flip flop → made from J & K.



Truth table.

clk	T	Q_{n+1}
0	x	hold state. (Q_n)
1	0	Q_n ← same as previous output
1	1	$\bar{Q}_n$ ← compliment of previous output

Characteristic table:

Inputs		output.	according to
Q_n	T	Q_{n+1}.	Truth table
0	0	0 (Q_n previous output)	at values of T.
0	1	1 ($\bar{Q}_n$)	
1	0	1 (Q_n)	
1	1	0 ($\bar{Q}_n$)	

Excitation table: based on characteristic table.

Q_n	Q_{n+1}	T.	
0	0	0	based on values from characteristic table.
0	1	1	
1	0	1	
1	1	0	

charact. input → FF & Q_n Out Q_{n+1}

excitation input → Q_n Q_{n+1} Out FF.

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∴ Q_{n+1} is high at odd values.

i.e. XOR gate.

∴ $Q_n \oplus T$

characteristic eqn → $Q_n \oplus T$

Flip Flop Conversion

① Identify available & Required F.F.

② make characteristic table of required F.F.

③ make excitation table of available FF.
(Now merge both tables)

④ boolean expression for available FF.

⑤ Draw circuit

eg JK to D.
available required.

→ D ff. characteristic table. → Excitation table of JK.

Q_n	D	Q_{n+1}
0	0	0
0	1	1
1	0	0
1	1	1

Q_n	Q_{n+1}	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

We know, D, D = Q_{n+1}

∴ merge tables.

Q_n	D	Q_{n+1}	J	K.
0	0	0	0	X
0	1	1	1	X
1	0	0	X	1
1	1	1	X	0

plot J. K. according to excitation table
&
values of Q_n & Q_{n+1}

* boolean ean. for available FF i.e. JK.

2→[2 variable K map.] inputs (Q_n & D)

↓ one for J
one for K.

For J

	$\bar{D}$	D
$\bar{Q_n}$	0	1
Q_n	X	X

J is high at 1, 2(x), 3(x)

= J = D

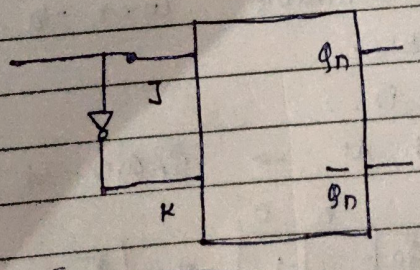
For K

	$\bar{D}$	D
$\bar{Q_n}$	0	X
Q_n	2	3

K is high at
0(x), 2(x), 2.

K = $\bar{D}$

∴



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* T F.F → D F.F
available required.

• characteristic table of required (D). $Q_{n+1} = D$

Q_n	D	Q_{n+1}
0	0	0
0	1	1
1	0	0
1	1	1

Excitation table of available i.e. T.

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

• for $Q_n = 0$,

basically T is XOR w.r.t to Q_n & Q_{n+1}

merge tables.

Q_n	D	Q_{n+1}	T.
0	0	0	0
0	1	1	1
1	0	0	1
1	1	1	0

** Get eqn. of available w.r.t to inputs of Charact. table.
i.e. Q_n & D.
∴ T is high at → 1 & 2.

Q_n \ D	$\bar{D}$	D
$\bar{Q}_n$	0	1 (1)
Q_n	1 (2)	0 (3)

$T = (\bar{Q}_n D + Q_n \bar{D})$