Myxa design notes

Phase signal sensing

This document describes main decisions when designing Myxa PMSM controller.

Sections:

MCU

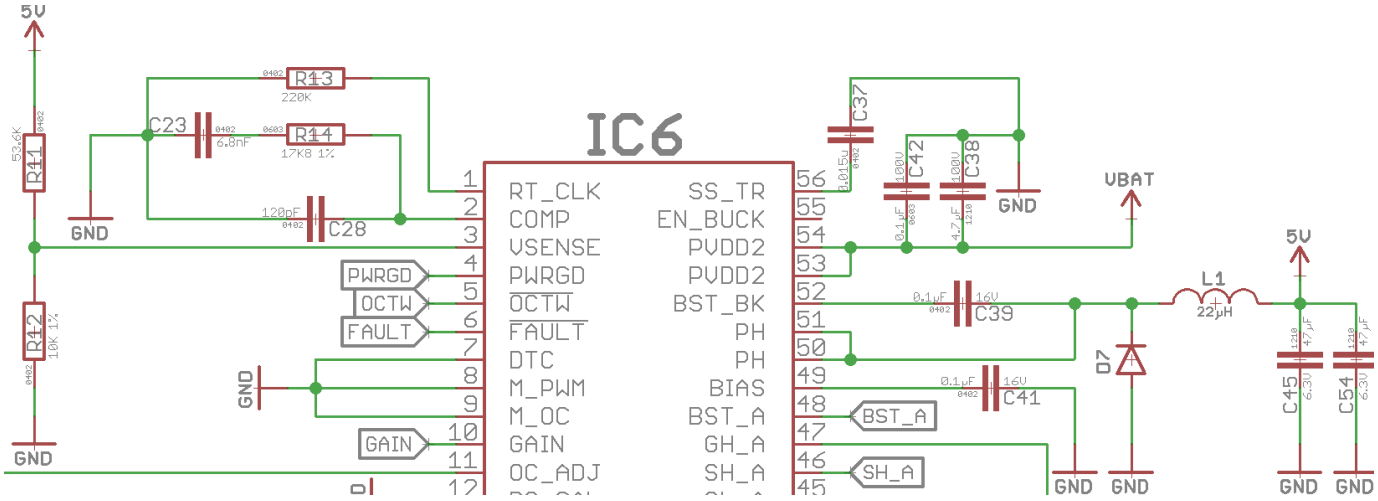
MYXA uses STM32F446 MCU, preferably with operating temperature range -40..+105C. Current boards though have only -40°C ~ 85°C MCU version. This is known issue and a least-evil solution due to the lack of proper MCUs in the world.

MCU is powered by dedicated 3.3V LDO.

VDDA is tied to reference voltage source REF3033. It may seem weird, but it is capable of providing up to 25mA current, so its ok.

Step-down converter

Step-down dc-dc converter is tps54160 embedded in DRV8302



Inductor SRP6540-220M (FIXED IND 22UH 2.5A 133 MOHM SMD)

Shottky diode: PMEG6020ER,115 (DIODE SCHOTTKY 60V 2A SOD123W)

Input:

Vin = 8..60V

Output:

R1 = 10K, R2 = 53,6K

Vout = 53,6/10 * 0,8 + 0,8 = 5,088V

Iout = 1.5A Max

Operating frequency:

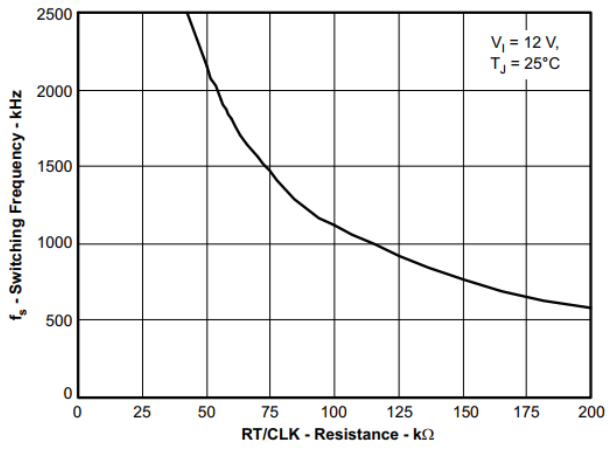


Figure 6. Switching Frequency vs RT/CLK Resistance High Frequency Range

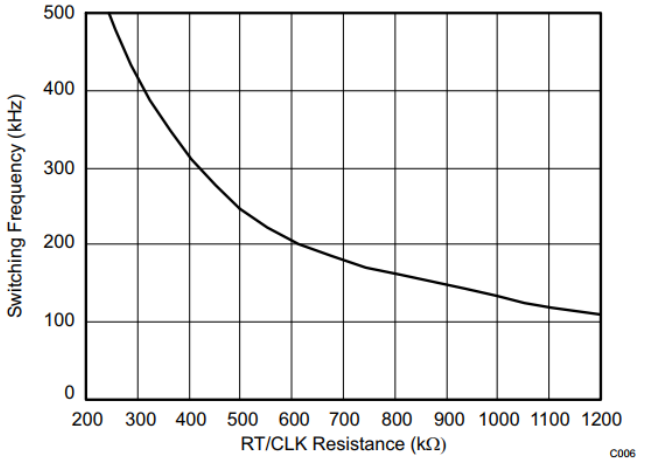
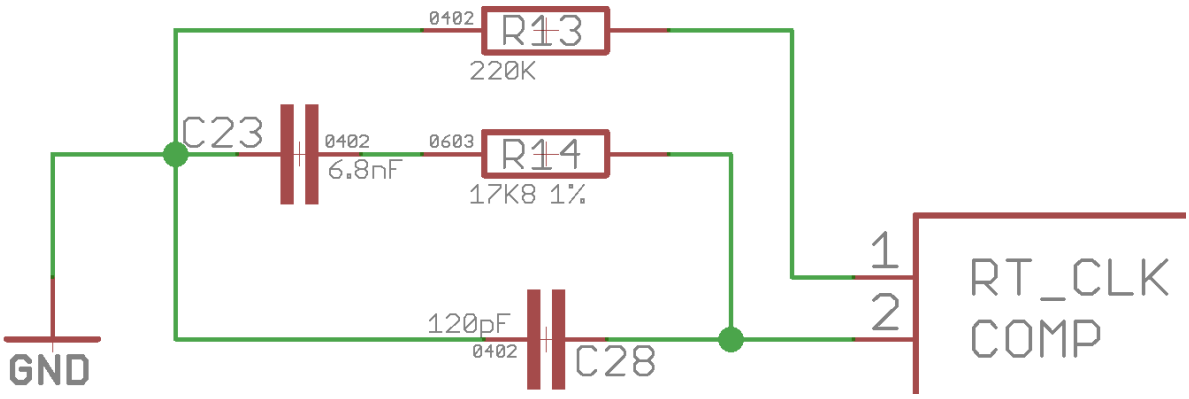


Figure 7. Switching Frequency vs RT/CLK Resistance Low Frequency Range

R rt/clk = 220K

F ~ 500 KHz

Compensation network



DRV8302

DRV8302 schematic is basically its reference schematic from datasheet

One of the differences are capacitors on current shunt amplifiers outputs. In MYXA they are 18pF.

Pins EN_GATE, PWRGD, OCTW, FAULD and GAIN are connected to MCU.

M_PWM, M_OC are set to LOW

DTC and DC_CAL are tied to GND

DRV8302 Reference voltage input is connected to the same voltage as MCU Vdda

Configuration pins description can be seen below:

Pin Functions

PIN		I/O(1)	DESCRIPTION
NO.	NAME		
1	RT_CLK	I	Resistor timing and external clock for buck regulator. Resistor should connect to GND (PowerPAD™) with very short trace to reduce the potential clock jitter due to noise.
2	COMP	O	Buck error amplifier output and input to the output switch current comparator.
3	VSENSE	I	Buck output voltage sense pin. Inverting node of error amplifier.
4	PWRGD	I	An open drain output with external pullup resistor required. Asserts low if buck output voltage is low due to thermal shutdown, dropout, overvoltage, or EN_BUCK shut down
5	nOCTW	O	Overcurrent and overtemperature warning indicator. This output is open drain with external pullup resistor required.
6	nFAULT	O	Fault report indicator. This output is open drain with external pullup resistor required.
7	DTC	I	Dead-time adjustment with external resistor to GND
8	M_PWM	I	Mode selection pin for PWM input configuration. If M_PWM = LOW, the device supports 6 independent PWM inputs. When M_PWM = HIGH, the device must be connected to ONLY 3 PWM input signals on INH_x. The complementary PWM signals for low side signaling will be internally generated from the high side inputs.
9	M_OC	I	Mode selection pin for over-current protection options. If M_OC = LOW, the gate driver will operate in a cycle-by-cycle current limiting mode. If M_OC = HIGH, the gate driver will shutdown the channel which detected an over-current event.
10	GAIN	O	Gain selection for integrated current shunt amplifiers. If GAIN = LOW, the internal current shunt amplifiers have a gain of 10V/V. If GAIN = HIGH, the current shunt amplifiers have a gain of 40V/V.
11	OC_ADJ	I	Overcurrent trip set pin. Apply a voltage on this pin to set the trip point for the internal overcurrent protection circuitry. A voltage divider from DVDD is recommended.
12	DC_CAL	I	When DC_CAL is high, device shorts inputs of shunt amplifiers and disconnects loads. DC offset calibration can be done through external microcontroller.

Overcurrent Protection (OCP)

7.3.4.1 Overcurrent Protection (OCP) and Reporting

To protect the power stage from damage due to excessive currents, V_{DS} sensing circuitry is implemented in the DRV8302. Based on the $R_{DS(on)}$ of the external MOSFETs and the maximum allowed I_{DS}, a voltage threshold can be determined to trigger the overcurrent protection features when exceeded. The voltage threshold is programmed through the OC_ADJ pin by applying an external reference voltage with a DAC or resistor divider from DVDD. Overcurrent protection should be used as a protection scheme only; it is not intended as a precise current regulation scheme. There can be up to a 20% tolerance across channels for the V_{DS} trip point.

$$V_{DS} = I_{DS} \times R_{DS(on)} \quad (2)$$

The V_{DS} sense circuit measures the voltage from the drain to the source of the external MOSFET while the MOSFET is enabled. The high-side sense is between the PVDD and SH_X pins. The low-side sense is between the SH_X and SL_X pins. Ensuring a differential, low impedance connection to the external MOSFETs for these lines helps provide accurate V_{DS} sensing.

There are two different overcurrent modes that can be set through the M_OC pin.

7.3.4.1.1 Current Limit Mode (M_OC = LOW)

In current limit mode the devices uses current limiting instead of device shutdown during an overcurrent event. After the overcurrent event, the MOSFET in which the overcurrent was detected in will shut off until the next PWM cycle. The overcurrent event will be reported through the nOCTW pin. The nOCTW pin will be held low for a maximum 64 µs period (internal timer) or until the next PWM cycle. If another overcurrent event is triggered from another MOSFET, during a previous overcurrent event, the reporting will continue for another 64 µs period (internal timer will restart) or until both PWM signals cycle.

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7.3.4.1.2 OC Latch Shutdown Mode

When an overcurrent event occurs, both the high-side and low-side MOSFETs will be disabled in the corresponding half-bridge. The nFAULT pin will latch until the fault is reset through a quick EN_GATE reset pulse.

7.3.4.2 OC_ADJ

When external MOSFET is turned on, the output current flows through the on resistance, $R_{DS(on)}$ of the MOSFET, which creates a voltage drop V_{DS}. The over current protection event will be enabled when the V_{DS} exceeds a pre-set value. The voltage on OC_ADJ pin will be used to pre-set the OC tripped value. The OC tripped value I_{OC} has to meet following equations:

$$\frac{R2}{(R1 + R2)} \times DVDD = V_{DS} \quad (3)$$

where

- R1 + R2 ≥ 1 KΩ
- DVDD = 3.3 V

$$I_{OC} = \frac{V_{DS}}{R_{DS(on)}} \quad (4)$$

Connect OC_ADJ pin to DVDD to disable the over-current protection feature.

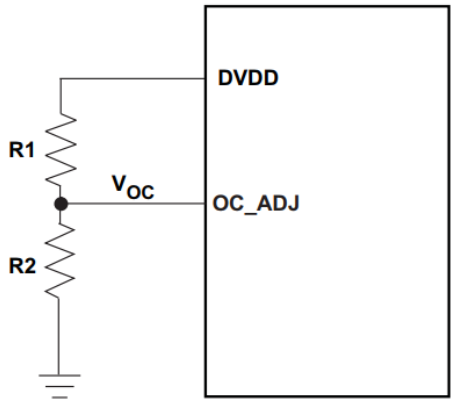


Figure 5. OC_ADJ Current Programming Pin Connection

In current MYXA design

R1 = 10K

R2 = 1.3K

DVDD = 3.3V

Vds = 1.3/(10+1.3) * 3.3 = 0.38

Vds = 0,005 * I,

I trip = 0.38/0,005 = 76A

As power keys MYXA uses state of the art mosfets BSC040N08NS5ATMA1 (MOSFET N-CH 80V 100A 8TDSON) from Infineon Technologies

Brief description

FET Type	N-Channel	
Technology	MOSFET (Metal Oxide)	
Drain to Source Voltage (Vdss)	80V	
Current - Continuous Drain (Id) @ 25°C	100A (Tc)	
Drive Voltage (Max Rds On, Min Rds On)	6V, 10V	
Vgs(th) (Max) @ Id	3.8V @ 67µA	
Gate Charge (Qg) (Max) @ Vgs	54nC @ 10V	
Input Capacitance (Ciss) (Max) @ Vds	3900pF @ 40V	
Vgs (Max)	±20V	
FET Feature	-	
Power Dissipation (Max)	2.5W (Ta), 104W (Tc)	
Rds On (Max) @ Id, Vgs	4 mOhm @ 50A, 10V	
Operating Temperature	-55°C ~ 150°C (TJ)	
Mounting Type	Surface Mount	
Supplier Device Package	PG-TDSON-8	
Package / Case	8-PowerTDFN	

Each mosfet has 4R3 gate resistor to eliminate gate-ringing

Loss estimation at 12S@30A:

Static loss:

P = (I^2 * R) = 0.004 * 30 * 30 = 3,6 W

Dynamic loss:

P = 1/2 * Vin * Iout * (Trise + Tfall) * Fswitch

According to DRV8302 datasheet

6.6 Gate Timing and Protection Characteristics

			MIN	NOM	MAX	UNIT
TIMING, OUTPUT PINS						
$t_{pd,lf-O}$	Positive input falling to GH_x falling	CL=1 nF, 50% to 50%		45		ns
$t_{pd,lr-O}$	Positive input rising to GL_x falling	CL=1 nF, 50% to 50%		45		ns
T_{d_min}	Minimum dead time after hand shaking(1)				50	ns
T_{dtp}	Dead Time	With R_{DTC} set to different values	50		500	ns
t_{GDr}	Rise time, gate drive output	CL=1 nF, 10% to 90%		25		ns
t_{GDF}	Fall time, gate drive output	CL=1 nF, 90% to 10%		25		ns

Trise = Tfall ~ 100 ns

P = 1/2 * 50,4 * 30 * (100 + 100) * 10^-9 * 45 000 ~ 6,8 W

Total loss per switch Ploss_sw ~ 11W

Total loss per phase Ploss_ph ~ 22W

A spreadsheet for calculations above

Also simulation models to find out tRise and tFall times more precisely can be found below. It should be opened with LTSpice

Phase current sensing

Current is sensed on two phases using CSNL2512FT3L00(RES SMD 0.003 OHM 1% 2W 2512) current shunts and current sense amplifiers integrated in DRV8302. Each current shunt has 1000pF capacitor connected across it.

Current shunt amplifier gain can be either 10 or 40x depending on GAIN pin of DRV8302 which is controlled by the MCU.

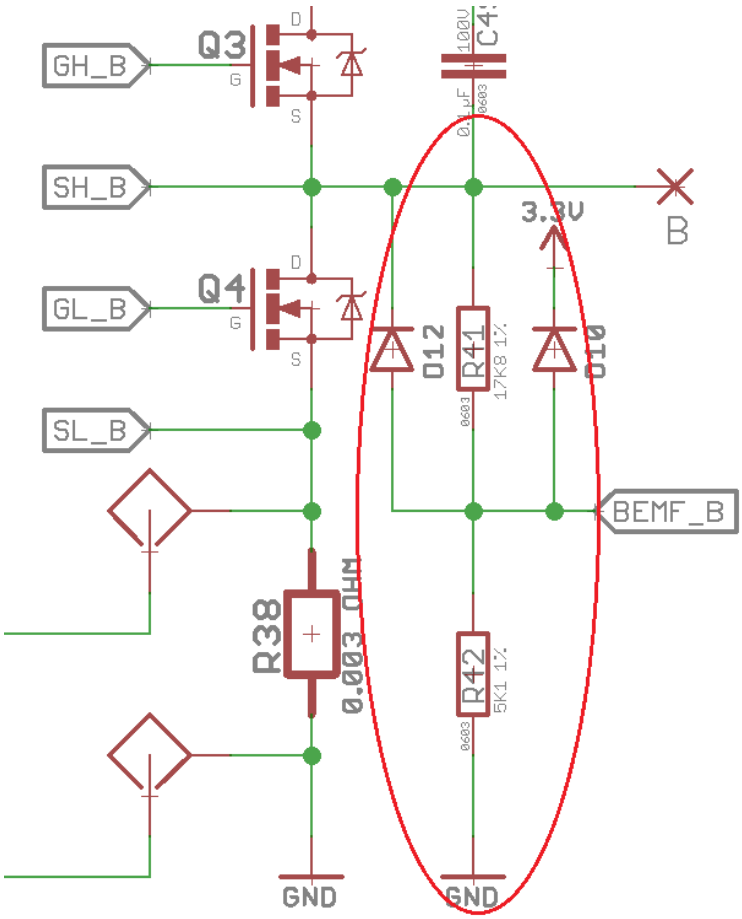
This gives maximum measurable current

I max = 3.3 / (10 * 0.003) = 110A for 10x gain. But max differential voltage of current amplifier is 300mV, so I max = 0,3/0,003 = 100A

I max = 3.3 / (40 * 0.003) = 27.5A for 40x gain

Phase signal sensing

Instead of more conventional analog voltage reading for phase signal MYXA uses different approach. It monitors signal transition from 0 to 1 on MCU pin, where phase signal is connected to. For that purpose resistor divider for each phase signal is implemented. One of them can be seen below:



In order for phase event to be detected BEMF_B voltage must exceed 0.7 * Vdd = 0.7 * 3.3 = 2,31V(according to table below)

Table 56. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	FT, FTf, TTa and NRST I/O input low level voltage	1.7 V≤V_{DD}≤3.6 V	-	-	$0.35V_{DD}$–$0.04^{(1)}$ / $0.3V_{DD}^{(2)}$	V
	BOOT0 I/O input low level voltage	1.75 V ≤ V_{DD} ≤ 3.6 V, – 40 °C≤ T_A ≤ 105 °C	-	-	$0.1V_{DD}+0.1^{(1)}$	
		1.7 V ≤ V_{DD} ≤ 3.6 V, 0 °C ≤ T_A ≤105 °C	-	-		
V_{IH}	FT, FTf, TTa and NRST I/O input high level voltage[4]	1.7 V≤V_{DD}≤3.6 V	$0.45V_{DD}+0.3^{(1)}$ / $0.7V_{DD}^{(2)}$	-	-	V
	BOOT0 I/O input high level voltage	1.75 V≤V_{DD} ≤3.6 V, – 40 °C≤T_A ≤105 °C	$0.17V_{DD}+0.7^{(1)}$	-	-	
		1.7 V≤V_{DD} ≤3.6 V, 0 °C≤T_A ≤105 °C				
V_{HYS}	FT, FTf, TTa and NRST I/O input hysteresis	1.7 V≤V_{DD}≤3.6 V	-	$10\%V_{DD}$	-	V
	BOOT0 I/O input hysteresis	1.75 V≤V_{DD} ≤3.6 V, –40 °C≤T_A ≤105 °C	-	100m	-	
		1.7 V≤V_{DD} ≤3.6 V, 0 °C≤T_A ≤105 °C	-		-	
I_{lkg}	I/O input leakage current [3]	V_{SS} ≤V_{IN} ≤V_{DD}	-	-	±1	µA
	I/O FT input leakage current [4]	V_{IN} = 5 V	-	-	3	

So, with resistor divider of 17K8 and 5K1 this will happen when phase B voltage will be

3,3 * 0,7 / (5,1/17,8 + 5,1) ~ 10,3 V

Input capacitor battery

Main input capacitor is 820uF 80V aluminum cap, which is placed as near to power mosfets as possible. Also at least two low-esr 4.7UF 100V ca ps are added per phase.

UAVCAN

MYXA has two UAVCAN interfaces. MYXA can provide UAVCAN with 5V power source through controllable Current Switch Regulator TPD3S014 DBVR, which can also act as e-fuse limiting UAVCAN current to 500mA

Both UAVCAN interfaces use TJA1051TK/3,118 (IC TXRX CAN HIGH SPEED 8HVSON) driver chips, which are supplied with 5V line and IO line is connected to 3.3V.

USB

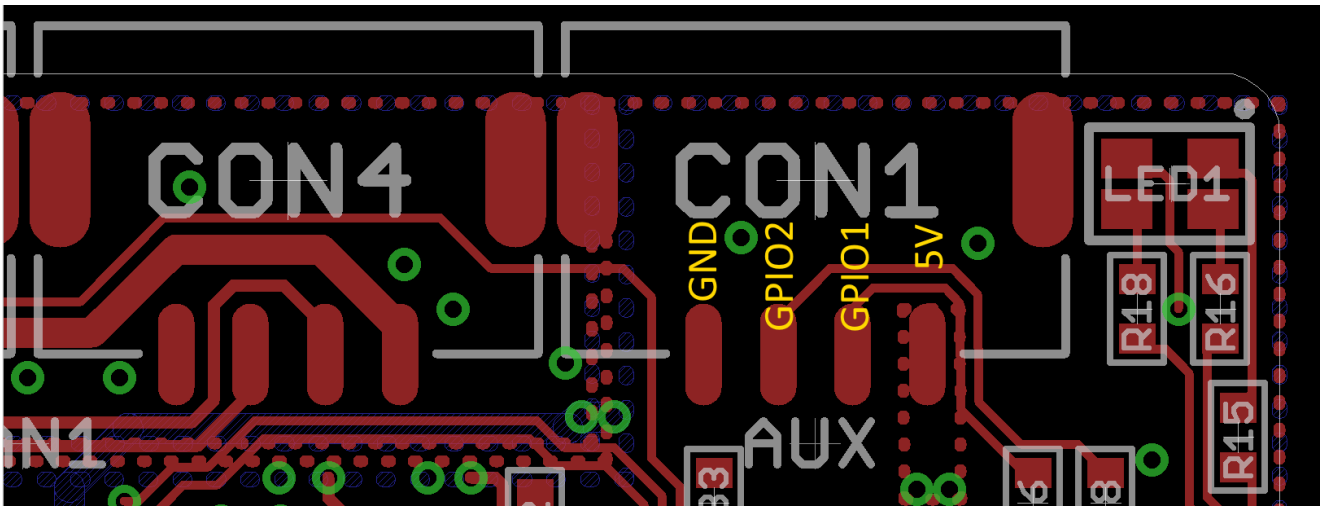
USB consists of only one microUSB connector and miniature USB-specific TVS-diode array

MYXA can be powered via USB(obviously without powerstage), as USB Vdd is connected to 5V line with CRS08 Shottky diode

There are also footprints for serial resistors for D+ and D- lines in case some more protection needed. As for now they are replaced with 0 ohm resistors.

AUX input

MYXA has two AUX inputs which are routed to UAVCAN-like 4-pin connector. This connector can provide 5V power to external circuitry as well. 5V AUX line current consumption is limited with resettable fuse (PTC RESTTBLE 0.50A 16V CHIP 1210) and one of UAVCAN Current Switch Regulators.



Both AUX inputs are protected with diode half-bridge

GPIO2 is routed directly to the output connector and can be found on pin PA4(ADC3_IN4) of MCU.

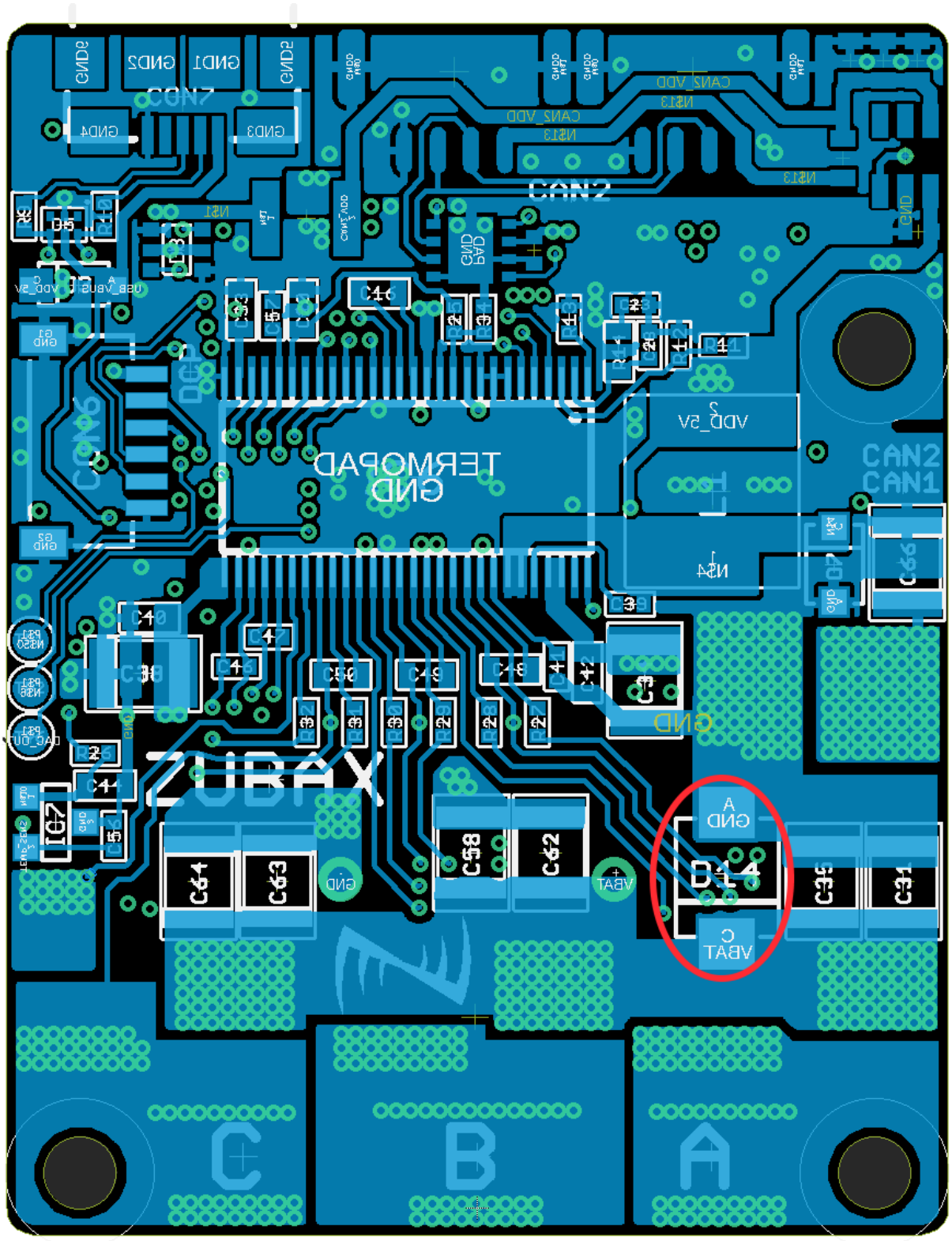
GPIO1 is routed to PA3(ADC3_IN3) pin of MCU and also to PB14 pin(where TIM12_CH1 can be found). It is also connected to PC4 with 1K series resistor, so it can be used to connect NTC or PTC thermistor with typical resistance of about 1K(like this one). The thermistor should be connected between GND and GPIO1 pins of the AUX connector. Then PC5 should activate PULL-UP to 3.3V and form a resistor divider with 1K resistor(between 3.3v and measured voltage) and thermistor(between measured voltage and gnd) and GPIO1(ADC3_IN3) may be measured.

Also digital 1wire thermometers(like ds18b20) may be used on GPIO1 using PWM generation on TIM12_CH1 and DMA to guarantee proper 1-wire timings. This may come handy in extremely noisy environments when analog readings on long thermistor wires are corrupted

TVS diode

Although by default Myxa is shipped without TVS diode installed, there may be some situations that require it installed. In that case user can install it by himself on the provided footprint. The best choice is SMBJ54A from Littlefuse although any other TVS diode in DO214AA package and with breakdown voltage no more than 60V will fit.

The footprint for the diode is shown on the picture below


CAN2
CAN1
TERMOPAD
GND
VDD_5V
VBAT
A
B
C