1/9” VGA CMOS Image Sensor

GC0339

DataSheet

V1.0

2011-11-30

GalaxyCore Inc.

Content

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1. Sensor Overview

1.1 General Description

The GC0339 features 640V x 480H resolution with 1/9-inch optical format, and 4-transistor pixel structure for high image quality and low noise variations. It delivers superior image quality by powerful on-chip design of a 10-bit ADC

The full scale integration of high-performance and low-power functions makes the GC0339 best fit the design, reduce implementation process, and extend the battery life of cell phones, PDAs, and a wide variety of mobile applications.

It provides RAW10 and RAW8 data formats with MIPI interface. It has a commonly used two-wire serial interface for host to control the operation of the whole sensor.

1.2 Features

- Standard optical format of 1/9 inch
- output formats: Single lane MIPI(CSI-2 V1.0/PHY-1.0)
- Date formats: RAW8/RAW10
- power supply requirement : IOVDD： 1.7~3.0V
  AVDD28： 2.7~3.0V
  MVDD18： 1.7~1.9V
- PLL support
- Windowing support
- Horizontal /Vertical mirror
- Package: CSP / Wafer

1.3 Application

- Cellular Phone Cameras
- Notebook and desktop PC cameras
- PDAs
- Toys
- Digital still cameras and camcorders
- Video telephony and conferencing equipment
- Security systems
- Industrial and environmental systems
- Bar code reader

1.4 Technical Specifications

Parameter	Typical value
Optical Format	1/9 inch
Pixel Size	2.5μm x 2.5μm
Active pixel array	648 x 496
ADC resolution	10 bit ADC
Max Frame rate	30fps@24Mhz,VGA
Power Supply	IOVDD: 1.7 ~ 3.0V AVDD28: 2.7 ~ 3.0V MVDD18: 1.7~1.9V
Power Consumption	70mW @ 30fps VGA 10uA @ standby
SNR	TBD
Dark Current	TBD
Sensitivity	TBD
Operating temperature:	-20~70℃
Stable Image temperature	0~50℃
Optimal lens chief ray angle(CRA)	27º(linear)
Package type	CSP/Wafer

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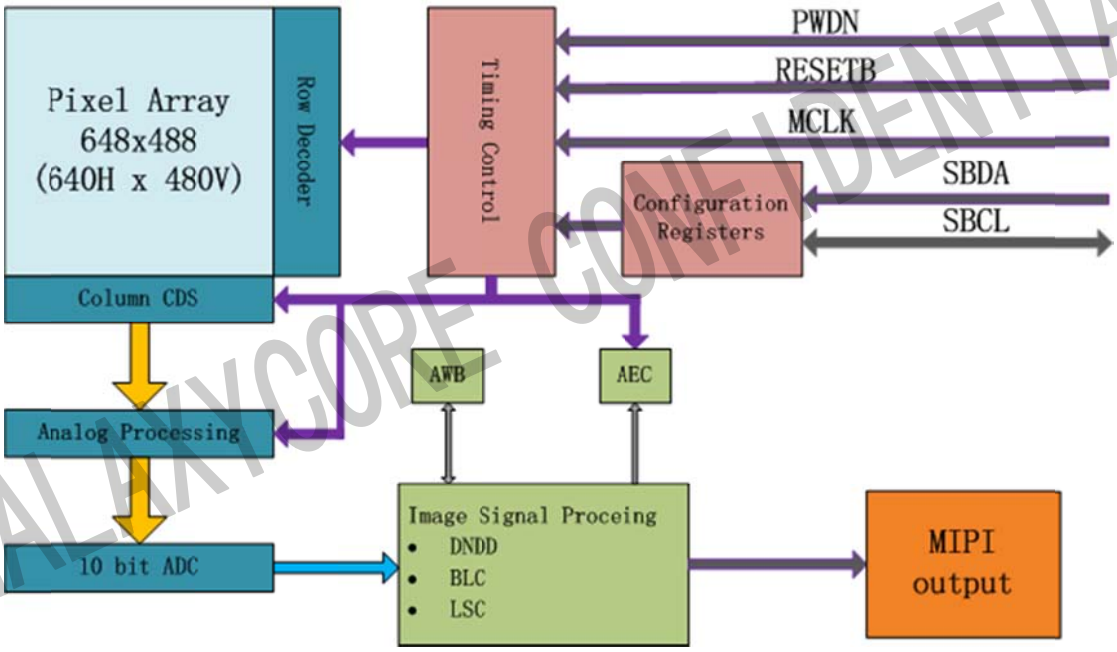
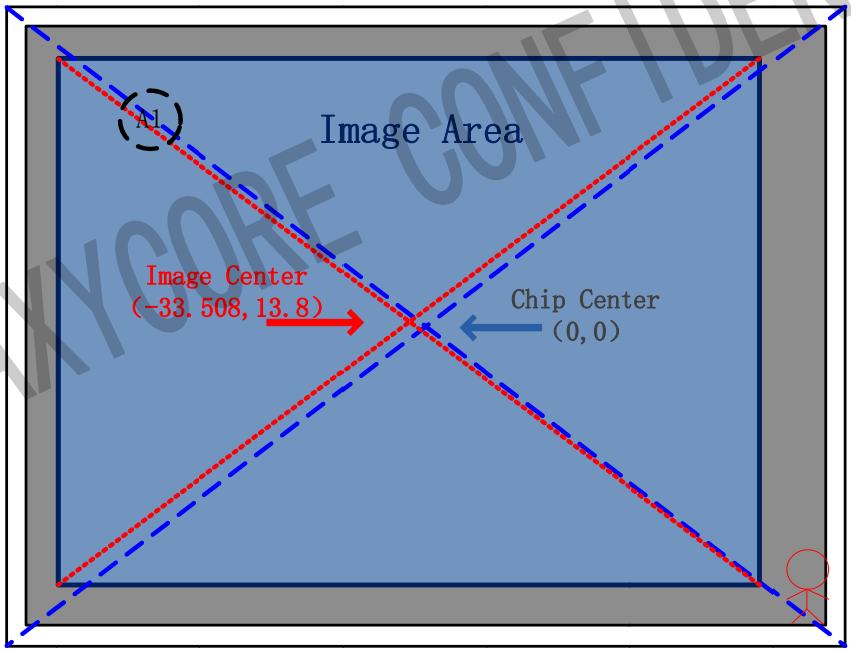
1.5 Block Diagram



GC0339 has an active image array of 648x488 pixels. The active pixels are read out progressively through column/row driver circuits. In order to reduce fixed pattern noise, CDS circuits are adopted. The analog signal is transferred to digital signal by 10 bit A/D converter. The digital signals are processed in the ISP Block, including Bayer filter, denoise and so on. Users can easily control these functions via two-wire serial interface bus.

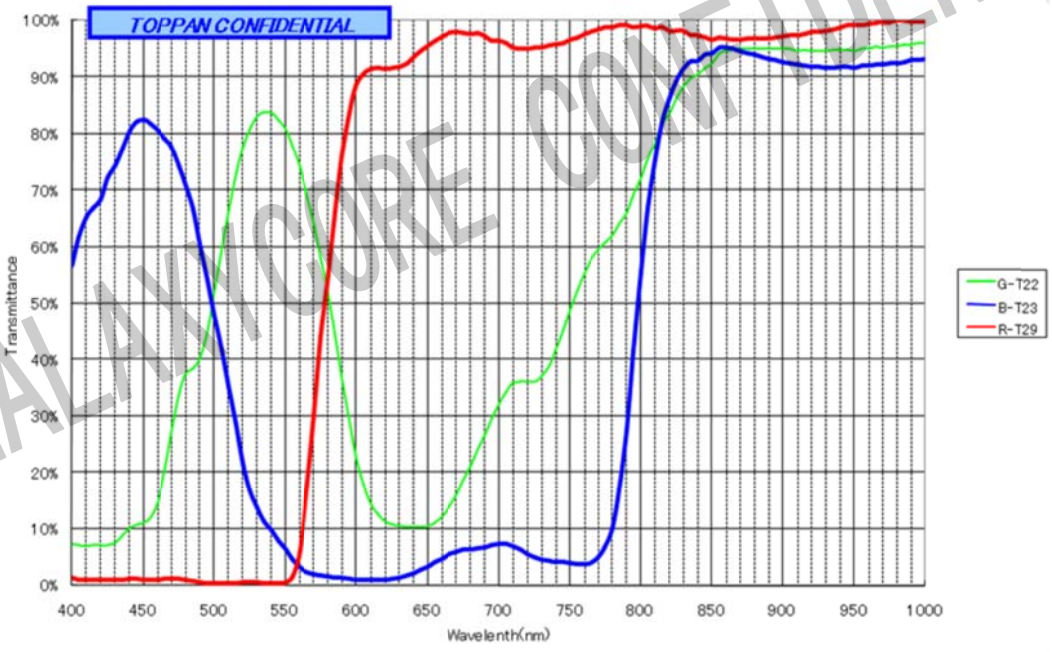
2. Optical Specifications

2.1 Sensor Array Center



2.2 Color Filter Spectral Characteristics

The optical spectrum of color filters is shown below:

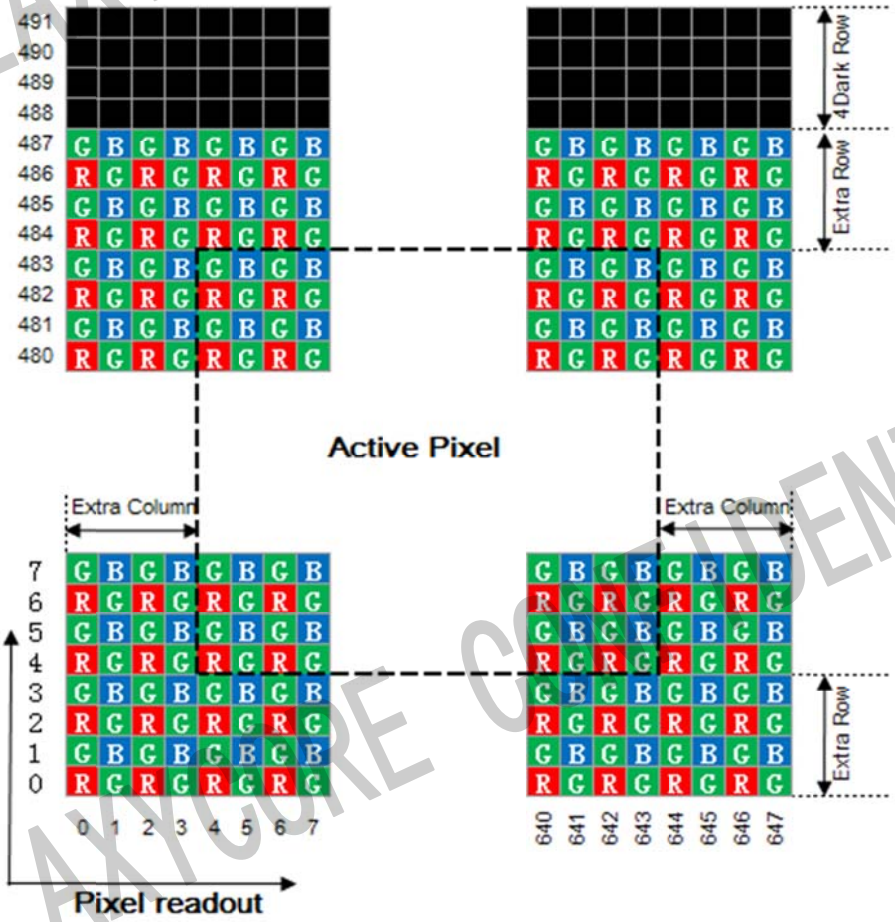


2.3 Pixel Array Structure

Pixel array is covered by Bayer pattern color filters. The primary color BG/GR array is arranged in line-alternating way.

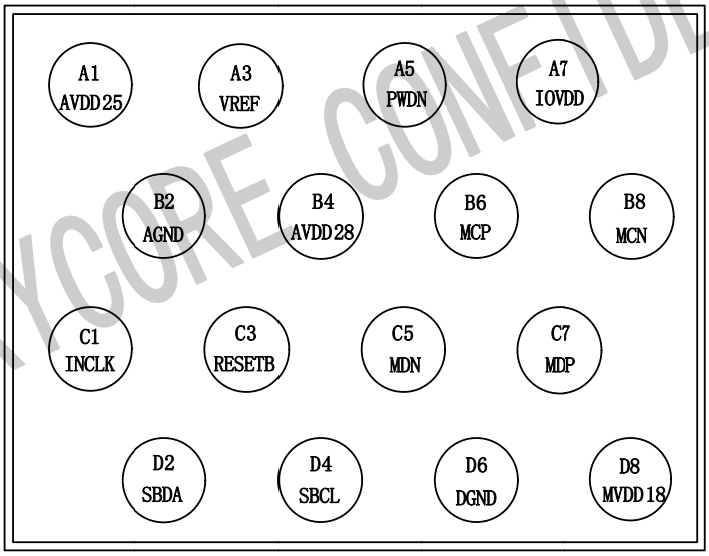
If no flip in column, column is read out from 0 to 647. If flip in column, column is read out from 647 to 0.

If no flip in row, row is read out from 0 to 487. If flip in row, row is read out from 487 to 0.



3. Pin Description

3.1 GC0339 Pin Diagram



Pin diagram (Top View)

3.2 GC0339 Signal description

Pin	Name	Pin Type	Description
A1	AVDD25	Power	internal analog reference,
A3	VREF	Power	internal analog reference
A5	PWDN	Input	power down (active high)
A7	IOVDD	Power	Power Supply for I/O circuits, 1.7~3.0V
B2	AGND	Ground	Ground for Analog
B4	AVDD28	Power	Power for analog circuit/sensor array, 2.7~3.0V
B6	MCP	Output	MIPI clock (+)
B8	MCN	Output	MIPI clock (-)
C1	INCLK	Input	sensor input clock
C3	RESETB	Input	reset (active low)
C5	MDN	Output	MIPI data (-)
C7	MDP	Output	MIPI data (+)
D2	SBDA	I/O	SCCB data
D4	SBCL	Input	SCCB input clock

D6	DGND	Ground	Ground for digital
D8	MVDD18	Power	Power Supplier pin for MIPI Driver，1.7~1.9V

4. Two-wire Serial Bus Communication

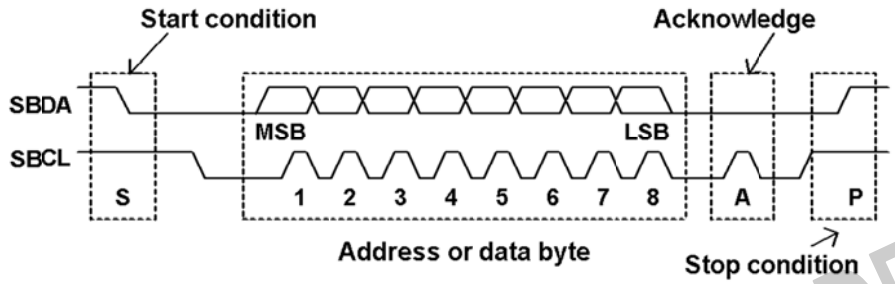
GC0339 Device Address:

serial bus write address = **0x42,** serial bus read address = **0x43**

4.1 Protocol

The host must perform the role of a communications master and GC0339 acts as either a slave receiver or transmitter. The master must do

- Generate the **Start(S)/Stop(P)** condition
- Provide the serial clock on **SBCL**.



Single Register Writing：

S	42H	A	Register Address	A	Data	A	P

Incremental Register Writing:

S	42H	A	Register Address	A	Data(1)	A	……	Data(N)	A	P

Single Register Reading:

S	42H	A	Register Address	A	S	43H	A	Data	A	P

Incremental Register Reading:

S	42H	A	Register Address	A	S	43H	A	Data(1)	A	……	Data(N)	NA	P

Notes:

From master to slave　　From slave to master

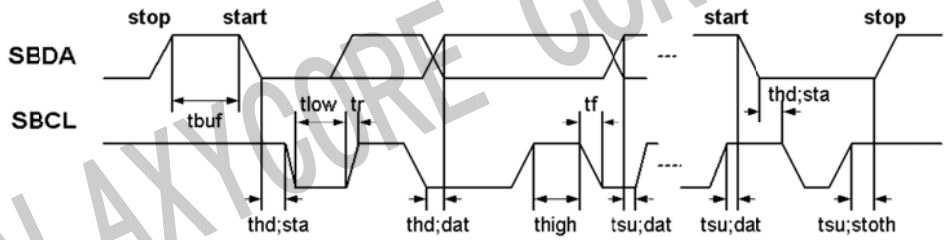
S: Start condition　　**P:** Stop condition

A: Acknowledge bit　　**NA:** No acknowledge

Register Address: Sensor register address

Data: Sensor register value

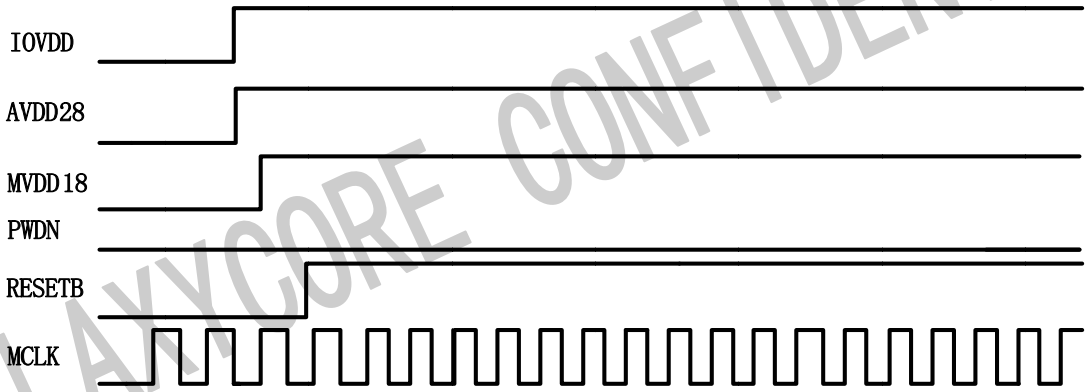
4.2 Serial Bus Timing



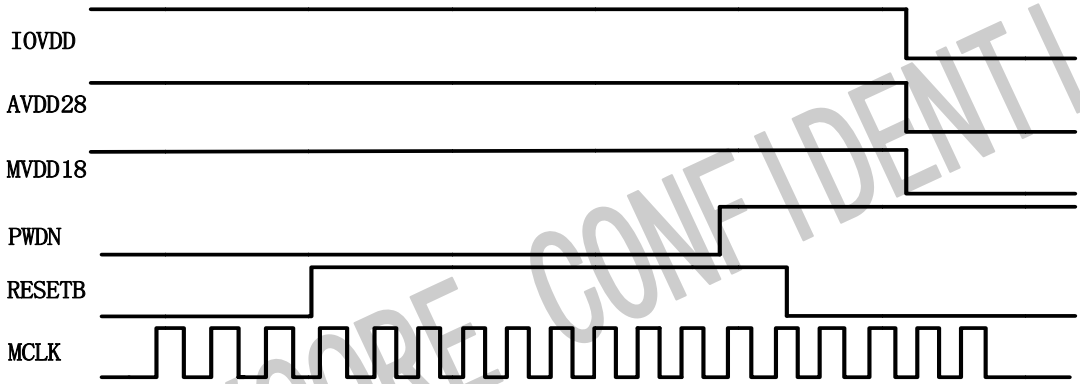
Parameter	Symbol	Min.	Max.	Unit
SBCL clock frequency	fscl	0	400	KHz
Bus free time between a stop and a start	tbuf	1.2	*	μs
Hold time for a repeated start	thd;sta	1.0	*	μs
LOW period of SBCL	tlow	1.2	*	μs
HIGH period of SBCL	thigh	1.0	*	μs
Set-up time for a repeated start	tsu;sta	1.2	*	ns
Data hold time	thd;dat	1.3	*	ns
Data Set-up time	tsu;dat	250	*	ns
Rise time of SBCL, SBDA	tr	*	250	ns
Fall time of SBCL, SBDA	tf	*	300	ns
Set-up time for a stop	tsu;sto	1.2	*	μs
Capacitive load of bus line (SBCL, SBDA)	Cb	*	*	pf

5. Power off/on sequence

5.1 Power on sequence

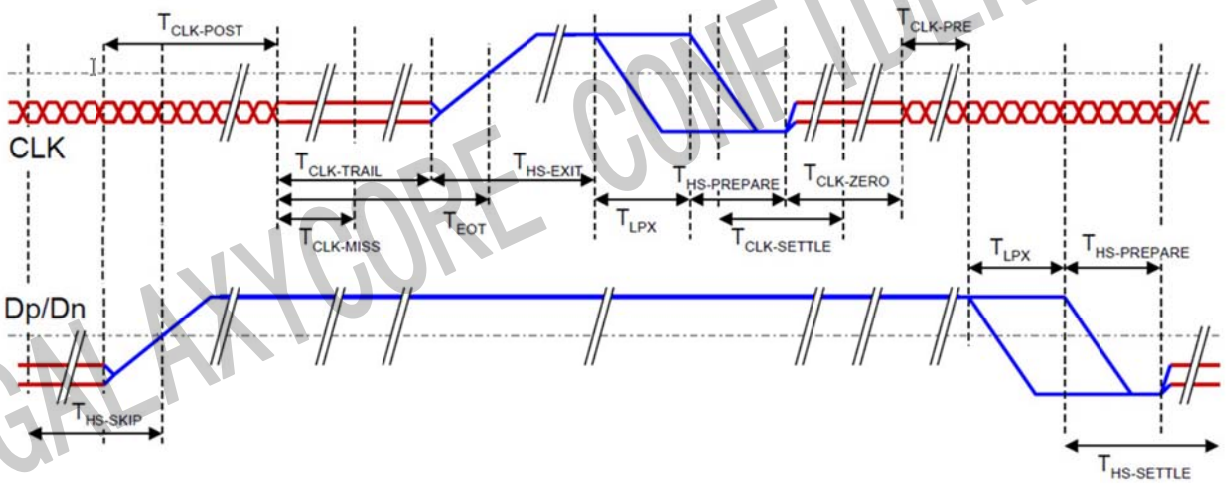


5.2 Power off sequence



6. Timing

6.1 Clock lane low-power



Notice:

- Clock must be reliable during high speed transmission and mode-switching
- Clock can go to LP only if data lanes are in LP(and nothing relies on it),
- In Low –Power data lanes are conceptually asynchronous(independent of the high speed clock)

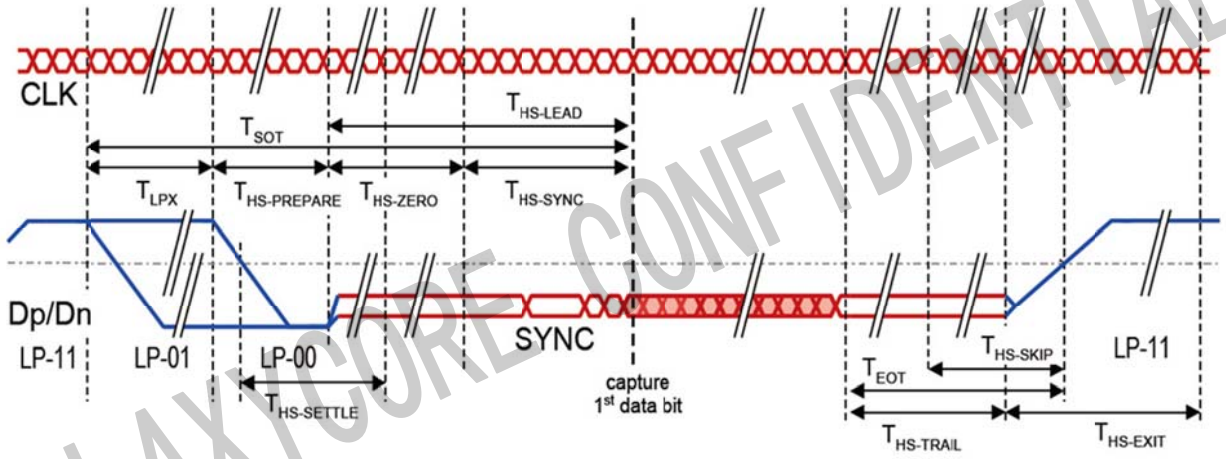
  T_{CLK_PRE}: setting by Register 0x74

  T_{CLK_POST} : setting by Register 0x75

  $T_{CLK\text{-}ZERO}$: setting by Register 0x73

  T_{CLK_TRAIL}: setting by Register 0x76

6.2 Data Burst



Notice:

- Clock Keeps running and samples data lanes(except for lanes in LPS)
- Unambiguous leader and trailer sequences required to distill real dits,
- trailer is removed inside PHY(a few bytes)
- Time-out to ignore line values during line state transition

T_{LPX} : setting by Register 0x71

$T_{HS\text{-}PREPARE}$: setting by Register 0x79

$T_{HS\text{-}ZERO}$: setting by Register 0x7a

$T_{HS\text{-}TRAIL}$: setting by Register 0x7b

$T_{HS\text{-}EXIT}$: setting by Register 0x77

7. Electrical Specification

7.1 DC Characteristics

Parameter	Description	Min	Type	Max	Unit
AVDD28	Power supply	2.7	2.8	3.0	V
IOVDD	Power supply	1.7	2.8	3.0	V
MVDD18	Power supply	1.7	1.8	1.9	V
I_{DD}	Active(Operating) Current	--	25	--	mA
$I_{DDS-PWDN}$	Standby Current	--	10	--	uA

7.2 D-PHY Electrical Specification

7.2.1 HS Transmitter DC specifications

Parameter	Description	Min	Type	Max	Unit
VCMTX	HS transmit static common-mode voltage	150	200	250	mV
|ΔVCMTX(1,0)|	VCMTX mismatch when output is Differential-1 or Differential-0			5	mV
|VOD|	HS transmit differential voltage	140	200	270	mV
|ΔVOD|	VOD mismatch when output is Differential-1 or Differential-0			10	mV
|ΔVOD|	HS output high voltage			360	mV
ZOS	Single ended output impedance	40	50	62.5	Ω
ΔZOS	Single ended output impedance mismatch			10	%

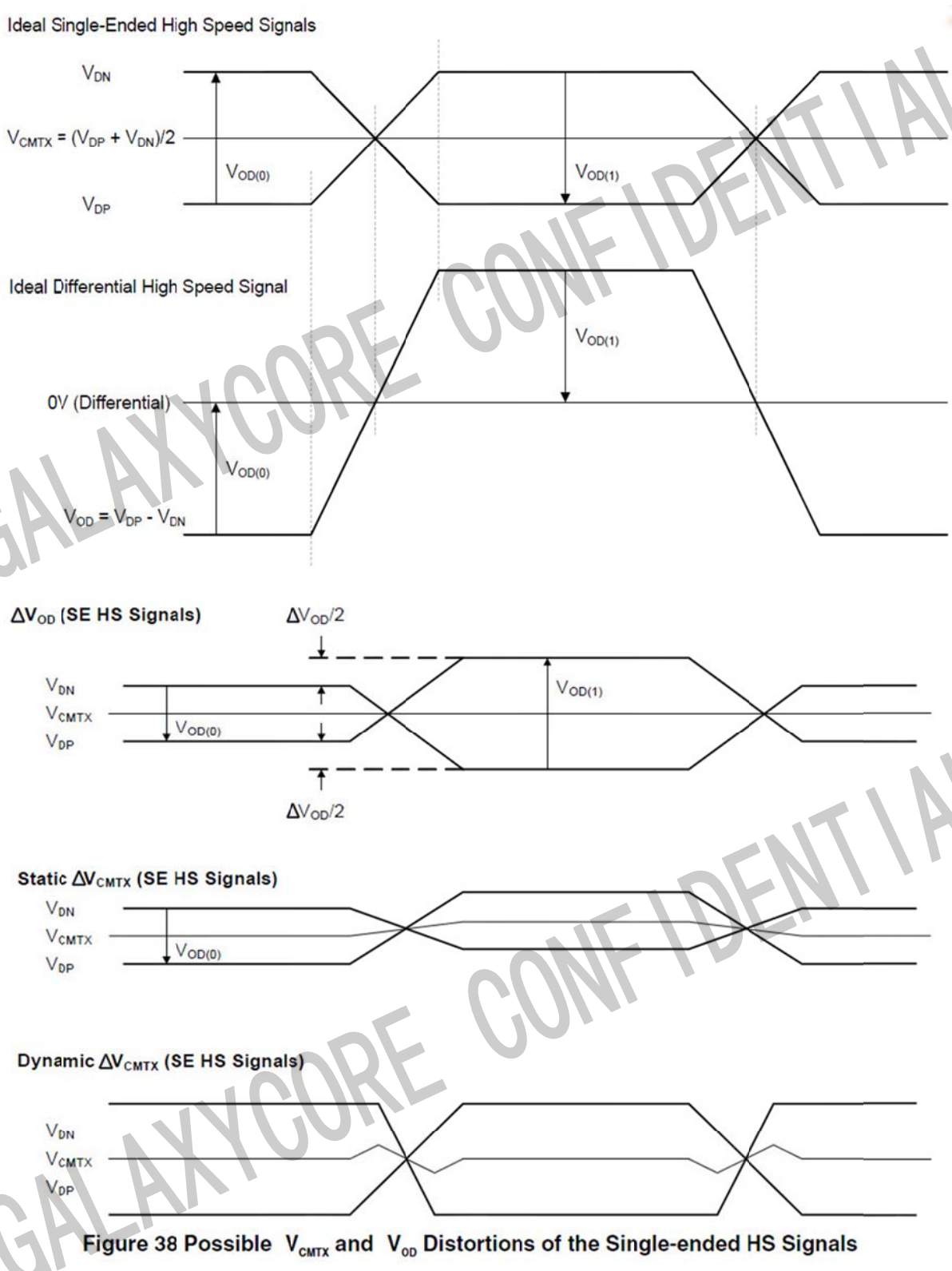


Figure 38 Possible V_{CMTX} and V_{OD} Distortions of the Single-ended HS Signals

HS Transmitter AC Specifications

Parameter	Description	Min	Type	Max	Unit
ΔVCMTX(HF)	Common-level variations above 450MHz	150	200	250	mVRMS
ΔVCMTX(LF)	Common-level variation between 50-450MHz			5	mVRMS
tR and tF	20%-80% rise time and fall time			0.3	UI
		150			ps

7.2.2 LP Transmitter DC specifications

Parameter	Description	Min	Type	Max	Unit
V_{OH}	Thevenin output high level	1.1	1.2	1.3	mV
V_{OL}	Thevenin output low level	-50		50	mV
Z_{OLP}	Output impedance of LP transmitter	110			Ω

8. Register List

SYS_REG

Addr	Name	Width	Default Value	R/W	Description
0xf6	PLL_mode	3	0x00	RW	[7:3] NA [2] Pll mode 0: CLK x32 1: CLK x16 [1] div2en 1: MCLK/2 0: MCLK [0] analog pll enable
0xf7	Digital_clock_mode	3	0x00	RW	[7:3] NA [2] pll clk mode serial clk is half of pll_clk 0: half 1: pll clk [1] pll_enable [0] use pll_clk or MCLK 0: use mclk

					1: use pll_clock
0xf8	Pad_updn	5	0x00	RW	[7:5] NA [4] pwd_dnb 0 pull down 1 not pull [3:0] Reserved
0xf9	Reserved				
0xfa	isp_div_mode	8	0x00	RW	[7:4] +1 represent the frequency division number [3:0] represent the high level in one pulse after frequency division Mclk by Div duty 0x11 2 1:1 0x21 3 1:2 0x22 3 2:1 0x31 4 1:3 0x32 4 2:2 0x33 4 3:1 …
0xfb	I2C_device_ID	7	0x42	RW	[7:1] I2C device ID, can write once [0] NA
0xfc	Analog_pwc	5	0x03	RW	[7:5] NA [4] digital_clock_enable [3] NA [2] da25_en [1] da18_en [0] apwd
0xfe	Reset related	8	0x00	RW	[7] soft_reset [6] mipi_rst [5] Reserved [4] CISCTL_restart_n [3:0] NA

Analog Register

Addr	Name	Width	Default Value	R/W	Description
0x00	Chip_ID	8	0xc8	RO	Chip ID
0x01	HB[7:0]	8	0x1a	RW	Horizontal blanking low 8 bit, unit pixel clock
0x02	VB[7:0]	8	0x2f	RW	Vertical blanking low 8 bit, if current exposure < (VB + window Height), frame rate will be (VB + window

					Height); otherwise frame rate will be determined by exposure
0x03	Exposure[11:8]	4	0x00	RW	[7:4] NA [3:0] exposure[11:8], use line processing time as the unit.
0x04	Exposure[7:0]	8	0x96	RW	Exposure[7:0], controlled by AEC if AEC is in function
0x05	Row_start[8]	1	0x00	RW	Defines the starting row of the pixel array
0x06	Row_start[7:0]	8	0x00		
0x07	Column start[9:8]	2	0x00	RW	Defines the starting column of the pixel array
0x08	Column start[7:0]	8	0x00		
0x09	Window height[8]	1	0x01	RW	[7:1] NA [0] Window height high bit
0x0a	Window height[7:0]	8	0xe8	RW	Window height low 8 bits
0x0b	Window width[9:8]	2	0x02	RW	[7:2] NA [1:0] Window width high bits
0x0c	Window width[7:0]	8	0x88	RW	Window width low 8 bits
0x0d	Vs_st	8	0x02	RW	number of Row time from frame start to first HSYNC valid
0x0e	Vs_et	8	0x04	RW	number of Row time from last HSYNC valid to frame end Notice the relation with VB, VB > Vs_st+Vs_et
0x0f	Vb[11:8] Hb[11:8]	8	0x05	RW	[7:4] Vertical blanking high bit [3:0] Horizontal blanking high bit
0x10	Rsh_width	8	0x22	RW	[7:4] restg_width, X2 [3:0] sh_width, X2
0x11	Tsp_width	8	0x0d	RW	[7:2] tx_width [1:0] space width, X2
0x12	Sh_delay	8	0x2a	RW	sh_delay
0x13	Row_tail_width	4	0x00	RW	[3:0] row_tail_width
0x14	CISCTL_mode1	8	0X00	RW	[7] HSYNC always [6] NA [5:4] CFA sequence [3:2] NA [1] Updown [0] mirror
0x15	CISCTL_mode2	8	0x0a	RW	[7:6] output_mode 00: VGA 01: evenskip 10: CIF 11: rowbin

					[5:2] Reserved [1:0] exposure mode [1] new exposure/normal badframe [0] badframe enable
0x16	CISCTL_mode3	8	0x05	RW	Reserved
0x17	CISCTL_mode4	8	0x05	RW	Reserved
0x18	CISCTL_mode5	8	0x00	RW	[7] double_reset_mode [6] double_reset_tx_mode [5]double_reset_only_tx [4] double_reset_skip_sh [3] shr_mode [2] shs_mode [1] shr_b_mode [0] shs_b_mode
0x1a	Analog_mode 1	8	0x21	RW	[7:1] Reserved [0] clk_delay
0x1b	Analog_mode 2	8	0x88	RW	Reserved
0x1c	Analog_mode 3	8	0xb1	RW	Reserved
0x1d	Analog_mode 4	8	0xba	RW	Reserved
0x1e	Analog_mode 5	8	0x11	RW	Reserved
0x1f	Reserved				

BLK

Addr	Name	Width	Default Value	R/W	Description
0x30	Blk_mode	8	0x27	RW	[7] dark_current_mode 1: use exp_rated_darkc 0: use ndark_row calculated [6:4] BLK_smooth_speed [3:2] BLK_row_select_mode [1] dark_current_en [0] offset_en
0x31	BLK_limit_value	7	0x40	RW	[7] NA [6:0]When Dark data big than it, while get this to replace it for protect dark data. low align 11bits
0x32	global_offset	7	0x00	RW	[7] NA [6:0]low align 11bits
0x33	current_R_offset	7		RO	[7] NA [6:0] Current_R_offset

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0x34	current_G_offset	7		RO	[7] NA [6:0] Current_G_offset
0x35	current_B_offset	7		RO	[7] NA [6:0] Current_B_offset
0x36	current_R_dark_current	7		RO	[7] NA [6:0] Current_R_dark_current
0x37	Current_G_dark_current	7		RO	[7] NA [6:0] Current_G_dark_current
0x38	current_B_dark_current	7		RO	[7] NA [6:0] Current_B_dark_current
0x39	Exp_rate_darkc	8	0x04	RW	Low 8 bits of 0.12, 4 means when exp =1024, dark current portion is 4
0x3a	offset_submode offset_ratio	8	0x20	RW	[7:6] offset submode [5:0] offset ratio of G1 channel, 1.5 bits
0x3b	darkc_submode dark_current_ratio	8	0x10	RW	[7:6] darkc submode [5:0] dark current ratio of G1 channel, 1.5 bits
0x3c	manual_G1_offset	6	0x00	RW	[7:6] NA [5:0]S5, aligned to lower 8 of 11 bits data
0x3d	manual_R1_offset	6	0x00	RW	[7:6] NA [5:0] S5, aligned to lower 8 of 11 bits data
0x3e	manual_B2_offset	6	0x00	RW	[7:6] NA [5:0] S5, aligned to lower 8 of 11 bits data
0x3f	manual_G2_offset	6	0x00	RW	[7:6] NA [5:0] S5, aligned to lower 8 of 11 bits data

ISP Related

Addr	Name	Width	Default Value	R/W	Description
0x20	Block_enable1	8	0x00	RW	[7] normal_data_out [6] dark_out_valid [5] DN_en [4] DD_en [3] NA [2] NA [1] AWB_en [0] LSC_en

0x21	AWB_update_mode AEC_update_mode	2	0x00	RW	[7:2] NA [1] when use external I2C control can be set 1 [0] when use external I2C control can be set 1 AEC_update_mode 1
0x22	AEC_exp_update	1	0x00	RW	[7:1] NA [0] value 1 to let buf_exp and buf_gain to valid when new frame
0x23	Awb_protect Awb_gain_update	8	0x00	RW	[7] AWB_protect awb gain from buf gain when Awb_protect is 1 [6:1] NA [0] value 1 to let buf_gain to valid when AWB_update_mode valid and AWB_protect valid
0x2a	Clock_gating	8	0x84	RW	[7] ISP_quiet_mode [6:3] NA [2] DIVMUX_clkg_en [1:0] NA
0x2b	DNDD_test_data[7:0]	8	0x00	RW	DNDD_test_data
0x2c	DNAA_test_data[9:8]	2	0x00	RW	DNDD_test_data
0x2d	Debug_mode1	8	0x08	RW	[7:4] NA [3:2] pipe_gate_mode, **4** type check in CTL [1:0] bff_gate_mode
0x2e	Debug_mode2	8	0x10	RW	[7:6] NA [5] INBF_EN [4] update_gain_mode [3:2] NA [1] LSC_test_image [0] DNDD_out_test_image

Gain

Addr	Name	Width	Default Value	R/W	Description
0x4a	AWB_R_gain	8	0x50	RO	2.6 bits, red channel gain from auto white balancing
0x4b	AWB_G_gain	8	0x40	RO	2.6 bits, green channel gain from auto white balancing
0x4c	AWB_B_gain	8	0x48	RO	2.6 bits, blue channel gain from auto

					white balancing
0x4d	Analog_Debug1	8	0x00	RW	
0x50	Global_gain	8	0x40	RW	2.6bits, Global gain
0x51	Auto_pregain	8	0x40	RO	Controlled by AEC, can be manually controlled when disable AEC
0x53	Channel_gain_G1	8	0x80	RW	1.7 bits, G1 channel pre gain
0x54	Channel_gain_R	8	0x80	RW	1.7 bits, R channel pre gain
0x55	Channel_gain_B	8	0x80	RW	1.7 bits, B channel pre gain
0x56	Channel_gain_G2	8	0x80	RW	1.7 bits, G2 channel pre gain

CSI2/DPHY

Addr	Name	Width	Default Value	R/W	Description
0x60	CSI2_mode	8	0x00	RW	[7] lane enable [6] NA [5] ULP mode [4] MIPI enable [3] RAW10switch mode [2] RAW data 1: Raw 8bit 0: Raw 10bit [1] line_sync_mode [0] NA
0x61	LDI_set	8	0x2b	RW	Long packet DI set
0x62	LWC_set[7:0]	8	0x20	RW	Long packet WC set
0x63	LWC_Set[15:8]	8	0x03	RW	
0x64	SYNC_set	8	0xb8	RW	Data start SYNC code
0x65	DPHY_mode	8	0x00	RW	[7] NA [6] NA [5] when half of fifo full start DPHY transfer [4] when fifo prog full will start DPHY transfer [3:1] NA [0] clklane_mode 0: every frame stop clklane mode 1: clock lane sync with data lane
0x66	LP_set	8	0x09	RW	[7:6] analog LP hi-z set [5:4] NA [3:2] analog LP one set

					[1:0] analog LP zero set
0x67	MIPI_wdiv_set MIPI_rdiv_set	8	0x10	RW	[7:4] default 1/2, soc_pclk with mclk ratio [3:0] when mclk to hclk is 1:4, it should be 1, default is 0 for 1:8 ratio
0x68	DPHY_switch_msb_mode	3	0x00	RW	[2] NA [1] data_lane [0] clk_lane
0x69	DPHY_analog_mode1	8	0x00	RW	[6] NA [5] CTD_lane [4] CTD_clk（match resistance） [2] NA [1] phy-lane enable [0] phy_clk_en
0x6a	DPHY_analog_mode2	8	0x00	RW	[6:4] lane_driver [2:0] clk_driver
0x6b	DPHY_analog_mode3	8	0x10	RW	[5] lane_delay [4] clk_delay [2:0] NA
0x6c	Fifo_prog_full_level[7:0]	8	0x90	RW	Fifo_prog_full set
0x6d	Fifo_mode Fifo_prog_full_level[8]	5	0x01	RW	[7] fifo reset_mode [6] NA [5] store_switch [4] read_switch [3:1] NA [0] Fifo_prog_full_set
0x70	T_init_set	8	0x80	RW	Timing of initial setting
0x71	T_LPX_set	8	0x10	RW	Timing of LP setting
0x72	T_CLK_HS_PREPARE_set	8	0x05	RW	Timing of COCLK HS PREPARE setting
0x73	T_CLK_zero_set	8	0x30	RW	Timing of COCLK HS zero setting
0x74	T_CLK_PRE_set	8	0x02	RW	Timing of COCLK HS PRE of Data setting
0x75	T_CLK_POST_set	8	0x10	RW	Timing of COCLK HS Post of Data setting
0x76	T_CLK_TRAIL_set	8	0x08	RW	Timing of COCLK tail setting
0x77	T_HS_exit_set	8	0x10	RW	Timing of HS exit setting
0x78	T_wakeup_set	8	0xa0	RW	Timing of wakeup setting
0x79	T_HS_PREPARE_set	8	0x06	RW	Timing of data HS PREPARE setting
0x7a	T_HS_zero_set	8	0x0a	RW	Timing of data HS zero setting

0x7b	T_HS_TRAIL_set	8	0x08	RW	Timing of data HS trail setting

LSC(Lens shading correct)

Addr	Name	Width	Default Value	R/W	Description
0x80	LSC red b2	8	0x40	RW	Square coefficient for R channel
0x81	LSC green b2	8	0x40	RW	Square coefficient for G channel
0x82	LSC blue b2	8	0x40	RW	Square coefficient for B channel
0x83	LSC red b4	8	0x30	RW	Quadra coefficient for R channel
0x84	LSC green b4	8	0x30	RW	Quadra coefficient for G channel
0x85	LSC blue b4	8	0x30	RW	Quadra coefficient for B channel
0x86	LSC_signed_b4	1	0x00	RW	[0] controls the sign of quadric coefficient, default 0
0x87	LSC column center	8	0x50	RW	Column center for LSC correction X4
0x88	LSC row center	7	0x3c	RW	[6:0] row center for LSC correction X4
0x89	LSC_dec_mode decrease_gain_1	7	0x12	RW	[6] LSC dec mode [5:0] decrease_gain_1
0x8a	decrease_gain_2	6	0x1a	RW	[5:0] decrease_gain_2
0x8b	decrease_gain_3	6	0x24	RW	[5:0] decrease_gain_3

DNDD(De-noise & De-defect)

Addr	Name	Width	Default Value	R/W	Description
0x40	DN_mode_en	5	0x07	RW	[7:5] NA [4] zero_weight_mode [3] share mode [2] c_weight_adap_mode [1] dn_lsc_mode [0] dn_b_mode
0x41	DN_mode_ratio	6	0x22	RW	[7:6] NA [5:4] C_weight_adaptive_ratio [3:2] dn_lsc_ratio [1:0] dn_b_mode_ratio
0x42	DN_bilat_b	6	0x15	RW	[7:6] NA [5:0] Fixed bilateral b value
0x43	DN_bilat_n DN_C_weight	8	0x05	RW	[7:4] Base noise level of each frame [3:0] base center pixel weight
0x44	DD_dark_bright_TH	8	0xe5	RW	DD_dark_bright_TH
0x45	DD_flat_TH	8	0x86	RW	//max-min/dd_ratio smaller DD_flat_TH

					[7:4] dd_th subtract one //max-min/dd_ratio smaller DD_flat_TH [3:0] dd_th subtract two
0x46	DD_limit DD_ratio	8	0x00 0x02	RW	[7:4] DD_limit, threshold of a defect pixel [3:2] NA [1:0] DD_ratio
0x47	DN_b_in_dark_en DN_C_coeff	6	0x90	RW	[7] DN_b_in_dark_en [6:5] NA [4:0] C_coeff
0x48	DN_b_in_dark_th DN_b_in_dark_slope	8	0xff	RW	[7:4]DN_b in dark th [3:0]DN b in dark slope
0x49	DN_BCR_mode	2	0x00	RW	[7:2] NA [1:0] DN BCR mode

AWB(Auto White Balance)

Addr	Name	Width	Default Value	R/W	Description
0x90	AWB_RGB _high	8	0xf5	RW	Defines the high RGB range of gray pixel to be selected
0x91	AWB_RGB _low	8	0x0a	RW	Defines the low RGB range of gray pixel to be selected
0x92	AWB_Y_to_C_diff	8	0x18	RW	Gray pixel criteria
0x93	AWB_Y_to_C_diff_big	8	0x10	RW	Gray pixel criteria when big_c mode enable
0x94	AWB_C_inter	8	0x20	RW	Cr and Cb line 1
0x95	AWB_C_inter2	8	0x40	RW	Cr and Cb line 2
0x96	AWB_C_inter_big	8	0x40	RW	Cr and Cb line 1 when big_c mode enable
0x97	AWB_C_inter2_big	8	0x80	RW	Cr and Cb line 2 when big_c mode enable
0x98	AWB_C_max	8	0x20	RW	Chroma limit
0x99	AWB_C_max_big	8	0x60	RW	Chroma limit when big_c mode enable
0x9a	AWB_Y_high	8	0xa0	RW	Give high luminance point more weight
0x9b	AWB_number_limit	8	0xa0	RW	Number limit
0x9c	AWB_C_number_limit	8	0x50	RW	Number limit when big C
0x9d	AWB_auto_window AWB_Skip_mode	3	0x08	RW	[3] AWB_auto_window [2] NA [1:0] AWB skip mode

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					00: 2x2 01: 4x4 10: 4x8 11: 8x8
0x9e	Light_gain_range	8	0x30	RW	When dark mode enable, if luma < th, stop AWB. Used in dark mode.
0x9f	move_number_limit	4	0x02	RW	[3:0] AWB is frozen in motion case, this parameter provides stability criteria
0xa0	show_and_mode	8	0x04	RW	[7:6] AWB show select mode, for debugging [5:3] NA [2] big_C_max mode [1] dark_mode [0] C_max_sel mode
0xa1	adjust_speed adjust_margin	7	0x42	RW	[7] NA [6:4] AWB gain adjust speed, the bigger the quicker. [3:0] if averages of R/G/B's difference is smaller than margin, it means AWB is OK, and AWB will stop.
0xa2	every_N	3	0x20	RW	[7] NA [6:4] AWB every N [3:0] NA
0xa3	AWB_outdoor_mode	8	0x00	RW	[7:6] NA [5] outdoor stop delay [4] outdoor start delay [3] outdoor valid, delay or soon [2] RGB low up gain mode [1] outdoor for gain limit enable [0] outdoor for RGB low auto extend
0xa4	AWB_C_weight_mode	8	0x20	RW	[7] when use_big_C add high luma gray pixel weight [6] when outdoor, add high luma gray pixel weight [5] anytime, add high luma gray pixel weight [4] when block sum is 0, allow adjust or not adjust [3:0] NA
0xa5	AWB_uplow_luma_v	8	0xe0	RW	Outdoor valid limit, when exp little

	alue				than it is enter outdoor
0xa6	AWB_R_gain_limit	8	0x70	RW	channel gain limit for R, G, B.
0xa7	AWB_G_gain_limit	8	0x58	RW	Float 2.6
0xa8	AWB_B_gain_limit	8	0x78	RW	
0xa9	AWB_R_out_h_gain_limit	8	0x50	RW	AWB outdoor R gain high limit
0xaa	AWB_G_out_h_gain_limit	8	0x58	RW	AWB outdoor G gain high limit
0xab	AWB_B_out_h_gain_limit	8	0x46	RW	AWB outdoor B gain high limit
0xac	AWB_R_out_l_gain_limit	8	0x40	RW	AWB outdoor R gain low limit
0xad	AWB_G_out_l_gain_limit	8	0x40	RW	AWB outdoor G gain low limit
0xae	AWB_B_out_l_gain_limit	8	0x40	RW	AWB outdoor B gain low limit
0xaf	AWB_CFA_seq	2	0x00	RW	AWB_pixel_type
0xb0	AWB_small_win_width_step	8	0x4d	RW	When auto_awb_window is 0, can be write
0xb1	AWB_small_win_height_step	8	0x3a	RW	When auto_awb_window is 0, can be write
0xb4	R_avg_use	8		RO	Average R by AWB module
0xb5	G_avg_use	8		RO	Average G by AWB module
0xb6	B_avg_use	8		RO	Average B by AWB module

AEC(Auto Exposure Control)

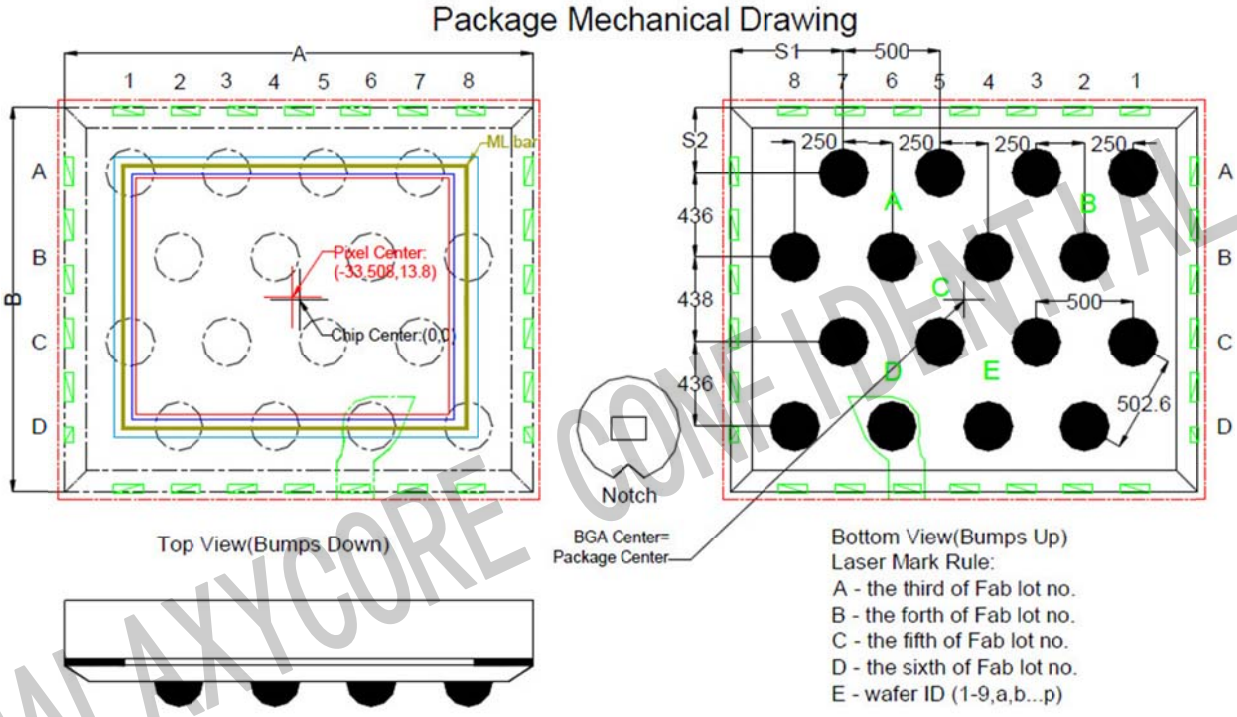
Addr	Name	Width	Default Value	R/W	Description
0xd0	AEC_mode1	8	0x00	RW	[7] ignore _more [6:4] select_mode [3] NA [2] mesure skip_mode [1:0] divde mode
0xd1	AEC_mode2	7	0x40	RW	[7] NA [6:4] AEC take action every N frame [3:2] close frame number to eliminate bad frame [1] change exp_gain_mode [0] dead_zone_mode:
0xd2	AEC_mode3	8	0x9e	RW	[7] AEC_enable

					[6:4] low_range X4 [3:0] high_range X16+15
0xd3	AEC_target_Y	8	0x50	RW	expected luminance value
0xd4	Y_average	8		RO	Current frame luma average
0xdb	AEC_slow_margin AEC_slow_speed	8	0x91	RW	[7:4] AEC slow margin, X4 [3] NA [2:0] AEC slow speed
0xdc	AEC_fast_margin AEC_fast_speed	8	0x96	RW	[7:4] AEC fast margin, X4 [3] NA [2:0] AEC fast speed
0xdd	AEC_exp_change _gain_ratio	8	0x96	RW	Gain change criteria, float 1.7, default use 1.2x
0xde	AEC_step2_sunlight	8	0x02	RW	AEC_step2_sunlight
0xdf	AEC_D_ratio	4	0x03	RW	[7:4] NA [3:0] PID D ratio
0xe0	AEC_I_stop_L _margin	7	0x07	RW	[7] NA [6:0] x2, Will be used as AEC convergence margin when 0xd1[0] =0
0xe1	AEC_I_stop_margin AEC_I_ratio	8	0x61	RW	[7:4] AEC adjust stop margin [3:0] integration coefficient
0xe2	AEC_anti_flicker_ste p[11:8]	4	0x00	RW	Anti_flicker step
0xe3	AEC_anti_flicker_ste p[7:0]	8	0x96	RW	
0xe4	AEC_exp_level_0[11 :8]	4	0x01	RW	Exposure level 0
0xe5	AEC_exp_level_0[7: 0]	8	0x2c	RW	
0xe6	AEC_exp_level_1[11 :8]	4	0x02	RW	Exposure level 1
0xe7	AEC_exp_level_1[7: 0]	8	0x58	RW	
0xe8	AEC_exp_level_2[11 :8]	4	0x03	RW	Exposure level 2
0xe9	AEC_exp_level_2[7: 0]	8	0x84	RW	
0xea	AEC_exp_level_3[11 :8]	4	0x05	RW	Exposure level 3
0xeb	AEC_exp_level_3[7: 0]	8	0xdc	RW	

0xec	AEC_max_exp_level AEC_exp_min_l[11:8]	6	0x20	RW	[5:4] Max level setting [4:0] exp_min[12:8]
0xed	AEC_exp_min_l[7:0]	8	0x04	RW	exp_min[7:0]
0xef	AEC_max_pre_dg_gain	8	0xc0	RW	The max of pregain AEC can output
0x24	big_win_x0	6	0x04	RW	Window setting for AEC & AWB
0x25	big_win_y0	6	0x02	RW	
0x26	big_win_x1	8	0x9c	RW	
0x27	big_win_y1	8	0x74	RW	

9. CSP package mechanical specifications

9.1 CSP package specifications



Package Dimensions

Description	Symbol	Nominal	Min.	Max.
		Millimeters		
Package Body Dimension X	A	2.420	2.395	2.445
Package Body Dimension Y	B	1.990	1.965	2.015
Package Height	C	0.750	0.690	0.810
Ball Height	C1	0.130	0.100	0.160
Package Body Thickness	C2	0.620	0.585	0.655
Thickness from top glass surface to wafer	C3	0.435	0.415	0.455
Ball Diameter	D	0.250	0.220	0.280
Total Ball Count	N	16		
Ball Count X axis	N1	4		
Ball Count Y axis	N2	4		
Edge to Pin Center Distance along X	S1	0.585	0.555	0.615
Edge to Pin Center Distance along Y	S2	0.340	0.310	0.370

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Revision History

Version1.0 2011.11.14

- Document Release

Version1.0 2011.11.30

- Update Register File