Summary of Changes Introduced According to Reviewers' Comments

January 6, 2014

Journal: Journal: ACM Journal of Emerging Technologies

Manuscript ID: CACM-12-04-1344

Original paper title: A Space-Efficient Design for a Reversible Floating Point Adder in Quantum Computing

Revised paper title: A Resource-Efficient Design for a Reversible Floating Point Adder in Quantum Computing

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Dear Editor,

We have addressed all of the reviewers' extensive (and very helpful) comments. As suggested, herewith we submit a new version of the paper.

We are submitting three documents: the article itself, a "diff" version of this paper and this document, detailing the changes.

Below, please find the detailed list of changes, together with the reviewers' comments. This letter ends with a list of additional modifications and a proposed list of additional references beyond those currently included in the article.

Best regards,

Trung Duc Nguyen and Rodney Van Meter

1 Reviewer: 1

Comments to the Author

1.1 Comment

I'm not an expert in hardware design, so it is a bit difficult for me to judge the novelty of this compared to related work. From the perspective of reversible computation generally, the problem approached is relevant, and the contribution of the work seems worthwhile. The results are not very exciting, but present a moderate improvement over an existing design. The paper is well written and accessible. It provides good motivation and builds up towards the proposed solution. There is balanced comparison to previous work, and a fair assessment of weaknesses of the new design (and of the suitability of floating-point arithmetic for quantum realisation in general).

Answer

Thank you for the positive comments. We believe the substantially reduced resource consumption, the correction of errors in the prior design, and the analysis of suitability for quantum computing are the primary contributions of the paper, and hope you find them important enough for the journal.

1.2 Comment

Where the paper leaves something to be desired is discussion of possible general lessons derived from the concrete solution. Are the improvements achieved, and the means for achieving them, a one-off thing, or can the ideas be reused in a principled way for related problems? Is there potential for transfer of these implementation ideas, to reap similar benefits for other units than the specific case of floating-point addition? The paper would be more convincing if some such considerations could be added.

Answer

There are some proposed units can be used in general not only in specific case of floating-point adder. For example, conditional swap unit and two's complement to sign-magnitude converter. In our proposed design, the conditional swap unit even got an improvement of the number of garbage output to 0. And in the two's complement to sign-magnitude converter we archive a truly reversible circuit

which can execute with both sign-magnitude and two's complement input while the existing design just leave garbage output and cannot run reversely.

1.3 Comment

page 2, line 34: Do you really mean "adapt", or "adopt"?

Answer

Changed to "adapt".

1.4 Comment

p 3, l 19: This line should not be indented.

Answer

Done.

1.5 Comment

p 4, l 42: "And example" → "An example"

Answer

Done.

1.6 Comment

p 4, l 49/50: "num bers" → "numbers" or "num-bers"

Answer

Done

1.7 Comment

p 7, l 52: "a n-bit" → "an n-bit" (pronunciation of "n-bit" starts with a vowel if read out, so the indefinite article needs to be "an")

Answer

Done.

1.8 Comment

p 11, l 35: "..., and the evaluation apparently contains several errors." Say, right away, that you will discuss these miscountings later in this section.

Answer

Rewritten. New text:

> This section describes in detail the resource miscountings and the differences between our proposed design and the NTR design.

1.9 Comment

p 12, l 29: "compare to" → "compared to"

Answer

Done.

1.10 Comment

p 15, l 47: "in term of" → "in terms of"

Answer

Done.

1.11 Comment

p 15, l 54: "can evaluation of" → "can evaluate", and "in term of" → "in terms of"

Answer

Done.

2 Reviewer: 2

Comments to the Author

2.1 Comment

The title of the paper does not truthfully reflect the content: The results are evaluated using no metric that takes the space of the physical implementation into account at all.

Answer

The "Space" in our title was intended to refer to number of logical qubit memories, but we now recognize that it might mislead readers into thinking we are addressing physical layout.

Moreover, our paper saves some 70% of the required memory capacity, but it also reduces the number of gates that must be applied by a similar amount, and we don't want to under-emphasize that contribution.

After consideration, we suggest, "A Resource-Efficient Design..." as a revised title.

2.2 Comment

In the introduction the authors claim that a reversible computer necessarily has no energy dissipation. This is false. A computer with no energy dissipation is necessarily reversible but not the other way round.

Answer

Rewritten. New text:

> In irreversible systems, Landauer showed that erasure of a single bit generates $kT \ln 2$ joules of heat energy where k is Boltzmann's constant of $1.38 \times 10^{-23} m^2 s^{-2} kg K^{-1}$ and T is the absolute temperature of the environment. If no information is erased, computation requires no release of heat. This has led to considerable interest in the study of reversible computing.

2.3 Comment

The authors should state more clearly that by "reducing the garbage" they refer to decreasing the amount of auxiliary variables that remain in a dirty state. In equation (1), $4 \times 32 + |G|$ variables are used whereas the original approach uses $3 \times 32 + |G|$ variables. As no size for either of the Gs (presumably they are different) is given it is impossible to judge whether the new approach uses less variables, which is a crucial point as variables are expensive to realize.

Answer

Here, we believe the reviewer has misread the paper. There is no reason to believe that the G in Eq. 1 is different from the G in the text just above, and in either case the point of Eq. 1 is that G can be erased.

The formulation just above uses three 32-bit registers and a fourth whose size is unspecified but described as "large". (In fact, it is hundreds of bits, as detailed later in the paper, but it is too early to introduce this here.) All four of those registers are in permanent use, with dirty (and, in the case of quantum variables, possibly entangled) data.

The formulation in Eq. 1, uses those same four registers plus a fifth (unspecified but fairly obviously 32 bits) *temporary* register. Both the large G register and the fifth register are *cleaned* by the process of Eq. 1, resulting in far less garbage after completion.

We believe that the explanation as it stands is as clear as possible at this point in the paper, and would like to leave it as-is.

2.4 Comment

I do not understand why the number of steps containing T gates is used as a metric. This would lead to different costs for the following two circuits
-T-H-
-H-T-
and
-T-H-
-T-H-
Intuitively the costs of these circuits should be identical. Unfortunately the authors do not justify this way of counting or give a reference for this metric.

Answer

The T and $T^\dagger$ gates are the most expensive elements in a fault-tolerant implementation of the Clifford+T set. Therefore, it has become common practice to ignore the cost of H and $CNOT$ gates, and count only the T and $T^\dagger$ gates when assessing circuit depth and total execution cost. There is a paper of Selinger [2] which explain how to design a Toffoli gate with least of T-depth. The paper actually archive a Toffoli circuit with T-depth one.

2.5 Comment

In figure 4 the bitwidth for the alignment operation is stated to be 64. But counting the rectangles with 0/1 in it as 1 bit and the long blocks with the amount stated above I count 67 bits.

Answer

We are sorry for drawing an ambiguous figure that make the misunderstanding for the reviewer. The bitwidth for the alignment operation is exactly 64 bits, includes 40 additional 0-bits and 23 bits from *Conditional Swap* unit plus a bit of 1 at the first place. The figure is redrawn to avoid this misunderstanding.

2.6 Comment

The background section should give a more detailed introduction/explanation of the KQ metric.

Answer

Newly written text:

> Roughly speaking, KQ is the time-space product of the circuit. Assuming the error probability of each qubit is independent and the same for one time step, we need to engineer the error correction system to give a post-correction error probability of $e \ll 1/KQ$ to ensure successful operation of our circuit with high probability.

2.7 Comment

I do not understand the last sentence of the paper. The authors want to restrict the range of the input values in order to improve the reversibility. If one restricts the input then it wouldn't be conform to IEEE-754 anymore. Furthermore, reversibility is nothing that can be "improved". A function/circuit is either reversible or irreversible. There is nothing in between.

Answer

Deleted.

2.8 Comment

The authors do not cite properly. In section 2 Steane's KQ metric is mentioned with no reference (later in the paper they do cite the corresponding work correctly), the statement that "quantum computers are susceptible to making errors" has no reference at all and for the IEEE-754 format wikipedia is cited instead of the official standard.

Answer

We have added the citation of corresponding work for Steane's KQ metric at the first place it mentioned and replaced the reference of the IEEE-754 format wikipedia by the official standard from IEEE [4]. We also added reference for "quantum computers are susceptible to making errors" [3].

2.9 Comment

When printed, the figures 10, 12a), 14 , and 4 loose the whitespaces between the characters and are difficult to read.

Answer

We have printed out the paper and check the mistakes but the figures seem not to have the mentioned problem. But we realize that the improper size of these figures might cause the problem for some readers, thus we adjust the sizes slightly bigger.

2.10 Comment

The authors reference related work in the abstract. I consider this as bad style.

Answer

The reference for related work in the abstract has been removed.

3 Additional Modifications

In addition to the requests from the reviewers and editor, the following modifications have been made:

- Figure 4 has been redrawn.

4 Additional Proposed References

The following references has been added to the paper as reviewers asked

References

[1] A. Ambainis, A. Childs, and B. Reichardt. Any and-or formula of size n can be evaluated in time $n^{1/2+o(1)}$ on a quantum computer. In *Foundations of Computer Science, 2007. FOCS'07. 48th Annual IEEE Symposium on*, pages 363–372. IEEE, 2007.

[2] Peter Selinger. 2013. Quantum circuits of T-depth one. *Phys. Rev. A* 87 (Apr 2013), 042302. Issue 4.

`http://dx.doi.org/10.1103/PhysRevA.87.042302`

[3] John Preskill. 1997b. Reliable Quantum Computers. (1997).

[4] IEEE Task P754. 2008. *IEEE 754-2008, Standard for Floating-Point Arithmetic*. 58 pages. (electronic)

`http://dx.doi.org/10.1109/IEEESTD.2008.4610935`