Department of Electrical and Computer Engineering

ENEL 453: Digital System Design

Fall 2019

Lab 5: Direct Digital Synthesis and AM/FM Modulation

1. Overview

In this lab project, you will build upon your previous lab projects to create a system which performs AM and FM modulation using Direct Digital Synthesis (DDS). This lab project is worth 35% of your term grade (replaces final exam) and only qualified students will receive credit for this project and be able to replace the final exam. It is expected that students perform some background research to understand the design challenge and possible solutions. These topics include:

- Direct Digital Synthesis (DDS)
- Numerically Controlled Oscillator (NCO)
- Phase Accumulator
- AM modulation
- FM modulation
- Linear Feedback Shift Register (LFSR).

The two main components of Lab 5 are:

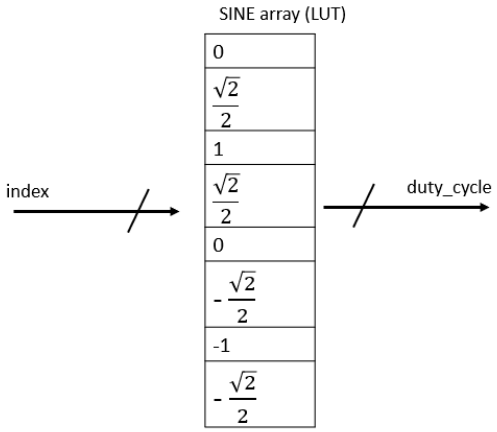
- Implement a sine-wave output waveform using the array technique used in Lab 3, i.e. a look-up table for the sine values. This sine-wave will be the carrier waveform for the AM and FM modulation, with a frequency of 650 kHz.
- The system will be able to switch between AM and FM modulation, based on a slide switch position. The output of the distance measurer will control the modulation of the carrier, e.g. moving your had in front of the distance measurer will result in changes to the carrier (AM or FM, as selected).

This project is optional and only for students who qualified with at least 80% on the midterm and 80% for Labs 1 to 3. These qualifying students will use this project in replacement of their final exam. The qualified students who choose to complete Lab 5 have the option to abandon the project and write the final exam instead.

2. Direct Digital Synthesis

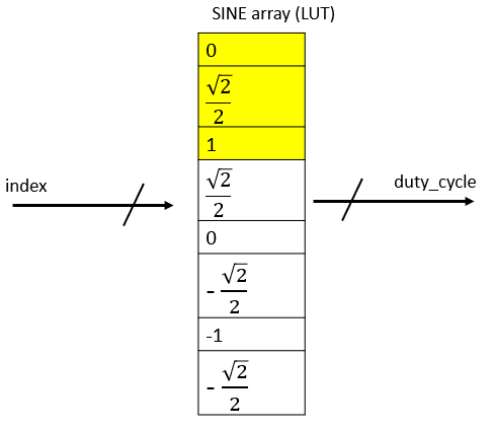
Direct Digital Synthesis (DDS) is a very widespread and powerful technique that is used in telecommunications and instrumentation. With DDS, a look-up-table (LUT) stores the values of a waveform to be generated. In our case the waveform is a sine-wave. We used a LUT in the format of an array in Lab 3 to convert voltage to distance. A very important part of DDS is a Numerically Controlled Oscillator (NCO). You are encouraged to research DDS and NCO, but some basics are given below.

The NCO contains a LUT to store the values of a waveform, which is a sine wave in our case, and shown in the figure below for a very small LUT. The output of the LUT is a duty cycle which you would pass as an input to the PWM DAC to generate the final output waveform.



However, we can notice that the sine wave between 180 to 360 degrees is the negation of the sine wave values between 0 and 180 degrees. Thus, we can save space in our LUT by negating our values when our index (the input to the LUT) is in the range 180 to 360 degrees.

However, we can also notice further symmetry in the sine waveform as the range 0 to 90 degrees is the mirror image of the range 90 to 180 degrees. So, we can have a LUT whose contents store only the first ¼ cycle of the sine wave, as shown highlighted in yellow below, as long as we are clever with how we manipulate our index and selectively negate our output. We would also need to determine how we manage our negative values, which will be another design decision.



3. AM AND FM MODULATION

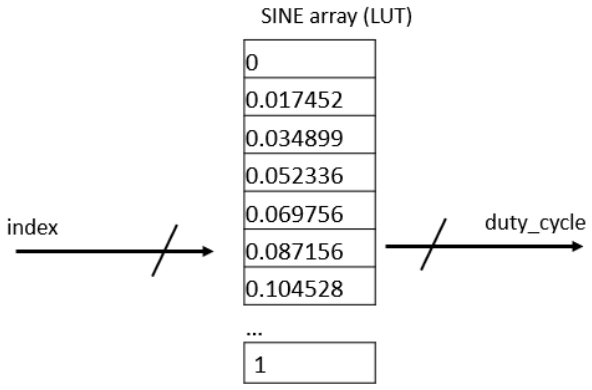
In both AM and FM modulation, a carrier waveform is modified to generate the output signal. In our case the carrier waveform will be a 650 kHz sine wave, which is in the range of AM radio.

In AM modulation, the amplitude of the carrier waveform will be modified by a signal. You will implement this with a multiplier controlled by the distance measurer output, e.g. if the distance is close (4 cm) then the amplitude of the carrier is approximately 0 V_{p-p} and if the distance gradually increases to (33 cm) then the amplitude of the carrier will gradually increase to approximately 3.3 V_{p-p}. You will determine how to implement the multiplier, whether it is in straight VHDL code or using one of the multipliers built into the FPGA (like how we used the FPGA's ADC component).

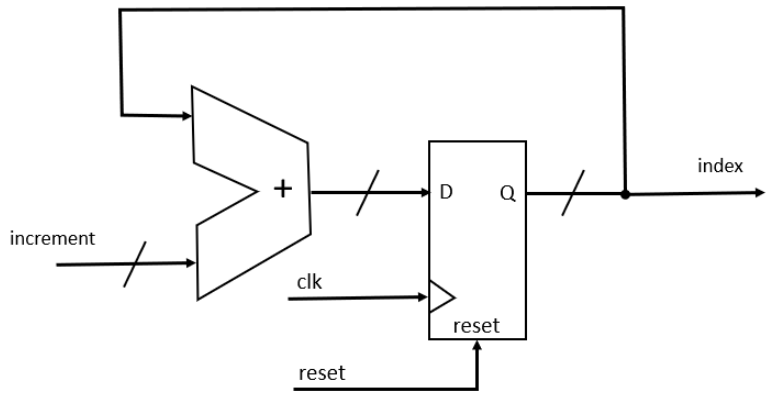
In FM modulation, the frequency of the carrier is modified by a signal. You will implement this with a smart way to manipulate the index to the LUT and modify the frequency of the carrier, e.g. if the distance is close (4 cm) then the frequency will be around 640 kHz and if the distance gradually increases to (33 cm) then the frequency will gradually increase to 660 kHz.

To explain manipulating the index using a hypothetical example, if you increment the index to the LUT by 1 (i.e. 0, 1, 2, 3, etc), you will obtain a sine wave of a certain frequency, say 100 kHz. However, if you increment the index by 2 (i.e. 0, 2, 4, 6, etc), then the output frequency will be doubled, at 200 kHz.

For illustration, below is shown an LUT with each index value separated by 1 degree, and this LUT stores only a ¼ cycle of the sine wave. If we increment by 1, then we would obtain a sine wave of say 100 kHz. If we increment by 2, we obtain 200 kHz. If we increment by 3, we obtain obtain 300 kHz. In our case, perhaps an increment of 100 may be a reasonable place to start for generating the 640 kHz carrier sine wave.

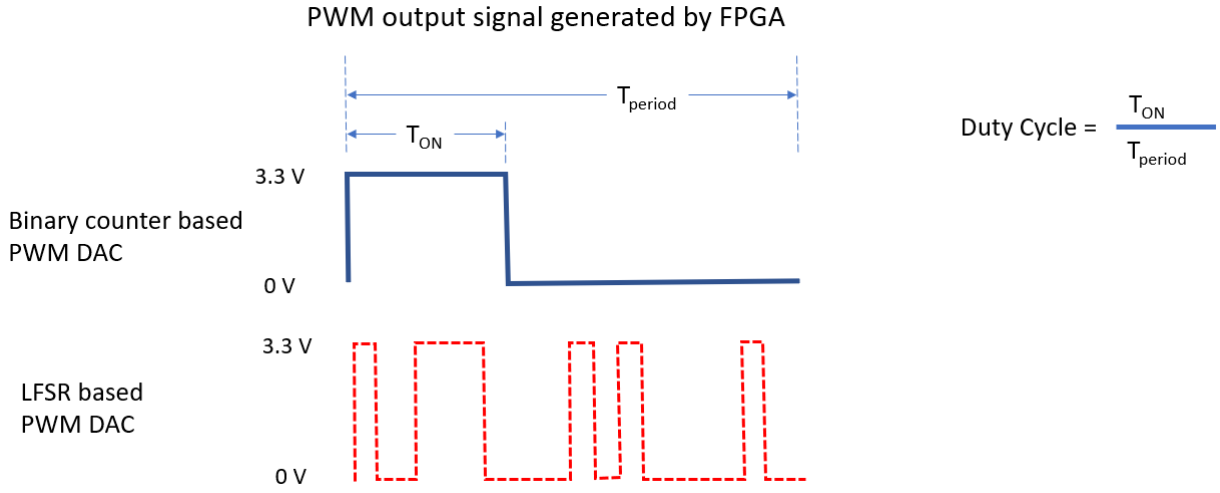


A way to control the increment to the LUT is shown below, using a well-known circuit called a Phase Accumulator. The phase accumulator stores the current phase (i.e. the current index value to the LUT) and adds the desired increment (e.g. a value related to the distance measurer output).



4. A CLEVER TRICK TO SPEED UP YOUR PWM DAC

The period of your PWM DAC is limited by the count period (2^n values for a n-bit counter). However, if you use the simple Linear Feedback Shift Register (LFSR) to replace the counter in your PWM DAC, then you can generate much higher speed analog signals from your DAC. The LFSR produces a pseudo-random number sequence, and the result for the PWM DAC will be to spread the high time of the duty cycle in the count period to be a pseudo-random sequence of short pulses of the same high time, as shown in the illustration below. In this case you must also increase the cutoff frequency (f_c) of your RC filter.



5. Design Record Document

Within 24 hours of completing your demonstration, upload to D2L the following (**for each student**):

1. Your VHDL design files for the complete design as demonstrated.
2. Your constraints files (.sdc and .qsf).
3. Optional: Your top-level VHDL testbench (only if you have one, you are free to choose to make one for you own development).
4. Your Design Record document with the following:
   - 4.1 Your name and your partner's name on the first page of your document.
   - 4.2 A screenshot of your top-level RTL schematic.
   - 4.3 Screenshot of your Timing Report, showing the maximum clock frequency of your design.
   - 4.4 Optional: Screenshots of the simulation waveforms showing the correct operation of the top-level design (only if you created a top-level testbench).
   - 4.5 Note that no write-up is required.

6. GRADING

You must show the following to the instructor to obtain your credit for the lab, and the instructor may request further demonstration than listed below.

All team members must be able to explain their design and answer questions about any part of the lab project in order to receive credit for the project.

Only qualified students are permitted to complete Lab 5 to replace their final exam.

Description	Marks
In-lab demonstration: 1. FM modulation of the 650 kHz carrier waveform, controlled by the distance measurer output. The frequency range should be approximately in the range of +/- 10 kHz of the 650 kHz carrier (i.e. an FM modulation index of $\frac{10\ kHz}{650\ kHz} = 1.5\%$), based on the distance measurer output. 2. AM modulation of the 650 kHz carrier waveform, controlled by the distance measurer output. The amplitude of the carrier should approximately range from 0 V to 3.3 V (i.e. an AM modulation index of $\frac{\frac{3.3\ V}{2}}{\frac{3.3\ V}{2}} = 100\%$), based on the distance measurer output. The above functionality must be demonstrated to receive credit for completing the lab. Students **must be able to explain their design and answer questions to receive credit** for completing the lab. The maximum frequency in the Timing Summary must be **at least 50 MHz**. The design must be synchronous: • all asynchronous inputs to the system **must be synchronized** (i.e. pushbuttons and switches), • only one clock edge must be used, i.e. only **rising_edge(clk)**. Demonstrations can be held at converted lecture/lab periods on Tuesdays and Thursdays starting 9:30 am, or or in the lab periods. All demonstrations must be completed by the last lab period, Thursday Dec 5. • Late demonstrations will receive zero marks. If your project does not go well, you still have the option to write the final exam.	20 15
To receive the above marks and credit for the lab, **all the files specified in Section 6 must be uploaded by each student to the Dropbox in D2L within 24 hours after you demonstrate**. Do not worry about special formatting or documenting the screenshots, just paste them into a Word document, PDF it, and upload the PDF.	