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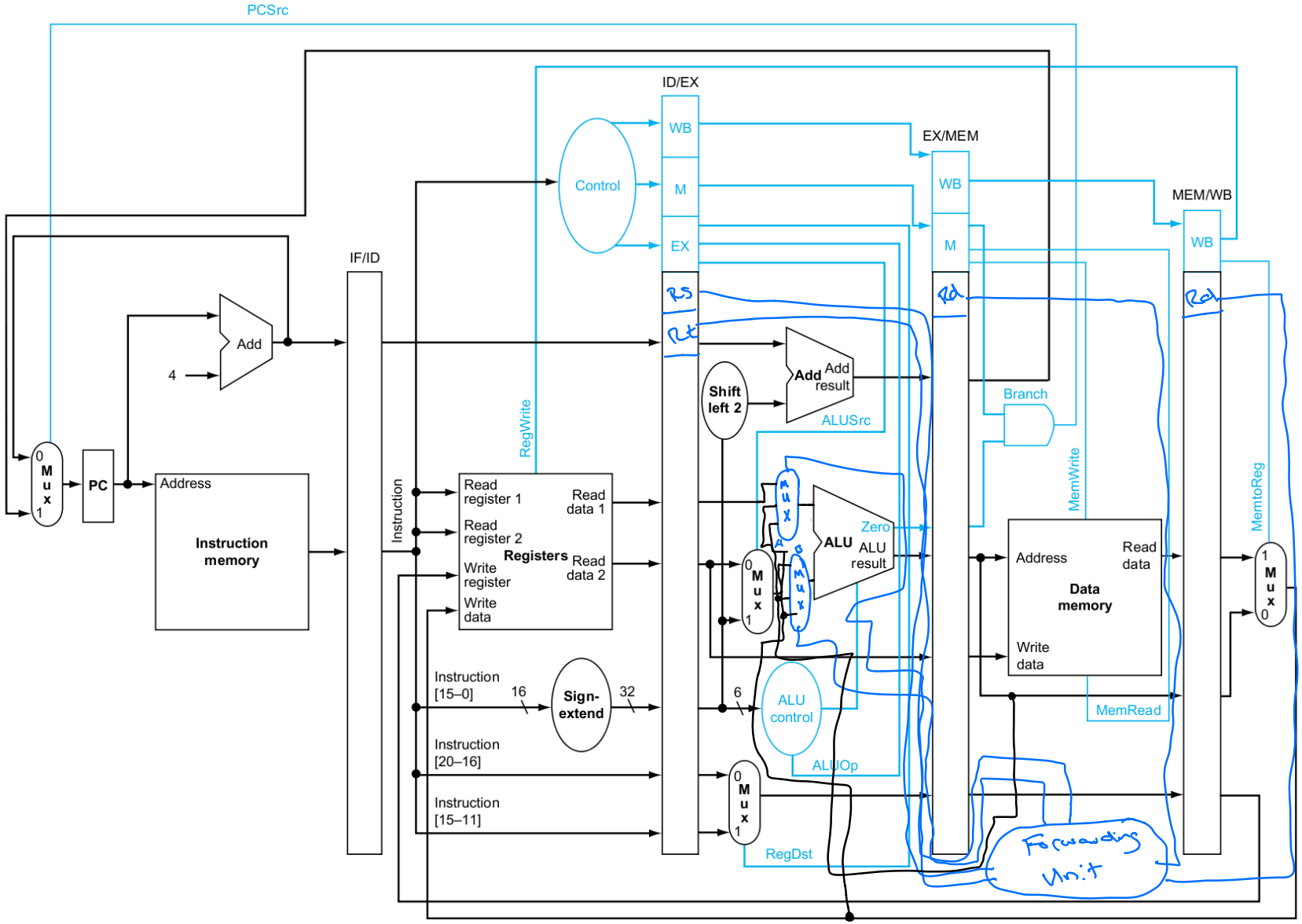
EC413 lab 7

- Task 1: see pre-lab
- Task 2: Implemented a forwarding unit that checks if the Rd in EX/MEM stage is the same as Rs or Rt in ID/EX stage. It then sends out a 2 bit mux signal to the corresponding mux that outputs into the ALU.
- Task 3: Implemented a new part of the forwarding unit that checks if Rd in MEM/WB is the same as Rs or Rt in ID/EX. It also directs the forwarding unit to output a 2 bit mux signal to the corresponding muxA or muxB.
- Task 4: Add a new condition to 2-ahead: as long as Rd in EX/MEM isn't the same as Rd in MEM/WB (and thus requiring a 1 ahead), the 2 ahead mux signals are outputted.
- Task 5: Added logic to the forwarding unit that checks that Rd in EX/MEM isn't equal to 0 for the 1 ahead cases, and MEM/WB for the 2 ahead cases.
- Task 6: Added RegWrite as an input to our forwarding unit. Added conditions in the if statements that checks if RegWrite is = 0 for corresponding cases (1 ahead A/B, 2 ahead A/B).
- Task 7: added a test case to the testbench that uses BEQ (which is a no-write instruction)


PCSrc
ID/EX
EX/MEM
MEM/WB
IF/ID
WB
M
EX
Control
Add
4
PC
Address
Instruction memory
Instruction
RegWrite
Read register 1
Read register 2
Registers
Write register
Write data
Read data 1
Read data 2
Instruction [15–0]
16
Sign-extend
32
Instruction [20–16]
Instruction [15–11]
Shift left 2
Add
Add result
ALUSrc
ALU
Zero
ALU result
6
ALU control
ALUOp
RegDst
Branch
MemWrite
MemRead
MemtoReg
Address
Read data
Data memory
Write data
Forwarding Unit