EC413 Lab – Pipelined CPUs

Overview

The purpose of the Pipelined CPUs Lab is to learn in-depth how a *pipelined* CPU works. Given the standard five-stage MIPS CPU with no forwarding support, you will add, debug, and test several new features.

Tasks

1. Synthesize the project and generate outputs for the given instruction sequence. [Pre-lab]
2. Add “1 ahead” forwarding
3. Add “2 ahead” forwarding
4. Add arbitration logic for deciding between 1 & 2 ahead
5. Add logic for $0 write
6. Add logic for No Write
7. Check register bypass works

Extra Credit

Handle LW followed by SW (RAW hazard). Note that this does not require any stalls.

Report

For each task, describe what you did. For your modified hardware, submit a modified diagram.