



THIS DOCUMENT AND THE DATA DISCLOSED HEREIN OR  
HEREWITH IS THE PROPERTY OF ALTIUM LIMITED AND MAY  
BE FREELY DISTRIBUTED IN WHOLE. NO RIGHTS ARE  
RESERVED OR EXPRESS OR IMPLIED WARANTEE GIVEN.

REVISION	DESCRIPTION	DATE	APPROVED

F

F

E

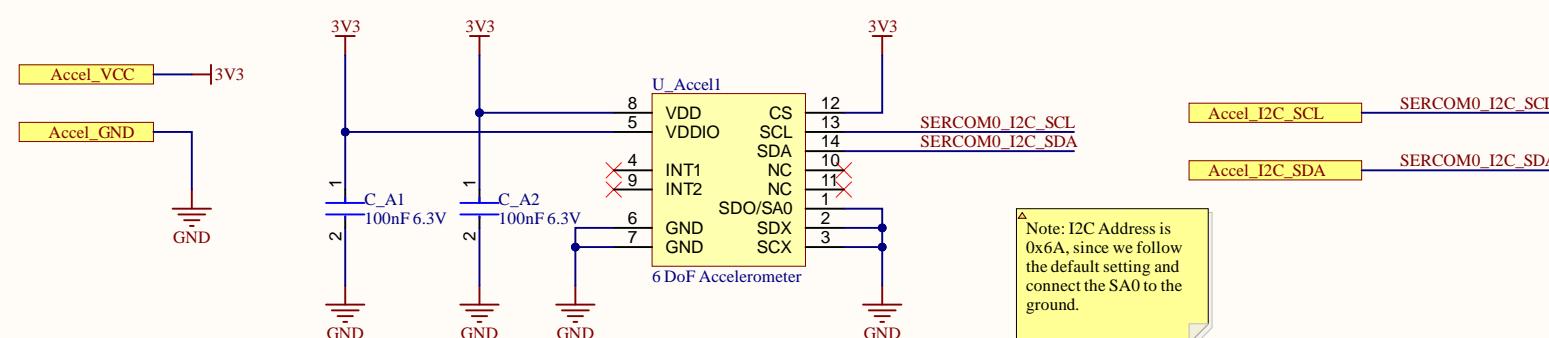
E

D

D

C

C



APPROVALS	DATE	PROJECT	Penn Engineering	*
ENG: *		UNIVERSITY OF PENNSYLVANIA	*	*
DSN: *		PROJECT REVISION:	DOCUMENT REVISION:	DESIGN ITEM:
CHK: *		TITLE		
REFERENCE DOCUMENTS				
BOM:	Accelerometer			
ASSY DWG:	SIZE	CAGE CODE	DWG NO.	REV
FAB DWG:	B			1.0
PCB DWG:	SCALE:	FILE NAME	Accelerometer.SchDoc	SHEET 1 OF 1

THIS DOCUMENT AND THE DATA DISCLOSED HEREIN OR  
HEREWITH IS THE PROPERTY OF ALTIUM LIMITED AND MAY  
BE FREELY DISTRIBUTED IN WHOLE. NO RIGHTS ARE  
RESERVED OR EXPRESS OR IMPLIED WARANTEE GIVEN.

REVISION	DESCRIPTION	DATE	APPROVED

F

F

E

E

D

D

C

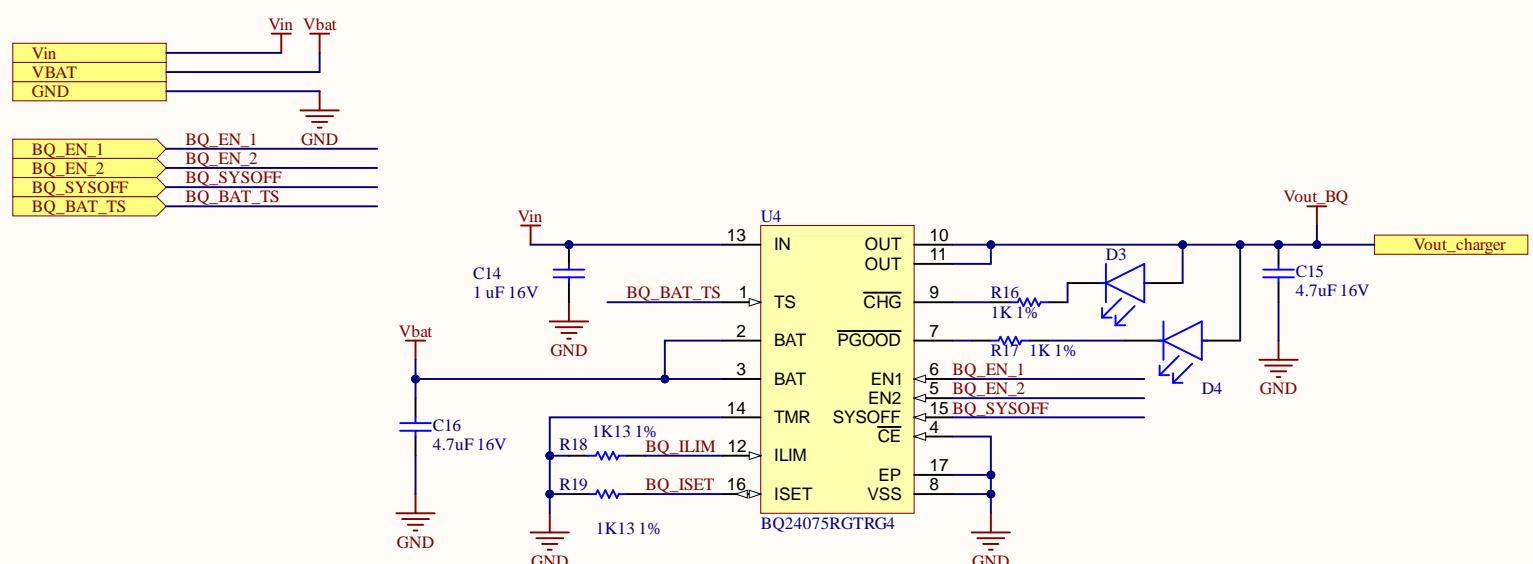
C

B

B

A

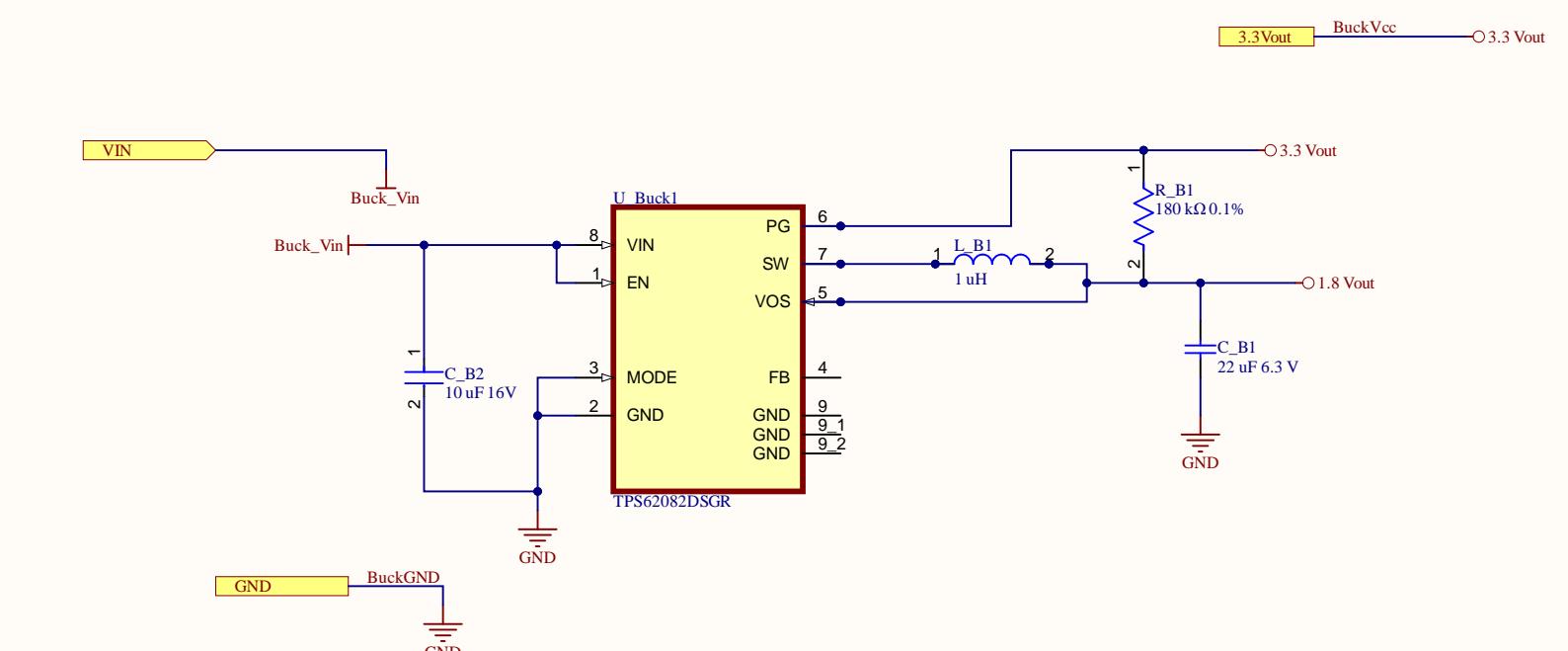
A



APPROVALS	DATE	PROJECT	Penn Engineering
ENG:	*	UNIVERSITY OF PENNSYLVANIA	*
DSN:	*	PROJECT REVISION:	DOCUMENT REVISION:
CHK:	*	DESIGN ITEM:	
REFERENCE DOCUMENTS		TITLE	
BOM:	LiPo Charger		
ASSY DWG:	SIZE	CAGE CODE	DWG NO.
FAB DWG:	B		
PCB DWG:	SCALE:	FILE NAME	LiPo_Charger.SchDoc
		SHEET	1 OF 1

THIS DOCUMENT AND THE DATA DISCLOSED HEREIN OR  
HEREWITH IS THE PROPERTY OF ALTIUM LIMITED AND MAY  
BE FREELY DISTRIBUTED IN WHOLE. NO RIGHTS ARE  
RESERVED OR EXPRESS OR IMPLIED WARANTEE GIVEN.

REVISION	DESCRIPTION	DATE	APPROVED



APPROVALS	DATE	PROJECT	Penn Engineering
ENG:	*	UNIVERSITY OF PENNSYLVANIA	*
DSN:	*	PROJECT REVISION:	DOCUMENT REVISION:
CHK:	*	DESIGN ITEM:	
REFERENCE DOCUMENTS		TITLE	
BOM:		Buck Converter	
ASSY DWG:		SIZE	CAGE CODE
FAB DWG:		DWG NO.	
PCB DWG:		REV	1.0
SCALE:	FILE NAME	BuckConverter.SchDoc	SHEET 1 OF 1

THIS DOCUMENT AND THE DATA DISCLOSED HEREIN OR  
HEREWITH IS THE PROPERTY OF ALTIUM LIMITED AND MAY  
BE FREELY DISTRIBUTED IN WHOLE. NO RIGHTS ARE  
RESERVED OR EXPRESS OR IMPLIED WARANTEE GIVEN.

DWG. NO. 1.0.1 REV. SHT.		REVISION	DESCRIPTION	DATE	APPROVED

F

F

E

E

D

D

C

C

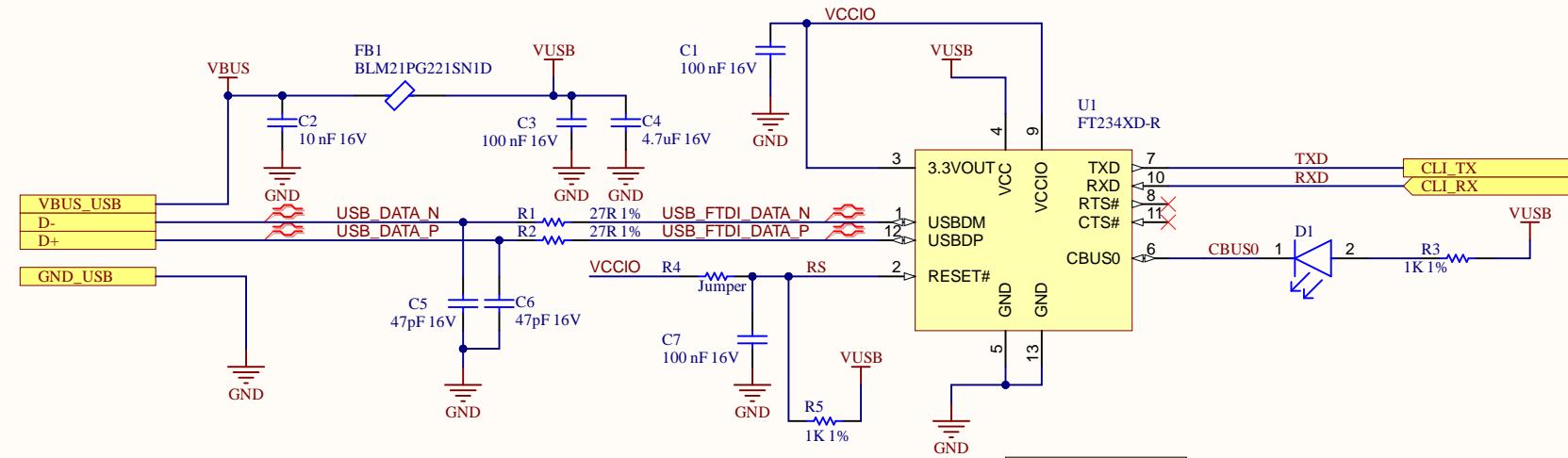
B

B

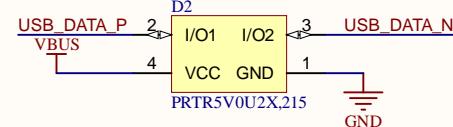
A

A

## FTDI CHIP



## USB ESD PROTECTION



APPROVALS	DATE	PROJECT	Penn Engineering
ENG:		PROJECT REVISION:	DOCUMENT REVISION:
DSN:		DESIGN ITEM:	
CHK:		TITLE:	
REFERENCE DOCUMENTS		USB Slot + FTDI	
BOM:	ASSY DWG:	SIZE	CAGE CODE
	FAB DWG:	DWG NO.	
	PCB DWG:	REV	1.0
SCALE:	FILE NAME	FTDI.SchDoc	SHEET 1 OF 1

F

F

E

E

D

D

C

C

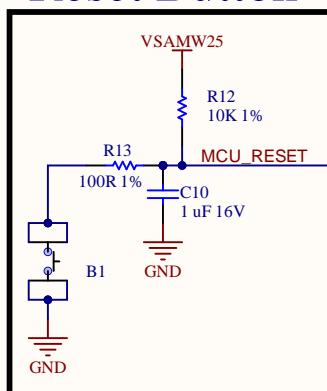
B

B

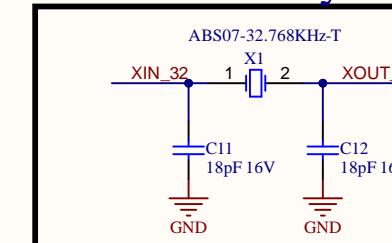
A

A

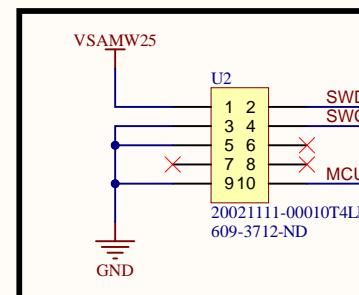
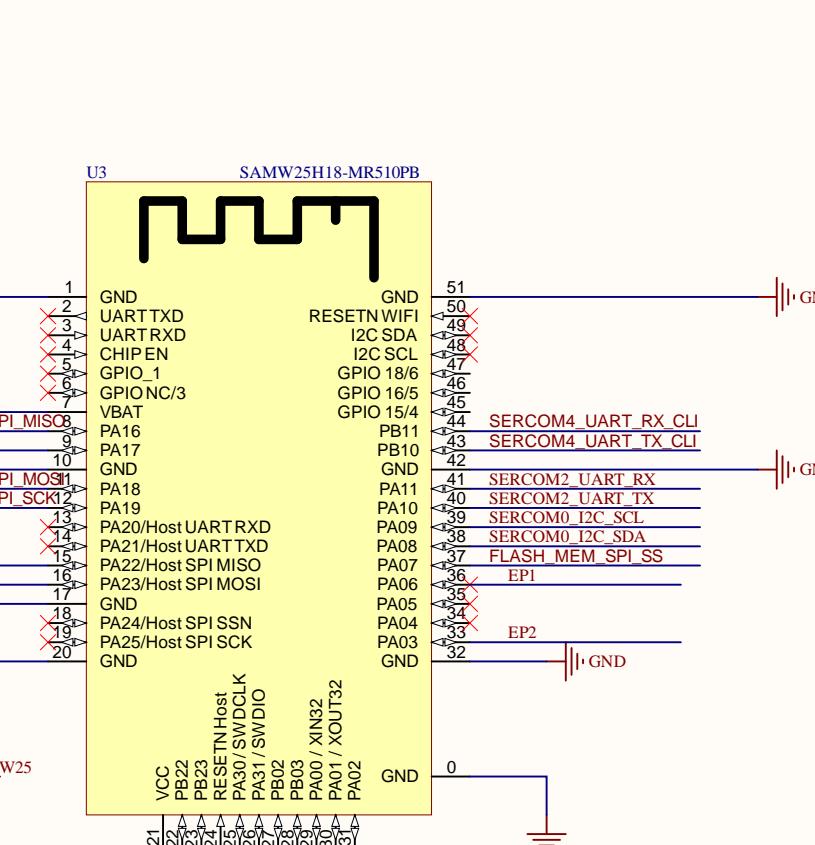
## Reset Button



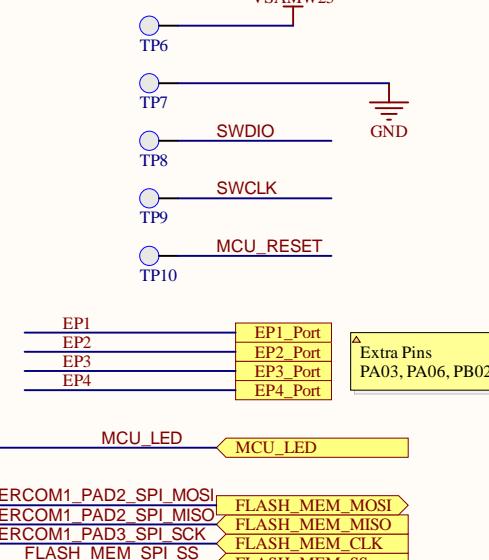
## 32.768 Crystal



Calculation of crystal load capacitors:  
 $C_{ext} = 2 \times (C_{crystal} - C_{para} - C_{pcb})$   
 Ccrystal = 12.5pF (from crystal - Ccrystal)  
 Cpara = 3.15pF (from MCU datasheet)  
 Cpcb = 0.5pF (estimate)  
 $C_{ext} = 2 \times (12.5pF - 3.15pF - 0.5pF) = 17.7pF$



## DEBUGGER PORT



SERCOM2\_UART\_RX  
SERCOM2\_UART\_TX  
SERCOM3\_I2C\_SCL  
SERCOM3\_I2C\_SDA  
SERCOM0\_I2C\_SCL  
SERCOM0\_I2C\_SDA

GPS\_RX  
GPS\_TX  
OLED\_I2C\_SCL  
OLED\_I2C\_SDA  
Accel\_I2C\_SCL  
Accel\_I2C\_SDA

APPROVALS	DATE	PROJECT	Penn Engineering
ENG:	*	DOCUMENT REVISION:	UNIVERSITY OF PENNSYLVANIA
DSN:	*	DESIGN ITEM:	
CHK:	*	MCU Module	
REFERENCE DOCUMENTS			
BOM:			
ASSY DWG:			
FAB DWG:			
PCB DWG:			
SCALE:	FILE NAME	MCU.SchDoc	REV 1.0
CAGE CODE		DWG NO.	
1		1	

THIS DOCUMENT AND THE DATA DISCLOSED HEREIN OR  
HEREWITH IS THE PROPERTY OF ALTIUM LIMITED AND MAY  
BE FREELY DISTRIBUTED IN WHOLE. NO RIGHTS ARE  
RESERVED OR EXPRESS OR IMPLIED WARANTEE GIVEN.

DWG. NO.	1.0.1	REV. SHT.	REVISION	DESCRIPTION	DATE	APPROVED

F

F

E

E

D

D

C

C

## TESTPOINTS

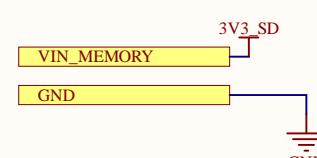
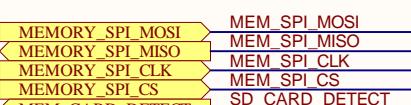
TP11	3V3_SD
TP12	SD_CARD_DETECT
TP13	MEM_SPI_MOSI
TP14	MEM_SPI_MISO
TP15	MEM_SPI_CLK
TP16	MEM_SPI_CS

B

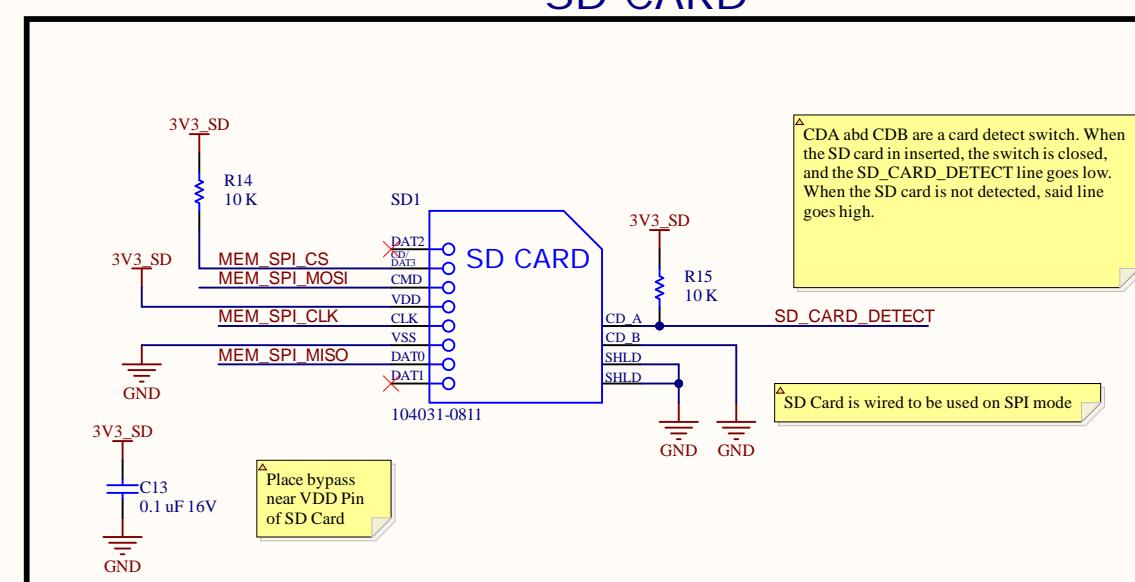
B

A

A



## SD CARD

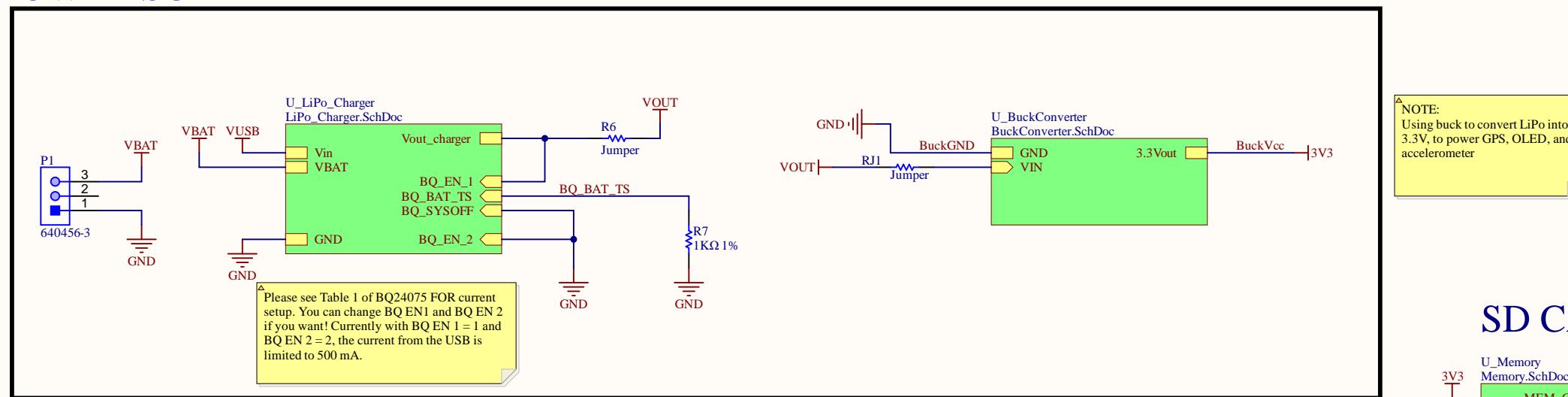


APPROVALS	DATE	PROJECT	Penn Engineering
ENG: Weihsio Huang		UNIVERSITY OF PENNSYLVANIA	*
DSN: *		PROJECT REVISION:	DOCUMENT REVISION:
CHK: *		DESIGN ITEM:	
REFERENCE DOCUMENTS		TITLE: SD Card Module	
BOM:	ASSY DWG:	SIZE	CAGE CODE
		DWG NO.	
	FAB DWG:		
	PCB DWG:	SCALE:	FILE NAME Memory.SchDoc
			SHEET 1 OF 1

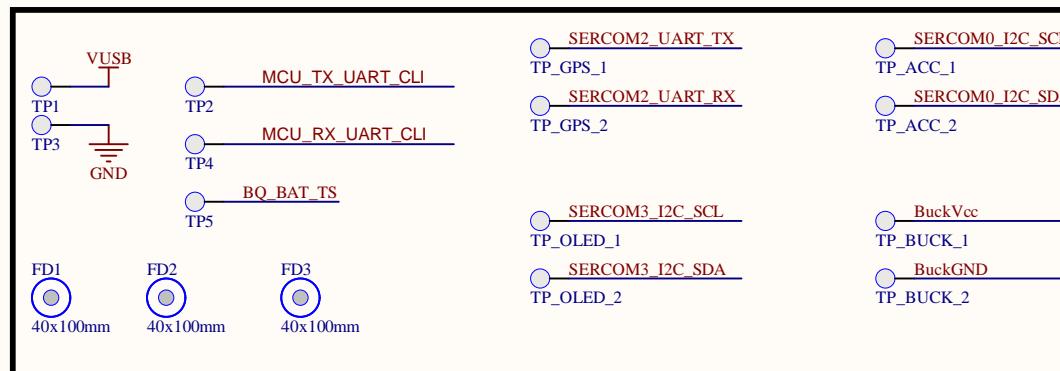
THIS DOCUMENT AND THE DATA DISCLOSED HEREIN OR  
HEREWITH IS THE PROPERTY OF ALTIUM LIMITED AND MAY  
BE FREELY DISTRIBUTED IN WHOLE. NO RIGHTS ARE  
RESERVED OR EXPRESS OR IMPLIED WARANTEE GIVEN.

DWG. NO.	REV.	SHT.	REVISION	DESCRIPTION	DATE	APPROVED
1.0.1						

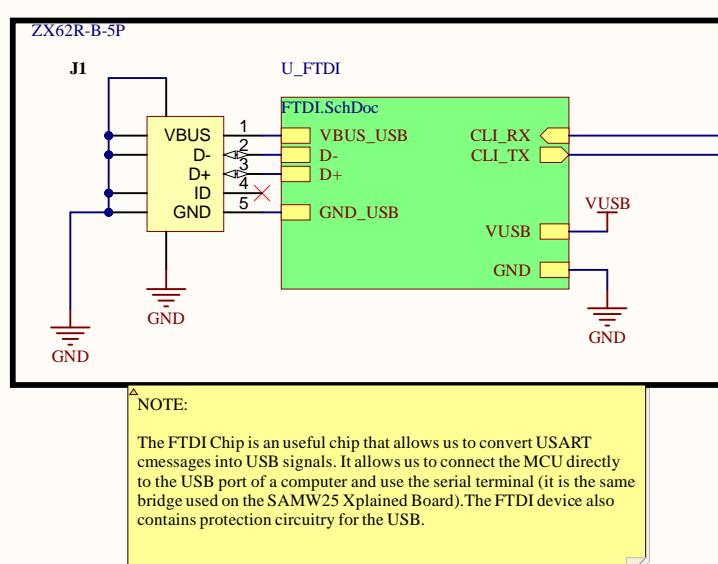
## F POWER SUPPLY



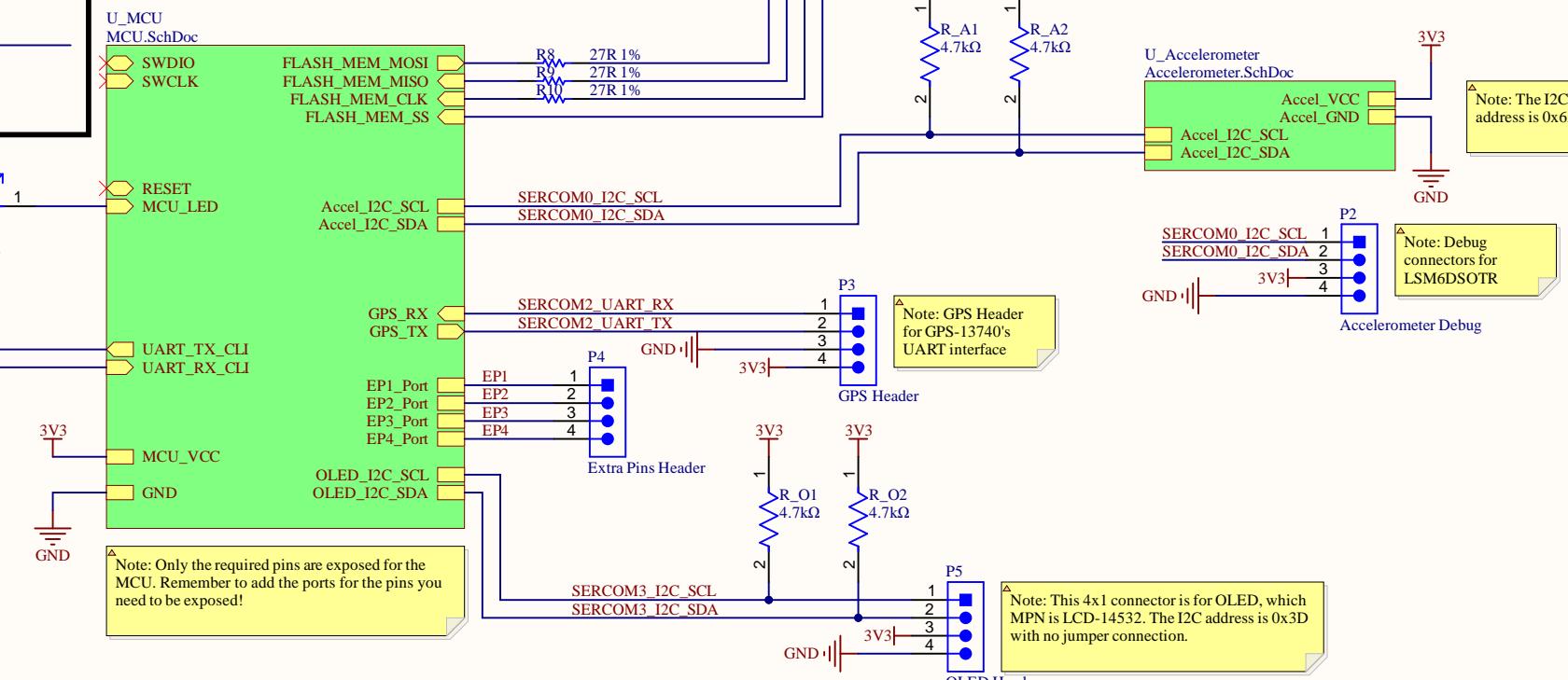
## D TEST POINTS AND FIDUCIALS



## B USB CONNECTOR + FTDI



## C MCU



APPROVALS		DATE	PROJECT	Penn Engineering
ENG:	Weihao Huang			UNIVERSITY OF PENNSYLVANIA
DSN:	*		PROJECT REVISION:	DOCUMENT REVISION:
CHK:	*		DESIGN ITEM:	Mainboard
REFERENCE DOCUMENTS		TITLE	IoTracking_Main	
BOM:			SIZE	CAGE CODE
ASSY DWG:			DWG NO.	
FAB DWG:			REV	1.0
PCB DWG:			SCALE:	FILE NAME MAIN.SchDoc
			SHEET	1 OF 1

## Manufacturing Notes

Four (4) Layers

Dimensions: 70mm x 70mm

Thickness: 0.062"

Material: FR4

All layers are unmirrored - should be able to "see straight through"

Scoring: None

Finished Thickness: 0.062 inches

Surface Finish: ENIG

Gold Fingers: No

Outer layer finish copper: 1 oz

Number of Holes: 202

Min. Hole Diameter = 0.508mm

Min. Trace (Outer Layer) = 0.006 inches

Min. Distance = 0.006 inches

Solder Mask Color: Red

Soil Screen Sides: Both

Silk Screen Color: White

Thickness Tolerance: +/- 10%

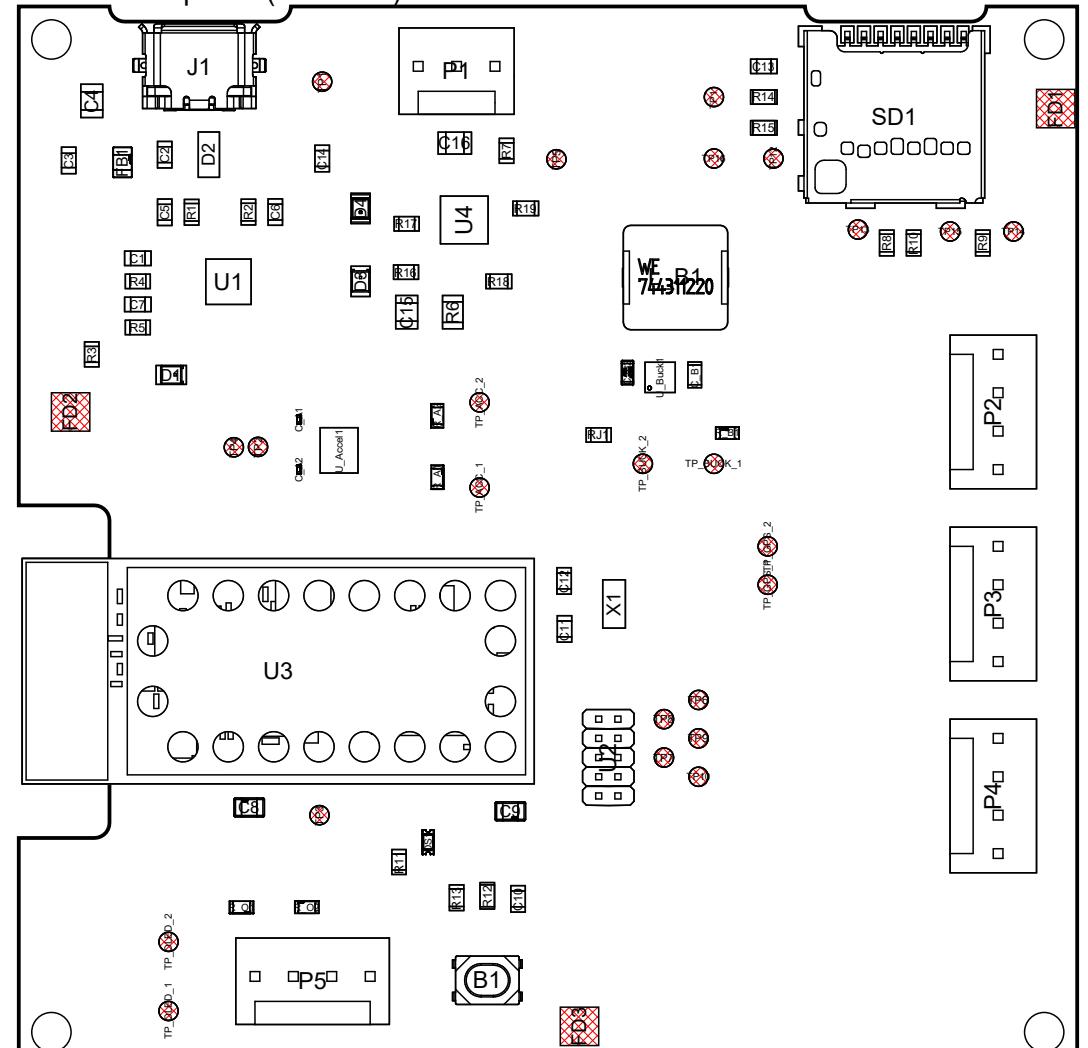
### Layer Stack Legend

Material	Layer	Thickness	Dielectric Material	Type	Gerber
Surface Material	Top Overlay			Legend	GTO
Copper	Top Solder	0.03mm	Solder Resist	Solder Mask	GTS
<b>Prepreg</b>	<b>Top Layer</b>	<b>0.04mm</b>		<b>Signal</b>	<b>GTL</b>
CF-001	GroundPlane	0.33mm	PP-006	Dielectric	
Core	CF-001	0.02mm		Signal	G1
CF-001	PowerPlane	0.71mm	Core-009	Dielectric	
Prepreg	PowerPlane	0.02mm		Signal	G2
Copper	Bottom Solder	0.33mm	PP-006	Dielectric	
Surface Material	Bottom Layer	0.04mm	Solder Resist	Signal	GBL
	Bottom Overlay	0.03mm		Solder Mask	GBS
				Legend	GBO

Total thickness: 1.53mm

REV STATUS OF SHEETS		REV				
DWG NO.: =DOC_NO_ASSY_DWG						
ZONE		REV				
REVISIONS						
DESCRIPTION						
DATE						
APPROVED						

View from Top side (Scale 2:1)



Altium  
DESIGN ITEM: PCB  
DESIGN ITEM REVISION: 1.1  
TITLE: IoTracking

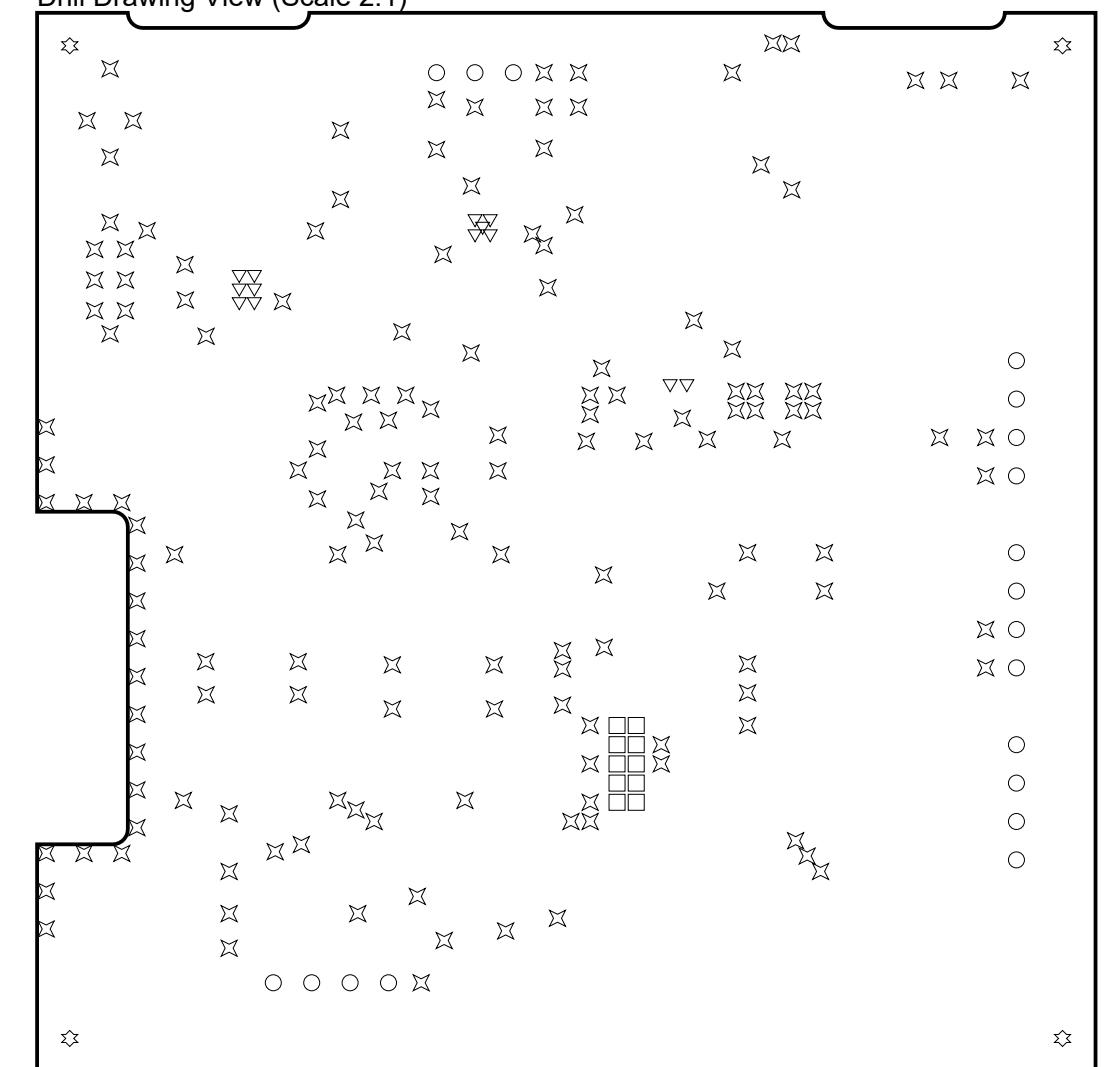
APPROVALS	DATE
ENGINEER: Weihao Huang	3/2/2022
DESIGNER: Weihao Huang	3/2/2022
CHECKER: Weihao Huang	3/2/2022
Reference Documents	
SIZE: B DWG NO:	
SCALE: FILE NAME: IoTracking_Fabrication.PCBDw	
REV: SHEET: 1 OF 12	

REV STATUS OF SHEETS				REV					DWG NO: =DOC_NO_ASSY_DWG	REV: .ltc
SHEET									ZONE	REV

Drill Table

Symbol	Count	Hole Size	Plated	Hole Tolerance
▽	13	0.20mm	Plated	
☒	156	0.20mm	Plated	
□	10	0.65mm	Plated	
○	19	1.27mm	Plated	
☆	4	2.70mm	Plated	
202 Total				

Drill Drawing View (Scale 2:1)

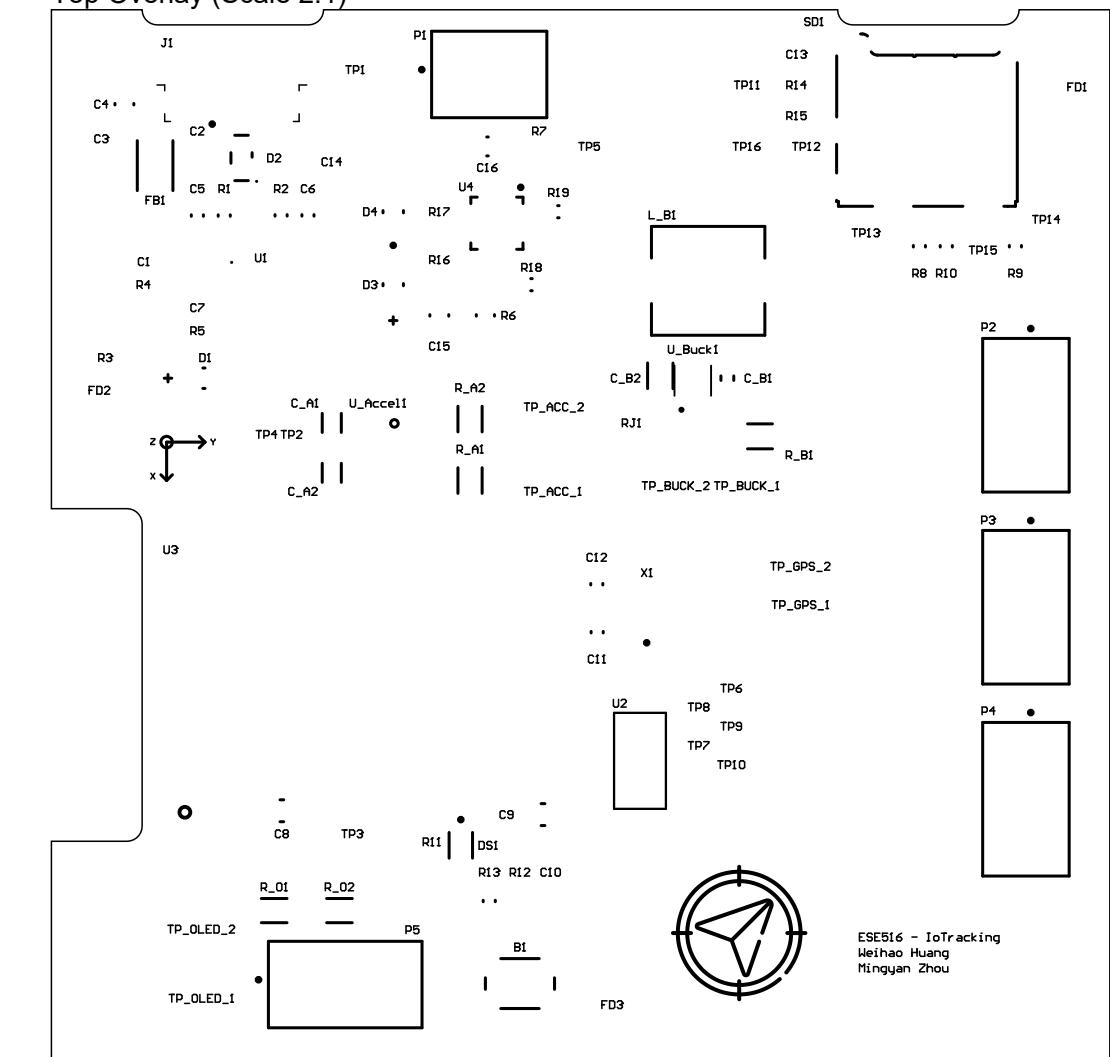


APPROVALS	DATE	<b>Altium</b> TM
ENGINEER:	Weihao Huang	
DESIGNER:	Weihao Huang	
CHECKER:	Weihao Huang	
Reference Documents		
SIZE:	B	DWG NO:
SCALE:	IoTracking	REV:
FILE NAME:	IoTracking_Board_Fabrication.PCBDw	Sheet: 2 of 12
APPLICATION		

REV STATUS OF SHEETS		REV							
SHEET									

REVISIONS		DESCRIPTION	DATE	APPROVED

Top Overlay (Scale 2:1)



APPROVALS	DATE	<b>Altium</b> TM
ENGINEER:	Weihao Huang	
DESIGNER:	Weihao Huang	
CHECKER:	Weihao Huang	
Reference Documents		
Design Item: PCB		Design Item Revision: 1.1
Title: IoTTracking		
SIZE:	DWG NO:	REV:
<b>B</b>	IoTracking_Board_Fabrication.PCBDw	
SCALE:	FILE NAME:	Sheet: 3 of 12
APPLICATION		

A

B

C

D

E

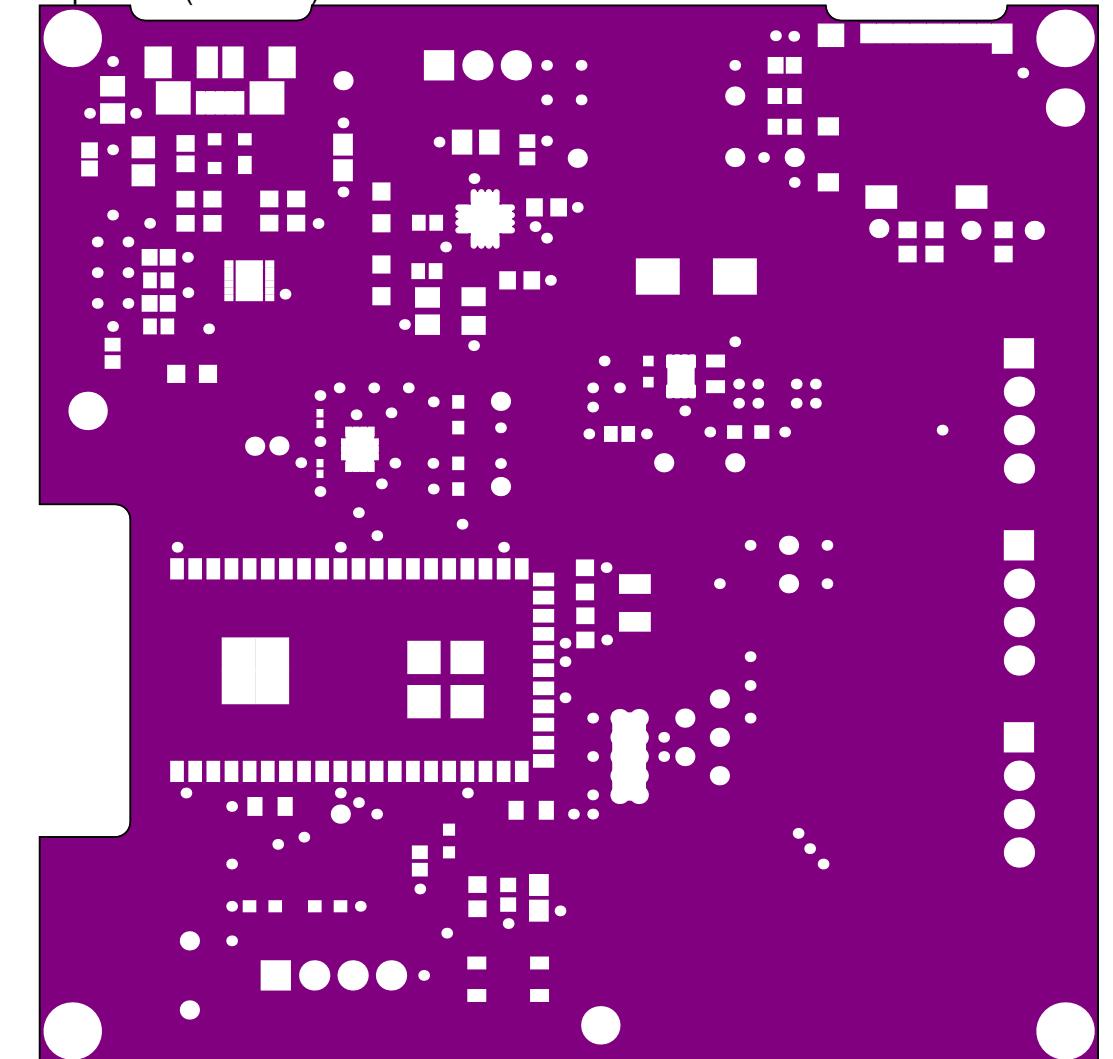
F

THIS DOCUMENT AND THE DATA DISCLOSED HEREIN OR  
HEREWITH IS THE PROPERTY OF ALTIUM LIMITED AND MAY  
BE FREELY DISTRIBUTED IN WHOLE. NO RIGHTS ARE  
RESERVED OR EXPRESS OR IMPLIED WARANTEE GIVEN.

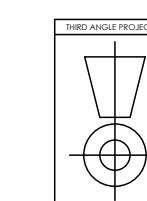
REV STATUS OF SHEETS		REV						DWG NO: =DOC_NO_ASSY_DWG	REV: .lfe
SHEET									

REVISIONS		DESCRIPTION	DATE	APPROVED

Top Solder (Scale 2:1)



APPROVALS	DATE	<b>Altium</b> TM
ENGINEER: Weihao Huang	3/2/2022	
DESIGNER: Weihao Huang	3/2/2022	
CHECKER: Weihao Huang	3/2/2022	
DESIGN ITEM: PCB	DESIGN ITEM REVISION: 1.1	
TITLE: IoTracking		
SIZE: B	DWG NO:	
REV: .lfe	FILE NAME: IoTracking_Board_Fabrication.PCBDw	
SCALE: 1:1	FILE NAME: IoTracking_Board_Fabrication.PCBDw	
Sheet: 4 of 12		



THIRD ANGLE PROJECTION

NEXT ASSY

USED ON

APPLICATION

REFERENCE DOCUMENTS

CHECKER

DESIGNER

ENGINEER

TITLE

SIZE

SCALE

REV

A

B

C

D

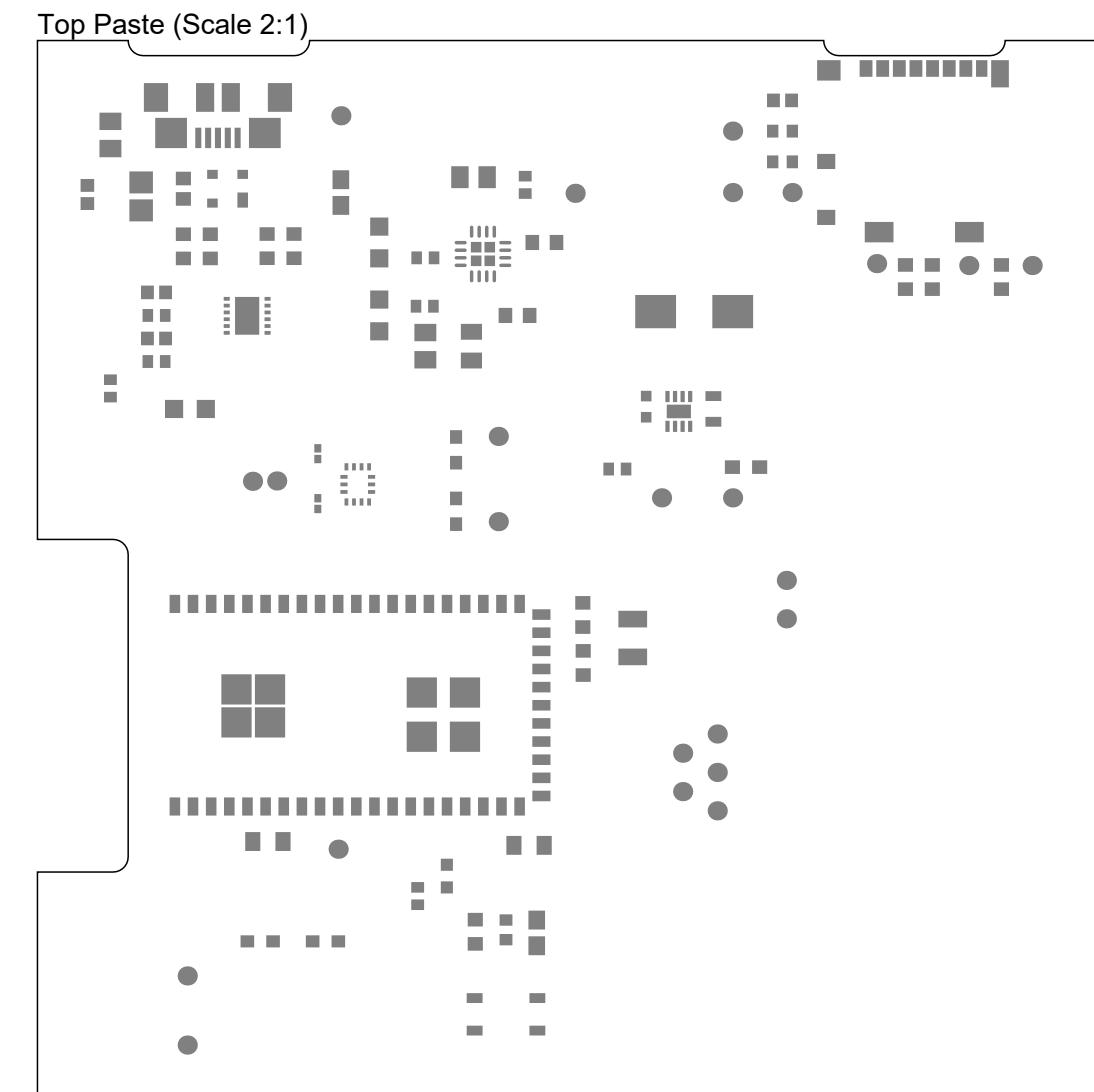
E

F

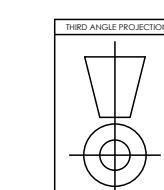
THIS DOCUMENT AND THE DATA DISCLOSED HEREIN OR  
HEREWITH IS THE PROPERTY OF ALTIUM LIMITED AND MAY  
BE FREELY DISTRIBUTED IN WHOLE. NO RIGHTS ARE  
RESERVED OR EXPRESS OR IMPLIED WARANTEE GIVEN.

REV STATUS OF SHEETS		REV						DWG NO: =DOC_NO_ASSY_DWG	REV: .lfe
SHEET									

REVISIONS		DESCRIPTION	DATE	APPROVED



APPROVALS	DATE	<b>Altium</b> TM
ENGINEER: Weihao Huang	3/2/2022	
DESIGNER: Weihao Huang	3/2/2022	
CHECKER: Weihao Huang	3/2/2022	
DESIGN ITEM: PCB	DESIGN ITEM REVISION: 1.1	
TITLE: IoTracking		
SIZE: B	DWG NO:	
REV: .lfe	FILE NAME: IoTracking_Board_Fabrication.PCBDw	
SCALE: 1:1	FILE NAME: IoTracking_Board_Fabrication.PCBDw	
Sheet: 5 of 12		



A

B

C

D

E

F

A

B

C

D

E

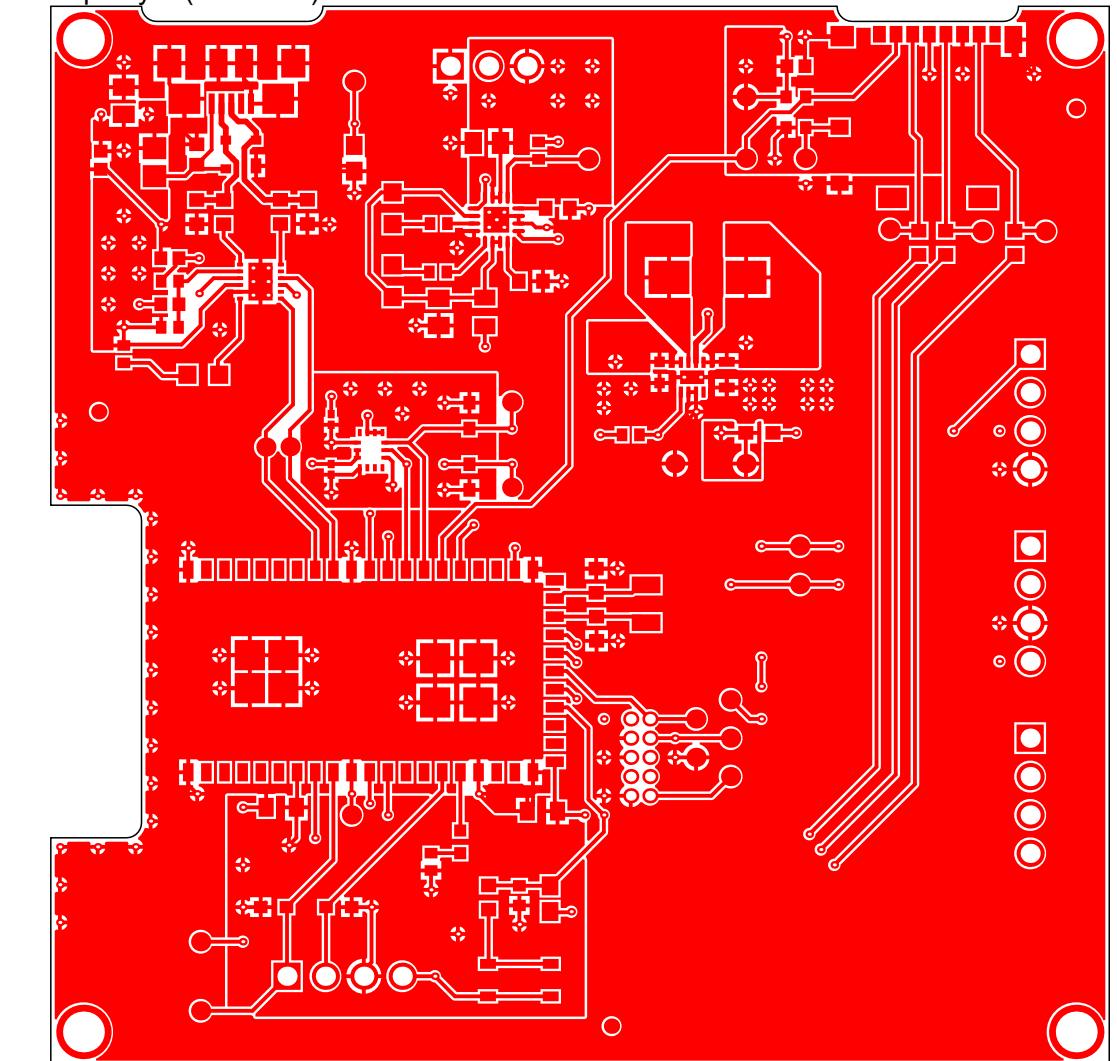
F

THIS DOCUMENT AND THE DATA DISCLOSED HEREIN OR  
HEREWITH IS THE PROPERTY OF ALTIUM LIMITED AND MAY  
BE FREELY DISTRIBUTED IN WHOLE. NO RIGHTS ARE  
RESERVED OR EXPRESS OR IMPLIED WARANTEE GIVEN.

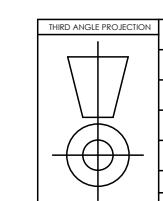
REV STATUS OF SHEETS		REV					DWG NO: =DOC_NO_ASSY_DWG	REV: .lfe
SHEET								

REVISIONS		DESCRIPTION	DATE	APPROVED

Top Layer (Scale 2:1)



APPROVALS	DATE	<b>Altium</b> TM
ENGINEER: Weihao Huang	3/2/2022	
DESIGNER: Weihao Huang	3/2/2022	
CHECKER: Weihao Huang	3/2/2022	
Reference Documents		DESIGN ITEM: PCB
		DESIGN ITEM REVISION: 1.1
		TITLE: IoTracking
		SIZE: B
		DWG NO:
		IoTracking_Board_Fabrication.PCBDw
SCALE:	FILE NAME:	REV:



A

B

C

D

E

F

A

B

C

D

E

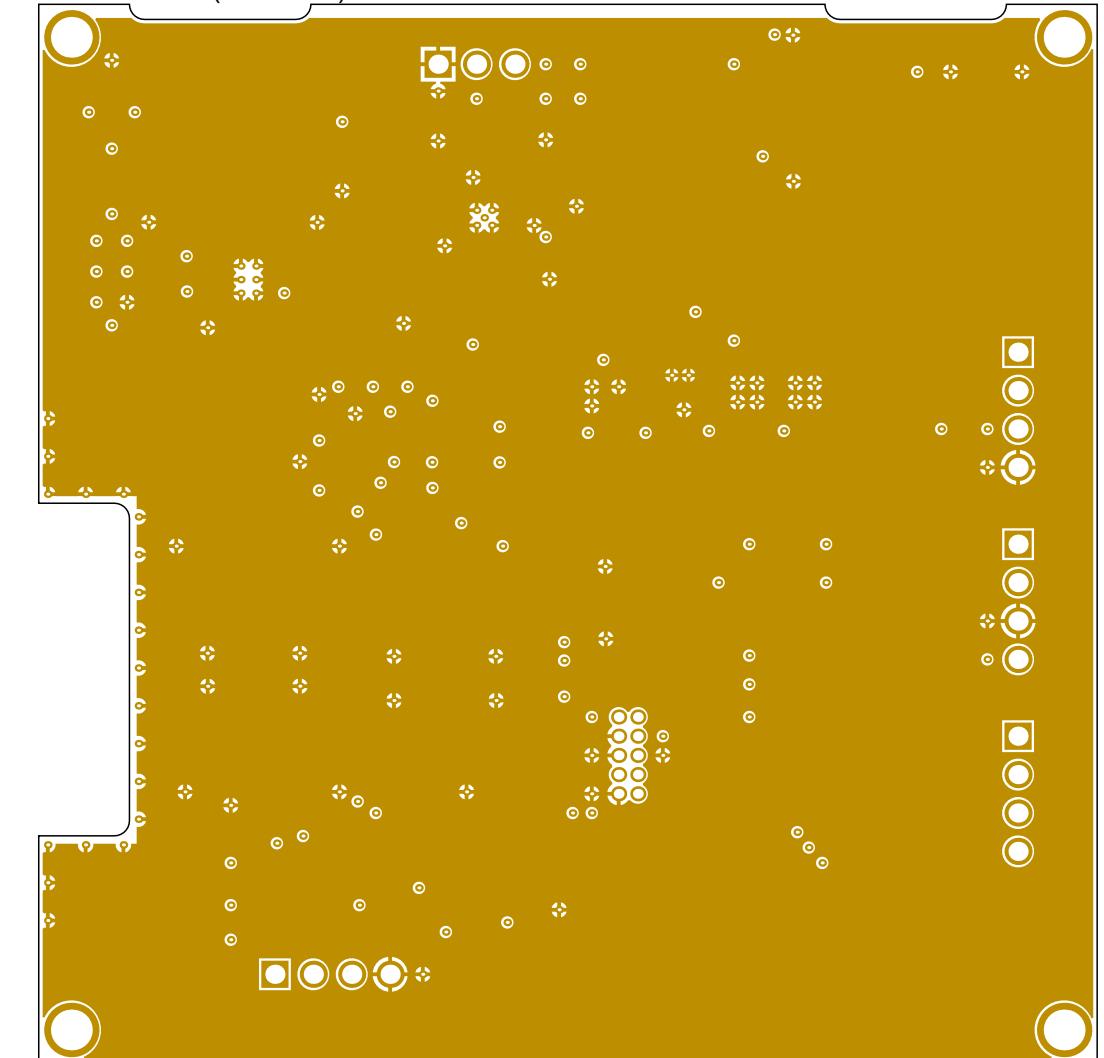
F

THIS DOCUMENT AND THE DATA DISCLOSED HEREIN OR  
HEREWITH IS THE PROPERTY OF ALTIUM LIMITED AND MAY  
BE FREELY DISTRIBUTED IN WHOLE. NO RIGHTS ARE  
RESERVED OR EXPRESS OR IMPLIED WARANTEE GIVEN.

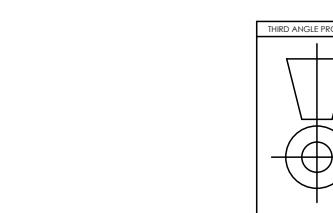
DWG NO: =DOC_NO_ASSY_DWG	REV: .lfe

REVISIONS		
DESCRIPTION	DATE	APPROVED

GroundPlane (Scale 2:1)



APPROVALS		DATE	DESIGN ITEM: PCB	DESIGN ITEM REVISION: 1.1
ENGINEER:	Weihao Huang	3/2/2022		
DESIGNER:	Weihao Huang	3/2/2022		
CHECKER:	Weihao Huang	3/2/2022		
Reference Documents			TITLE: IoTracking	
SIZE:	B	DWG NO:		
SCALE:	IoTracking_Board_Fabrication.PCBDw	FILE NAME:		
REV:				

**Altium**DWG NO:  
=DOC\_NO\_ASSY\_.lfe

SHEET: 7 OF 12

A

B

C

D

E

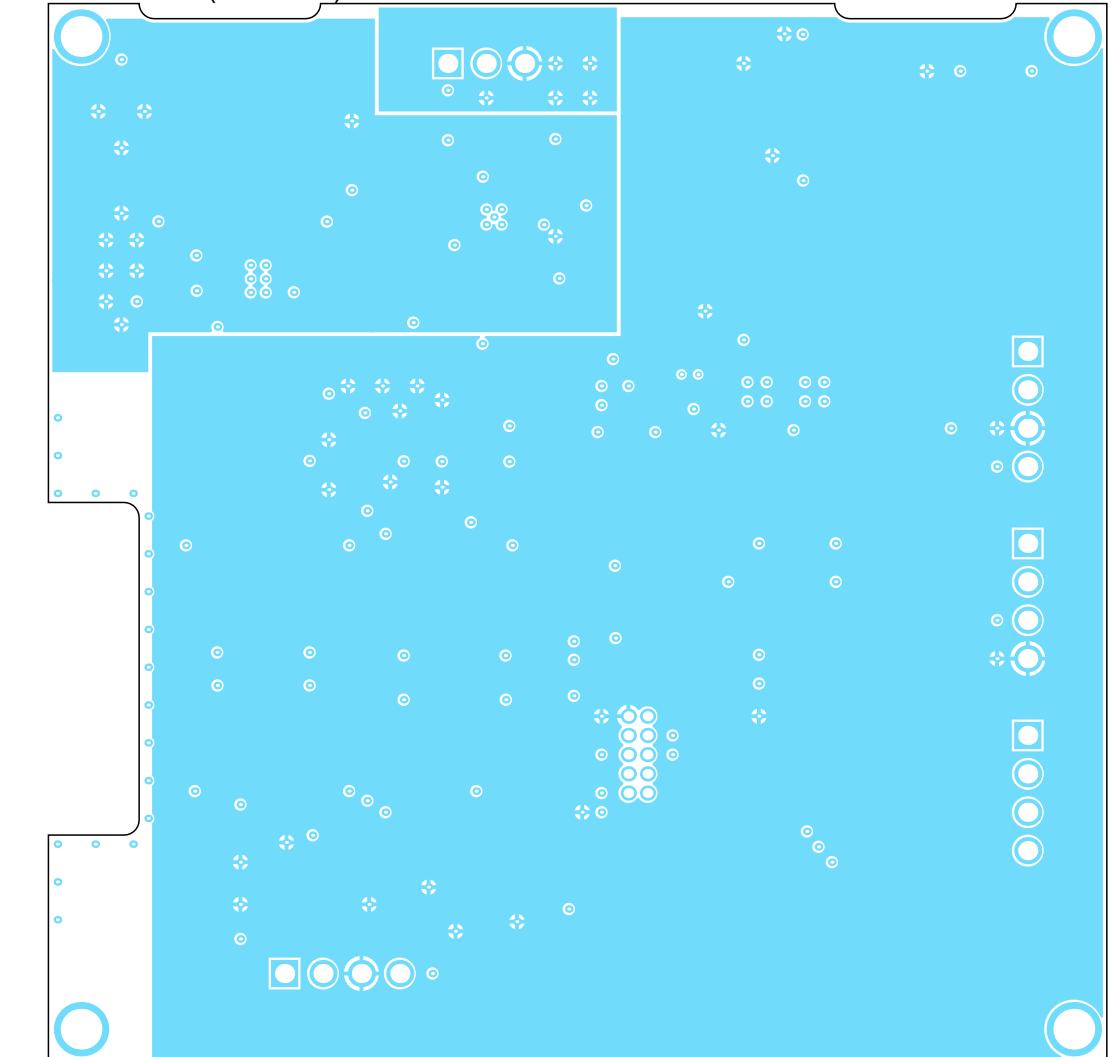
F

THIS DOCUMENT AND THE DATA DISCLOSED HEREIN OR  
HEREWITH IS THE PROPERTY OF ALTIUM LIMITED AND MAY  
BE FREELY DISTRIBUTED IN WHOLE. NO RIGHTS ARE  
RESERVED OR EXPRESS OR IMPLIED WARANTEE GIVEN.

REV STATUS OF SHEETS		REV									
SHEET											

REVISIONS		REV:									
ZONE	REV	DESCRIPTION	DATE	APPROVED							

PowerPlane (Scale 2:1)



APPROVALS	DATE	<b>Altium</b> DESIGN ITEM: PCB TITLE: IoTracking SIZE: B DWG NO: IoTracking_Fabrication.PCDBdw FILE NAME: IoTracking_Fabrication.PCDBdw SCALE: 1:1 REV: 1.1
ENGINEER: Weihao Huang	3/2/2022	
DESIGNER: Weihao Huang	3/2/2022	
CHECKER: Weihao Huang	3/2/2022	
THIRD ANGLE PROJECTION	Reference Documents	
NEXT ASSY	USED ON	
APPLICATION		
SCALE:	FILE NAME:	

1

1

2

2

3

3

4

4

A

B

C

D

E

F

.lt

DWG NO: =DOC\_NO\_ASSY\_.dwg

8 OF 12

A

B

C

D

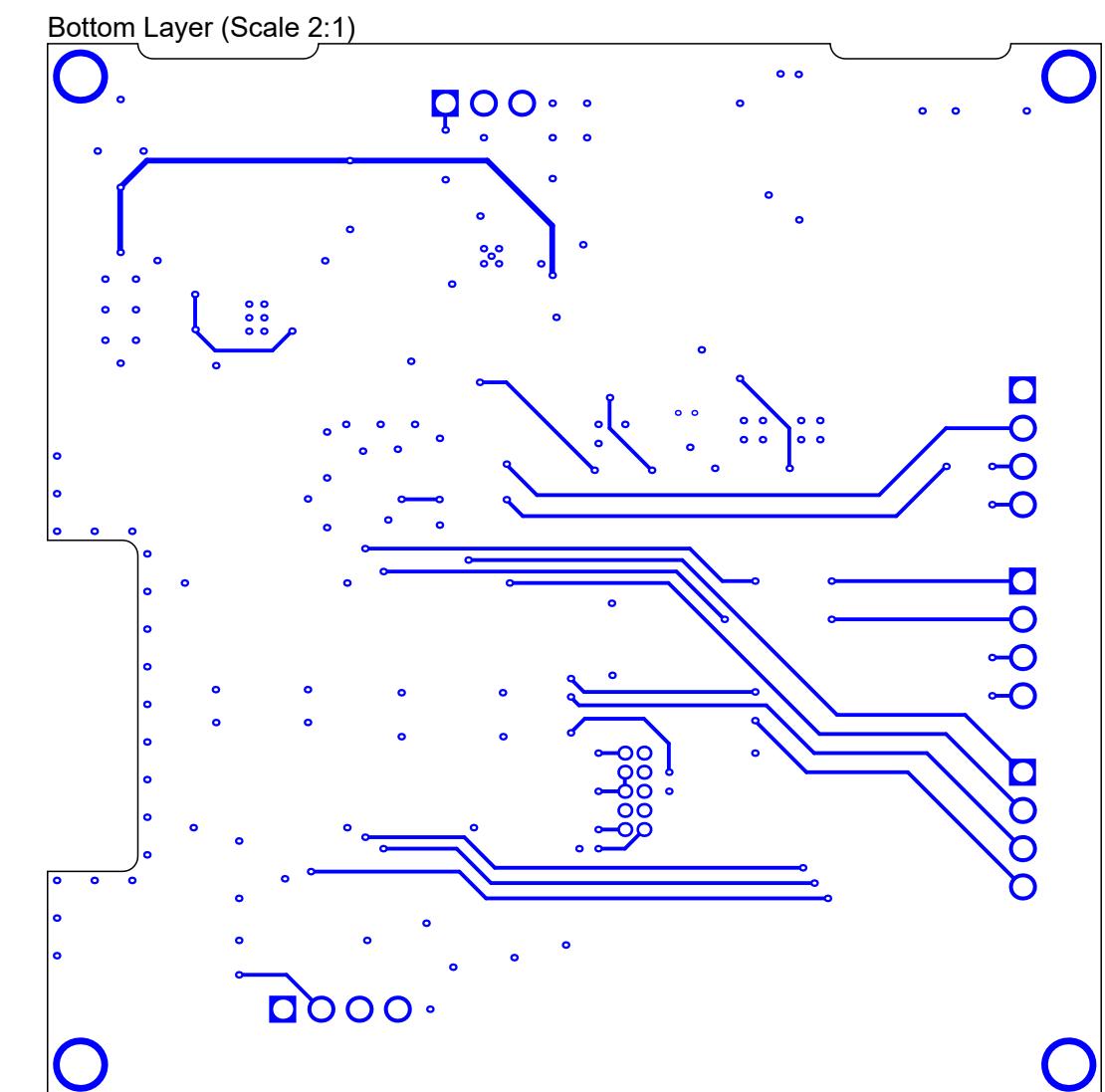
E

F

THIS DOCUMENT AND THE DATA DISCLOSED HEREIN OR  
HEREWITH IS THE PROPERTY OF ALTIUM LIMITED AND MAY  
BE FREELY DISTRIBUTED IN WHOLE. NO RIGHTS ARE  
RESERVED OR EXPRESS OR IMPLIED WARANTEE GIVEN.

REV STATUS OF SHEETS		REV						DWG NO. =DOC_NO_ASSY_DWG	REV .lfe
SHEET									

REVISIONS		DESCRIPTION	DATE	APPROVED



APPROVALS	DATE	<b>Altium</b> TM
ENGINEER: Weihao Huang	3/2/2022	
DESIGNER: Weihao Huang	3/2/2022	
CHECKER: Weihao Huang	3/2/2022	
Reference Documents		
DESIGN ITEM: PCB		DESIGN ITEM REVISION: 1.1
TITLE: IoTTracking		
SIZE: B	DWG NO:	REV:
IoTracking Board Fabrication.PCBDw		
SCALE:	FILE NAME:	9 OF 12

THIRD ANGLE PROJECTION

NEXT ASSY USED ON APPLICATION

A

B

C

D

E

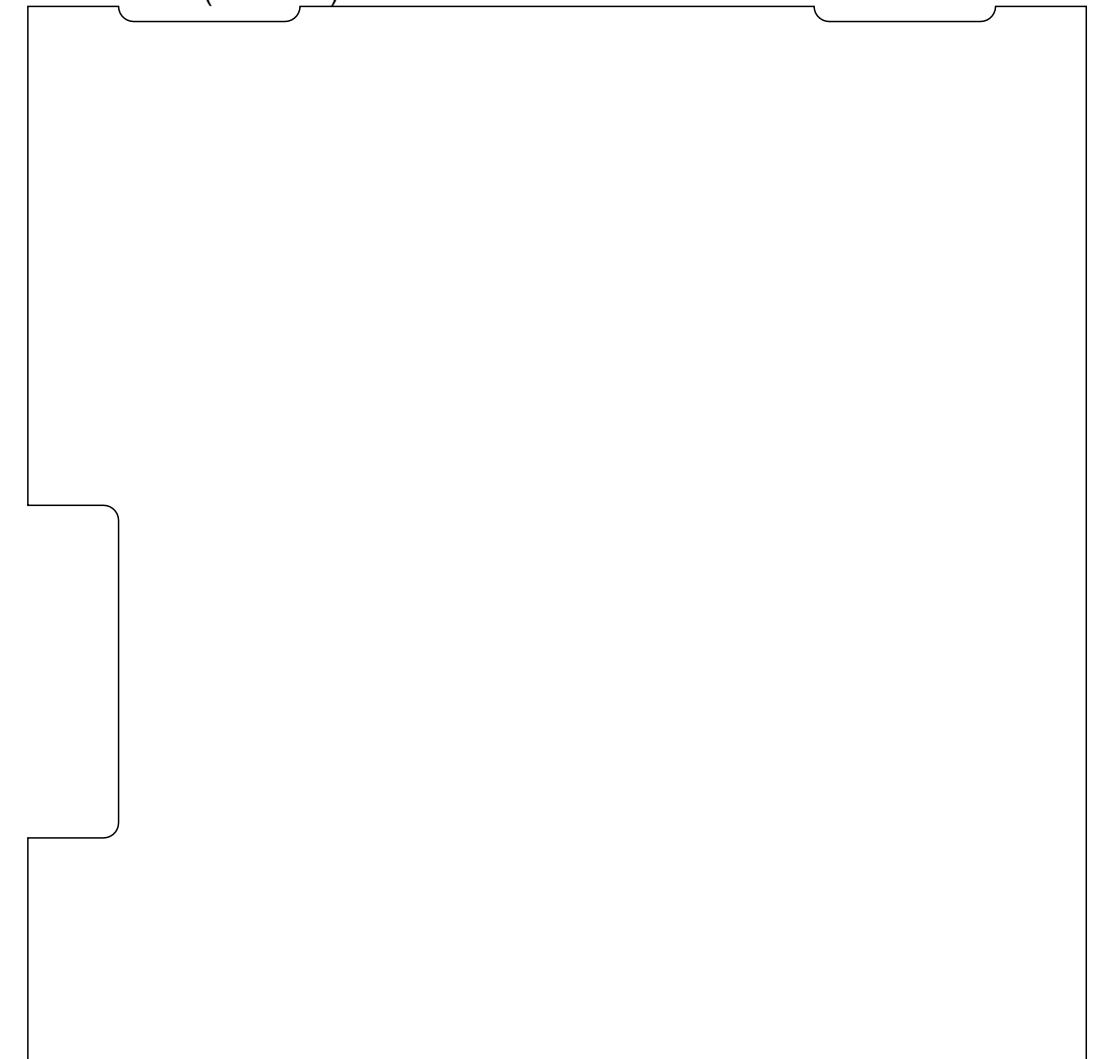
F

THIS DOCUMENT AND THE DATA DISCLOSED HEREIN OR  
HEREWITH IS THE PROPERTY OF ALTIUM LIMITED AND MAY  
BE FREELY DISTRIBUTED IN WHOLE. NO RIGHTS ARE  
RESERVED OR EXPRESS OR IMPLIED WARANTEE GIVEN.

DWG NO: =DOC_NO_ASSY_DWG		REV: .lfe
REV STATUS OF SHEETS	REV	
SHEET		

REVISIONS		
DESCRIPTION	DATE	APPROVED

Bottom Paste (Scale 2:1)



1

2

3

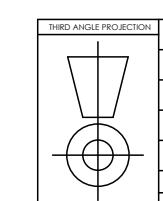
4

.lt

DWG NO:  
=DOC\_NO\_ASSY\_

.lfe

APPROVALS	DATE	<b>Altium</b> TM
ENGINEER:	Weihao Huang	
DESIGNER:	Weihao Huang	
CHECKER:	Weihao Huang	
Reference Documents		DESIGN ITEM: PCB
		DESIGN ITEM REVISION: 1.1
		TITLE: IoTracking
		SIZE: B
		DWG NO:
		REV:
		IoTracking_Board_Fabrication.PCBDw
SCALE:	FILE NAME:	
		Sheet: 10 OF 12



NEXT ASSY

USED ON

APPLICATION

APPROVALS DATE  
ENGINEER: Weihao Huang 3/2/2022  
DESIGNER: Weihao Huang 3/2/2022  
CHECKER: Weihao Huang 3/2/2022

Reference Documents  
DESIGN ITEM: PCB  
DESIGN ITEM REVISION: 1.1  
TITLE: IoTracking

SIZE: B  
DWG NO:  
REV:  
IoTracking\_Board\_Fabrication.PCBDw

SCALE: FILE NAME:  
Sheet: 10 OF 12

A

B

C

D

E

F

A

B

C

D

E

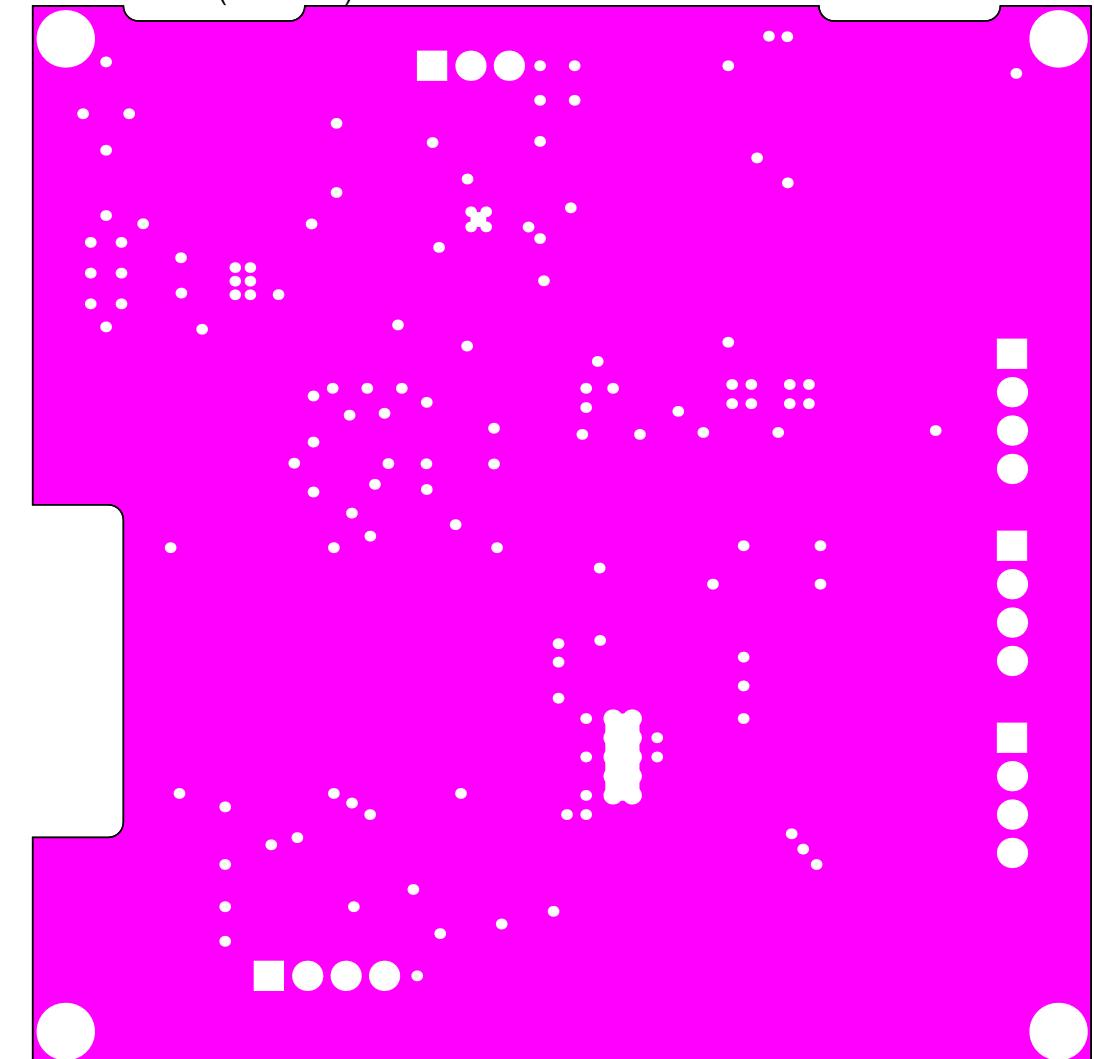
F

THIS DOCUMENT AND THE DATA DISCLOSED HEREIN OR  
HEREWITH IS THE PROPERTY OF ALTIUM LIMITED AND MAY  
BE FREELY DISTRIBUTED IN WHOLE. NO RIGHTS ARE  
RESERVED OR EXPRESS OR IMPLIED WARANTEE GIVEN.

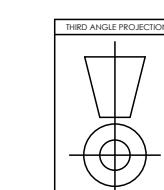
DWG NO. =DOC_NO_ASSY_DWG	REV. .lfe				
REV STATUS OF SHEETS	REV				
SHEET					

REVISIONS		DESCRIPTION	DATE	APPROVED

Bottom Solder (Scale 2:1)



APPROVALS	DATE	<b>Altium</b> TM
ENGINEER: Weihao Huang	3/2/2022	
DESIGNER: Weihao Huang	3/2/2022	
CHECKER: Weihao Huang	3/2/2022	
DESIGN ITEM: PCB	DESIGN ITEM REVISION: 1.1	
TITLE: IoTracking		
SIZE: <b>B</b>	DWG NO:	
REV:		
NEXT ASSY	USED ON	
APPLICATION		
SCALE:	FILE NAME: IoTracking_Board_Fabrication.PCBDw	Sheet: 11 of 12



A

B

C

D

E

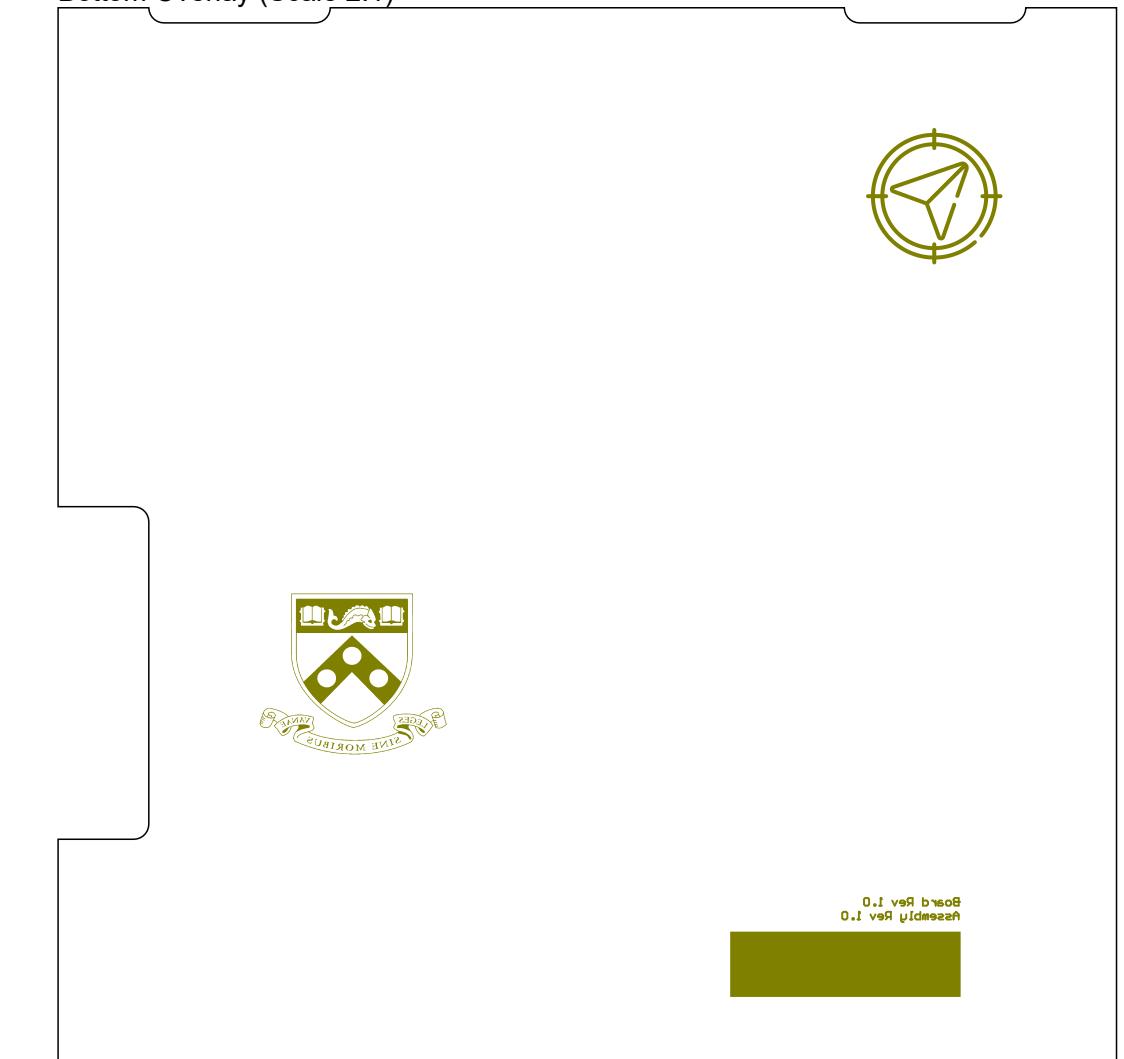
F

THIS DOCUMENT AND THE DATA DISCLOSED HEREIN OR  
HEREWITH IS THE PROPERTY OF ALTIUM LIMITED AND MAY  
BE FREELY DISTRIBUTED IN WHOLE. NO RIGHTS ARE  
RESERVED OR EXPRESS OR IMPLIED WARANTEE GIVEN.

REV STATUS OF SHEETS		REV							DWG NO: =DOC_NO_ASSY_DWG	REV: .lfe
SHEET										

REVISIONS		DESCRIPTION	DATE	APPROVED

Bottom Overlay (Scale 2:1)



APPROVALS	DATE	<b>Altium</b> TM
ENGINEER:	Weihao Huang	
DESIGNER:	Weihao Huang	
CHECKER:	Weihao Huang	
Reference Documents		
SIZE:	DWG NO:	
<b>B</b>		
IoTracking		
SCALE:	FILE NAME:	
IoTracking_Board_Fabrication.PCBDw		
Sheet: 12 of 12		

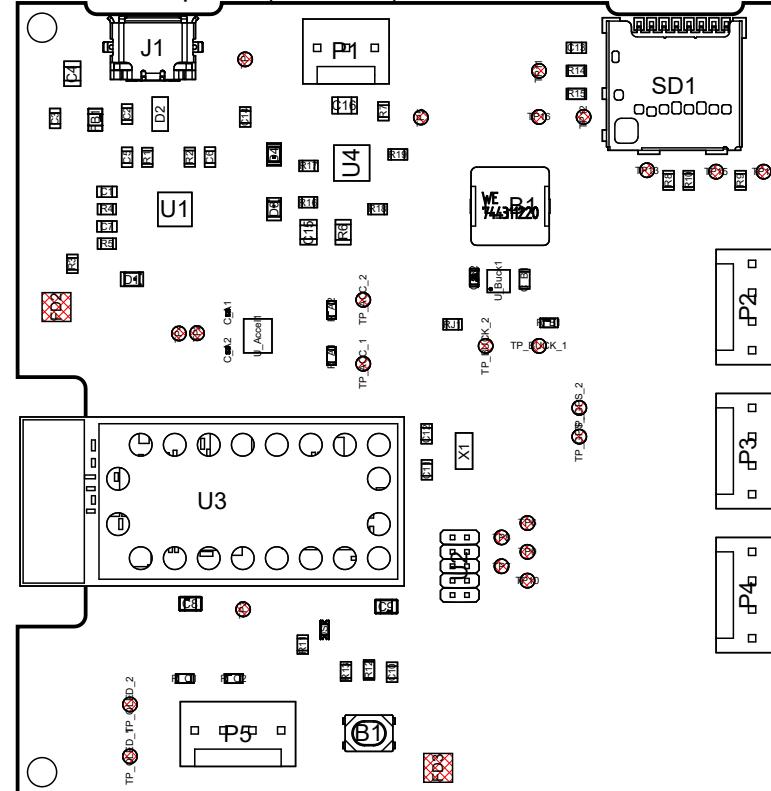
THIRD ANGLE PROJECTION

NEXT ASSY	USED ON
APPLICATION	

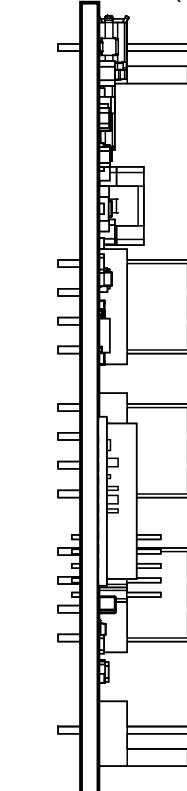
## **NOTES (unless otherwise specified)**

1. This item is electrostatic sensitive and shall be handled accordingly

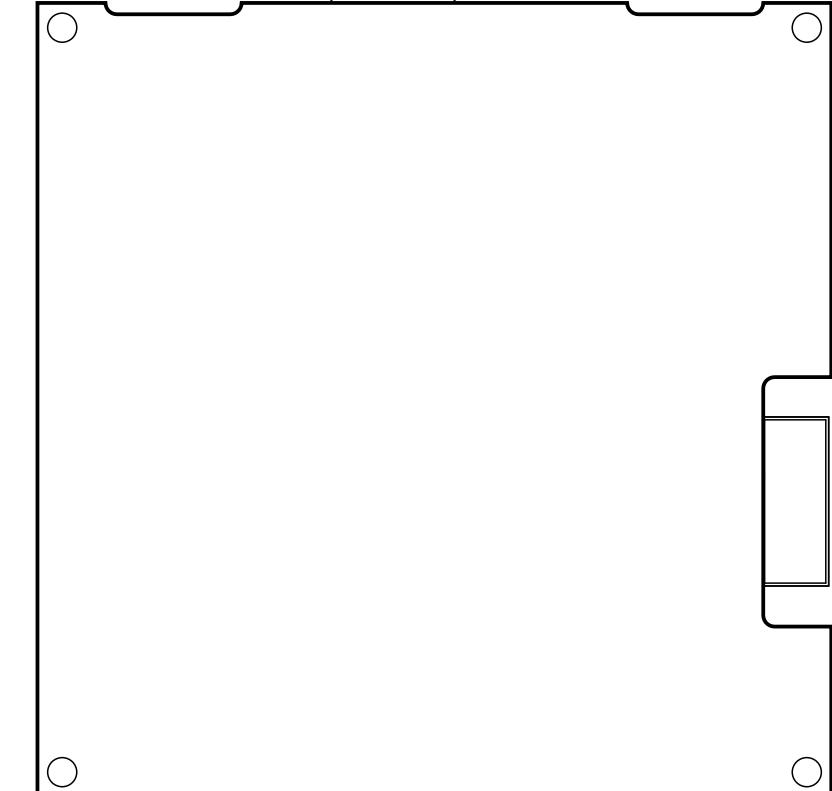
View from Top side (Scale 3:2)



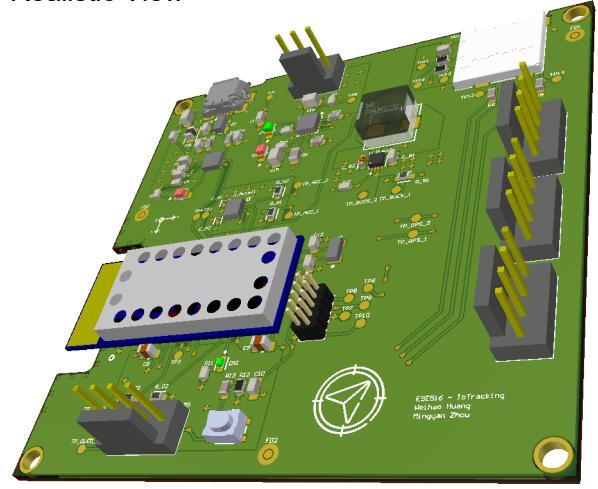
View from Left side (Scale 3:)



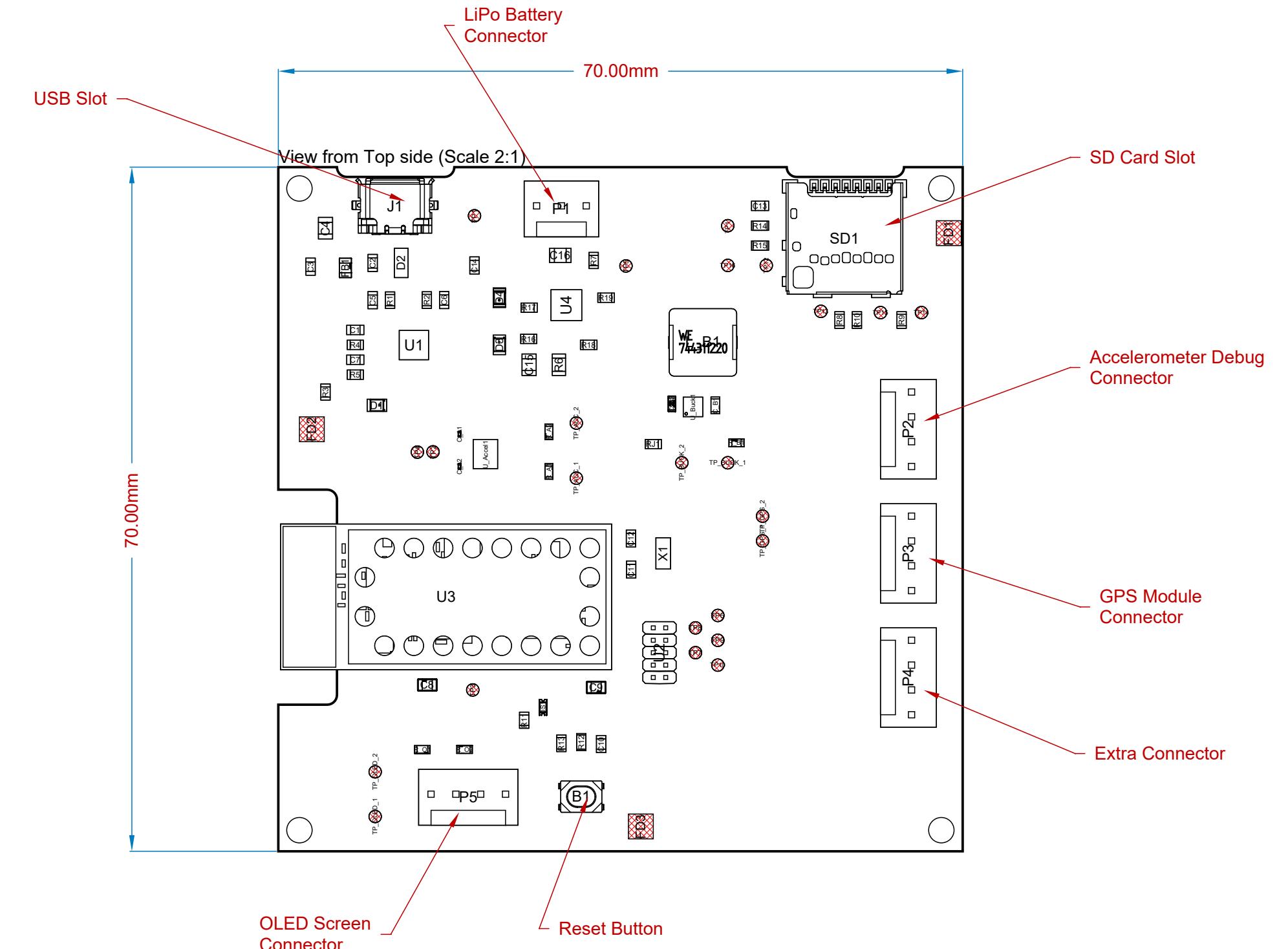
View from Bottom side (Scale 3:2)



## Realistic View



		APPROVALS	DATE							
ENGINEER:		Weihao Huang	2/26/2022							
DESIGNER:		Weihao Huang	2/26/2022							
CHECKER:		Weihao Huang	2/26/2022	DESIGN ITEM: PCB Board Assembly		DESIGN ITEM REVISION: 1.0				
		Reference Documents		TITLE: IoTTracking						
					<b>B</b>	SIZE: B		DWG NO:		
NEXT ASSY		USED ON		SCALE:	FILE NAME: IoTTracking_Board_Assembly.PCBDwf	SHEET: 1 OF 4				
APPLICATION										



APPROVALS		DATE	DESIGN ITEM: PCB Board Assembly	DESIGN ITEM REVISION: 1.0	
ENGINEER:	Weihao Huang	2/26/2022			
DESIGNER:	Weihao Huang	2/26/2022	CHECKER:	Weihao Huang	2/26/2022
REFERENCE DOCUMENTS					
THIRD ANGLE PROJECTION					
NEXT ASSY	USED ON				
APPLICATION					
SIZE: B	DWG NO:			REV: .lfe	
SCALE:	FILE NAME: IoTracking_Board_Assembly.PCBDwf				
SHEET: 2 OF 4					

**Altium**

A

B

C

D

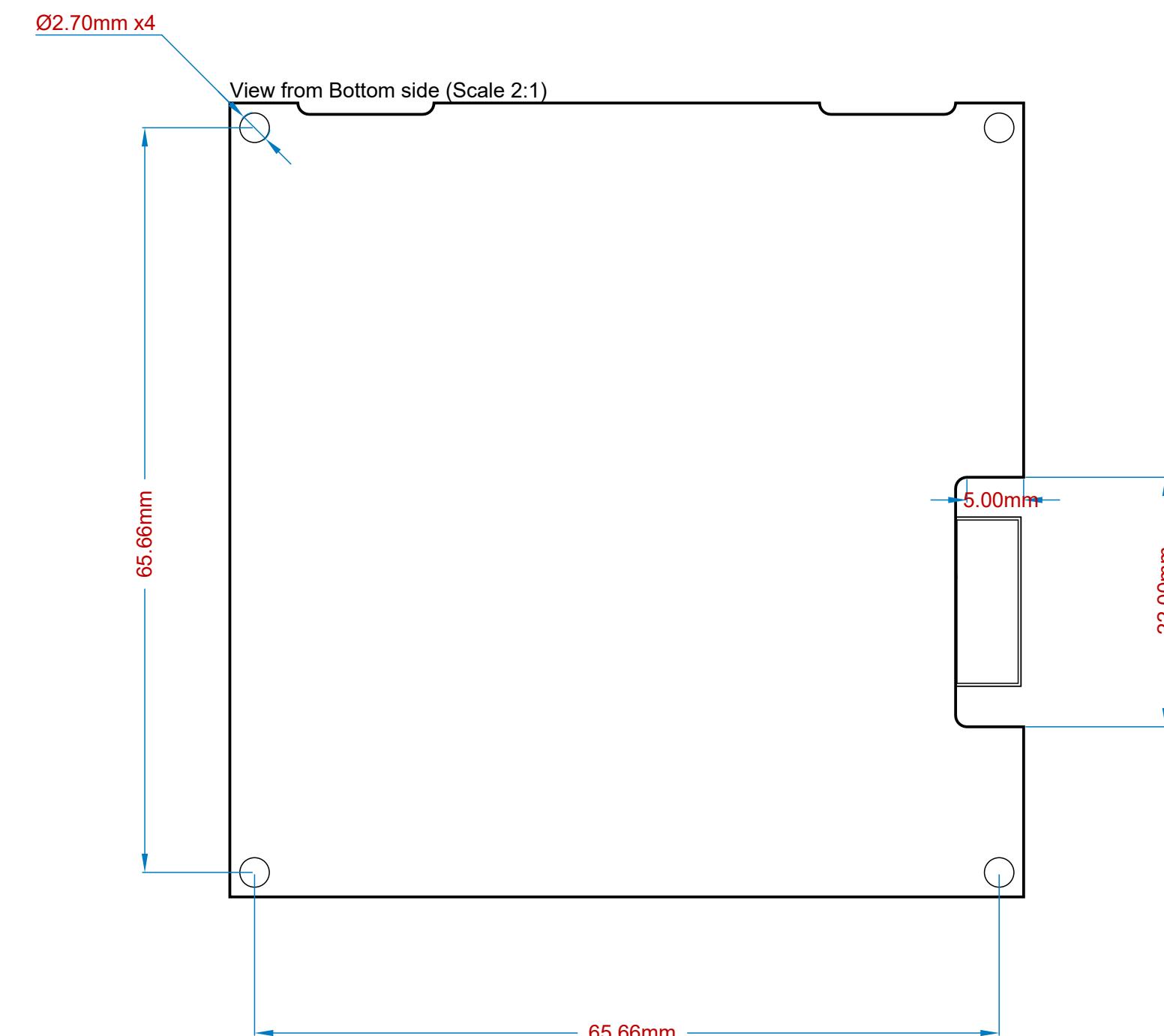
E

F

THIS DOCUMENT AND THE DATA DISCLOSED HEREIN OR  
HEREWITH IS THE PROPERTY OF ALTIUM LIMITED AND MAY  
BE FREELY DISTRIBUTED IN WHOLE. NO RIGHTS ARE  
RESERVED OR EXPRESS OR IMPLIED WARANTEE GIVEN.

REV STATUS OF SHEETS		REV							DWG NO: =DOC_NO_ASSY_DWG	REV: .lfe
SHEET										

REVISIONS		DESCRIPTION	DATE	APPROVED



APPROVALS	DATE	<b>Altium</b> PCB Board Assembly 1.0
ENGINEER: Weihao Huang	2/26/2022	
DESIGNER: Weihao Huang	2/26/2022	
CHECKER: Weihao Huang	2/26/2022	
Reference Documents		
THIRD ANGLE PROJECTION		
NEXT ASSY	USED ON	
APPLICATION		
SIZE: B	DWG NO:	
SCALE:	FILE NAME: IoTracking_Board_Assembly.PCBDwf	REV:

Bill Of Materials

Line #	Designator	Name	Quantity
1	B1	PTS810 SJK 250 SMTR LFS	1
2	Battery1	LiPo Battery	1
3	C1, C3, C7, C13	VJ0603Y104KXJCW1BC	4
4	C2	C0603C103K4RACTU	1
5	C4, C15, C16	CAP 4.7uF 16V 0805(2012)	3
6	C5, C6	CAP 47pF 16V 0603(1608)	2
7	C8, C9	0805YD106KAT2A	2
8	C10, C14	0603YC105JAT2A	2
9	C11, C12	CAP 18pF 16V 0603(1608)	2
10	C_A1, C_A2	GRM033C80J104ME15D	2
11	C_B1	C1608X5R0J226M080AC	1
12	C_B2	C1608X5R1C106M080AB	1
13	D1, D3	LTST-C170CKT	2
14	D2	PRTR5V0U2X,215	1
15	D4	LTST-C170GKT	1
16	DS1	LTST-C191KGKT	1
17	FB1	BLM21PG221SN1D	1
18	GPS_Module1	GPS 13740	1
19	J1	ZX62R-B-5P	1
20	L_B1	744311100	1
21	LCD1	OLED LCD Screen	1
22	P1	640456-3	1
23	P2, P3, P4, P5	640456-4	4
24	R1, R2, R8, R9, R10	27R 1% 0603(1608)	5
25	R3, R5, R7, R11, R16, R17	CRCW06031K00FKEB	6
26	R4, RJ1	CRCW06030000Z0EC	2
27	R6	Jumper 0805(2012)	1
28	R12, R14, R15	ERJ3EKF1002V	3
29	R13	100R 1% 0603(1608)	1
30	R18, R19	1K13 1% 0603(1608)	2
31	R_A1, R_A2, R_O1, R_O2	AT0603DRD074K7L	4
32	R_B1	CPF0603B180KE	1
33	SD1	104031-0811	1
34	U1	FT234XD-R	1
35	U2	20021111-00010T4LF	1
36	U3	SAMW25H18-MR510PB	1
37	U4	BQ24075RGTRG4	1
38	U_Accel1	6 DoF Accelerometer	1
39	U_Buck1	TPS62082DSGR	1
22	X1	ABS07-32.768kHz-T	1

REV STATUS OF SHEETS		REV	DWG NO. =DOC_NO_ASSY_DWG		REV	REVISIONS				
SHEET						ZONE	REV	DESCRIPTION	DATE	APPROVED

APPROVALS		DATE	
ENGINEER:	Weihao Huang	2/26/2022	
DESIGNER:	Weihao Huang	2/26/2022	
CHECKER:	Weihao Huang	2/26/2022	
Reference Documents		DESIGN ITEM: PCB_Board Assembly DESIGN ITEM REVISION: 1.0	
NEXT ASSY		USED ON	TITLE: IoTracking
APPLICATION			SIZE: B DWG NO:
SCALE:	FILE NAME: IoTracking_Board_Assembly.PCBDwf	REV:	4 OF 4