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REVISION	DESCRIPTION	DATE	APPROVED

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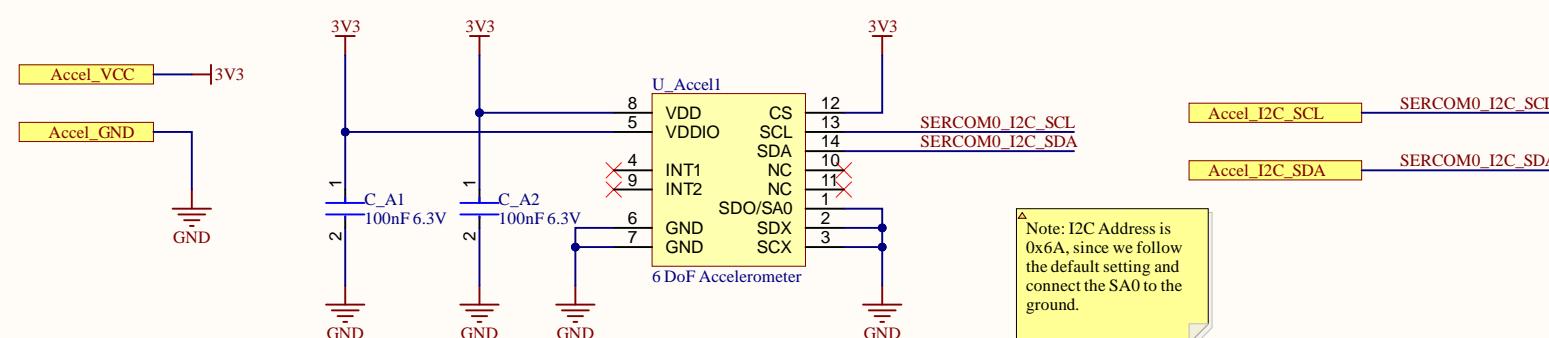
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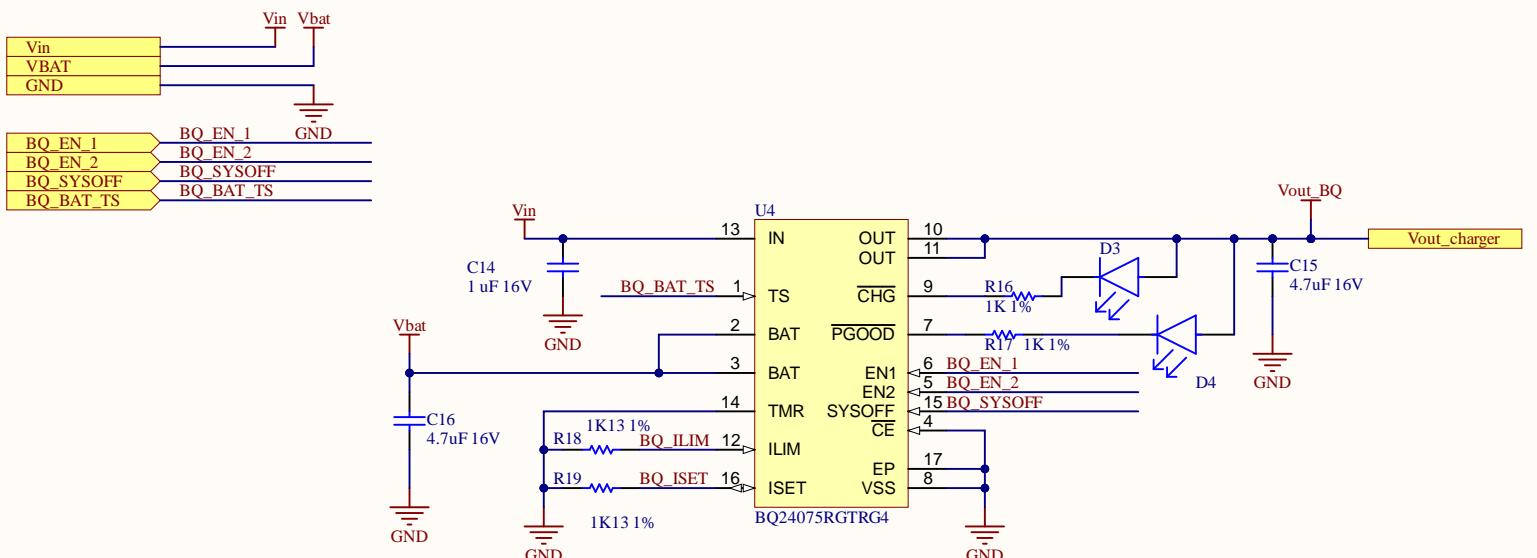
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APPROVALS	DATE	PROJECT	Penn Engineering	*
ENG: *		UNIVERSITY OF PENNSYLVANIA	*	*
DSN: *		PROJECT REVISION:	DOCUMENT REVISION:	DESIGN ITEM:
CHK: *		TITLE		
REFERENCE DOCUMENTS		Accelerometer		
BOM:				
ASSY DWG:		SIZE	CAGE CODE	DWG NO.
FAB DWG:		B		REV 1.0
PCB DWG:		SCALE:	FILE NAME Accelerometer.SchDoc	SHEET 1 OF 1

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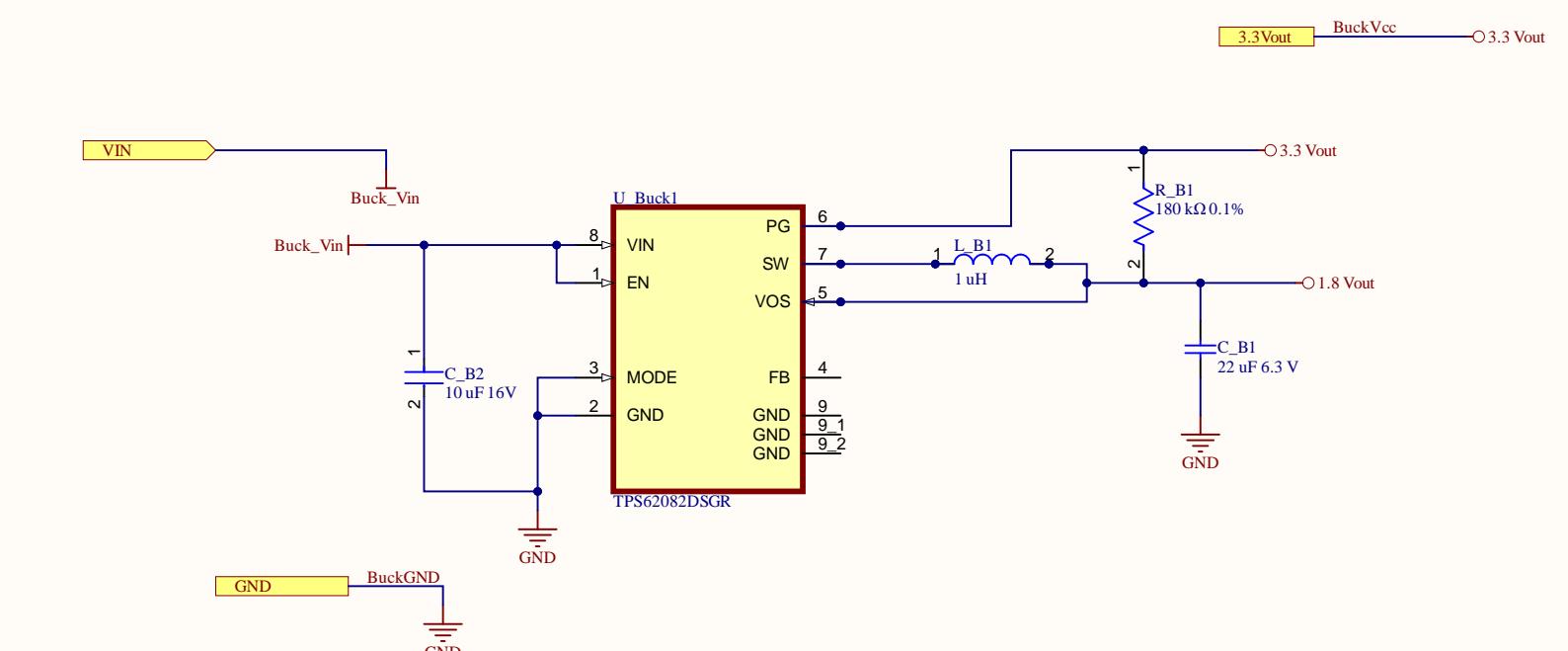
REVISION	DESCRIPTION	DATE	APPROVED



APPROVALS	DATE	PROJECT	Penn Engineering
ENG:	*	UNIVERSITY OF PENNSYLVANIA	*
DSN:	*	PROJECT REVISION:	DOCUMENT REVISION:
CHK:	*	DESIGN ITEM:	
REFERENCE DOCUMENTS		TITLE	
BOM:	LiPo Charger		
ASSY DWG:	SIZE	CAGE CODE	DWG NO.
FAB DWG:	B		
PCB DWG:	SCALE:	FILE NAME	LiPo_Charger.SchDoc
		SHEET	1 OF 1

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DSN:	*	PROJECT REVISION:	DOCUMENT REVISION:	DESIGN ITEM:
CHK:	*	TITLE		
REFERENCE DOCUMENTS				
BOM:				
ASSY DWG:				
FAB DWG:				
PCB DWG:				
SIZE	CAGE CODE	DWG NO.		REV
B				1.0
SCALE:	FILE NAME BuckConverter.SchDoc			SHEET 1 OF 1

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DWG. NO.	REV. SHT.	1.0.1	REVISION	DESCRIPTION	DATE	APPROVED

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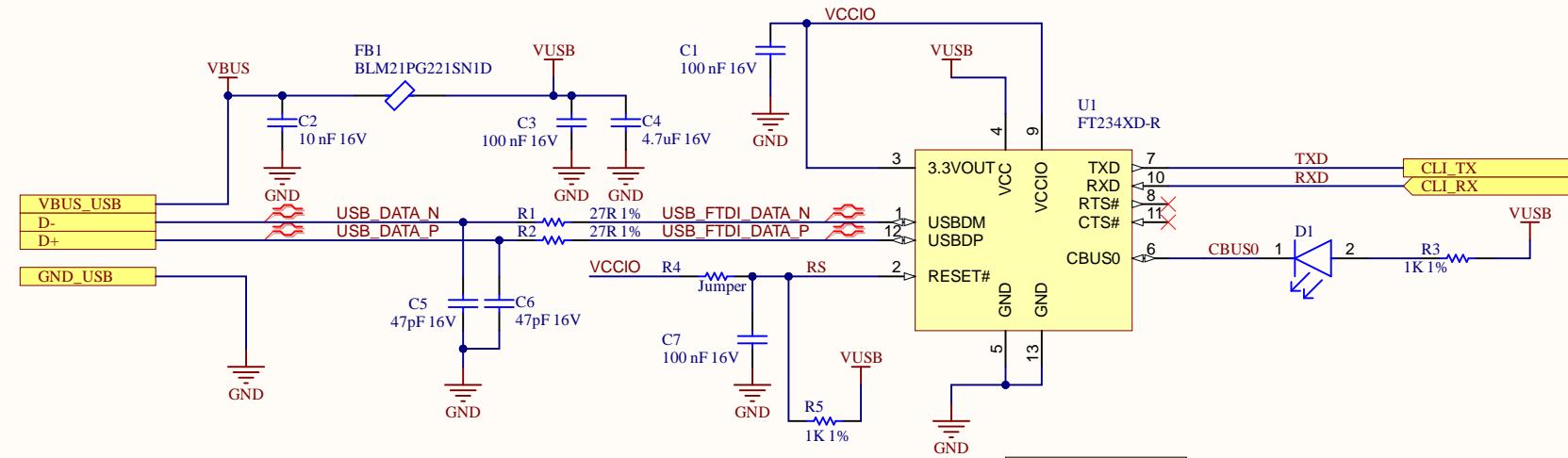
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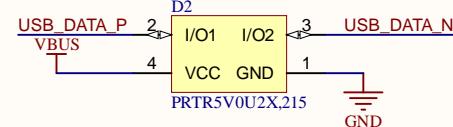
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FTDI CHIP



USB ESD PROTECTION



APPROVALS	DATE	PROJECT	Penn Engineering	
ENG:	*	DSN:	*	
CHK:	*	PROJECT REVISION:	DOCUMENT REVISION:	DESIGN ITEM:
REFERENCE DOCUMENTS				
BOM:	ASSY DWG:			SIZE
				CAGE CODE
				DWG NO.
FAB DWG:				REV
PCB DWG:				1.0
SCALE:	FILE NAME			FTDI.SchDoc
				SHEET 1 OF 1

USB Slot + FTDI

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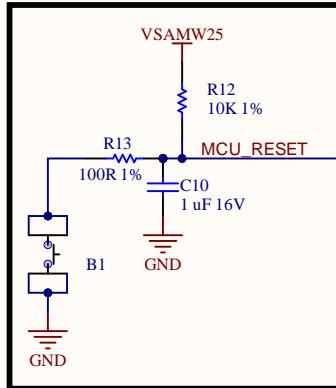
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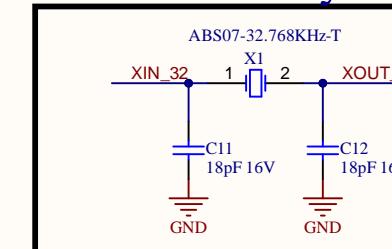
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Reset Button



32.768 Crystal



Calculation of crystal load capacitors:
 $C_{ext} = 2 \times (C_{crystal} - C_{para} - C_{pcb})$
 Ccrystal = 12.5pF (from crystal - Cdatasheet)
 Cpara = 3.15pF (from MCU datasheet)
 Cpcb = 0.5pF (estimate)
 $C_{ext} = 2 \times (12.5pF - 3.15pF - 0.5pF) = 17.7pF$

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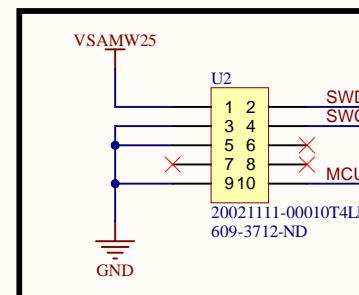
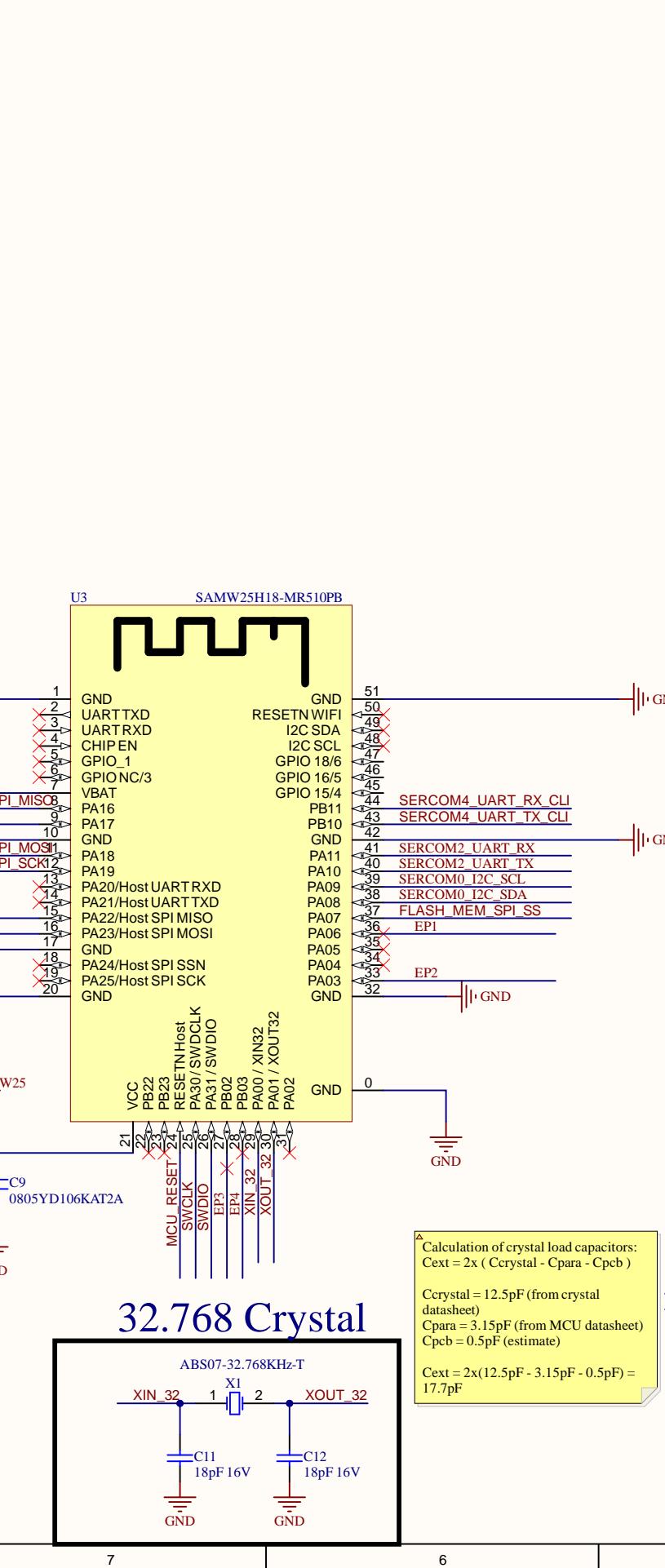
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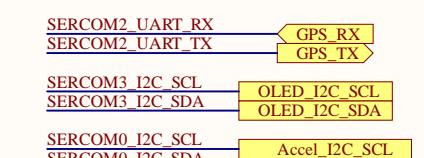
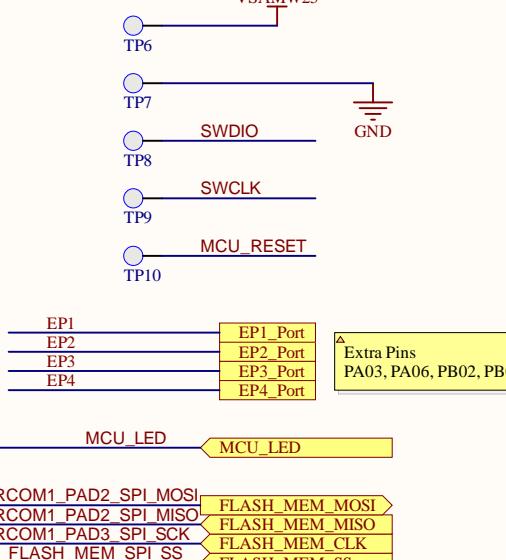
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DEBUGGER PORT



APPROVALS	DATE	PROJECT	Penn Engineering
ENG:	*	DOCUMENT REVISION:	1.0
DSN:	*	DESIGN ITEM:	
CHK:	*	MCU Module	
REFERENCE DOCUMENTS			
BOM:			
ASSY DWG:			
FAB DWG:			
PCB DWG:			
SCALE:	FILE NAME	MCU.SchDoc	SHEET 1 OF 1

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DWG. NO.	1.0.1	REV. SHT.	REVISION	DESCRIPTION	DATE	APPROVED

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TESTPOINTS

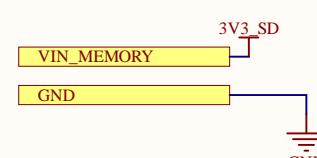
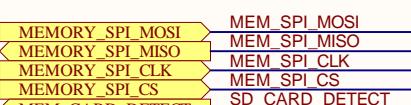
TP11	3V3_SD
TP12	SD_CARD_DETECT
TP13	MEM_SPI_MOSI
TP14	MEM_SPI_MISO
TP15	MEM_SPI_CLK
TP16	MEM_SPI_CS

B

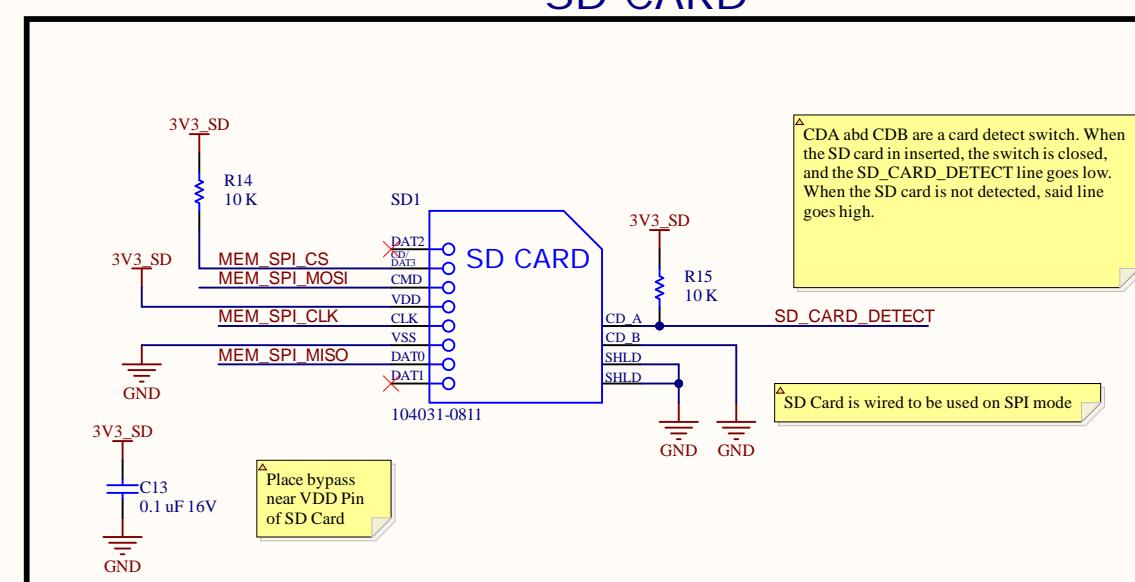
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SD CARD

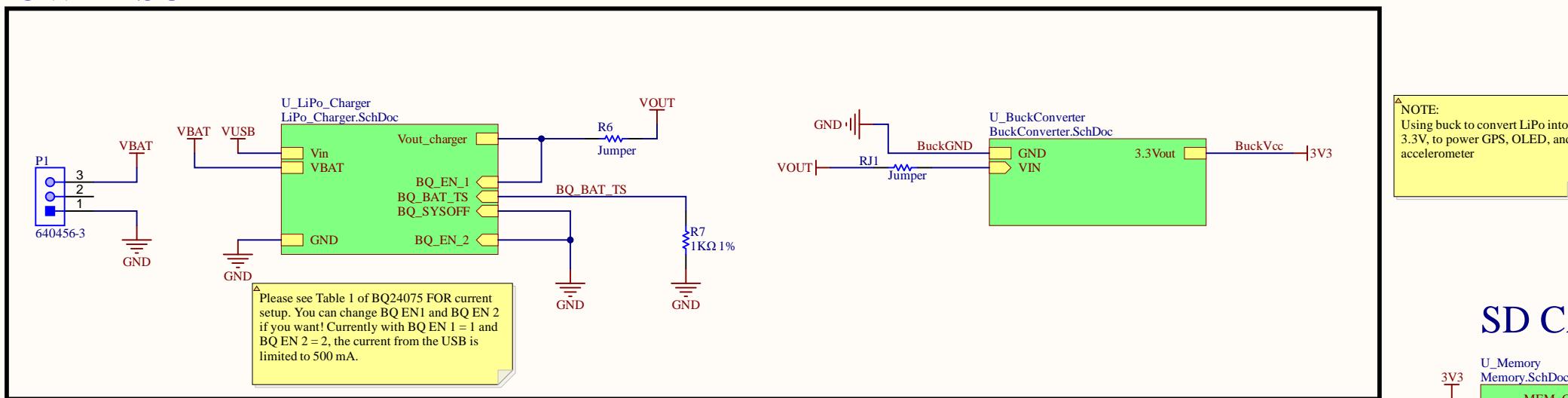


APPROVALS	DATE	PROJECT	Penn Engineering
ENG: Weihsio Huang			UNIVERSITY OF PENNSYLVANIA
DSN: *		PROJECT REVISION:	DOCUMENT REVISION:
CHK: *		DESIGN ITEM:	
REFERENCE DOCUMENTS		TITLE: SD Card Module	
BOM:	ASSY DWG:	SIZE	CAGE CODE
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	FAB DWG:		
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			SHEET 1 OF 1

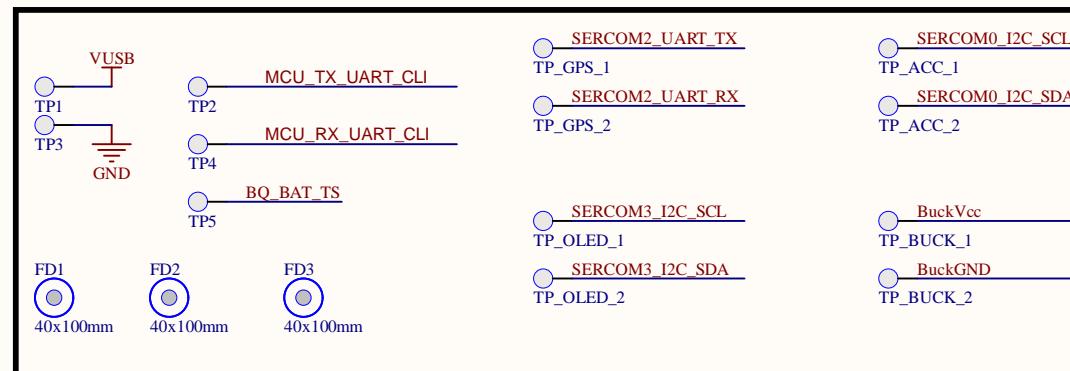
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1.0.1						

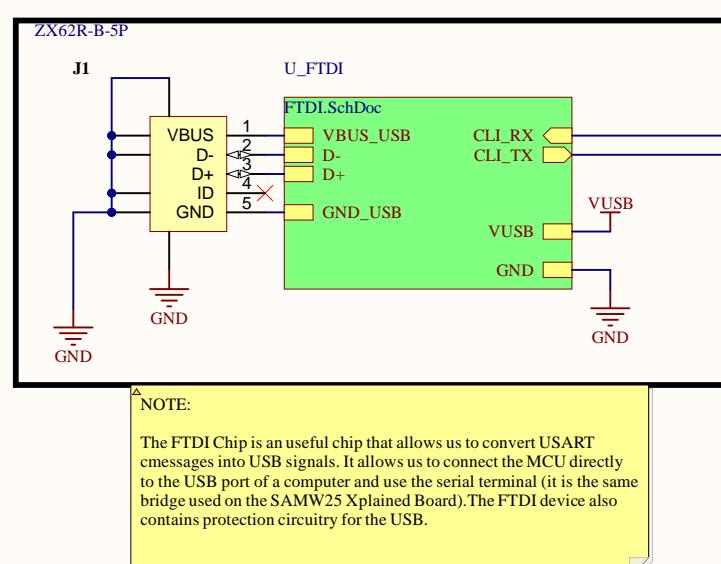
F POWER SUPPLY



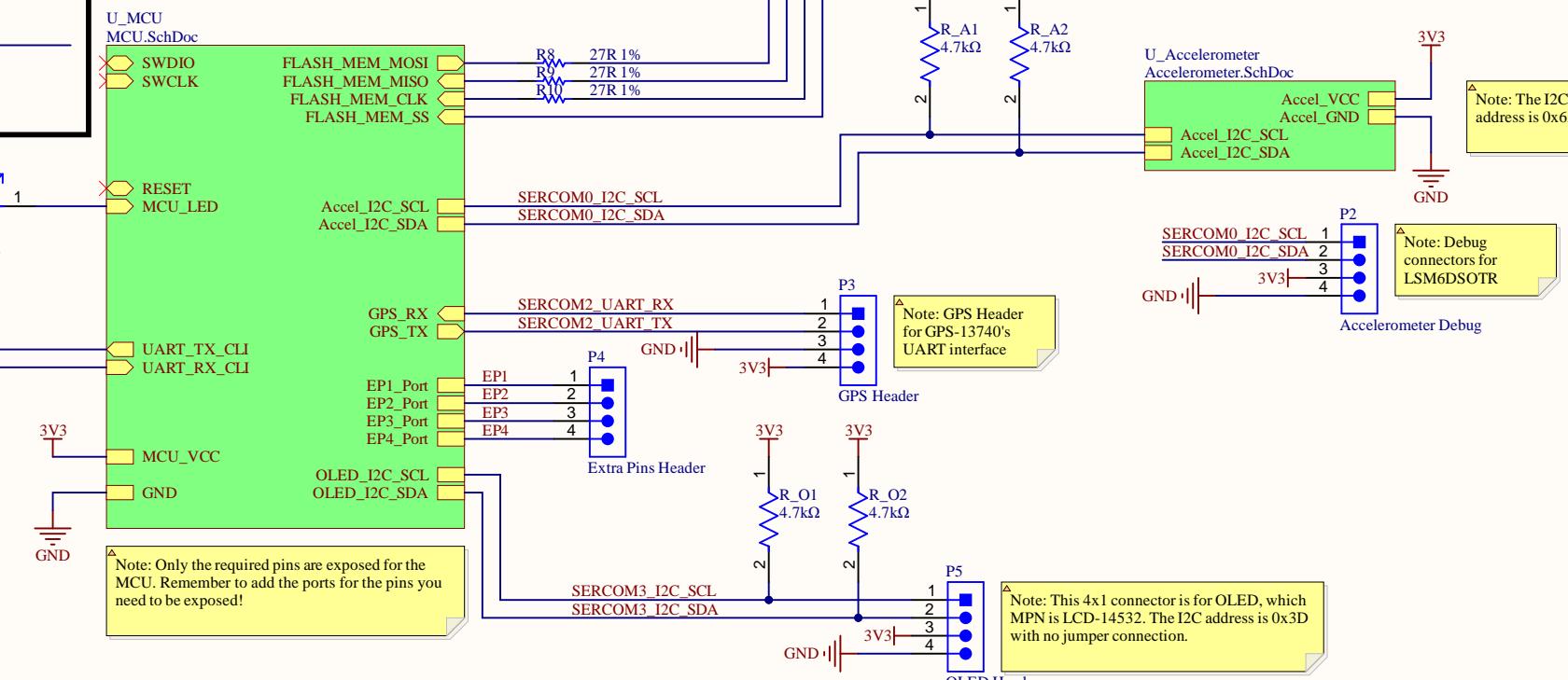
D TEST POINTS AND FIDUCIALS



B USB CONNECTOR + FTDI



C MCU



APPROVALS	DATE	PROJECT	Penn Engineering
ENG:	Weihao Huang		*
DSN:	*		*
CHK:	*		*
REFERENCE DOCUMENTS		DOCUMENT REVISION:	
BOM:		DESIGN ITEM:	Mainboard
ASSY DWG:			
FAB DWG:			
PCB DWG:			
SCALE:	FILE NAME	MAIN.SchDoc	REV. 1.0

IoTracking_Main

Manufacturing Notes

Four (4) Layers

Dimensions: 70mm x 70mm

Thickness: 0.062"

Material: FR4

All layers are unmirrored - should be able to "see straight through"

Scoring: None

Finished Thickness: 0.062 inches

Surface Finish: ENEPIG

Gold Fingers: No

Outer layer finish copper: 1 oz

Number of Holes: 183

Min. Hole Diameter = 0.508mm

Min. Trace (Outer Layer) = 0.006 inches

Min. Distance = 0.006 inches

Solder Mask Color: Red

Soilk Screen Sides: Both

Silk Screen Color: White

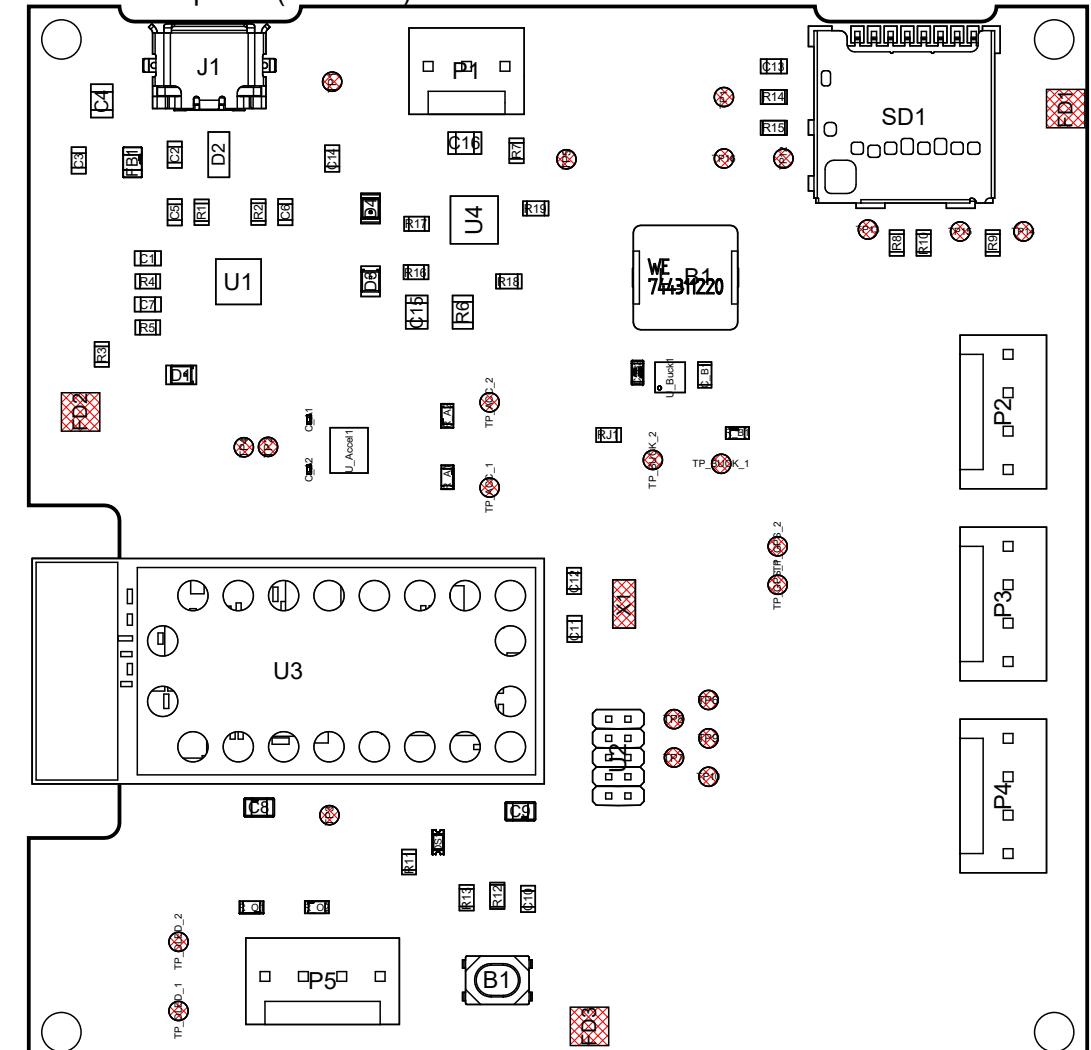
Thickness Tolerance: +/- 10%

Layer Stack Legend

Material	Layer	Thickness	Dielectric Material	Type	Gerber
Surface Material	Top Overlay			Legend	GTO
Copper	Top Solder	0.03mm	Solder Resist	Solder Mask	GTS
Prepreg	Top Layer	0.04mm		Signal	GTL
CF-001	GroundPlane	0.33mm	PP-006	Dielectric	
CF-001	Core	0.02mm		Signal	G1
Core	PowerPlane	0.71mm	Core-009	Dielectric	
CF-001	PowerPlane	0.02mm		Signal	G2
Prepreg	Bottom Solder	0.33mm	PP-006	Dielectric	
Copper	Bottom Layer	0.04mm		Signal	GBL
Surface Material	Bottom Overlay	0.03mm	Solder Resist	Solder Mask	GBS
				Legend	GBO

Total thickness: 1.53mm

View from Top side (Scale 2:1)



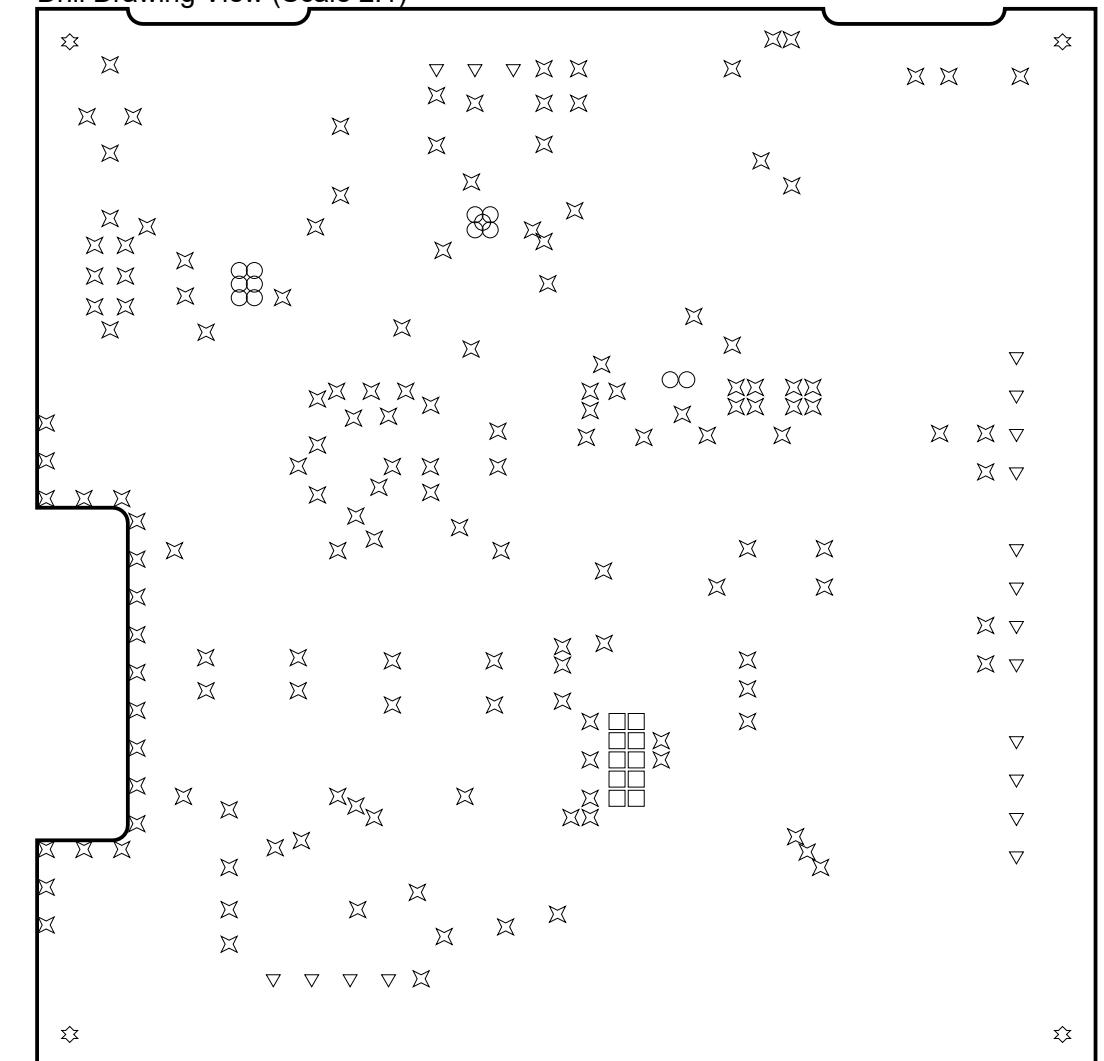
APPROVALS	DATE
ENGINEER: Weihao Huang	2/26/2022
DESIGNER: Weihao Huang	2/26/2022
CHECKER: Weihao Huang	2/26/2022
Reference Documents	
NEXT ASSY USED ON	
APPLICATION	
SIZE: B	DWG NO:
IoTracking Board Fabrication.PCBDw	
SCALE:	FILE NAME:
Sheet: 1 of 12	

Altium

DESIGN ITEM: PCB_Board DESIGN ITEM REVISION: 1.0
TITLE: IoTracking

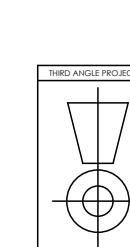
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Drill Drawing View (Scale 2:1)

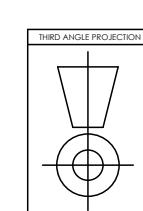
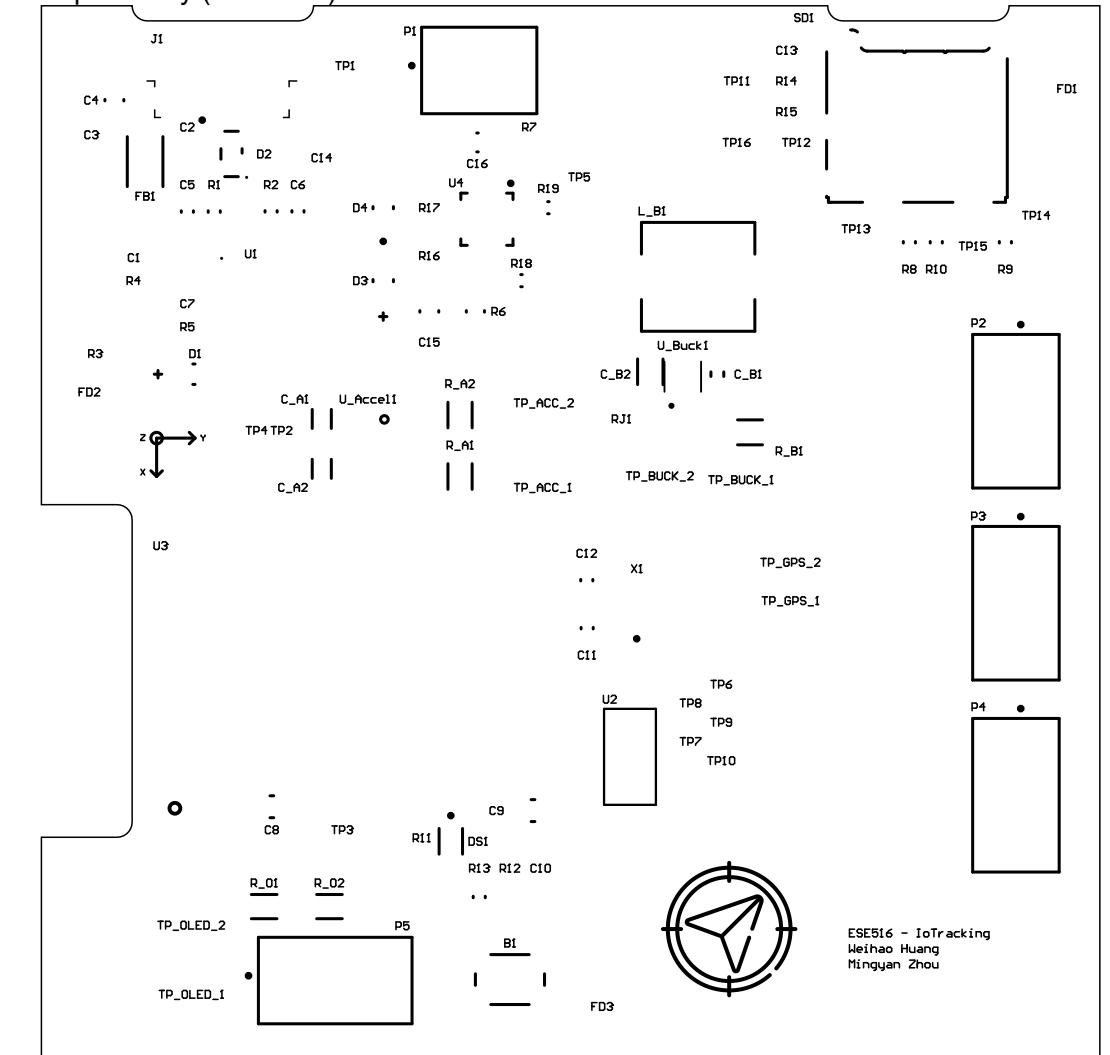


Drill Ta

Symbol	Count	Hole Size	Plated	Hole Tolerance
○	13	0.20mm	Plated	
☒	156	0.20mm	Plated	
□	10	0.65mm	Plated	
▽	19	1.27mm	Plated	
☆	4	2.70mm	Plated	
202 Total				

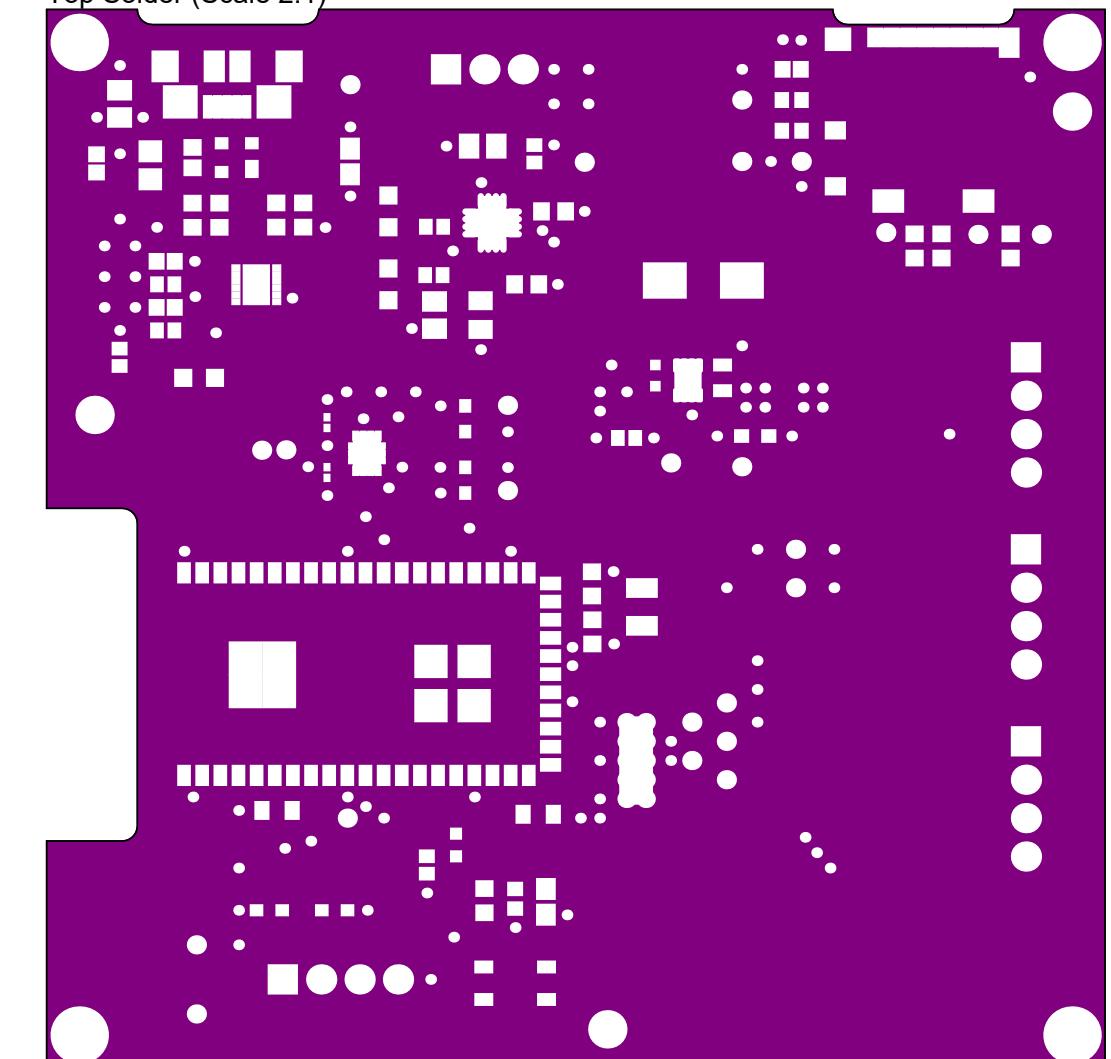


Top Overlay (Scale 2:



APPROVALS	DATE			
ENGINEER:	Weihao Huang			
DESIGNER:	Weihao Huang	2/26/2022		
CHECKER:	Weihao Huang	2/26/2022	DESIGN ITEM:	PCB Board
			DESIGN ITEM REVISION:	1.0
Reference Documents			TITLE: IoTracking	
			SIZE: B	
			DWG NO:	
			REV:	
SCALE:		FILE NAME:		Sheet: 1 OF 10
IoTracking_Board_Fabrication.PCBDw				

Top Solder (Scale 2:1)



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		APPROVALS	DATE
ENGINEER:	Weihao Huang	2/26/2022	
DESIGNER:	Weihao Huang	2/26/2022	
CHECKER:	Weihao Huang	2/26/2022	
Reference Documents			
NEXT ASSY		USED ON	
APPLICATION			

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DESIGN ITEM: PCB_Board DESIGN ITEM REVISION: 1.0

TITLE: IoTTracking

SIZE: B DWG NO: _____ REV: _____

SCALE: FILE NAME: IoTTracking_Board_Fabrication.PCBDw SHEET: 4 OF 12



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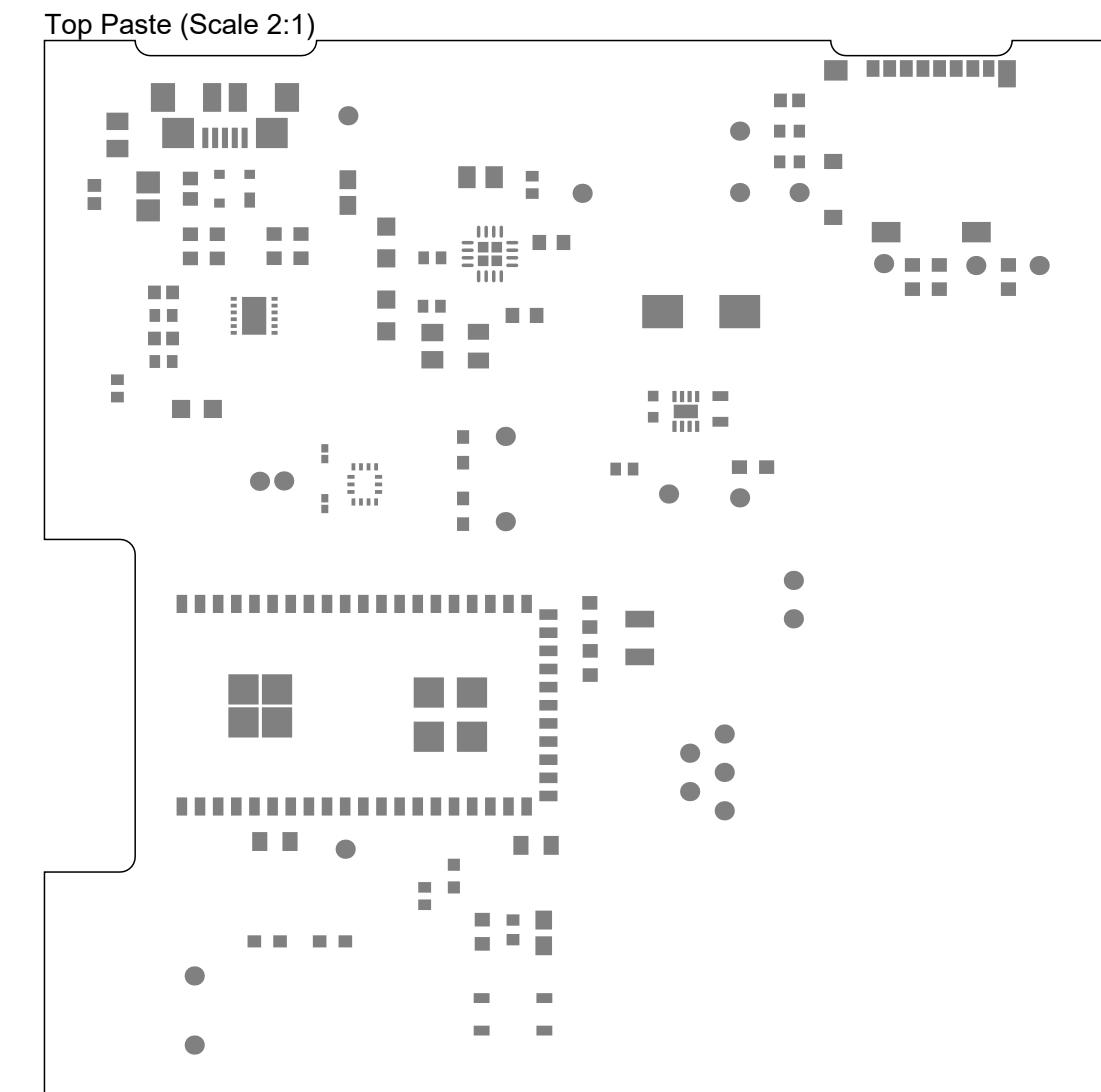
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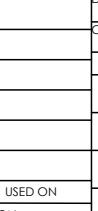
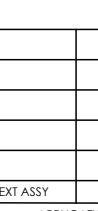
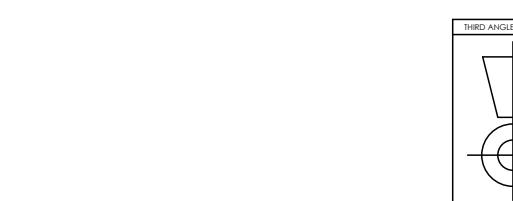
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SHEET									

REVISIONS		DESCRIPTION	DATE	APPROVED

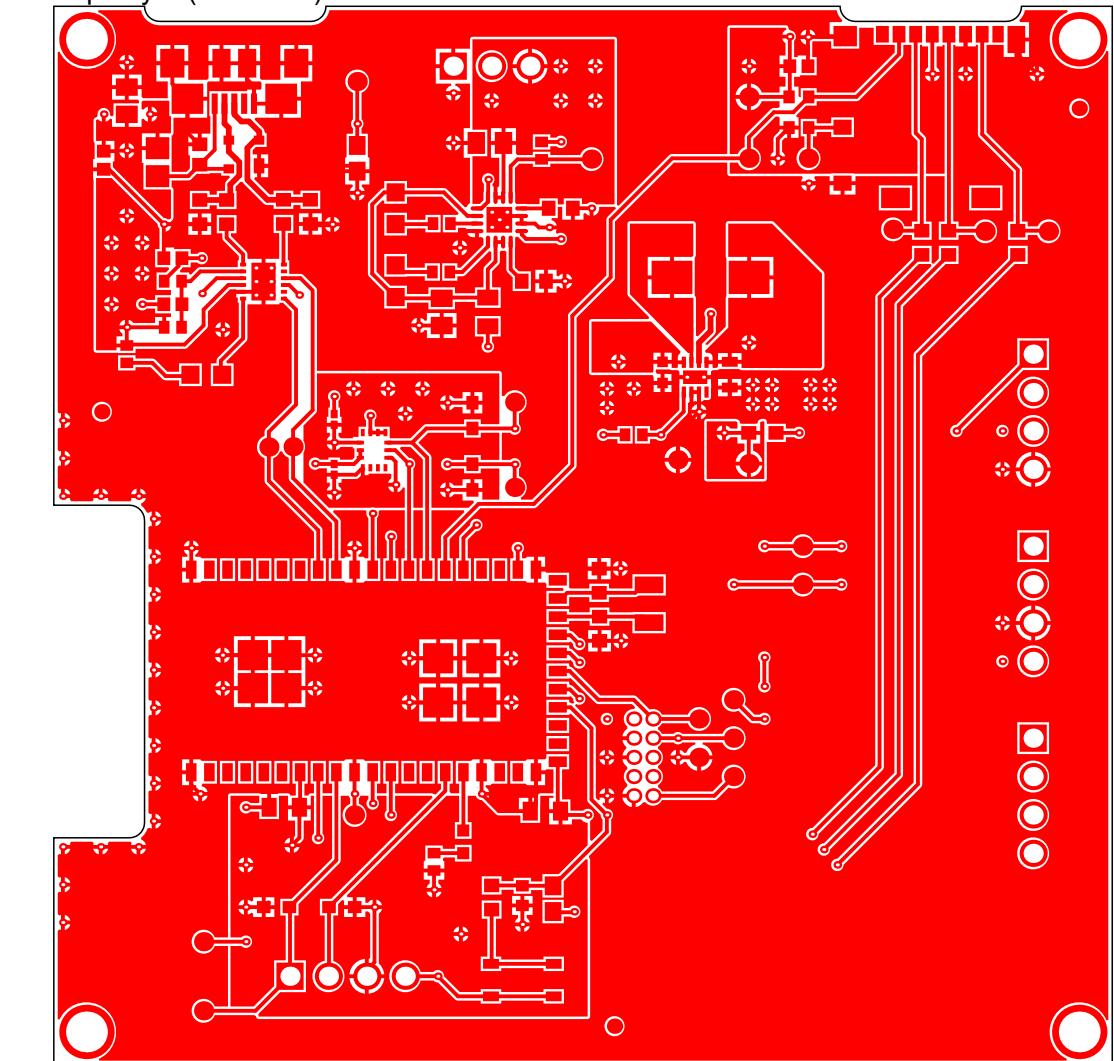


APPROVALS	DATE	Altium TM
ENGINEER: Weihao Huang	2/26/2022	
DESIGNER: Weihao Huang	2/26/2022	
CHECKER: Weihao Huang	2/26/2022	
DESIGN ITEM: PCB_Board	DESIGN ITEM REVISION: 1.0	
TITLE: IoTracking		
SIZE: B	DWG NO:	
REV: .lfe	FILE NAME: IoTracking_Board_Fabrication.PCBDw	
SCALE: 1:1	FILE NAME: IoTracking_Board_Fabrication.PCBDw	
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Sheet: 5 of 12		



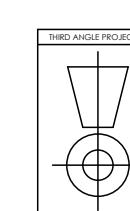
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SHEET								ZONE	REV	

Top Layer (Scale 2:1)



APPROVALS	DATE	DWG NO: =DOC_NO_ASSY_	
ENGINEER:	Weihao Huang	2/26/2022	
DESIGNER:	Weihao Huang	2/26/2022	
CHECKER:	Weihao Huang	2/26/2022	
Reference Documents		DESIGN ITEM: PCB_Board	
		DESIGN ITEM REVISION: 1.0	
TITLE: IoTracking			
SIZE:	B	DWG NO:	
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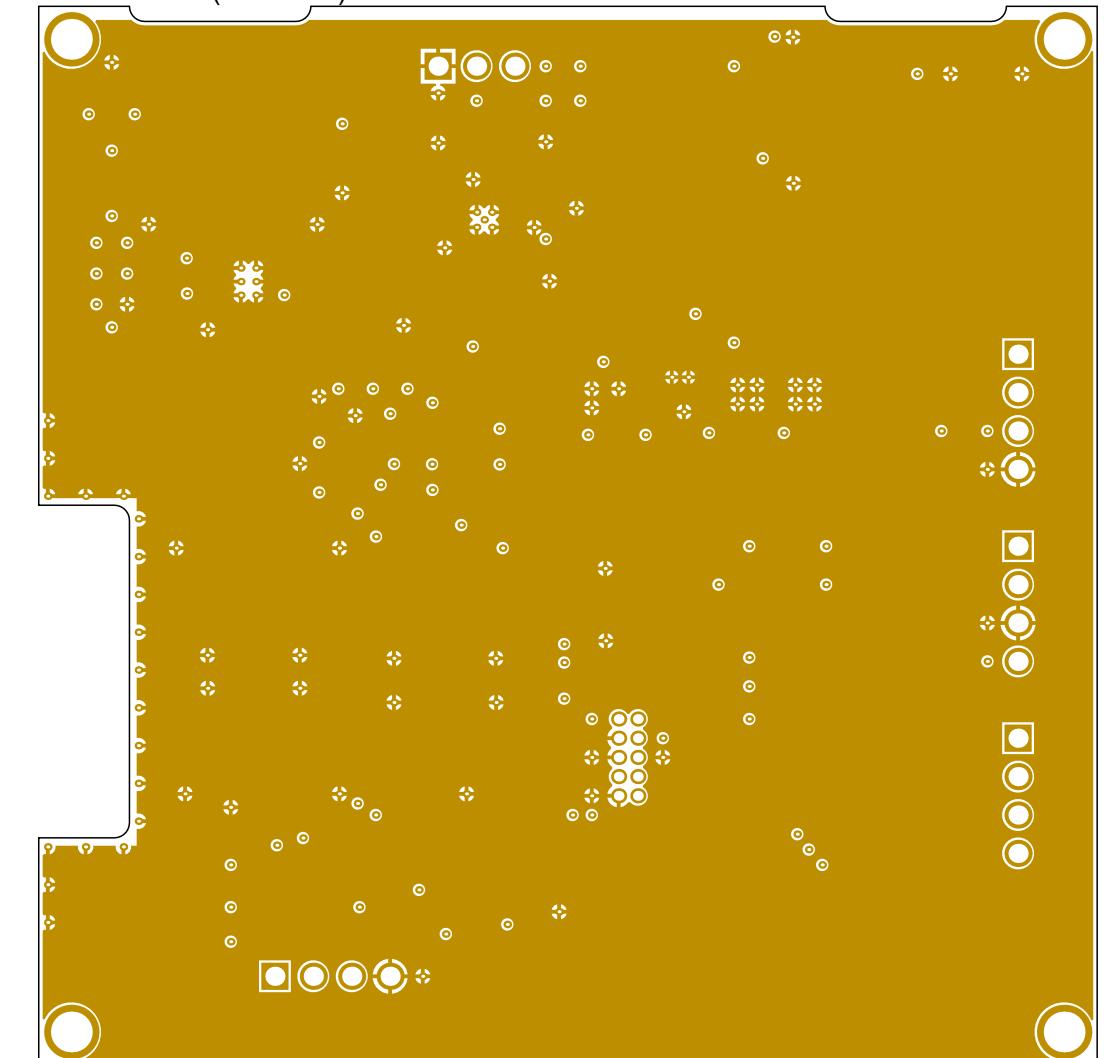
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DWG NO. =DOC_NO_ASSY_DWG	REV. .lfe

REVISIONS		
DESCRIPTION	DATE	APPROVED

GroundPlane (Scale 2:1)



APPROVALS		DATE	DESIGN ITEM: PCB_Board	DESIGN ITEM REVISION: 1.0
ENGINEER:	Weihao Huang	2/26/2022		
DESIGNER:	Weihao Huang	2/26/2022		
CHECKER:	Weihao Huang	2/26/2022		
Reference Documents				TITLE: IoTracking
THIRD ANGLE PROJECTION				SIZE: B
				DWG NO.: IoTracking_Board_Fabrication.PCBDw
				REV.: 7 OF 12
NEXT ASSY	USED ON	APPLICATION	SCALE:	FILE NAME:

AltiumDWG NO.
=DOC_NO_ASSY_.lfe

A

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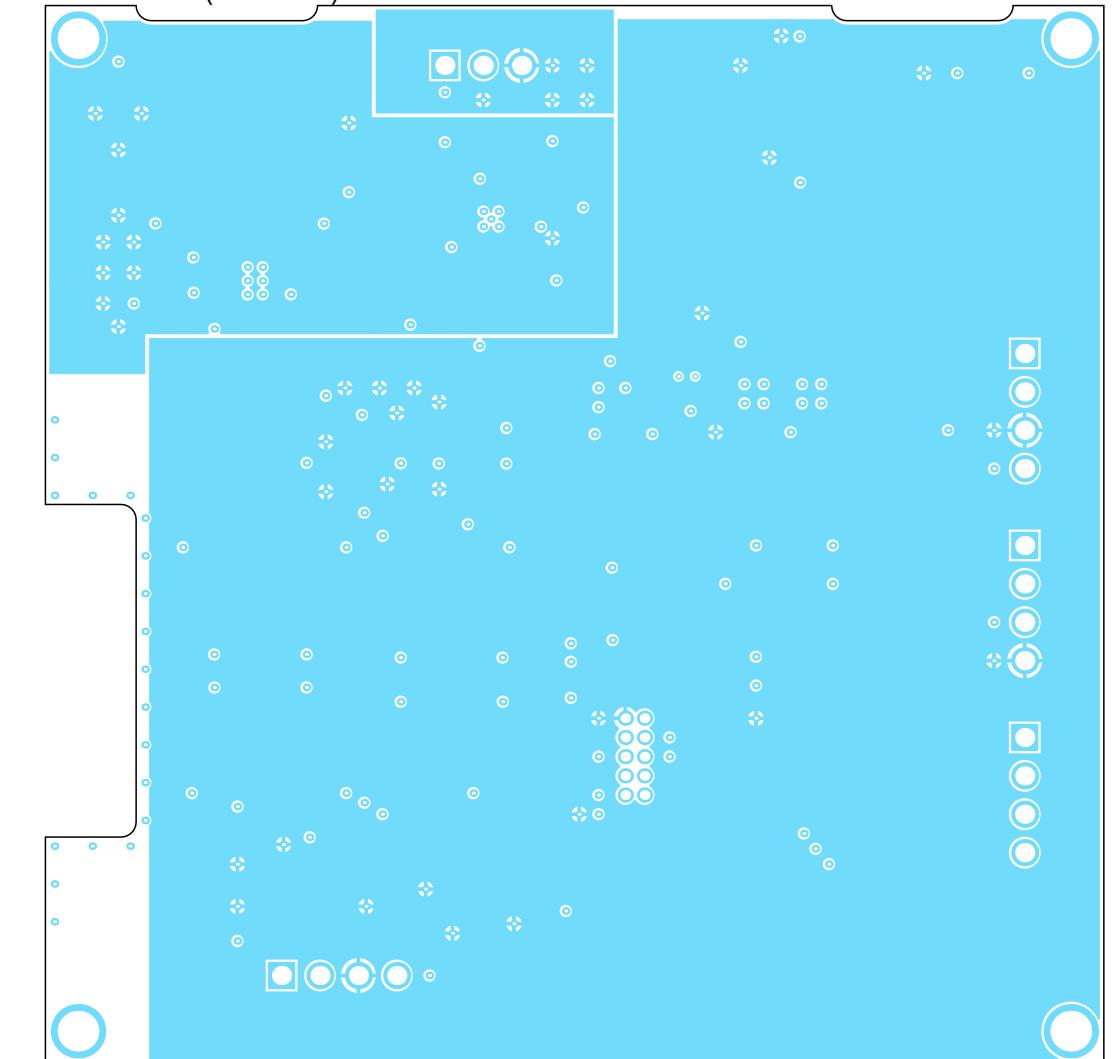
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REV STATUS OF SHEETS		REV									
SHEET											

REVISIONS		REV:									
DESCRIPTION	DATE										

PowerPlane (Scale 2:1)



APPROVALS	DATE	Altium PCB Board IoTracking
ENGINEER: Weihao Huang	2/26/2022	
DESIGNER: Weihao Huang	2/26/2022	
CHECKER: Weihao Huang	2/26/2022	
Reference Documents		
SIZE: B	DWG NO:	
SCALE: 1.0	FILE NAME: IoTracking_Board_Fabrication.PCBDw	REV: 8 OF 12



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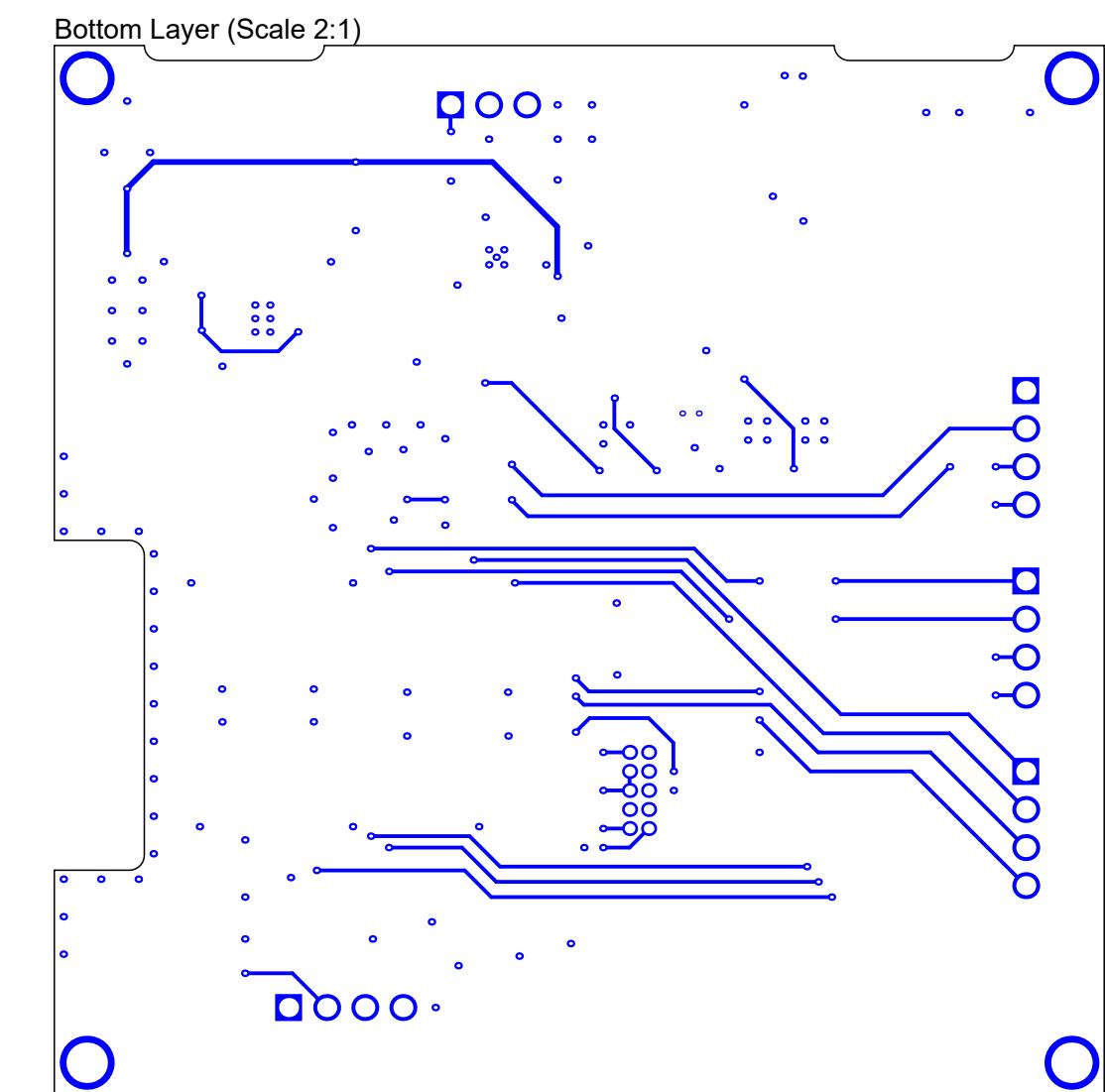
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REV STATUS OF SHEETS		REV					DWG NO. =DOC_NO_ASSY_DWG	REV .lfe
SHEET								

REVISIONS		DESCRIPTION	DATE	APPROVED



APPROVALS	DATE	Altium TM
ENGINEER: Weihao Huang	2/26/2022	
DESIGNER: Weihao Huang	2/26/2022	
CHECKER: Weihao Huang	2/26/2022	
Reference Documents		
DESIGN ITEM: PCB_Board DESIGN ITEM REVISION: 1.0		
TITLE: IoTTracking		
SIZE: B	DWG NO:	
IoTracking_Board_Fabrication.PCBDw		
SCALE: 1:1	FILE NAME: IoTracking_Board_Fabrication.PCBDw	
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THIRD ANGLE PROJECTION

NEXT ASSY USED ON APPLICATION

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FILE NAME: IoTracking_Board_Fabrication.PCBDw

SCALE: 1:1

ZONE REV

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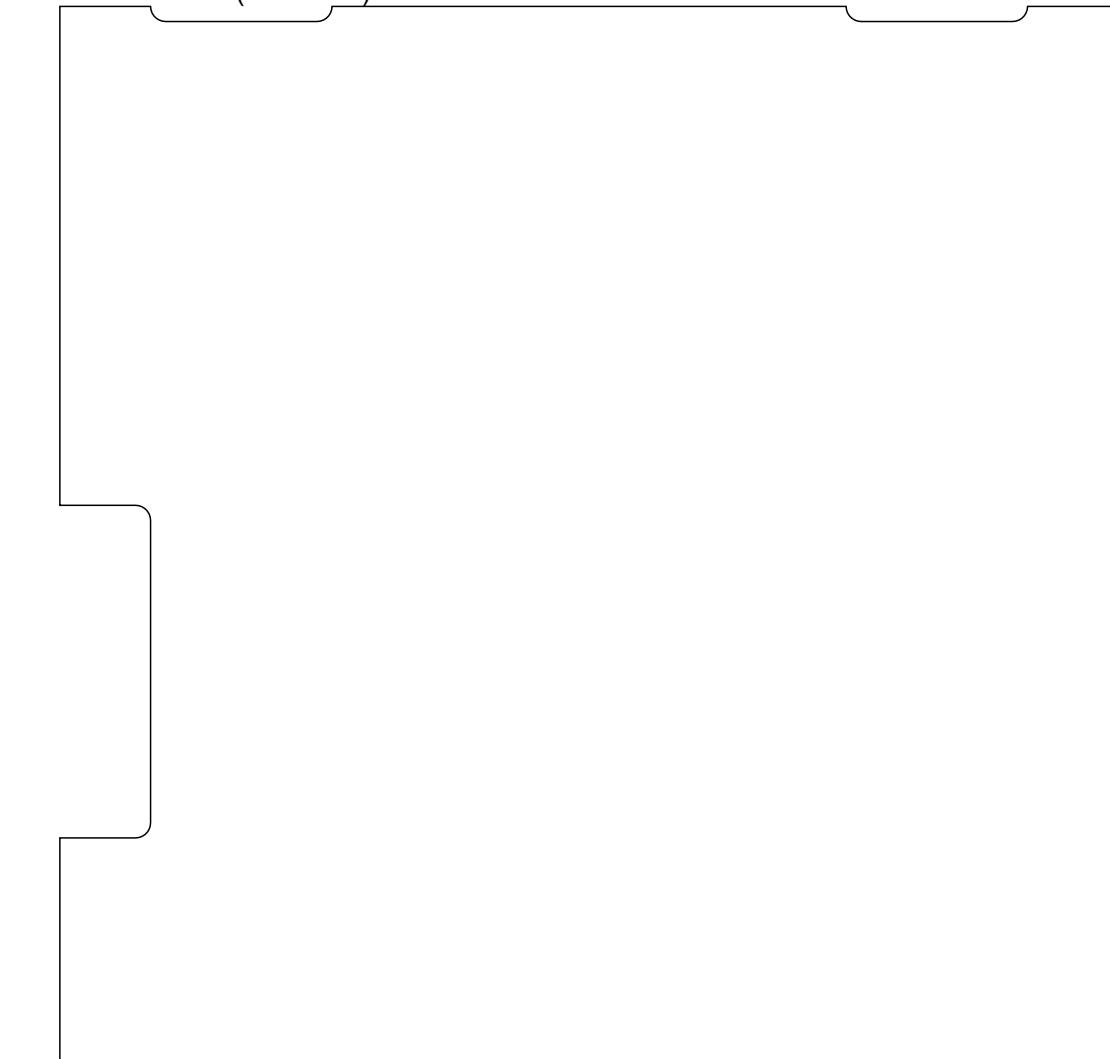
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Bottom Paste (Scale 2:1)



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11 of 11

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REV:

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 	APPROVALS		DATE
	ENGINEER:	Weihao Huang	2/26/2022
	DESIGNER:	Weihao Huang	2/26/2022
	CHECKER:	Weihao Huang	2/26/2022
		Reference Documents	
NEXT ASSY	USED ON		
APPLICATION			

Altium™

DESIGN ITEM: PCB_Board DESIGN ITEM REVISION: 1.0

TITLE: IoTTracking

SIZE: B DWG NO: IoTTracking_Board_Fabrication.PCBDw

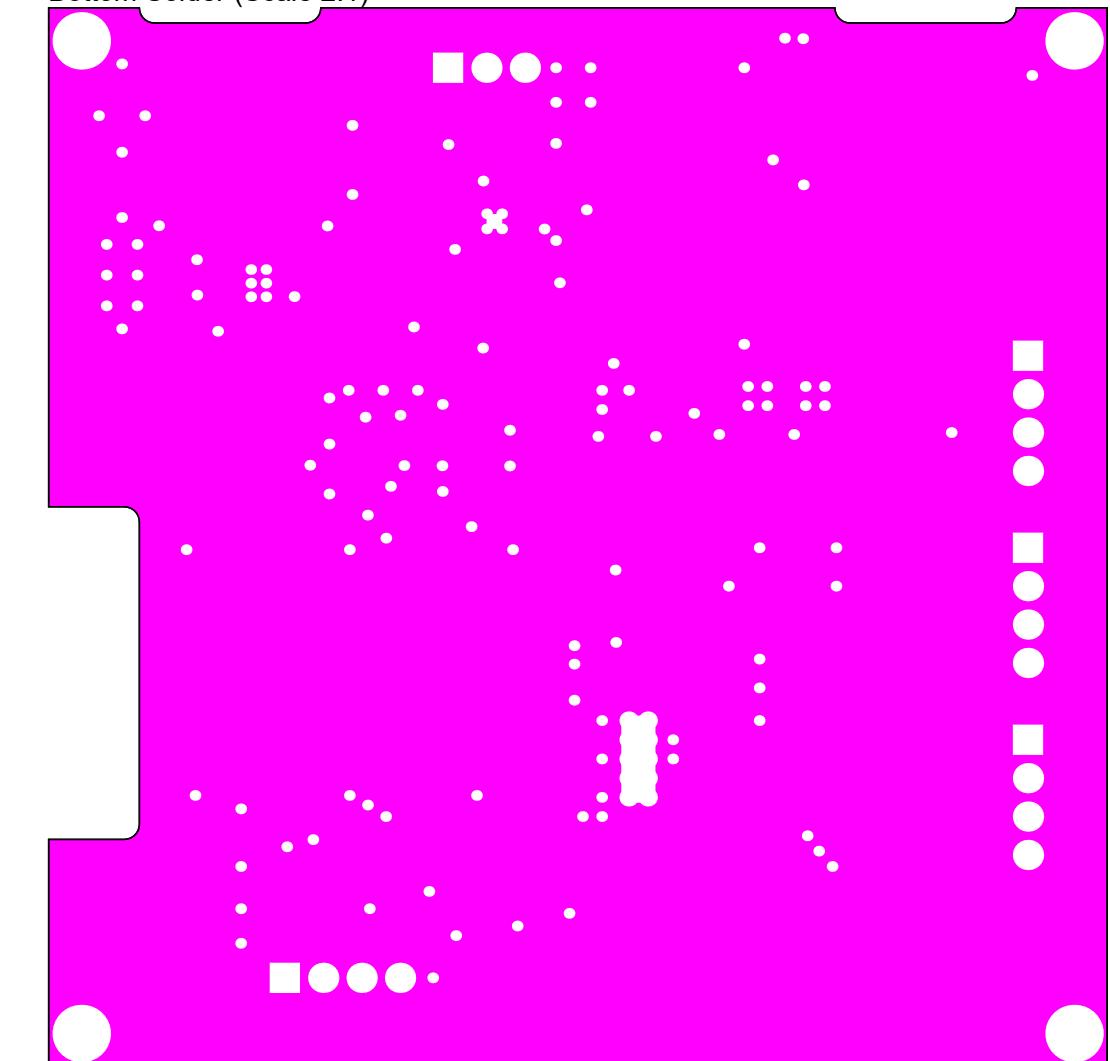
SCALE: FILE NAME: REV: 10 OF 12

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Bottom Solder (Scale 2:1)



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REV:

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APPROVALS	DATE			
ENGINEER:	Weihao Huang	2/26/2022		
DESIGNER:	Weihao Huang	2/26/2022		
CHECKER:	Weihao Huang	2/26/2022		
Reference Documents				
TITLE: IoTracking				
SIZE: B	DWG NO:		REV:	
IoTracking_Board_Fabrication.PCBDw				
SCALE:	FILE NAME:			SHEET: 11 OF 12

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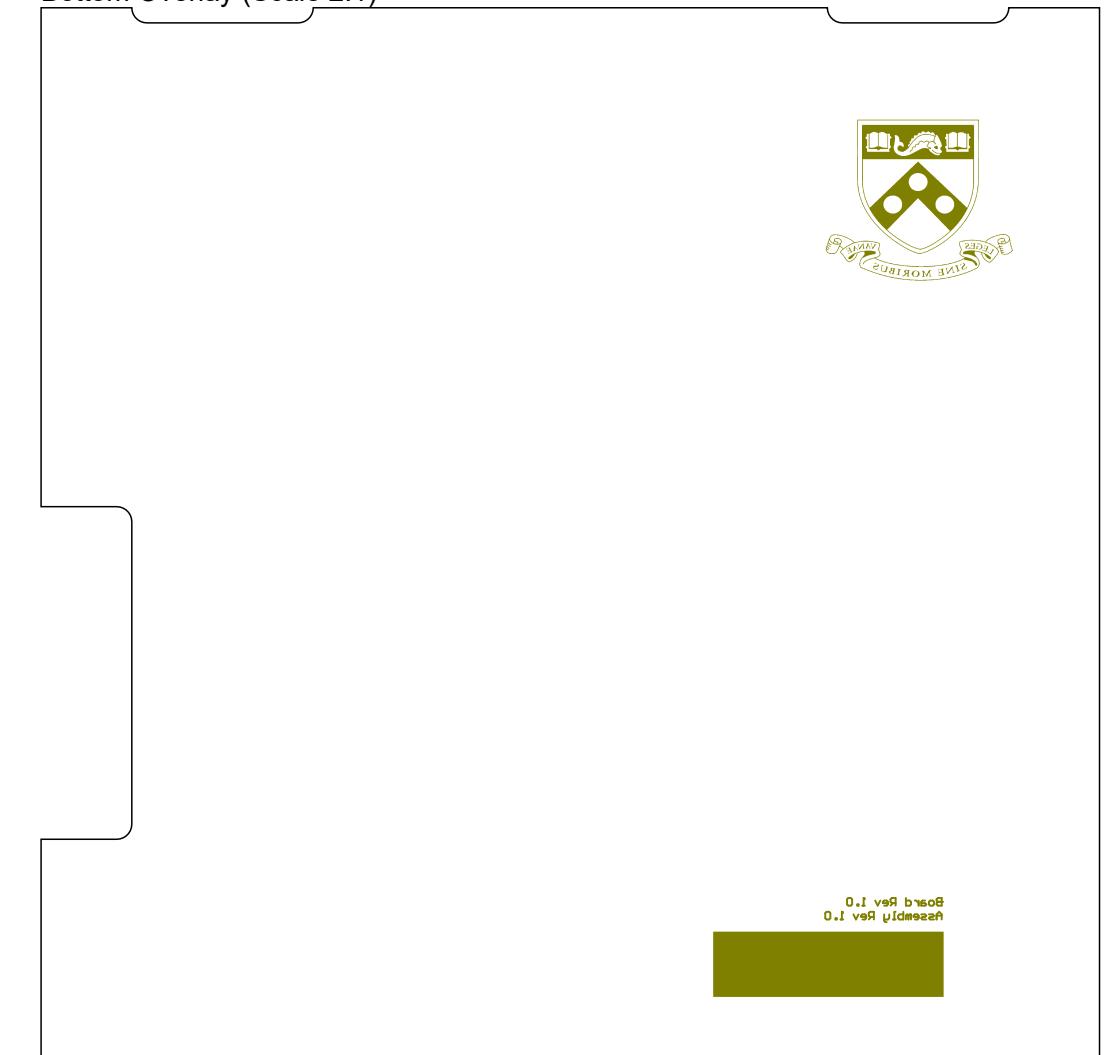
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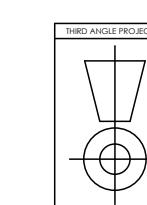
REV STATUS OF SHEETS		REV							DWG NO: =DOC_NO_ASSY_DWG	REV: .lfe
SHEET										

REVISIONS		DESCRIPTION	DATE	APPROVED

Bottom Overlay (Scale 2:1)



APPROVALS	DATE	Altium PCB Board
ENGINEER:	Weihao Huang	
DESIGNER:	Weihao Huang	
CHECKER:	Weihao Huang	
Reference Documents		DESIGN ITEM REVISION: 1.0
SIZE:	B	DESIGN ITEM: PCB_Board
SCALES:		TITLE: IoTracking
FILE NAME:		DWG NO: IoTracking_Board_Fabrication.PCBDw
REV:		Sheet: 12 of 12



NEXT ASSY

USED ON

APPLICATION

USED ON

APPLICATION

REV STATUS OF SHEETS		REV							
SHEET									

REVISIONS		DESCRIPTION	DATE	APPROVED

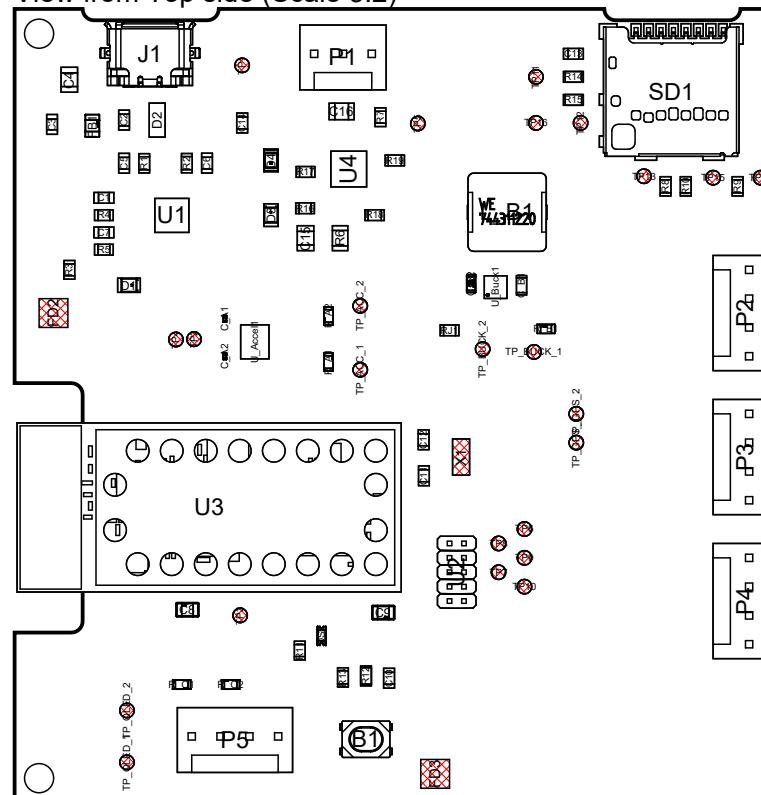
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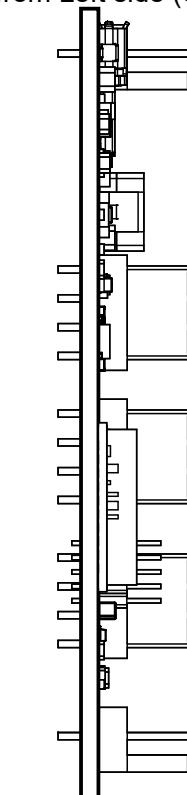
NOTES (unless otherwise specified):

- This item is electrostatic sensitive and shall be handled accordingly

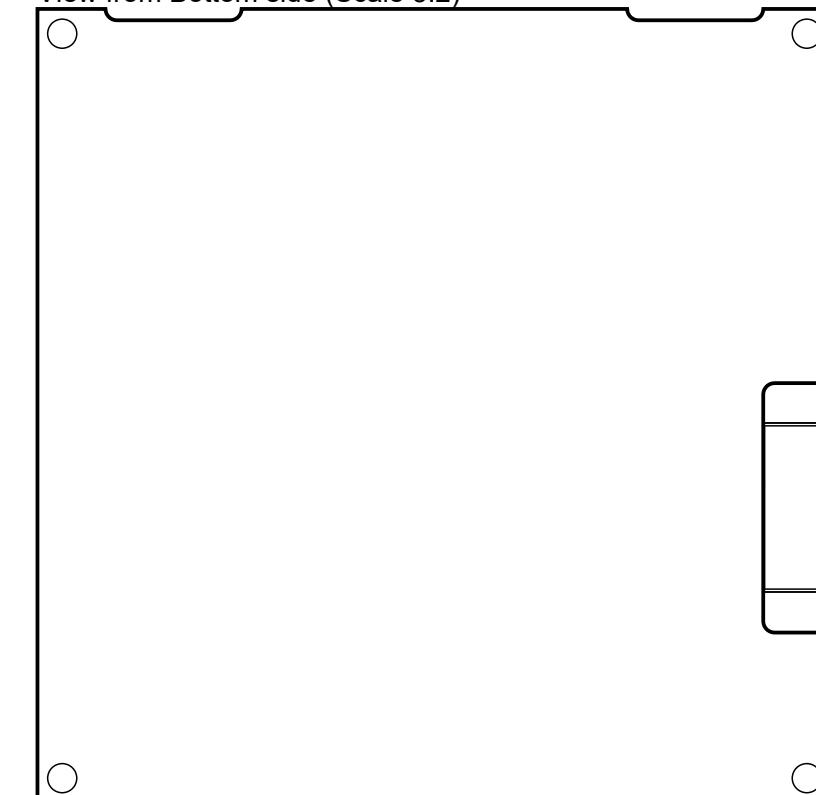
View from Top side (Scale 3:2)



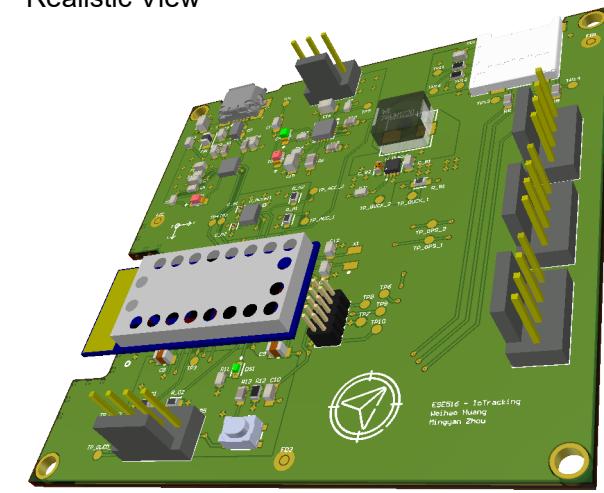
View from Left side (Scale 3:2)



View from Bottom side (Scale 3:2)



Realistic View



2

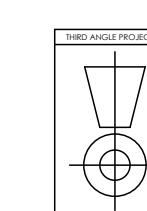
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3

3

4

4



APPROVALS		DATE	DESIGN ITEM: PCB Board Assembly TITLE: IoTracking SIZE: B SCALE: FILE NAME: IoTracking_Board_Assembly.PCBDwf
ENGINEER:	Weihao Huang	2/26/2022	
DESIGNER:	Weihao Huang	2/26/2022	
CHECKER:	Weihao Huang	2/26/2022	
Reference Documents			
NEXT ASSY		USED ON	
APPLICATION			
DWG NO:			REV:

Altium

TM

1.0

IoTracking

DOC_NO_ASSY_DWG.lte

1

OF

4

A

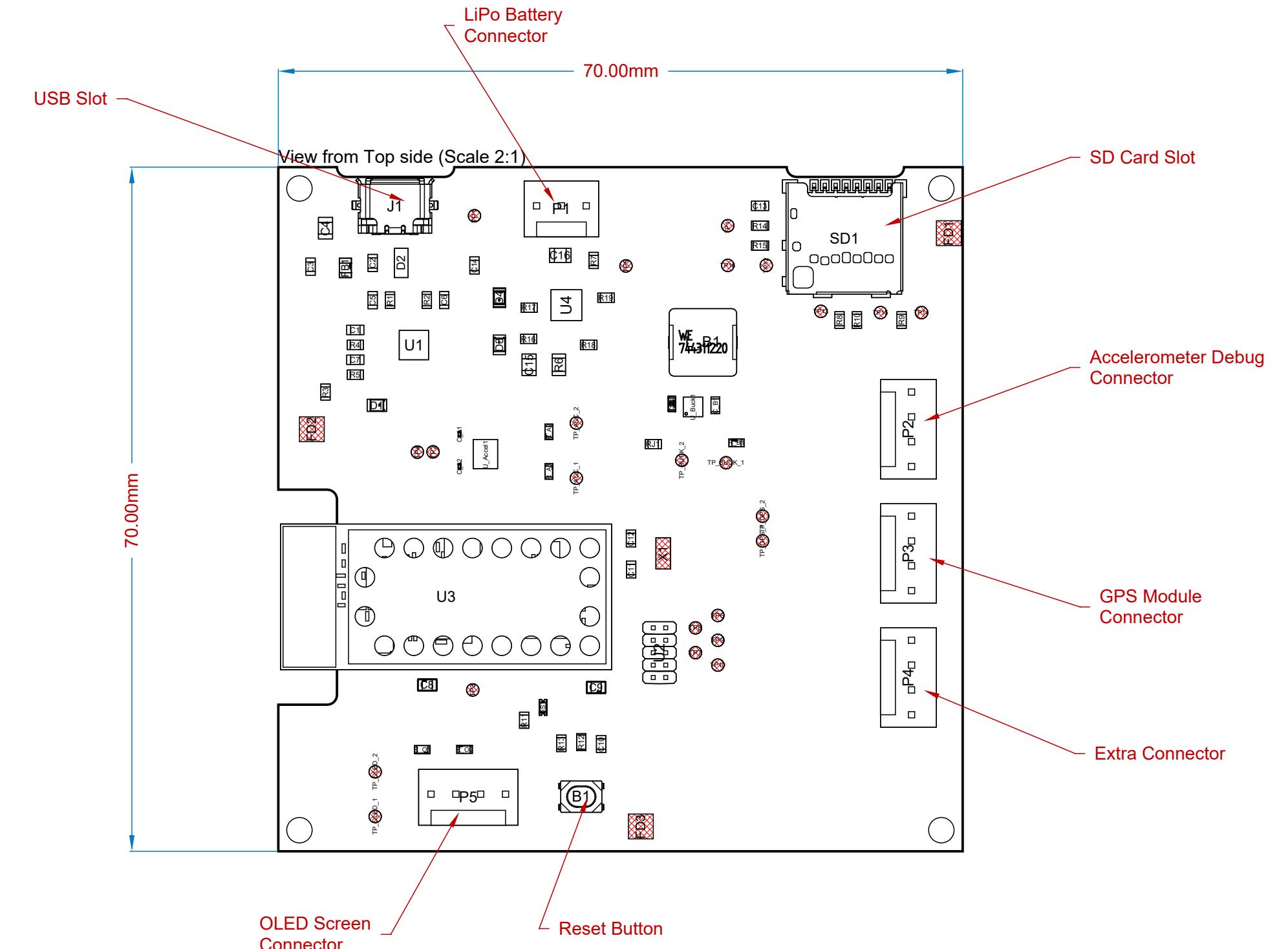
B

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A

B

C

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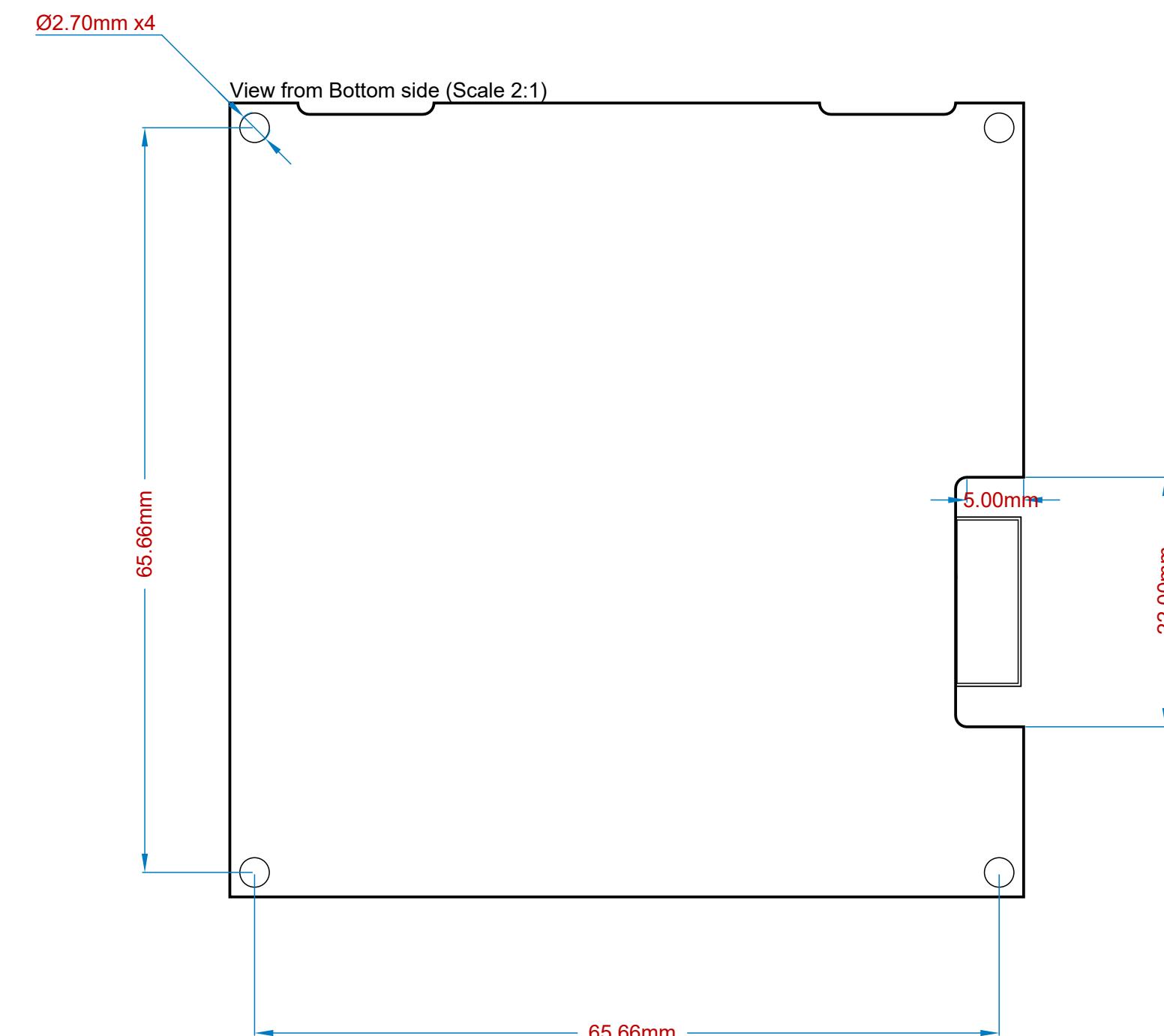
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REV STATUS OF SHEETS		REV							DWG NO: =DOC_NO_ASSY_DWG	REV: .lfe
SHEET										

REVISIONS		DESCRIPTION	DATE	APPROVED



APPROVALS	DATE	Altium PCB Board Assembly 1.0
ENGINEER: Weihao Huang	2/26/2022	
DESIGNER: Weihao Huang	2/26/2022	
CHECKER: Weihao Huang	2/26/2022	
Reference Documents		IoTracking
NEXT ASSY	USED ON	SIZE: B DWG NO:
APPLICATION		REV: .lfe
SCALE:	FILE NAME: IoTracking_Board_Assembly.PCBDwf	3 OF 4

Bill Of Materials

Line #	Designator	Name	Quantity
	U_Accel1	6 DoF Accelerometer	1
	GPS_Module1	GPS 13740	1
27	U1	FT234XD-R	1
36	U3	SAMW25H18-MR510PB	1
28	R4, RJ1	CRCW06030000Z0EC	2
	C_A1, C_A2	GRM033C80J104ME15D	2
6	R12, R14, R15	ERJ3EKF1002V	3
3	R3, R5, R7, R11, R16, R17	CRCW06031K00FKEB	6
11	R1, R2, R8, R9, R10	27R 1% 0603(1608)	5
16	C1, C3, C7, C13	VJ0603Y104KXJCW1BC	4
	R_A1, R_A2, R_O1, R_O2	AT0603DRD074K7L	4
	R_B1	CPF0603B180KE	1
2	R18, R19	1K13 1% 0603(1608)	2
7	C2	C0603C103K4RACTU	1
17	R13	100R 1% 0603(1608)	1
24	FB1	BLM21PG221SN1D	1
29	R6	Jumper 0805(2012)	1
20	P1	640456-3	1
	P2, P3, P4, P5	640456-4	4
4	C10, C14	0603YC105JAT2A	2
5	C4, C15, C16	CAP 4.7uF 16V 0805(2012)	3
9	C11, C12	CAP 18pF 16V 0603(1608)	2
14	C5, C6	CAP 47pF 16V 0603(1608)	2
32	DS1	LTST-C191KGKT	1
31	D4	LTST-C170GKT	1
35	B1	PTS810 SJK 250 SMTR LFS	1
34	D2	PRTR5V0U2X,215	1
30	D1, D3	LTST-C170CKT	2
	C_B2	C1608X5R1C106M080AB	1
21	U2	20021111-00010T4LF	1
39	J1	ZX62R-B-5P	1
8	C8, C9	0805YD106KAT2A	2
	U_Buck1	TPS62082DSGR	1
19	SD1	104031-0811	1
25	U4	BQ24075RGTRG4	1
	L_B1	744311100	1
	LCD1	OLED LCD Screen	1
	Battery1	LiPo Battery	1
	C_B1	C1608X5R0J226M080AC	1

REV STATUS OF SHEETS		REV	DWG NO. =DOC_NO_ASSY_DWG		REV	REVISIONS				
SHEET						ZONE	REV	DESCRIPTION	DATE	APPROVED

APPROVALS		DATE	
ENGINEER:	Weihao Huang	2/26/2022	
DESIGNER:	Weihao Huang	2/26/2022	
CHECKER:	Weihao Huang	2/26/2022	
Reference Documents		DESIGN ITEM: PCB_Board Assembly DESIGN ITEM REVISION: 1.0	
NEXT ASSY		USED ON	TITLE: IoTracking
APPLICATION			SIZE: B DWG NO:
SCALE:	FILE NAME: IoTracking_Board_Assembly.PCBDwf	REV:	4 OF 4